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SBOS268C – DECEMBER 2002 – DECEMBER 2008

Wideband, Low Distortion, Medium Gain, Voltage-Feedback OPERATIONAL AMPLIFIER

FEATURES

- HIGH BANDWIDTH: 260MHz (G = +5)
- GAIN BANDWIDTH PRODUCT: 800MHz
- LOW INPUT VOLTAGE NOISE: 2.0nV/$\sqrt{Hz}$
- VERY LOW DISTORTION: –96dBc (5MHz)
- HIGH OPEN-LOOP GAIN: 110dB
- FAST 12-BIT SETTLING: 10.5ns (0.01%)
- LOW INPUT OFFSET VOLTAGE: 300μV
- OUTPUT CURRENT: ±100mA

APPLICATIONS

- ADC/DAC BUFFER AMPLIFIER
- LOW DISTORTION “IF” AMPLIFIER
- ACTIVE FILTERS
- LOW-NOISE RECEIVER
- WIDEBAND TRANSIMPEDANCE
- TEST INSTRUMENTATION
- PROFESSIONAL AUDIO
- OPA643 UPGRADE

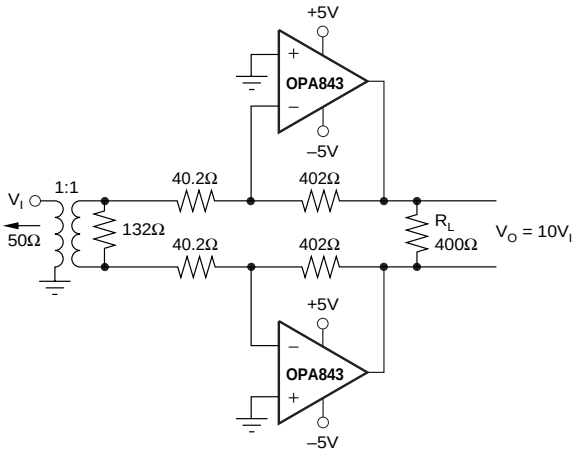
DESCRIPTION

The OPA843 provides a level of speed and dynamic range previously unattainable in a monolithic op amp. Using a high Gain Bandwidth (GBW), two gain-stage design, the OPA843 gives a medium gain range device with exceptional dynamic range. The “classic” differential input complements this high dynamic range with DC precision beyond most high-speed amplifier products. Very low input offset voltage and current, high Common-Mode Rejection Ratio (CMRR) and Power-Supply Rejection Ratio (PSRR), and high open-loop gain combine to give a high DC precision amplifier along with low noise and high 3rd-order intercept.

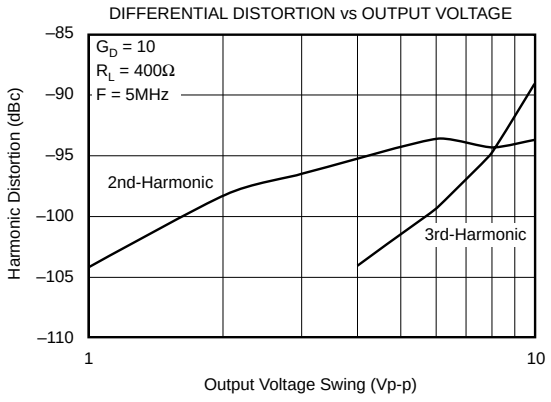
12- to 16-bit converter interfaces will benefit from this combination of features. High-speed transimpedance applications can be implemented with exceptional DC precision as well. Differential configurations using two OPA843s can deliver very low distortion to high output voltages, as shown below.

OPA843 RELATED PRODUCTS

SINGLES	INPUT NOISE VOLTAGE (nV/$\sqrt{Hz}$)	GAIN-BANDWIDTH PRODUCT (MHz)
OPA842	2.6	200
OPA846	1.2	1750
OPA847	0.85	3900



Very Low Distortion Differential Driver



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5 V_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Voltage Range: D, DBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Charge Device Model)	1500V
(Machine Model)	200V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

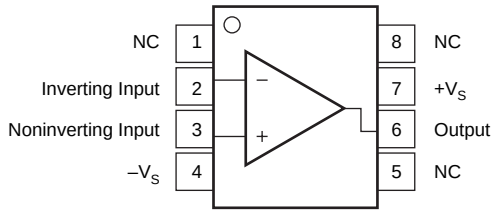
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA843	SO-8	D	–40°C to +85°C	OPA843	OPA843ID	Rails, 100
"	"	"	"	"	OPA843IDR	Tape and Reel, 2500
OPA843	SOT23-5	DBV	–40°C to +85°C	OARI	OPA843IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA843IDBVR	Tape and Reel, 3000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

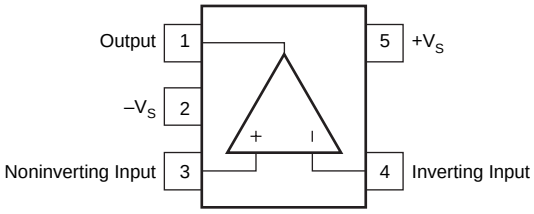
PIN CONFIGURATIONS

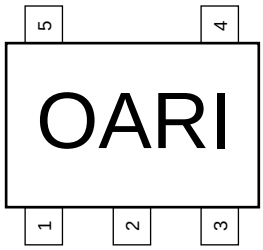
Top View **SO**



NC = No Connection

Top View **SOT**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

At T_A = +25°C, V_S = ±5V, R_F = 402Ω, R_L = 100Ω, and G = +5, unless otherwise noted. See Figure 1 for AC performance.

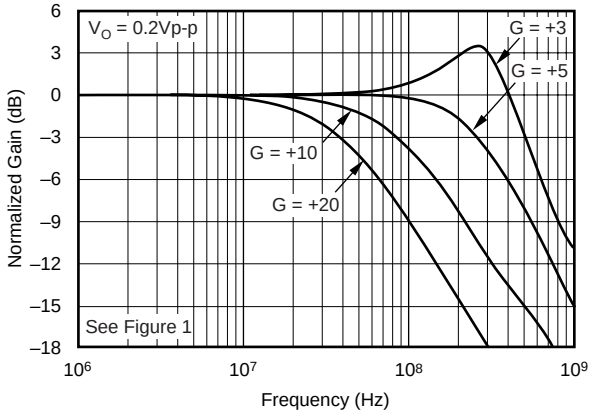
PARAMETER	CONDITIONS	OPA843ID, OPA843IDBV						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C	–40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 200mV_{PP})	G = +3	500				MHz	typ	C
	G = +5	260	185	180	175	MHz	min	B
	G = +10	85	66	65	64	MHz	min	B
	G = +20	40	30	30	30	MHz	min	B
Gain-Bandwidth Product		800	562	560	558	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +5, R_L = 100Ω, V_O = 200mV_{PP}	65	34	33	32	MHz	min	B
Peaking at a Gain of +3		3.5				dB	typ	C
Harmonic Distortion	G = +5, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–76	–74	–72	–70	dBc	max	B
	R_L = 500Ω	–96	–94	–92	–90	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–102	–100	–98	–95	dBc	max	B
	R_L = 500Ω	–110	–105	–102	–100	dBc	max	B
2-Tone, 3rd-Order Intercept	G = +5, f = 25MHz	40				dBm	typ	C
Input Voltage Noise	f > 1MHz	2.0	2.2	2.31	2.36	nV/$\sqrt{Hz}$	max	B
Input Current Noise	f > 1MHz	2.8	3.35	3.4	3.45	pA/$\sqrt{Hz}$	max	B
Rise-and-Fall Time	0.2V Step	1.2	1.95	2.0	2.1	ns	max	B
Slew Rate	2V Step	1000	650	600	525	V/µs	min	B
Settling Time to 0.01%	2V Step	10.5				ns	typ	C
0.1%	2V Step	7.5	10	10.3	10.6	ns	max	B
1.0%	2V Step	3.2	5.4	5.8	6.4	ns	max	B
Differential Gain	G = +4, NTSC, R_L = 150Ω	0.001				%	typ	C
Differential Phase	G = +4, NTSC, R_L = 150Ω	0.012				deg	typ	C
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V	110	**100**	96	92	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.30	**±1.20**	±1.4	±1.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±4	±4	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	–20	**–35**	–36	–37	µA	max	A
Input Bias Current Drift	V_{CM} = 0V			25	25	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.25	**±1.0**	±1.15	±1.17	µA	max	A
Input Offset Current Drift	V_{CM} = 0V			±2	±2	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)(5)		±3.2	**±3.0**	±2.9	±2.8	V	min	A
Common-Mode Rejection (CMRR)	V_{CM} = ±1V, Input Referred	95	**85**	84	82	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0V	12 || 1				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	3.2 || 1.2				MΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	R_L > 1kΩ, Positive Output	3.2	**3.0**	2.9	2.8	V	min	A
	R_L > 1kΩ, Negative Output	–3.7	**–3.5**	–3.4	–3.3	V	min	A
	R_L = 100Ω, Positive Output	3.0	**2.8**	2.7	2.6	V	min	A
	R_L = 100Ω, Negative Output	–3.5	**–3.3**	–3.2	–3.1	V	min	A
Current Output	V_O = 0V	±100	**±90**	±85	±80	mA	min	A
Closed-Loop Output Impedance	G = +5, f = 1kHz	0.0001				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Minimum Operating Voltage			**±4**	±4	±4	V	min	A
Max Quiescent Current	V_S = ±5V	20.2	**20.8**	22.2	22.5	mA	max	A
Min Quiescent Current	V_S = ±5V	20.2	**19.6**	19.1	18.3	mA	min	A
Power-Supply Rejection Ratio (+PSRR, –PSRR)	$\|V_S\|$ = 4.5V to 5.5V, Input Referred	100	**90**	88	85	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C	typ	C
DBV SOT23-5		150				°C	typ	C

NOTES: (1) Junction temperature = ambient temperature for 25°C min/max specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature min/max specifications. (3) Test Levels: (A) 100% tested at 25°C over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

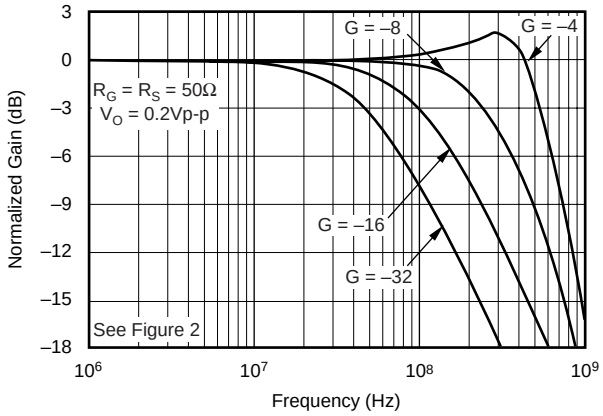
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

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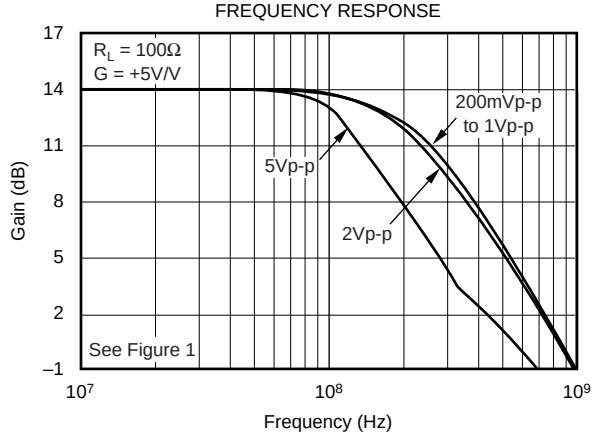
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



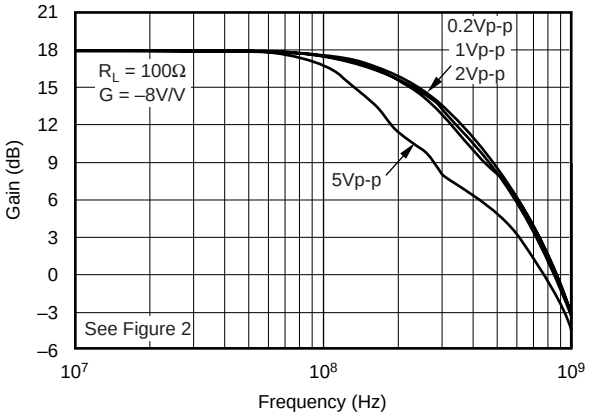
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



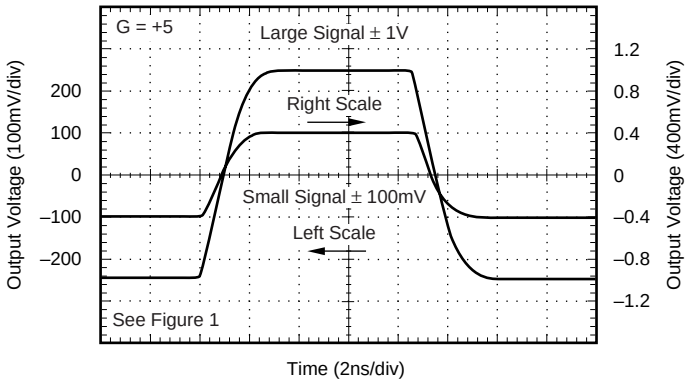
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



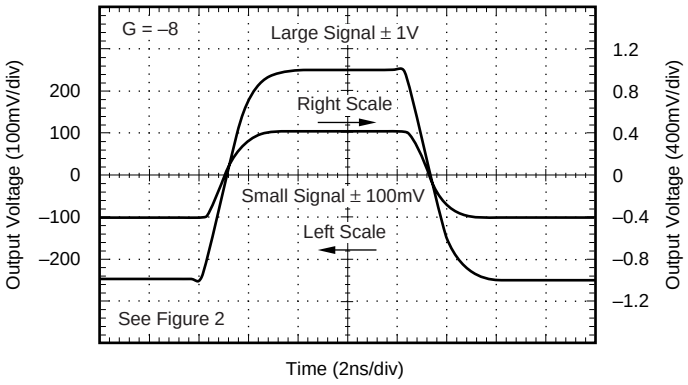
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



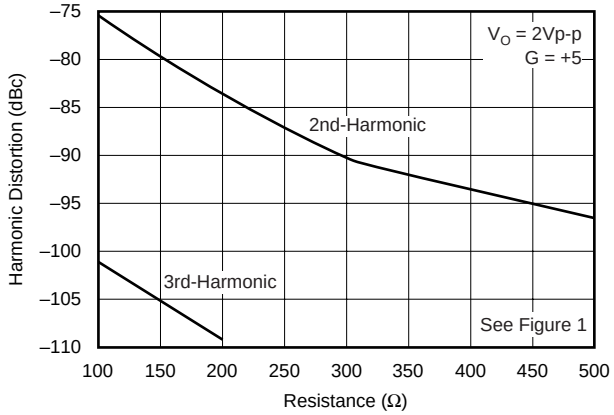
INVERTING PULSE RESPONSE



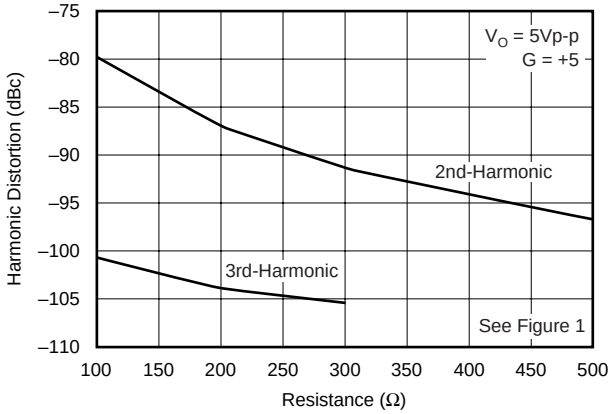
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

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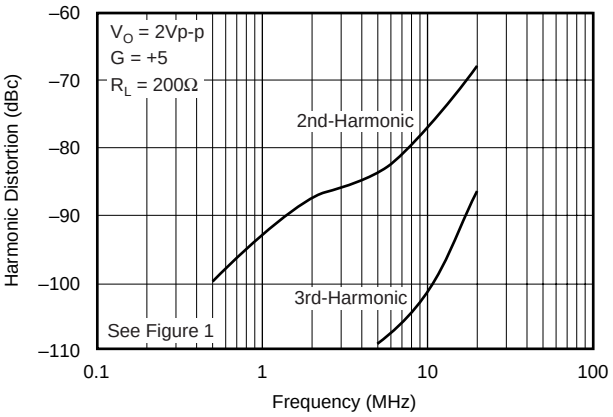
5MHz HARMONIC DISTORTION vs LOAD RESISTANCE



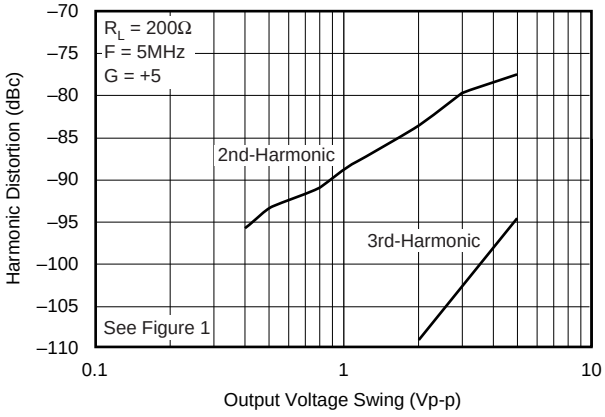
1MHz HARMONIC DISTORTION vs LOAD RESISTANCE



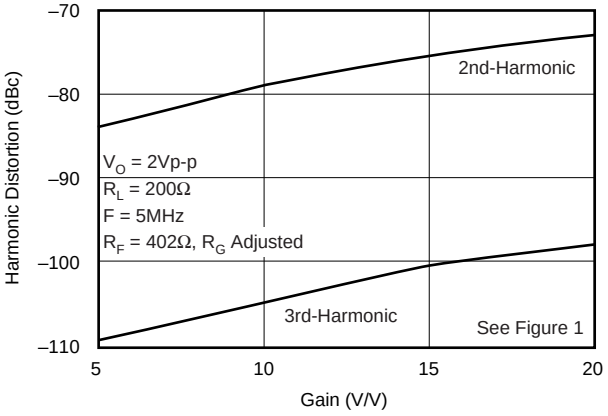
HARMONIC DISTORTION vs FREQUENCY



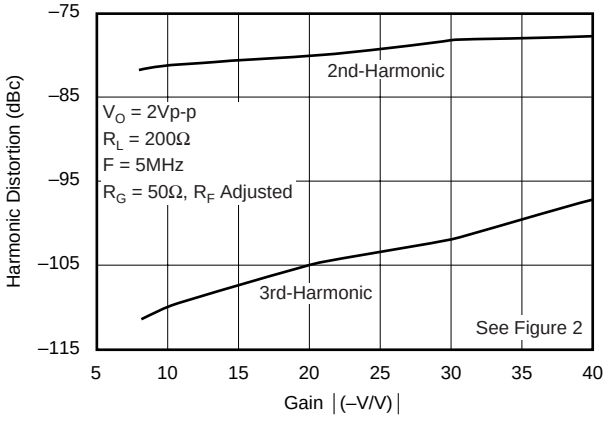
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



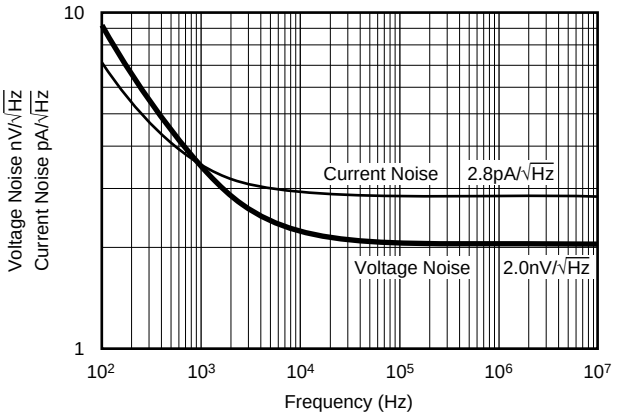
HARMONIC DISTORTION vs INVERTING GAIN



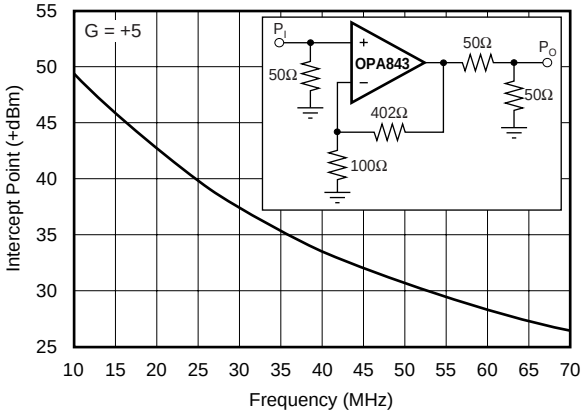
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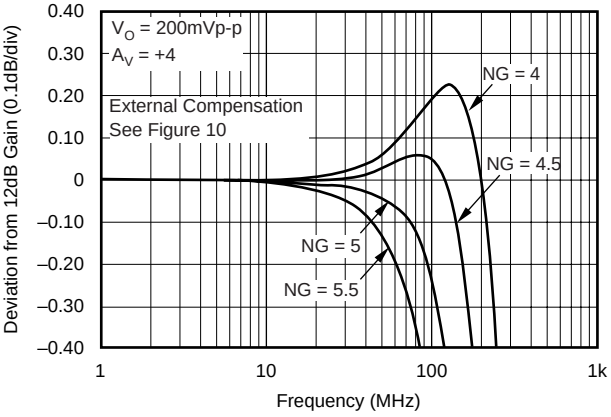
INPUT VOLTAGE AND CURRENT NOISE DENSITY



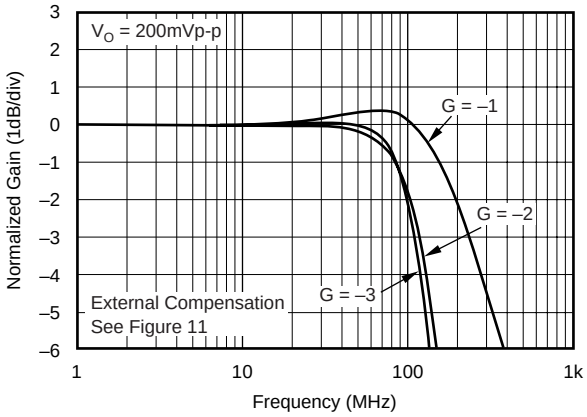
2-TONE, 3RD-ORDER
INTERMODULATION INTERCEPT



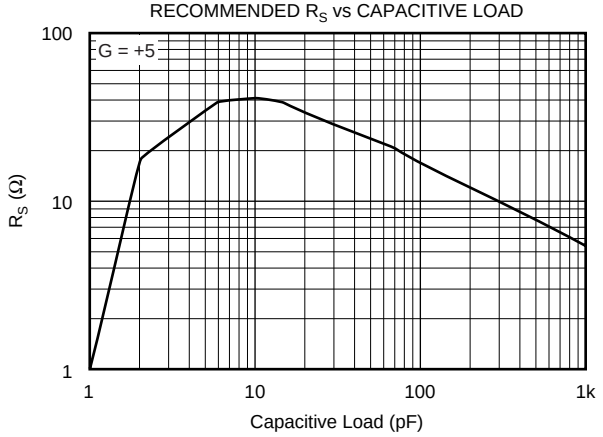
NONINVERTING GAIN FLATNESS TUNE



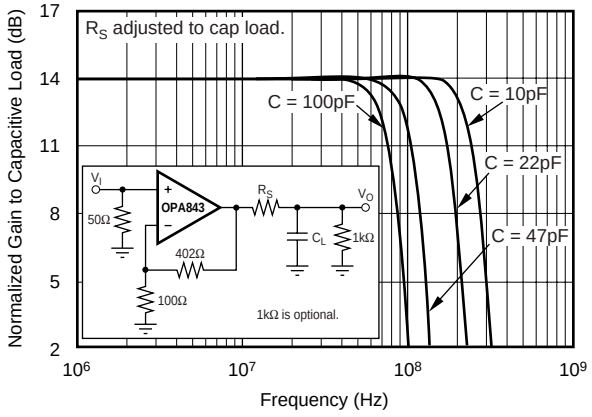
LOW GAIN INVERTING BANDWIDTH



RECOMMENDED R_S vs CAPACITIVE LOAD



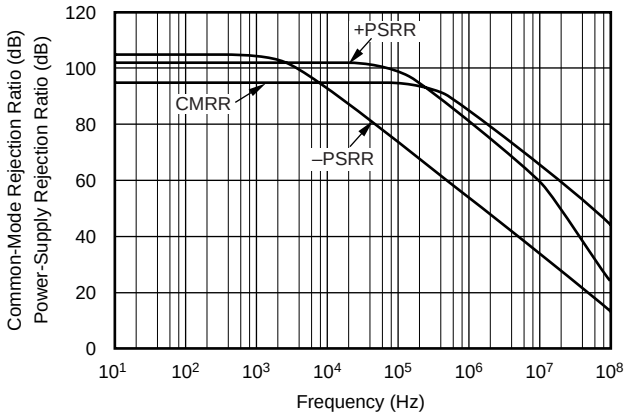
FREQUENCY RESPONSE vs CAPACITIVE LOAD



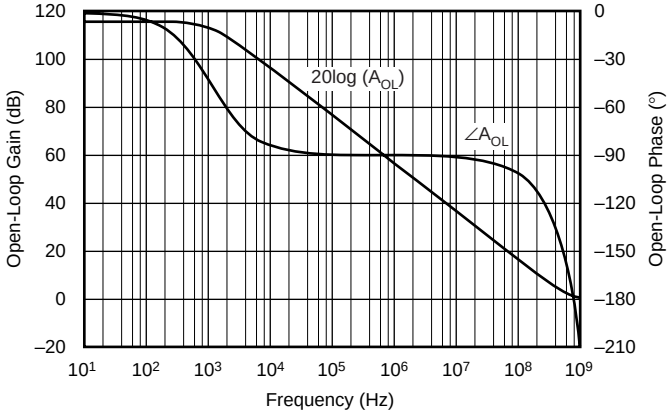
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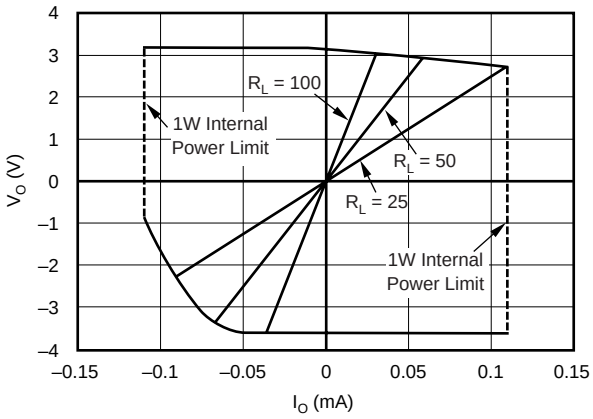
CMRR AND PSRR vs FREQUENCY



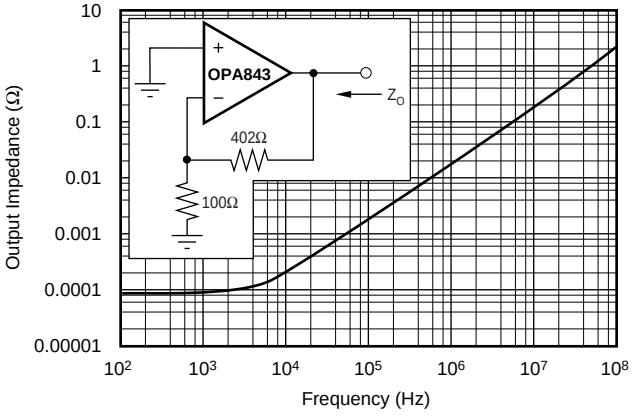
OPEN-LOOP GAIN AND PHASE



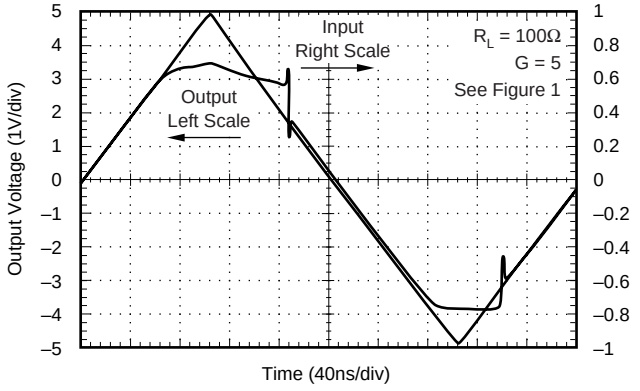
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



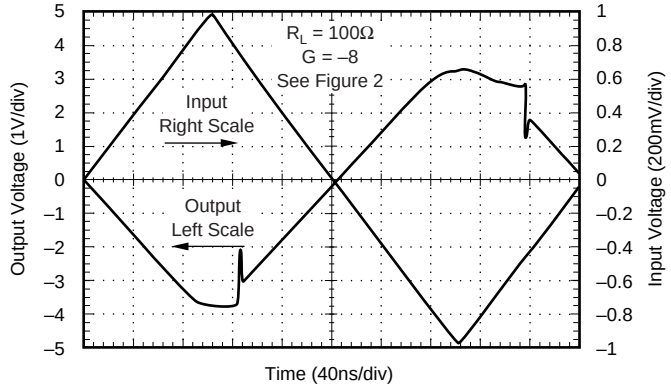
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



NONINVERTING OVERDRIVE RECOVERY



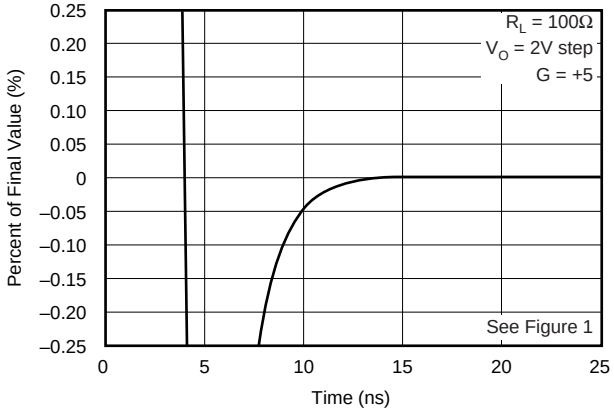
INVERTING OVERDRIVE RECOVERY



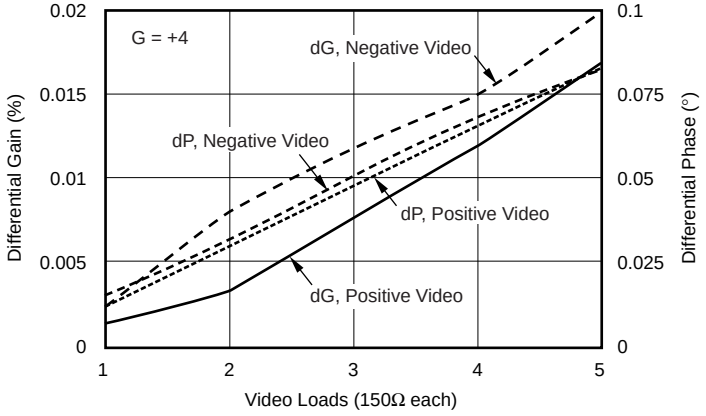
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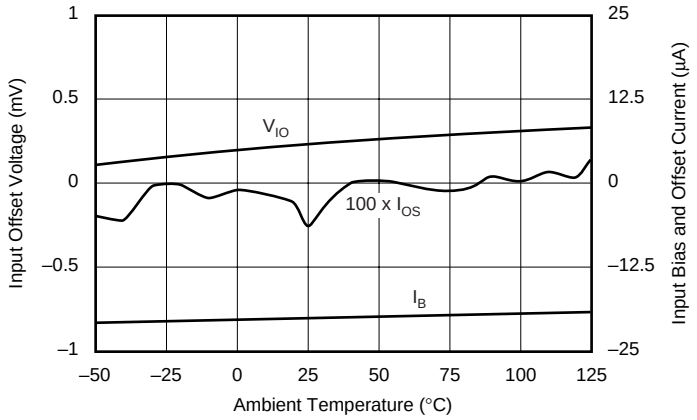
SETTLING TIME



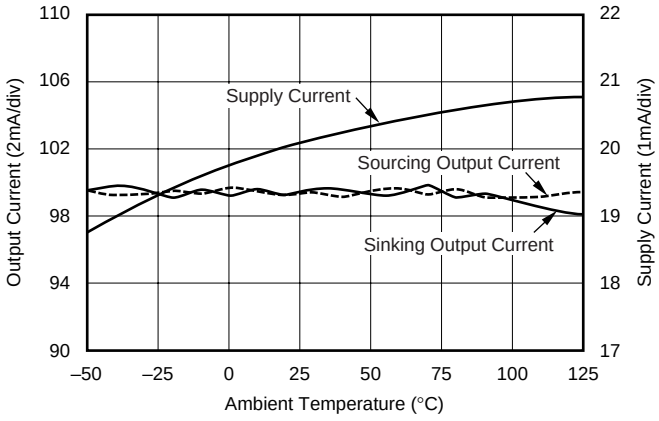
VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE



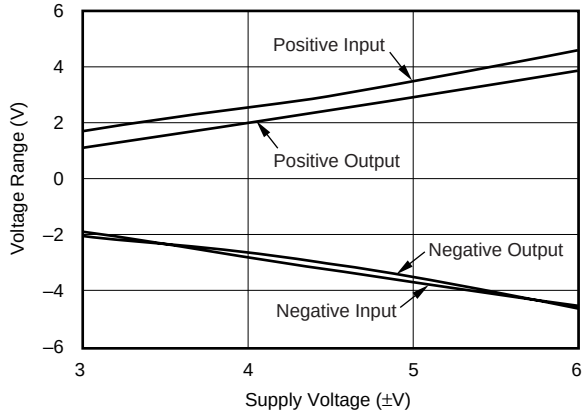
TYPICAL DC DRIFT OVER TEMPERATURE



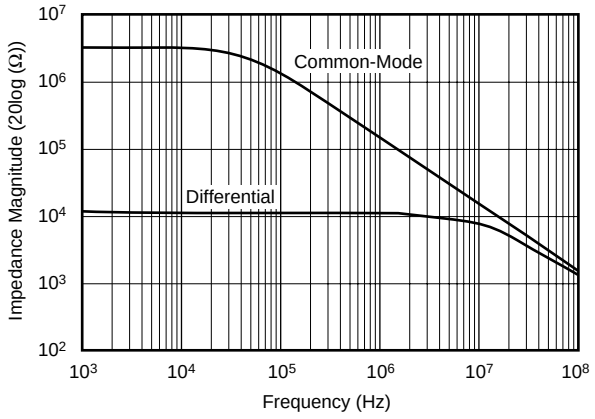
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



COMMON-MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



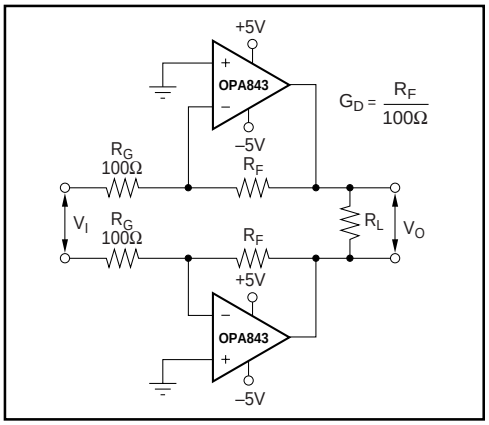
COMMON-MODE AND DIFFERENTIAL INPUT IMPEDANCE



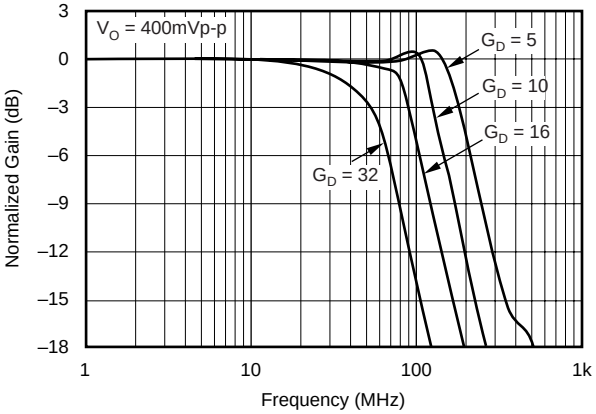
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G_D = 10, R_F = 1kΩ, R_G = 100Ω, and R_L = 100Ω, unless otherwise noted.

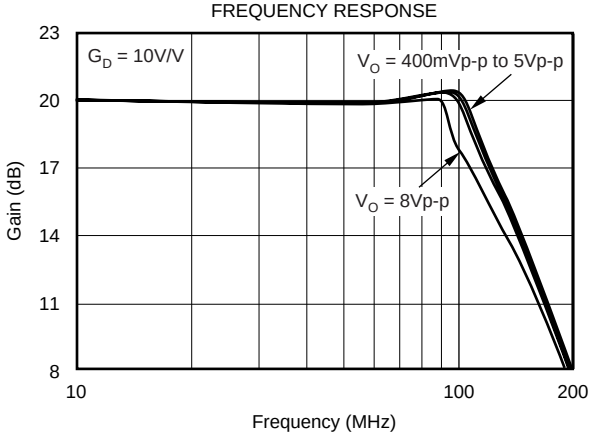
DIFFERENTIAL PERFORMANCE
TEST CIRCUIT



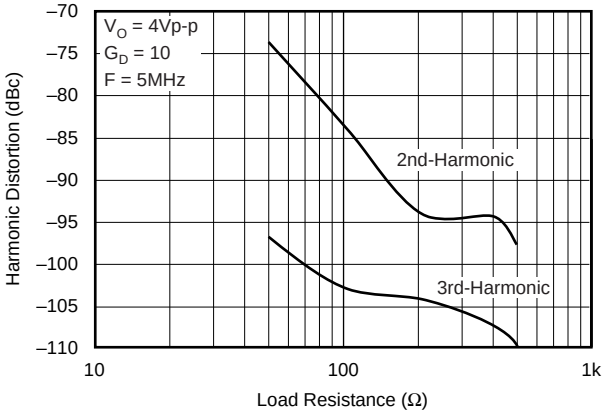
DIFFERENTIAL SMALL-SIGNAL
FREQUENCY RESPONSE



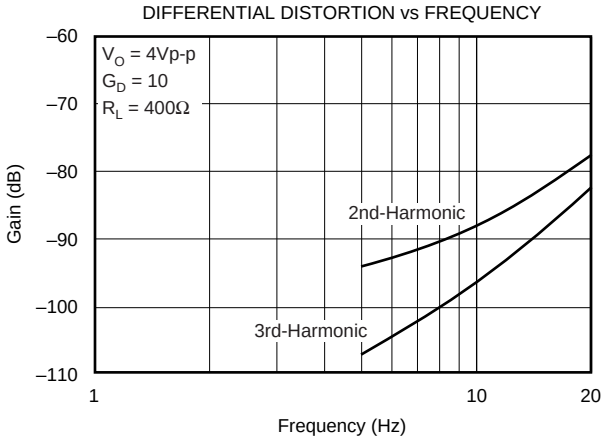
DIFFERENTIAL LARGE-SIGNAL
FREQUENCY RESPONSE



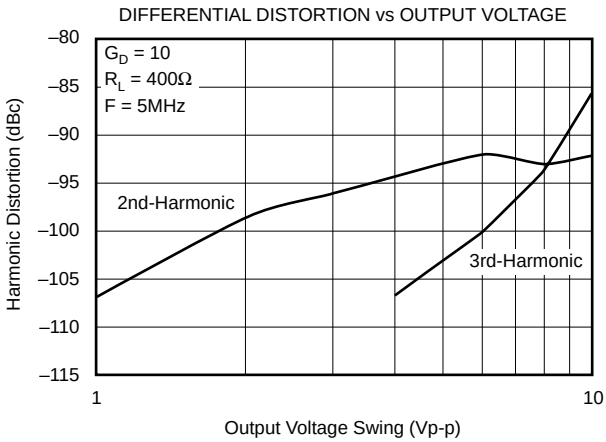
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND NONINVERTING OPERATION

The OPA843's combination of speed and dynamic range is useful in a wide variety of application circuits, as long as simple guidelines common to all high-speed amplifiers are observed. For example, good power-supply decoupling, as shown in Figure 1, is essential to achieve the lowest possible harmonic distortion and smooth frequency response. Careful PC board layout and component selection will maximize the performance of the OPA843 in all applications, as discussed in the following sections of this data sheet. Figure 1 shows the gain of +5 configuration used as the basis for most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance and with measurement equipment presenting 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the input terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swing at the output pin (V_O in Figure 1) while those referring to load power are at the 50Ω load. The total 100Ω load from the series and shunt matching resistors, combined with the 502Ω total feedback network load, presents the OPA843 with an effective output load of approximately 83Ω.

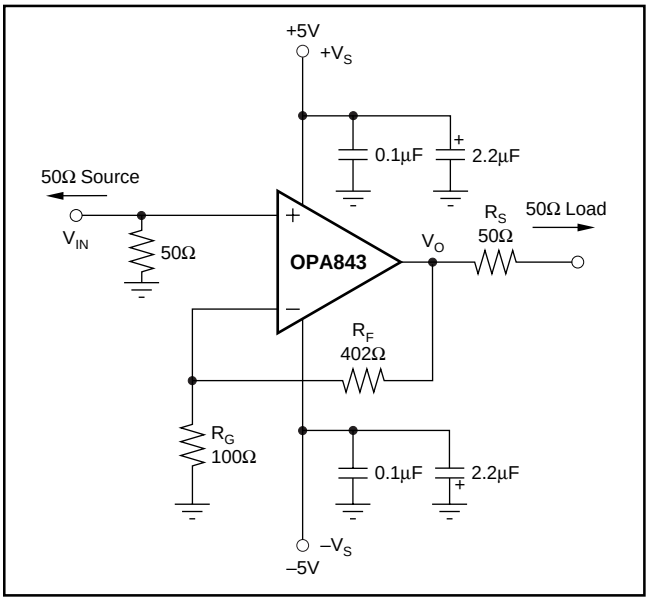


FIGURE 1. Gain of +5, High-Frequency Application and Characterization Circuit.

WIDEBAND, INVERTING GAIN OPERATION

There can be significant benefits to operating the OPA843 as an inverting amplifier. This is particularly true when a matched input impedance is required. Figure 2 shows the inverting gain circuit used as a starting point for the typical characteristics showing inverting mode performance.

Driving this circuit from a 50Ω source, and constraining the gain resistor, R_G, to equal 50Ω will give both a signal bandwidth and noise advantage. R_G in this case is acting as

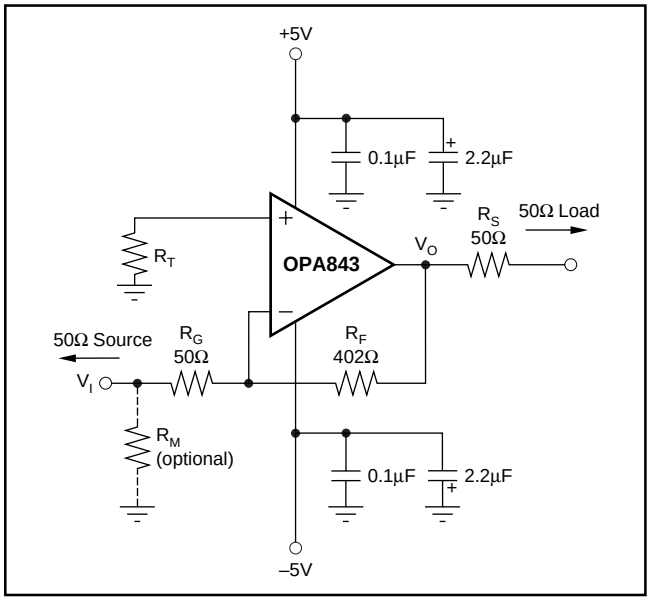


FIGURE 2. Inverting G = –8 Specification and Test Circuit.

both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain for the circuit of Figure 2 is equal to –8V/V (versus the +5V/V for Figure 1), their noise gains are equal when the 50Ω source resistor is included. This has the interesting effect of nearly doubling the equivalent Gain Bandwidth Product (GBP) for the amplifier. This can be seen in comparing the G = +5 and G = –8 small-signal frequency response curves. Both show approximately 260MHz bandwidth, but the inverting configuration of Figure 2 is giving 4dB higher signal gain. If the signal source is actually the low impedance output of another amplifier, R_G is increased to the minimum value allowed at the output of that amplifier and R_F is adjusted to get the desired gain. It is critical for stable operation of the OPA843 that this driving amplifier show a very low output impedance through frequencies exceeding the expected closed-loop bandwidth for the OPA843.

An optional input termination resistor is also shown in Figure 2. This R_M resistor may be used to adjust the input impedance to lower values when R_G needs to be adjusted higher. This might be desirable at lower gains where increasing R_F will reduce the output loading improving harmonic distortion performance. For instance, at a gain of –4 an R_G set to 50Ω will require a 200Ω feedback resistor. In this case, adjusting R_F to 400Ω, setting R_G to 100Ω, and then adding a 100Ω R_M resistor will deliver a gain of –4 with a 50Ω input match.

BUFFERING HIGH-PERFORMANCE ADCs

A single-channel interface using the OPA843 can provide a low noise/distortion interface to emerging 14-bit Analog-to-Digital Converters (ADCs) through approximately 5MHz for medium gain applications. Since the dominant distortion mechanism is 2nd-harmonic distortion, differential circuits using the OPA843 can extend this frequency range and/or power level to much higher levels. The example on the front page of this data sheet, for instance, shows better than 93dB SFDR at 5MHz for up to $8V_{PP}$ signals. This is still being limited by the 2nd-harmonic with

the 3rd-harmonic much lower. 2-tone 3rd-order intermodulation terms will be much lower than most other solutions using the circuit shown on the front page. The differential typical characteristic curves also show that a $4V_{PP}$ output will have > 80dBc SFDR through 20MHz using this differential approach.

WIDE DYNAMIC RANGE "IF" AMPLIFIER

The OPA843 offers an attractive alternative to standard fixed-gain IF amplifier stages. Narrowband systems will benefit from the exceptionally high 2-tone 3rd-order intermodulation intercept, as shown in the Typical Characteristics. Op amps with high open-loop gain, like the OPA843, provide an intercept that decreases with frequency along with the loop gain. The OPA843's 3rd-order intercept shows a decreasing intercept with frequency. The OPA843's intercept is > 30dBm up to 50MHz but improves to > 50dBm as the operating frequency is reduced below 10MHz. Broadband systems will also benefit from the very low even-order harmonics and intermodulation components produced by the OPA843. Compared to standard fixed-gain IF amplifiers, the OPA843 operating at IF's below 50MHz provides much higher intercepts for its quiescent power dissipation (200mW), superior gain accuracy, higher reverse isolation, and lower I/O return loss. The noise figure for the OPA843 will be higher than alternative fixed-gain stages. If the application comes late in the amplifier chain with significant gain in prior stages, this higher noise figure may be acceptable. Figure 3 shows an example of a noninverting configuration for the OPA843 used as an IF amplifier.

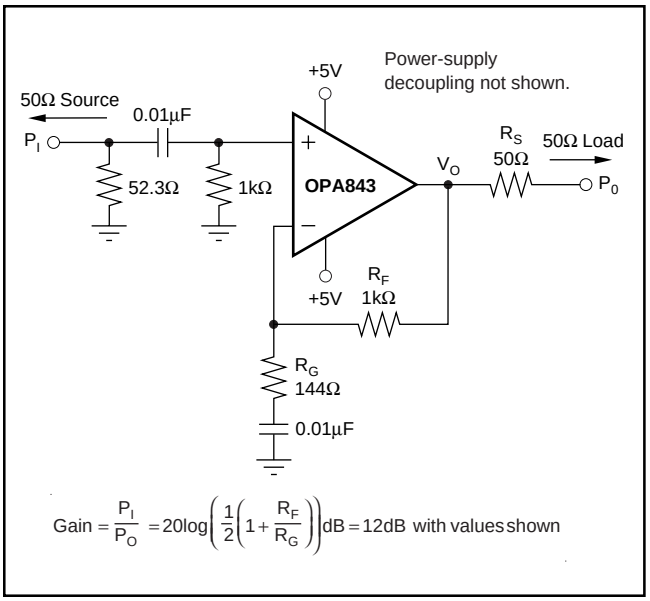


FIGURE 3. High Dynamic Range IF Amplifier.

The input signal and the gain resistor are AC-coupled through the 0.01µF blocking capacitors. This holds the DC input and output operating point at ground independent of source impedance and gain setting. The R_G value in Figure 3 (144Ω), sets the gain to the matched load at 12dB. Using standard 1% tolerance resistors for R_F and R_G will hold the gain to a ±0.2dB tolerance. This example will give a –3dB bandwidth of approximately 100MHz while maintaining gain flatness within 1dB through 50MHz. For narrowband IF's in the 44MHz region, this configuration of the OPA843 will show a 3rd-order intercept of 33dBm while dissipating only 200mW (23dBm) power from ±5V supplies.

PHOTODIODE TRANSIMPEDANCE AMPLIFIER

High Gain Bandwidth Product (GBP) and low input voltage and current noise make the OPA843 an ideal wideband transimpedance amplifier for low to moderate gains. Note that unity-gain stability is not required for transimpedance applications. Figure 4 shows an example photodiode amplifier circuit. The key parameters of this design are the estimated diode capacitance (C_D) at the applied DC reverse bias voltage ($-V_B$), the desired transimpedance gain (R_F), and the GBP for the OPA843 (800MHz). With these three variables set (and adding the OPA843's parasitic input capacitance to the value of C_D to get C_S), the feedback capacitor value (C_F) is selected to provide stability for the transimpedance frequency response.

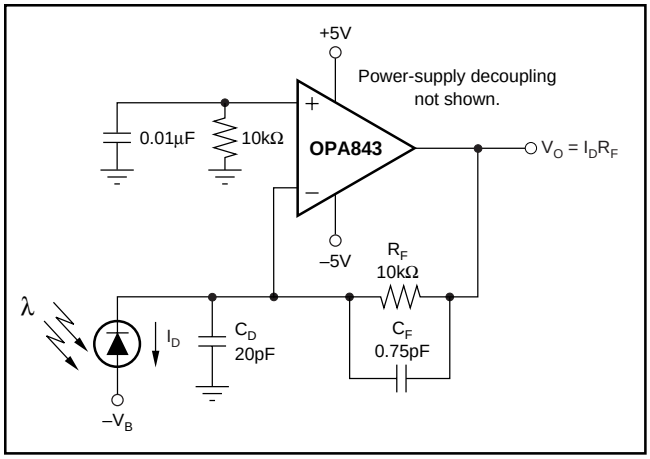


FIGURE 3. High Dynamic Range IF Amplifier.

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_S}} \qquad C_S = C_D + C_I \tag{1}$$

Adding the OPA843's common-mode and differential mode input capacitances C_I = (1.0 + 1.2)pF to the 20pF diode source capacitance of Figure 4, and targeting a 10kΩ transimpedance gain using the 800MHz GBP for the OPA843, the required feedback pole frequency is 16.9MHz. This will require a total feedback capacitance of 0.94pF. Typical surface-mount resistors have a parasitic capacitance of 0.2pF, leaving the required 0.75pF value shown in Figure 4 to get the required feedback pole.

This will set the –3dB bandwidth according to:

$$F_{-3dB} \cong \sqrt{\frac{GBP}{2\pi R_F C_S}} Hz \tag{2}$$

The example of Figure 4 will give approximately 24MHz –3dB bandwidth using the 0.75pF feedback compensation.

WIDEBAND INVERTING SUMMING AMPLIFIER

One common application for a wideband op amp like the OPA843 is to sum a number of signal sources together. Figure 5 shows the inverting summing configuration that is most often used. This circuit offers the benefit that each input sees an input impedance set only by its individual input resistor, since the summing junction (inverting op amp node) is a virtual ground. Each input is non-interactive with every other. However, the bandwidth from any input to the summed output is set by the op amp noise gain (NG), which is equal to the noninverting voltage gain. Therefore, each inverting channel may have a low gain to the output (like the –1 shown in Figure 5); this noise gain will set the frequency response and the loop stability. The noninverting gain for Figure 5 is equal to +5, which will give a 260MHz bandwidth at a gain of –1 for each of the input signals.

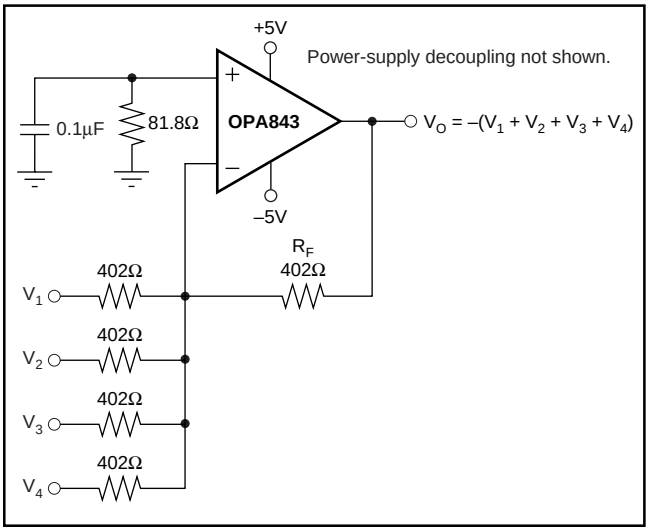


FIGURE 5. Wideband Inverting Summing Amplifier.

2nd-Order Filter Topology

High-speed amplifiers like the OPA843 are good choices for 2nd-order filter building blocks as part of ADC driver channels. These can provide noise bandlimiting to improve the SNR for the amplifier/converter combination. The circuit of Figure 6 shows an example of a 10MHz Butterworth low-pass filter where the amplifier provides a low frequency gain of 5 and a 2nd-order cutoff at 10MHz. The resistor values have been adjusted slightly to account for the amplifier bandwidth. Figure 7 shows the small-signal frequency response for this filter.

EQUALIZING FILTER APPLICATION

In sensor receiver applications, where the pickup is a sensor or cable giving a bandlimited frequency response, an equalizing filter can sometimes be used to extend the useable frequency range for the sensor. This is done mathematically by taking the inverse of the rolloff transfer function and implementing that as the amplifier frequency response. See Figure 8 for one example of a wideband equalizer where two stages of the OPA843 are used. This example is set to

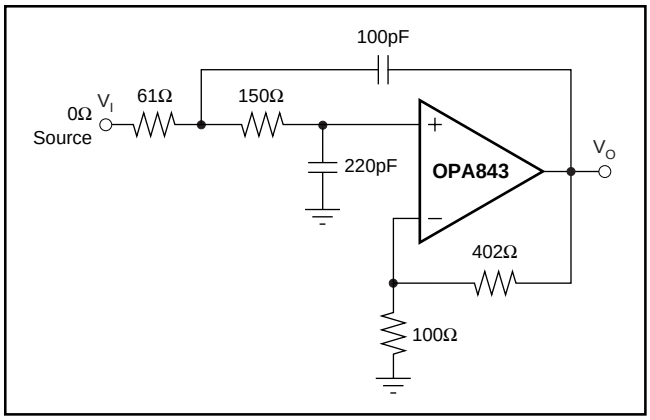


FIGURE 6. 10MHz Butterworth Low-Pass Filter.

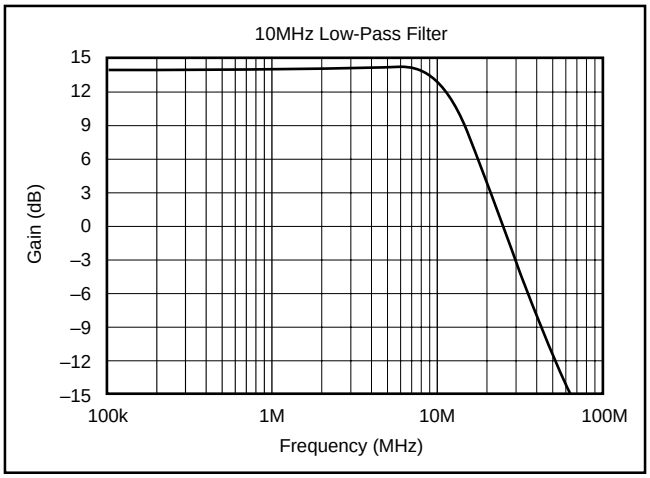


FIGURE 7. Frequency Response for Figure 6.

transition from a unity gain receiver at lower frequencies (through the R_5 path) to a gain of 20dB (10V/V) through the R_1 path at higher frequencies. The component values have been selected to set the peak gain at approximately 30MHz. A unique feature for this circuit is an independent tune on the width of the peaking (Q of the response) by adjusting R_G. See Figure 9 for the effect of adjusting R_G over the range of 20Ω to 100Ω.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA843 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in the table below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA843U	SO-8	DEM-OPA-SO-1A	SBOU009
OPA843N	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA843 product folder.

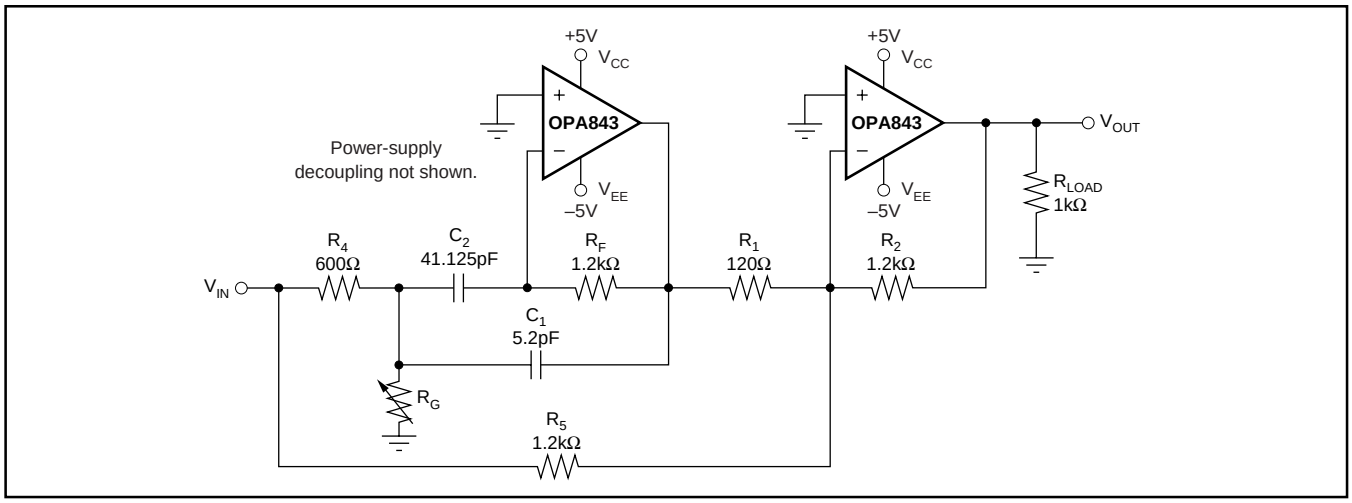


FIGURE 8. Adjustable Equalizer.

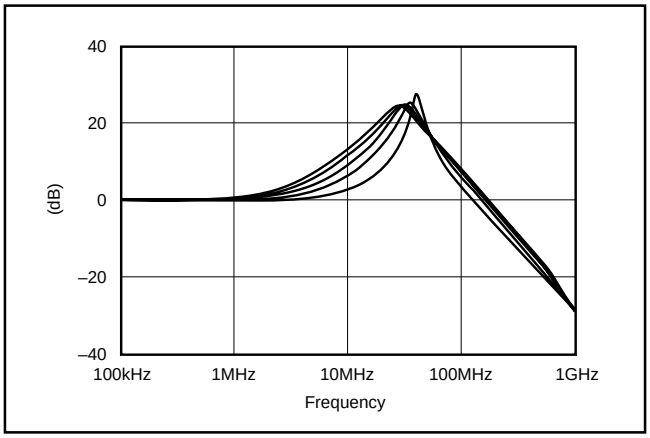


FIGURE 9. Equalizer Plot, Multiple Settings.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA843 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA843 is available through the TI web page (http://www.ti.com). The applications department is also available for design assistance. These models predict typical small-signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of this data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA843 is a voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. Usually, the feedback resistor value should be between 200Ω and 1kΩ. Below 200Ω, the feedback network will present additional output loading that can degrade the harmonic distortion performance of the OPA843. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 1) to be less than about 200Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G < 200\Omega$ will keep this pole above 400MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and, therefore, the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains the resultant feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of –4 with a 50Ω input matching resistor (= R_G) would require a 200Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground; see Figure 2. The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH vs GAIN

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when

the phase margin approaches 90°, as it does in high-gain configurations. At low signal gains, most amplifiers will exhibit a more complex response with lower phase margin. The OPA843 is optimized to give a maximally flat 2nd-order Butterworth response in a gain of 5. In this configuration, the OPA843 has approximately 60° of phase margin and will show a typical –3dB bandwidth of 260MHz. When the phase margin is 60°, the closed-loop bandwidth is approximately $\sqrt{2}$ greater than the value predicted by dividing GBP by the noise gain. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +20, the 40MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 800MHz.

LOW GAIN OPERATION

Decreasing the operating gain for the OPA843 from the nominal design point of +5 will decrease the phase margin. This will increase the Q for the closed-loop poles, peak up the frequency response, and extend the bandwidth. A peaked frequency response will show overshoot and ringing in the pulse response as well as a higher integrated output noise. Operating at a noise gain less than +3 runs the risk of sustained oscillation (loop instability). However, operation at low gains would be desirable to take advantage of the much higher slew rate and lower input noise voltage available in the OPA843, as compared to the performance offered by unity-gain stable op amps. Numerous external compensation techniques have been suggested for operating a high-gain op amp at low gains. Most of these give zero/pole pairs in the closed-loop response that cause long term settling tails in the pulse response and/or phase nonlinearity in the frequency response. Figure 10 shows an external compensation method for a noninverting configuration that does not suffer from these drawbacks.

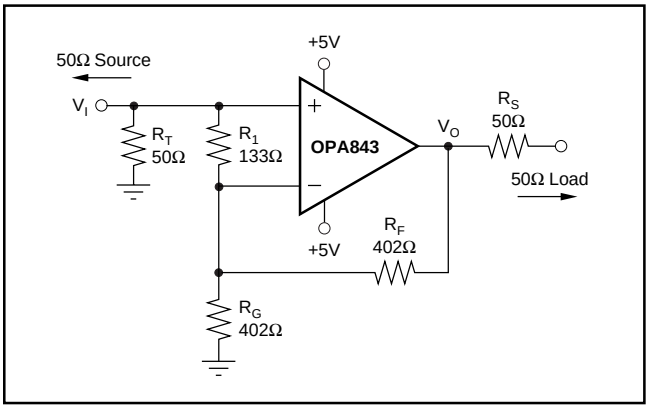


FIGURE 10. Noninverting Low Gain Circuit.

The R_1 resistor across the two inputs will increase the noise gain (i.e., decrease the loop gain) without changing the signal gain. This approach will retain the full slew rate to the output but will give up some of the low-noise benefit of the OPA843. Assuming a low source impedance, set R_1 so that $1 + R_F/(R_G \parallel R_I)$ is ≥ +3. This approach may also be used to tune the flatness by adjusting R_I. The Typical Characteristics show a signal gain of +4 with the noise gain adjusted for flatness using different values for R_1.

Where low gain is desired, and inverting operation is acceptable, a new external compensation technique may be used to retain the full slew rate and noise benefits of the OPA843 while maintaining the increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the noise gain for good stability while giving an easily controlled 2nd-order low-pass frequency response. Figure 11 shows this circuit. Considering only the noise gain for the circuit of Figure 11, the low-frequency noise gain (NG_1) will be set by the resistor ratios while the high-frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole (set by $1/R_FC_F$) is placed correctly, a very well controlled 2nd-order low-pass frequency response will result.

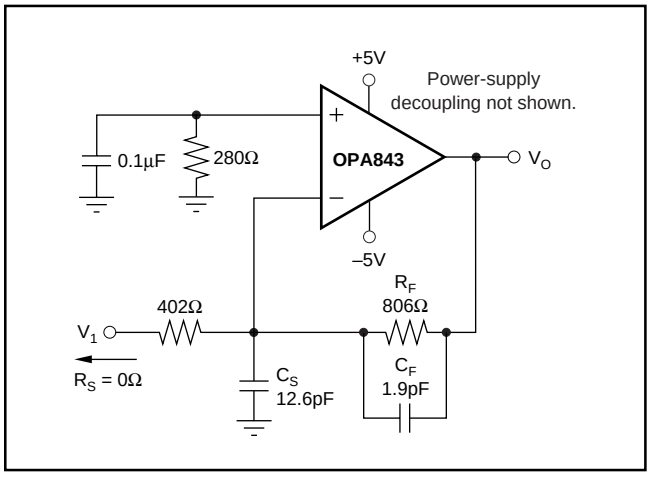


FIGURE 10. Noninverting Low Gain Circuit.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain, NG_2, which should be greater than the minimum stable gain for the OPA843. Here, a target NG_2 of 7.5 will be used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain, NG_1. To simplify this discussion, we will target a maximally flat 2nd-order low-pass Butterworth frequency response (Q = 0.707). The signal gain of –2 shown in Figure 11 will set the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 3 in this example). Then, using only these two gains and the GBP for the OPA843 (800MHz), the key frequency in the compensation is determined by:

$$Z_0 = \frac{GBP}{NG_1^2}\left(1 - \frac{NG_1}{NG_2} - \sqrt{1 - 2\frac{NG_1}{NG_2}}\right) \qquad (11)$$

Physically, this Z_0 (13.6MHz for the values shown in Figure 11) is set by $1/(2\pi \cdot R_F (C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect unity gain if projected back to 0dB gain. The actual zero in the noise gain

occurs at $NG_1 \bullet Z_0$ and the pole in the noise gain occurs at $NG_2 \bullet Z_0$. Since GBP is expressed in Hz, multiply Z_0 by 2π and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi R_F Z_0 NG_2} \quad (12)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S by:

$$C_S = (NG_2 - 1)C_F \quad (13)$$

The resulting closed-loop bandwidth will be approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_0 GBP} \quad (14)$$

For the values shown in Figure 10, the f_{-3dB} will be approximately 105MHz. This is less than that predicted by simply dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value while providing full slew rate and exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_0$. The capacitor values shown in Figure 10 are calculated for $NG_1 = 3$ and $NG_2 = 7.5$ with no adjustment for parasitics.

OUTPUT DRIVE CAPABILITY

The OPA843 has been optimized to drive the demanding load of a doubly-terminated transmission line. When a 50Ω line is driven, a series 50Ω into the cable and a terminating 50Ω load at the end of the cable are used. Under these conditions, the impedance of the cable appears resistive over a wide frequency range and the total effective load on the OPA843 is 100Ω in parallel with the resistance of the feedback network. The Electrical Characteristics show a $6.1V_{PP}$ swing into a 100Ω load—which is then reduced to a $3V_{PP}$ swing at the termination resistor. The ±85mA output drive over temperature provides adequate current drive margin for this load.

A common IF amplifier specification, which describes available output power is the –1dB compression point. This is usually defined at a matched 50Ω load to be the sinusoidal power where the gain has compressed by –1dB vs the gain seen at very low power levels. This compression level is frequency dependent for an op amp, due to both bandwidth and slew rate limitations. For frequencies well within the bandwidth and slew rate limit of the OPA843, the –1dB compression at a matched 50Ω load will be > 13dBm based on the minimum available 3Vp-p swing at the load. One common use for the –1dB compression is to predict intermodulation intercept. This is normally 10dB greater than the –1dB compression power for a standard RF amplifier. This simple rule of thumb does NOT apply to the OPA843. The high open-loop gain and Class AB output stage of the OPA843 produce a much higher intercept than the –1dB compression would predict, as shown in the Typical Characteristics.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. A high-speed, high open-loop gain amplifier like the OPA843 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency-response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended *R_S vs Capacitive Load* and the resulting frequency response at the load. The criterion for setting the recommended resistor is maximum bandwidth and flat frequency response at the load. Since there is now a passive low-pass filter between the output pin and the load capacitance, the response at the output pin itself is typically somewhat peaked, and becomes flat after the roll off action of the RC network. This is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the amplifier's swing limit.

Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA843. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA843 output pin (see Board Layout section).

DISTORTION PERFORMANCE

The OPA843 is capable of delivering an exceptionally low distortion signal at high frequencies and medium gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100dB dynamic range. The OPA843's distortion does not rise above –100dBc until either the signal level exceeds 0.5Vp-p and/or the fundamental frequency exceeds 500kHz.

Distortion in the audio band is < –120dBc.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is the sum of $R_F + R_G$, whereas in the inverting configuration this is just R_F (see Figure 1). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase

the 2nd-harmonic 12dB and the 3rd-harmonic 18dB. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again, a 6dB increase in gain will increase the 2nd- and 3rd-harmonic by 6dB even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases due to the roll off in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 3kHz. Starting from the –100dBc 2nd-harmonic for $2V_{PP}$ into 200Ω, G = +5 distortion at 500kHz (from the Typical Characteristics), the 2nd-harmonic distortion at 20kHz should be approximately:

–100dB – 20log (500kHz/20kHz) = –128dBc.

The OPA843 has an extremely low 3rd-order harmonic distortion. This also gives an exceptionally good 2-tone, 3rd-order intermodulation intercept, as shown in the Typical Characteristics. This intercept curve is defined at the 50Ω load when driven through a 50Ω-matching resistor to allow direct comparisons to RF MMIC devices. This network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA843 drives directly into the input of a high-impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept will increase by a minimum of 6dBm. The intercept is used to predict the intermodulation spurious for two closely spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\mu f = |f_2 – f_1|/2$, the two, 3rd-order, close-in spurious tones will appear at $f_O \pm (3 \bullet \Delta f)$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by $2 \bullet (IM3 – P_O)$ where IM3 is the intercept taken from the typical characteristic curve and P_O is the power level in dBm at the 50Ω load for one of the two closely spaced test frequencies. For instance, at 10MHz the OPA843 at a gain of +5 has an intercept of 49dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be 2Vp-p, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones will then be 2 • (49 – 4) = 90dBc below the test-tone power level (–86dBm). If this same 2Vp-p 2-tone envelope were delivered directly into the input of an ADC without the matching loss or loading of the 50Ω network, the intercept would increase to at least 55dBm. With the same signal and gain conditions now driving directly into a light load, the spurious tones will then be at least 2 • (55 – 4) = 102dBc below the $1V_{PP}$ test-tone signal levels.

NOISE PERFORMANCE

The OPA843 complements its ultra low harmonic distortion with low input noise terms. Both the input-referred voltage noise, and the two input-referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 12 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either $nV/\sqrt{Hz}$ or $pA/\sqrt{Hz}$.

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, and then taking the square root to get back to a spot noise voltage. Equation 15 shows the general form for this output noise voltage using the terms presented in Figure 12.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (15)$$

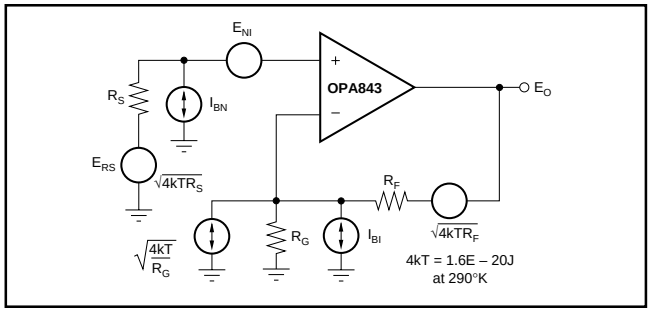


FIGURE 12. Op Amp Noise Analysis Model.

Dividing this expression by the noise gain ($NG = 1 + R_F/R_G$) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 16.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (16)$$

Evaluating these two equations for the OPA843 circuit presented in Figure 1 will give a total output spot noise voltage of $12.4nV/\sqrt{Hz}$ and an equivalent input spot noise voltage of $2.48nV/\sqrt{Hz}$.

DC OFFSET CONTROL

The OPA843 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA843 has a relatively high input bias current (20µA typical into the pins) but with a very close match between the two input currents—typically 0.17µA input offset current. Figures 13 and 14 show typical distribution of input offset voltage and current for the OPA843.

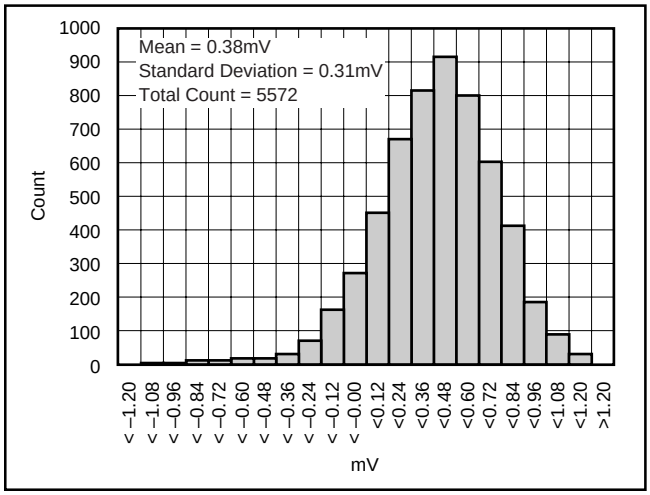


FIGURE 13. Input Offset Voltage Distributing in mV.

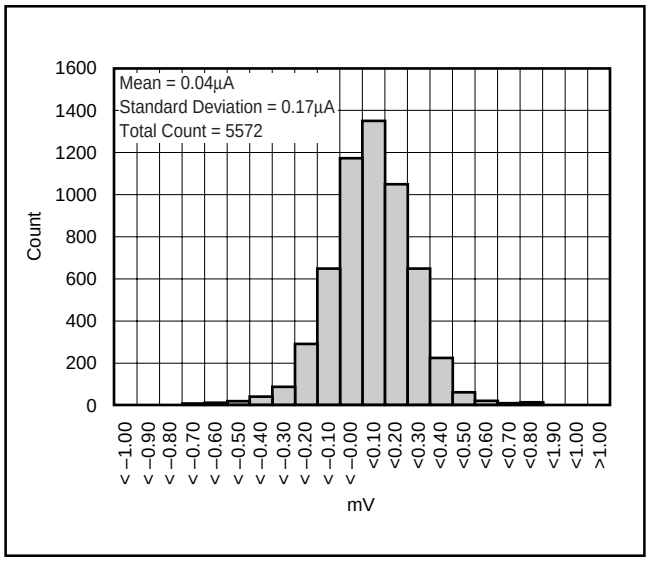


FIGURE 14.

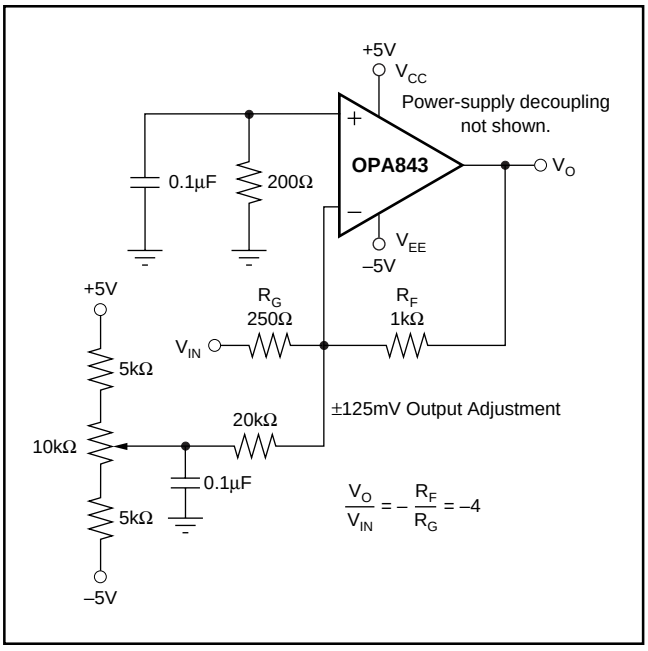


FIGURE 15. DC-Coupled, Inverting Gain of –4 with Output Offset Adjustment.

The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 55Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC coupled, this will increase the source impedance for the noninverting input bias current to 80Ω. Since this is now equal to the impedance looking out of the inverting input (R_F || R_G), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402Ω feedback resistor, this output error will now be less than 1µA • 402Ω = 0.4mV at 25°C.

A fine-scale output offset null, or DC operating point adjustment, is sometimes required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to insure that it has a minimal impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path uses the inverting mode, applying an offset control to the noninverting input can be considered. For a DC-coupled inverting input signal, this DC offset signal will set up a DC current back into the source that must be considered. An offset adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness. Figure 15 shows one example of an offset adjustment for a DC-coupled signal path that will have minimum impact on the signal frequency response. In this case, the input is brought into an inverting gain resistor with the DC adjustment an additional current summed into the inverting node. The resistor values for setting this offset adjustment are chosen to be much larger than the signal path resistors. This will insure that this adjustment has minimal impact on the loop gain and hence, the frequency response.

THERMAL ANALYSIS

The OPA843 will not require heat sinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA843IDBV (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C. $P_D = 10V(22.5mA) + 5^2/(4 \bullet (100\Omega \,||\, 500\Omega)) = 300mW$. Maximum T_J = +85°C + (0.30W • 150°C/W) = 130°C.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the OPA843 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA843. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-feedback side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended *R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA843 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA843 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA843 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA843 onto the board.

INPUT AND ESD PROTECTION

The OPA843 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 16.

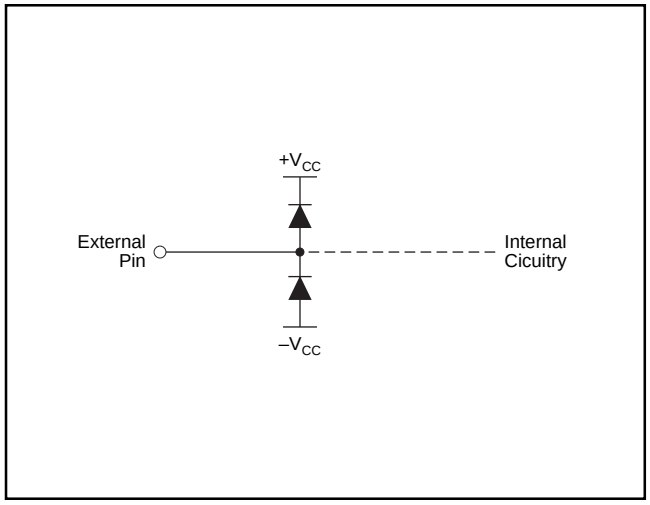


FIGURE 16. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA843), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Figure 17 shows one example of an overdrive protection circuit added to a G = +5V/V design.

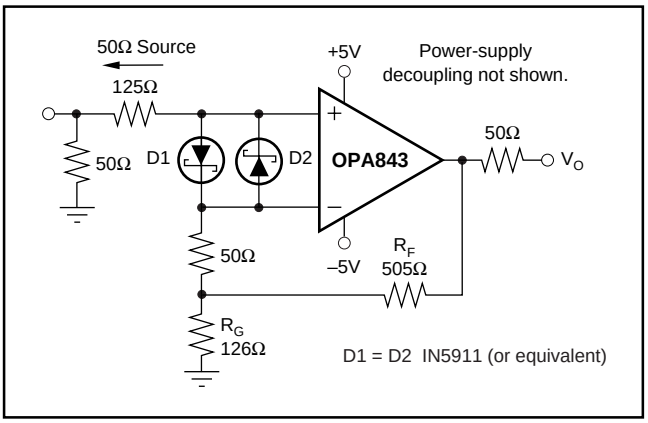


FIGURE 17. Gain of +5 with Input Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	C	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
3/06	B	13	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA843ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 843	Samples
OPA843IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OARI	Samples
OPA843IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OARI	Samples
OPA843IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 843	Samples
OPA843IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 843	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

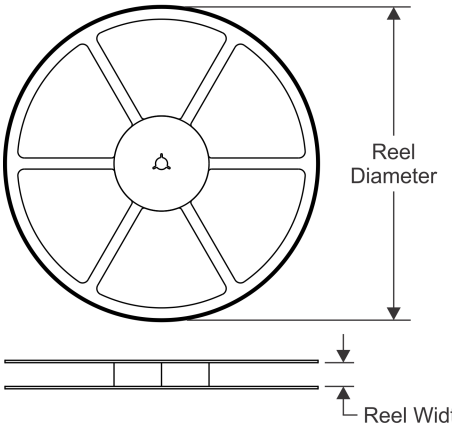
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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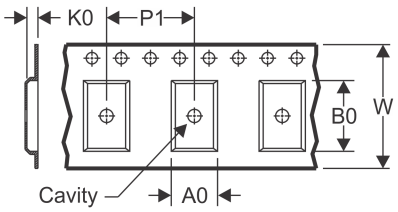
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

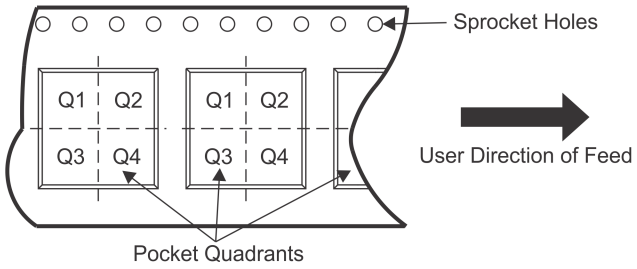


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

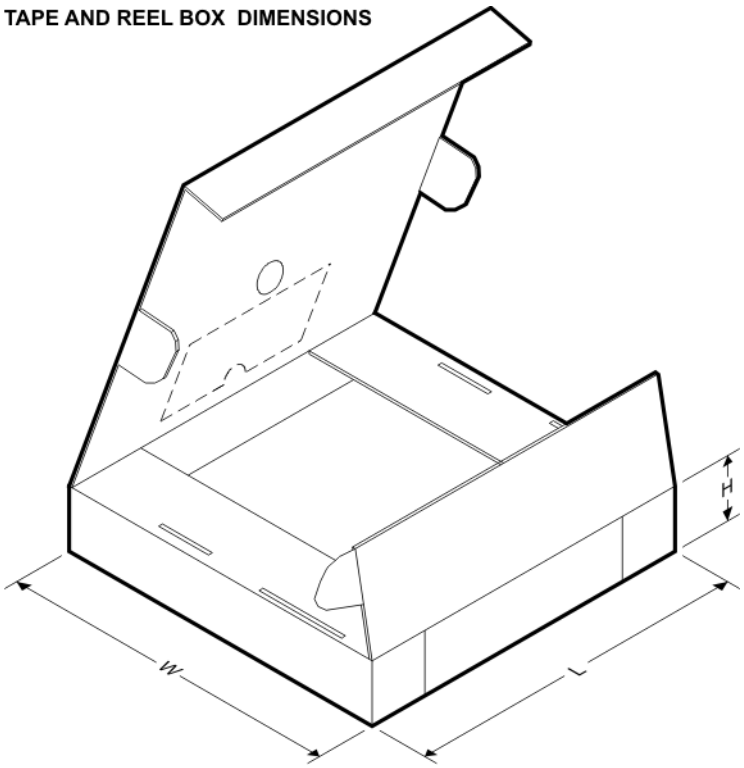
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

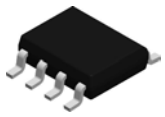
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA843IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA843IDR	SOIC	D	8	2500	367.0	367.0	35.0

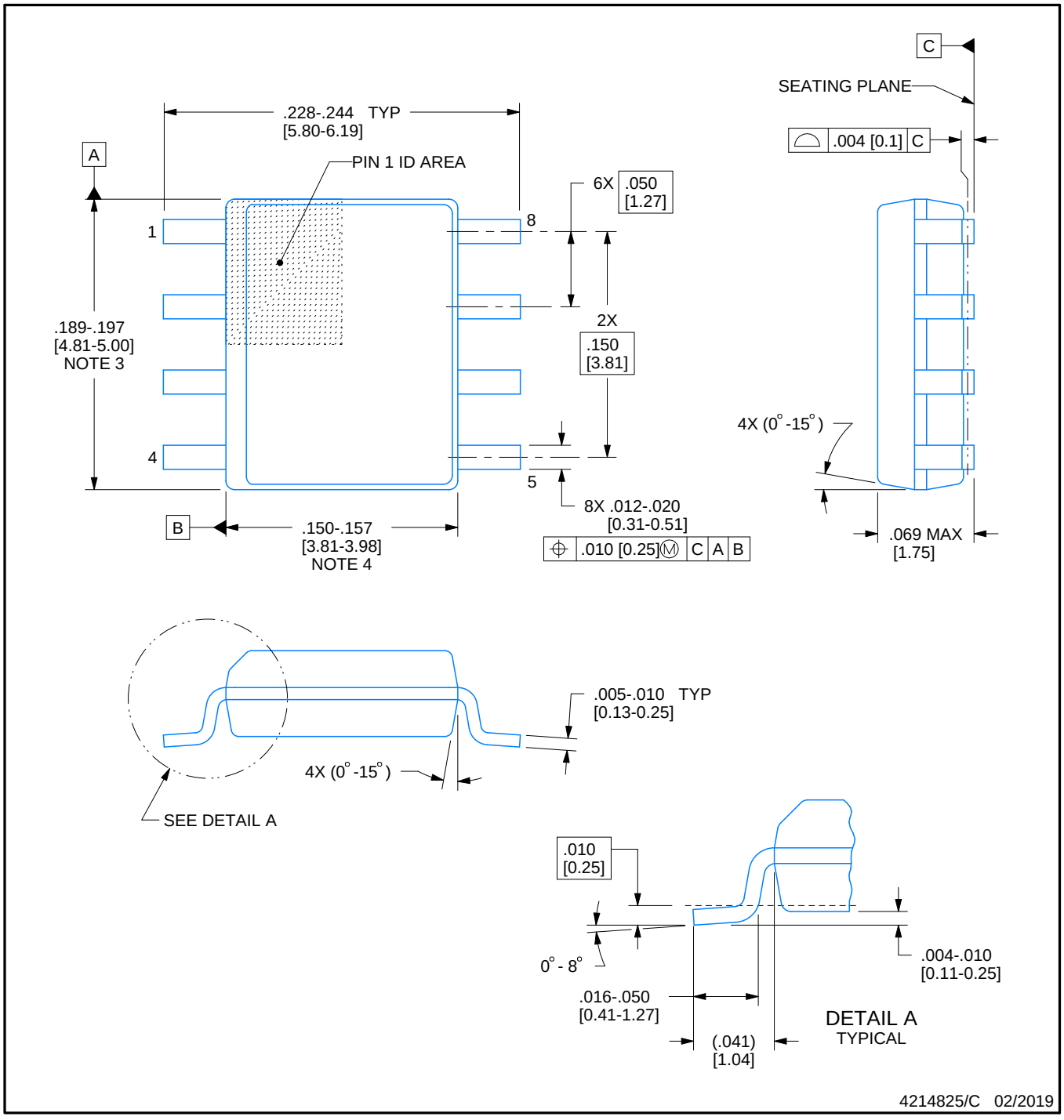


PACKAGE OUTLINE

D0008A

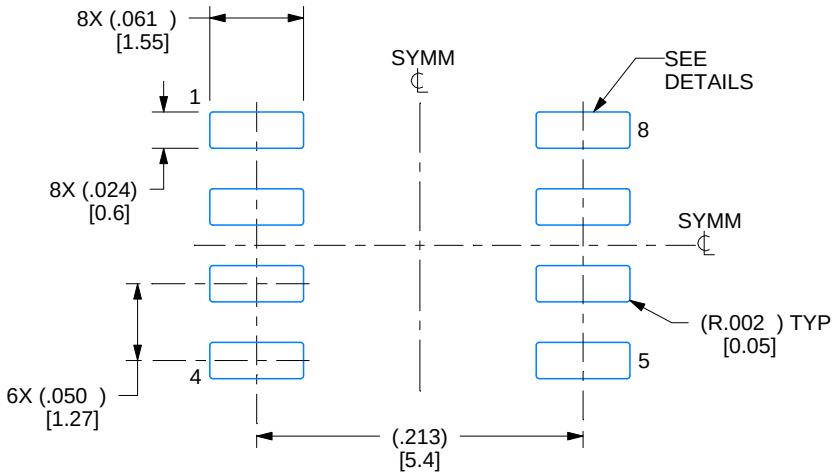
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

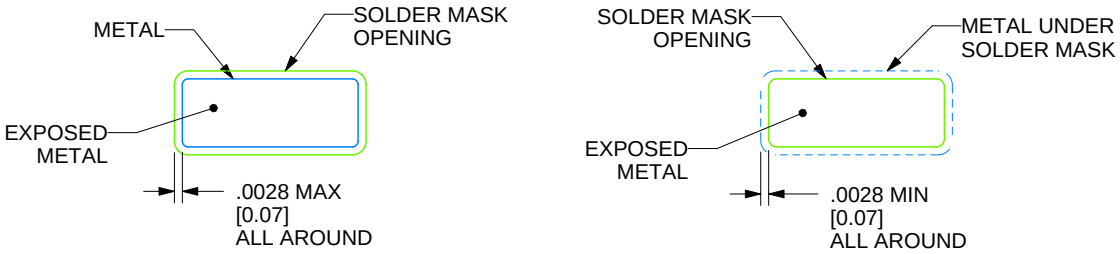


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

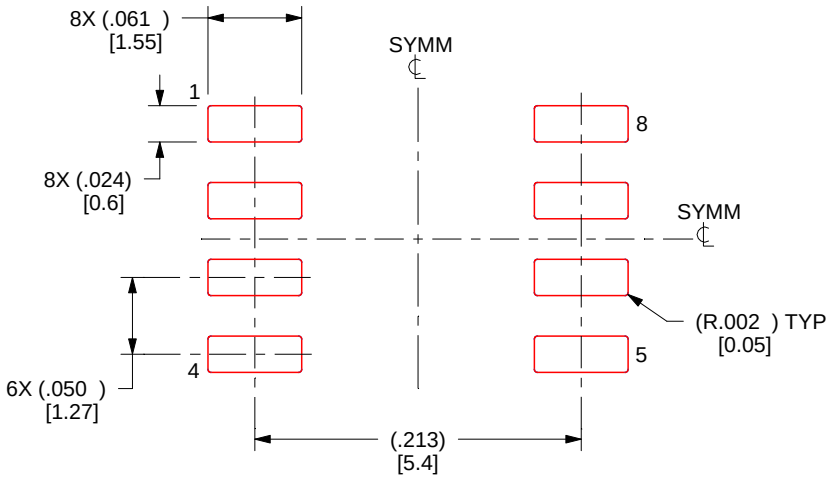
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

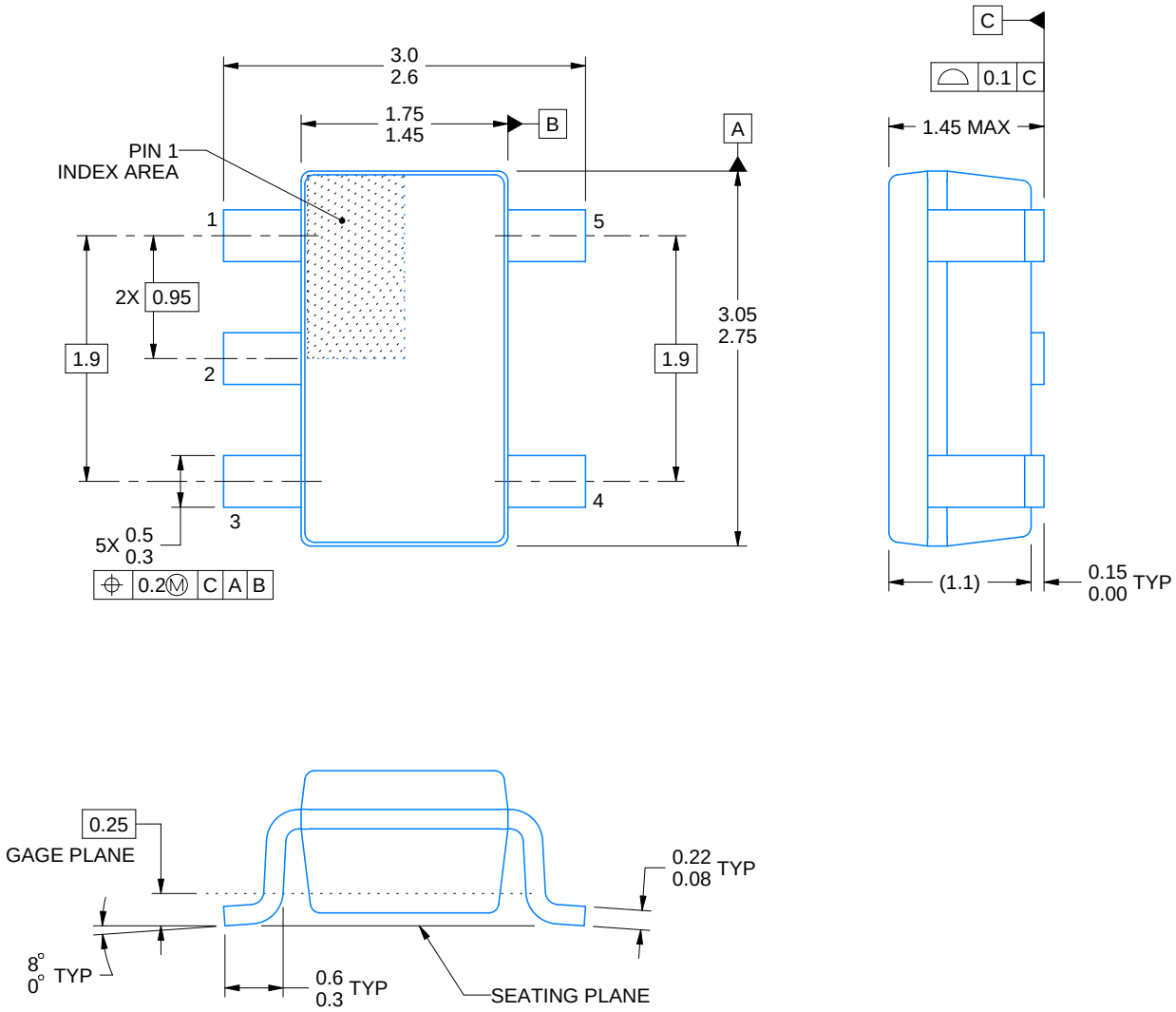
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

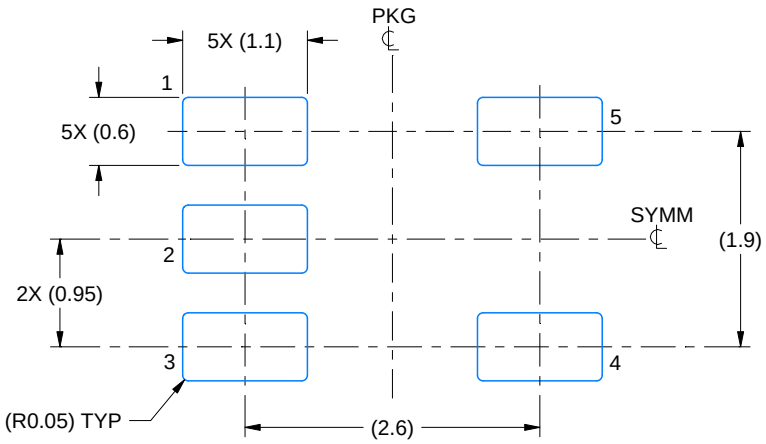
SMALL OUTLINE TRANSISTOR



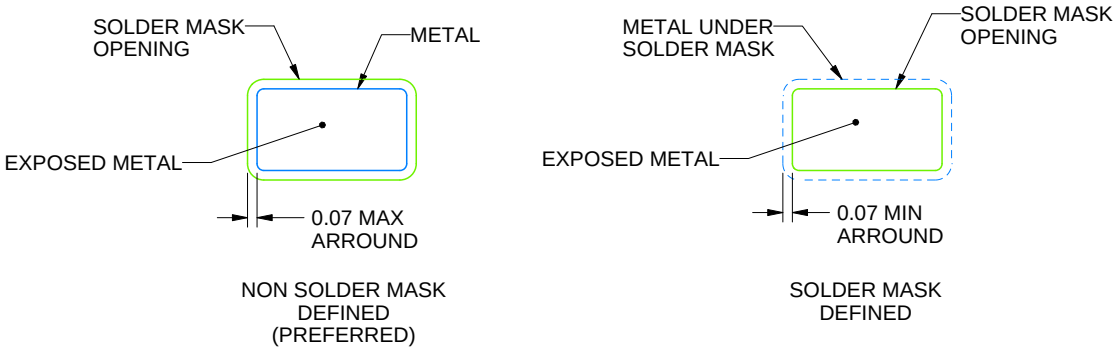
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

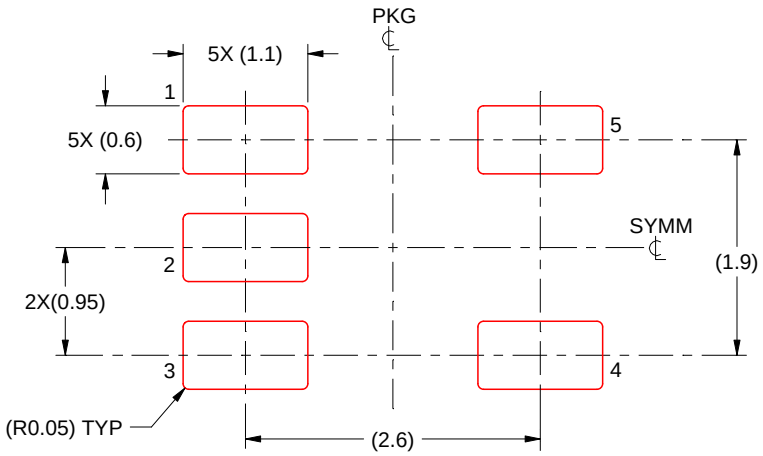


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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