Wideband, Low-Noise, Voltage-Feedback OPERATIONAL AMPLIFIER

FEATURES

- HIGH BANDWIDTH: 400MHz (G = +10)
- LOW INPUT VOLTAGE NOISE: 1.2nV/$\sqrt{Hz}$
- VERY LOW DISTORTION: –100dBc (5MHz)
- HIGH SLEW RATE: 625V/µs
- HIGH DC ACCURACY: V_{IO} ±150µV
- LOW SUPPLY CURRENT: 12.6mA
- HIGH GAIN BANDWIDTH PRODUCT: 1750MHz
- STABLE FOR GAINS ≥ 7

APPLICATIONS

- HIGH DYNAMIC RANGE ADC PREAMPS
- LOW-NOISE, WIDEBAND, TRANSIMPEDANCE AMPLIFIERS
- WIDEBAND, HIGH GAIN AMPLIFIERS
- LOW-NOISE DIFFERENTIAL RECEIVERS
- VDSL LINE RECEIVERS
- ULTRASOUND CHANNEL AMPLIFIERS
- SECURITY SENSOR FRONT ENDS
- UPGRADE FOR THE OPA686, CLC425, AND LMH6624

DESCRIPTION

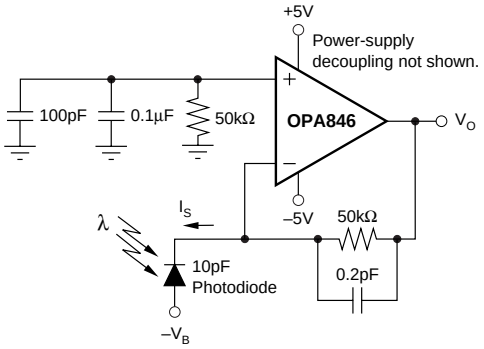
The OPA846 combines very high gain bandwidth and large signal performance with very low input voltage noise, while dissipating a low 12.6mA supply current. The classical differential input stage, along with two stages of forward gain and a high power output stage, combine to make the OPA846 an exceptionally low distortion amplifier with excellent DC accuracy and output drive. The voltage-feedback architecture allows all standard op amp applications to be implemented with very high performance.

The combination of low input voltage and current noise, along with a 1.75GHz gain bandwidth product, make the OPA846 an ideal amplifier for wideband transimpedance stages. As a voltage gain stage, the OPA846 is optimized for a flat response at a gain of +10 and is stable down to a gain of +7.

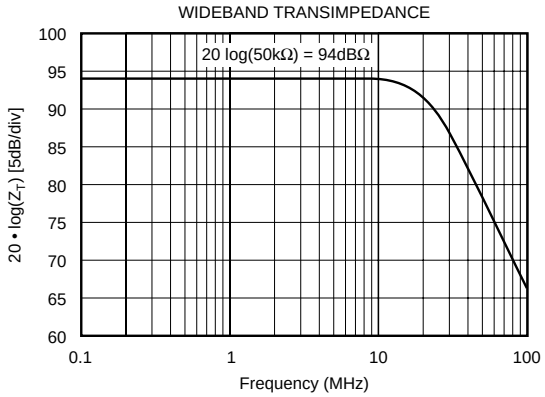
A new external compensation technique can be used to give a very flat frequency response below the minimum stable gain for the OPA846, further improving its already exceptional distortion performance. Using this compensation makes the OPA846 one of the premier 12- to 16-bit Analog-to-Digital (A/D) converter input drivers. The supply current for the OPA846 is precisely trimmed to 12.6mA at +25°C. This, along with carefully defined supply current tempco in the input and output stages, combine to provide exceptional performance over the full specified temperature range.

OPA846 RELATED PRODUCTS

SINGLES	INPUT NOISE VOLTAGE (nV/$\sqrt{Hz}$)	GAIN BANDWIDTH PRODUCT (MHz)
OPA842	2.4	200
OPA843	2.0	800
OPA847	0.85	3900



High Gain, 20MHz Transimpedance Amplifier



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Analysis Section
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: D, DBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Charge Device Model)	1500V
(Machine Model)	200V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

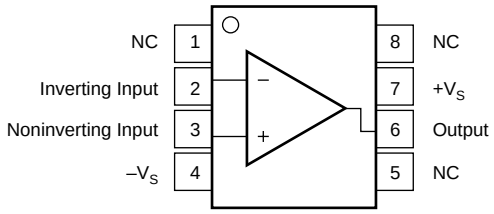
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA846	SO-8	D	–40°C to +85°C	OPA846	OPA846ID	Rails, 100
"	"	"	"	"	OPA846IDR	Tape and Reel, 2500
OPA846	SOT23-5	DBV	–40°C to +85°C	OASI	OPA846IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA846IDBVR	Tape and Reel, 3000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

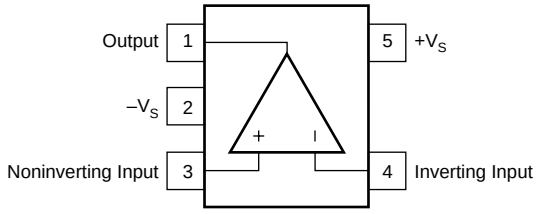
PIN CONFIGURATIONS

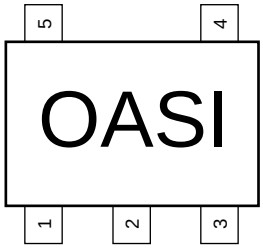
Top View **SO**



NC = No Connection

Top View **SOT23**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 453\Omega$, $R_L = 100\Omega$, and G = +10, unless otherwise noted. See Figure 1 for AC performance.

PARAMETER	CONDITIONS	OPA846ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 1)								
Closed-Loop Bandwidth	G = +7, $R_G = 50\Omega$, $V_O = 200mV_{PP}$	500				MHz	typ	C
	G = +10, $R_G = 50\Omega$, $V_O = 200mV_{PP}$	400	270	250	225	MHz	min	B
	G = +20, $R_G = 50\Omega$, $V_O = 200mV_{PP}$	110	82	80	75	MHz	min	B
Gain Bandwidth Product (GBP)	G ≥ +40	1750	1275	1245	1200	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +10, $R_L = 100\Omega$, $V_O = 200mV_{PP}$	140	40	36	35	MHz	min	B
Peaking at a Gain of +7						dB	typ	C
Harmonic Distortion	G = +10, f = 5MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–76	–70	–68	–66	dBc	max	B
	$R_L = 500\Omega$	–100	–89	–87	–85	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–109	–95	–92	–90	dBc	max	B
	$R_L = 500\Omega$	–112	–105	–101	–96	dBc	max	B
2-Tone, 3rd-Order Intercept	G = +10, f = 10MHz	44	41	40	38	dBm	min	B
Input Voltage Noise	f > 1MHz	1.2	1.3	1.4	1.5	$nV/\sqrt{Hz}$	max	B
Input Current Noise	f > 1MHz	2.8	3.5	3.6	3.6	$pA/\sqrt{Hz}$	max	B
Rise-and-Fall Time	0.2V Step	1.2	1.5	1.6	1.8	ns	max	B
Slew Rate	2V Step	625	500	425	350	V/µs	min	B
Settling Time to 0.01%	2V Step	15				ns	typ	C
0.1%	2V Step	10	12	14	16	ns	max	B
1%	2V Step	6	8	10	12	ns	max	B
Differential Gain	G = +10, NTSC, $R_L = 150\Omega$	0.02				%	typ	C
Differential Phase	G = +10, NTSC, $R_L = 150\Omega$	0.02				deg	typ	C
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	$V_O = 0V$	90	**82**	81	80	dB	min	A
Input Offset Voltage	$V_{CM} = 0V$	±0.15	**±0.60**	±0.68	±0.70	mV	max	A
Average Offset Voltage Drift	$V_{CM} = 0V$	±0.4	±1.5	±1.5	±1.5	µV/°C	max	B
Input Bias Current	$V_{CM} = 0V$	–10	**–19**	–19.8	–21	µA	max	A
Input Bias Current Drift	$V_{CM} = 0V$	±1	±20	±20	±35	nA/°C	max	B
Input Offset Current	$V_{CM} = 0V$	±0.1	**±0.35**	±0.45	±0.60	µA	max	A
Input Offset Current Drift	$V_{CM} = 0V$	±0.7	±2	±2	±3.5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±3.2	**±3.0**	±2.9	±2.8	V	min	A
Common-Mode Rejection (CMR)	$V_{CM} = \pm 1V$, Input Referred	110	**95**	93	90	dB	min	A
Input Impedance								
Differential-Mode	$V_{CM} = 0V$	6.6 || 2.0				kΩ || pF	typ	C
Common-Mode	$V_{CM} = 0V$	4.7 || 1.8				MΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	≥ 400Ω Load	±3.4	**±3.3**	±3.2	±3.1	V	min	A
	100Ω Load	±3.3	**±3.2**	±3.0	±2.9	V	min	A
Current Output, Sourcing	$V_O = 0V$	80	**65**	61	60	mA	min	A
Current Output, Sinking	$V_O = 0V$	–80	**–65**	–61	–60	mA	min	A
Closed-Loop Output Impedance	G = +10, f = 100kHz	0.002				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Maximum Quiescent Current	$V_S = \pm 5V$	12.6	**12.9**	13.0	13.2	mA	max	A
Minimum Quiescent Current	$V_S = \pm 5V$	12.6	**12.3**	12.1	11.8	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	$-V_S = -4.5$ to -5.5 (Input Referred)	95	**90**	88	85	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range: D, DBV Package		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT23-5		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C min/max specifications.

(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature min/max specifications.

(3) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

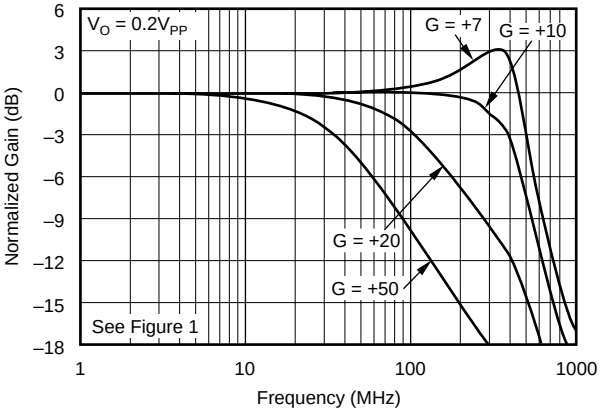
(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

(5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

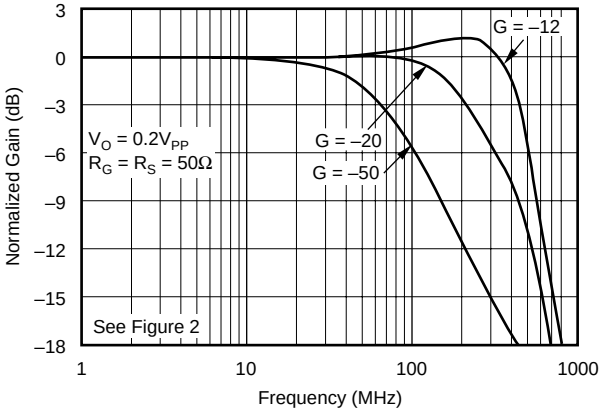
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = 25°C, G = +10, R_F = 453Ω, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted.

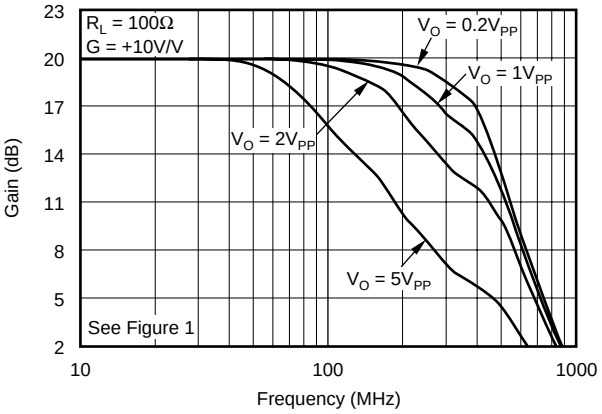
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



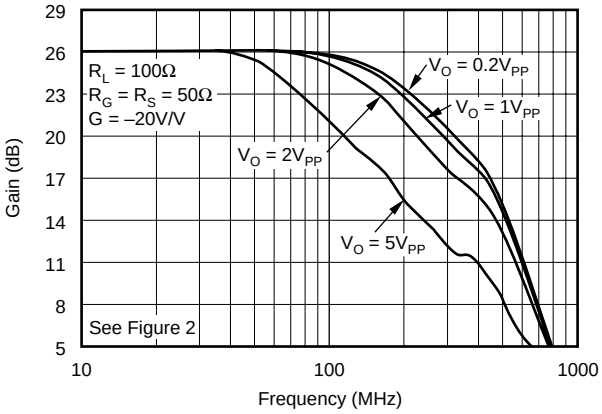
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



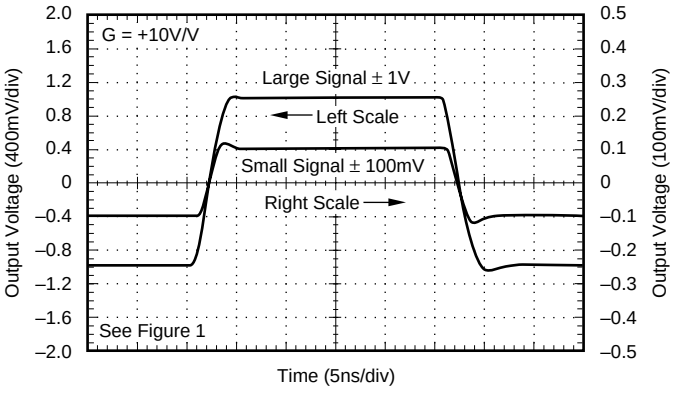
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



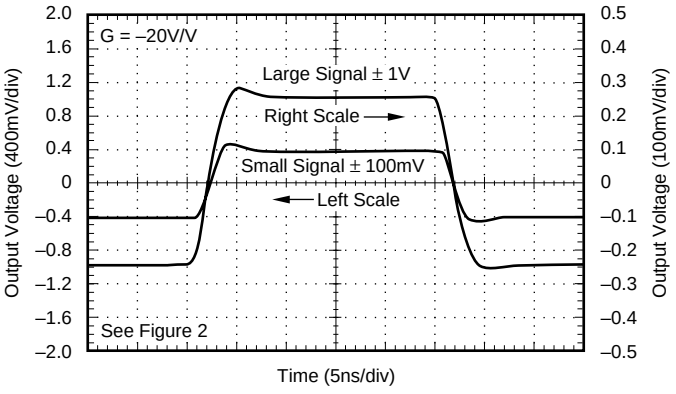
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



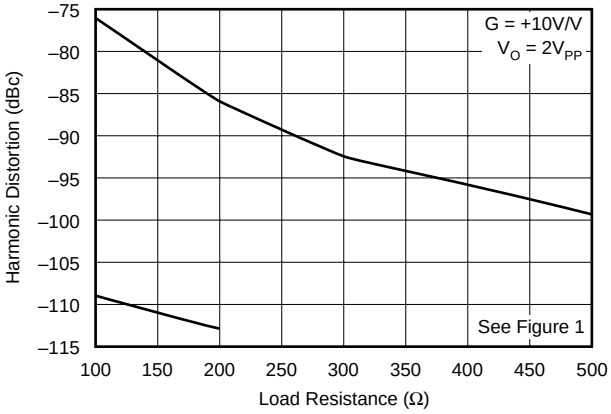
INVERTING PULSE RESPONSE



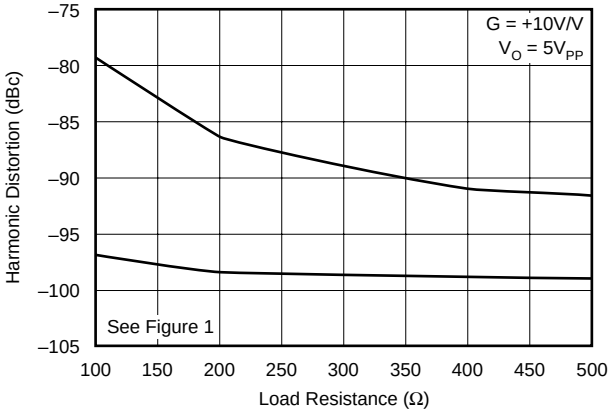
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = 25°C, G = +10, R_F = 453Ω, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted.

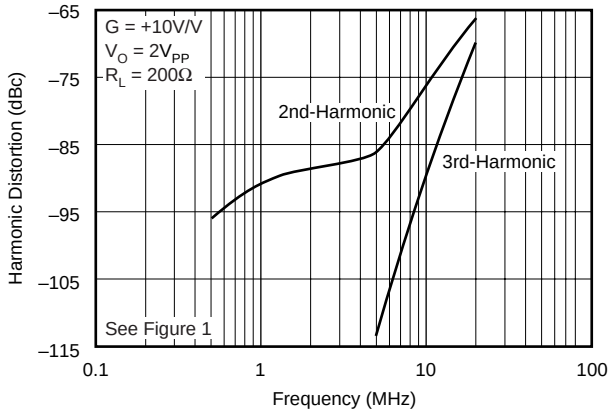
5MHz HARMONIC DISTORTION vs LOAD RESISTANCE



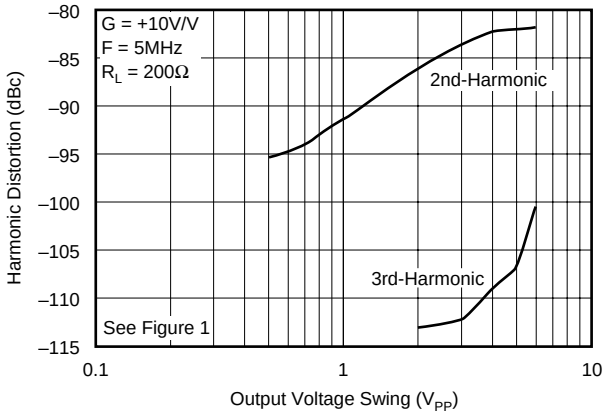
1MHz HARMONIC DISTORTION vs LOAD RESISTANCE



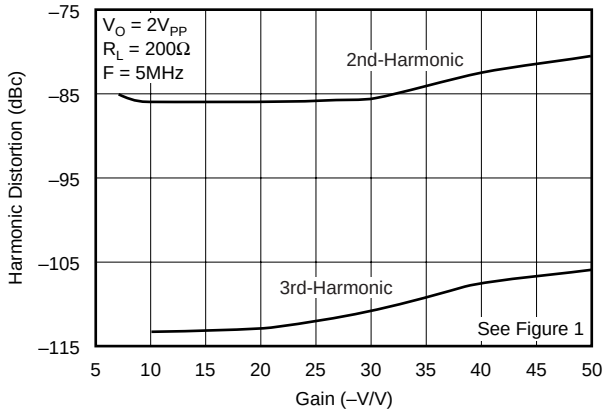
HARMONIC DISTORTION vs FREQUENCY



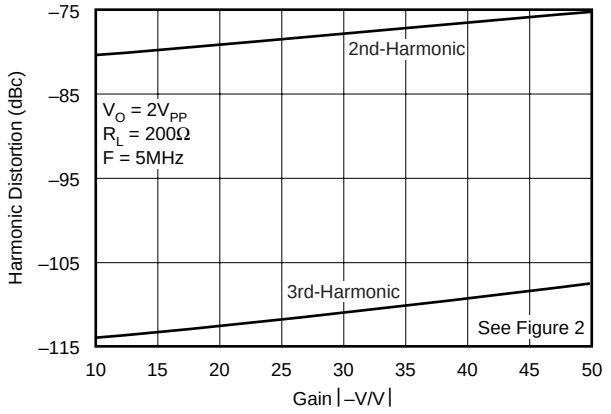
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



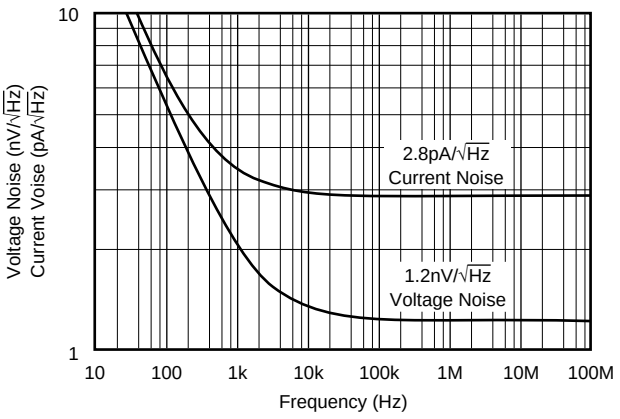
HARMONIC DISTORTION vs INVERTING GAIN



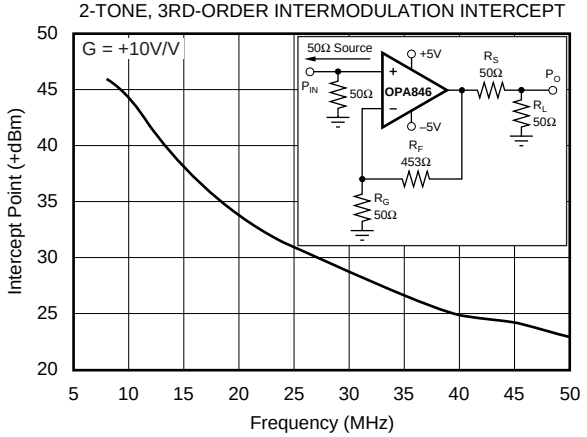
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = 25°C, G = +10, R_F = 453Ω, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted.

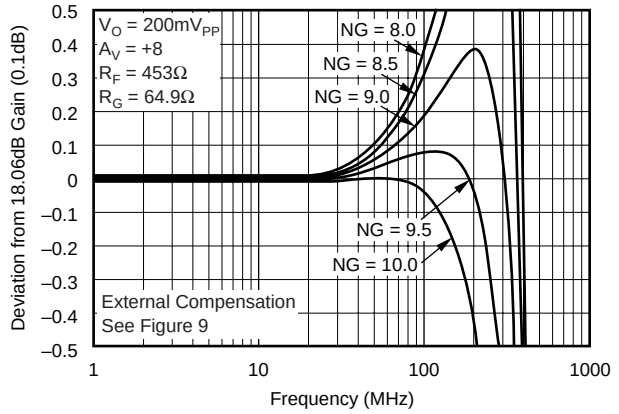
INPUT VOLTAGE AND CURRENT NOISE



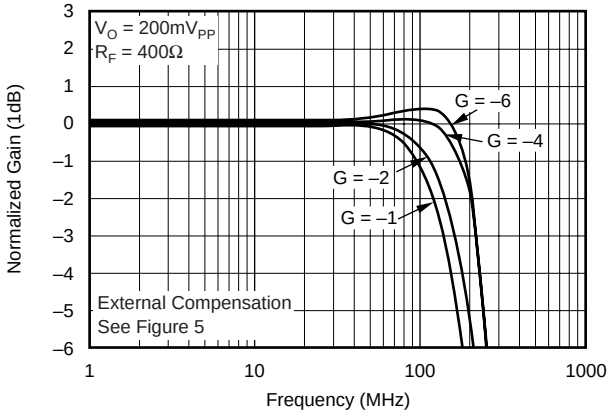
2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT



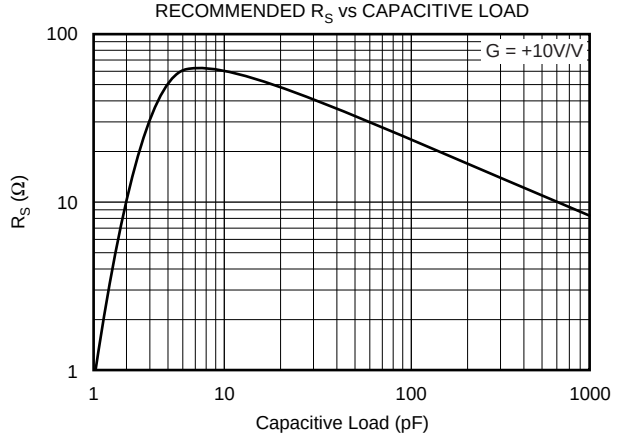
NONINVERTING GAIN FLATNESS TUNE



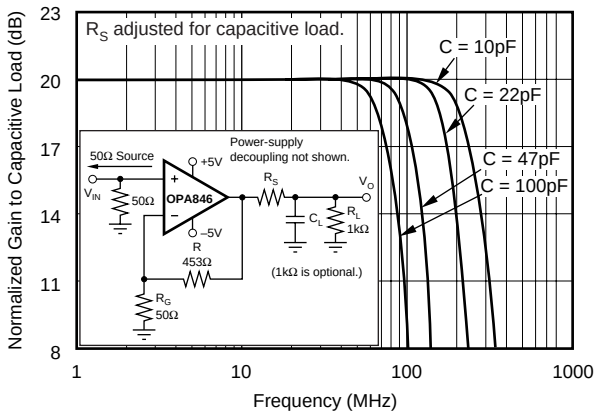
LOW GAIN INVERTING BANDWIDTH



RECOMMENDED R_S vs CAPACITIVE LOAD



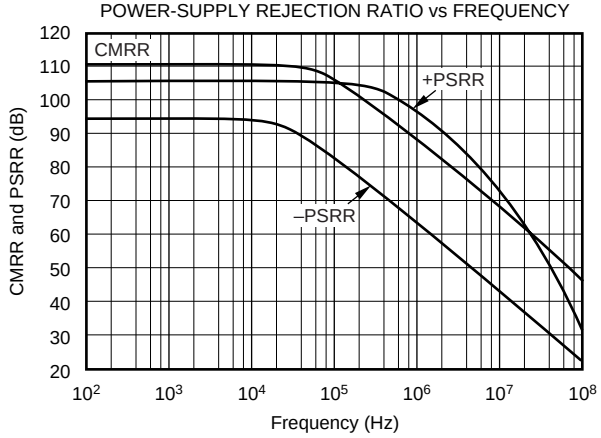
FREQUENCY RESPONSE vs CAPACITIVE LOAD



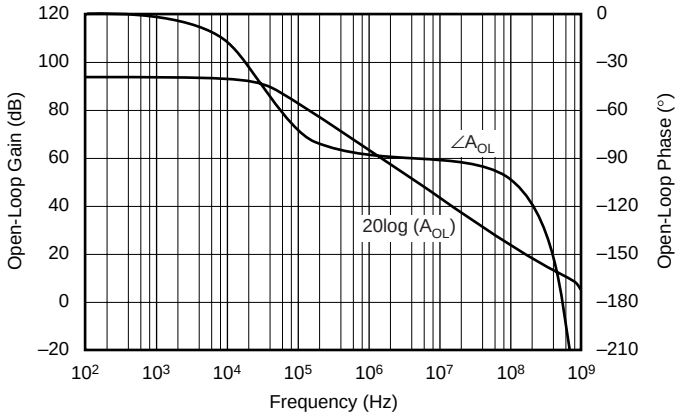
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = 25°C, G = +10, R_F = 453Ω, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted.

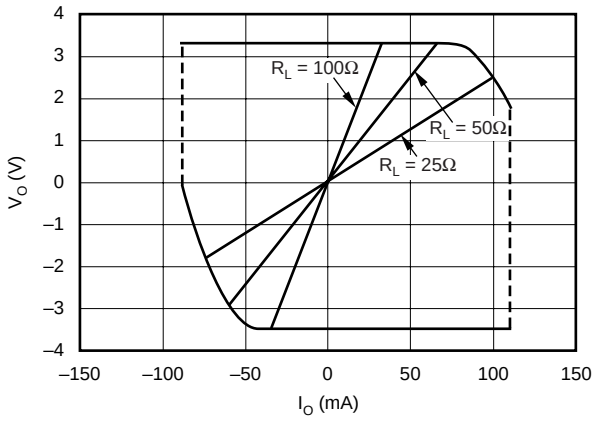
COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY



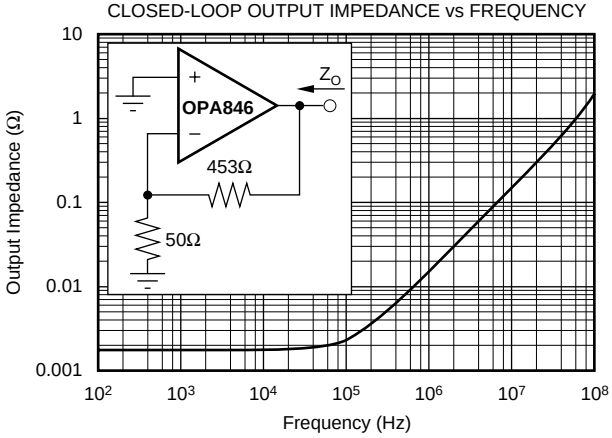
OPEN-LOOP GAIN AND PHASE



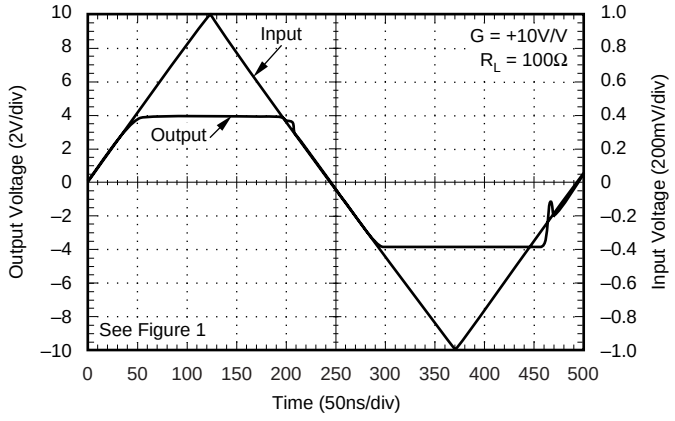
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



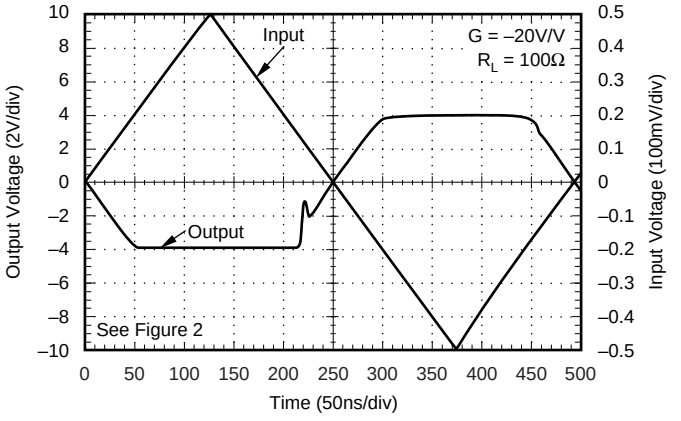
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



NONINVERTING OVERDRIVE RECOVERY



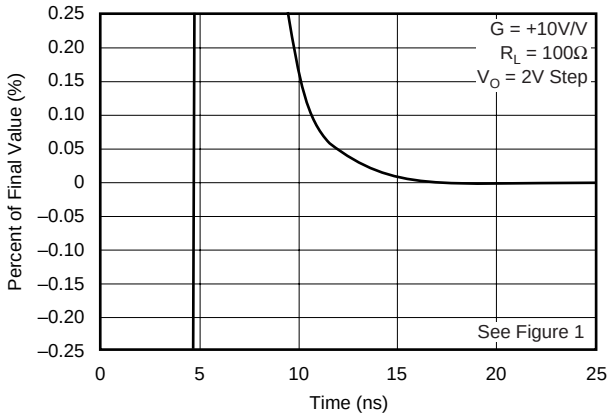
INVERTING OVERDRIVE RECOVERY



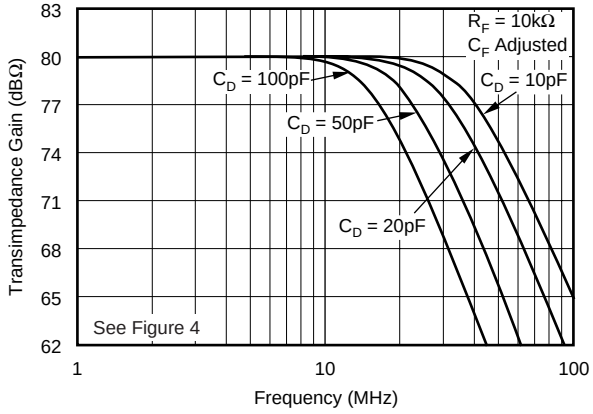
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = 25°C, G = +10, R_F = 453Ω, R_G = 50Ω, and R_L = 100Ω, unless otherwise noted.

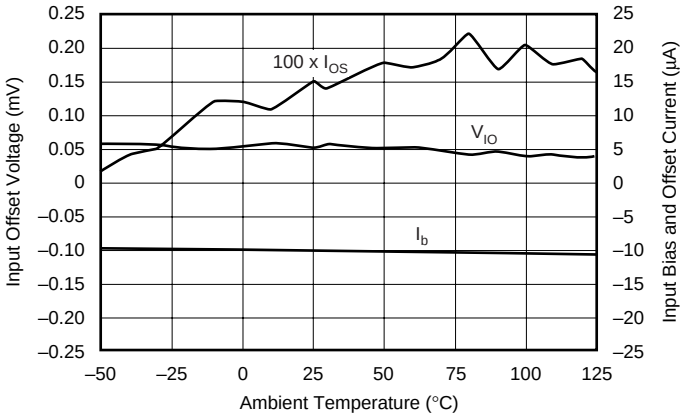
SETTLING TIME



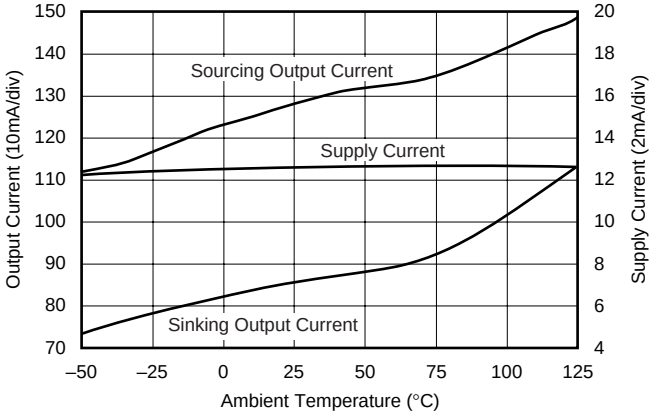
PHOTODIODE TRANSIMPEDANCE FREQUENCY RESPONSE



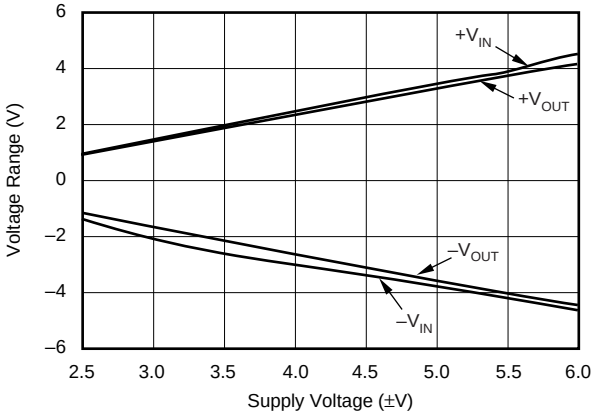
TYPICAL DC DRIFT OVER TEMPERATURE



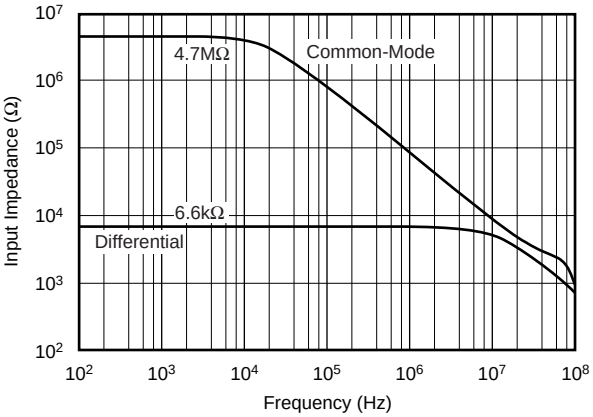
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



COMMON-MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



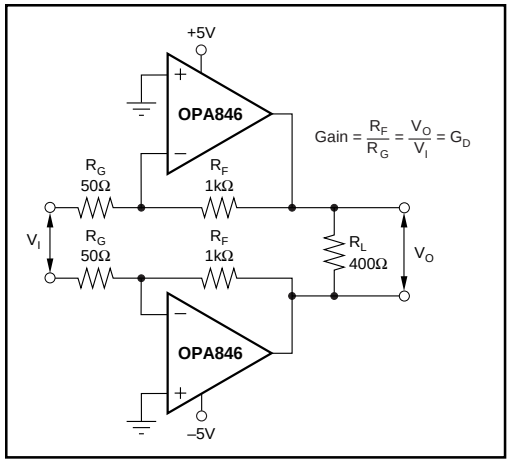
COMMON-MODE AND DIFFERENTIAL INPUT IMPEDANCE



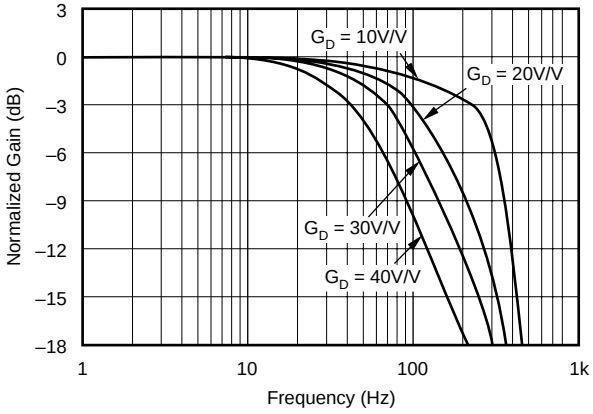
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = 25°C, G_D = 20, R_G = 50Ω, and R_L = 400Ω, unless otherwise noted.

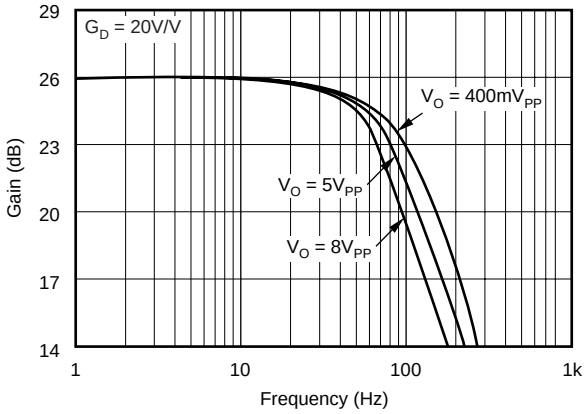
DIFFERENTIAL PERFORMANCE TEST CIRCUIT



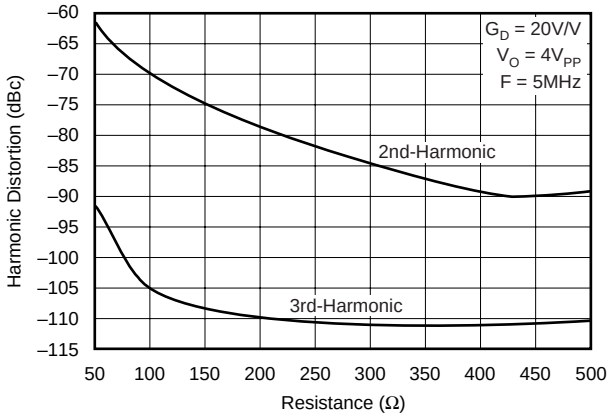
DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE



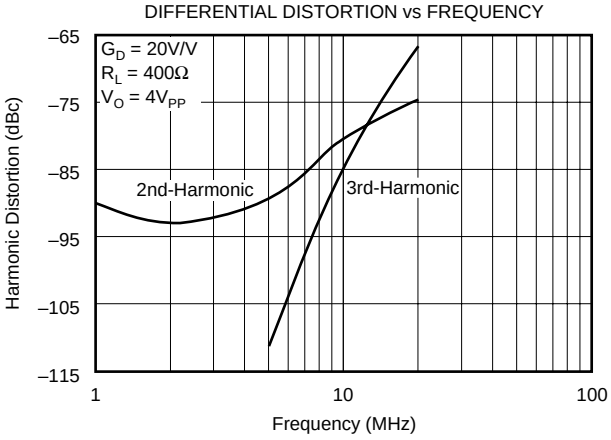
DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE



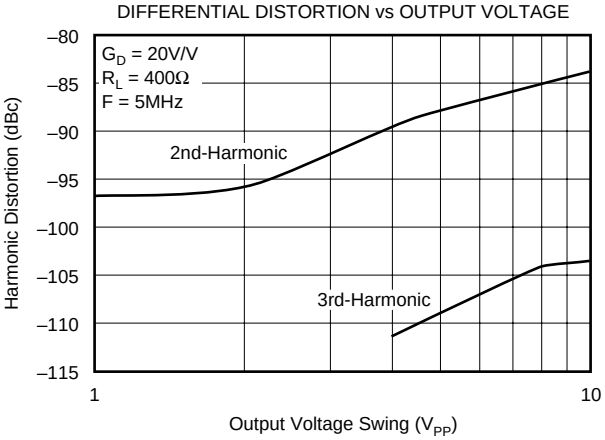
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND, NONINVERTING OPERATION

The OPA846 provides a unique combination of features. Low input voltage noise, along with a very low distortion output stage, gives one of the highest dynamic range op amps available. The very high Gain Bandwidth Product (GBP) can be used either to deliver high signal bandwidths at high gain, or to deliver very low distortion signals at moderate frequencies and lower gains. To achieve the full performance of the OPA846, careful attention to PC board layout and component selection is required, as discussed in the following sections of this data sheet.

Figure 1 shows the noninverting gain of a 10V/V circuit used as the basis of the Electrical Characteristics and most of the Typical Characteristic curves. Most of the curves are characterized using signal sources with a 50Ω driving impedance, and with a 50Ω load impedance presented by the measurement equipment. In Figure 1, the 50Ω resistor at the V_{IN} terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, the data sheet voltage swing specifications are at the output pin (V_O in Figure 1), while the output power (dBm) specifications are at the matched 50Ω load. The total 100Ω load at the output, combined with the 503Ω total feedback network load, presents the OPA846 with an effective output load of 83Ω for the circuit of Figure 1.

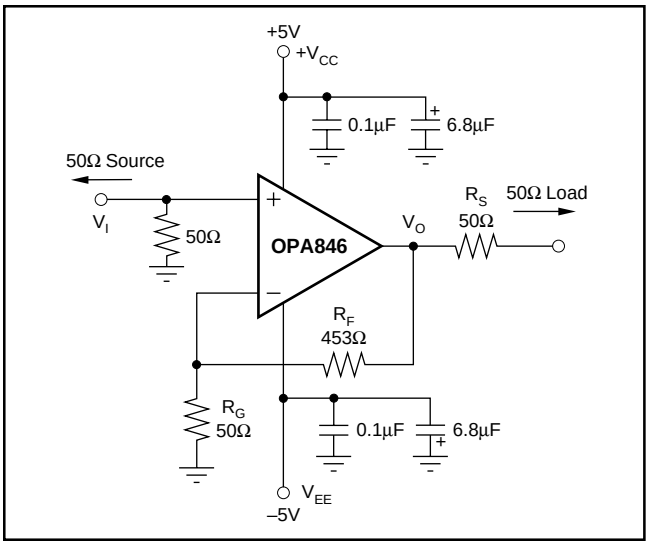


FIGURE 1. DC-Coupled, G = +10V/V, Bipolar Supply, Specification and Test Circuit.

Voltage-feedback op amps (unlike current-feedback designs) can use a wide range of resistor values to set the gain, although these resistors usually have low values to maintain a low total output noise. The circuit of Figure 1, and the specifications at other gains, use the constraint that R_G be set to 50Ω and R_F adjusted to get the desired gain. Using this guideline ensures that the noise added at the output due to the Johnson noise of the resistors does not significantly increase the total noise over that due to the 1.2nV/$\sqrt{Hz}$ input voltage noise for the op amp. Higher resistor values can certainly be used where the application requires it, but can start to add significantly to the output noise power as described in the Setting Resistor Values to Minimize Noise section.

WIDEBAND INVERTING GAIN OPERATION

Operating the OPA846 as an inverting amplifier has several benefits and is particularly appropriate when a matched input impedance is required. Figure 2 shows the inverting gain circuit used as the basis of the inverting mode of the Typical Characteristic curves.

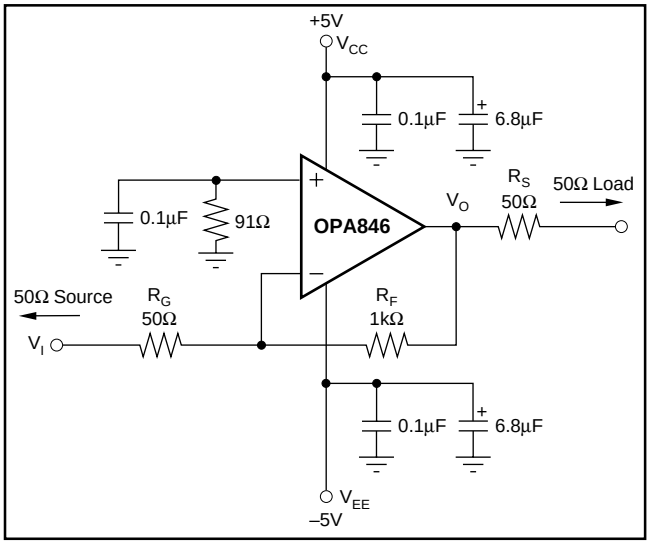


FIGURE 2. DC-Coupled, G = –20V/V, Bipolar Supply, Specification and Test Circuit.

Driving this circuit from a 50Ω source, and constraining the gain resistor (R_G) to equal 50Ω, gives both a signal bandwidth and noise advantage. R_G acts as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain (V_O/V_I) for the circuit of Figure 2 is double that for Figure 1, the noise gains are in fact equal when the 50Ω source resistor is included. This has the interesting effect of doubling the equivalent GBP of the amplifier. This can be seen by observing the 200MHz bandwidth for the inverting gain of –20. This implies a GBP of 4GHz, when in fact this extended bandwidth is given by the reduced noise gain when the matched source resistor is included. If the signal source is actually the low impedance output of another amplifier, R_G is increased to the minimum load resistance value allowed for that amplifier and R_F is then adjusted to achieve the desired gain. For stable operation of the OPA846, it is critical that this driving amplifier show very low output impedance at frequencies beyond the expected closed-loop bandwidth for the OPA846.

WIDEBAND, HIGH-SENSITIVITY TRANSIMPEDANCE DESIGN

The high GBP and low input voltage and current noise for the OPA846 make it an ideal wideband transimpedance amplifier. Very high transimpedance gains (> 100kΩ) benefit from the low input noise current of a JFET-input op amp, such as the OPA657. Unity-gain stability in the op amp is not required for application as a transimpedance amplifier. One transimpedance design example is shown on the front page of this data sheet. Designs that require high bandwidths from a large area (high capacitance) detector with relatively low transimpedance gain will benefit from the low input voltage noise offered by the OPA846. This input voltage noise is peaked up over frequency at the output by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements of the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain (R_F), and the GBP of the OPA846 (1750MHz). Figure 3 shows a design using a 50pF detector diode capacitance and a 10kΩ transimpedance gain. With these three variables set (including the parasitic input capacitance for the OPA846 added to C_D) the feedback capacitor (C_F) value can be set to control the frequency response. To achieve a maximally flat 2nd-order Butterworth frequency response, set the feedback pole as shown in Equation 1.

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \qquad (1)$$

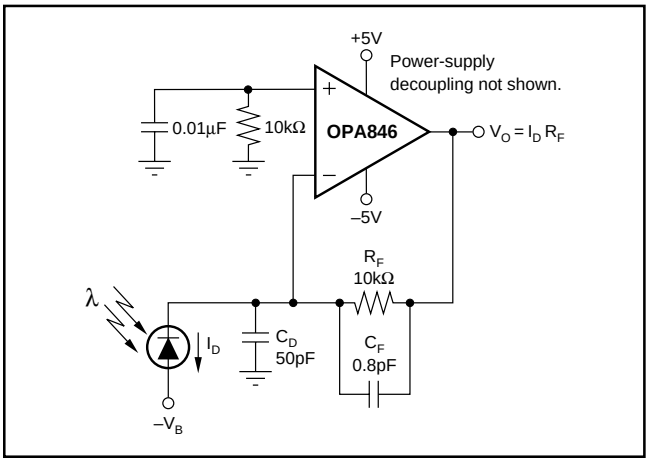


FIGURE 3. Wideband, Low Noise, Transimpedance Amplifier.

Adding the common-mode and differential-mode input capacitance (1.8 + 2.0)pF to the 50pF diode source capacitance of Figure 3, with a 10kΩ transimpedance gain using the 1750MHz GBP for the OPA846, requires a feedback pole set to 16.1MHz. This requires a 1pF total feedback capacitance. Typical surface-mount resistors have 0.2pF parasitic capacitance leaving a required extrinsic 0.8pF value, as shown in Figure 3. Equation 2 gives the approximate –3dB bandwidth, if C_F is set using Equation 1.

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} (Hz) \qquad (2)$$

The example of Figure 3 gives approximately 23MHz flat bandwidth using the 0.8pF feedback compensation. If the total output noise is bandlimited to a frequency less than the feedback pole frequency, a simple expression for the equivalent input noise current is given as Equation 3.

$$I_{EQ} = \sqrt{I_N^2 + \frac{4kT}{R_F} + \left(\frac{E_N}{R_F}\right)^2 + \frac{(E_N 2\pi F C_D)^2}{3}} \qquad (3)$$

Where:

I_{EQ} = equivalent input noise current if the output noise is bandlimited to $F < 1/(2\pi R_F C_F)$

I_N = input current noise for the op amp inverting input

E_N = input voltage noise for the op amp

C_D = diode capacitance

F = bandlimiting frequency in Hz (usually a post filter prior to further signal processing)

4kT = 1.6E – 20J at T = 290K

Evaluating this expression up to the feedback pole frequency at 16.1MHz for the circuit of Figure 3 gives an equivalent input noise current of 4.9pA/$\sqrt{Hz}$. This is much higher than the 2.8pA/$\sqrt{Hz}$ for just the op amp. This result is dominated by the last term in the equivalent input noise current calculation from Equation 3. It is essential in this case to use a low-voltage noise op amp. For example, if a slightly higher input noise voltage, but otherwise identical op amp, was used instead of the OPA846 amplifier in this application noise amplifier (say 2.0nV/$\sqrt{Hz}$), the total input-referred current noise would increase to 7.0pA/$\sqrt{Hz}$.

The output DC error for the circuit of Figure 3 is minimized by including the 10kΩ to ground on the noninverting input. This reduces the impact at the output of input bias current errors to the offset current times the feedback resistor. To minimize the output noise contribution of this resistor, a 0.01µF capacitor is included in parallel. Worst-case output DC error for the circuit of Figure 3 at 25°C is:

V_{OS} = ±0.6mV (input offset voltage) ± 0.35µA (input offset current) • 10kΩ = ±4.1mV

Worst-case output offset DC drift is over the 0°C to 70°C span is dV_{OS}/dT = ±1.5µV/°C (input offset drift) ± 2nA/C (input offset current drift) • 10kΩ = ±21.5µV/°C

Improved output DC precision and drift is possible, particularly at higher transimpedance gains, using the JFET input of the OPA657. The JFET input removes the input bias current from the error equation (eliminating the need for the resistor to ground on the noninverting input), leaving only the input offset voltage and drift as an output error term.

Included in the characteristic curves are transimpedance frequency response curves for a fixed 10kΩ gain over various detector diode capacitance settings. These curves, along with the test circuit, are repeated in Figure 4. As the photo-

diode capacitance changes, the feedback capacitor must change to maintain a stable and flat frequency response. Using Equation 1, C_F is adjusted to give the Butterworth frequency responses presented in Figure 4.

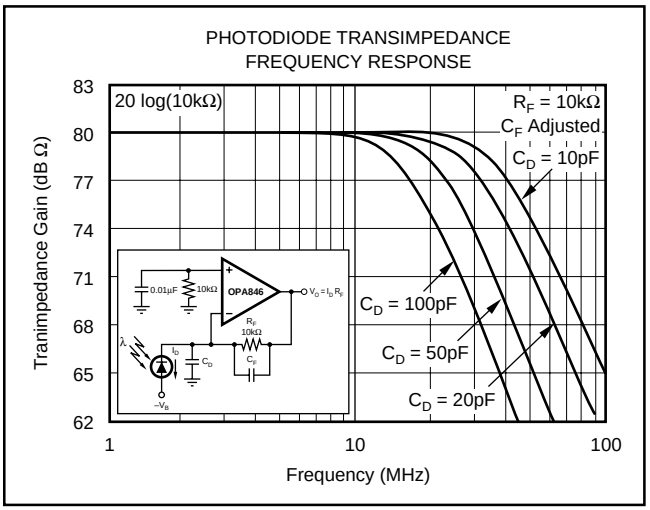


FIGURE 4. Transimpedance Bandwidth versus C_D.

LOW-GAIN COMPENSATION FOR IMPROVED SFDR

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique may be used to retain the full slew rate and noise benefits of the OPA846, while giving increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the loop gain for good stability, while giving an easily controlled 2nd-order low-pass frequency response. Considering only the noise gain (noninverting signal gain) for the circuit of Figure 5, the low-frequency noise gain (NG_1) is set by the resistor ratios, while the high-frequency noise gain (NG_2) is set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain (determined by $NG_2 = 1 + C_S/C_F$) is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole (set by $1/R_FC_F$) is placed correctly, a very well controlled, 2nd-order, low-pass frequency response results.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain (NG_2), which should be greater than the minimum stable gain for the OPA846. Here, a target NG_2 of 10.5 is used. The second parameter is the desired low-frequency signal gain $-(R_F/R_G)$, which also sets the low-frequency noise gain NG_1 (= $1 + R_F/R_G$). To simplify this discussion, target a maximally flat 2nd-order, low-pass Butterworth frequency response (Q = 0.707). The signal gain of –2 shown in Figure 5 sets the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 3 in this example). Then, using only these two gains and the GBP for the OPA846 (1750MHz), the key frequency in the compensation can be determined as:

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right] \qquad (4)$$

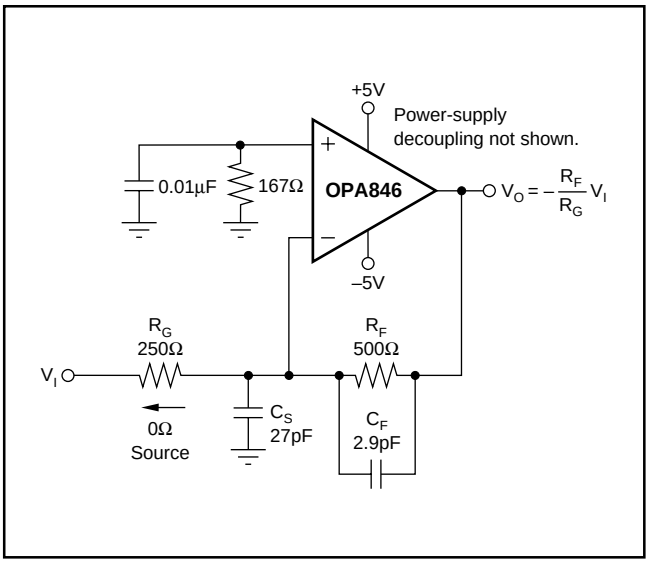


FIGURE 5. Broadband, Low-Gain, Inverting Amplifier.

Physically, this Z_O (11.6MHz for these values) is set by:

$$\frac{1}{2\pi R_F\left(C_F + C_S\right)}$$

and is the frequency at which the rising portion of the noise gain would intersect the unity gain if projected back to a 0dB gain. The actual zero in the noise gain occurs at $NG_1 \bullet Z_O$, and the pole in the noise gain occurs at $NG_2 \bullet Z_O$. Since GBP is expressed in Hz, multiply Z_O by 2π, and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi R_F Z_O NG_2}\left(= 2.86\text{pF}\right) \qquad (5)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S by using NG_2 = 10.5:

$$C_S = \left(NG_2 - 1\right)C_F, \text{ which gives } C_S = 24.9\text{pF} \qquad (6)$$

The resulting closed-loop bandwidth is approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_O \bullet GBP} \qquad (7)$$

For the values of Figure 5, f_{-3dB} is approximately 142MHz. This is less than that predicted by dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value, while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_O$. The capacitor values shown in Figure 5 are calculated for NG_1 = 3 and NG_2 = 10.5 with no adjustment for parasitic components.

See Figure 6 for the measured frequency response for the circuit of Figure 5. This shows the expected gain of –2 (6dB) with exceptional flatness through 70MHz and a –3dB bandwidth of 170MHz. Repeating the swept frequency distortion measurement for a $2V_{PP}$ output into a 200Ω load and comparing to the gain of +10 data shown in the Typical Characteristic curves illustrates the improved distortion for this low-gain compensation circuit.

Figure 7 compares the distortion at a gain of +10 for the circuit of Figure 1 to the distortion at a gain of –2 for the circuit of Figure 5.

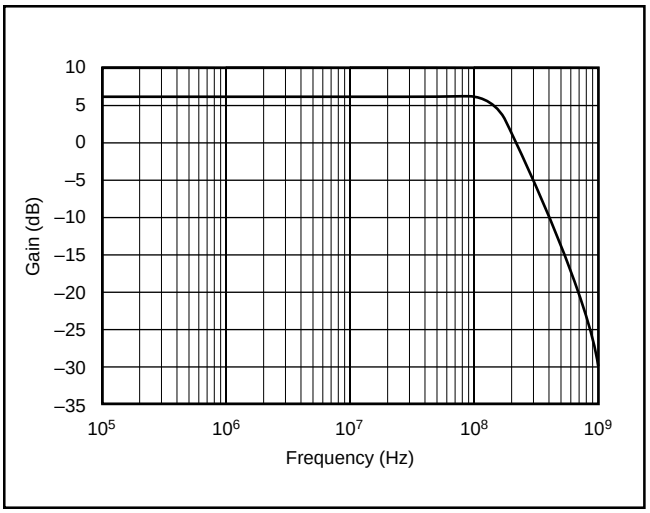


FIGURE 6. Gain of –2 Frequency Response Using External Compensation.

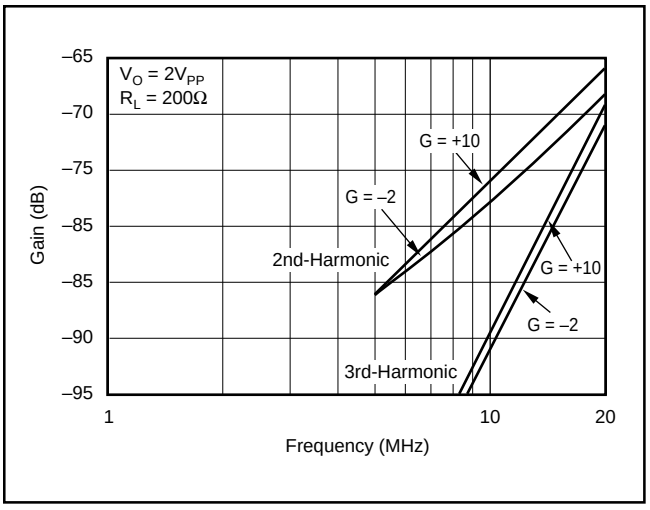


FIGURE 7. Distortion Comparison at G = +10 versus G = –2.

LOW-NOISE FIGURE, HIGH DYNAMIC RANGE IF AMPLIFIER

The low input noise voltage of the OPA846, and its high 2-tone, 3rd-order intercept, can be used to good advantage as a fixed-gain IF amplifier. While input noise figures in the 10dB range (for a matched 50Ω input) are easily achieved with just the OPA846 alone, Figure 8 shows a technique that reduces the noise figure even further, while providing a broadband, moderate-gain IF amplifier stage using the OPA846.

Bringing the signal in through a step-up transformer to the inverting input gain resistor has several advantages for the OPA846. First, grounding the noninverting input eliminates the contribution of the noninverting input current noise to the output noise. Second, the noninverting input voltage noise of the op amp is actually attenuated if reflected to the input side of R_G. Using the 1:2 (turns ratio) step-up transformer reflects the 50Ω source impedance at the primary through to the secondary as a 200Ω source impedance. The 200Ω R_G resistor is reflected through to the transformer primary as a 50Ω input matching impedance. The noninverting signal gain (noise gain, NG) to the amplifier output is then 1 + 1000/400 = 3.5V/V. Taking the input voltage noise (1.2nV/$\sqrt{Hz}$) for the OPA846 times this noise gain to the output, then reflecting this noise term to the input side of the R_G resistor, divides it by 5. This gives a net gain of 0.7 for the noninverting input voltage noise when reflected to the input point for the op amp circuit. This term is further reduced when referred back to the transformer input.

The 14dB gain to the matched load, for the circuit of Figure 8, is precisely controlled (±0.2dB) and gives a 6dB noise figure at the input of the transformer. The DC noise gain for this circuit (3.5) is below the specified minimum stable gain. The amplifier portion of the circuit uses the low-gain inverting compensation described in the previous section. Measured results show 140MHz small-signal bandwidth for the circuit of Figure 8 with ±0.1dB flatness through 50MHz. The OPA846 easily delivers a $2V_{PP}$ A/D converter full-scale input at the matched 50Ω load. 2-tone testing at 20MHz for the circuit of Figure 8 ($1V_{PP}$ for each test tone) shows that the 2-tone intermodulation intercept has improved to 40dBm versus the 34dBm shown in the Typical Characteristic curves, giving a 72dBc SFDR for the two 4dBm test tones at the load. This high SFDR comes with relatively low total power dissipation versus fixed-gain IF amplifier alternatives. Significantly higher SFDR is delivered at lower frequencies and/or for the lighter loads driving A/D converter inputs directly.

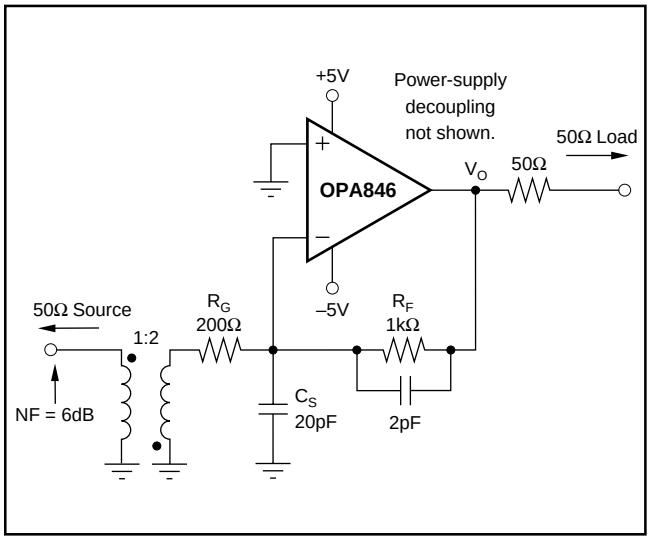


FIGURE 8. Low-Noise Figure IF Amplifier.

NONINVERTING LOW-GAIN COMPENSATION

Decreasing the operating gain for the OPA846 from the nominal design point of +10 decreases the phase margin. This increases Q for the closed-loop poles, peaks up the frequency response, and extends the bandwidth. A peaked frequency response shows overshoot and ringing in the pulse response, as well as a higher integrated output noise. When operating the amplifier at a noise gain less than +7, increased peaking and possible sustained oscillations may

result. However, operation at low gains may be desirable to take advantage of the higher slew rate and exceptional DC precision of the OPA846. Numerous external compensation techniques are suggested for operating a high-gain op amp at low gains. Most of these give zero/pole pairs in the closed-loop response that cause long term settling tails in the pulse response and/or phase nonlinearity in the frequency response. Figure 9 shows an external compensation method for a noninverting configuration that does not suffer from these drawbacks.

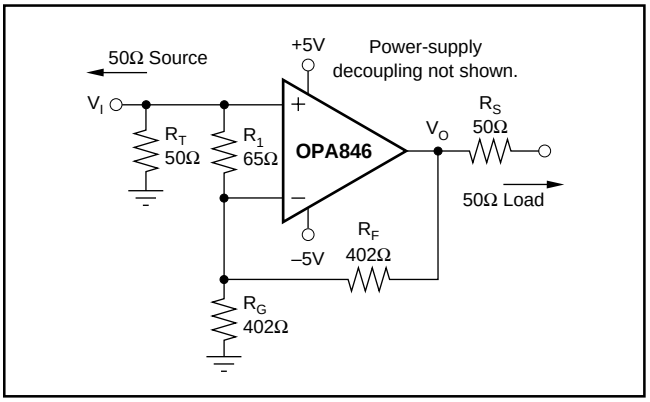


FIGURE 9. Noninverting Low-Gain Compensation.

The R_1 resistor across the two inputs increases the noise gain (i.e., decreases the loop gain) without changing the signal gain. This approach retains the full slew rate to the output but gives up some of the low-noise benefit of the OPA846. Assuming a low source impedance is used, set R_1 so that $1 + R_F /(R_G \parallel R_1)$ is > 7. This approach may also be used to tune the flatness by adjusting R_1. The Typical Characteristic curves show a signal gain of +8 with the noise gain adjusted for flatness using different values for R_1. Figure 10 shows the measured frequency response for the circuit of Figure 9 showing the flat frequency response possible with this compensation.

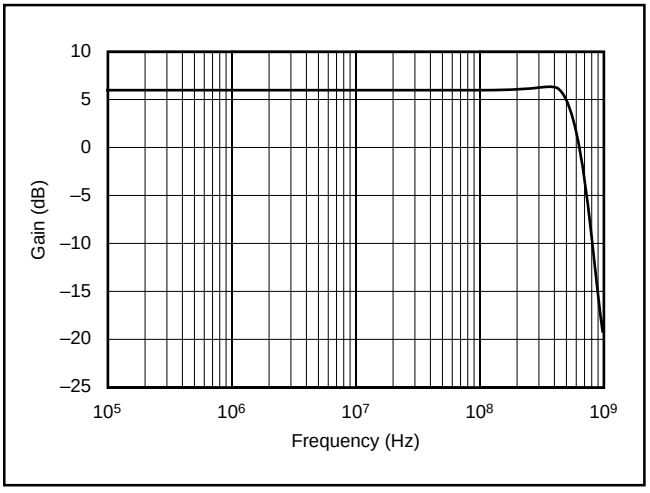


FIGURE 10. Noninverting Gain of +2 Response Using External Compensation.

DIFFERENTIAL OPERATION

Operating two OPA846 amplifiers in a differential inverting configuration can further suppress even-order harmonic terms. The Typical Characteristic curves show measured performance for this condition. For the distortion data, the output swing is increased to $4V_{PP}$ into 400Ω to allow direct comparison to the $2V_{PP}$ into 200Ω data for single-channel operation. Figure 11 shows the swept frequency 2nd- and 3rd-harmonic distortion for an inverting differential configuration, where each channel is set up for a gain of 20.

Comparing this to the single-channel distortion (at 10MHz for instance), about the same 3rd-harmonic and about a 5dB improvement in the 2nd-harmonic is shown.

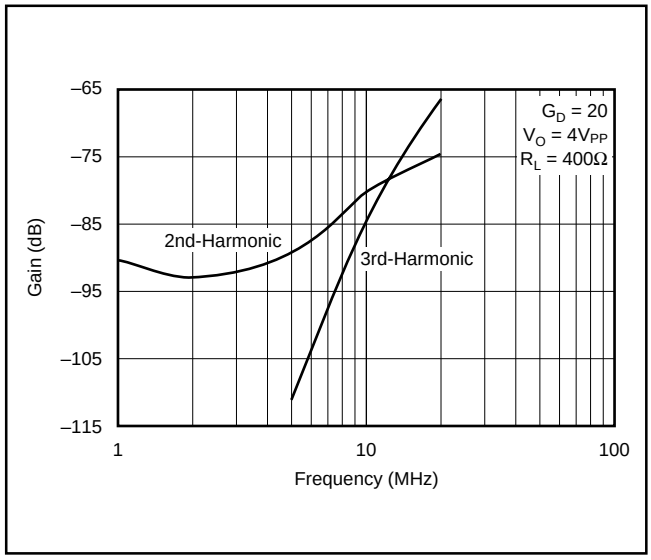


FIGURE 11. Differential Distortion vs Frequency.

SINGLE-SUPPLY OPERATION

The OPA846 may be operated from a single power supply if system constraints require it. Operation from a single +5V to +12V supply is possible with minimal change in AC performance. The Typical Characteristics show the input and output voltage ranges for a bipolar supply range from ±2.5V to ±6V. The Common-Mode Input Range and Output Swing vs Supply Voltage plot shows that the required headroom on both the input and output nodes remains at approximately 1.5V over this entire range. On a single +5V supply for instance, this means the noninverting input should remain centered at 2.5V ±1V, as should the output pin. See Figure 12 for an example application biasing the noninverting input at mid-supply and running an AC-coupled input to the inverting gain path. Since the gain resistor is blocked off for DC, the bias point on the noninverting input appears at the output, centering up that node, as well on the power supply. The OPA846 can support this mode of operation down to a single +5V supply and up to a single +12V supply.

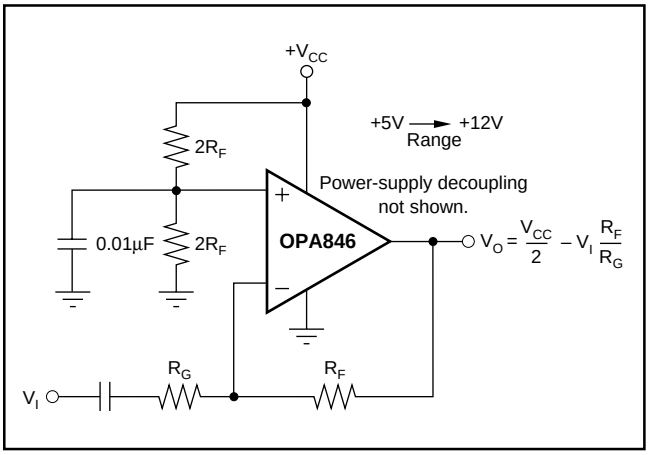


FIGURE 12. Single-Supply Inverting Amplifier.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA846 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA846ID	SO-8	DEM-OPA-SO-1B	SBOU026
OPA846IDBV	SOT23-5	DEM-OPA-SOT-1B	SBOU027

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA846 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA846 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA846 is available through the TI web page (www.ti.com). These models predict typical small-signal AC, transient steps, and DC performance under a wide variety of operating conditions. The models include the noise terms found in the electrical specification of this data sheet. These models do not attempt to distinguish between the package types in small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA846 provides a very low input noise voltage while requiring a low 12.6mA quiescent current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 13 shows the op amp noise analysis model with all the noise terms included. In this model, all the terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

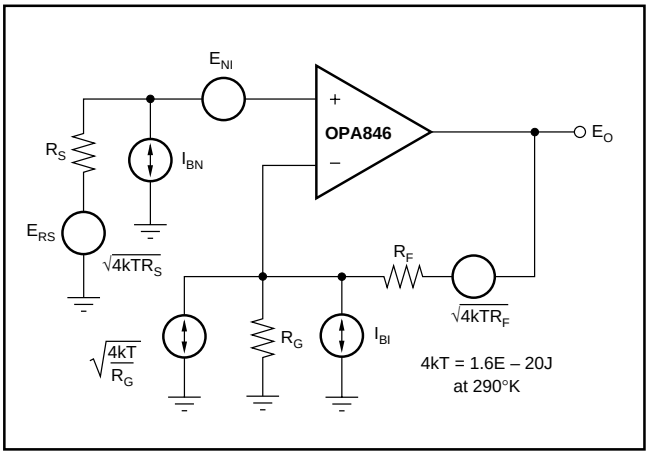


FIGURE 13. Op Amp Noise Analysis Model.

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition and then takes the square root of the terms to get back to a spot noise voltage. Equation 8 shows the general form for this output noise voltage using the terms of Figure 13.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_F NG} \qquad (8)$$

Dividing this expression by the noise gain (NG = 1 + R_F/R_G) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 9.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \qquad (9)$$

Setting high resistor values into Equation 9 can quickly dominate the total equivalent input referred noise. A 90Ω source impedance on the noninverting input adds a Johnson voltage noise term equal to that of the amplifier. As a simplifying constraint, set $R_G = R_S$ in Equation 9 and assume an $R_S/2$ source impedance is at the noninverting input (where R_S is the signal source impedance with another matching R_S to ground on the noninverting input). This results in Equation 10, where NG > 10 is assumed to further simplify the expression.

$$E_N = \sqrt{E_{NI}^2 + \frac{5}{4}(I_B R_S)^2 + 4kT\left(\frac{3R_S}{2}\right)} \qquad (10)$$

Evaluating this expression for R_S = 50Ω gives a total equivalent input noise of 1.7nV/$\sqrt{Hz}$. Note that the NG has dropped out of this expression.

This is valid only for NG > 10 as will typically be required by stability considerations.

FREQUENCY RESPONSE CONTROL

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factor), most high-speed amplifiers exhibit a more complex response with lower phase margin. The OPA846 is compensated to give a maximally flat 2nd-order Butterworth closed-loop response at a noninverting gain of +10 (see Figure 1). This results in a typical gain of +10 bandwidth of 400MHz, far exceeding that predicted by dividing the 1750MHz GBP by 10. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +50, the OPA846 shows the 35MHz bandwidth predicted using the simple formula F_{-3dB} = GBP/NG.

Inverting operation offers some interesting opportunities to increase the available GBP. When the source impedance is matched by the gain resistor (see Figure 2), the signal gain is ($-R_F/R_G$), while the noise gain for bandwidth purposes is ($1 + R_F/2R_G$). This cuts the noise gain almost in half, increasing the minimum stable gain for inverting operation under these conditions to –12V/V and increases the equivalent GBP to > 3.5GHz.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often the capacitive load is the input of an A/D converter, including additional external capacitance that may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the OPA846 is susceptible to decreasing stability with capacitive loads and results in closed-loop response peaking when a capacitive load is placed directly on the amplifier output pin. If the primary considerations are frequency response flatness, pulse fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristic curves help the designer pick a recommended R_S versus Capacitive Load. The resulting frequency response curves show the flat response for a given capacitive load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA846. Long PC board traces, unmatched cables, and connections to multiple devices can easily add additional capacitance to the existing circuit. Always consider these effects carefully and add the recommended series resistor as close to the output pin of the OPA846 as possible (see the Board Layout section).

The criterion for setting the R_S resistor for maximum bandwidth, flat frequency response at the load is a simple procedure. For the OPA846 operating in a gain of +10V/V, the frequency response at the output pin is very flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads. As the signal gain increases, the unloaded phase margin also increases. Driving capacitive loads at higher gain settings require lower R_S values than those shown for a gain of +10V/V.

DISTORTION PERFORMANCE

The OPA846 is capable of delivering an exceptionally low distortion signal at high frequencies over a wide range of gains. The distortion plots found in the Typical Characteristic curves show the typical distortion under a wide variety of conditions. Most of these plots are limited to 110dB dynamic range. The OPA846 distortion, while driving a 500Ω load, does not rise above –90dBc until either the signal level exceeds $2.0V_{PP}$ and/or the fundamental frequency exceeds 5MHz. Distortion in the audio band is < –120dBc.

Generally, until the fundamental signal reaches very high frequencies or power, the 2nd-harmonic dominates the distortion with negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network: in the noninverting configuration, this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F (see Figures 1 and 2). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing generally increases the 2nd-harmonic to 12dB and the 3rd-harmonic to 18dB. Increasing the signal gain also increases the 2nd-harmonic distortion. Again, a 6dB increase in gain increases the 2nd- and 3rd-harmonic by approximately 6dB, even with constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases, due to the roll-off in the loop gain with frequency. Conversely, the distortion improves going to lower frequencies down to the dominant open-loop pole at approximately 100kHz. Starting from the –86dBc 2nd-harmonic for a 5MHz, $2V_{PP}$ fundamental into a 200Ω load at a gain = +10V/V (from the Typical Characteristic curves), the 2nd-harmonic distortion for frequencies lower than 100KHz is approximately –86dBc – 20 log(5MHz/100kHz) = –120dBc.

The OPA846 has extremely low 3rd-order distortion. This also gives a high 2-tone, 3rd-order intermodulation intercept, as shown in the Typical Characteristic curves. This intercept curve is defined at the 50Ω load when driven through a 50Ω-matching resistor to allow direct comparisons to R_F devices. This matching network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA846 drives directly into the input of a high-impedance device, such as an A/D converter, the 6dB attenuation is not present. Under these conditions, the intercept increases by a minimum of 6dBm. The intercept is used to predict the intermodulation spurious for two closely-spaced frequencies. If the two test frequencies f_1 and f_2 are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta f = |f_2 - f_1|/2$, the two 3rd-order, close-in spurious tones appear at $f_O \pm 3 \cdot \Delta f$. The

difference between the two equal test-tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \bullet (IM3 - P_O)$ where IM3 is the intercept taken from the typical characteristic curve and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. At 5MHz for instance, the OPA846 at a gain of +10V/V has an intercept of 48dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones are 2 • (48 – 4) = 88dBc below the test-tone power level (–84dBm). If this same $2V_{PP}$, 2-tone envelope were delivered directly into the input of an A/D converter—without the matching loss or the loading of the 50Ω network—the intercept would increase to at least 54dBm. With the same signal and gain conditions, but now driving directly into a light load, the spurious tones will then be at least 2 • (54 – 4) = 100dBc below the 4dBm test-tone power levels centered on 5MHz.

DC ACCURACY AND OFFSET CONTROL

The OPA846 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of its low ±0.6mV maximum (25°C) input offset voltage, careful attention to input bias current cancellation is also required. The low-noise input stage for the OPA846 has a relatively high input bias current (10µA typical into the pins), but with a very close match between the two input currents—typically ±100nA input offset current. Figures 14 and 15 show typical distributions of input offset voltage and current for the OPA846. The total output offset voltage can be considerably reduced by matching the source impedances looking out of the two pins.

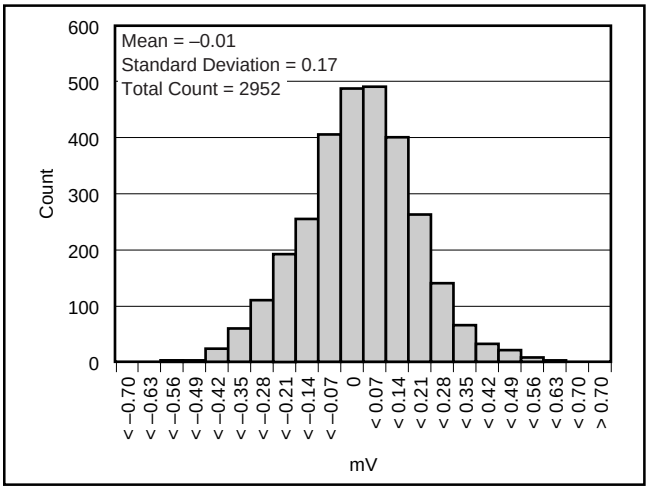


FIGURE 14. Input Offset Voltage Distribution.

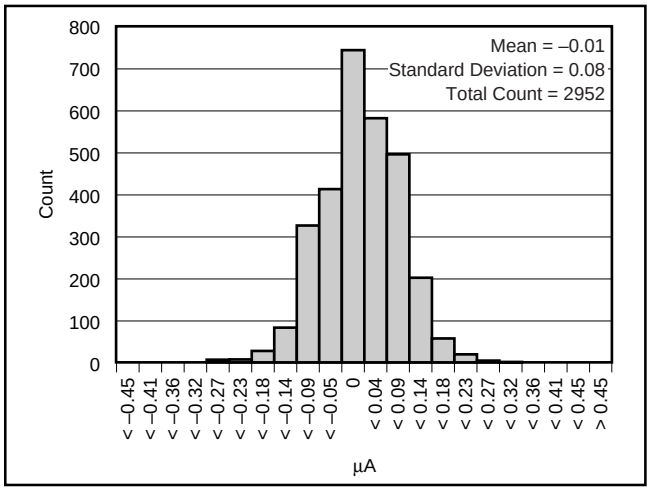


FIGURE 15. Input Offset Current Distribution.

For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 20Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this increases the source resistances for the noninverting input bias current to 45Ω. Since this is now equal to the resistance looking out of the inverting input ($R_F \parallel R_G$), the circuit cancels the gains for the bias currents to the output, leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using the 453Ω feedback resistor, this output error is now less than ±600nA • 453Ω = ±272µV over the full temperature range.

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to ensure that it has minimal impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path uses the inverting mode, applying an offset control to the noninverting input can be considered. For a DC-coupled inverting input signal, this DC offset signal sets up a DC current back into the source that must be considered. An offset adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness. See Figure 16 for one example of an offset adjustment for a DC-coupled signal path that has minimum impact on the signal frequency response. In this case, the input is brought into an inverting gain resistor with the DC adjustment as an additional current summed into the inverting node. The resistor values for setting this offset adjustment are chosen to be much larger than the signal path resistors. This ensures that the adjustment has minimal impact on the loop gain and hence, the frequency response.

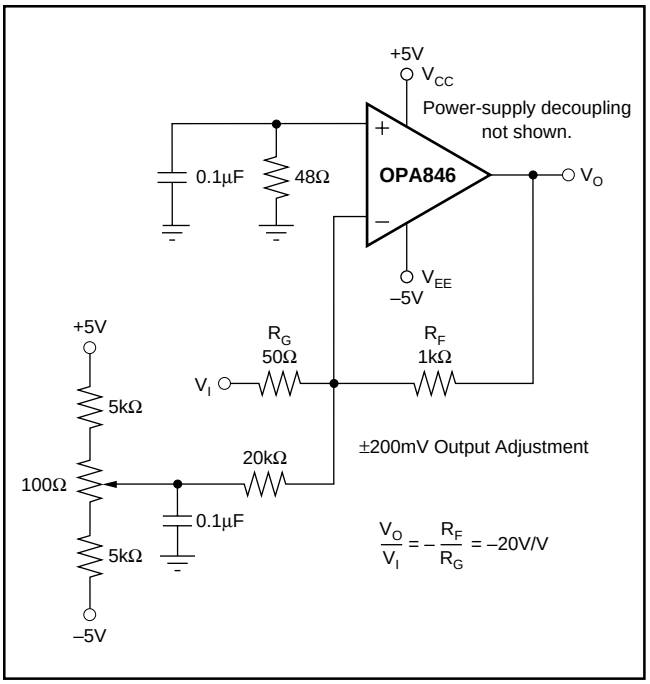


FIGURE 16. DC-Coupled, Inverting Gain of –20V/V with Output Offset Adjustment.

THERMAL ANALYSIS

The OPA846 does not require heat sinking or airflow in most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described following. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes the feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA846IDBV (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load at $+2.5V_{DC}$.

$$P_D = 10V(13.9mA) + 5^2/(4 \bullet (100\Omega \parallel 500\Omega)) = 214mW$$

$$\text{Maximum } T_J = +85°C + (0.21W \bullet 150°C/W) = 117°C$$

All actual applications will operate at a lower junction temperature than the 117°C computed above. Compute the actual stage power to get an accurate estimate of maximum junction temperature, or use the results shown here as an absolute maximum.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier such as the OPA846 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, create a window around the signal I/O pins leave opened in all of the ground and power planes around those pins.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors are effective at lower frequencies, and are recommended on the main supply pins. These may be placed somewhat further from the device and shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components preserves the high-frequency performance of the OPA846. Use resistors that have low reactance at high frequencies. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-feedback side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or a zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be set the R_G be set to 50Ω. Doing this automatically keeps the resistor noise terms low, and minimizes the effect of parasitic capacitance. Transimpedance applications can use much higher resistor values. The compensation techniques described in this data sheet allow excellent frequency response control, even with very high feedback resistor values.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S, since the OPA846 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed, as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard and, in fact, a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA846 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Recommended R_S vs Capacitive Load. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA846 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA846 onto the board.

INPUT AND ESD PROTECTION

The OPA846 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 17.

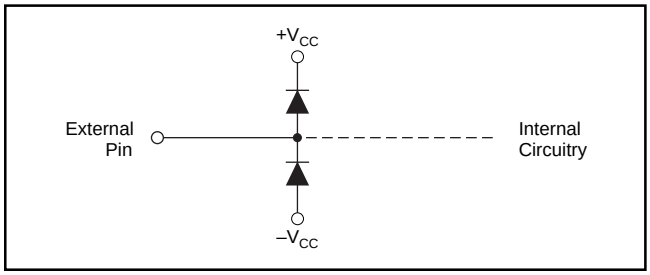


FIGURE 17. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA846), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	E	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
3/06	D	15	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA846ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 846	Samples
OPA846IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OASI	Samples
OPA846IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OASI	Samples
OPA846IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OASI	Samples
OPA846IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 846	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

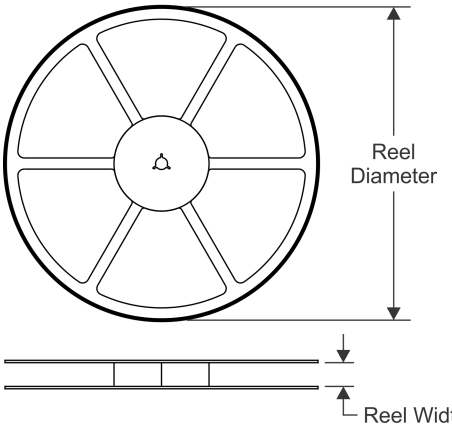
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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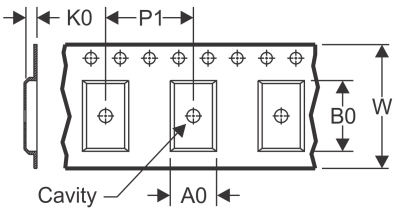
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

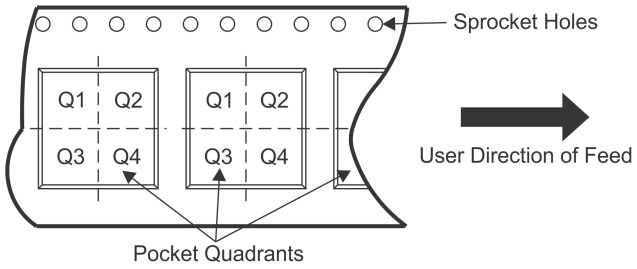


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

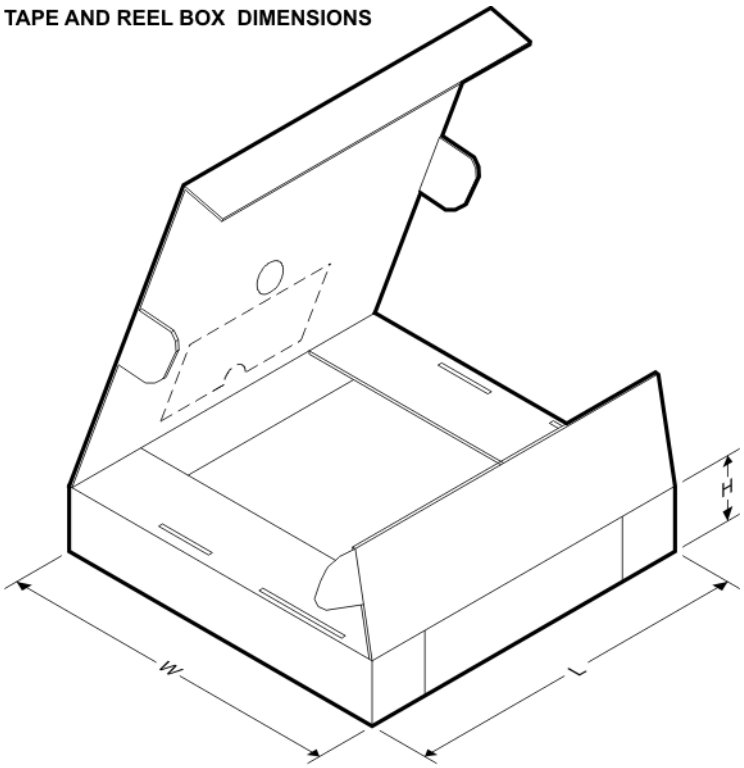
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

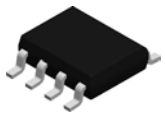
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA846IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA846IDR	SOIC	D	8	2500	367.0	367.0	35.0

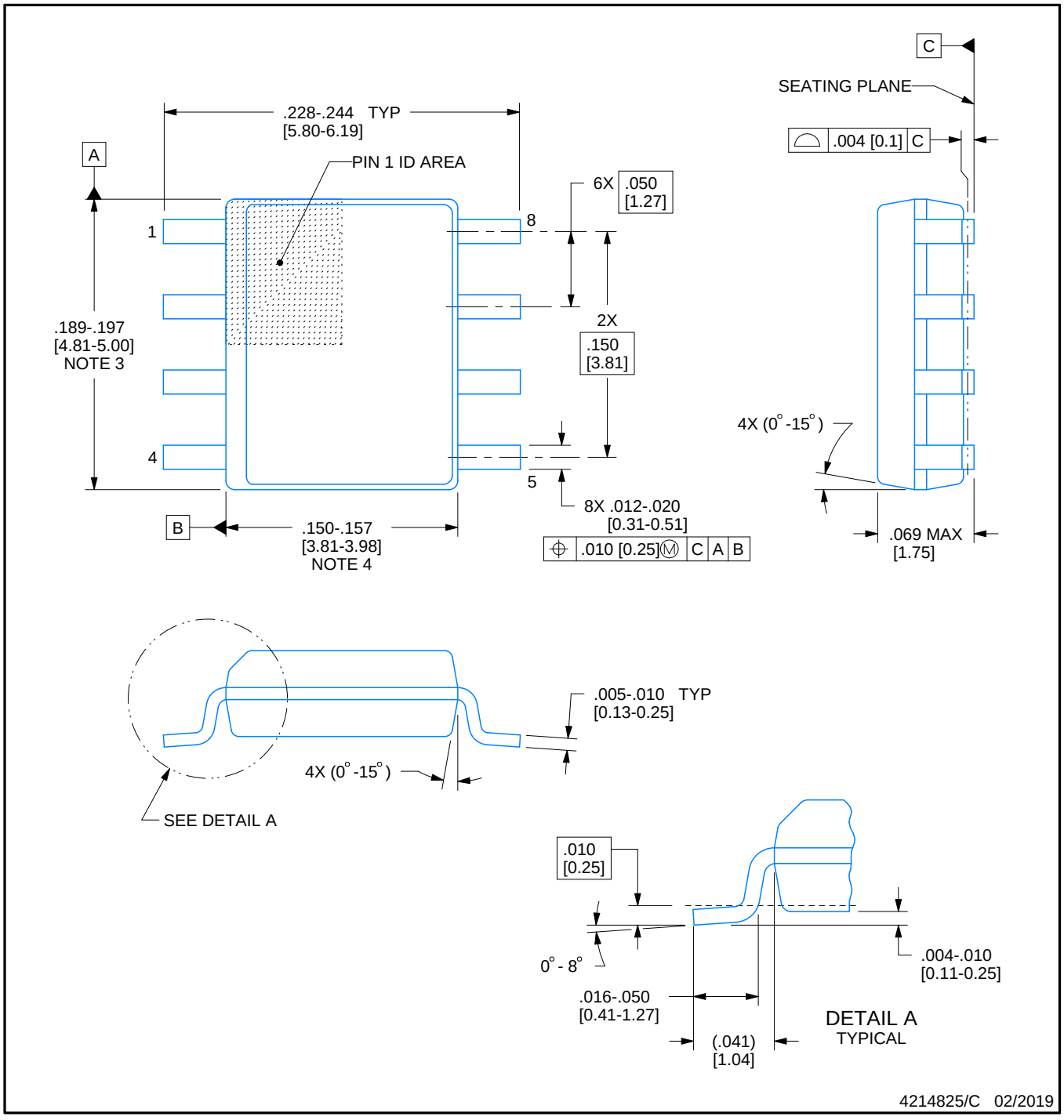


PACKAGE OUTLINE

D0008A

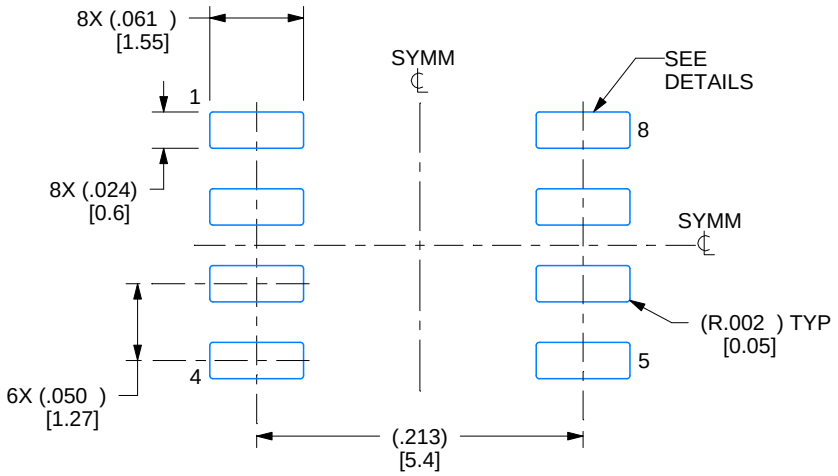
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

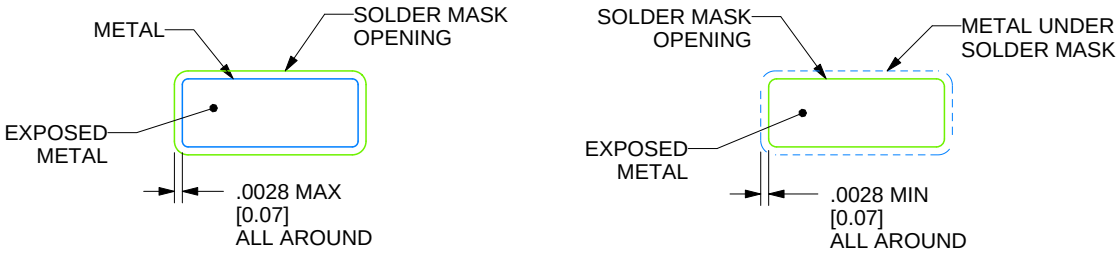


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

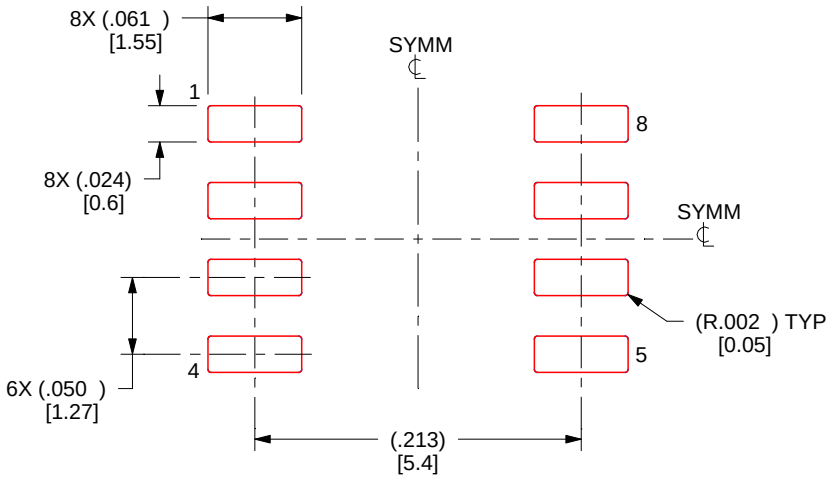
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

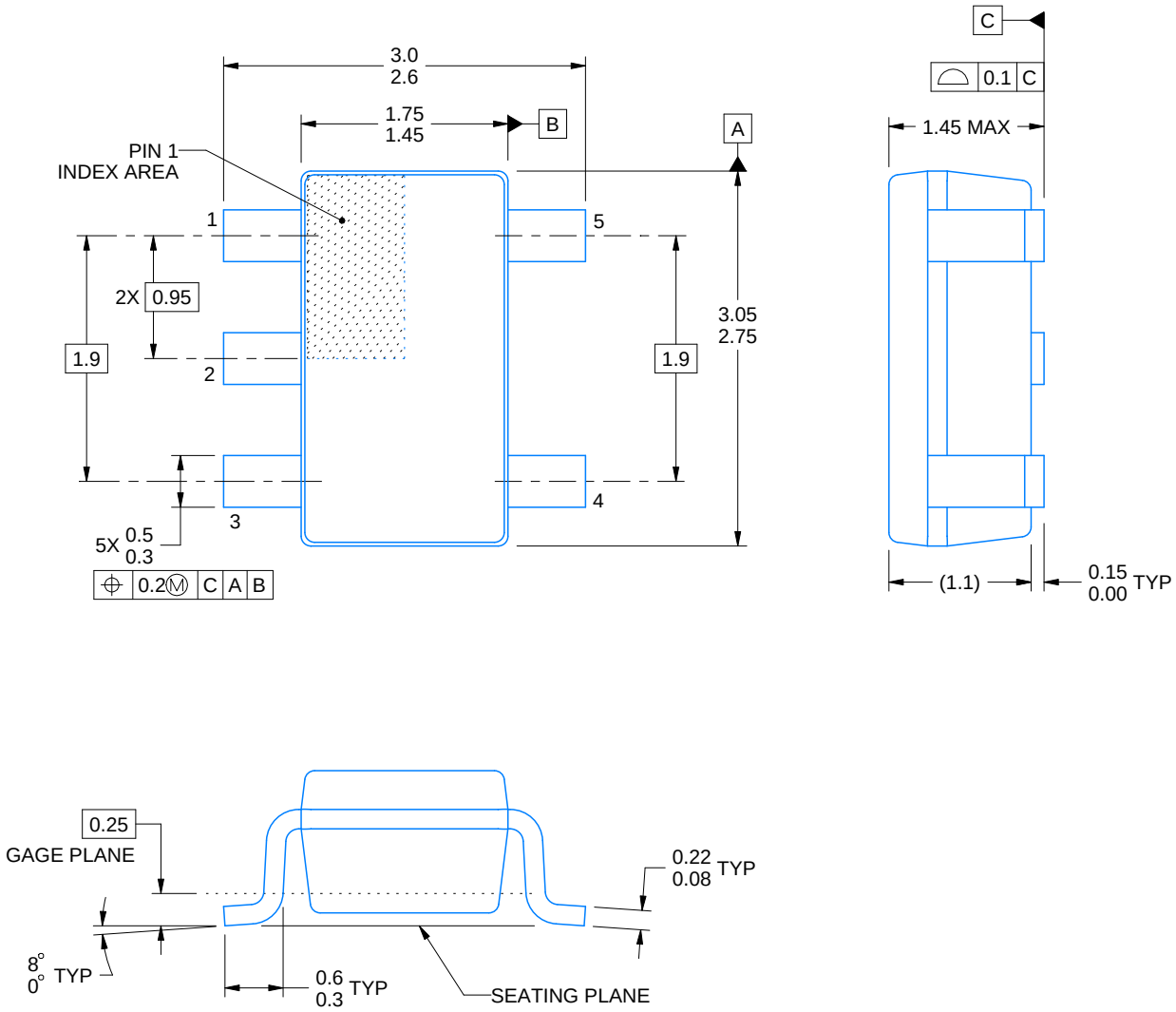
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

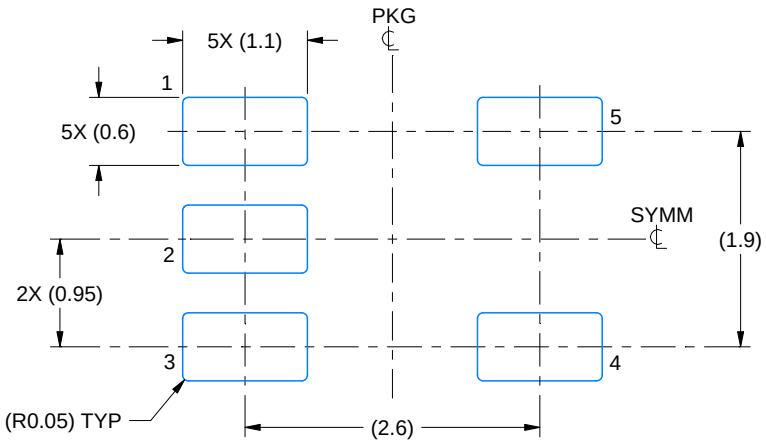
SMALL OUTLINE TRANSISTOR



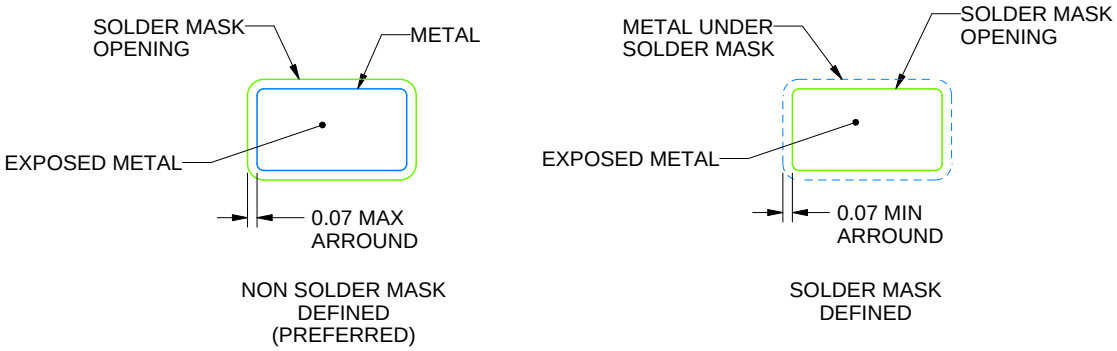
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

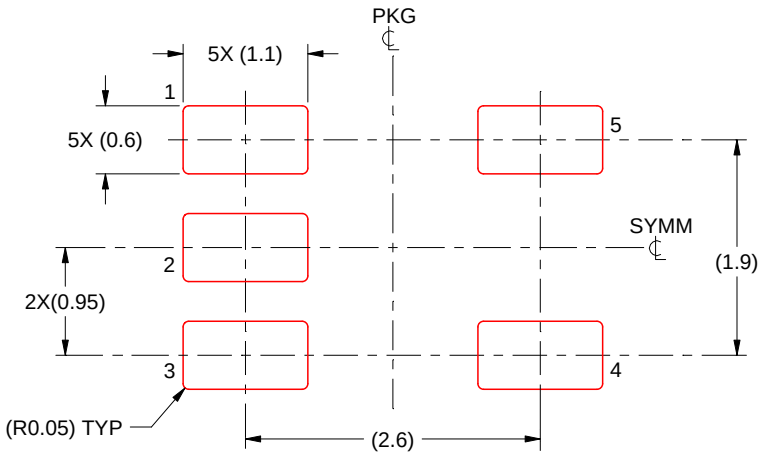


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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