

# Voltage Comparator

## DESCRIPTION

The **RH1011** is a general purpose comparator with significantly better input characteristics than the LM111. Although pin compatible with the LM111, it offers four times lower bias current, six times lower offset voltage and five times higher voltage gain.

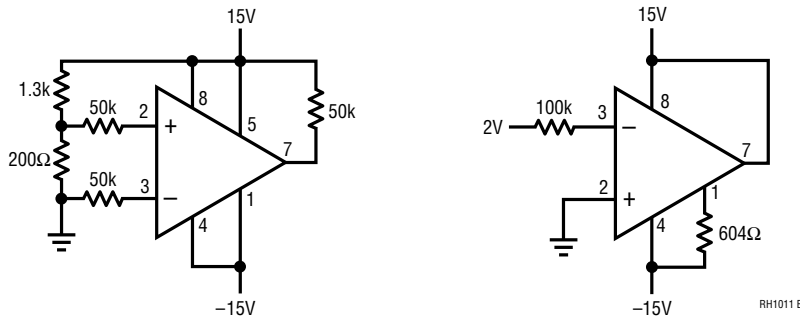
The wafer lots are processed to Analog Devices' in-house Class S flow to yield circuits usable in stringent military applications.

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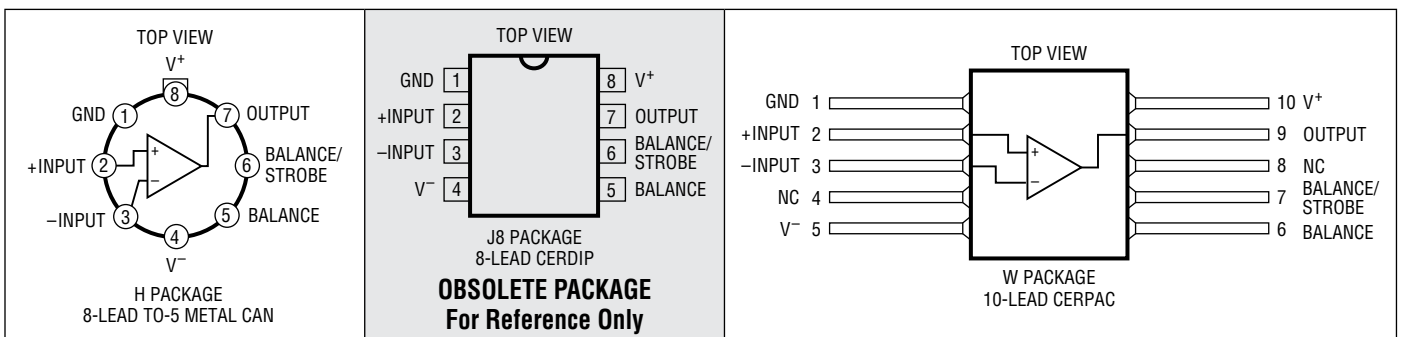
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 8 to Pin 4)	.....36V
Output to Negative Supply (Pin 7 to Pin 4)	..... 35V
Ground to Negative Supply (Pin 1 to Pin 4)	..... 30V
Differential Input Voltage	..... $\pm 35V$
Voltage at STROBE Pin (Pin 6 to Pin 8)	..... 5V
Input Voltage (Note 1)	..... Equal to Supplies
Output Short-Circuit Duration	..... 10 sec
Operating Temperature Range	
(Note 2)	..... $-55^{\circ}C$ to $125^{\circ}C$
Storage Temperature Range	..... $-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec)	..... $300^{\circ}C$

## BURN-IN CIRCUIT



## PACKAGE INFORMATION



**TABLE 1: ELECTRICAL CHARACTERISTICS** (Preirradiation) (Note 10)

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			SUB-GROUP	UNITS	
				MIN	TYP	MAX		MIN	TYP	MAX			
$V_{OS}$	Input Offset Voltage	$R_S \leq 50\text{k}\Omega$	3 4			1.5	1 1			3.0	2,3 2,3	mV	
						2.0			3.0	mV			
$I_{OS}$	Input Offset Current		3,4			4	1			20	2,3	nA	
$I_B$	Input Bias Current		3 4			50	1 1			80	2,3 2,3	nA	
						65			80	nA			
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift	$T_{MIN} \leq T \leq T_{MAX}$	5,9							25		$\mu\text{V}/^\circ\text{C}$	
$A_{VOL}$	Large Signal Voltage Gain	$V_S = \pm 15\text{V}$ , $R_L = 1\text{k}\Omega$ , $-10\text{V} \leq V_{OUT} \leq 14.5\text{V}$		200			4					V/mV	
		$V_S = 5\text{V}$ , $R_L = 500\Omega$ , $0.5\text{V} \leq V_{OUT} \leq 4.5\text{V}$		50				4					V/mV
CMRR	Common Mode Rejection Ratio			90			1					dB	
	Input Voltage Range	$V_S = \pm 15\text{V}$ $V_S = \text{Single } 5\text{V}$	8,9 8,9	-14.5	13				-14.5	13			V
				0.5	3.0			0.5	3.0	V			
$t_d$	Response Time		6,9			250						ns	
$V_{OL}$	Output Saturation Voltage	$V_{IN} = -5\text{mV}$ , $I_{SINK} = 8\text{mA}$ $I_{SINK} = 50\text{mA}$	11			0.4	1			0.5	2,3	V	
						1.5	1		1.5	2,3	V		
	Output Leakage Current	$V_{IN} = 5\text{mV}$ , $V_{GND} = -15\text{V}$ , $V_{OUT} = 20\text{V}$				10	1			500	2,3	nA	
	Positive Supply Current		11			4.0	1					mA	
	Negative Supply Current		11			2.5	1					mA	
	Strobe Current	Minimum to Ensure Output Transistor is Turned Off	7,9,11	500								$\mu\text{A}$	
	Input Capacitance					6						pF	

**TABLE 1A: ELECTRICAL CHARACTERISTICS** (Postirradiation) (Note 10)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si)		20KRAD (Si)		50KRAD (Si)		100KRAD (Si)		200KRAD (Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OS}$	Input Offset Voltage				1.5		1.5		1.5		2.5		4	mV
$I_{OS}$	Input Offset Current				4		4		4		20		50	nA
$I_B$	Input Bias Current				50		100		150		200		300	nA
$A_{VOL}$	Large-Signal Voltage Gain	$R_L = 1\text{k}\Omega$ , $-10\text{V} \leq V_{OUT} \leq 14.5\text{V}$		200		200		150		100		50		V/mV
CMRR	Common Mode Rejection Ratio			90		90		90		90		86		dB
	Input Voltage Range	$V_S = \pm 15\text{V}$ $V_S = \text{Single } 5\text{V}$	8,9	-14.5	13	-14.5	13	-14.5	13	-14.5	13	-14.5	13	V
				0.5	3.0	0.5	3.0	0.5	3.0	0.5	3.0	0.5	3.0	V
$V_{OL}$	Output Saturation Voltage	$V_{IN} = -5\text{mV}$ , $I_{SINK} = 8\text{mA}$ $I_{SINK} = 50\text{mA}$	11		0.4		0.4		0.4		0.4		0.4	V
					1.5		1.5		1.5		1.5		1.5	V
	Output Leakage Current	$V_{IN} = 5\text{mV}$ , $V_{GND} = -15\text{V}$ $V_{OUT} = 20\text{V}$		10		10		100		100		100		nA

**TABLE 1A: ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si)		20KRAD (Si)		50KRAD (Si)		100KRAD (Si)		200KRAD (Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Positive Supply Current		11		4.0		4.0		4.0		4.0		4.0	mA
	Negative Supply Current		11		2.5		2.5		2.5		2.5		2.5	mA
	Strobe Current	Minimum to Ensure Output Transistor is Turned Off	7,9,11	500		500		500		500		500		$\mu$ A
	Input Capacitance			6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)		pF

**Note 1:** Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection discussion in the LT<sup>®</sup>1011 data sheet.

**Note 2:**  $T_{JMAX} = 150^{\circ}\text{C}$ .

**Note 3:** Output is sinking 1.5mA with  $V_{OUT} = 0\text{V}$ .

**Note 4:** These specifications apply for all supply voltages from a single 5V to  $\pm 15\text{V}$ , the entire input voltage range and for both high and low output states. The high state is  $I_{SINK} = 100\mu\text{A}$ ,  $V_{OUT} = (V^+ - 1\text{V})$  and the low state is  $I_{SINK} = 8\text{mA}$ ,  $V_{OUT} = 0.8\text{V}$ . Therefore, this specification defines a worst-case error band that includes effects due to common mode signals, voltage gain and output load.

**Note 5:** Drift is calculated by dividing the offset difference measured at minimum and maximum temperatures by the temperature difference.

**Note 6:** Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500 $\Omega$  resistor tied to 5V. Time measurement is taken when the output crosses 1.4V.

**Note 7:** Do not short the STROBE pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500 $\mu\text{A}$  will strobe the RH1011 if speed is not important. External leakage on the STROBE pin in excess of 0.2 $\mu\text{A}$  when the strobe is "off" can cause offset voltage shifts.

**Note 8:** See graph, Input Offset Voltage vs Common Mode Voltage on the LT1011 data sheet.

**Note 9:** Guaranteed by design, characterization or correlation to other tested parameters.

**Note 10:**  $V_S = \pm 15\text{V}$ ,  $V_{CM} = 0\text{V}$ ,  $R_S = 0\Omega$ ,  $T_A = 25^{\circ}\text{C}$ ,  $V_{GND} = V^-$ , output at Pin 7, unless otherwise noted.

**Note 11:**  $V_{GND} = 0\text{V}$ .

**TABLE 2: ELECTRICAL TEST REQUIREMENTS**

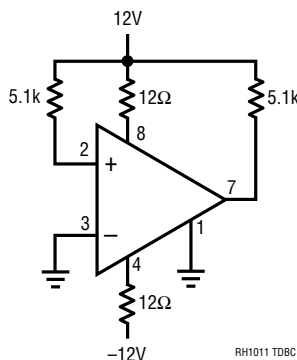
MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4
Group A Test Requirements (Method 5005)	1,2,3,4
Group B and D End Point Electrical Parameters (Method 5005)	1,2,3

\* PDA applies to subgroup 1. See PDA Test Notes.

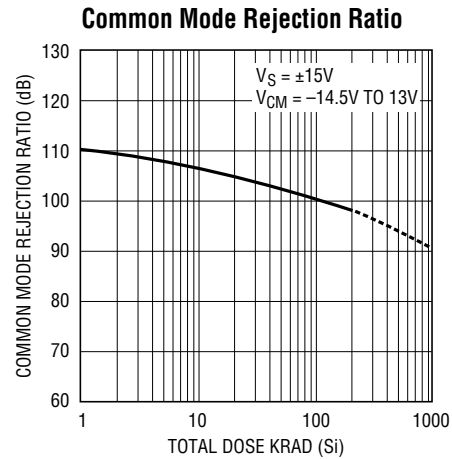
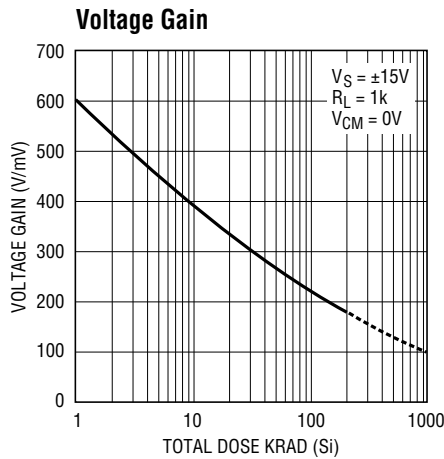
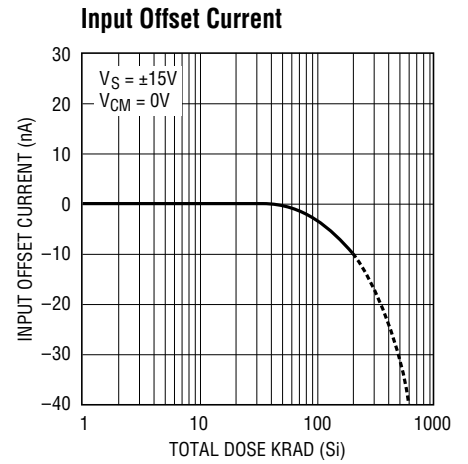
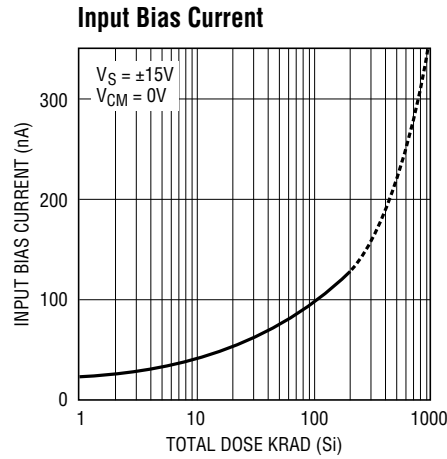
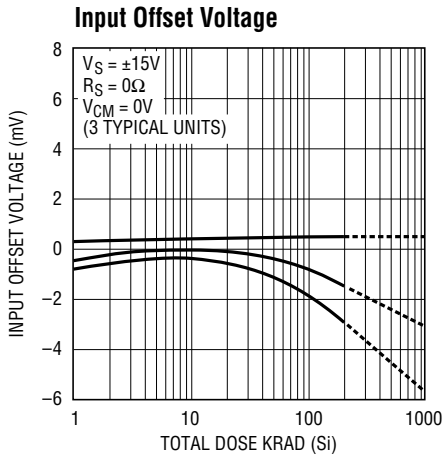
**PDA Test Notes**

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Analog Devices, Inc. reserves the right to test to tighter limits than those given.

**TOTAL DOSE BIAS CIRCUIT**

## TYPICAL PERFORMANCE CHARACTERISTICS



## REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	02/19	Obsoleting J8 package and updating document to ADI format	All Pages