Quad DC/DC µModule Regulator with Configurable Dual 12A, Dual 5A Output Array

FEATURES

- **Quad Output Step-Down µModule® Regulator with Dual 12A and Dual 5A Output**
- **Wide Input Voltage Range: 3.1V to 20V**
- **Dual 12A DC Output from 0.6V to 3.3V**
- **Dual 5A DC Output from 0.6V to 5.5V**
- **Up to 7W Power Dissipation (T_A = 60°C, 200LFM, No Heat Sink)**
- ±1.5% Total Output Voltage Regulation
- Dual Differential Sensing Amplifier
- Current Mode Control, Fast Transient Response
- Parallelable for Higher Output Current
- Selectable Burst Mode® Operation
- Output Voltage Tracking
- Internal Temperature Sensing Diode Output
- External Frequency Synchronization
- Overvoltage, Current and Temperature Protection
- 9.5mm × 16mm × 4.72mm BGA Package

APPLICATIONS

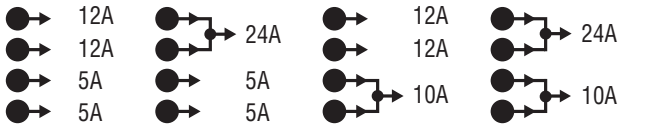
- Multirail Point-of-Load Regulation
- FPGAs, DSPs and ASICs Applications

DESCRIPTION

The LTM®4671 is a quad DC/DC step-down µModule (micromodule) regulator offering dual 12A and dual 5A output. Included in the package are the switching controllers, power FETs, inductors and support components. Operating over an input voltage range of 3.1V to 20V, the LTM4671 supports an output voltage range of 0.6V to 3.3V for two 12A channels and 0.6V to 5.5V for two 5A channels, each set by a single external resistor. Only bulk input and output capacitors are needed.

Fault protection features include overvoltage, overcurrent and overtemperature protection. The LTM4671 is offered in 9.5mm × 16mm × 4.72mm BGA package.

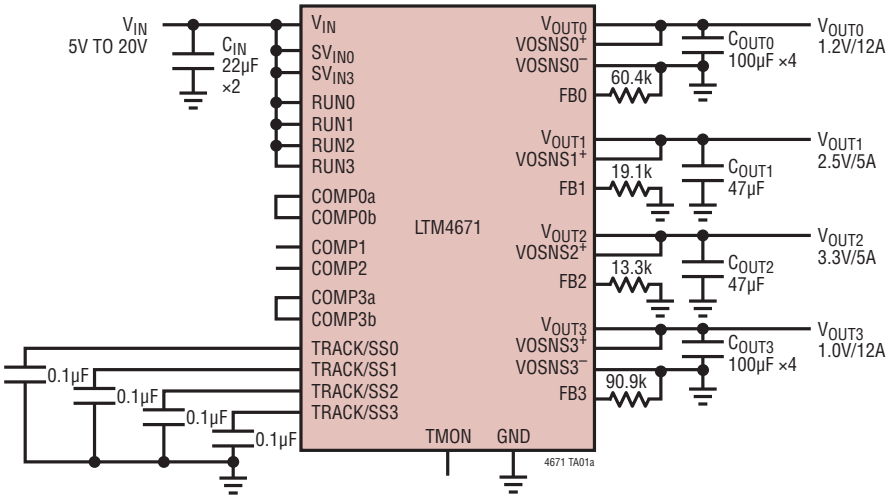
Configurable Output Array*



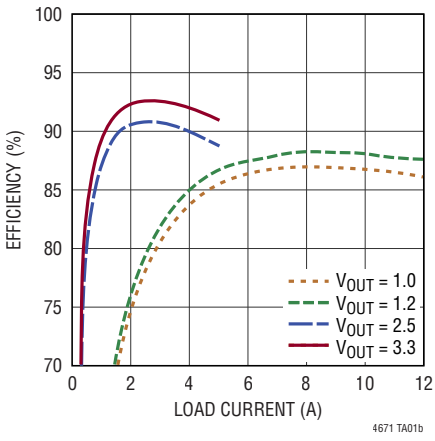
* Note 4

TYPICAL APPLICATION

4V to 20V Input, 12A, 12A, 5A, 5A DC/DC Step-Up µModule Regulator



$12V_{IN}$ Efficiency vs Load Current



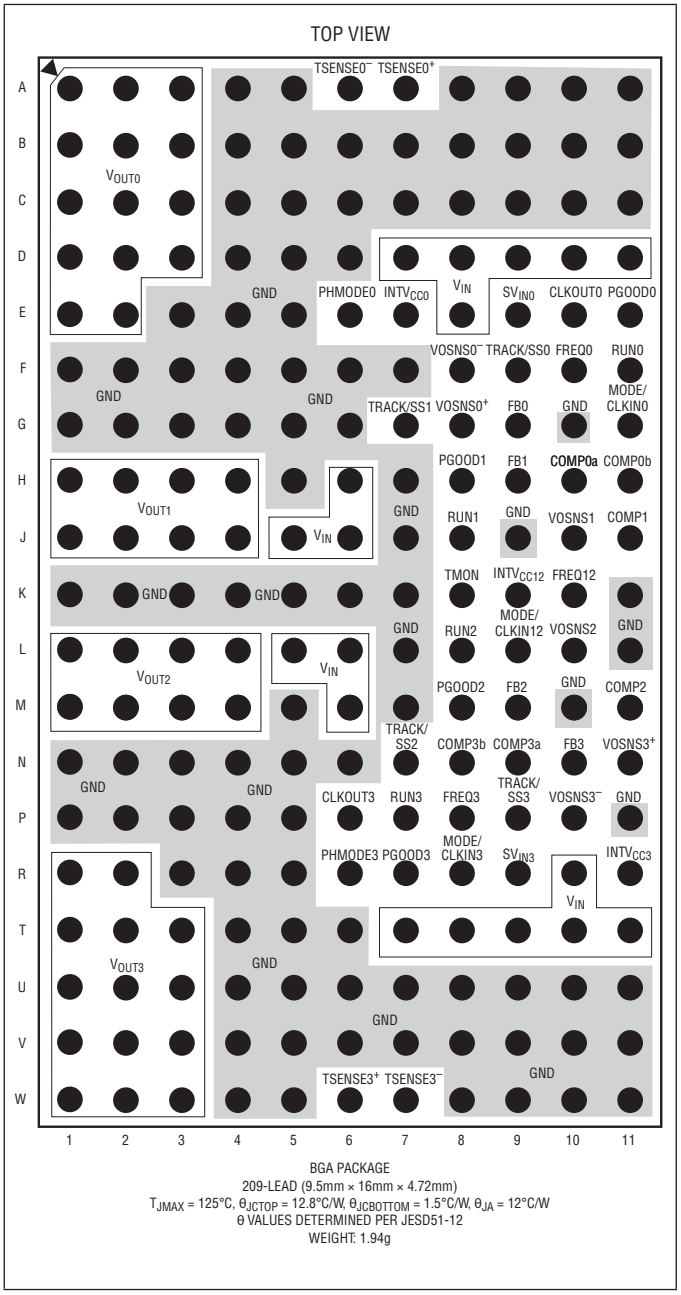
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SV_{IN0}, SV_{IN3} ..... –0.3V to 22V
V_{OUT0}, V_{OUT3} ..... –0.3V to 3.6V
V_{OUT1}, V_{OUT2} ..... –0.3V to 6V
$INTV_{CC0}$, $INTV_{CC12}$, $INTV_{CC3}$, ... –0.3V to 3.6V
FREQ0, FREQ12, FREQ3, ... –0.3V to 3.6V
FB0, FB1, FB2, FB3, ... –0.3V to 3.6V
COMP0a, COMP0b, COMP3a, COMP3b,
COMP1, COMP2, ... –0.3V to 3.6V
RUN0, RUN1, RUN2, RUN3 ..... –0.3V to 22V
TRACK/SS0, TRACK/SS1, TRACK/SS2,
TRACK/SS3, ... –0.3V to 3.6V
PGOOD0, PGOOD1, PGOOD2, PGOOD3, ... –0.3V to 3.6V
$VOSNS0^+$, $VOSNS0^-$, $VOSNS3^+$,
$VOSNS3^-$, ... –0.3V to 3.6V
VOSNS1, VOSNS2 ..... –0.3V to 6V
$TSENSE0^+$, $TSENSE0^-$, $TSENSE3^+$,
$TSENSE3^-$ ..... –0.3V to 0.8V
TMON ..... –0.3V to 3.6V
MODE/CLKIN0, CLKOUT0, MODE/CLKIN3,
CLKOUT3, MODE/CLKIN12 ..... –0.3V to 3.6V
Operating Junction Temperature (Note 2) –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

PIN CONFIGURATION

(See Pin Functions, Component BGA Pinout Table)



BGA PACKAGE
209-LEAD (9.5mm × 16mm × 4.72mm)
T_{JMAX} = 125°C, θ_{JCTOP} = 12.8°C/W, $\theta_{JCBOTTOM}$ = 1.5°C/W, θ_{JA} = 12°C/W
θ VALUES DETERMINED PER JESD51-12
WEIGHT: 1.94g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4671EY#PBF	SAC305 (RoHS)	LTM4671Y	e1	BGA	3	–40°C to 125°C
LTM4671IY#PBF		LTM4671Y				

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), SV_{IN} = V_{IN} = 12V, unless otherwise noted. Per the typical application in Figure 28.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: (12A Channels)							
V_{IN}	Input DC Voltage		●	3.1		20	V
$V_{IN(AFTER\ START\text{-}UP)}$	Input DC Voltage After Start-Up		●	2.9		20	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		3.3	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic R_{FB} = 40.2k, Continuous Current Mode SV_{IN} = V_{IN} = 3.1V to 20V, I_{OUT} = 0A to 12A	●	1.482	1.50	1.518	V
$I_{Q(VIN)}$	Input Supply Bias Current	SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V, Continuous Current Mode SV_{IN} = V_{IN} = 12V, RUN = 0, Shutdown			75 70		mA µA
$I_{S(VIN)}$	Input Supply Current	SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A			1.6		A
$I_{OUT(DC)}$	Output Continuous Current Range	SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		12	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 3.1V to 20V, I_{OUT} = 0A	●		0.001	0.025	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 12A	●		0.2	0.5	% %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V			6		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V			15		mV
t_{START}	Turn-On Time	TRACK/SS = 0.01µF, SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 3× 100µF Ceramic			1		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 3× 100µF Ceramic			±50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 3× 100µF Ceramic			50		µs
I_{OUTPK}	Output Current Limit	SV_{IN} = V_{IN} = 12V, V_{OUT} = 1.5V		14			A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.6	0.606	V
I_{FB}	Current at V_{FB} Pin	(Note 6)				±50	nA
$R_{FB(TOP)}$	Resistor Between V_{OUT} and V_{FB} Pins			60.05	60.40	60.75	kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), SV_{IN} = V_{IN} = 12V, unless otherwise noted. Per the typical application in Figure 28.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising Hysteresis		1.10	1.20 150	1.30	V mV
UVLO	Undervoltage Lockout	$INTV_{CC}$ Falling Hysteresis		2.4	2.55 0.4	2.7	V V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			6		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			25		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 5)			80		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –10 6	 –8 8	 –6 10	 % %
R_{PGOOD}	PGOOD Pull-Down Resistance	1mA Load			8	15	Ω
$INTV_{CC}$	Internal V_{CC} Voltage			3.2	3.3	3.4	V
FREQ	Default Switching Frequency				600		kHz
CLKIN_H	CLKIN_H Input High Threshold CLKIN_H Input Low Threshold			1		 0.3	V V
Switching Regulator Section: (5A Channels)							
V_{IN}	Input DC Voltage		●	3.1		20	V
$V_{IN(AFTER\ START\text{-}UP)}$	Input DC Voltage After Start-Up		●	2.9		20	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic R_{FB} = 40.2k, Continuous Current Mode V_{IN} = 3.1V to 20V, I_{OUT} = 0A to 5A	●	1.477	1.50	1.523	V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, Continuous Current Mode V_{IN} = 12V, V_{OUT} = 1.5V, Burst Mode Operation (I_{OUT} = 0.5A V_{IN} = 12V, RUN = 0V, Shutdown			18 82 75		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 5A			0.7		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		5	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 3.1V to 20V, I_{OUT} = 0A	●		0.001	0.025	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 5A	●		0.2	0.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic V_{IN} = 12V, V_{OUT} = 1.5V			8		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			15		mV
t_{START}	Turn-On Time	TRACK/SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 100µF Ceramic			5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 25% to 0% of Full Load V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 100µF Ceramic			30		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 25% to 0% of Full Load V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 100µF Ceramic			70		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V		6			A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.592	0.6	0.608	V
I_{FB}	Current at V_{FB} Pin	(Note 6)				±30	nA
$R_{FB(TOP)}$	Resistor Between V_{OUT} and V_{FB} Pins			60.05	60.40	60.75	kΩ
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising Hysteresis		1.15	1.25 200	1.35	V mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), SV_{IN} = V_{IN} = 12V, unless otherwise noted. Per the typical application in Figure 28.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
UVLO	Undervoltage Lockout	$INTV_{CC}$ Falling Hysteresis		2.2	2.4 0.5	2.6	V V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			1.4		µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 5)			45		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –10 5	 –8 8	 –5 10	 % %
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			25		Ω
$INTV_{CC}$	Internal V_{CC} Voltage			3.1	3.3	3.5	V
FREQ	Default Switching Frequency				1		MHz
MODE/CLKIN_L	MODE/CLKIN_L High Threshold MODE/CLKIN_L Low Threshold			1		 0.3	V V
TMON12	Temperature Monitor Temperature Monitor Slop	T_A = 25°C			1.5 200		V °C/V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4671 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4671E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4671I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The minimum on-time is tested at wafer sort.

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

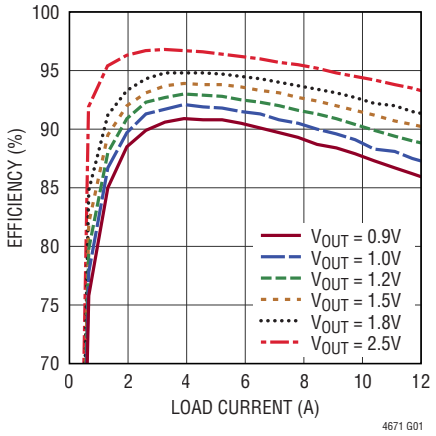
Note 5: Guaranteed by design.

Note 6: 100% tested at wafer level.

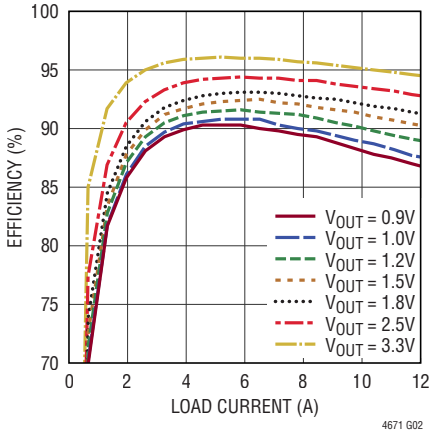
TYPICAL PERFORMANCE CHARACTERISTICS

Dual 12A Channels

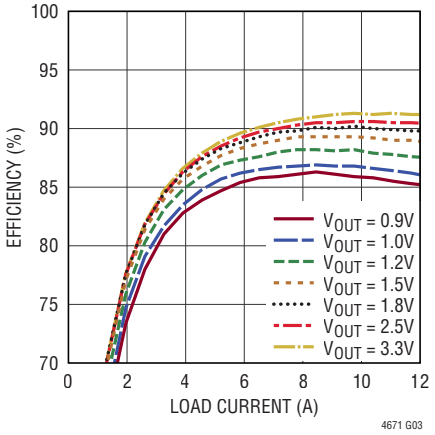
Efficiency vs Load Current from 3.3V_{IN}



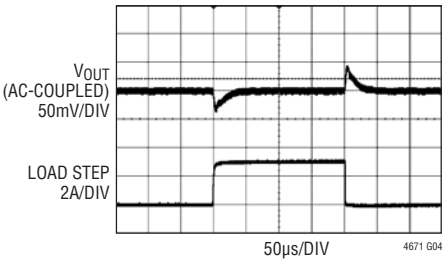
Efficiency vs Load Current from 5V_{IN}



Efficiency vs Load Current from 12V_{IN}

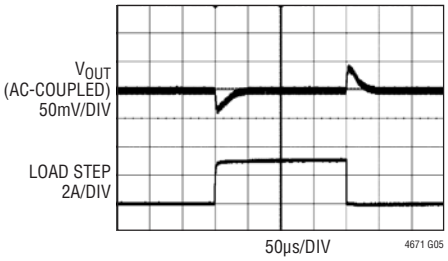


1.0V Output Transient Response



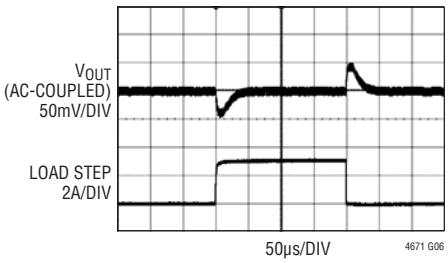
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS
EXT COMP, C_{TH} = 2200pF, R_{TH} = 5k, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

1.2V Output Transient Response



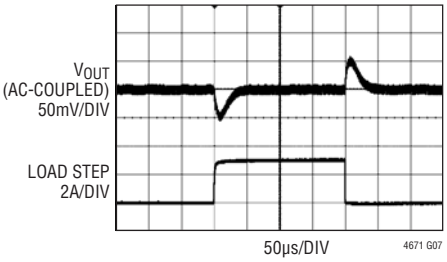
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS
EXT COMP, C_{TH} = 2200pF, R_{TH} = 5k, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

1.5V Output Transient Response



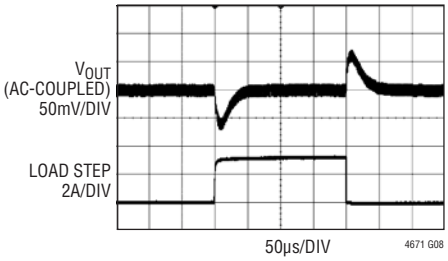
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS
EXT COMP, C_{TH} = 2200pF, R_{TH} = 5k, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

1.8V Output Transient Response



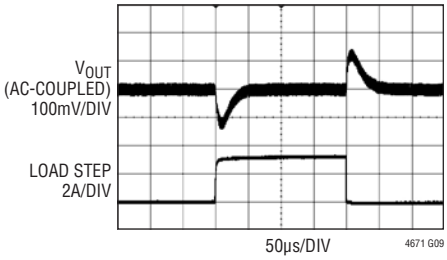
V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS
EXT COMP, C_{TH} = 2200pF, R_{TH} = 5k, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

2.5V Output Transient Response



V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS
EXT COMP, C_{TH} = 2200pF, R_{TH} = 5k, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

3.3V Output Transient Response

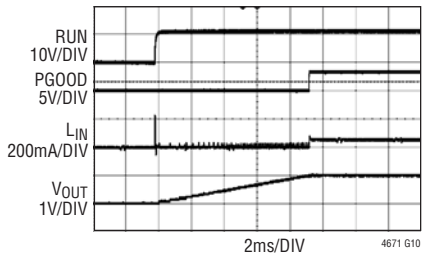


V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS
EXT COMP, C_{TH} = 2200pF, R_{TH} = 5k, C_{FF} = 33pF
3A (25%) LOAD STEP, 1A/µs

TYPICAL PERFORMANCE CHARACTERISTICS

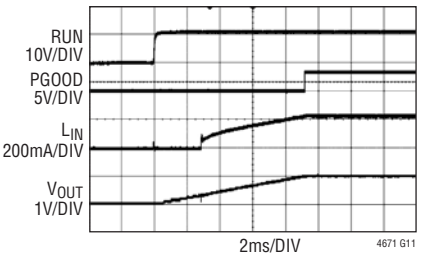
Dual 12A Channels

Start-Up Waveform with No Load Current Applied



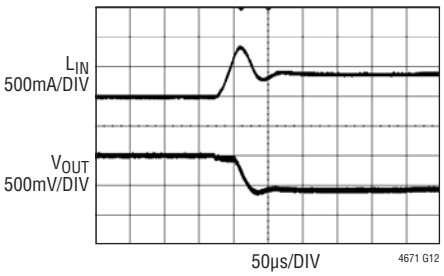
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 1× 330µF POSCAP,
2× 100µF CERAMIC CAPACITORS
C_{SS} = 0.1µF

Start-Up Waveform with 12A Load Current Applied



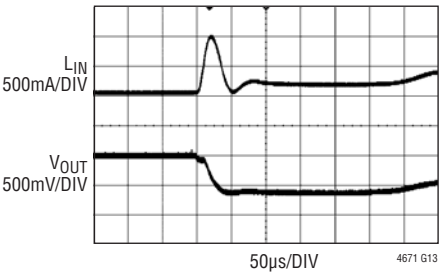
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 1× 330µF POSCAP,
2× 100µF CERAMIC CAPACITORS
C_{SS} = 0.1µF

Short-Circuit Waveform with No Load Current Exist



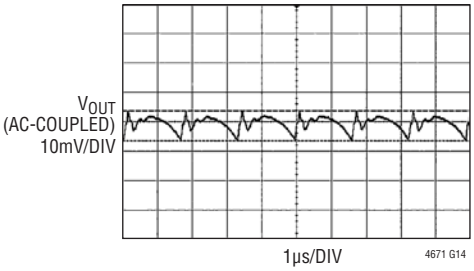
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 1× 330µF POSCAP,
2× 100µF CERAMIC CAPACITORS

Short-Circuit Waveform with 12A Load Current Exist



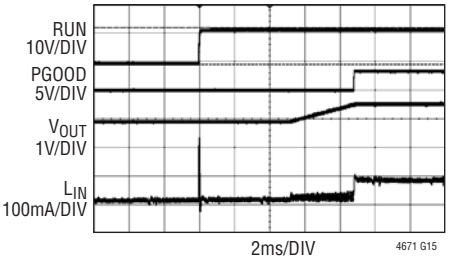
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 1× 330µF POSCAP,
2× 100µF CERAMIC CAPACITORS

Output Ripple



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 3× 100µF CERAMIC CAPACITORS

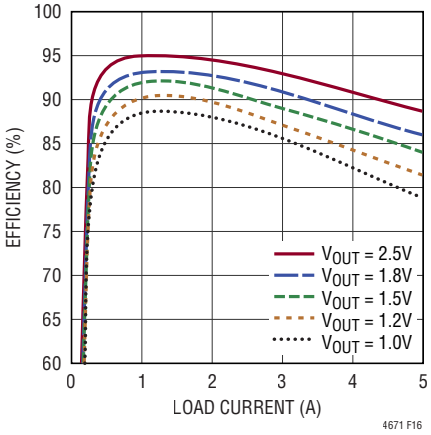
Start Into Pre-Biased Output



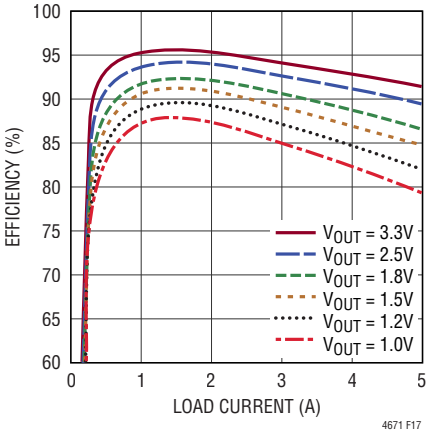
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 600kHz
C_{OUT} = 1× 330µF POSCAP +
2× 100µF CERAMIC CAPACITORS
V_{OUT} = PREBIASED TO 0.9V

Dual 5A Channels

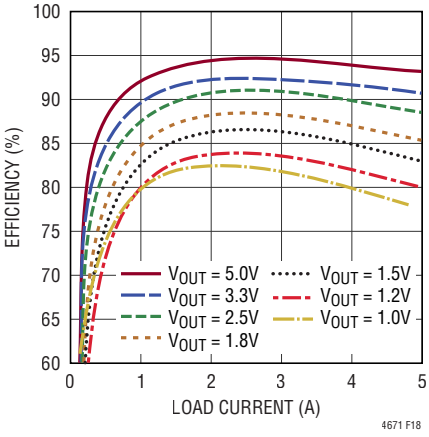
Efficiency vs Load Current from 3.3V_{IN}



Efficiency vs Load Current from 5V_{IN}

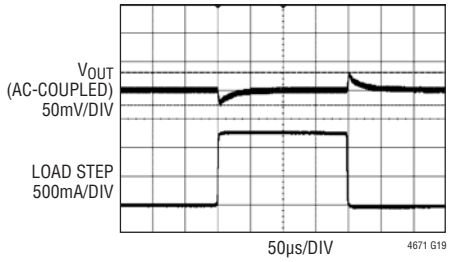


Efficiency vs Load Current from 12V_{IN}



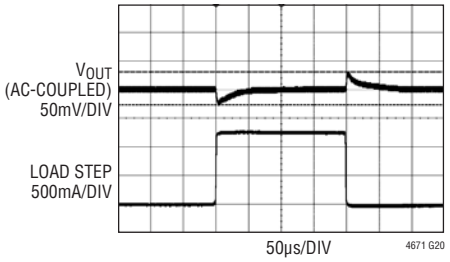
TYPICAL PERFORMANCE CHARACTERISTICS

1.0V Output Transient Response



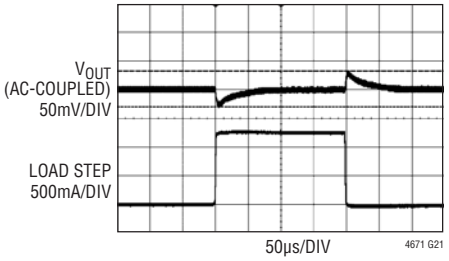
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

1.2V Output Transient Response



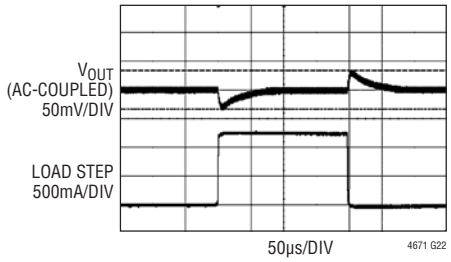
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

1.5V Output Transient Response



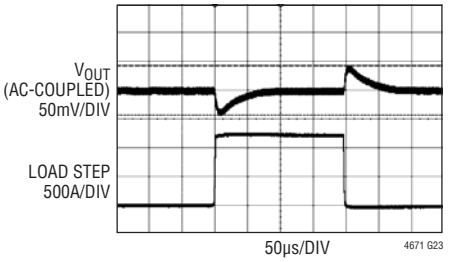
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

1.8V Output Transient Response



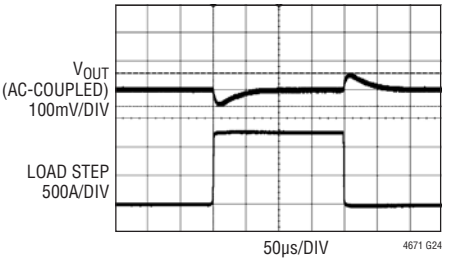
V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

2.5V Output Transient Response



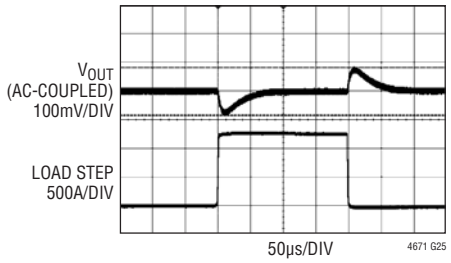
V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

3.3V Output Transient Response



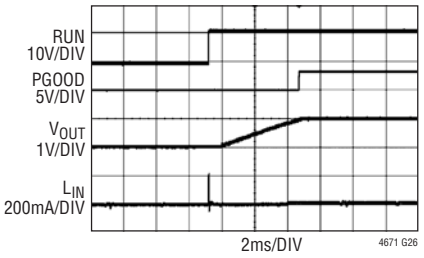
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

5V Output Transient Response



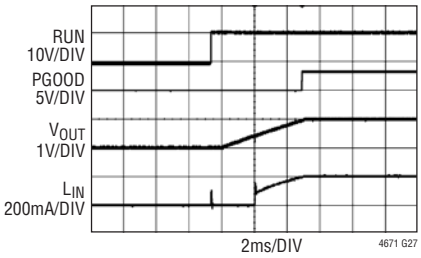
V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF
1.25A (25%) LOAD STEP, 1A/µs

Start-Up Waveform with No Load Current Applied



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF, C_{SS} = 0.1µF

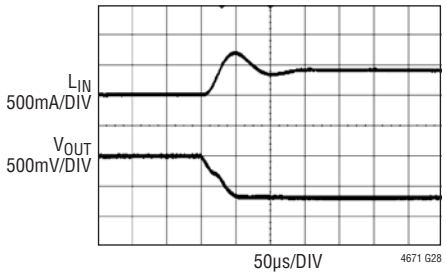
Start-Up Waveform with 5A Load Current Applied



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF, C_{SS} = 0.1µF

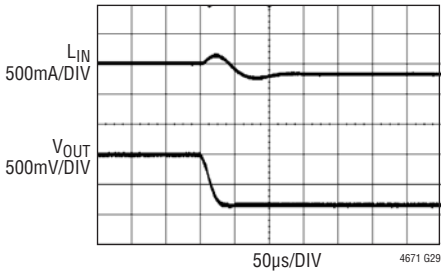
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Waveform with No Load Current Exist



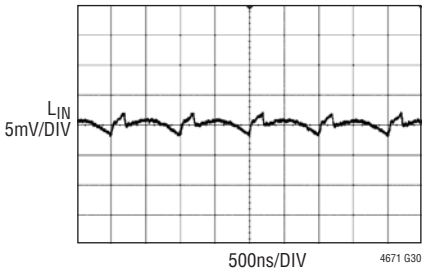
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Short-Circuit Waveform with 5A Load Current Exist



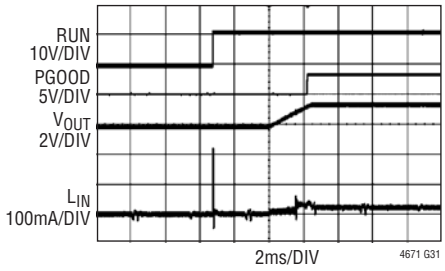
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Output Ripple



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF

Start Into Pre-Biased Output



V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz
C_{OUT} = 2× 47µF + 10µF CERAMIC CAPACITORS
C_{FF} = 100pF, V_{OUT} PREBIASED 2V

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (D7-D11, E8, H6, J5-J6, L5-L6, M6, R10, T7-T11): Power Input. Pins connect to the drain of the internal top MOSFET and Signal V_{IN} to the internal 3.3V regulator for the control circuitry for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of V_{IN} pins and GND pins.

GND (A4-A5, A8-A11, B4-B11, C4-C11, D4-D6, E3-E5, F1-F7, G1-G6, G10, H5, H7, J7, J9, K1-K7, K11, L7, L11, M5, M7, M10, N1-N6, P1-P5, P11, R3-R5, T4-T6, U4-U11, V4-V11, W4-W5, W8-W11): Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

PINS FOR DUAL 12A CHANNELS:

V_{OUT0} (A1-A3, B1-B3, C1-C3, D1-D3, E1-E2), V_{OUT3} (R1-R2, T1-T3, U1-U3, V1-V3, W1-W3): Power Output Pins of Each 12A Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

PGOOD0 (E11), PGOOD3 (R7): Output Power Good with Open-Drain Logic of Each 12A Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

$INTV_{CC0}$ (E7), $INTV_{CC3}$ (R11): Internal 3.3V Regulator Output of Each 12A Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. Decouple each pin to GND with a minimum of 2.2µF local low ESR ceramic capacitor.

RUN0 (F11), RUN3 (P7): Run Control Input of Each 12A Switching Mode Regulator Channel. Enable regulator operation by tying the specific RUN pin above 1.2V. Tying it below 1.1V shuts down the specific regulator channel.

COMP0a (H10), COMP3a (N9): Current Control Threshold and Error Amplifier Compensation Point of Each 12A Switching Mode Regulator Channel. The internal current comparator threshold is linearly proportional to this voltage. Tie the COMPa pins from different channels together for parallel operation. The device is internal compensated. Connect to COMP0b or COMP3b, respectively, to use the internal compensation. Or connect to a Type-II C-R-C network to use customized compensation.

COMP0b (H11), COMP3b (N8): Internal Loop Compensation Network for Each 12A Switching Mode Regulator Channel. Connect to COMP0a or COMP3a, respectively, to use the internal compensation in majority of applications.

FB0 (G9), FB3 (N10): The Negative Input of the Error Amplifier for Each 12A Switching Mode Regulator Channel. This pin is internally connected to $VOSNS0^+$ or $VOSNS3^+$, respectively, with a 60.4kΩ precision resistor. Output voltages can be programmed with an additional resistor between FB and $VOSNS^-$ pins. In PolyPhase® operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

TRACK/SS0 (F9), TRACK/SS3 (P9): Output Tracking and Soft-Start Pin of Each 12A Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 6µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function. See the Applications Information section for details.

PIN FUNCTIONS

FREQ0 (F10), FREQ3 (P8): Switching Frequency Program Pin of Each 12A Switching Mode Regulator Channel. Frequency is set internally to 600kHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

$VOSNS0^+$ (G8), $VOSNS3^+$ (N11): Positive Input to the Differential Remote Sense Amplifier of Each 12A Switching Mode Regulator Channel. Internally, this pin is connected to V_{FB} with a 60.4k 0.5% precision resistor. See the Applications Information section for details.

$VOSNS0^-$ (F8), $VOSNS3^-$ (P10): Negative Input to the Differential Remote Sense Amplifier of Each 12A Switching Mode Regulator Channel. Connect an external resistor between FB and $VOSNS^-$ pin to set the output voltage of the specific channel. See the Applications Information section for details.

MODE/CLKIN0 (G11), MODE/CLKIN3 (R8): Discontinuous Mode Select Pin and External Synchronization Input to Phase Detector of Each 12A Switching Mode Regulator Channel. Tie MODE/CLKIN to GND for discontinuous mode of operation. Floating MODE/CLKIN or tying it to a voltage above 1V will select forced continuous mode. Furthermore, connecting MODE/CLKIN to an external clock will synchronize the system clock to the external clock and puts the part in forced continuous mode. See Applications Information section for details.

CLKOUT0 (E10), CLKOUT3 (P6): Output Clock Signal for PolyPhase Operation of Each 12A Switching Mode Regulator Channel. The phase of CLKOUT with respect to CLKIN is determined by the state of the respective PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. See Applications Information section for details.

PHMODE0 (E6), PHMODE3 (R6): Control Input to the Phase Selector of Each 12A Switching Mode Regulator Channel. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to $INTV_{CC}$ for 2-phase operation, tie it to SGND for 3-phase operation, and floating for 4-phase operation. See Applications Information section for details.

$TSENSE0^+$ (A7), $TSENSE3^+$ (W6): Temperature Monitor of Each 12A Switching Mode Regulator Channel. An internal diode connected PNP transistor is placed between $TSENSE^+$ and $TSENSE^-$ pins. See the Applications Information section.

$TSENSE0^-$ (A6), $TSENSE3^-$ (W7): Low Side of the Internal Temperature Monitor.

SV_{IN0} (E9), SV_{IN3} (R9): Signal V_{IN}. Filtered input voltage to the on-chip 3.3V regulator. Tie this pin to the V_{IN} pin in most applications or connect SV_{IN} to an external voltage supply of at least 4V which must also be greater than V_{OUT}.

PINS FOR DUAL 5A CHANNELS:

V_{OUT1} (H1-H4, J1-J4), V_{OUT2} (L1-L4, M1-M4): Power Output Pins of Each 5A Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See the Applications Information section for paralleling outputs.

PGOOD1 (H8), PGOOD2 (M8): Output Power Good with Open-Drain Logic of Each 5A Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

$INTV_{CC12}$ (K9): Internal 3.3V Regulator Output for Both 5A Switching Mode Regulator Channels. The internal power drivers and control circuits are powered from this voltage. Decouple each pin to GND with a minimum of 2.2µF local low ESR ceramic capacitor.

RUN1 (J8), RUN2 (L8): Run Control Input of Each 5A Switching Mode Regulator Channel. Enable regulator operation by tying the specific RUN pin above 1.2V. Tying it below 1.1V shuts down the specific regulator channel.

COMP1 (J11), COMP2 (M11): Current Control Threshold and Error Amplifier Compensation Point of Each 5A Switching Mode Regulator Channel. The internal current compara-

PIN FUNCTIONS

tor threshold is linearly proportional to this voltage. Tie the COMP pins from different channels together for parallel operation. These channels are internal compensated.

FB1 (H9), FB2 (M9): The Negative Input of the Error Amplifier for Each 5A Switching Mode Regulator Channel. This pin is internally connected to VOSNS1 or VOSNS2, respectively, with a 60.4kΩ precision resistor. Output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

TRACK/SS1 (G7), TRACK/SS2 (N7): Output Tracking and Soft-Start Pin of Each 5A Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 1.4µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function. See the Applications Information section for details.

FREQ12 (K10): Switching Frequency Program Pin for Both 5A Switching Mode Regulator Channels. Frequency is set internally to 1MHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

VOSNS1 (J10), VOSNS2 (L10): Output Voltage Sense Pin of Each 5A Switching Mode Regulator Channel. Internally, this pin is connected to V_{FB} with a 60.4k 0.5% precision resistor. See the Applications Information section for details. It is very important to connect these pins to the V_{OUT} since this is the feedback path, and cannot be left open. See the Applications Information section for details.

MODE/CLKIN12 (L9): Mode Select and External Synchronization Input Pin for Both 5A Switching Mode Regulator Channels. Tie this pin to GND to force continuous synchronous operation. Floating this pin or tying it to $INTV_{CC12}$ enables high efficiency Burst Mode operation at light loads. When drive this pin with an external clock, the phase-locked loop will force the channel 1 turn on signal to be synchronized with the rising edge of the CLKIN12 signal. channel 2 will also be synchronized with the rising edge of the CLKIN12 signal with a 180° phase shift. See Applications Information section for details.

TMON (K8): Temperature Monitor for 5A Output Channels. A voltage proportional to the measured on-die temperature will appear at this pin. The voltage-to-temperature scaling factor is 200°K/V. See the Applications Information section for detailed information on the TMON function. Tie this pin to $INTV_{CC12}$ to disable the temperature monitor circuit.

BLOCK DIAGRAM

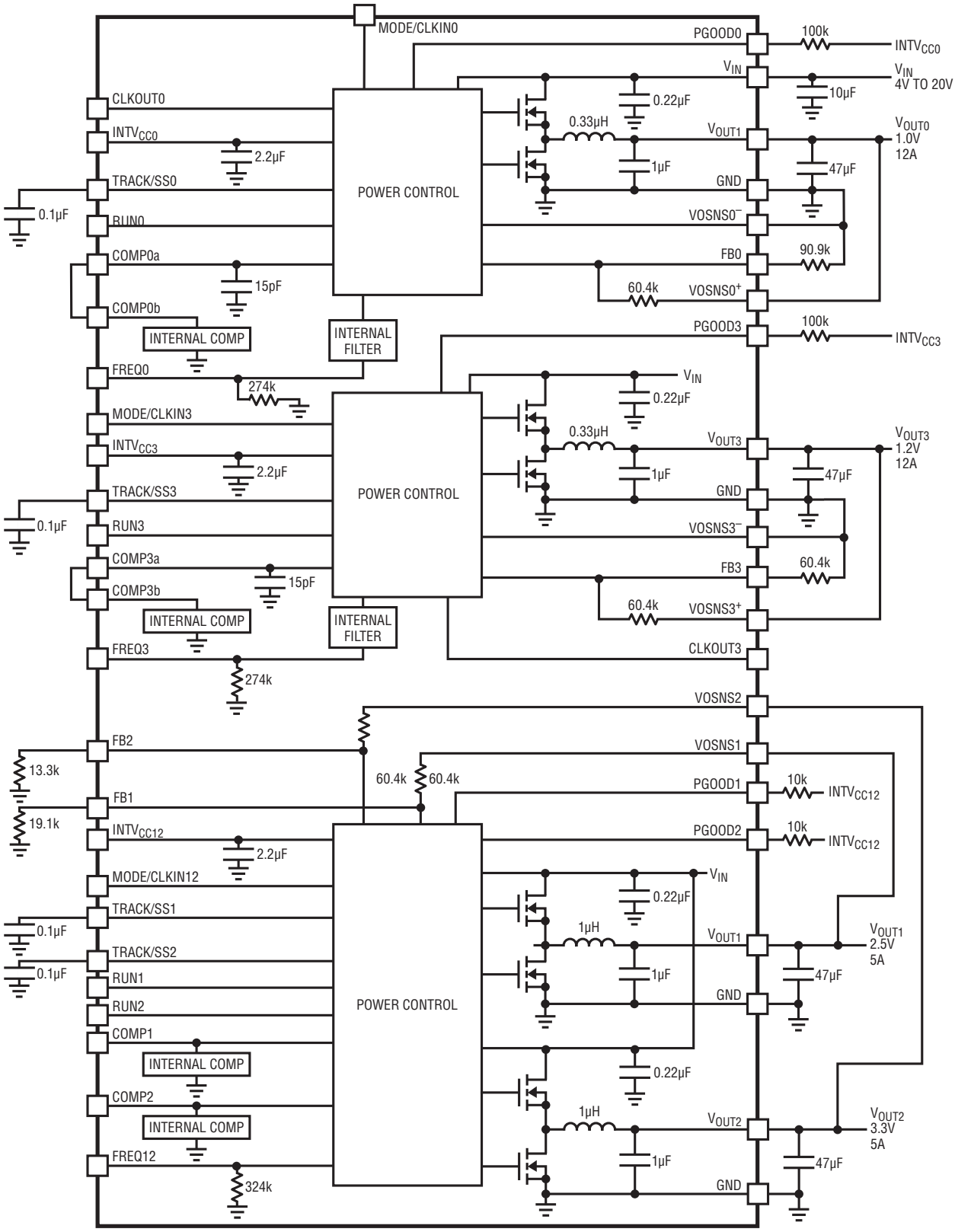


Figure 1. Simplified LTM4671 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)		44	66		µF
C_{OUT0}, C_{OUT3}	External Output Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 12A	100	200		µF
C_{OUT1}, C_{OUT2}	External Output Capacitor Requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 5A	22	47		µF

OPERATION

The LTM4671 is a quad output standalone non-isolated switch mode DC/DC power supply. It has built-in four separate regulator channels which can deliver 12A, 12A, 5A, 5A continuous output current with few external input and output capacitors. Two 12A regulator provides precisely regulated output voltage programmable from 0.6V to 3.3V via a single external resistor over 3.1V to 20V input voltage range while the other two 5A regulator can support output voltage from 0.6V to 5.5V. Dual true differential remote sensing amplifiers are included in the high current channels to get accurate regulation at load point. The typical application schematic is shown in Figure 28.

The LTM4671 has integrated four separate constant on-time valley current mode regulators, power MOSFETs, inductors, and other supporting discrete components. For switching noise-sensitive applications, the switching frequency can be adjusted by external resistors and the µModule can be externally synchronized to a clock. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4671 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors. For Dual 12A output rails, an optional Type II C-R-C external compensation network is allowed to customize the stability and transient performance.

Current mode control provides the flexibility of paralleling any of the separate regulator channels with accurate current sharing. With a build in clock interleaving between each two regulator channels, the LTM4671 could easily employ a 2+1+1 or 2+2 channels parallel operation which is more than flexible in a multirail POL application like FPGA. Furthermore, the LTM4671 has CLKIN and CLKOUT pins for frequency synchronization or PolyPhase multiple devices which allow up to 8 phases of 12A or 5A channels can be cascaded to run simultaneously.

Current mode control also provides cycle-by-cycle fast current monitoring. An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET is turned off and bottom FET is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 0.6V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, Burst Mode operation can be enabled to achieve higher efficiency compared to continuous mode for the dual 5A channels by setting MODE/PLLIN pin floating or tying to $INTV_{CC}$. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

Three different temperature sensing pins are included inside the module to monitor the temperature of the module for different channels. See the Applications Information section for details.

APPLICATIONS INFORMATION

The typical LTM4671 application circuit is shown in Figure 28. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 3 for specific external capacitor requirements for a particular application.

V_{IN} TO V_{OUT} STEP-DOWN RATIOS

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of each regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$D_{(MAX)} = 1 - t_{OFF(MIN)} \bullet f_{SW}$$

where $t_{OFF(MIN)}$ is the minimum off-time, 80ns typical for LTM4671, and f_{SW} is the switching frequency. Conversely, the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$D_{(MIN)} = t_{ON(MIN)} \bullet f_{SW}$$

where $T_{ON(MIN)}$ is the minimum on-time, 25ns typical for LTM4671. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. These constraints are shown in the Typical Performance Characteristic curve labeled "V_{IN} to V_{OUT} Step-Down Ratio." Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

OUTPUT VOLTAGE PROGRAMMING

The PWM controller has an internal 0.6V reference voltage.

For the 12A channels (CH0, CH3), a 60.4k 0.5% internal feedback resistor connects each regulator channel VOSNS$^+$ and FB pin together. Adding a resistor R_{FB} from FB pin to VOSNS$^-$ programs the output voltage.

For the 5A channels (CH1, CH2), a 60.4k 0.5% internal feedback resistor connects each regulator channel VOSNS and FB pin together. Adding a resistor R_{FB} from FB pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

For parallel operation of N-channels, tie the V_{OUT}, the FB pins and VOSNS$^-$ pins together but only hooking up one VOSNS$^+$ (VOSNS) pin to the V_{OUT} so that all the paralleling channels can share the same error amplifier and same top 60.4k feedback resistor. See PolyPhase Operation for details.

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB}(k)	OPEN	90.9	60.4	40.2	30.1	19.1	13.3	8.25

INPUT DECOUPLING CAPACITORS

The LTM4671 module should be connected to a low AC-impedance DC source. For each 12A regulator channel, one piece 22µF input ceramic capacitor is required, for each 5A regulator channel, one piece 10µF input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where η% is the estimated efficiency of the power module.

OUTPUT DECOUPLING CAPACITORS

With an optimized high frequency, high bandwidth design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 3 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 25% load step transient. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more

APPLICATIONS INFORMATION

a function of stability and transient response. The Analog Devices LTpowerCAD® Design Tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

FORCED CONTINUOUS CURRENT MODE (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse.

For the 12A channels (CH0, CH3), CCM can be enabled by tying the MODE/CLKIN0 or MODE/CLKIN3 pin to the respective $INTV_{CC}$ or simply floating it.

For the 5A channels (CH1, CH2), CCM can be enabled by tying the MODE/CLKIN12 pin to GND.

During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4671's output voltage is in regulation.

DISCONTINUOUS MODE/BURST MODE OPERATION

In applications where high efficiency at intermediate current is desired, discontinuous mode or Burst Mode operation can be achieved.

For the 12A channels (CH0, CH3), discontinuous mode (DCM) can be achieved by tying the MODE/CLKIN0 or MODE/CLKIN3 pin to GND. In discontinuous mode, the reverse current comparator will sense the inductor current and turn of bottom MOSFET when the inductor current drops to zero and becomes negative. Both power MOSFETs will remain off with the output capacitor supplying the load current until the COMP voltage rises above its zero current threshold to initiate the next switching cycle.

For the 5A channels (CH1, CH2), Burst Mode operation can be achieved by tying MODE/CLKIN12 pin to $INTV_{CC12}$ or simply floating. In Burst Mode operation, a current reversal comparator (I_{REV}) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off until the ITH voltage rises above the zero current level to initiate another cycle. During this time, the output capacitor supplies the load current and the part is placed into a low current sleep mode.

OPERATING FREQUENCY

The operating frequency of the LTM4671 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 600kHz for 12A channels and 1MHz for 5A channels. In most applications, no additional frequency adjusting is required.

If any operating frequency other than the default is required by application, it can be increased by adding a resistor, R_{FSET}, between the FREQ pin and SGND or be decreased by adding a resistor between the FREQ pin and $INTV_{CC}$. Also the µModule can be externally synchronized to a clock at ±30% around set operating frequency.

FREQUENCY SYNCHRONIZATION AND CLOCK IN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±30% around the set frequency.

A pulse detection circuit is used to detect a clock on the MODE/CLKIN0 pin for CH0 (12A) channel, MODE/CLKIN3 pin for CH3 (12A) channel and MODE/CLKIN12 pin for both CH1 and CH2 5A channels to turn on the phase-locked loop.

The pulse width of the clock has to be at least 400ns. The clock high level must be above 1V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled. When the module is driven with an external clock, forced continuous mode (CCM) is automatically enabled.

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MULTICHANNEL PARALLEL OPERATION

For the application that demand more than 12A of output current, the LTM4671 multiple regulator channels can be easily paralleled to run out of phase to provide more output current without increasing input and output voltage ripples.

For the 12A channels (CH0, CH3), each channel has its own MODE/CLKIN and CLKOUT pin. The CLKOUT signal can be connected to the CLKIN pin of the following stage to line up both frequency and the phase of the entire system. Tying the PHMODE pin to $INTV_{CC}$, SGND or floating the pin generates a phase difference between the clock applied on the MODE/CLKIN pin and CLKOUT of 180° degrees, 120° degrees, or 90° degrees respectively, which corresponds to 2-phase, 3-phase, or 4-phase operation.

For the 5A channels (CH1, CH2), a preset built-in 180° phase different between channel 1 and channel 2. MODE/CLKIN12 allows both channels to be synchronized to an external clock or the CLKOUT signal from any of the 12A channels.

Figure 2 shows a 2 + 2 and a 4-channels parallel concept schematic for clock phasing.

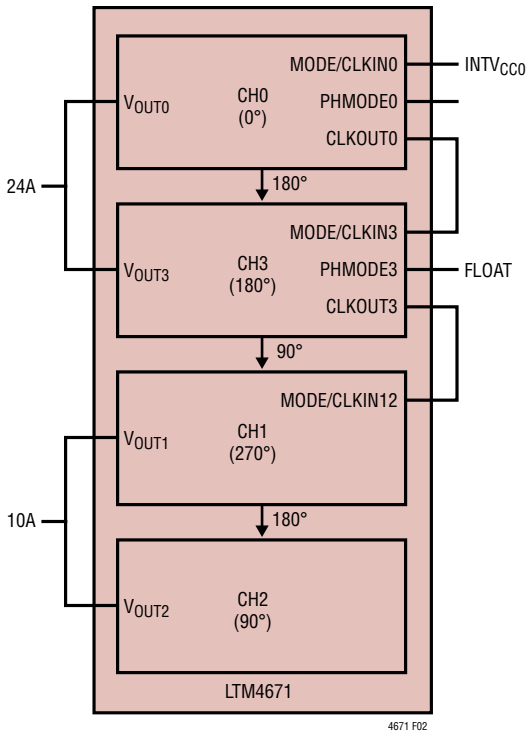

Figure 2. 2 + 2 Parallel Concept Schematic

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4671 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie RUN, TRACK/SS, FB and COMP pins of each paralleling channel together. Figure 29 shows an example of parallel operation and pin connection.

INPUT RMS RIPPLE CURRENT CANCELLATION

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 3 shows this graph.

SOFT-START AND OUTPUT VOLTAGE TRACKING

The TRACK/SS pin provides a means to either soft-start of each regulator channel or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal soft-start current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{I_{SS}}$$

where C_{SS} is the capacitance on the TRACK/SS pin and the I_{SS} is the soft-start current which equals 6µA for the 12A output channels (CH0, CH3) and 1.4µA for the 5A output channels (CH1, CH2).

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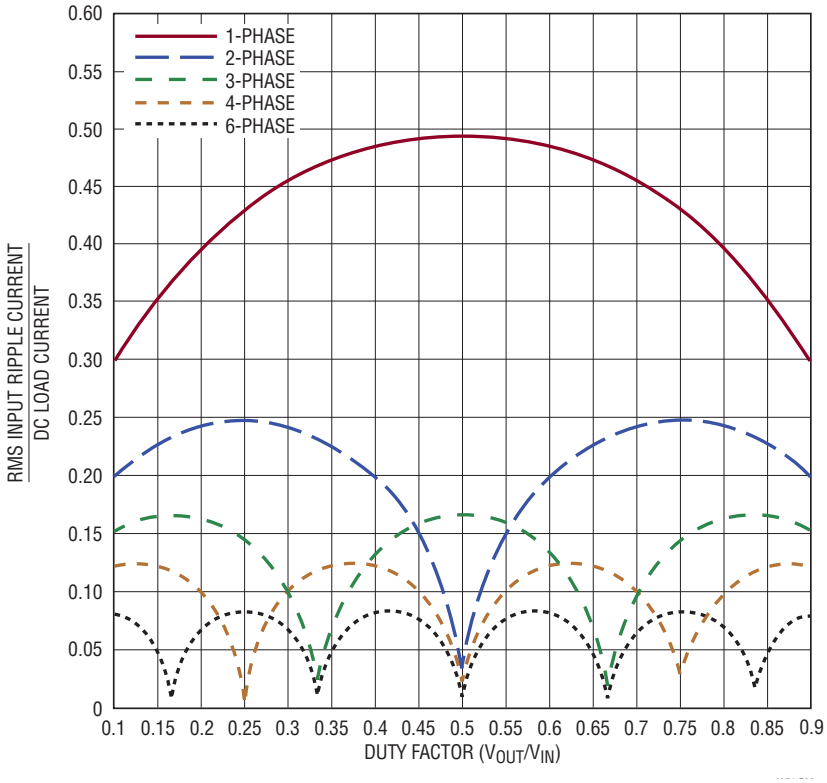

Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

Output voltage tracking can also be programmed externally using the TRACK/SS pin of each regulator channel. The output can be tracked up and down with another regulator. Figure 4 and Figure 5 show an example waveform and schematic of a ratiometric tracking where the slave regulator's (V_{OUT2}, V_{OUT3} and V_{OUT0}) output slew rate is proportional to the master's (V_{OUT1}).

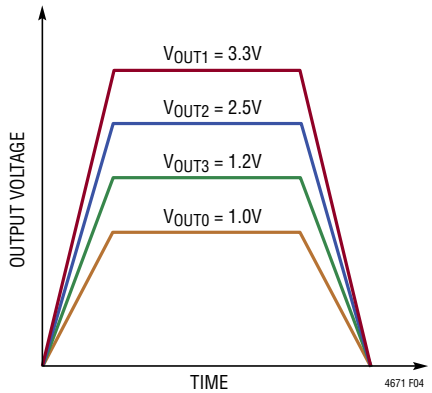

Figure 4. Output Ratiometric Tracking Waveform

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $RTR_{(TOP)}/RTR_{(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 5.

Following the upper equation, the master's output slew rate (MR) and the slave's output slew rate (SR) in Volts/Time is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

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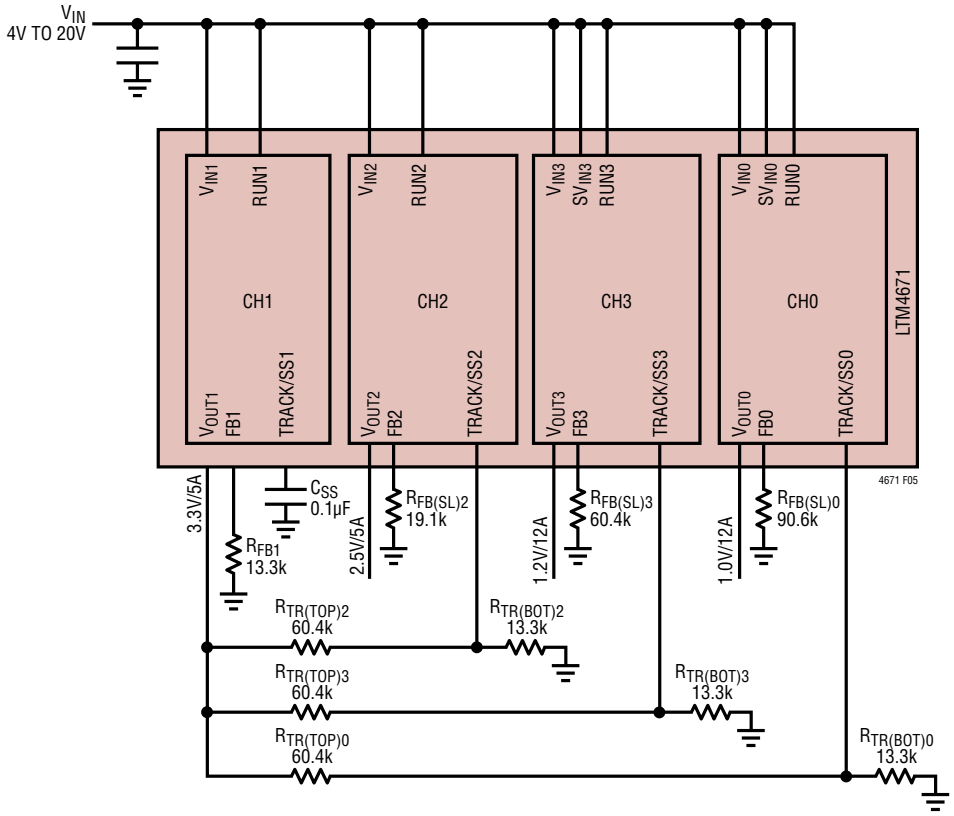

Figure 5. Output Ratiometric Tracking Schematic

For example, $V_{OUT(MA)}$ = 3.3V, MR = 3.3V/ms and $V_{OUT(SL)}$ = 1.0V, SR = 1.0V/ms as V_{OUT1} and V_{OUT0} from the equation, we could solve out that $R_{TR(TOP)0}$ = 60.4k and $R_{TR(BOT)0}$ = 13.3k is a good combination. Follow the same equation, we can get the same $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider value for V_{OUT2} and V_{OUT3}.

The TRACK pins will have the 1.5µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The coincident output tracking can be recognized as a special ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), see Figure 6.

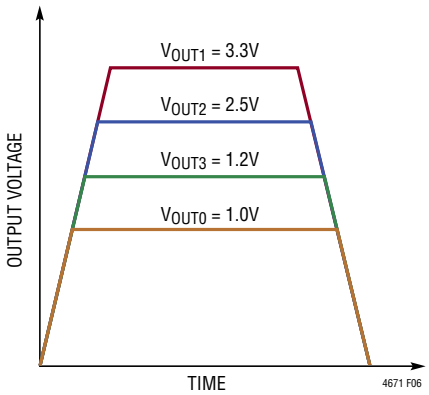

Figure 6. Output Coincident Tracking Waveform

$$\frac{R_{FB(SL)}}{R_{FB(SL)}+60.4k}=\frac{R_{TR(BOT)}}{R_{TR(TOP)}+R_{TR(BOT)}}$$

From the equation, we could easily find out that, in the coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider.

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For example, $R_{TR(TOP)3}$ = 60.4k and $R_{TR(BOT)3}$ = 60.4k is a good combination for coincident tracking for $V_{OUT(MA)}$ = 3.3V and $V_{OUT(SL)}$ =1.2V application.

POWER GOOD

The PGOOD pins are open-drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4671's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

STABILITY COMPENSATION

The LTM4671 module internal compensation loop of each regulator channel is designed and optimized for low ESR ceramic output capacitors only application (COMPb tied to COMPa for 12A channels). Table 3 is provided for most application requirements using the optimized internal compensation. In case of all ceramic output capacitors is required for output ripples or dynamic transient spike reduction, an additional 10pF to 15pF phase boost cap is required between V_{OUT} and FB pins.

For specific optimized requirement for the dual 12A channels, disconnect COMPb from COMPa and apply a Type II C-R-C compensation network from COMPa to SGND to achieve external compensation.

The LTpowerCAD design tool is available to download online to perform specific control loop optimization and analyze the control stability and load transient performance.

RUN ENABLE

Pulling the RUN pin of each regulator channel to ground forces the regulator into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN pin voltage above 1.2V will turn on the entire regulator channel.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection

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causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.

4. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

5. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 7; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED 51-9 to

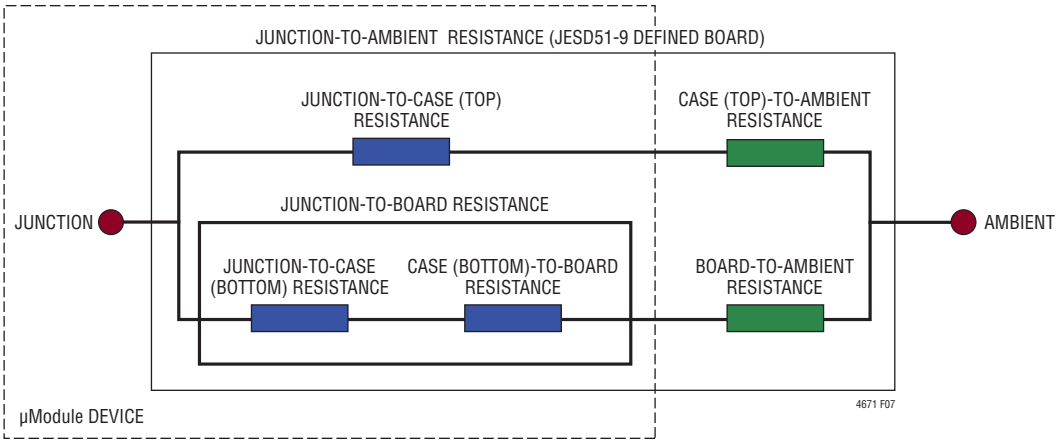

Figure 7. Graphical Representation of JESD51-12 Thermal Coefficients

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predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This θ_{JB} + θ_{BA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1V to 5V power loss curves in Figure 8 to Figure 14 can be used in coordination with the load current derating curves in Figure 15 to Figure 24 for calculating an approximate θ_{JA} thermal resistance for the LTM4671 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature and are increased with a multiplicative factor according to the junction temperature. This approximate factor is 1.3 considering internal junction temperature hitting 120°C at the point of derating starts. The derating curves are taken with three different output power combinations, low power (V_{OUT0} = V_{OUT3} = 1V, V_{OUT1} = V_{OUT2} = 1.5V), medium power (V_{OUT0} = V_{OUT3} = 1.8V, V_{OUT1} = V_{OUT2} = 3.3V) and high power (V_{OUT0} = V_{OUT3} = 3.3V, V_{OUT1} = V_{OUT2} = 5V). Output current starting at 100% of the full load current (I_{OUT0} = I_{OUT3} = 12A, I_{OUT1} = I_{OUT2} = 5A) and the ambient temperature starting at 30°C. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. The printed circuit board for this test is a 1.6mm thick six layers board with two ounce copper for the two outer layers and one ounce copper for the four inner layers. The PCB dimensions are 121mm × 112mm.

Figure 25 and Figure 26 display the maximum power loss allowance curves vs ambient temperature with various heat sinking and airflow conditions. This data was derived from the thermal derating curves in Figure 15 to Figure 24 with the junction temperature measured at 120°C. This maximum power loss limitation serves as a guideline when designing multiple output rails with different voltages and currents by calculating the total power loss. For example, to determine the maximum ambient temperature when V_{IN} = 12V, V_{OUT0} = 1V at 10A, V_{OUT1} = 1.8V at 3A, V_{OUT2} = 3.3V at 2A, V_{OUT3} = 1.5V at 10A, without a heat sink and any airflow, simply add up the total power loss for each channel read from Figure 8 to Figure 14 which in this example equals 4.8W (1.6W + 0.7W + 0.6W + 1.9W), then multiply by the 1.3 coefficient for 120°C junction temperature and compare the total power loss number, 6.3W with Figure 25. Figure 25 indicates with a 6.3W total power loss, the maximum ambient temperature for this application is around 66°C. Also from Figure 25, it is easy to determine with a 6.3W total power loss, the maximum ambient temperature is around 73°C with 200LFM airflow and 77°C with 400LFM airflow.

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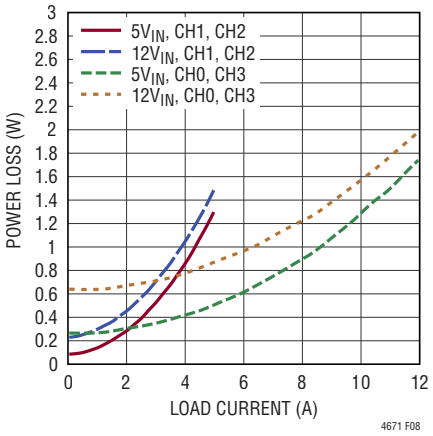

Figure 8. 1V Output Power Loss

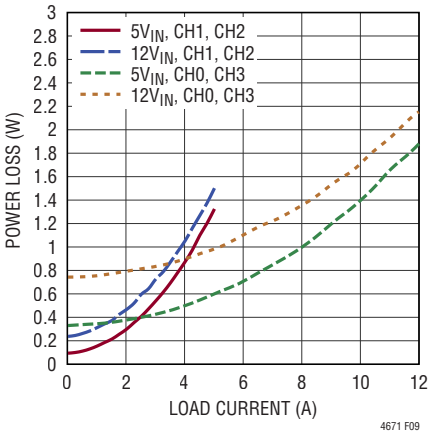

Figure 9. 1.2V Output Power Loss

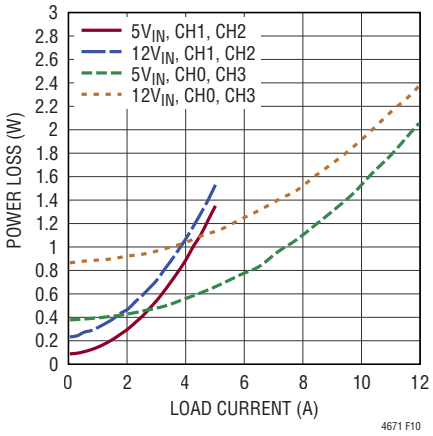

Figure 10. 1.5V Output Power Loss

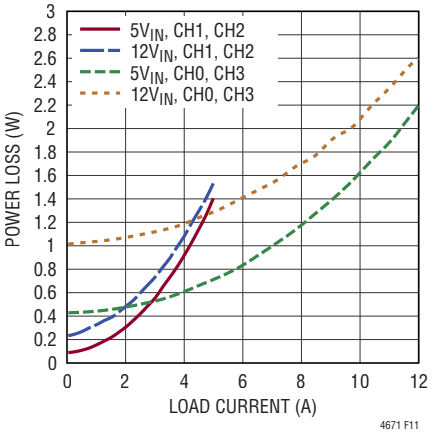

Figure 11. 5V Output Power Loss

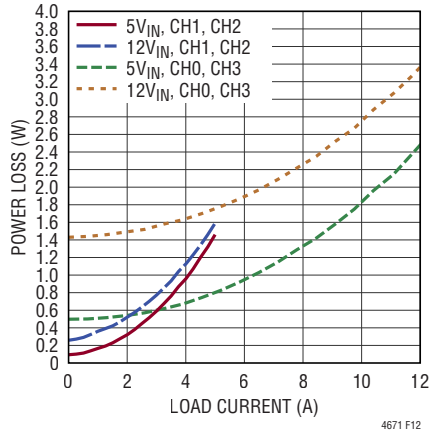

Figure 12. 2.5V Output Power Loss

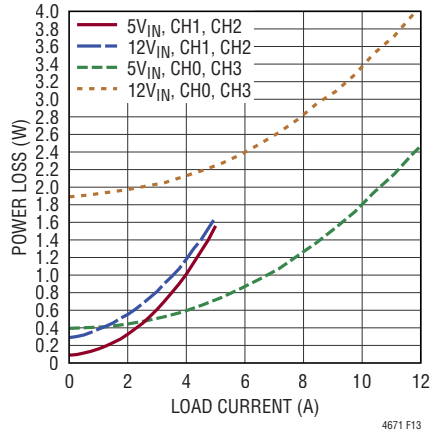

Figure 13. 3.3V Output Power Loss

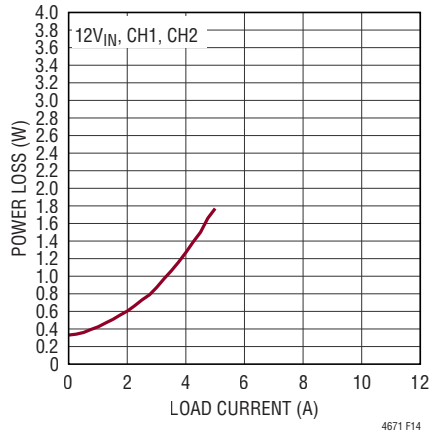

Figure 14. 5V Output Power Loss

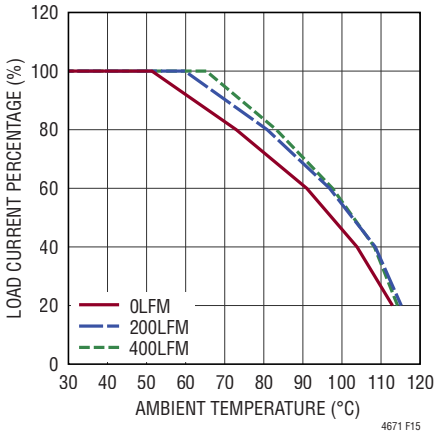

Figure 15. $5V_{IN}$ Derating Curve, No Heat Sink CH0 and CH3 Paralleled to 1V/24A CH1 and CH2 Paralleled to 1.5V/10A

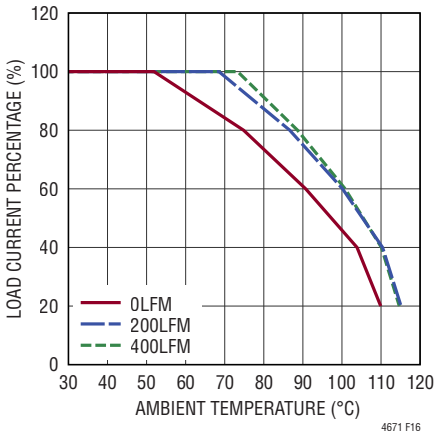

Figure 16. $5V_{IN}$ Derating Curve, with Heat Sink CH0 and CH3 Paralleled to 1V/24A CH1 and CH2 Paralleled to 1.5V/10A

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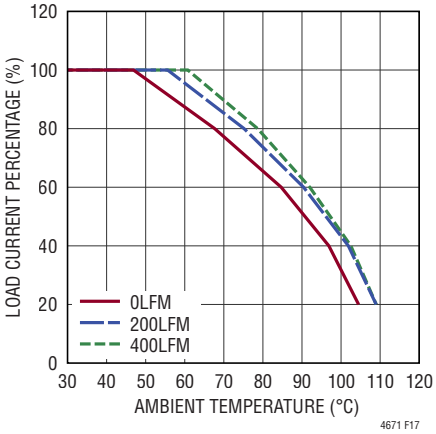


Figure 17. 12V_{IN} Derating Curve, No Heat Sink CH0 and CH3 Paralleled to 1V/24A CH1 and CH2 Paralleled to 1.5V/10A

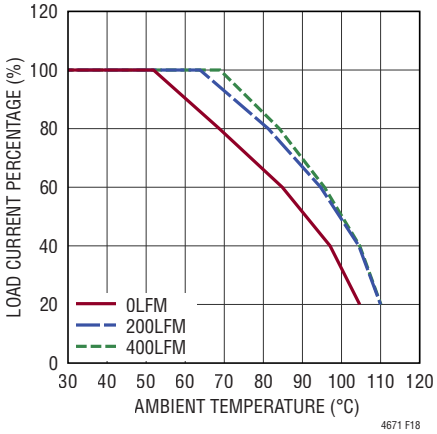


Figure 18. 12V_{IN} Derating Curve, with Heat Sink CH0 and CH3 Paralleled to 1V/24A CH1 and CH2 Paralleled to 1.5V/10A

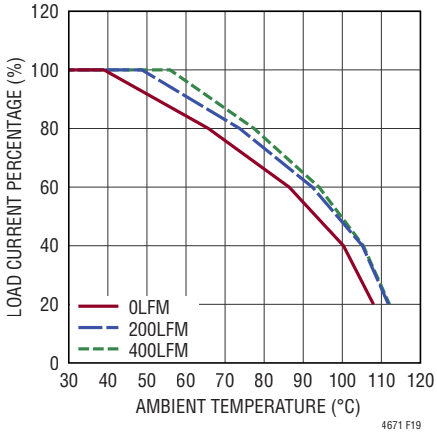


Figure 19. 5V_{IN} Derating Curve, No Heat Sink CH0 and CH3 Paralleled to 1.8V/24A CH1 and CH2 Paralleled to 3.3V/10A

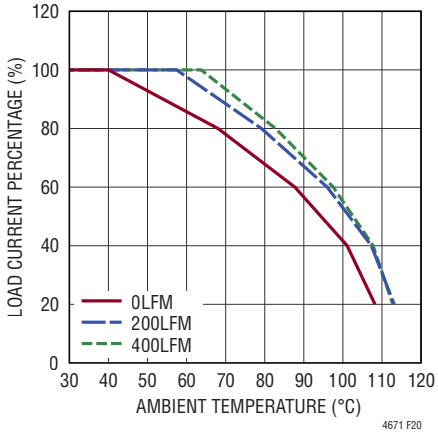


Figure 20. 5V_{IN} Derating Curve, with Heat Sink CH0 and CH3 Paralleled to 1.8V/24A CH1 and CH2 Paralleled to 3.3V/10A

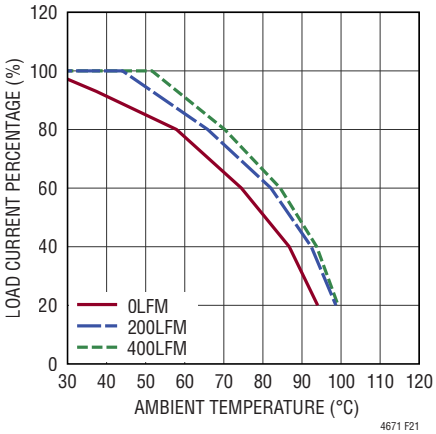


Figure 21. 12V_{IN} Derating Curve, No Heat Sink CH0 and CH3 Paralleled to 1.8V/24A CH1 and CH2 Paralleled to 3.3V/10A

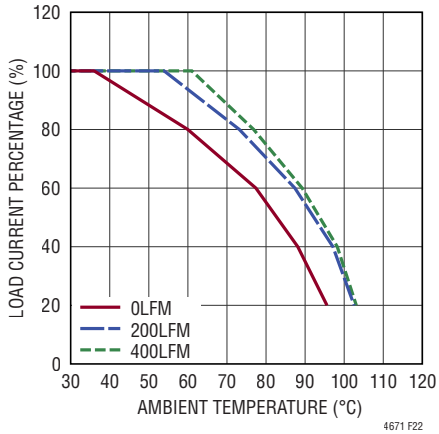


Figure 22. 12V_{IN} Derating Curve, with Heat Sink CH0 and CH3 Paralleled to 1.8V/24A CH1 and CH2 Paralleled to 3.3V/10A

APPLICATIONS INFORMATION

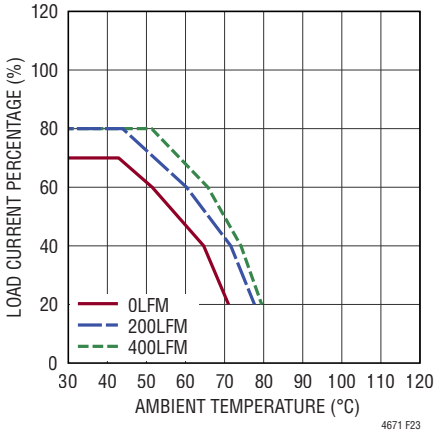


Figure 23. $12V_{IN}$ Derating Curve, No Heat Sink CH0 and CH3 Paralleled to 3.3V/24A CH1 and CH2 Paralleled to 5V/10A

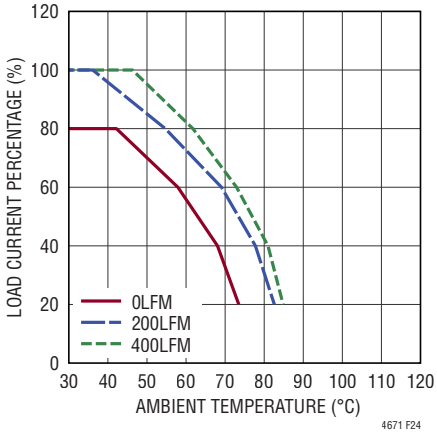


Figure 24. $12V_{IN}$ Derating Curve, with Heat Sink CH0 and CH3 Paralleled to 3.3V/24A CH1 and CH2 Paralleled to 5V/10A

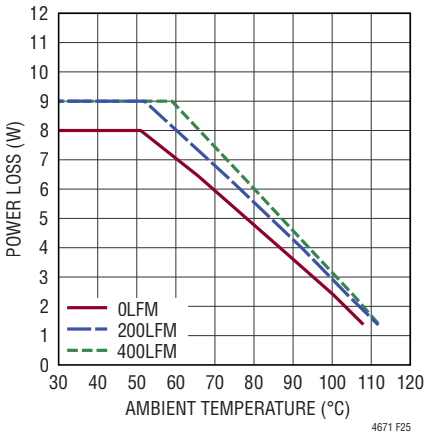


Figure 25. Power Loss Allowance vs Ambient Temperature No Heat Sink

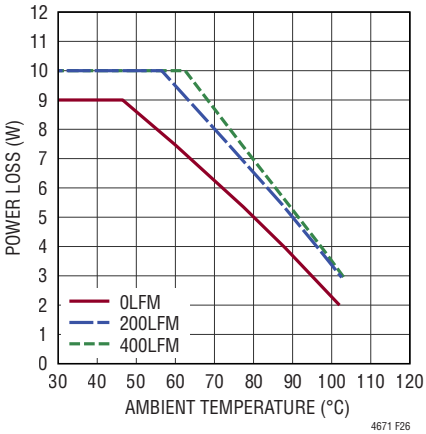


Figure 26. Power Loss Allowance vs Ambient Temperature with Heat Sink

APPLICATIONS INFORMATION

Table 2. Different Output, Junction-to-Ambient Thermal Resistance (θ_{JA})

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 25	5, 12	Figure 8 to Figure 14	0	None	8.5
Figure 25	5, 12	Figure 8 to Figure 14	200	None	7
Figure 25	5, 12	Figure 8 to Figure 14	400	None	6.5
Figure 26	5, 12	Figure 8 to Figure 14	0	BGA Heat Sink	8
Figure 26	5, 12	Figure 8 to Figure 14	200	BGA Heat Sink	6
Figure 26	5, 12	Figure 8 to Figure 14	400	BGA Heat Sink	5.5

Table 3. Output Voltage Response vs Component Matrix (Refer to Figure 28) 0A to 4A Load Step Typical Measured Values

C_{IN} (CERAMIC)			C_{OUT} (CERAMIC)			C_{OUT} (BULK)		
VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER
Murata	22µF, 25V, X5R, 1206	GRT31CR61E226ME01L	Murata	47µF, 6.3V, X5R, 0805	GRM21BR60J476ME15K	Panasonic	680µF, 6.3V, 25mΩ	6TPE330ML
Murata	22µF, 25V, X5R, 1210	GRM32ER61E226KE15K	Murata	100µF, 6.3V, X5R, 1210	GRM32ER60J107ME20L			
Taiyo Yuden	22µF, 25V, X5R, 1206	TMK316BBJ226ML-T	Taiyo Yuden	47µF, 6.3V, X5R, 0805	JMK212BBJ476MG-T			
			Taiyo Yuden	100µF, 6.3V, X5R, 1210	JMK325BJ107MM-T			

CH0 and CH3 Transient Response

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN}* (BULK)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	C_{TH} (pF)	R_{TH} (kΩ)	C_{FF} (pF)	V_{IN} (V)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (k)
1	22 × 2	100	100 × 3	NA	1500	5	33	5, 12	79.7	30	3	10	90.9
1	22 × 2	100	100	330	1000	8	NA	5, 12	76.3	30	3	10	90.9
1.2	22 × 2	100	100 × 3	NA	1500	5	33	5, 12	83.7	30	3	10	60.4
1.2	22 × 2	100	100	330	1000	8	NA	5, 12	80	30	3	10	60.4
1.5	22 × 2	100	100 × 3	NA	1500	5	33	5, 12	90.4	30	3	10	40.2
1.5	22 × 2	100	100	330	1000	8	NA	5, 12	89.7	40	3	10	40.2
1.8	22 × 2	100	100 × 3	NA	1500	5	33	5, 12	103.8	30	3	10	30.1
1.8	22 × 2	100	100	330	1000	8	NA	5, 12	99.1	40	3	10	30.1
2.5	22 × 2	100	100	330	1000	8	NA	5, 12	147.3	50	3	10	19.1
3.3	22 × 2	100	100	330	1000	8	NA	5, 12	203	50	3	10	13.3

CH1 and CH2 Transient Response

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN}* (BULK)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	C_{TH} (pF)	R_{TH} (kΩ)	C_{FF} (pF)	V_{IN} (V)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (k)
1	22	100	47 × 2	NA	Internal	Internal	100	5, 12	56.9	50	1.25	10	90.9
1.2	22	100	47 × 2	NA	Internal	Internal	100	5, 12	57.8	60	1.25	10	60.4
1.5	22	100	47 × 2	NA	Internal	Internal	100	5, 12	62.3	60	1.25	10	40.2
1.8	22	100	47 × 2	NA	Internal	Internal	100	5, 12	67.6	70	1.25	10	30.1
2.5	22	100	47 × 2	NA	Internal	Internal	100	5, 12	85.7	70	1.25	10	19.1
3.3	22	100	47 × 2	NA	Internal	Internal	100	12	115	70	1.25	10	13.3
5	22	100	47 × 2	NA	Internal	Internal	100	12	167	70	1.25	10	8.25

*Optional

APPLICATIONS INFORMATION

SAFETY CONSIDERATIONS

The LTM4671 modules do not provide galvanic isolation from VIN to VOUT. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4671 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 27 gives a good example of the recommended layout.

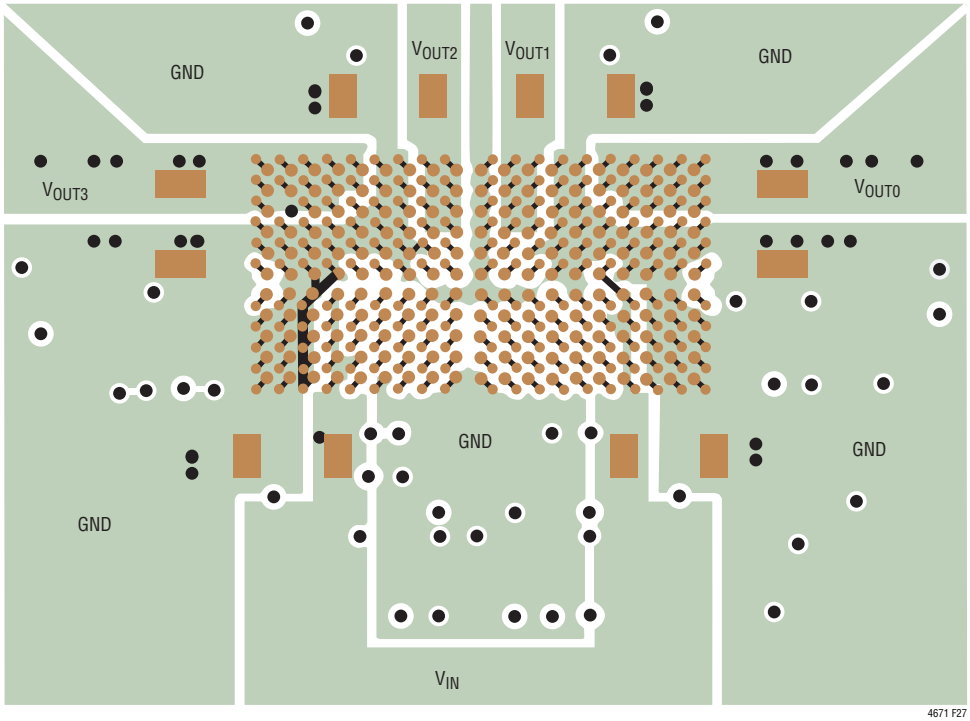


Figure 27. Recommended PCB Layout

TYPICAL APPLICATIONS

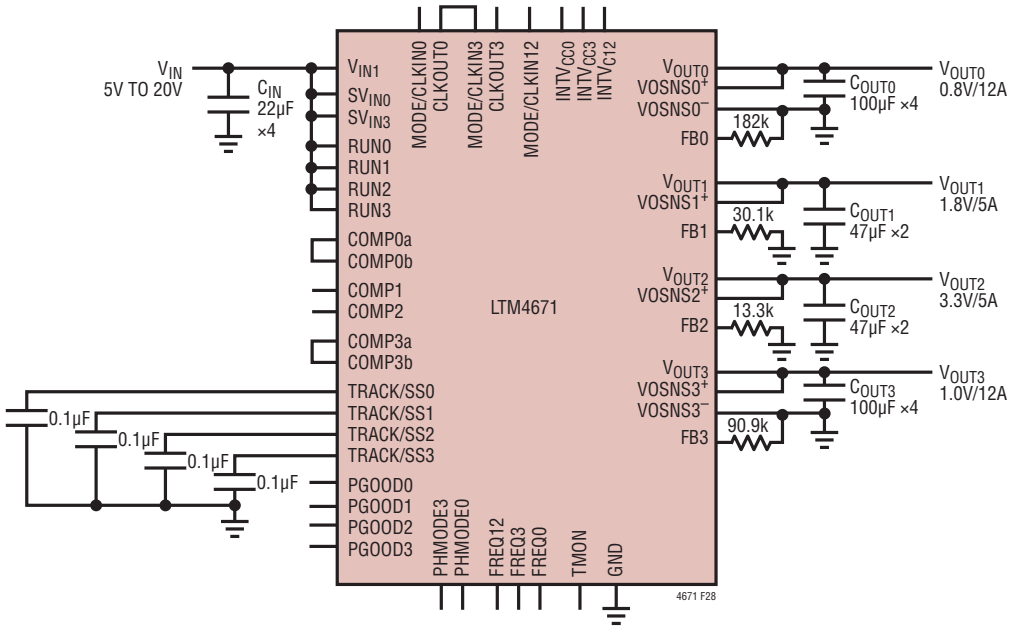
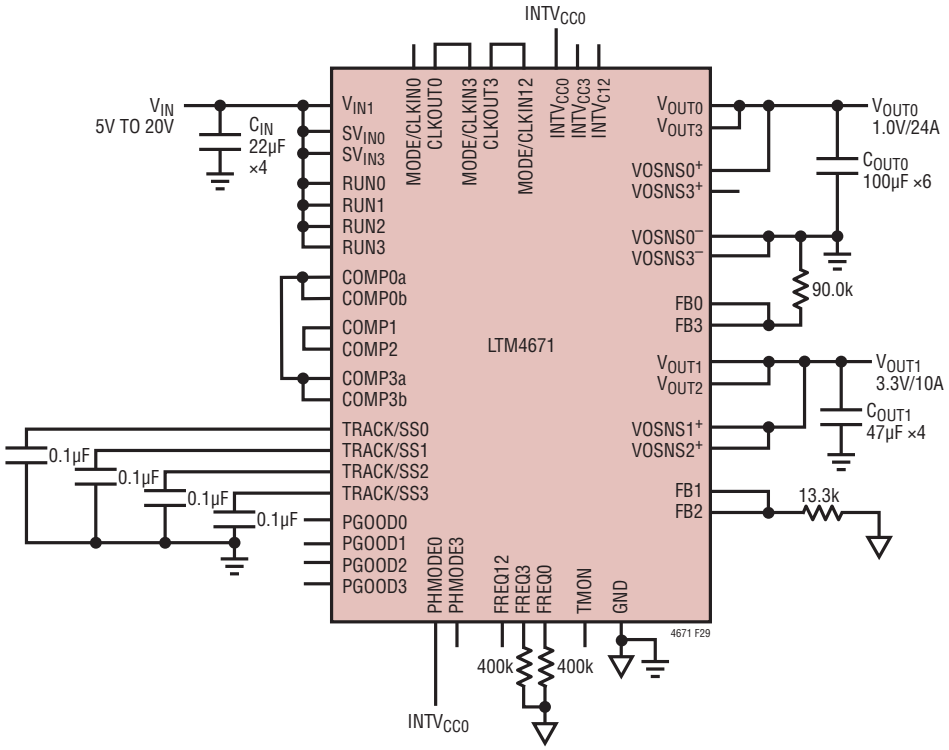


Figure 28. 5V to 20V Input, Quad Output Design



	CH0	CH1	CH2	CH3
Phase Shift	180°		90°	180°
Phase	0°	180°	270°	90°

Figure 29. Parallel Operation with 1MHz Clock and Interleaved Phases

TYPICAL APPLICATIONS

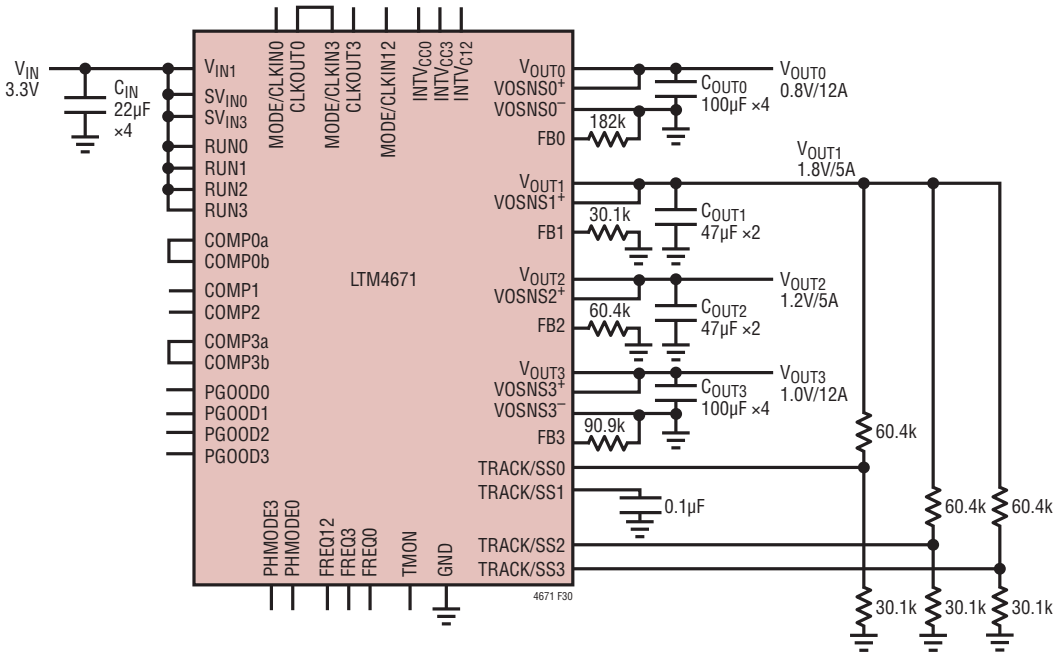


Figure 30. 3.3V_{IN} , 1.8V, 1.2V, 1V, 0.8V with Ratiometric Tracking

COMPONENT BGA PINOUT

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT0}	B1	V_{OUT0}	C1	V_{OUT0}	D1	V_{OUT0}	E1	V_{OUT0}
A2	V_{OUT0}	B2	V_{OUT0}	C2	V_{OUT0}	D2	V_{OUT0}	E2	V_{OUT0}
A3	V_{OUT0}	B3	V_{OUT0}	C3	V_{OUT0}	D3	V_{OUT0}	E3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND
A6	$TSENSE0^-$	B6	GND	C6	GND	D6	GND	E6	PHMODE0
A7	$TSENSE0^+$	B7	GND	C7	GND	D7	V_{IN}	E7	$INTV_{CC0}$
A8	GND	B8	GND	C8	GND	D8	V_{IN}	E8	V_{IN}
A9	GND	B9	GND	C9	GND	D9	V_{IN}	E9	SV_{IN0}
A10	GND	B10	GND	C10	GND	D10	V_{IN}	E10	CLKOUT0
A11	GND	B11	GND	C11	GND	D11	V_{IN}	E11	PGOOD0

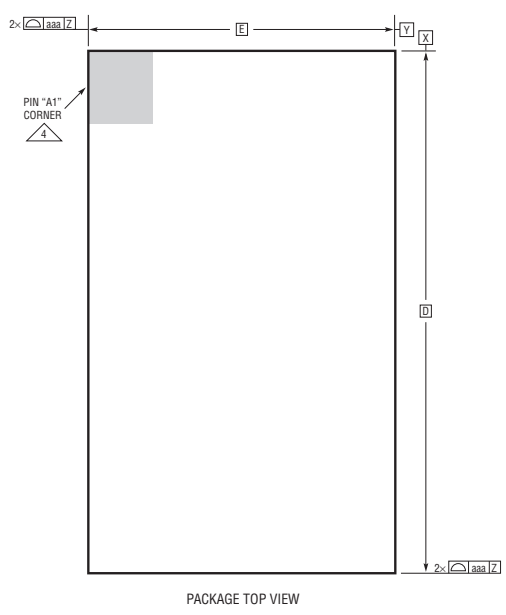
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
F1	GND	G1	GND	H1	V_{OUT1}	J1	V_{OUT1}	K1	GND
F2	GND	G2	GND	H2	V_{OUT1}	J2	V_{OUT1}	K2	GND
F3	GND	G3	GND	H3	V_{OUT1}	J3	V_{OUT1}	K3	GND
F4	GND	G4	GND	H4	V_{OUT1}	J4	V_{OUT1}	K4	GND
F5	GND	G5	GND	H5	GND	J5	V_{IN}	K5	GND
F6	GND	G6	GND	H6	V_{IN}	J6	V_{IN}	K6	GND
F7	GND	G7	TRACK/SS1	H7	GND	J7	GND	K7	GND
F8	$VOSNS0^-$	G8	$V0SNS0^+$	H8	PGOOD1	J8	RUN1	K8	TMON
F9	TRACK/SS0	G9	FB0	H9	FB1	J9	GND	K9	$INTV_{CC12}$
F10	FREQ0	G10	GND	H10	COMP0a	J10	$VOSNS1^+$	K10	FREQ12
F11	RUN0	G11	MODE/CLKIN0	H11	COMP0b	J11	COMP1	K11	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
L1	V_{OUT2}	M1	V_{OUT2}	N1	GND	P1	GND	R1	V_{OUT3}
L2	V_{OUT2}	M2	V_{OUT2}	N2	GND	P2	GND	R2	V_{OUT3}
L3	V_{OUT2}	M3	V_{OUT2}	N3	GND	P3	GND	R3	GND
L4	V_{OUT2}	M4	V_{OUT2}	N4	GND	P4	GND	R4	GND
L5	V_{IN}	M5	GND	N5	GND	P5	GND	R5	GND
L6	V_{IN}	M6	V_{IN}	N6	GND	P6	CLKOUT3	R6	PHMODE3
L7	GND	M7	GND	N7	TRACK/SS2	P7	RUN3	R7	PGOOD3
L8	RUN2	M8	PGOOD2	N8	COMP3b	P8	FREQ3	R8	MODE/CLKIN3
L9	MODE/CLKIN12	M9	FB2	N9	COMP3a	P9	TRACK/SS3	R9	SV_{IN3}
L10	$V0SNS2^+$	M10	GND	N10	FB3	P10	$V0SNS3^-$	R10	V_{IN}
L11	GND	M11	COMP2	N11	$V0SNS3^+$	P11	GND	R11	$INTV_{CC3}$

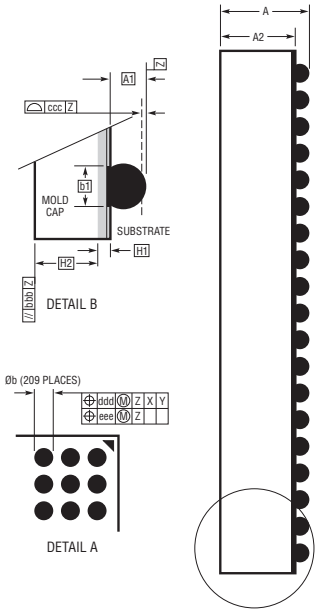
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
T1	V_{OUT3}	U1	V_{OUT3}	V1	V_{OUT3}	W1	V_{OUT3}
T2	V_{OUT3}	U2	V_{OUT3}	V2	V_{OUT3}	W2	V_{OUT3}
T3	V_{OUT3}	U3	V_{OUT3}	V3	V_{OUT3}	W3	V_{OUT3}
T4	GND	U4	GND	V4	GND	W4	GND
T5	GND	U5	GND	V5	GND	W5	GND
T6	GND	U6	GND	V6	GND	W6	$TSENSE3^+$
T7	V_{IN}	U7	GND	V7	GND	W7	$TSENSE3^-$
T8	V_{IN}	U8	GND	V8	GND	W8	GND
T9	V_{IN}	U9	GND	V9	GND	W9	GND
T10	V_{IN}	U10	GND	V10	GND	W10	GND
T11	V_{IN}	U11	GND	V11	GND	W11	GND

PACKAGE DESCRIPTION

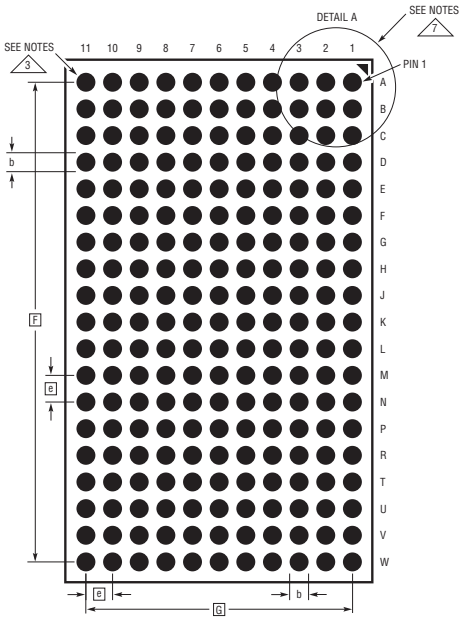
BGA Package
209-Lead (16mm × 9.50mm × 4.72mm)
(Reference LTC DWG# 05-08-1561 Rev B)



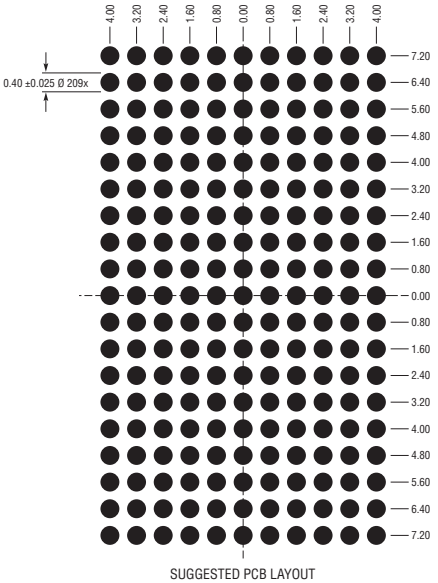
PACKAGE TOP VIEW



DETAIL B
PACKAGE SIDE VIEW



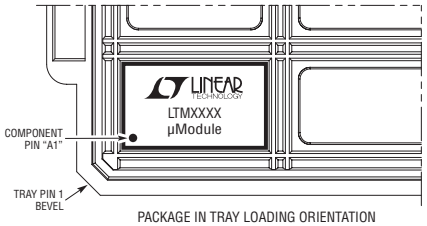
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	4.53	4.72	4.91	
A1	0.30	0.40	0.50	BALL HT
A2	4.23	4.32	4.41	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		16.00		
E		9.50		
e		0.80		
F		14.40		
G		8.00		
H1		0.32		SUBSTRATE THK
H2		4.00		MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 209				

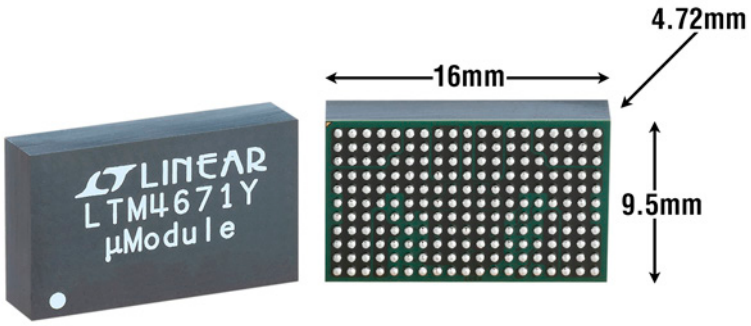
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



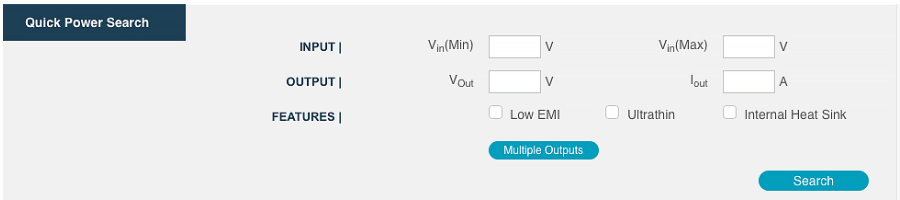
PACKAGE IN TRAY LOADING ORIENTATION

BGA 209 0218 REV B

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4644	Quad 4A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 14V$, $0.6V \le V_{OUT} \le 5.5V$, 9mm × 15mm × 5.01mm BGA
LTM4633	Triple 3A Step-Down µModule Regulator	$4.7V \le V_{IN} \le 16V$, $0.8V \le V_{OUT1}$ and $V_{OUT2} \le 1.8V$, $0.8V \le V_{OUT3} \le 5.5V$, 15mm × 15mm × 5.01mm BGA
LTM4622	Ultrathin, Dual 2.5A or Single 5A Step-Down µModule Regulator	$3.6V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm x 6.25mm × 2.42mm BGA
LTM4646	Dual 10A or Single 20A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 11.25mm × 15mm × 5.01mm BGA
LTM4662	Dual 15A or Single 30A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 11.25mm × 15mm × 5.74mm BGA
LTM4650A	Dual 25A or Single 50A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 5.5V$, 16mm × 16mm × 4.41mm LGA, 16mm × 16mm × 5.01mm BGA
LTM4626	12A µModule Regulator	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule Regulator	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 5.02mm BGA