

Wideband, High Gain VOLTAGE LIMITING AMPLIFIER

FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 1ns
- LIMITING VOLTAGE ACCURACY: ±10mV
- –3dB BANDWIDTH (G = +6): 260MHz
- GAIN BANDWIDTH PRODUCT: 1000MHz
- STABLE FOR G ≥ +4V/V
- SLEW RATE: 1400V/μs
- ±5V AND +5V SUPPLY OPERATION
- LOW GAIN VERSION: OPA698

APPLICATIONS

- TRANSIMPEDANCE WITH FAST OVERDRIVE RECOVERY
- FAST LIMITING ADC INPUT DRIVER
- LOW PROP DELAY COMPARATOR
- NONLINEAR ANALOG SIGNAL PROCESSING
- DIFFERENCE AMPLIFIER
- IF LIMITING AMPLIFIER
- OPA689 UPGRADE

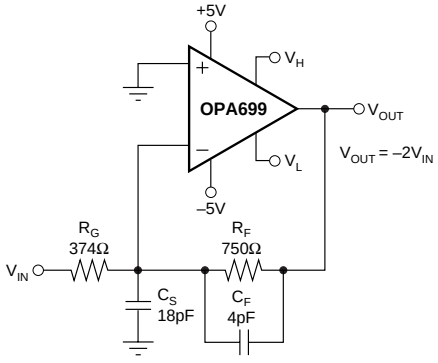
DESCRIPTION

The OPA699 is a wideband, voltage-feedback op amp that offers bipolar output voltage limiting, and is stable for gains ≥ +4. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±10mV. The op amp operates linearly to within 20mV of the limits.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 1ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA699 to be used in all standard op amp applications.

Nonlinear analog signal processing circuits will benefit from the OPA699 sharp transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

The OPA699 is available in an industry-standard pinout in an SO-8 package. For lower gain applications requiring output limiting with fast recovery, consider the OPA698.



Low Gain, Improved SFDR Amplifier with Output Limiting

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Input Voltage Range	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Limiter Voltage Range	$\pm(V_S - 0.7V)$
Storage Temperature Range: D	–65°C to +125°C
Lead Temperature (SO-8, soldering, 3s)	+260°C
Junction Temperature	+150°C
ESD Resistance: HBM	2000V
MM	200V
CDM	1000V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RELATED PRODUCTS

	SINGLES	DUALS	DESCRIPTION
Output Limiting	OPA698		Unity Gain Stable, Wideband
Voltage Feedback	OPA690	OPA2690	High Slew, Unity Gain Stable

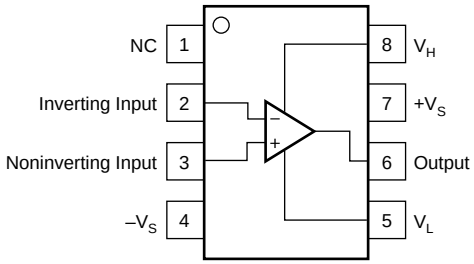
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA699	SO-8	D	–40°C to +85°C	OPA699ID	OPA699ID	Rails, 100
"	"	"	"	"	OPA699IDR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

Top View **SO**



NC = No Connection

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C**.

G = +6, R_F = 750Ω, R_L = 500Ω, and $V_H = -V_L$ = 2V, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA699ID TYP +25°C	OPA699ID MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small Signal Bandwidth (V_O < 0.5V_{PP})	G = +6	260	220	215	210	MHz	min	B
	G = +12	86				MHz	typ	C
	G = –6	269				MHz	typ	C
Gain Bandwidth Product (G ≥ +20)	V_O < 0.5V_{PP}, G = +6	1000	820	800	750	MHz	min	B
Gain Peaking	V_O < 0.5V_{PP}, G = +4	7.5				dB	typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.5V_{PP}	30				MHz	typ	C
Large-Signal Bandwidth	V_O = 4V_{PP}	290	190	180	170	MHz	min	B
Step Response								
Slew Rate	4V Step	1400	1300	1200	1100	V/µs	min	B
Rise-and-Fall Time	0.5V Step	1.6	1.65	1.8	2	ns	max	B
Settling Time: 0.05%	2V Step	8				ns	typ	C
Spurious-Free Dynamic Range, Even	f = 5MHz, V_O = 2V_{PP}	67	64	62	60	dB	min	B
Odd	f = 5MHz, V_O = 2V_{PP}	87	85	84	80	dB	min	B
Differential Gain	NTSC, PAL, R_L = 500Ω	0.012				%	typ	C
Differential Phase	NTSC, PAL, R_L = 500Ω	0.008				°	typ	C
Input Noise Density								
Voltage Noise	f ≥ 1MHz	4.1	4.6	5.2	5.5	nV/√Hz	max	B
Current Noise	f ≥ 1MHz	2.0	2.5	2.7	2.9	pA/√Hz	max	B
DC PERFORMANCE (V_{CM} = 0V)								
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.5V	66	**58**	56	55	dB	min	A
Input Offset Voltage		±1.5	**±5.0**	±6	±7	mV	max	A
Average Drift		—		±15	±20	µV/°C	max	B
Input Bias Current(4)		+3	**±10**	±11	±12	µA	max	A
Average Drift		—		±15	±20	nA/°C	max	B
Input Offset Current		±0.3	**±2**	±2.5	±3	µA	max	A
Average Drift		—		±10	±10	nA/°C	max	B
INPUT								
Common-Mode Rejection Ratio	Input Referred, V_{CM} = ±0.5V	61	**55**	54	52	dB	min	A
Common-Mode Input Range(5)		±3.3	**±3.2**	±3.2	±3.1	V	min	A
Input Impedance								
Differential-Mode		0.32 || 1				MΩ || pF	typ	C
Common-Mode		3.5 || 1				MΩ || pF	typ	C
OUTPUT	$V_H = -V_L$ = 4.3V							
Output Voltage Range	R_L ≥ 500Ω	±4.1	**±3.9**	±3.9	±3.8	V	min	A
Current Output, Sourcing		+120	**+90**	+85	+80	mA	min	A
Sinking		–120	**–90**	–85	–80	mA	min	A
Closed-Loop Output Impedance	G = +4, f < 100kHz	0.8				Ω	typ	C
POWER SUPPLY								
Operating Voltage, Specified		±5				V	typ	C
Maximum		—	**±6**	±6	±6	V	max	A
Quiescent Current, Maximum	V_S = ±5V	15.5	**15.9**	16.3	16.6	mA	max	A
Minimum	V_S = ±5V	15.5	**15.2**	14.9	14.6	mA	min	A
Power-Supply Rejection Ratio	$+V_S$ = 4.5V to 5.5V							
+PSRR (Input Referred)		75	**68**	67	66	dB	min	A

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C Test Level A specifications. Junction temperature = ambient temperature + 23°C at high temperature limit Test Level A specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +1°C at high temperature limit for over-temperature tested specifications.
(3) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only.
(4) Current is considered positive out-of-node.
(5) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
(6) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3 and Figures 1 and 12.
(7) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

Boldface limits are tested at **+25°C.**

G = +6, R_F = 750Ω, R_L = 500Ω, $V_H = -V_L$ = 2V, (Figure 1 for AC performance only), unless otherwise noted.

		OPA699ID						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
OUTPUT VOLTAGE LIMITERS	Pins 5 and 8							
Output Voltage Limited Range		±3.8					typ	C
Default Limit Voltage, Upper	Limiter Pins Open	+3.5	**+3.3**	+3.2	+3.1	V	min	A
Lower		–3.5	**–3.3**	–3.2	–3.1	V	max	A
Minimum Limiter Separation ($V_H - V_L$)		400	400	400	400	mV	min	B
Maximum Limit Voltage		—	±4.3	±4.3	±4.3	V	max	B
Limiter Input Bias Current Magnitude[6]	V_O = 0							
Maximum		50	**60**	62	64	µA	max	A
Minimum		50	**40**	38	36	µA	min	A
Average Drift		—		30	35	nA/°C	max	B
Limiter Input Impedance		3.4 || 1				MΩ || pF	typ	C
Limiter Feedthrough[7]	f = 5MHz	–60				dB	typ	C
DC Performance in Limit Mode	V_{IN} = ±0.7V							
Limiter Offset Voltage	($V_O - V_H$) or ($V_O - V_L$)	±10	**±30**	±35	±40	mV	max	A
Op Amp Input Bias Current Shift[4]	Linear ↔ Limited Operation	3				µA	typ	C
AC Performance in Limit Mode								
Limiter Small-Signal Bandwidth	V_{IN} = ±0.7V, V_O < 0.02V_{PP}	600				MHz	typ	C
Limiter Slew Rate[8]		125				V/µs	typ	C
Limited Step Response								
Overshoot	V_{IN} = 0V to ±0.7V Step	250				mV	typ	C
Recovery Time	V_{IN} = ±0.7V to 0V Step	1	1.9	2	2.1	ns	max	B
Linearity Guardband[9]	f = 5MHz, V_O = 2V_{PP}	30				mV	typ	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification, I	–40 to +85				°C	typ	C
Thermal Resistance	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C Test Level A specifications. Junction temperature = ambient temperature +23°C at high temperature limit Test Level A specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +1°C at high temperature limit for over-temperature tested specifications.
(3) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only.
(4) Current is considered positive out-of-node.
(5) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
(6) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3 and Figures 1 and 12.
(7) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
(8) V_H slew rate conditions are: V_{IN} = +0.7V, G = +6, V_L = –2V, V_H = step between 2V and 0V. V_L slew rate conditions are similar.
(9) Linearity Guardband is defined for an output sinusoid (f = 1MHz, V_O = 2V_{PP}) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

G = +6, R_F = 750Ω, R_L = 500Ω tied to V_{CM} = +2.5V, V_L = V_{CM} –1.2V, and V_H = V_{CM} +1.2V, (see Figure 2 for AC performance only), unless otherwise noted.

		OPA699ID						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 2)								
Small Signal Bandwidth (V_O < 0.5V_{PP})	G = +6	234	200	190	180	MHz	min	B
	G = +12	83				MHz	typ	C
	G = –6	242				MHz	typ	C
Gain Bandwidth Product (G ≥ +20)	V_O < 0.5V_{PP}	880	700	650	600	MHz	min	B
Gain Peaking	V_O < 0.5V_{PP}, G = +4	8				dB	typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.5V_{PP}, G = +6	30				MHz	typ	C
Large-Signal Bandwidth	V_O = 2V_{PP}	250	200	190	180	MHz	min	B
Step Response								
Slew Rate	2V Step	1050	850	800	700	V/µs	min	B
Rise-and-Fall Time	0.5V Step	1.75	1.8	1.9	2.1	ns	max	B
Settling Time: 0.05%	2V Step	8				ns	typ	C
Spurious-Free Dynamic Range, Even	f = 5MHz, V_O = 2V_{PP}	64	61	60	58	dB	min	B
Odd	f = 5MHz, V_O = 2V_{PP}	70	69	67	65	dB	min	B
Input Noise								
Voltage Noise Density	f ≥ 1MHz	4.2	4.6	5.2	5.6	nV/√Hz	max	B
Current Noise Density	f ≥ 1MHz	2.1	2.6	2.8	3.0	pA/√Hz	max	B
DC PERFORMANCE								
Open-Loop Voltage Gain (A_{OL})	V_O = V_{CM} ± 0.5V	66	**56**	54	53	dB	min	A
Input Offset Voltage		±2	**±6**	±7	±8	mV	max	A
Average Drift		—		±14	±14	µV/°C	max	B
Input Bias Current(4)		+3	**±10**	±11	±12	µA	max	A
Average Drift		—		±25	±25	nA/°C	max	B
Input Offset Current		±0.4	**±2**	±2.5	±3	µA	max	A
Average Drift		—		±15	±15	nA/°C	max	B
INPUT								
Common-Mode Rejection Ratio	Input Referred, V_{CM} ±0.5V	58	**54**	53	52	dB	min	A
Common-Mode Input Range(5)		V_{CM} ±0.8	**V_{CM} ±0.7**	V_{CM} ±0.7	V_{CM} ±0.6	V	min	A
Input Impedance						MΩ || pF	typ	C
Differential-Mode		0.32 || 1						
Common-Mode		3.5 || 1				MΩ || pF	typ	C
OUTPUT	V_H = V_{CM} + 1.8V, V_L = V_{CM} – 1.8V							
Output Voltage Range	R_L ≥ 500Ω	V_{CM} ±1.6	**V_{CM} ±1.4**	V_{CM} ±1.4	V_{CM} ±1.3	V	min	A
Current Output, Sourcing		+70	**+60**	+55	+50	mA	min	A
Sinking		–70	**–60**	–55	–50	mA	min	A
Closed-Loop Output Impedance	G = +4, f < 100kHz	0.2				Ω	typ	C
POWER SUPPLY								
Operating Voltage, Specified		5				V	typ	C
Maximum		**—**	**+12**	+12	+12	V	max	A
Quiescent Current, Maximum	V_S = +5V	14.3	**14.9**	15.1	15.3	mA	max	A
Minimum	V_S = +5V	14.3	**13.6**	13.4	13.2	mA	min	A
Power-Supply Rejection Ratio	V_S = 4.5V to 5.5V							
+PSRR (Input Referred)		70				dB	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C Test Level A specifications. Junction temperature = ambient temperature +23°C at high temperature limit Test Level A specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +1°C at high temperature limit for over-temperature tested specifications.
(3) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value for information only.
(4) Current is considered positive out of node.
(5) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
(6) I_{VH} (V_H bias current) is negative, and I_{VL} (V_L bias current) is positive, under these conditions. See Note 3 and Figures 2 and 12.
(7) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
(8) V_H slew rate conditions are: V_{IN} = V_{CM} +0.4V, G = +6, V_L = V_{CM} –1.2V, V_H = step between V_{CM} +1.2V and V_{CM}. V_L slew rate conditions are similar.
(9) Linearity Guardband is defined for an output sinusoid (f = 5MHz, V_O = V_{CM} ±1V_{PP}) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

ELECTRICAL CHARACTERISTICS: V_S = +5V (Cont.)

Boldface limits are tested at **+25°C.**

G = +6, R_F = 750Ω, R_L = 500Ω tied to V_{CM} = +2.5V, V_L = V_{CM} –1.2V, and V_H = V_{CM} +1.2V, (see Figure 2 for AC performance only), unless otherwise noted.

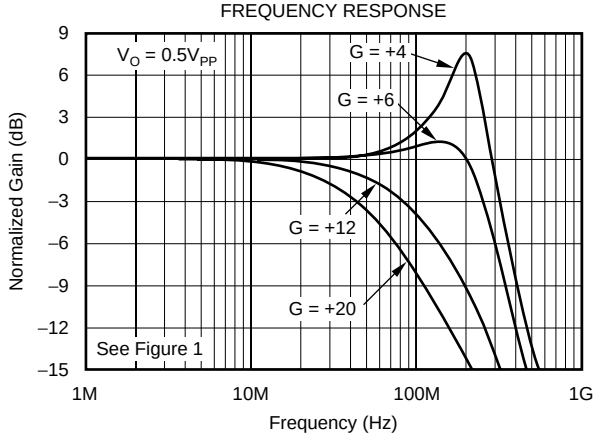
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		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
OUTPUT VOLTAGE LIMITERS								
Maximum Limited Voltage		+3.9				V	typ	C
Minimum Limited Voltage		+1.1				V	typ	C
Default Limiter Voltage	Limiter Pins Open	V_{CM} ±1.1	**V_{CM} ±0.9**	V_{CM} ±0.8	V_{CM} ±0.7	V	min	B
Minimum Limiter Separation (V_H – V_L)		400	400	400	400	mV	min	B
Maximum Limit Voltage		—	V_{CM} ±1.8	V_{CM} ±1.8	V_{CM} ±1.8	V	max	B
Limiter Input Bias Current Magnitude(6)	V_O = 2.5V	–15				µA	typ	C
Limiter Input Impedance		3.4 || 1				MΩ || pF	typ	C
Limiter Isolation(7)	f = 5MHz	–60				dB	typ	C
DC Performance in Limit Mode	V_{IN} = V_{CM} ±0.4V							
Limiter Voltage Accuracy	(V_O – V_H) or (V_O – V_L)	±15	**±30**	±35	±40	mV	max	A
Op Amp Bias Current Shift(4)	Linear ↔ Limited Operation	5				µA	typ	C
AC Performance in Limit Mode								
Limiter Small-Signal Bandwidth	V_{IN} = ±0.4V, V_O < 0.02V_{PP}	450				MHz	typ	C
Limiter Slew Rate(8)		100				V/µs	typ	C
Limited Step Response								
Overshoot	V_{IN} = V_{CM} to V_{CM} ±0.4V Step	55				mV	typ	C
Recovery Time	V_{IN} = V_{CM} ±0.4V to V_{CM} Step	3				ns	typ	C
Linearity Guardband(9)	f = 5MHz, V_O = 2V_{PP}	30				mV	typ	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification, I	–40 to +85				°C	typ	C
Thermal Resistance	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C Test Level A specifications. Junction temperature = ambient temperature +23°C at high temperature limit Test Level A specifications.
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(8) V_H slew rate conditions are: V_{IN} = V_{CM} +0.4V, G = +6, V_L = V_{CM} –1.2V, V_H = step between V_{CM} +1.2V and V_{CM}. V_L slew rate conditions are similar.
(9) Linearity Guardband is defined for an output sinusoid (f = 5MHz, V_O = V_{CM} ±1V_{PP}) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 8).

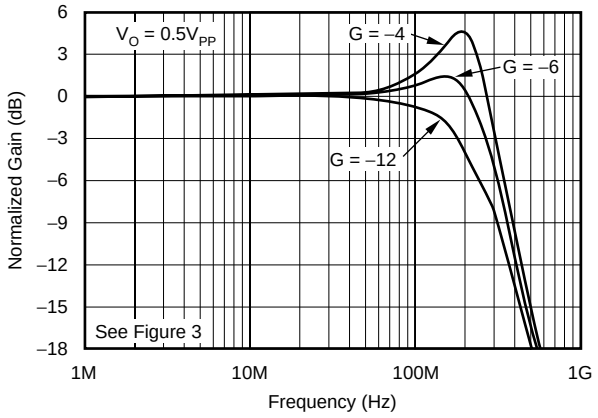
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

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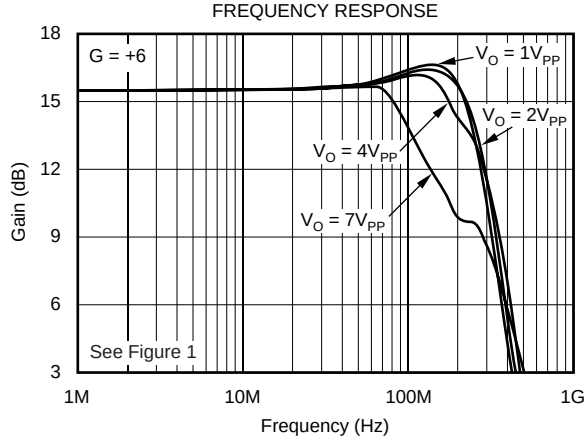
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



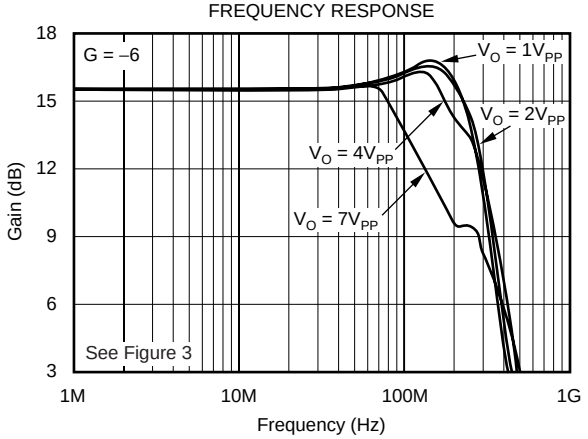
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



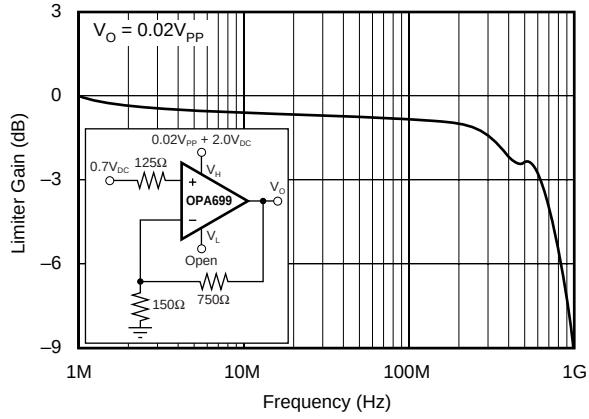
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



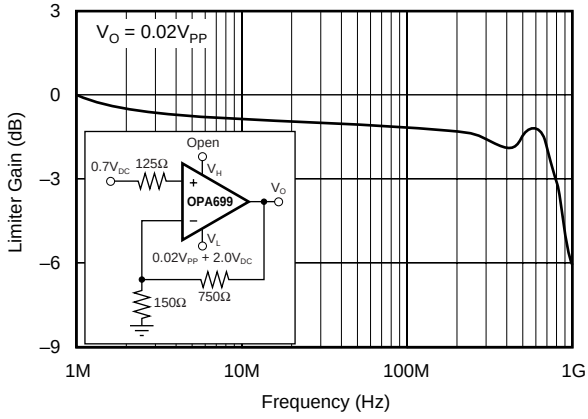
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



V_H—LIMITER SMALL-SIGNAL FREQUENCY RESPONSE



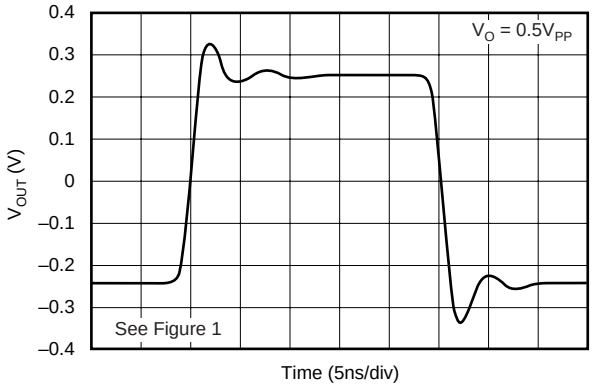
V_L—LIMITER SMALL-SIGNAL FREQUENCY RESPONSE



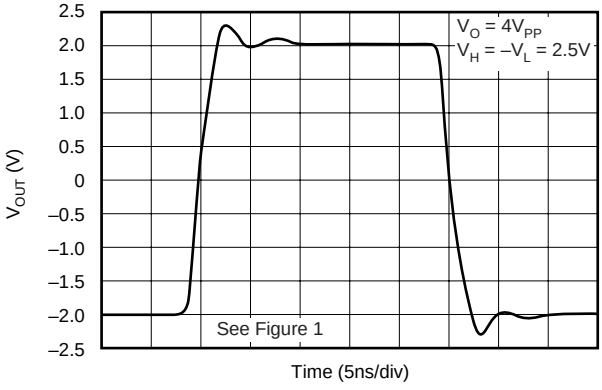
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +6, R_F = 750Ω, and R_L = 500Ω, $V_H = -V_L$ = 2V, unless otherwise noted.

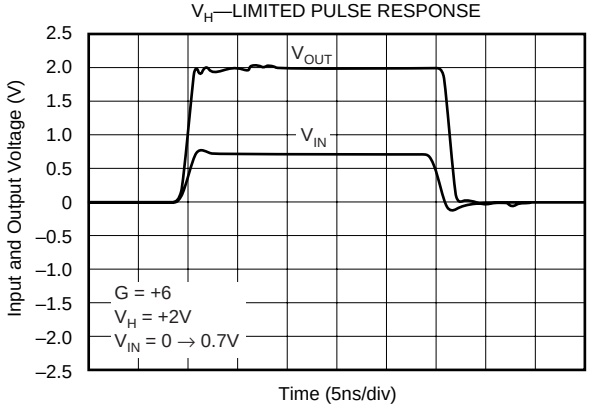
SMALL-SIGNAL PULSE RESPONSE



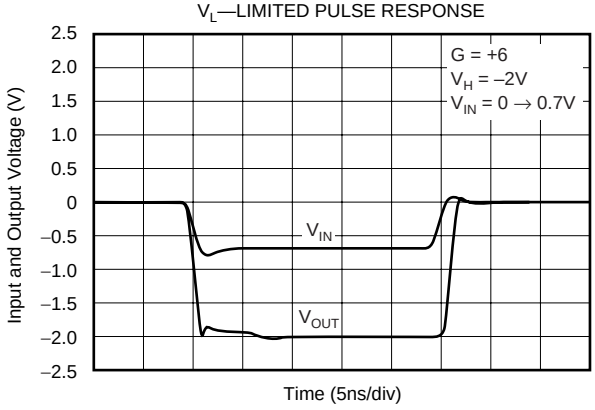
LARGE-SIGNAL PULSE RESPONSE



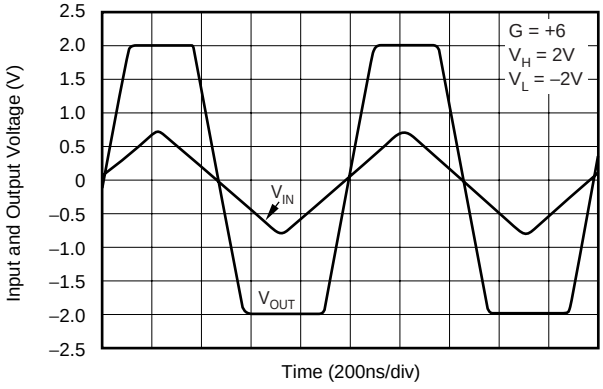
V_H—LIMITED PULSE RESPONSE



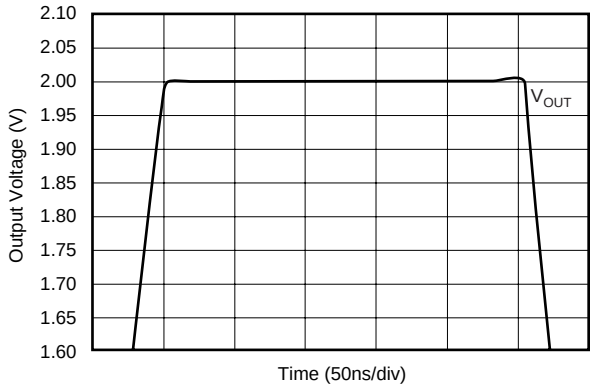
V_L—LIMITED PULSE RESPONSE



LIMITED OUTPUT RESPONSE



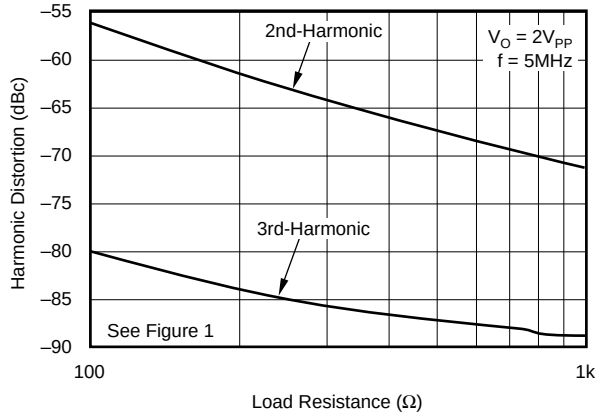
DETAIL OF LIMITED OUTPUT RESPONSE



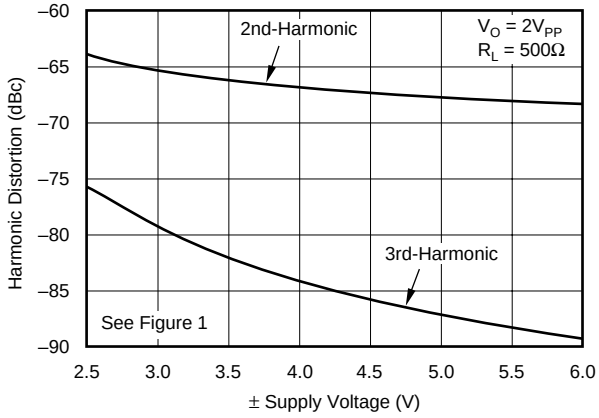
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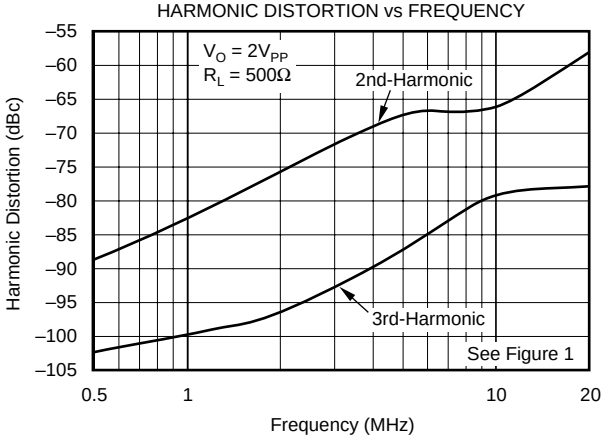
HARMONIC DISTORTION vs LOAD RESISTANCE



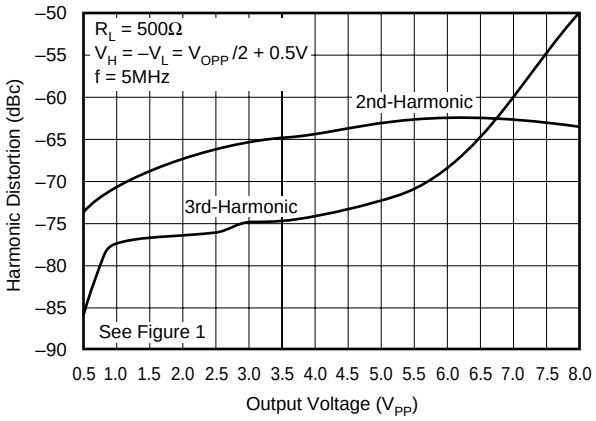
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



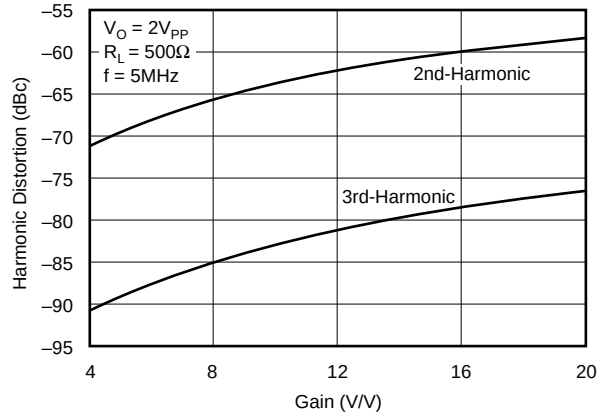
HARMONIC DISTORTION vs FREQUENCY



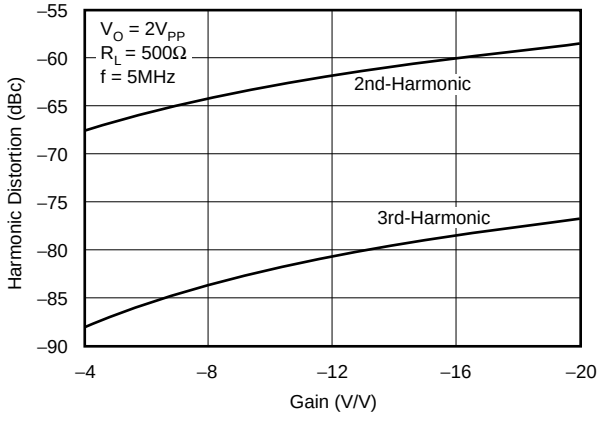
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



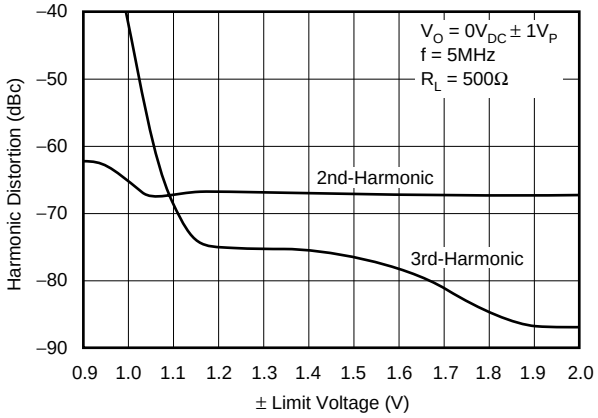
HARMONIC DISTORTION vs INVERTING GAIN



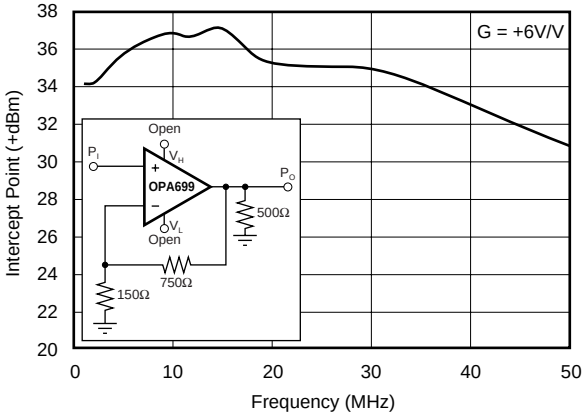
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +6, R_F = 750Ω, and R_L = 500Ω, $V_H = -V_L$ = 2V, unless otherwise noted.

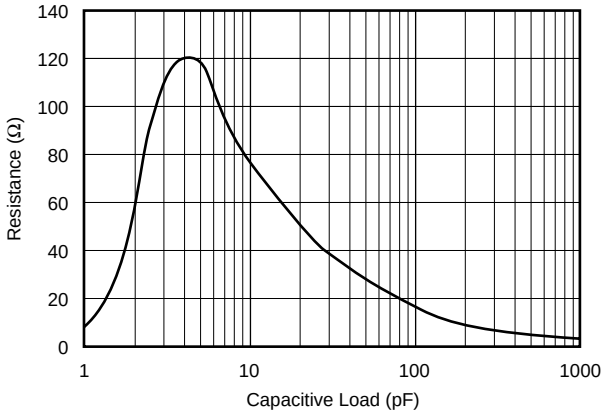
HARMONIC DISTORTION NEAR LIMITING VOLTAGES



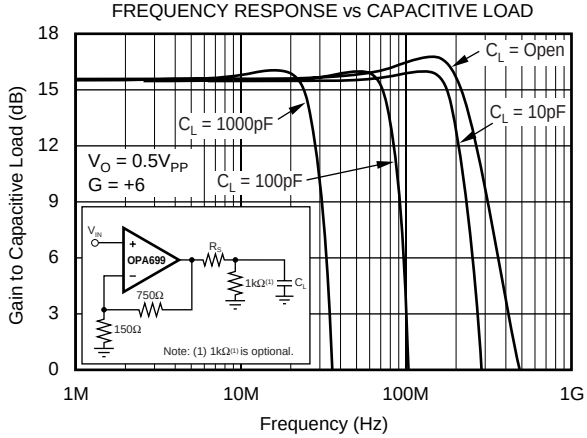
2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT



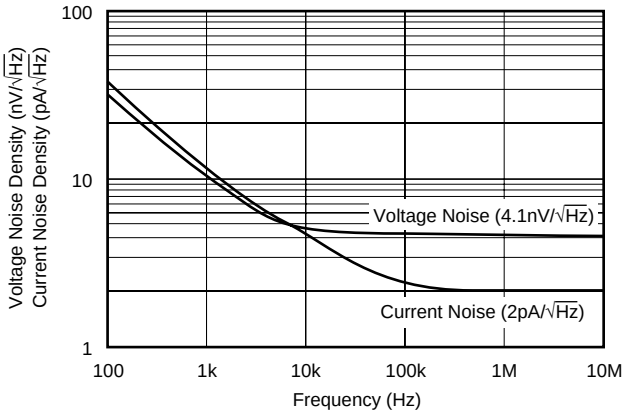
RECOMMENDED R_S vs CAPACITIVE LOAD



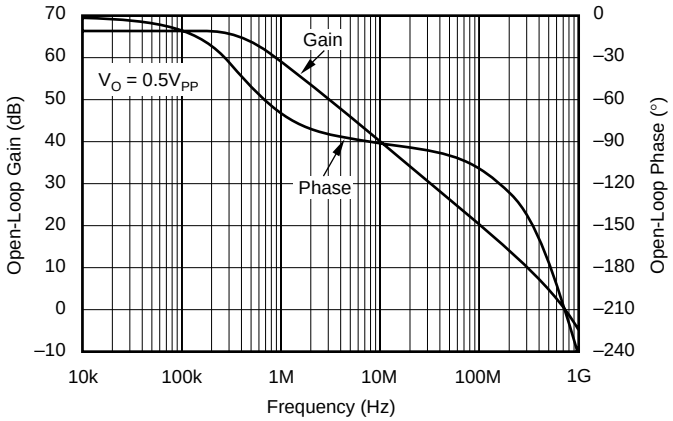
FREQUENCY RESPONSE vs CAPACITIVE LOAD



INPUT VOLTAGE AND CURRENT NOISE DENSITY



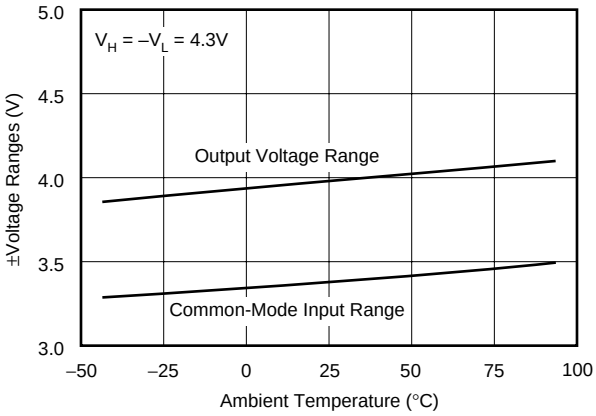
OPEN-LOOP GAIN AND PHASE



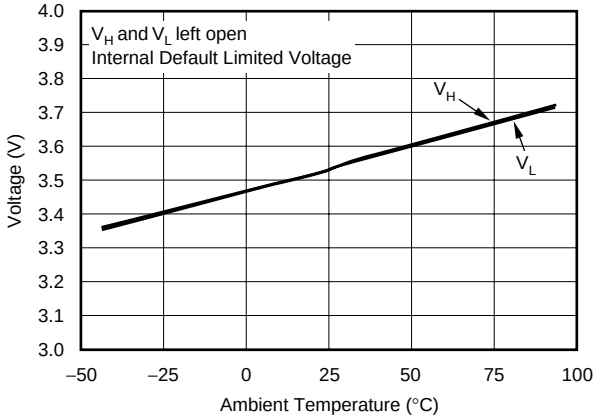
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +6, R_F = 750Ω, and R_L = 500Ω, $V_H = -V_L$ = 2V, unless otherwise noted.

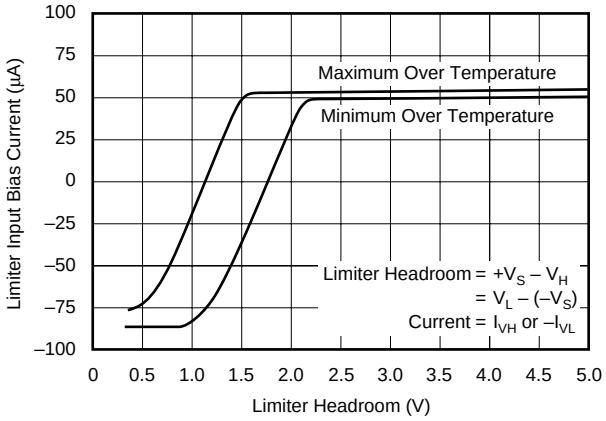
VOLTAGE RANGES vs TEMPERATURE



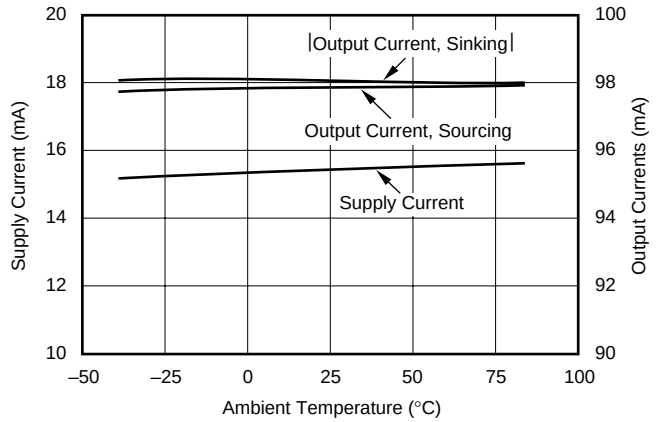
LIMITED VOLTAGE RANGE vs TEMPERATURE



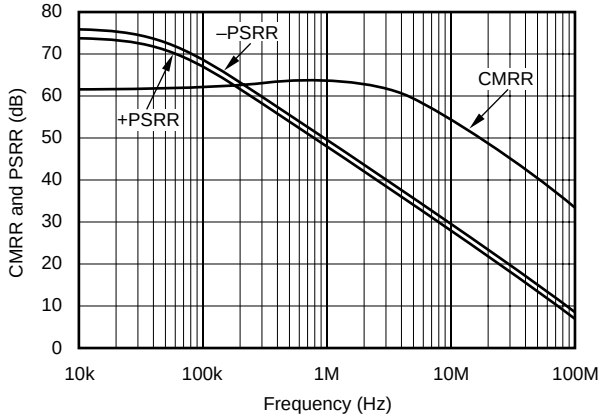
LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE



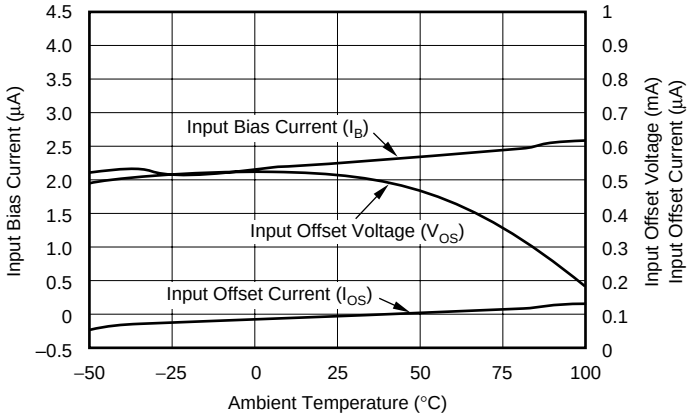
SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE



COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION vs FREQUENCY



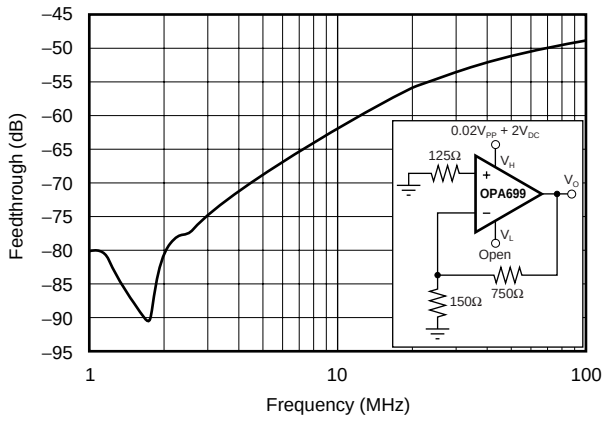
TYPICAL DRIFT OVER TEMPERATURE



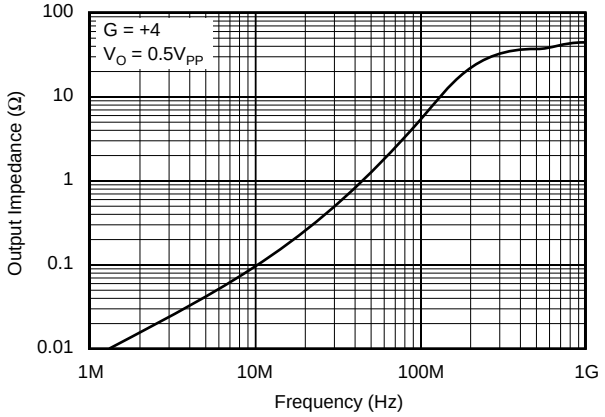
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

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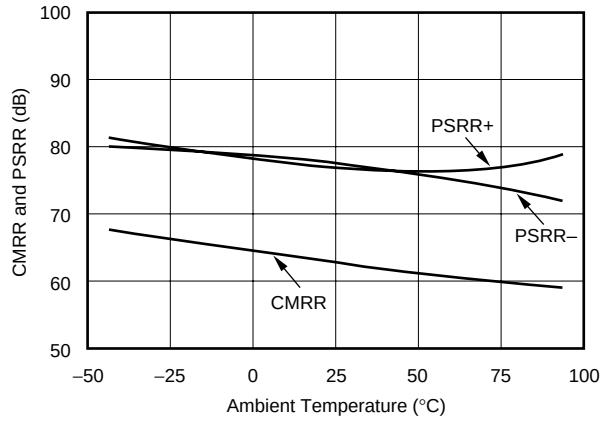
LIMITER FEEDTHROUGH



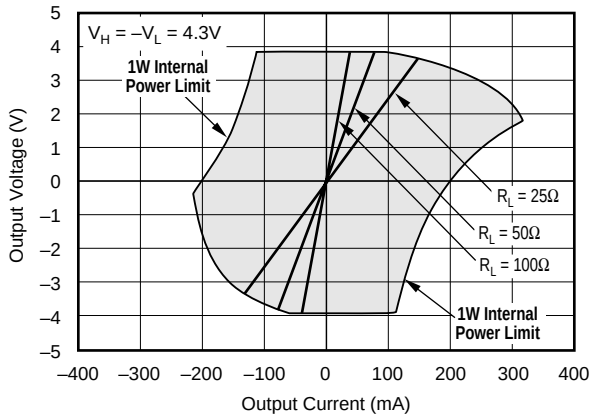
CLOSED-LOOP OUTPUT IMPEDANCE



CMRR and PSRR(±) vs TEMPERATURE



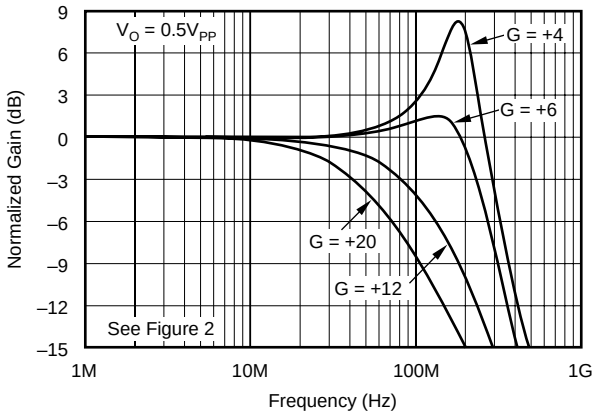
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



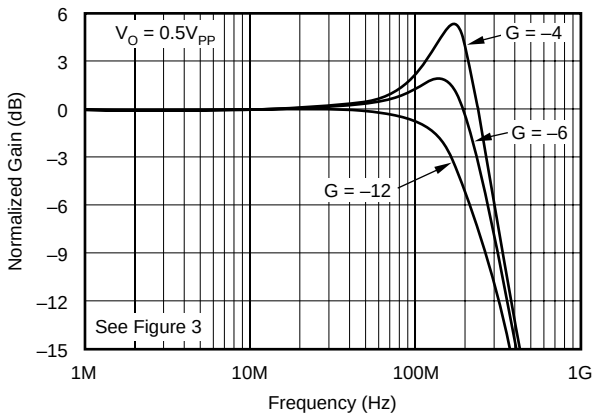
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, G = +6, R_F = 750Ω, and R_L = 500Ω to V_{CM} = +2.5V, V_L = V_{CM} – 1.2V, V_H = V_{CM} + 1.2V, unless otherwise noted.

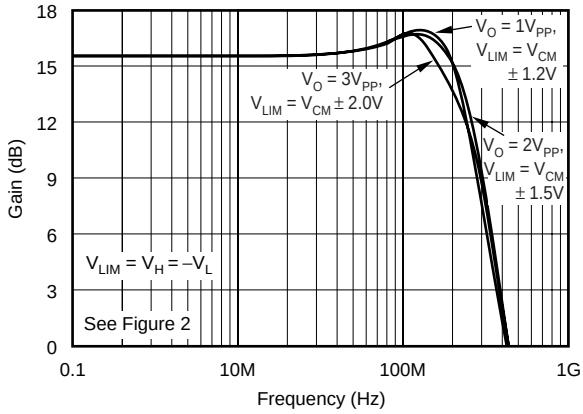
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



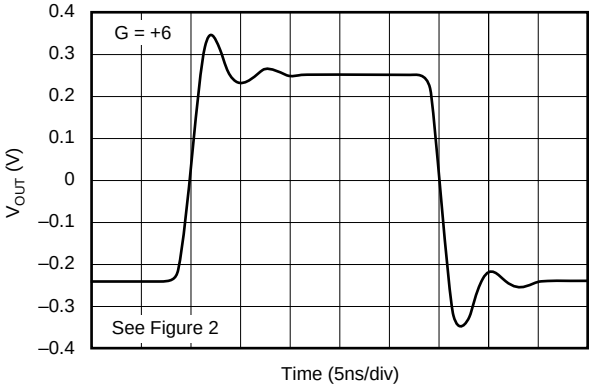
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



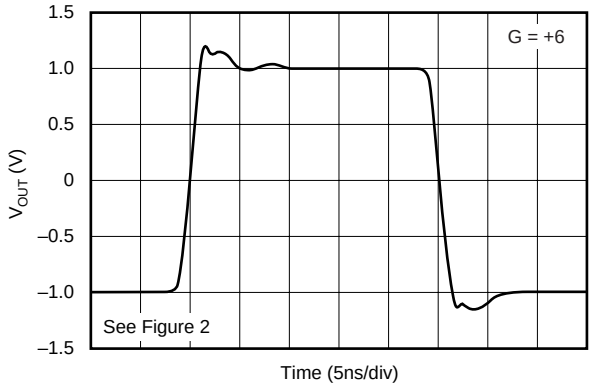
LARGE-SIGNAL FREQUENCY RESPONSE



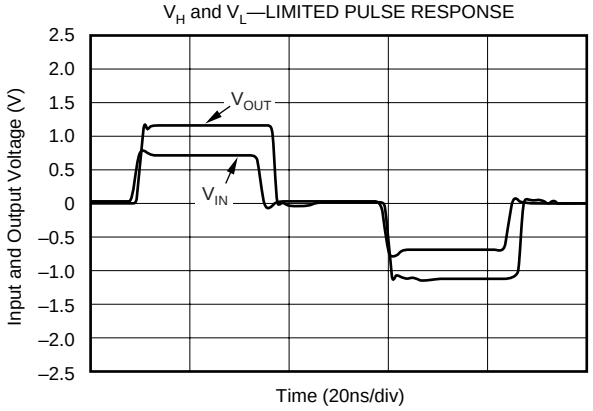
SMALL-SIGNAL PULSE RESPONSE



LARGE-SIGNAL PULSE RESPONSE



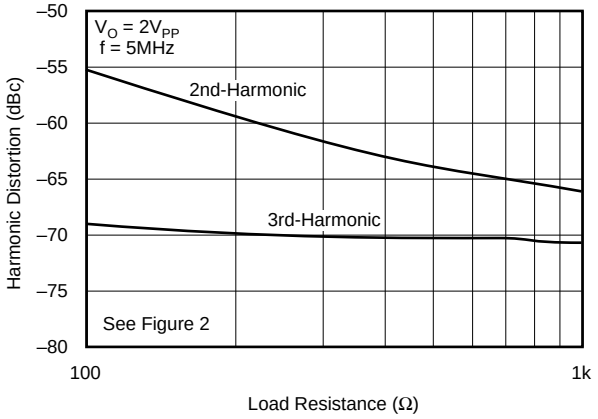
V_H and V_L—LIMITED PULSE RESPONSE



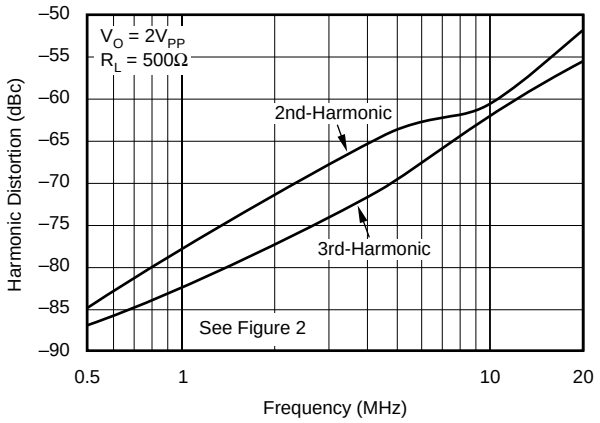
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

T_A = +25°C, G = +6, R_F = 750Ω, and R_L = 500Ω to V_{CM} = +2.5V, V_L = V_{CM} – 1.2V, V_H = V_{CM} + 1.2V, unless otherwise noted.

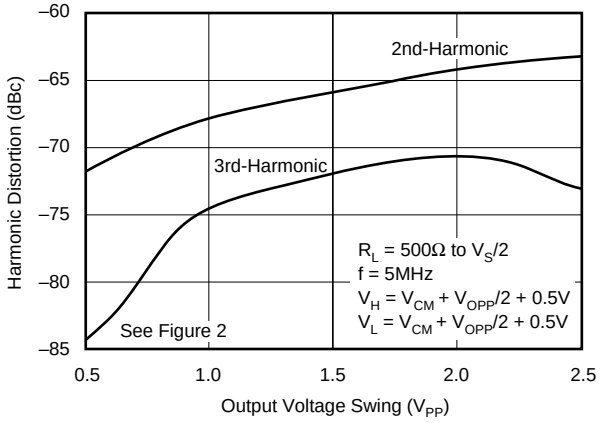
HARMONIC DISTORTION vs LOAD RESISTANCE



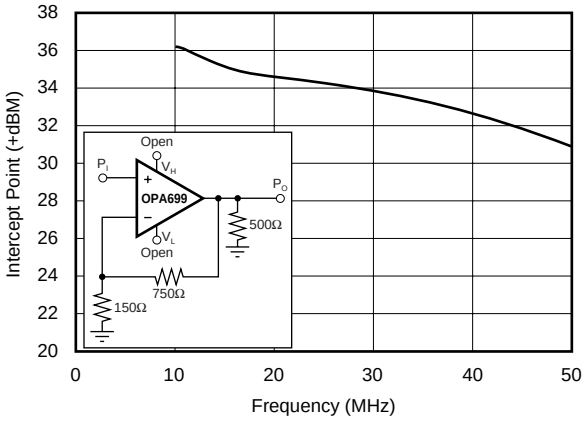
HARMONIC DISTORTION vs FREQUENCY



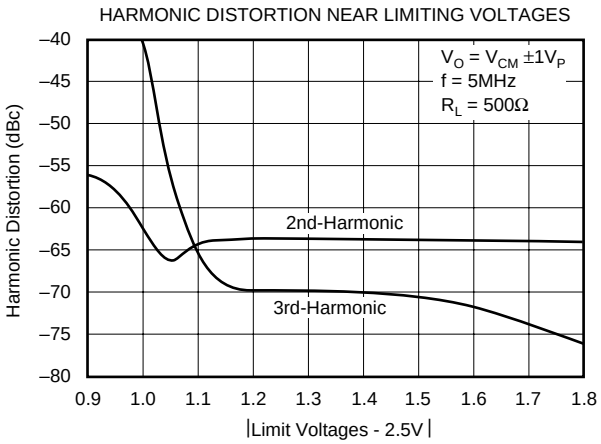
HARMONIC DISTORTION vs OUTPUT VOLTAGE



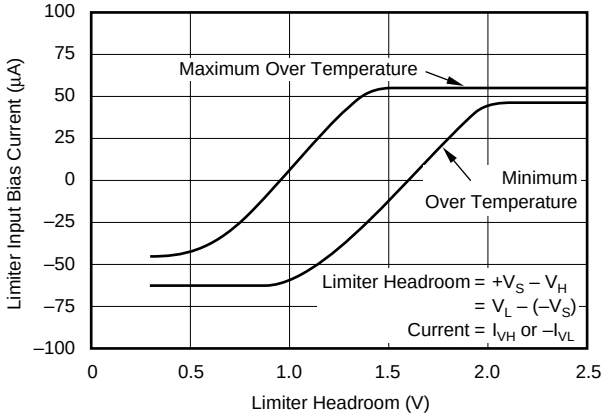
2-TONE, 3RD-ORDER
INTERMODULATION INTERCEPT



HARMONIC DISTORTION NEAR LIMITING VOLTAGES



LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE



TYPICAL APPLICATIONS

WIDEBAND VOLTAGE LIMITING OPERATION

The OPA699 is a gain voltage of +4V/V, voltage-feedback amplifier that combines features of a wideband, high slew rate amplifier with output voltage limiters. Its output can swing up to 1V from each rail and can deliver up to 120mA. These capabilities make it an ideal interface to drive an ADC while adding overdrive protection for the ADC inputs.

Figure 1 shows the DC-coupled, gain of +6V/V, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output is set to 500Ω. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 1, the total output load will be 500Ω || 900Ω = 321Ω. The voltage limiting pins are set to ±2V through a voltage divider network between the $+V_S$ and ground for V_H, and between $-V_S$ and ground for V_L. These limiter voltages are adequately bypassed with a 0.1µF ceramic capacitor to ground. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. One additional component is included in Figure 1. An additional resistor (100Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current-canceling resistance that matches the 125Ω source resistance seen at the inverting input (see the DC accuracy and offset control section). The power-supply bypass for each supply consists of two capacitors: one electrolytic 2.2µF and one ceramic 0.1µF. The power-supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. An additional 0.01µF power-supply decoupling capacitor (not shown here) can be included between the two power-supply pins. In practical PC board layouts, this optional, added capacitor will typically improve the 2nd harmonic distortion performance by 3dB to 6dB.

SINGLE-SUPPLY, NONINVERTING AMPLIFIER

Figure 2 shows an AC-coupled, noninverting gain amplifier for single +5V supply operation. This circuit was used for AC characterization of the OPA699, with a 50Ω source (which it matches) and a 500Ω load. The mid-point reference on the noninverting input is set by two 1.5kΩ resistors. This gives an input bias current-canceling resistance that matches the 750Ω DC source resistance seen at the inverting input (see the DC accuracy and offset control section). The power-supply bypass for the supply consists of two capacitors: one electrolytic 2.2µF and one ceramic 0.1µF. The power-supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. These limiter voltages are adequately bypassed with a 0.1µF ceramic capacitor to ground. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground. While this circuit shows +5V operation, the same circuit may be used for single supplies up to +12V.

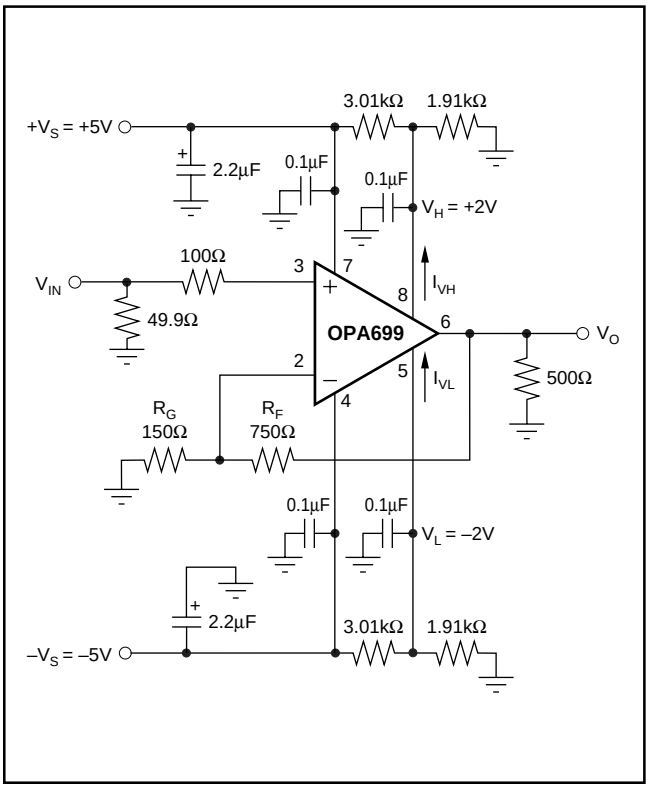


FIGURE 1. DC-Coupled, Dual-Supply Amplifier.

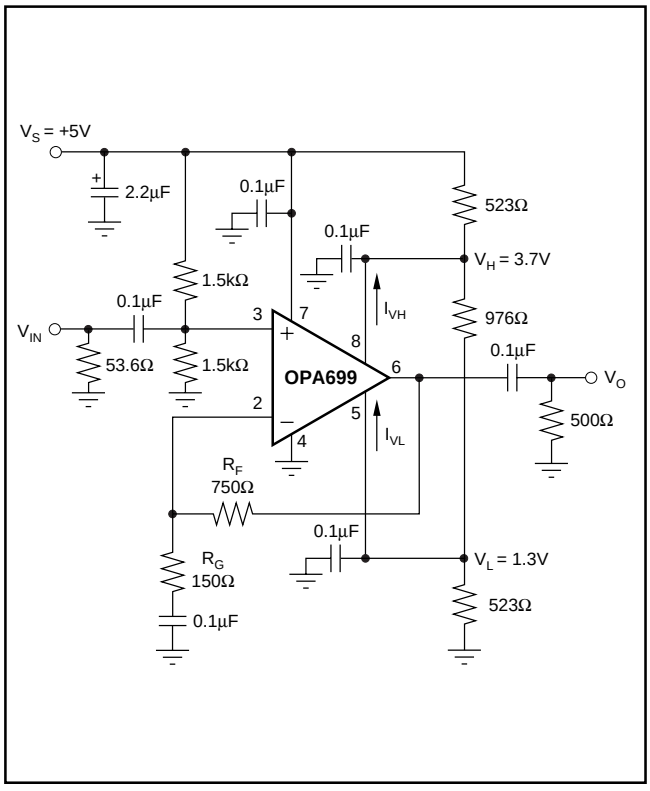


FIGURE 2. AC-Coupled, Single-Supply Amplifier.

WIDEBAND INVERTING OPERATION

Operating the OPA699 as an inverting amplifier has several benefits and is particularly useful when a matched 50Ω source and input impedance are required. Figure 3 shows the inverting gain of –4V/V circuit used as the basis of the inverting mode typical characteristics.

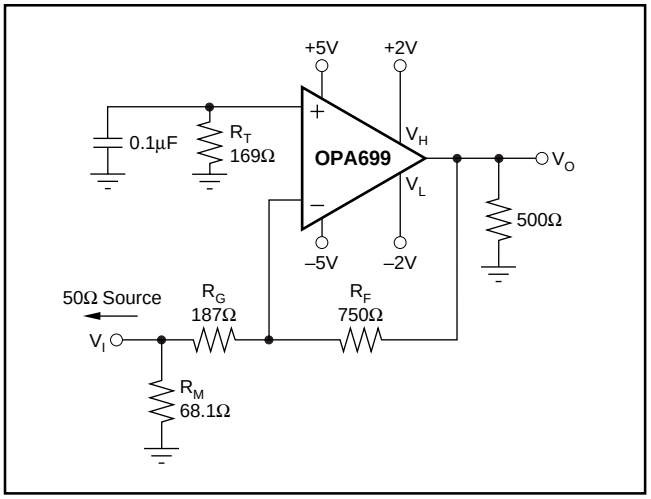


FIGURE 3. Inverting G = –4 Specifications and Test Circuit.

In the inverting case, only the feedback resistor appears as part of the total output load in parallel with the actual load. For a 500Ω load used in the typical characteristics, this gives a total load of 329Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case, 187Ω for a gain of –4) while an additional input resistor (R_M) can be used to set the total input impedance equal to the source, if desired. In this case, R_M = 68.1Ω in parallel with the 187Ω gain setting resistor gives a matched input impedance of 50Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 3.

For bias current-cancellation matching, the noninverting input requires a 169Ω resistor to ground. The calculation for this resistor includes a DC-coupled 50Ω source impedance along with R_G and R_M. Although this resistor will provide cancellation for the bias current, it must be well-decoupled (0.1µF in Figure 3) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 3 will far exceed the bandwidth at that same gain magnitude for the noninverting circuit of Figure 1. This occurs due to the lower noise gain for the circuit of Figure 3 when the 50Ω source impedance is included in the analysis. For instance, at a signal gain of –15 (R_G = 50Ω, R_M = open, R_F = 750Ω) the noise gain for the circuit of Figure 3 will be 1 + 750Ω/(50Ω + 50Ω) = 8.5 due to the addition of the 50Ω source in the noise gain equation. This approach gives considerably higher bandwidth than the noninverting gain of +15. Using the 1GHz gain bandwidth product for the OPA699, an inverting gain of –15 from a 50Ω source to a 50Ω R_G will give 140MHz bandwidth, whereas the noninverting gain of +8 will give 55MHz, as shown in the measured results of Figure 4.

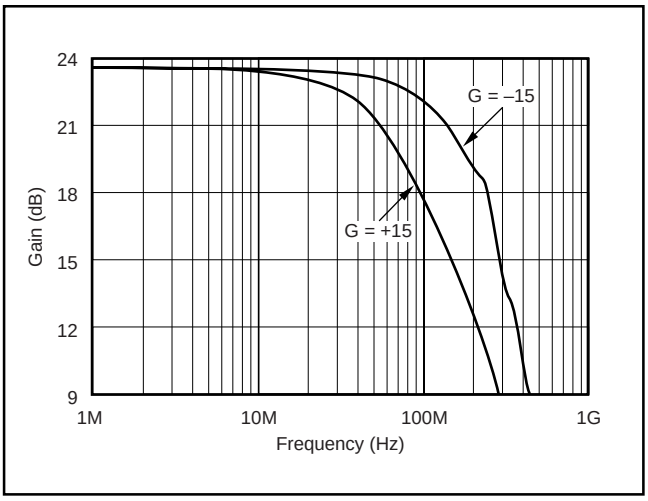


FIGURE 4. G = +15 and –15 Frequency Response.

LOW-GAIN COMPENSATION FOR IMPROVED SFDR

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique can be used to retain the full slew rate and noise benefits of the OPA699, while giving increased loop gain and the associated distortion improvements offered by a non-unity-gain stable op amp. This technique shapes the loop gain for good stability, while giving an easily controlled 2nd-order low-pass frequency response. To set the compensation capacitors (C_S and C_F), consider the half-circuit of Figure 5, where the 50Ω source is used.

Considering only the noise gain for the circuit of Figure 5, the low-frequency noise gain (N_{G1}) is set by the resistor ratio, while the high-frequency noise gain (N_{G2}) is set by the capacitor ratio. The capacitor values set both the transition frequencies and the high-frequency noise gain. If the high-frequency noise gain, determined by $N_{G2} = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp, and the noise gain pole (set by $1/R_FC_F$) is placed correctly, a very well controlled 2nd-order low-pass frequency response results.

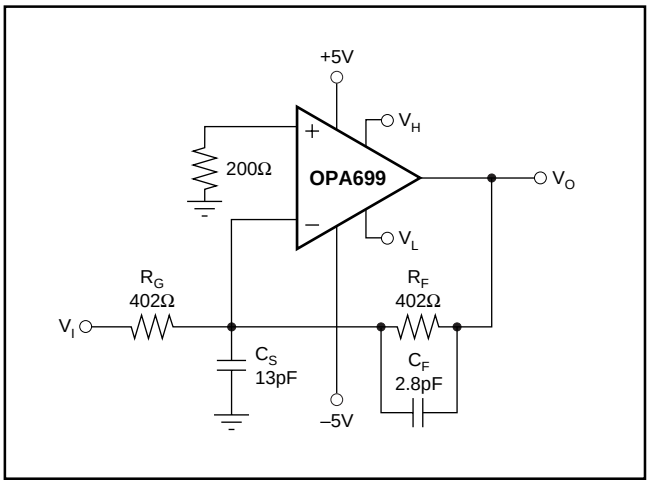


FIGURE 5. Broadband, Low-Inverting Gain External Compensation.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain (NG_2), which should be greater than the minimum stable gain for the OPA699. Here, a target of NG_2 = 26 is used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain (NG_1). To simplify this discussion, we will target a maximally flat 2nd-order low-pass Butterworth frequency response (Q = 0.707). The signal gain shown in Figure 5 sets the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 2 in this example). Then, using only these two gains and the gain bandwidth product for the OPA699 (1000MHz), the key frequency in the compensation is set by Equation1.

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right] \quad (1)$$

Physically, this Z_O (22.3MHz for the values shown above) is set by $1/(2\pi R_F(C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect the unity gain if projected back to a 0dB gain. The actual zero in the noise gain occurs at $NG_1 \bullet Z_O$ and the pole in the noise gain occurs at $NG_2 \bullet Z_O$. That pole is physically set by $1/(R_F C_F)$. Since GBP is expressed in Hz, multiply Z_O by 2π and use to get C_F by solving Equation 2.

$$C_F = \frac{1}{2\pi R_F Z_O NG_2} (= 3pF) \quad (2)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S using Equation 3 (solving for C_S by using NG_2 = 6):

$$C_S = (NG_2 - 1)C_F \quad (3)$$

which gives C_S = 15pF.

Both of these calculated values have been reduced slightly in Figure 5 to account for parasitics. The resulting closed-loop bandwidth is approximately equal to Equation 4.

$$f_{-3dB} \cong \sqrt{Z_O \bullet GBP} \quad (4)$$

For the values shown in Figure 5, f_{-3dB} is approximately 149MHz. This is less than that predicted by simply dividing the Gain Bandwidth Product (GBP) product by NG_1. The compensation network controls the bandwidth to a lower value, while providing the full slew rate at the output and an improved distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_O$.

LOW DISTORTION, LIMITED OUTPUT, ADC INPUT DRIVER

Figure 6 shows a simple ADC driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive. Note that the limiting voltages have been set 100mV above/below the corresponding reference voltage from the converter. This circuit also implements an improved distortion for an inverting gain of –2 using external compensation.

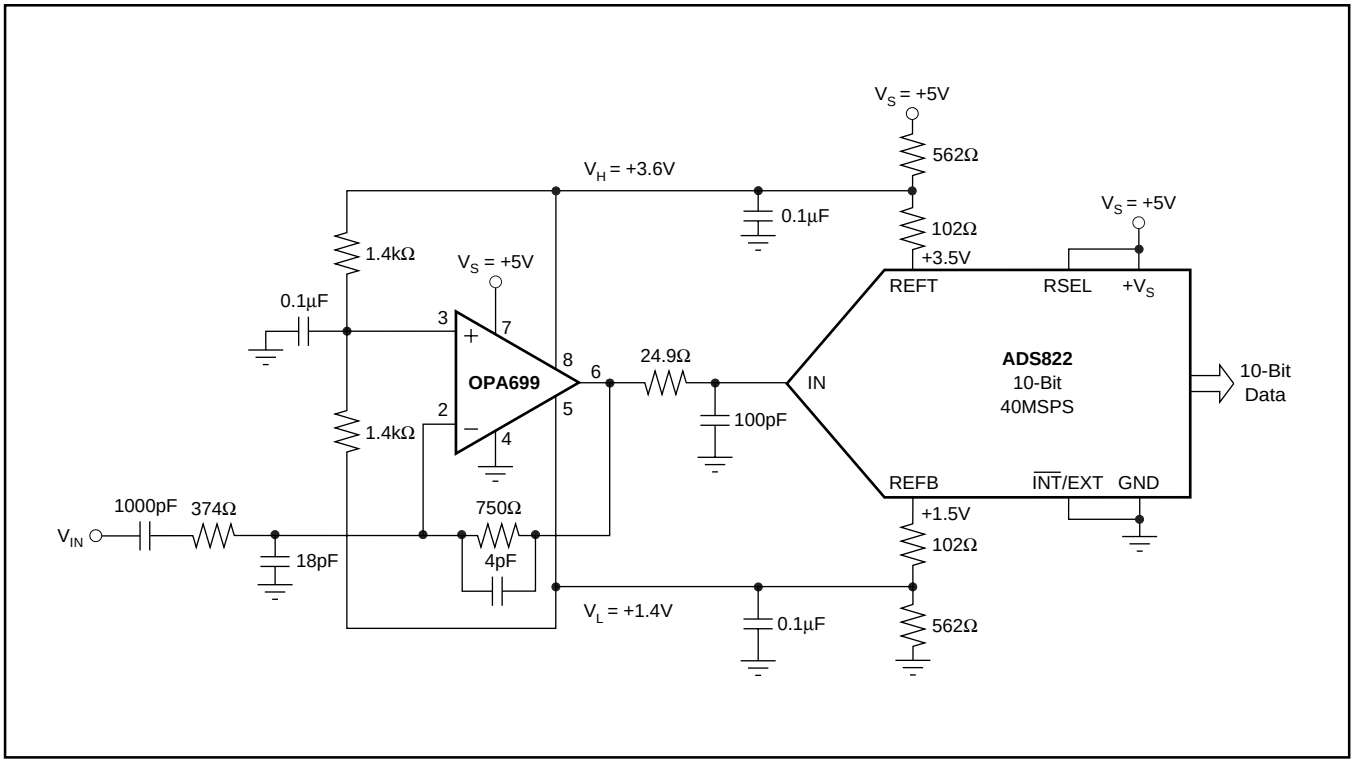


FIGURE 6. Single Supply, Limiting ADC Input Driver.

LIMITED OUTPUT, DIFFERENTIAL ADC INPUT DRIVER

Figure 7 shows a differential ADC driver that takes advantage of the OPA699 limiters to protect the input of the ADC. Two OPA699s are used. The first one is an inverting configuration at a gain of –2. The second one is in a noninverting configuration at a gain of +2. Refer to the section, *Low Gain Compensation for Improved SFDR*, for a discussion of stability issues of the OPA699 operating at a gain less than 4. Each amplifier is swinging $2V_{PP}$ providing a $4V_{PP}$ differential signal to drive the input of the ADC. Limiters have been set 100mV away from the magnitude of each amplifier maximum signal to provide input protection for the ADC while maintaining an acceptable distortion level.

PRECISION HALF WAVE RECTIFIER

Figure 8 shows a half wave rectifier with outstanding precision and speed. V_H (pin 8) will default to a 3.5 typically if left open, while the negative limit is set to ground.

The gain for the circuit in Figure 8 is set at +6. Figure 9 shows input and output for ±0.5V 100MHz input.

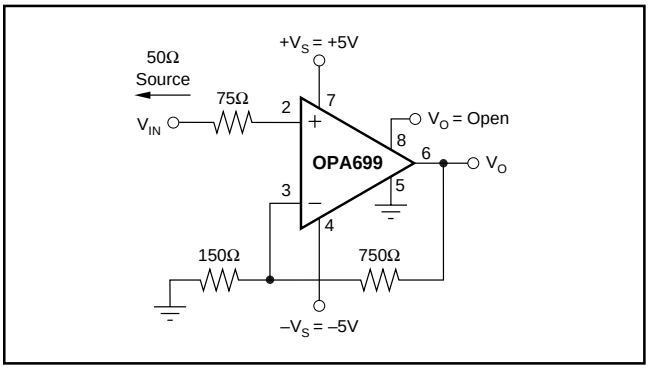


FIGURE 8. Precision Half-Wave Rectifier.

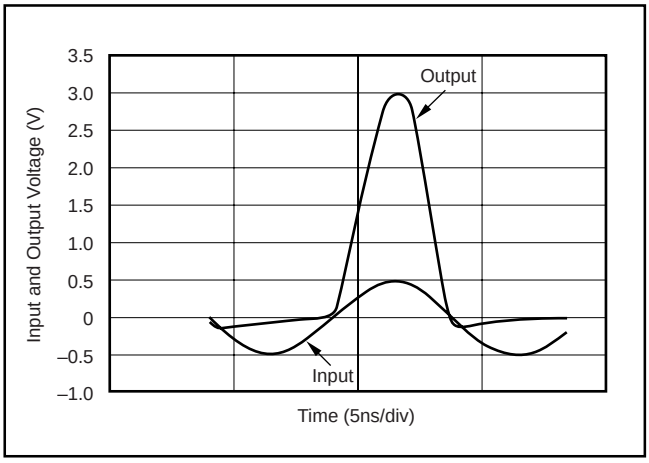


FIGURE 9. 100MHz Sinewave Rectified.

VERY HIGH-SPEED SCHMITT TRIGGER

Figure 10 shows a very high-speed Schmitt Trigger. The output levels are precisely defined, and the switching time is exceptional. The output voltage swings between V_H and V_L.

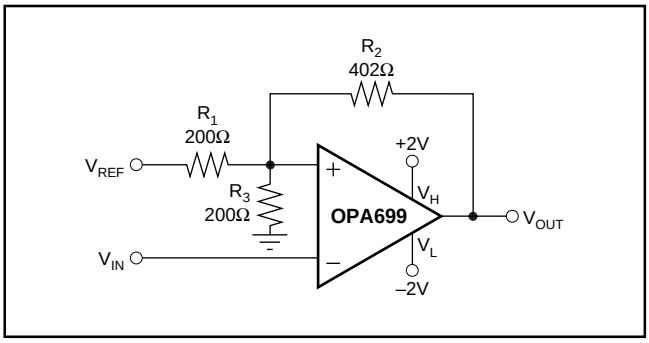


FIGURE 10. Very High-Speed Schmitt Trigger.

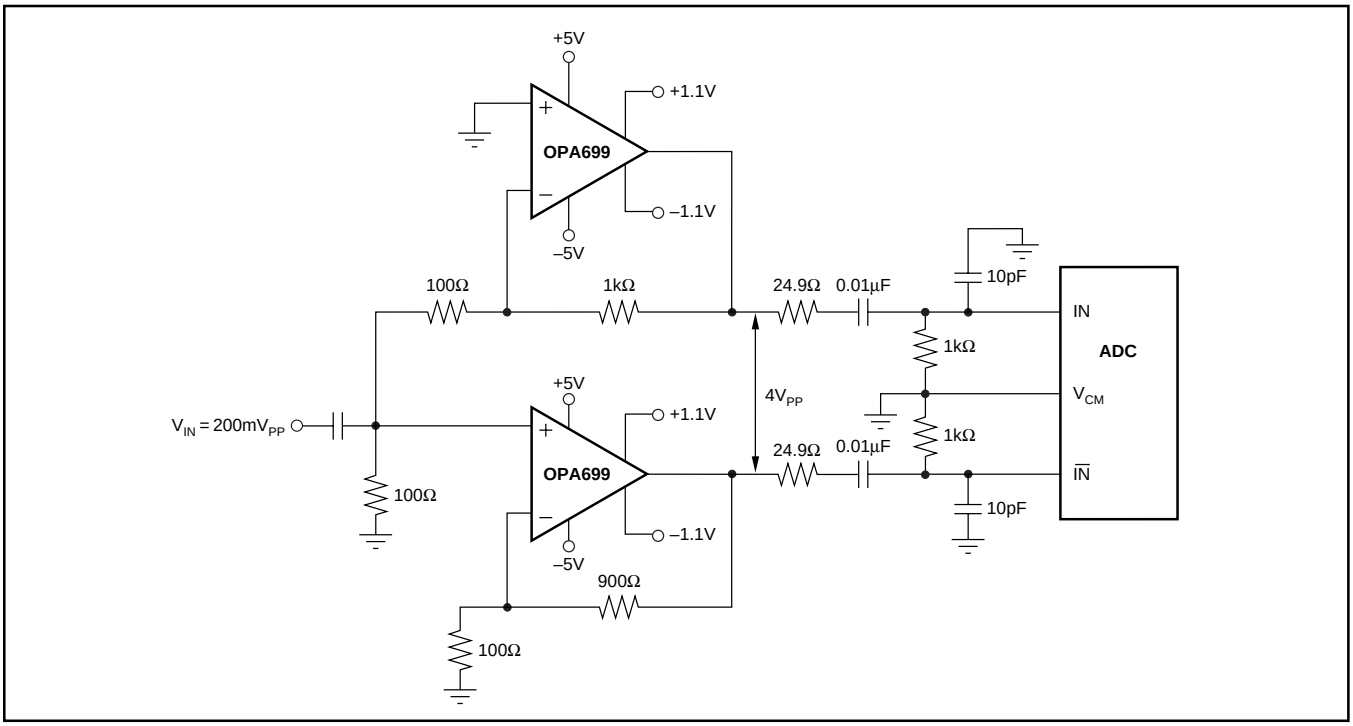


FIGURE 7. Single to Differential AC-Coupled, High Gain Output Limited ADC Driver.

The circuit operates as follows. When the input voltage is less than V_{HL} then the output is limiting at V_H. When the input is greater than V_{HH}, then the output is limiting at V_L, with V_{HL} and V_{HH} defined as the following:

$$V_{HL,\,HH} = \left(\frac{R_1 \,||\, R_2 \,||\, R_3}{R_1} \times V_{REF}\right) + \left(\frac{R_1 \,||\, R_2 \,||\, R_3}{R_2} \times V_{OUT}\right)$$

Due to the inverting function realized by the Schmitt Trigger, V_{HL} corresponds to $V_{OUT} = V_H$, and V_{HH} corresponds to $V_{OUT} = V_L$.

Figure 11 shows the Schmitt Trigger operating with V_{REF} = +5V. This gives us V_{HH} = 2.4V and V_{HL} = 1.6V. The propagation delay for the OPA699 in a Schmitt Trigger configuration is 4ns from high-to-low, and 4ns from low-to-high.

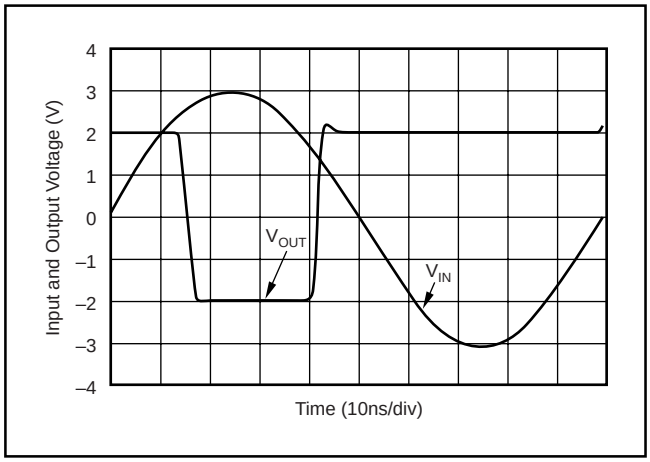


FIGURE 11. Schmitt Trigger Time Domain Response for a 10MHz Sinewave.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURE

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA699. The fixture is offered free of charge as an unpopulated PCB, delivered with user's guide. The summary information for this fixture is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA699ID	SO-8	DEM-OPA-SO-1A	SBOU009

TABLE I. Demonstration Fixture.

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA699 product folder.

OPERATING SUGGESTIONS

THEORY OF OPERATION

The OPA699 is a voltage-feedback, gain of +4V/V stable op amp. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This action from the limiters avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain. The limiters have a very sharp transition from the linear region of operation to output limiting. This transition allows the limiter voltages to be set very near (< 100mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

OUTPUT LIMITERS

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L. Because the limiters act on the output, their accuracy does not change with the gain. The transition from the linear region of operation to output limiting is very sharp—the desired output signal can safely come to within 30mV of V_H or V_L with no onset of non-linearity. The limiter voltages can be set to within 0.7V of the supplies ($V_L \geq -V_S$ + 0.7V, $V_H \leq +V_S - 0.7V$). They must also be at least 400mV apart ($V_H - V_L \geq 0.4V$). When pins 5 and 8 are left open, V_H and V_L go to the default voltage limit; the minimum values are given in the electrical specifications. Looking at Figure 12 for the zero bias current case shows the expected range of (V_S – default limit voltages) = headroom.

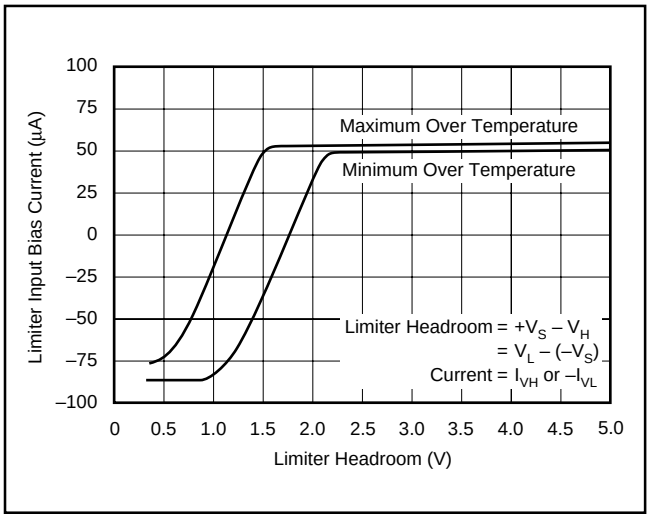


FIGURE 12. Limiter Bias Current vs Bias Voltage.

When the limiter voltages are more than 2.1V from the supplies ($V_L \geq -V_S + 2.1V$ or $V_H \leq +V_S - 2.1V$), you can use simple resistor dividers to set V_H and V_L (see Figure 1). Make sure to include the limiter input bias currents (Figure 8) in the calculations (that is, I_{VL} = 50µA into pin 5, and I_{VH} = +50µA out of pin 8). For good limiter voltage accuracy, run a minimum 1mA quiescent bias current through these resistors. When the limiter voltages need to be within 2.1V of the supplies ($V_L \leq -V_S + 2.1V$ or $V_H \geq +V_S - 2.1V$), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This condition will typically be the case for single-supply operation (V_S = +5V). Figure 2 runs 2.5mA through the resistive divider that sets V_H and V_L. This limits errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages. The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (for example, ±5%). Using a more accurate source, and bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

  Other error sources also contribute, but should have little impact on the limiters' DC accuracy:

- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to uncertainty in the useable output swing.
- The limiter offset voltage only slightly degrades limiter accuracy. Figure 13 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages. In this plot a fixed ±1V output swing is driven while the limiter voltages are reduced symmetrically. Until the limiters are reduced to ±1.1V, little distortion degradation is observed.

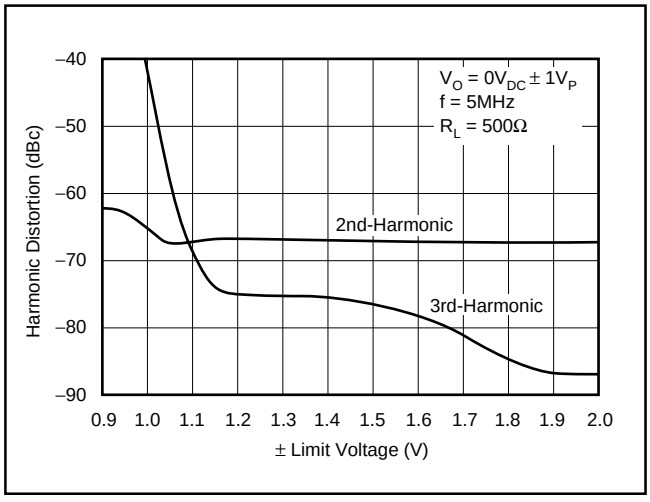


FIGURE 13. Harmonic Distortion Near Limit Voltages.

OUTPUT DRIVE

The OPA699 has been optimized to drive 500Ω loads, such as ADCs. It still performs very well driving 100Ω loads; the specifications are shown for the 500Ω load. This makes the OPA699 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve *Output Impedance vs Frequency*, the OPA699 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

THERMAL CONSIDERATIONS

The OPA699 will not require heat sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \times \theta_{JA}$, where T_A is the ambient temperature. For example, the maximum T_J for a OPA699ID with G = +6, R_F = 750Ω, R_L = 500Ω, and $\pm V_S$ = ±5V at the maximum T_A = +85°C is calculated as:

$$P_{DQ} = (10V \times 15.5mA) = 155mW$$

$$P_{DL} = \frac{(5V)^2}{4 \times (500\Omega \parallel 900\Omega)} = 19.4mW$$

$$P_D = 155mW + 19.4mW = 174.4mW$$

$$T_J = 85°C + 174.4mW \times 125°C/W = 107°C$$

This would be the maximum T_J from $V_O = \pm 2.5V_{DC}$. Most applications will be at a lower output stage power and have a lower T_J.

CAPACITIVE LOADS

Capacitive loads, such as the input to ADCs, will decrease the amplifier phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads ≥ 2pF should be isolated by connecting a small resistor in series with the output, as shown in Figure 14. Increasing the gain from +2 will improve the capacitive drive capabilities due to increased phase margin.

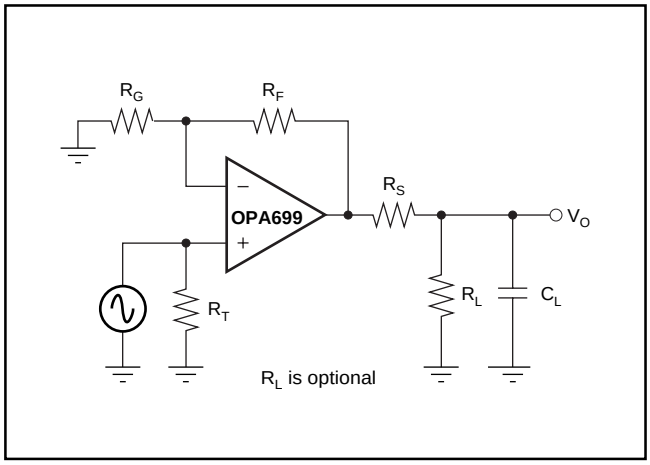


FIGURE 14. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

FREQUENCY RESPONSE COMPENSATION

The OPA699 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of +6. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –5 is equivalent to a gain of +6 for bandwidth purposes (that is, noise gain = 6). Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

If a unity-gain stable amplifier is needed, the OPA698 is recommended.

In applications where a large feedback resistor is required, such as a photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high-gain applications, use a three-resistor *Tee* network to reduce the RC time constants set by the parasitic capacitances.

PULSE SETTLING TIME

The OPA699 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve *Recommended R_S vs Capacitive Load*. Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics, when recovering from overdrive, are extremely good as shown in the typical characteristics.

DISTORTION

The OPA699 distortion performance is specified for a 500Ω load, such as an ADC. Driving loads with smaller resistance will increase the distortion, as illustrated in Figure 15. Remember to include the feedback network in the load resistance calculations.

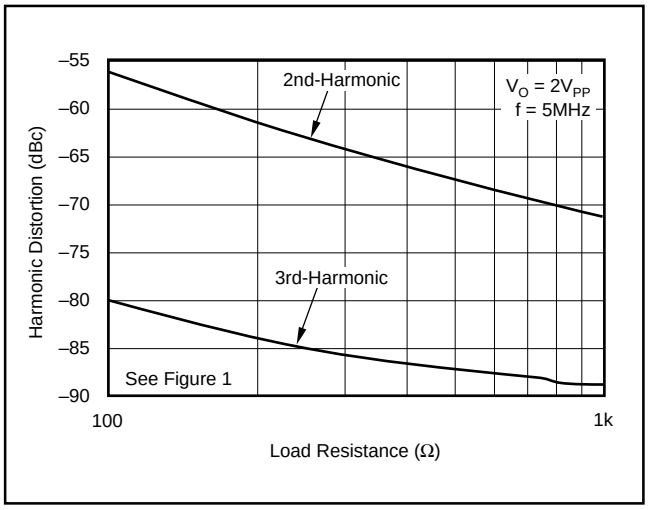


FIGURE 15. 5MHz Harmonic Distortion vs Load Resistance.

NOISE PERFORMANCE

High slew rate, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 4.1nV/$\sqrt{Hz}$ input voltage noise for the OPA699, however, is much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 16 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

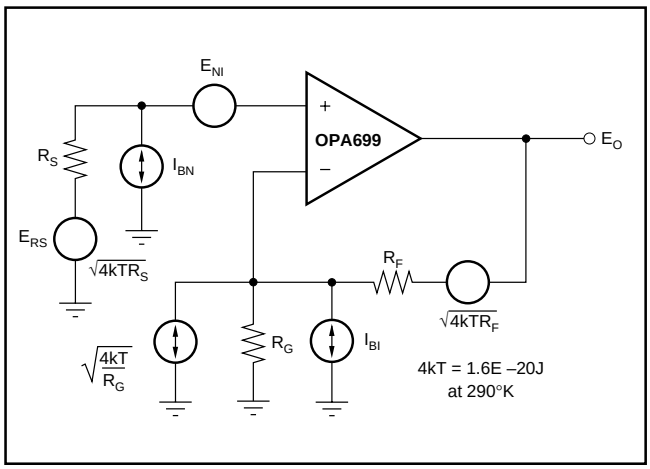


FIGURE 16. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 5 shows the general form for the output noise voltage using the terms shown in Figure 16.

(5)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 6.

(6)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA699 circuit and component values (see Figure 1) will give a total output spot noise voltage of 27.4nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 4.6nV/$\sqrt{Hz}$. This total input-referred spot noise voltage is only slightly higher than the 4.1nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to a maximum value of 300Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300Ω will satisfy both noise and frequency response flatness considerations. Since the resistor-induced noise is negligible, additional capacitive decoupling across the bias current cancellation resistor (R_T) for the inverting op amp configuration of Figure 3 is not required, but is still desirable.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage feedback op amp allows good output DC accuracy in a large variety of applications. The power-supply current trim for the OPA699 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 3μA at each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. The total output offset voltage may be considerably reduced by matching the DC source resistances appearing at the two inputs. This reduces the output DC error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage, with NG = noninverting signal gain, equal to:

$\pm(NG \bullet V_{OS(MAX)}) \pm (R_F \bullet I_{OS(MAX)})$

$= \pm(2 \bullet 5mV) \pm (750\Omega \bullet 2.0\mu A)$

$= \pm 11.5mV$

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques eventually reduce to adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the DC offset voltage on the summing junction will set up a DC current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 17 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the DC offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain as well as the frequency response.

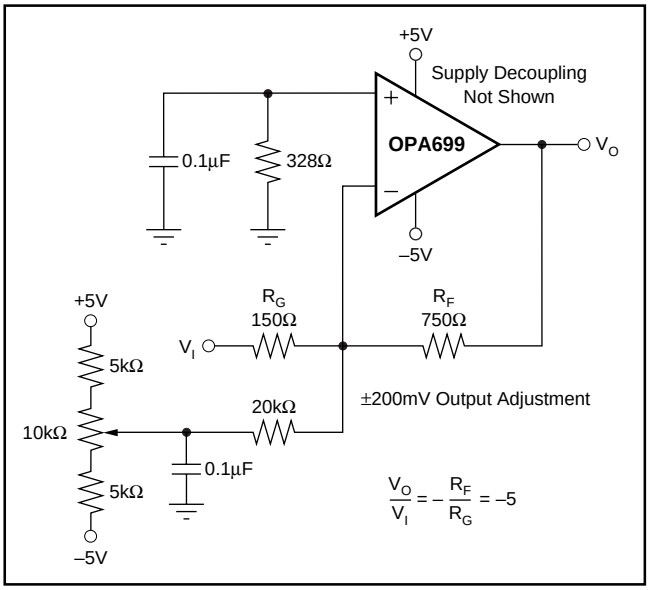


FIGURE 17. DC-Coupled, Inverting Gain of –5, with Offset Adjustment.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with the high-frequency OPA699 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

a) **Minimize parasitic capacitance to any AC ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.

b) **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high frequency 0.1μF decoupling capacitors < 0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2μF to 6.8μF) high-frequency decoupling

capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.

c) **Place external components close** to the OPA699. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.

d) **Use high-frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances. Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use R_F type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2µF to 6.8µF) should be tantalum for better high frequency and pulse performance.

e) **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2pF parasitic parallel capacitance. For resistors > 1.5kΩ, this adds a pole and/or zero below 500MHz. Make sure that the output loading is not too heavy. The recommended 750Ω feedback resistor is a good starting point in most designs.

f) **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve, *Recommended R_S vs Capacitive Load*. Parasitic loads < 2pF may not need the isolation resistor.

g) **When long traces are necessary,** use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the source from the reactive load presented by the line, but the frequency response will be degraded. Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.

h) **Do not use sockets** for high-speed parts like the OPA699. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

POWER SUPPLIES

The OPA699 is nominally specified for operation using either ±5V supplies or a single +5V supply. The maximum specified total supply voltage of 13V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common-mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single-supply operation circuits. Figure 2 shows one approach to single-supply operation.

INPUT AND ESD PROTECTION

The OPA699 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 18.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA699), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

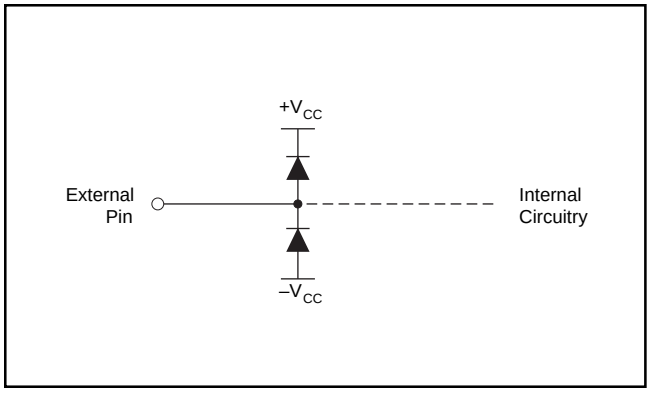


FIGURE 18. I/O Pin ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	D	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
3/06	C	19	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA699ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 699	Samples
OPA699IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 699	Samples
OPA699IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 699	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA699 :

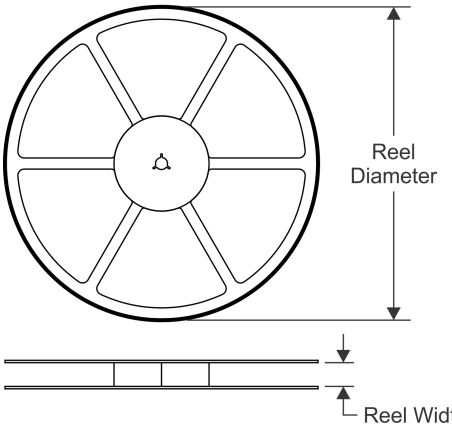
- Military: OPA699M

NOTE: Qualified Version Definitions:

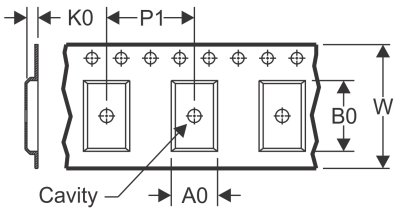
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

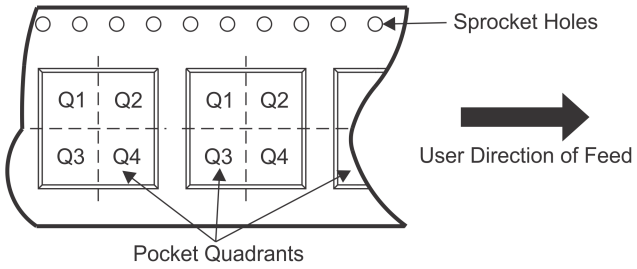


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

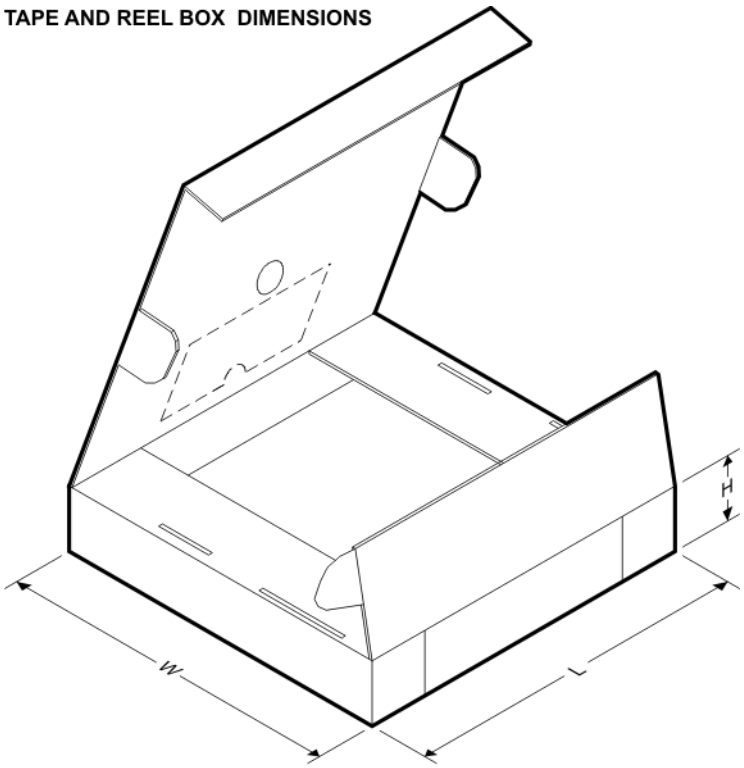
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

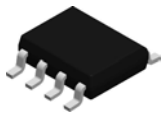
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA699IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA699IDR	SOIC	D	8	2500	367.0	367.0	35.0

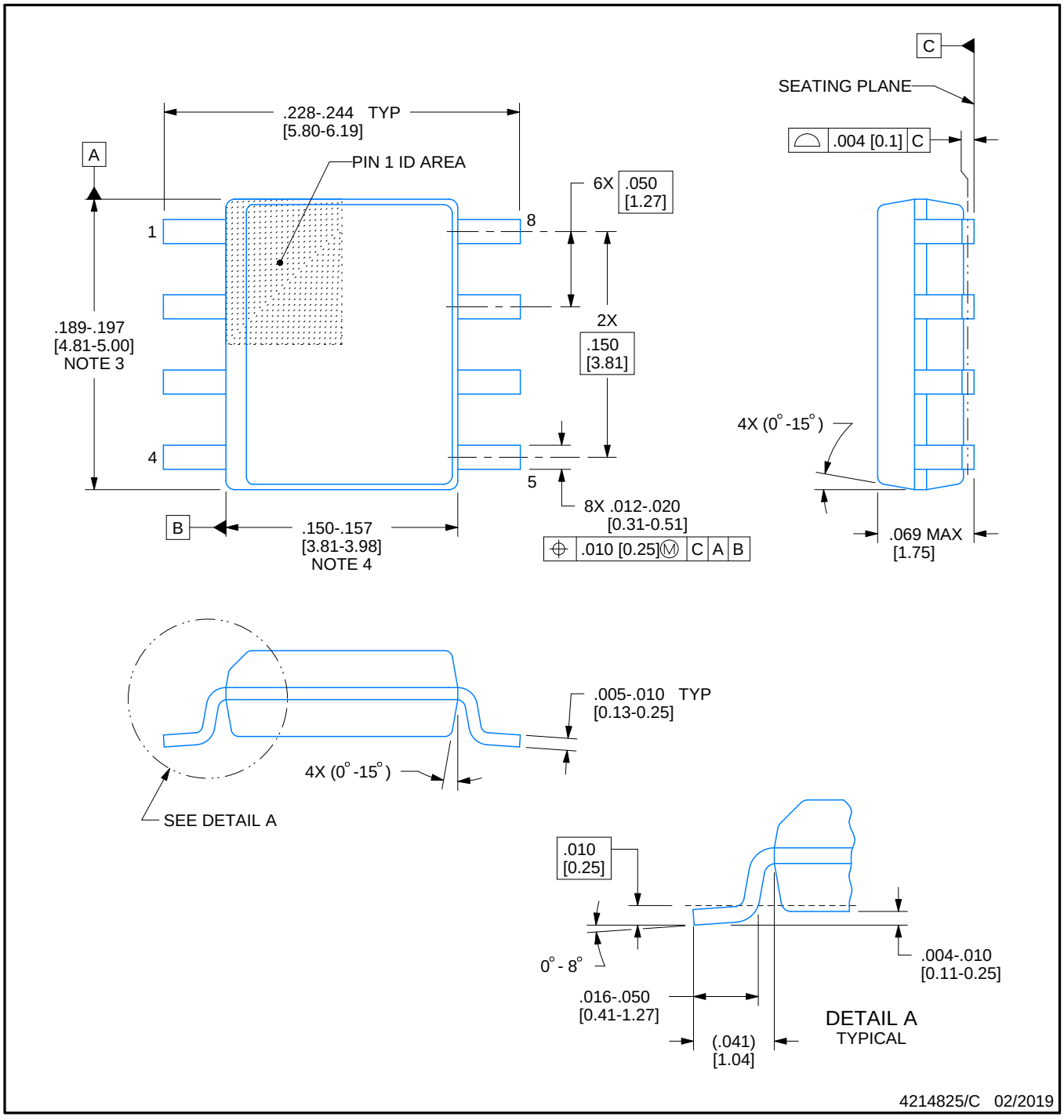


PACKAGE OUTLINE

D0008A

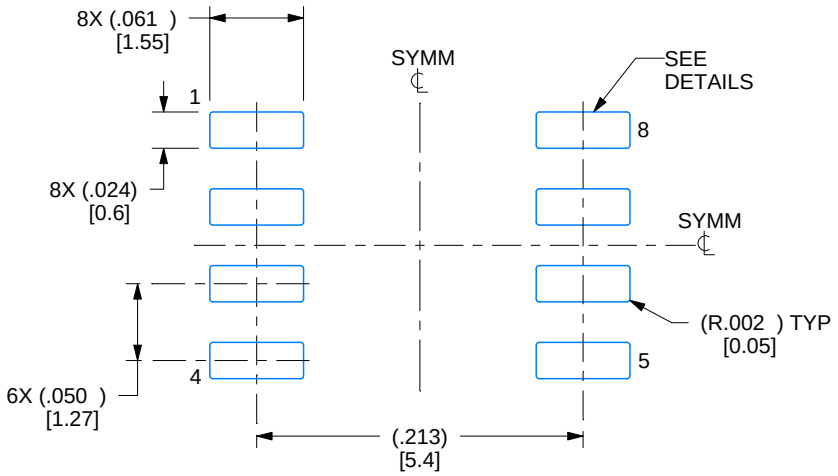
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

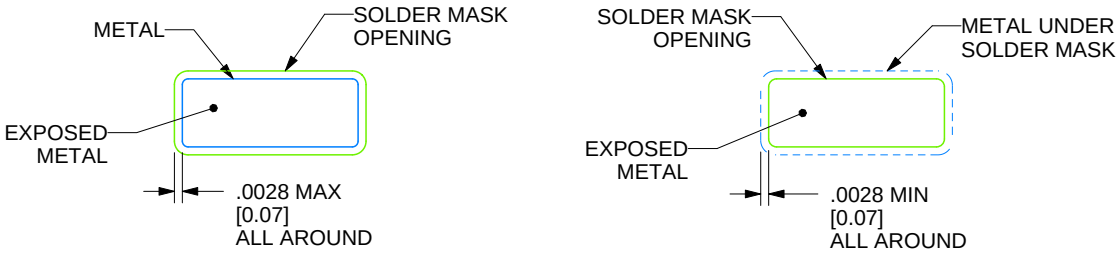


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

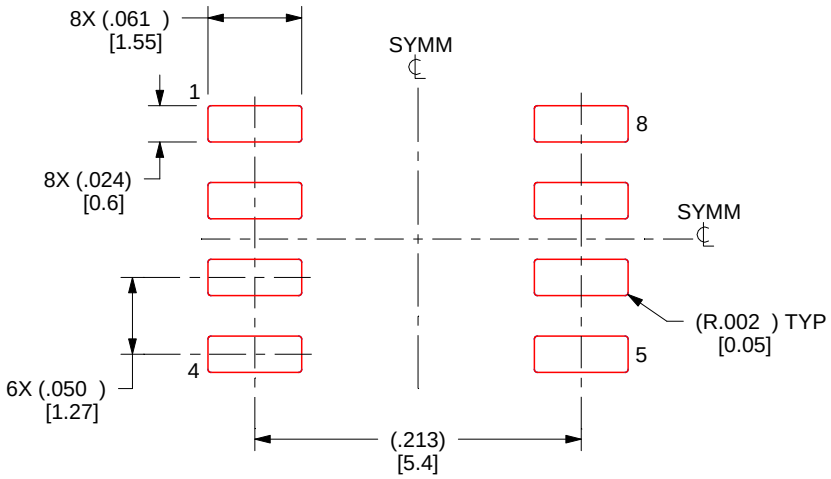
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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