LMH6574 4:1 高速视频多路复用器

1 特性

- 500MHz、500mV −3dB 带宽、A_V = 2
- 400MHz、$2V_{PP}$ −3dB 带宽、A_V = 2
- 8ns 通道开关时间
- 70dB 通道到通道隔离（在 10MHz 条件下）
- 0.02% 差动增益，0.05° 差动相位
- 0.1dB 增益平坦度：150MHz
- 2200V/µs 压摆率
- 宽电源电压范围：6V (±3V) 至 12V (±6V)
- 5MHz 时为 −68dB HD2
- 5MHz 时为 −84dB HD3

2 应用

- 视频路由器
- 多输入视频监控器
- 仪表/测试设备
- 接收器中频分集开关
- 多通道模数转换驱动器
- 画中画视频开关

3 说明

LMH6574 是一款经过优化的高性能模拟多路复用器，适用于专业级视频应用和其他高保真度、高带宽模拟应用。输出放大器可根据两个地址位的状态选择四个输入信号中的任何一个。LMH6574 可在 $2V_{PP}$ 输出信号电平提供 400MHz 带宽。LMH6574 具有 150MHz 的 0.1dB 带宽和 2200V/µs 的压摆率，这对多媒体和高清电视 (HDTV) 应用 非常有利。

LMH6574 针对 NTSC 和 PAL 视频信号的差动增益误差和差动相位误差分别为 0.02% 和 0.05°，支持复合视频 应用 ，同时可驱动后部端接的单个 75Ω 负载。该器件可提供 80mA 线性输出电流来驱动多个视频负载 应用。

LMH6574 支持通过外部反馈和增益设置电阻器来设置增益，以实现最大灵活性。

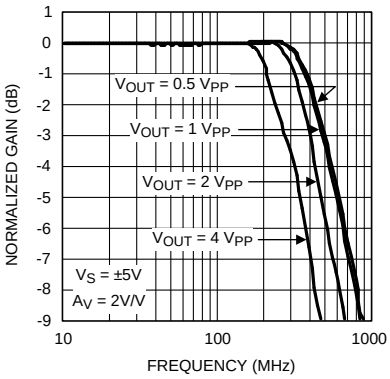
LMH6574 可提供 14 引脚 SOIC 封装。

器件信息(1)

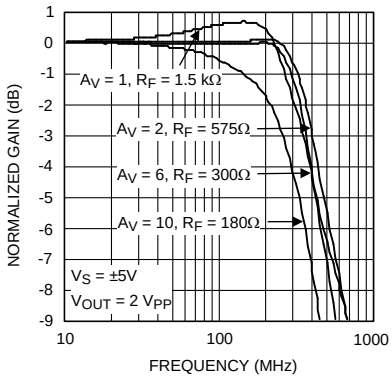
器件型号	封装	封装尺寸（标称值）
LMH6574	SOIC (14)	8.65mm × 3.91mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

频率响应与 V_{OUT} 间的关系



频率响应与增益间的关系



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ±5 V ... 5
6.6 Electrical Characteristics ±3.3 V ... 7
6.7 Typical Characteristics ... 8
7 **Detailed Description** ... 13
7.1 Functional Block Diagram ... 13
7.2 Feature Description ... 13
7.3 Device Functional Modes ... 16
8 **Application and Implementation** ... 17
8.1 Application Information ... 17
9 **Power Supply Recommendations** ... 21
9.1 Power Dissipation ... 21
10 **Layout** ... 21
10.1 Layout Guidelines ... 21
11 器件和文档支持 ... 22
11.1 文档支持 ... 22
11.2 接收文档更新通知 ... 22
11.3 社区资源 ... 22
11.4 商标 ... 22
11.5 静电放电警告 ... 22
11.6 术语表 ... 22
12 机械、封装和可订购信息 ... 22

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (December 2014) to Revision E **Page**

- Changed IBN parameter maximum specifications from ±*5 µA* to ±*5.2 µA* and from ±*5.6 µA* to ±*5.8 µA* ... 5
- Changed PSRR parameter minimum specifications from *47 dB* to *43 dB* and from *45 dB* to *41 dB* ... 5
- Changed *Supply Current Disabled* parameter maximum specifications from *5.8 mA* to *6.2 mA* and from *5.9 mA* to *6.3 mA* ... 6
- Changed IiL parameter minimum specifications from *–2.9 µA* to *–3.3 µA* and from *–8.5 µA* to *–9 µA* ... 6
- Added *Feature Description* and *Device Functional Modes* sections ... 13

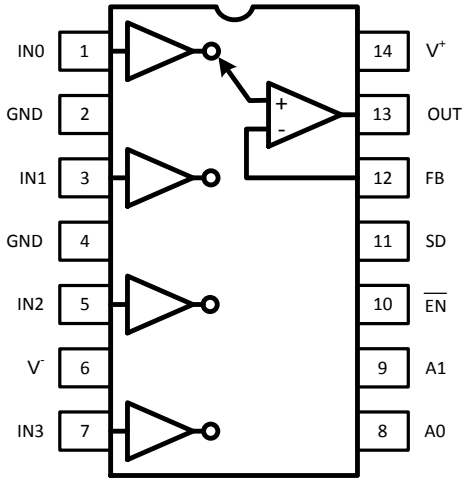
Changes from Revision C (November 2012) to Revision D **Page**

- 添加、更新或修订了以下部分：*引脚配置和功能*、*规格*、*应用和实施*、*电源建议*、*布局*、*器件和文档支持* 以及*机械、封装和可订购信息* ... 1
- Revised text in *Application and Implementation* section, formerly titled "Application Notes" ... 17
- Revised text in *Multiplexer Expansion* section. Added Figure 31, Figure 32, and Figure 33 ... 17

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5 Pin Configuration and Functions

14-Pin SOIC
Package D
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN0	I	Input Channel 0
2	GND	—	Ground
3	IN1	I	Input Channel 1
4	GND	—	Ground
5	IN2	I	Input Channel 2
6	V^-	I	V^- Supply
7	IN3	I	Input Channel 3
8	A0	I	Select Pin A0
9	A1	I	Select Pin A1
10	$\overline{EN}$	I	Enable
11	SD	I	Shutdown
12	FB	I	Feedback
13	OUT	O	Output
14	V^+	I	V^+ Supply

Truth Table

A1	A0	$\overline{EN}$	SD	OUT
1	1	0	0	CH 3
1	0	0	0	CH2
0	1	0	0	CH1
0	0	0	0	CH 0
X	X	1	0	Disable
X	X	X	1	Shutdown

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6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

	MIN	MAX	UNIT
Supply Voltage ($V^+ - V^-$)		13.2	V
I_{OUT}(3)		130	mA
Signal & Logic Input Pin Voltage		±(V_S+0.6)	V
Signal & Logic Input Pin Current		±20	mA
Maximum Junction Temperature		+150	°C
Storage Temperature	−65	+150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics ±5 V tables
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Machine model (MM)	±200	

(1) Human Body model, 1.5 kΩ in series with 100 pF. Machine model, 0 Ω In series with 200 pF.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Operating Temperature	−40		85	°C
Supply Voltage	6		12	V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics ±5 V tables

6.4 Thermal Information

THERMAL METRIC(1)		D	UNIT
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics ±5 V

V_S = ±5 V, R_L = 100 Ω, A_V = 2 V/V, R_F = 575 Ω, T_J = 25 °C, unless otherwise specified.

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE							
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}			500		MHz
LSBW	–3 dB Bandwidth	V_{OUT} = 2 V_{PP}			400		MHz
.1 dBBW	0. 1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}			150		MHz
DG	Differential Gain	R_L = 150 Ω, f = 4.43 MHz			0.02%		
DP	Differential Phase	R_L = 150 Ω, f = 4.43 MHz			0.05		deg
XTLK	Channel to Channel Crosstalk	All Hostile, 5 MHz			−85		dB
TIME DOMAIN RESPONSE							
TRS	Channel to Channel Switching Time	Logic Transition to 90% Output			8		ns
	Enable and Disable Times	Logic Transition to 90% or 10% Output			10		ns
TRL	Rise and Fall Time	4-V Step			2.4		ns
TSS	Settling Time to 0.05%	2-V Step			17		ns
OS	Overshoot	2-V Step			5%		
SR	Slew Rate	4-V Step			2200		V/µs
DISTORTION							
HD2	2nd Harmonic Distortion	2 V_{PP} , 5 MHz			−68		dBc
HD3	3rd Harmonic Distortion	2 V_{PP} , 5 MHz			−84		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two Tones 2 V_{PP} at Output			−80		dBc
EQUIVALENT INPUT NOISE							
VN	Voltage	>1 MHz, Input Referred			5		nV/√Hz
ICN	Current	>1 MHz, Input Referred			5		pA/√Hz
STATIC, DC PERFORMANCE							
CHGM	Channel to Channel Gain Difference	DC, Difference in Gain Between Channels			±0.005%	±0.032%	
			-40°C ≤ T_J ≤ 85°C			±0.035%	
VIO	Input Offset Voltage(2)	V_{IN} = 0 V			1	±20	mV
			-40°C ≤ T_J ≤ 85°C			±25	
DVIO	Offset Voltage Drift				30		µV/°C
IBN	Input Bias Current(2)(3)	V_{IN} = 0 V			−3	±5.2	µA
			-40°C ≤ T_J ≤ 85°C			±5.8	
DIBN	Bias Current Drift				11		nA/°C
	Inverting Input Bias Current	Pin 12, Feedback Point, V_{IN} = 0 V			−7	±10	
			-40°C ≤ T_J ≤ 85°C			±13	
PSRR	Power Supply Rejection Ratio(2)	DC, Input Referred		43	54		dB
			-40°C ≤ T_J ≤ 85°C	41			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. See *Application and Implementation* for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
(2) Parameters guaranteed by electrical testing at 25°C.
(3) Positive Value is current into device.

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Electrical Characteristics ±5 V (continued)

V_S = ±5 V, R_L = 100 Ω, A_V = 2 V/V, R_F = 575 Ω, T_J = 25 °C, unless otherwise specified.

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
ICC	Supply Current(2)	No Load			13	16	mA
			-40°C ≤ T_J ≤ 85°C			18	
	Supply Current Disabled(2)	$\overline{\text{ENABLE}}$ > 2 V			4.7	6.2	mA
			-40°C ≤ T_J ≤ 85°C			6.3	
	Supply Current Shutdown	SHUTDOWN > 2 V			1.8	2.5	mA
			-40°C ≤ T_J ≤ 85°C			2.6	
VIH	Logic High Threshold(2)	Select & Enable Pins (SD & $\overline{\text{EN}}$)		2.0			V
VIL	Logic Low Threshold(2)	Select & Enable Pins (SD & $\overline{\text{EN}}$)				0.8	V
IiL	Logic Pin Input Current Low(3)	Logic Input = 0 V Select & Enable Pins (SD & $\overline{\text{EN}}$)		−3.3	−1		µA
			-40°C ≤ T_J ≤ 85°C	–9			
IiH	Logic Pin Input Current High(3)	Logic Input = 2.0 V, Select & Enable Pins (SD & $\overline{\text{EN}}$)			47	68	µA
			-40°C ≤ T_J ≤ 85°C			72.5	
MISCELLANEOUS PERFORMANCE							
RIN+	Input Resistance				5		kΩ
CIN	Input Capacitance				0.8		pF
ROUT	Output Resistance	Output Active, ($\overline{\text{EN}}$ and SD < 0.8 V)			0.04		Ω
ROUT	Output Resistance	Output Disabled, ($\overline{\text{EN}}$ or SD > 2 V)			3000		Ω
COUT	Output Capacitance	Output Disabled, ($\overline{\text{EN}}$ or SD > 2 V)			3.1		pF
VO	Output Voltage Range	No Load		±3.54	±3.7		V
			-40°C ≤ T_J ≤ 85°C	±3.53			
VOL		R_L = 100 Ω		±3.18	±3.5		V
			-40°C ≤ T_J ≤ 85°C	±3.17			
CMIR	Input Voltage Range			±2.5	±2.6		V
IO	Linear Output Current(2)(3)	V_{IN} = 0 V		+60	±80		mA
				-70			
			-40°C ≤ T_J ≤ 85°C	+50			
			-40°C ≤ T_J ≤ 85°C	−60			
ISC	Short Circuit Current(4)	V_{IN} = ±2 V, Output Shorted to Ground			±230		mA

(4) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the *Power Dissipation* for more details. A short circuit condition should be limited to 5 seconds or less.

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6.6 Electrical Characteristics ±3.3 V

V_S = ±3.3 V, R_L = 100 Ω, A_V = 2 V/V, R_F = 575 Ω; unless otherwise specified.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		475		MHz
LSBW	−3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		375		MHz
0.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		100		MHz
GFP	Peaking	DC to 200 MHz		0.4		dB
XTLK	Channel to Channel Crosstalk	All Hostile, f = 5 MHz		−85		dBc
TIME DOMAIN RESPONSE						
TRL	Rise and Fall Time	2-V Step		2		ns
TSS	Settling Time to 0.05%	2-V Step		20		ns
OS	Overshoot	2-V Step		5%		
SR	Slew Rate	2-V Step		1400		V/µs
DISTORTION						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10 MHz		−67		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 10 MHz		−87		dBc
STATIC, DC PERFORMANCE						
VIO	Input Offset Voltage	V_{IN} = 0 V		-5		mV
IBN	Input Bias Current(2)	V_{IN} = 0 V		-3		µA
PSRR	Power Supply Rejection Ratio	DC, Input Referred		49		dB
ICC	Supply Current	No Load		12		mA
VIH	Logic High Threshold	Select & Enable Pins (SD & $\overline{EN}$)	1.3			V
VIL	Logic Low Threshold	Select & Enable Pins (SD & $\overline{EN}$)			0.4	V
MISCELLANEOUS PERFORMANCE						
RIN+	Input Resistance			5		kΩ
CIN	Input Capacitance			0.8		pF
ROUT	Output Resistance			0.06		Ω
VO	Output Voltage Range	No Load		±2		V
VOL		R_L = 100 Ω		±1.8		V
CMIR	Input Voltage Range			±1.2		V
IO	Linear Output Current	V_{IN} = 0 V		±60		mA
ISC	Short Circuit Current	V_{IN} = ±1 V, Output Shorted to Ground		±150		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See *Application and Implementation* for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Positive Value is current into device.

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6.7 Typical Characteristics

V_S = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 575 Ω, unless otherwise specified.

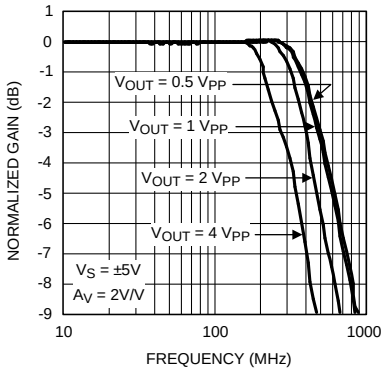


Figure 1. Frequency Response vs V_{OUT}

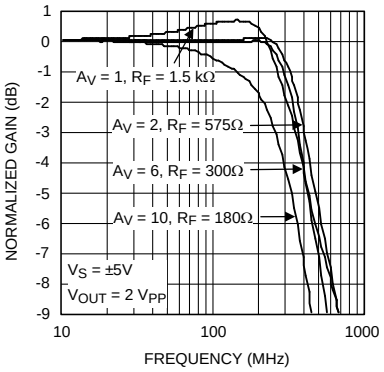


Figure 2. Frequency Response vs Gain

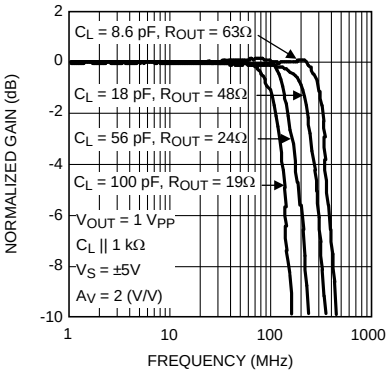


Figure 3. Frequency Response vs Capacitive Load

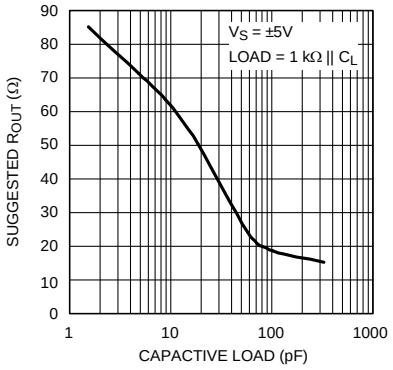


Figure 4. Suggested R_{OUT} vs Capacitive Load

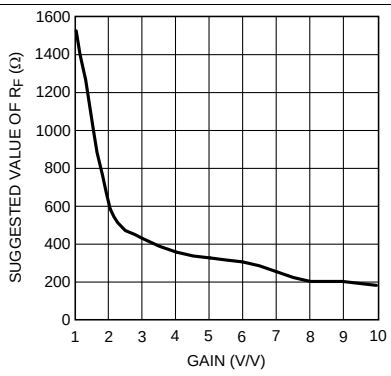


Figure 5. Suggested Value of R_F vs Gain

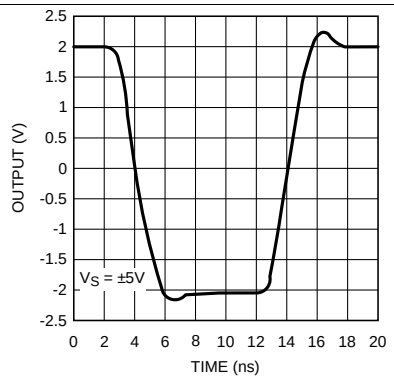


Figure 6. Pulse Response 4V_{PP}

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Typical Characteristics (continued)

V_S = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 575 Ω, unless otherwise specified.

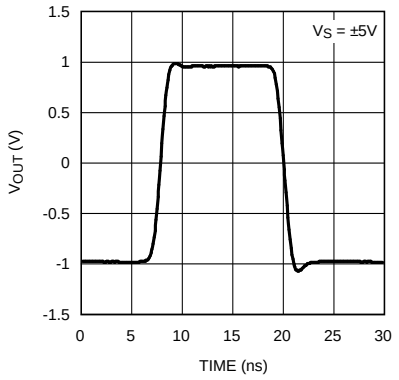


Figure 7. Pulse Response 2V_{PP}

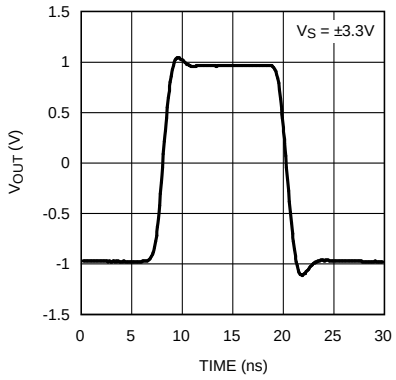


Figure 8. Pulse Response 2V_{PP}

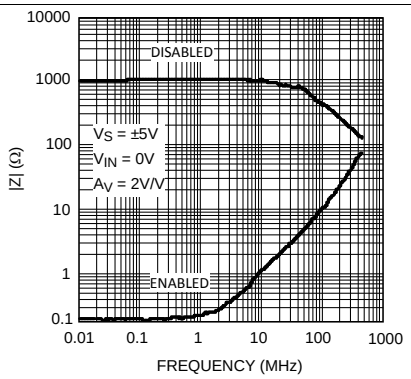


Figure 9. Closed Loop Output Impedance

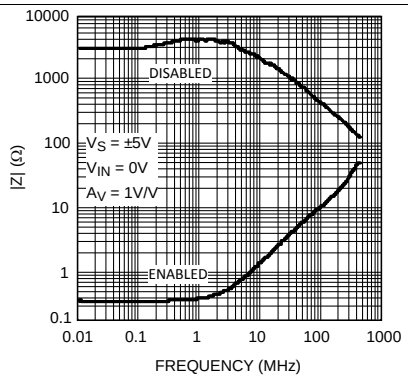


Figure 10. Closed Loop Output Impedance

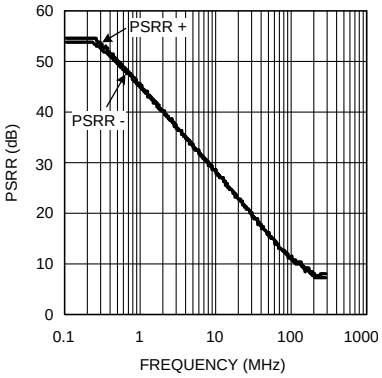


Figure 11. PSRR vs Frequency

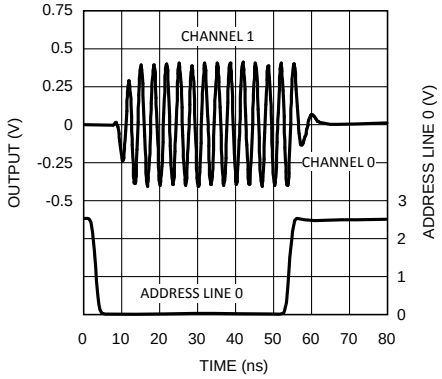


Figure 12. Channel Switching

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Typical Characteristics (continued)

V_S = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 575 Ω, unless otherwise specified.

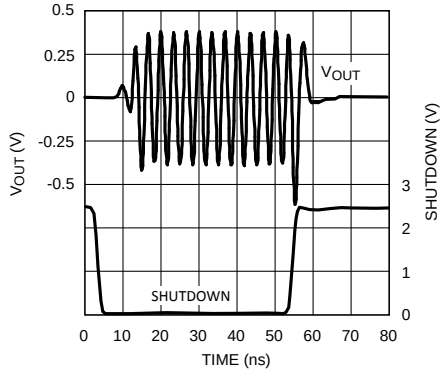


Figure 13. SHUTDOWN Switching

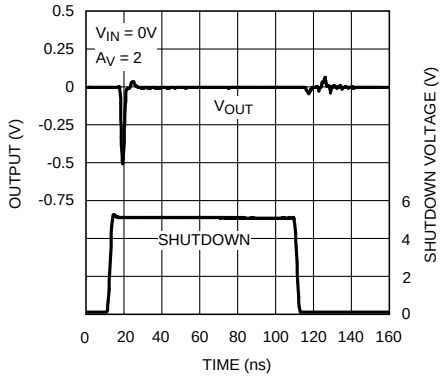


Figure 14. Shutdown Glitch

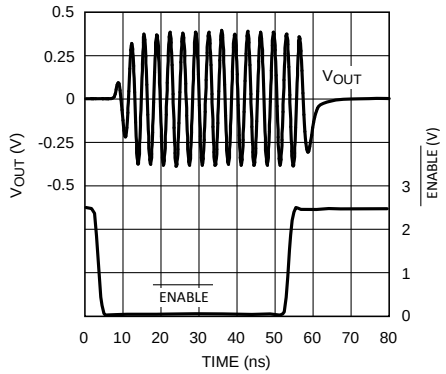


Figure 15. $\overline{\text{ENABLE}}$ Switching

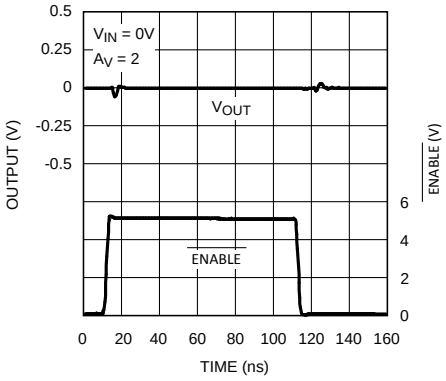


Figure 16. Disable Glitch

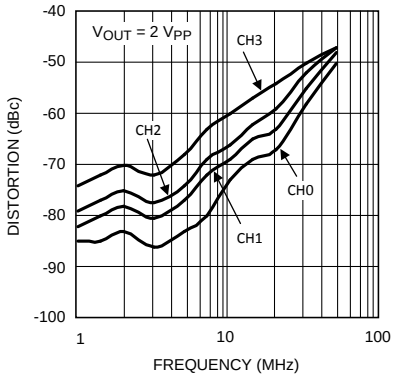


Figure 17. HD2 vs Frequency

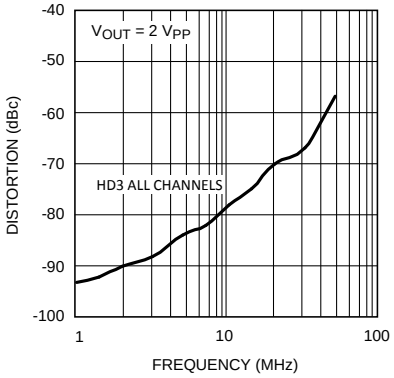


Figure 18. HD3 vs Frequency

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Typical Characteristics (continued)

V_S = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 575 Ω, unless otherwise specified.

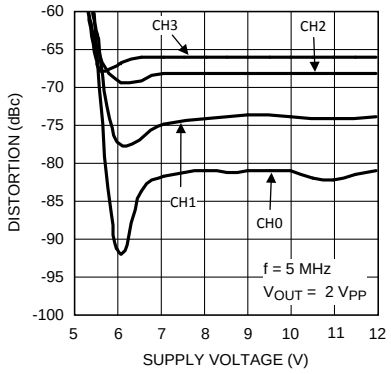


Figure 19. HD2 vs V_S

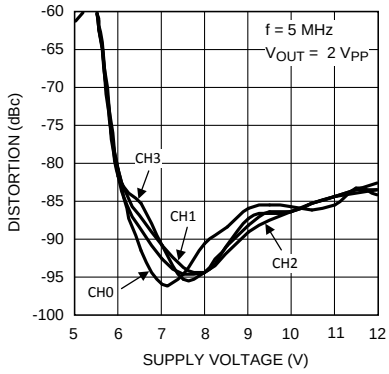


Figure 20. HD3 vs V_S

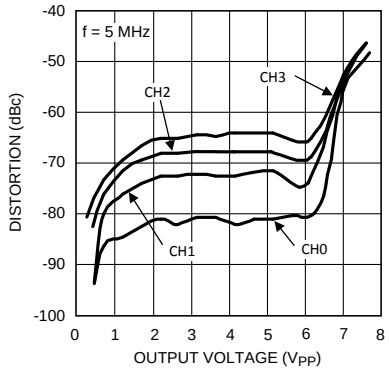


Figure 21. HD2 vs V_{OUT}

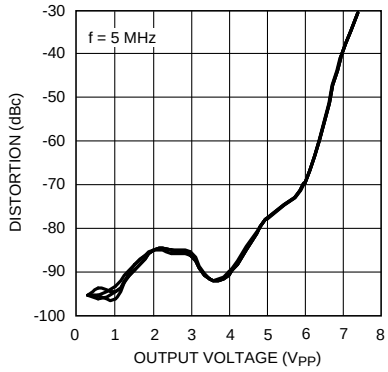
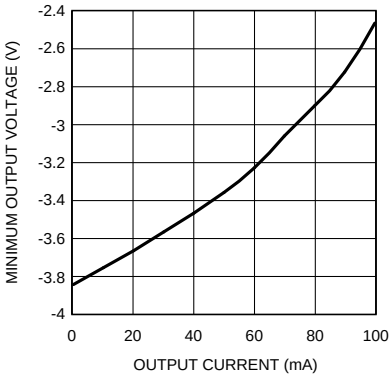
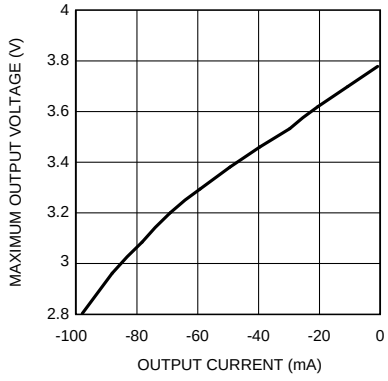


Figure 22. HD3 vs V_{OUT}



Positive Value is current into device

Figure 23. Minimum V_{OUT} vs I_{OUT}



Positive Value is current into device

Figure 24. Maximum V_{OUT} vs I_{OUT}

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Typical Characteristics (continued)

V_S = ±5 V, R_L = 100 Ω, A_V = 2, R_F = R_G = 575 Ω, unless otherwise specified.

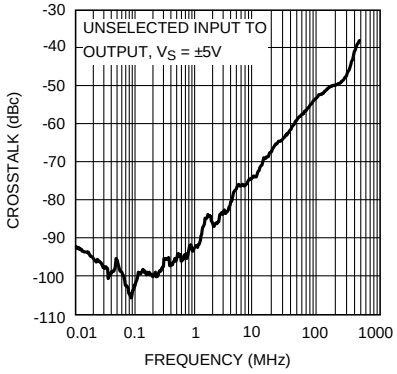


Figure 25. Crosstalk vs Frequency

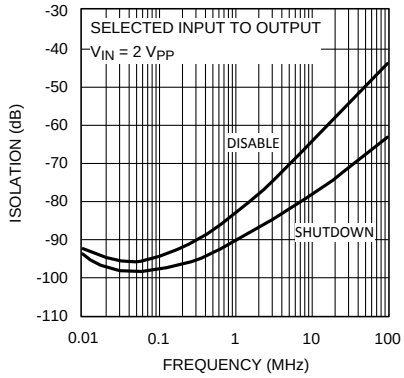
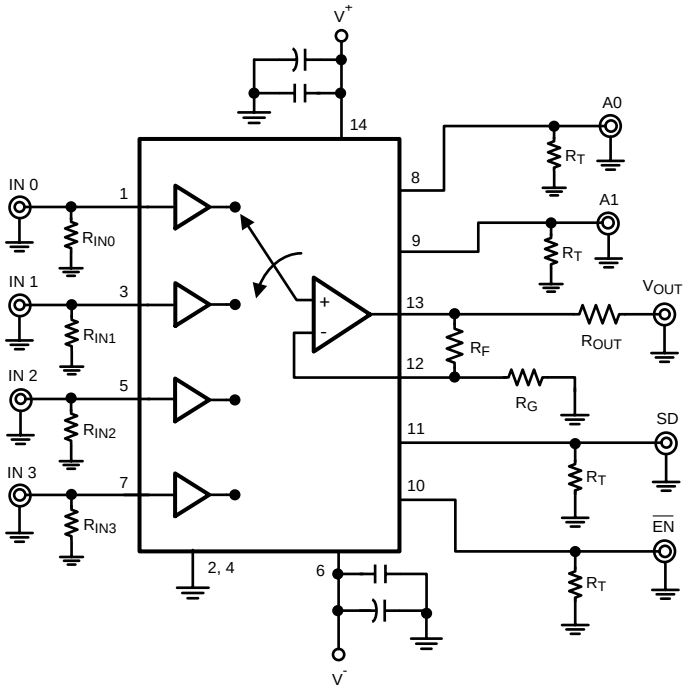


Figure 26. Off Isolation

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7 Detailed Description

7.1 Functional Block Diagram



7.2 Feature Description

7.2.1 Video Performance

The LMH6574 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. The *Functional Block Diagram* shows a typical configuration for driving a 75Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

7.2.2 Feedback Resistor Selection

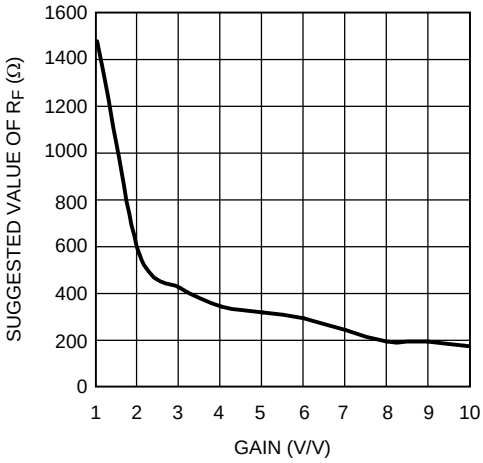


Figure 27. Suggested R_F vs Gain

Feature Description (continued)

The LMH6574 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F. For a gain of 2 V/V, the recommended value of R_F is 575Ω. For other gains see Figure 27. Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. For more information see *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 (SNOA366), which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 12 is approximately 20Ω. This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6574 will exhibit a “gain bandwidth product” similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 (SNOSA39) to provide additional gain.

7.2.3 Other Applications

The LMH6574 could support a multi antenna receiver with up to four separate antennas. Monitoring the signal strength of all 4 antennas and connecting the strongest signal to the final IF stage would provide effective spacial diversity.

For direction finding, the LMH6574 could be used to provide high speed sampling of four separate antennas to a single DSP which would use the information to calculate the direction of the received signal.

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Feature Description (continued)

7.2.4 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Figure 28 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 29 provides a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

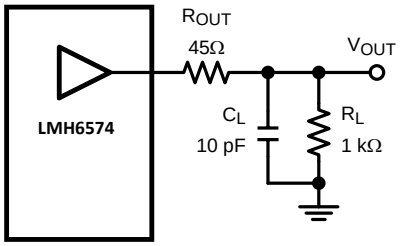


Figure 28. Decoupling Capacitive Loads

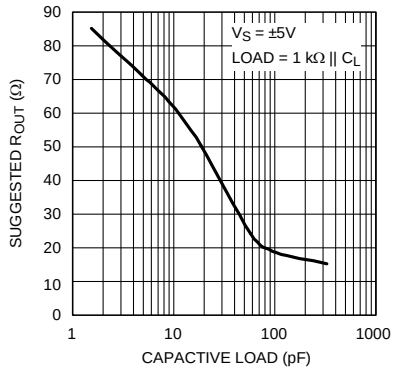


Figure 29. Suggested R_{OUT} vs Capacitive Load

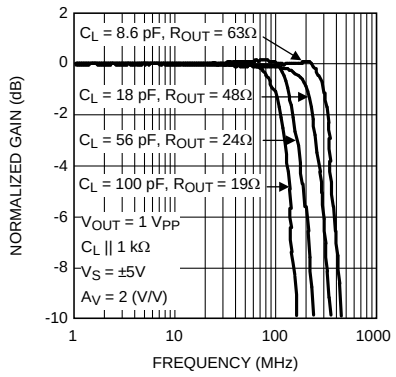


Figure 30. Frequency Response vs Capacitive Load

7.2.5 ESD Protection

The LMH6574 is protected against electrostatic discharge (ESD) on all pins. The LMH6574 will survive 2000-V Human Body model and 200-V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6574 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

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7.3 Device Functional Modes

7.3.1 SD vs $\overline{EN}$

The LMH6574 has both shutdown and disable capability. The shutdown feature affects the entire chip, whereas the disable function only affects the output buffer. When in shutdown mode, minimal power is consumed. The shutdown function is very fast, but causes a very brief spike of about 400 mV to appear on the output. When in shutdown mode the LMH6574 consumes only 1.8 mA of supply current. For maximum input to output isolation use the shutdown function.

The $\overline{EN}$ pin only disables the output buffer which results in a substantially reduced output glitch of only 50 mV. While disabled the chip consumes 4.7 mA, considerably more than when shutdown. This is because the input buffers are still active. For minimal output glitch use the $\overline{EN}$ pin. Also, care should be taken to ensure that, while in the disabled state, the voltage differential between the active input buffer (the one selected by pins A0 and A1) and the output pin stays less than 2V. As the voltage differential increases, input to output isolation decreases. Normally this is not an issue. See *Multiplexer Expansion* for further details.

To reduce the output glitch when using the SD pin, switch the $\overline{EN}$ pin at least 10 ns before switching the SD pin. This can be accomplished by using an RC delay circuit between the two pins if only one control signal is available.

Logic inputs "SD" and "$\overline{EN}$" will revert to the "High", while "A_0" and "A_1" will revert to the "Low" state when left floating.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH6574 is a high-speed 4:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6574 is ideally suited for switching high resolution, presentation grade video signals. The LMH6574 has no internal ground reference. Single or split supply configurations are both possible. The LMH6574 features very high speed channel switching and disable times. When disabled the LMH6574 output is high impedance making MUX expansion possible by combining multiple devices. See *Multiplexer Expansion*.

8.1.1 Multiplexer Expansion

It is possible to use multiple LMH6574 devices to expand the number of inputs that can be selected for output. Figure 31 shows an 8:1 MUX using two LMH6574 devices.

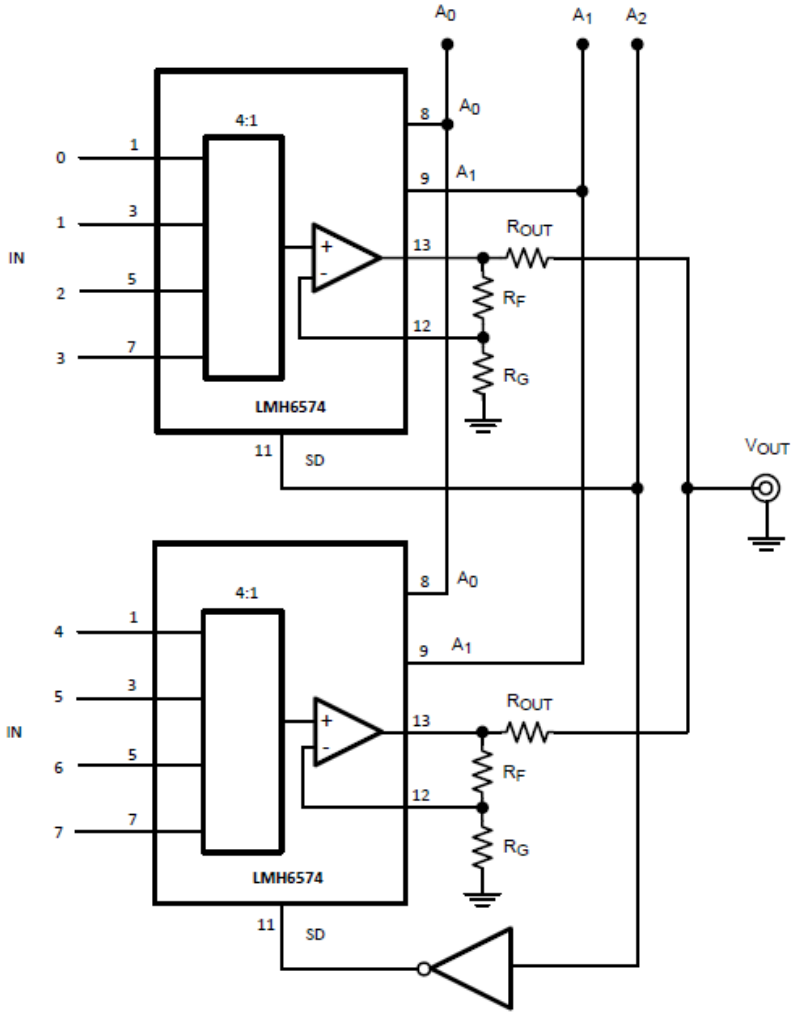


Figure 31. 8:1 MUX Using Two LMH6574 Devices

Application Information (continued)

In such an application, the output settling may be longer than the LMH6574 switching specifications (~20ns), while switching between two separate LMH6574 devices. The switching time limiting factor occurs when one LMH6574 is turned off and another one is turned on, using the SD (shutdown) pin. The output settling time consists of the time needed for the first LMH6574 to enter high impedance state plus the time required for the second LMH6574 output to dissipate the left-over output charge of the first device (limited by the output current capability of the second device) and the time needed to settle to the final voltage value.

While Figure 31 MUX expansion benefits from more isolation, originating from the parasitic loading of the un-selected channels on the selected channel, afforded by individual R_{OUT} on each multiplexer output, this configuration does not produce the fastest transition between individual LMH6574 devices. For the fastest transition, the configuration of Figure 32 can be used where the LMH6574 output pins are all shorted together.

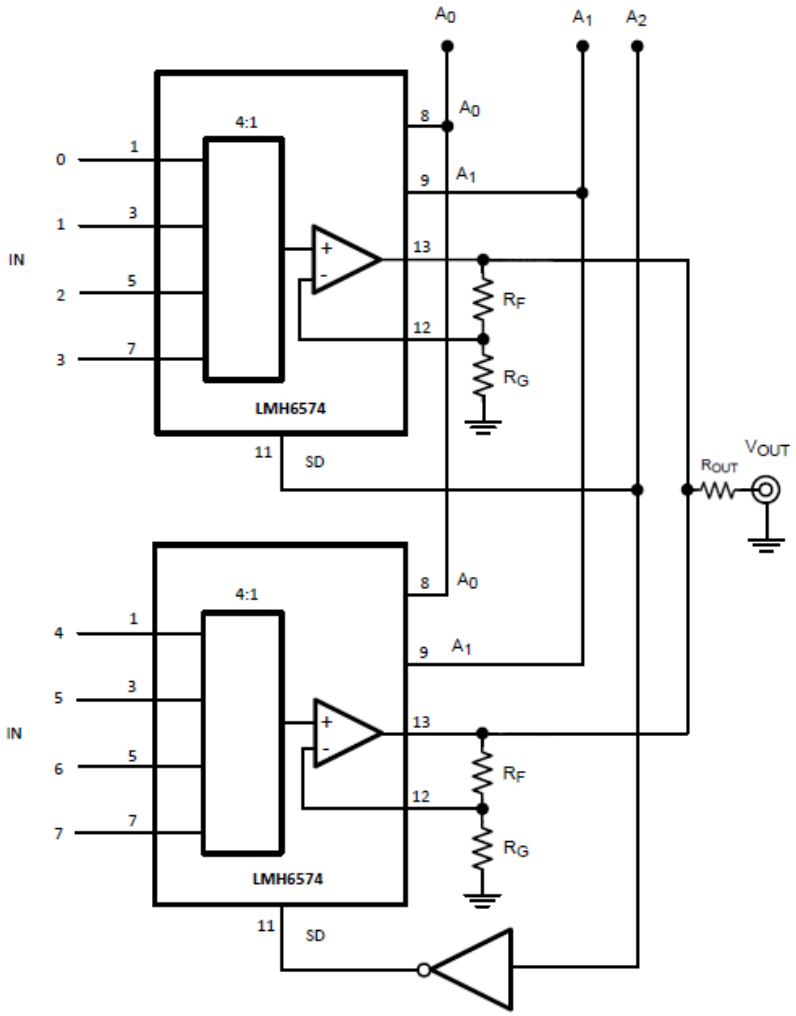


Figure 32. Alternate 8:1 MUX Expansion Schematic (for Faster SD Switching)

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Application Information (continued)

Figure 33 shows typical transition waveforms and shows that SD pin switching settles in less than 145 ns.

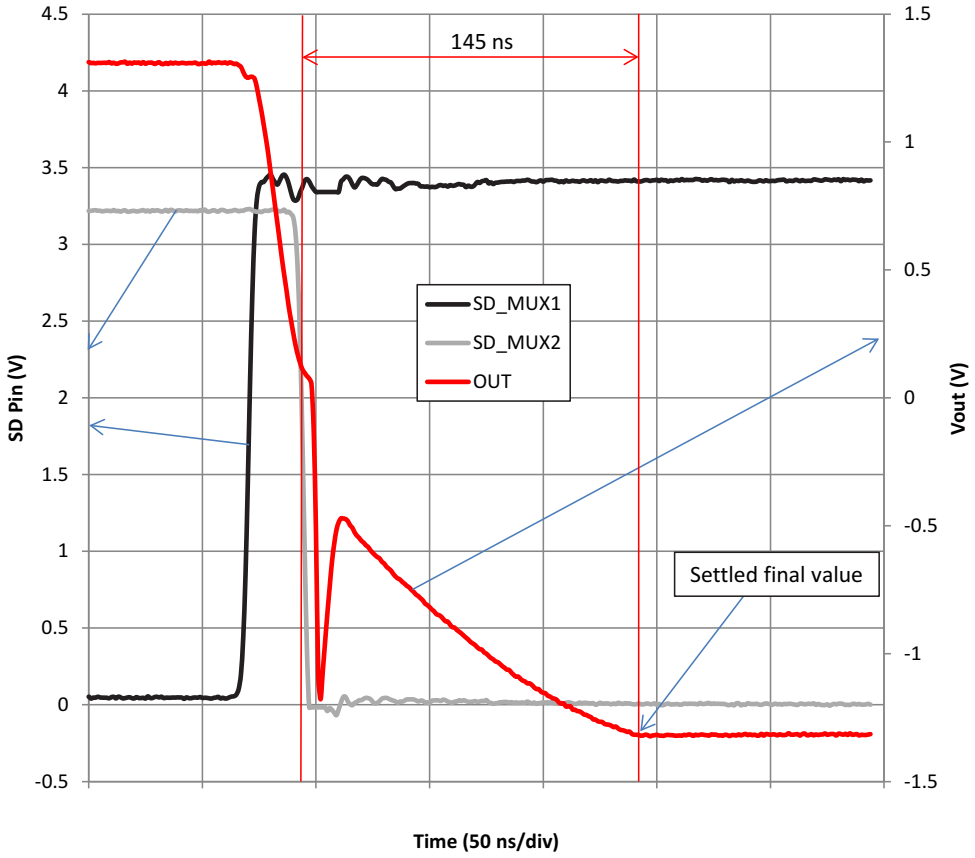


Figure 33. SD Pin Switching Waveform and Output Settling

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device. Figure 34 shows one possible approach to this delay circuit. The delay circuit shown will delay SHUTDOWN's H to L transitions (R1 and C1 decay) but will not delay its L to H transition. R2 should be kept small compared to R1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

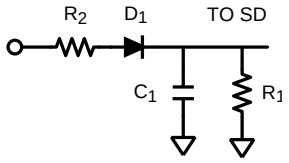


Figure 34. Delay Circuit Implementation

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Application Information (continued)

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6574's can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in Figure 35 shows how to compensate for this effect. For the 16:1 MUX function shown in Figure 35, the gain error would be about −0.8 dB, or about 9%. In the circuit in Figure 35, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

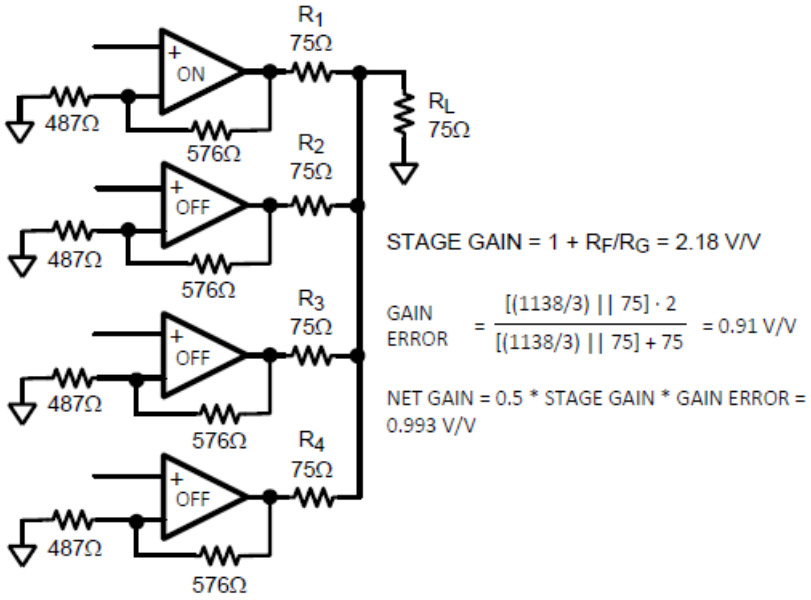


Figure 35. Multiplexer Gain Compensation

NOTE

Disabling of the LMH6574 using the EN pin is not recommended for use when doing multiplexer expansion. While disabled, If the voltage between the selected input and the chip output exceeds approximately 2V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

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9 Power Supply Recommendations

9.1 Power Dissipation

The LMH6574 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6574:

1. Calculate the quiescent (no-load) power.

   $P_{AMP} = I_{CC}* (V_S)$

   where

   - $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

   P_D (rms) = rms $((V_S - V_{OUT}) * I_{OUT})$

   where

   - V_{OUT} is the voltage across the external load
   - I_{OUT} is the current through the external load
   - V_S is the total supply voltage (2)

3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6574 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/R_{\theta JA}$

where

- T_{AMB} = Ambient temperature (°C)
- $R_{\theta JA}$ = Thermal resistance, from junction to ambient, for a given package (°C/W) (3)

For the SOIC package $R_{\theta JA}$ is 130 °C/W.

10 Layout

10.1 Layout Guidelines

Whenever questions about layout arise, use the evaluation board LMH730276 as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In the *Functional Block Diagram*, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μF and 0.1 μF ceramic capacitors for each supply bypass.

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

更多信息，请参见以下文档：

- *《OA-13 电流反馈环路增益分析和性能增强》* 应用手册
- *《IC 封装热指标》* 应用报告
- *《LMH730276 4:1 多路复用器评估板》*

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11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6574MA	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LMH65 74MA	
LMH6574MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 74MA	Samples
LMH6574MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 74MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

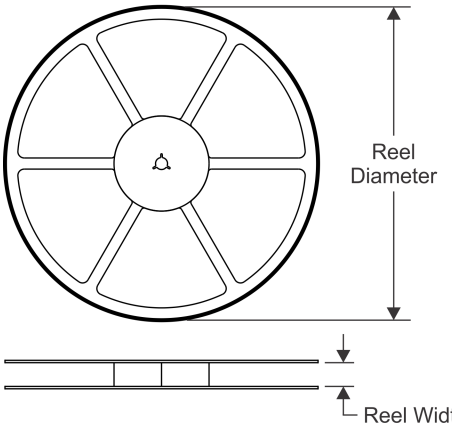
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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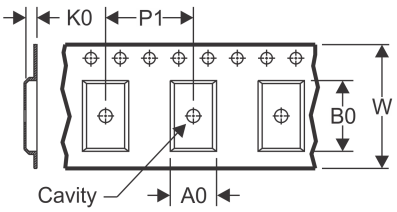
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

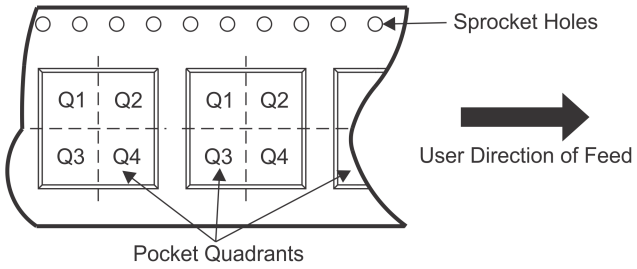


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

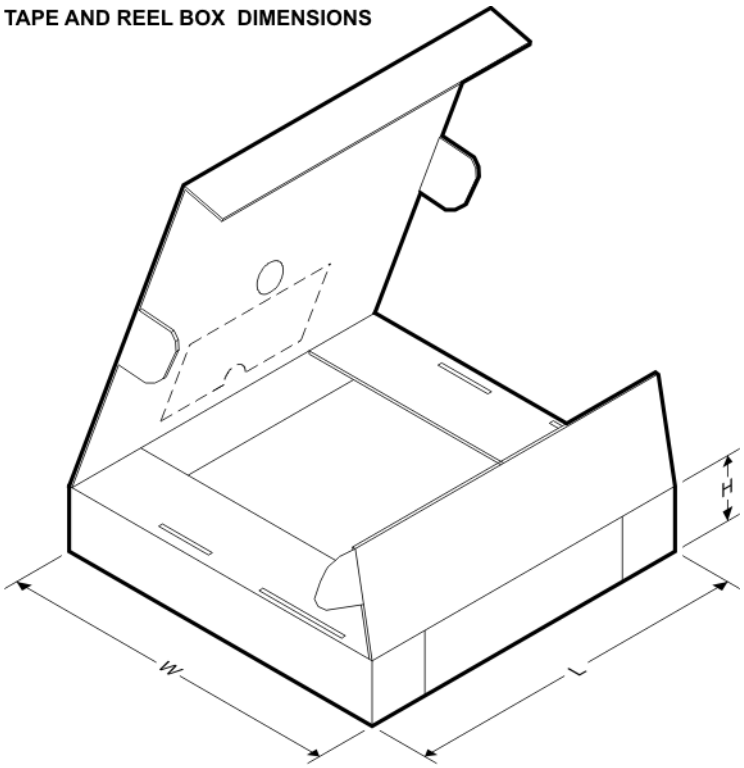
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6574MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

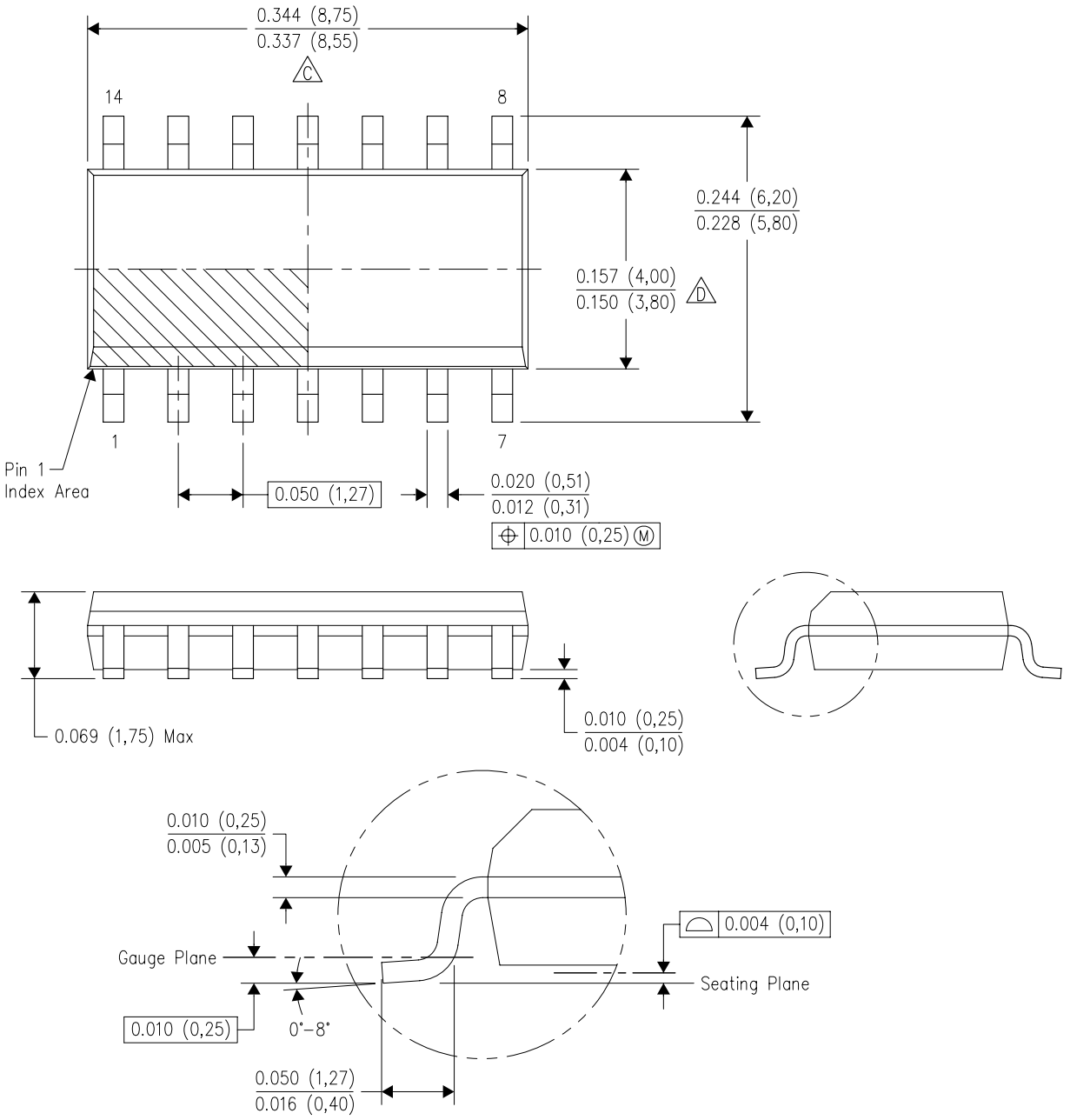
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6574MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

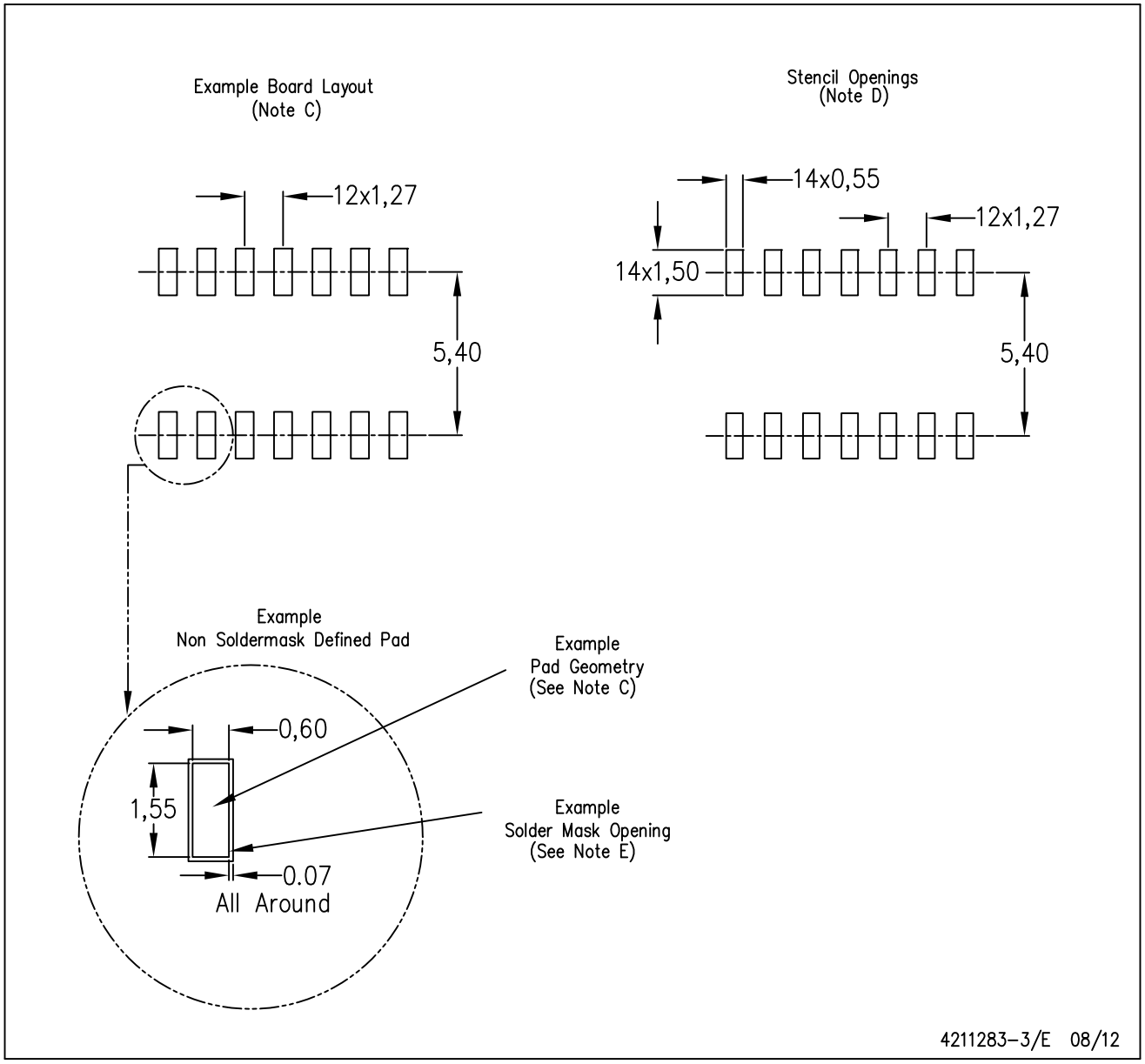
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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