SB0S296C − MARCH 2004 − REVISED FEBRUARY 2005

3V Single-Supply 80MHz High-Speed Op Amp in SC70

FEATURES

- HIGH BANDWIDTH: 80MHz
- HIGH SLEW RATE: 55V/μs
- EXCELLENT VIDEO PERFORMANCE
  - 0.5dB GAIN FLATNESS: 25MHz
  - DIFFERENTIAL GAIN: 0.3%
  - DIFFERENTIAL PHASE: 0.7°
- INPUT RANGE INCLUDES GROUND
- RAIL-TO-RAIL OUTPUT
- SHUTDOWN CURRENT: < 5μA
- LOW QUIESCENT CURRENT: 5.2mA
- SINGLE-SUPPLY OPERATING RANGE: +2.7V to +3.3V
- *Micro*SIZE PACKAGE: SC70-6

APPLICATIONS

- DIGITAL STILL CAMERAS
- CAMERA PHONES
- DIGITAL MEDIA PLAYERS
- DIGITAL VIDEO CAMERAS
- SET-TOP-BOX VIDEO FILTERS
- OPTICAL POWER MONITORING
- TRANSIMPEDANCE AMPLIFIERS
- AUTOMATIC TEST EQUIPMENT

DESCRIPTION

The high-speed OPA358 amplifier is optimized for 3V single-supply operation. The output typically swings within 5mV of GND with a 150Ω load connected to GND. The input common-mode range includes GND and swings to within 1V of the positive power supply. The OPA358 offers excellent video performance: 0.5dB gain flatness is 25MHz, differential gain is 0.3%, and differential phase is 0.7°.

The OPA358 is optimized for supply voltages from +2.7V to +3.3V, with an operating range of +2.5V to +3.6V. Quiescent current is only 5.2mA per channel.

In shutdown mode, the quiescent current is reduced to < 5μA, dramatically reducing power consumption. This is especially important in battery-operated equipment such as digital still cameras (DSCs) or mobile phones with integrated cameras.

The OPA358 is available in SC70-6, the smallest package currently available for video applications.

OPA358 RELATED PRODUCTS

FEATURES	PRODUCT
G = 2, Internal Filter, Sag Correction, Shutdown, Video Amp	OPA360
100MHz GBW, RR I/O, Shutdown, CMOS Amp	OPA357
200MHz GBW, RR Out, Shutdown, CMOS Amp	OPA355
38MHz GBW, RR I/O, CMOS Amp	OPA350
> 200MHz, Shutdown, Video Buffer Amp, G = 2	OPA692
100MHz BW, Differential Input/Output, 3.3V Supply	THS412x

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA358	SC70-6	DCK	−40°C to +85°C	AUS	OPA358AIDCKT	Tape and Reel, 250
					OPA358AIDCKR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

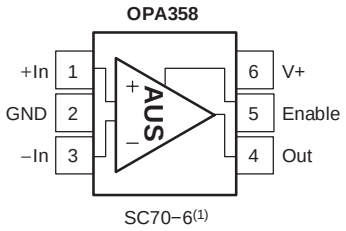
Supply Voltage, V+ to V−	+3.6V
Signal Input Terminals, Voltage(2)	(V−) −0.5V to (V+) + 0.5V
Signal Input Terminals, Current(2)	±10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+160°C
Lead Temperature (soldering, 10s)	+300°C
ESD Rating:	
Human Body Model (HBM)	4000V
Charged Device Model (CDM)	1500V
Machine Model (MM)	400V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS



SC70−6(1)

(1) Pin 1 is determined by orienting the package marking as indicated in the diagram.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +3.3V Single-Supply

Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C**.

All specifications at T_A = +25°C, R_L = 150Ω connected to V_S/2, unless otherwise noted.

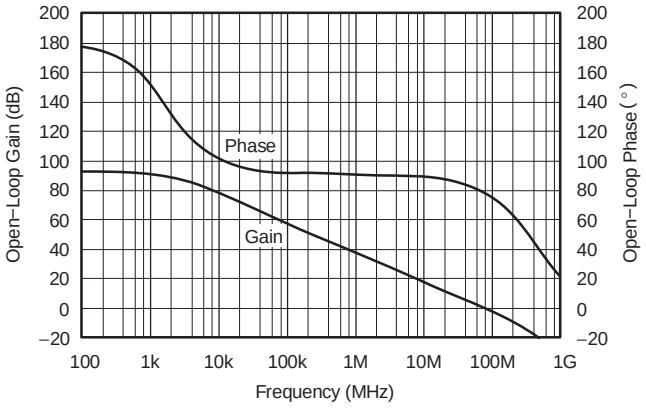
PARAMETER		CONDITIONS	OPA358 MIN	OPA358 TYP	OPA358 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +3.3V		±2	±6	mV
Over Temperature		**Specified Temperature Range**			**±15**	**mV**
Drift	**dV_{OS}/dT**	**Specified Temperature Range**		5		**µV/°C**
vs. Power Supply	PSRR	V_S = +2.7V to +3.3V		±80	±350	µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.3	±50	pA
Input Offset Current	I_{OS}			±1	±50	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1MHz		6.4		$nV/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.1		(V+) − 1.0	V
Common-Mode Rejection Ratio	CMRR	V_S = +3.3V, −0.1V < V_{CM} < 2.3V	60	80		dB
		Specified Temperature Range	**60**			**dB**
INPUT IMPEDANCE						
Differential				10^{13} || 1.5		Ω || pF
Common-Mode				10^{13} || 1.5		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_S = +3.3V, 0.1V < V_O < 3.1V	84	92		dB
Over Temperature			**See Typical Characteristics**			
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = +10, R_L = 1kΩ		80		MHz
Bandwidth for 0.1dB Gain Flatness	$f_{0.1dB}$	G = +2, V_O = 100mV_{PP}, R_F = 560Ω		12		MHz
Bandwidth for 0.5dB Gain Flatness	$f_{0.5dB}$	G = +2, V_O = 100mV_{PP}, R_F = 560Ω		25		MHz
Slew Rate	SR	V_S = +3.3V, G = +2, 2.5V Output Step		55		V/µs
Settling Time to 0.1%		G = 1, R_L = 150Ω		35		ns
Differential Gain Error		PAL, R_L = 150Ω		0.3		%
Differential Phase Error		PAL, R_L = 150Ω		0.7		°
OUTPUT						
Voltage Output Swing from Rail		V_S = +3.3V, A_{OL} > 84dB	(V−) + 100		(V+) − 200	mV
Over Temperature		**V_S = +3.3V**	**(V−) + 100**		**(V+) − 300**	**mV**
		V_S = +3.3V, V_{IN} = 0V, R_L = 150Ω to GND		5		mV
Output Current(1)	I_O	V_S = +3.3V, 0.5V from Supplies		±50		mA
Open-Loop Output Impedance		f = 1MHz, I_O = 0		20		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		3.3	V
Minimum Operating Voltage Range				2.5 to 3.6		V
Quiescent Current	I_Q	V_S = +3.3V, Enabled, I_O = 0		5.2	7.5	mA
		Specified Temperature Range			**8.5**	**mA**
ENABLE/SHUTDOWN FUNCTION						
Disabled (logic−LOW Threshold)					0.8	V
Enabled (logic−HIGH Threshold)			1.6			V
Enable Time				1.5		µs
Disable Time				50		ns
Shutdown Current		V_S = +3.3, Disabled		2.5	5	µA
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range			−40		+85	°C
Storage Range			−65		+150	°C
Thermal Resistance	θ_{JA}					
SC70				250		°C/W

(1) See typical characteristics chart, *Output Voltage Swing vs Output Current*.

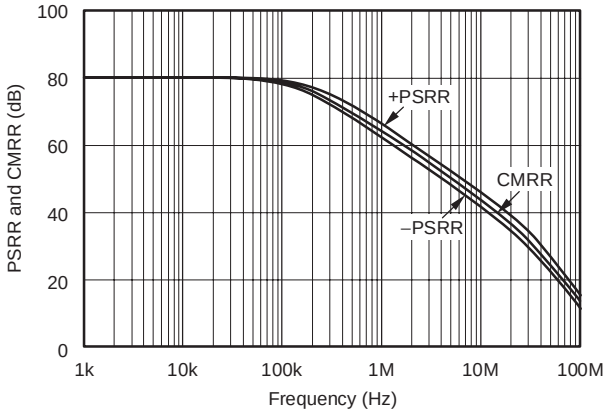
TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, R_L = 150Ω connected to V_S/2, unless otherwise noted.

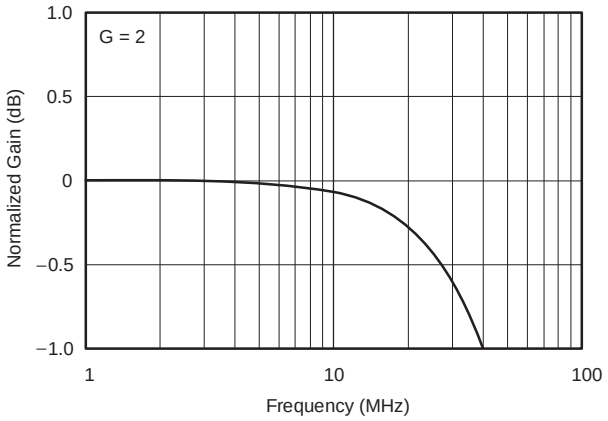
OPEN−LOOP GAIN AND PHASE vs FREQUENCY



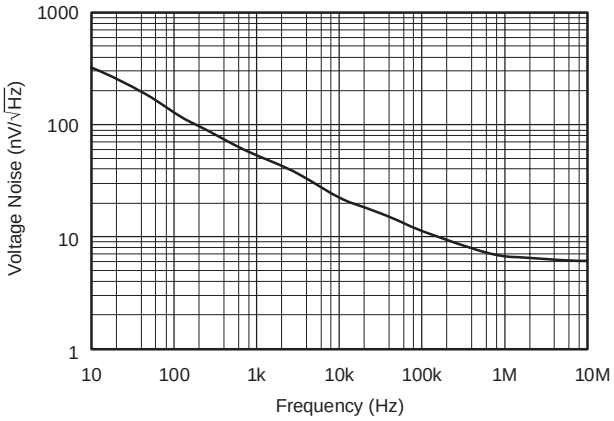
POWER−SUPPLY AND COMMON−MODE REJECTION RATIO vs FREQUENCY



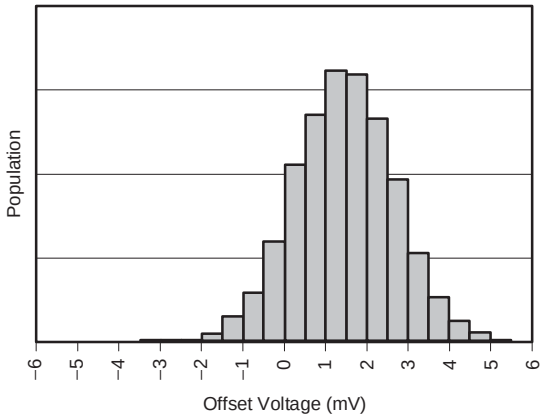
GAIN FLATNESS vs FREQUENCY



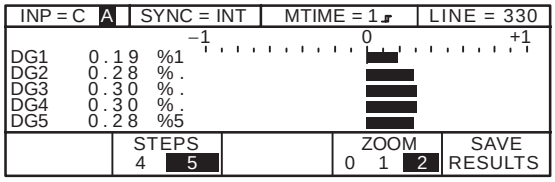
INPUT VOLTAGE NOISE SPECTRAL DENSITY



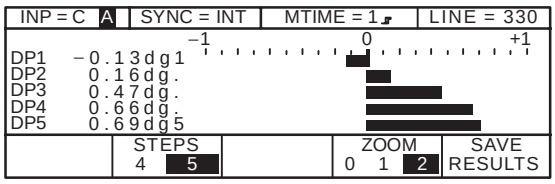
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



DIFFERENTIAL GAIN



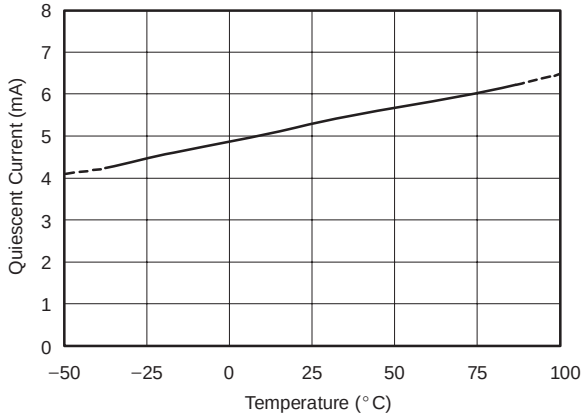
DIFFERENTIAL PHASE



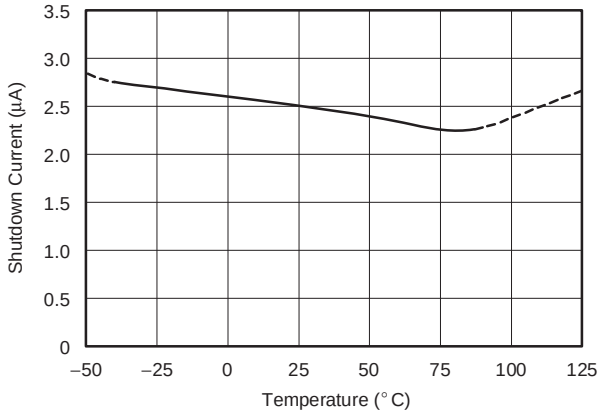
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, R_L = 150Ω connected to V_S/2, unless otherwise noted.

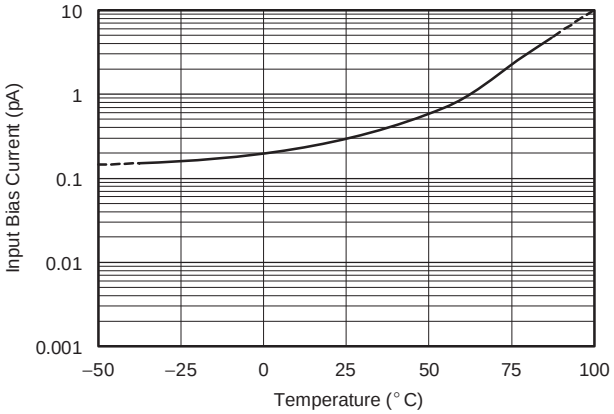
QUIESCENT CURRENT vs TEMPERATURE



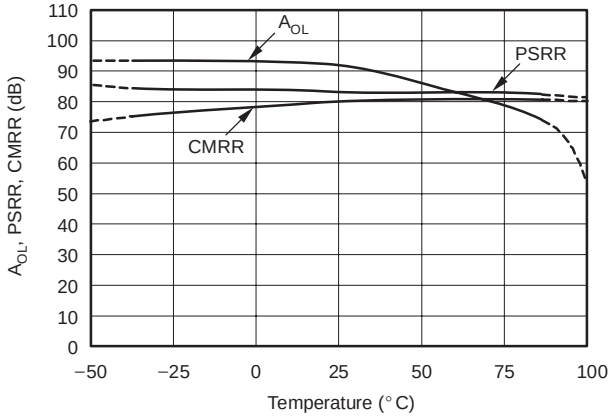
SHUTDOWN CURRENT vs TEMPERATURE



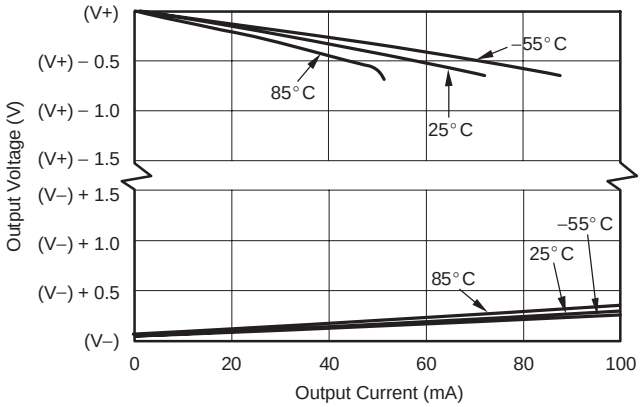
INPUT BIAS CURRENT vs TEMPERATURE



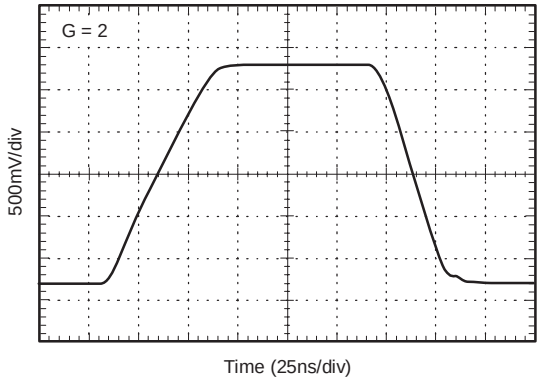
OPEN−LOOP GAIN, COMMON−MODE REJECTION, AND POWER−SUPPLY REJECTION RATIO vs TEMPERATURE



OUTPUT VOLTAGE vs OUTPUT CURRENT



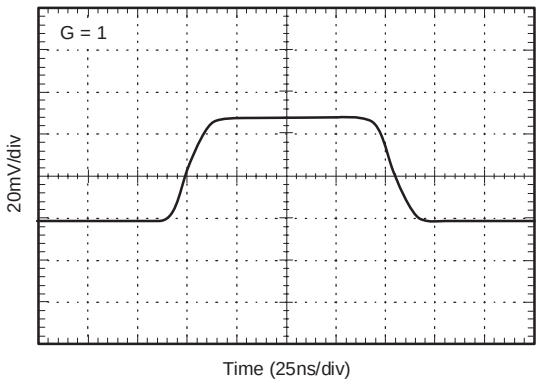
LARGE−SIGNAL TRANSIENT



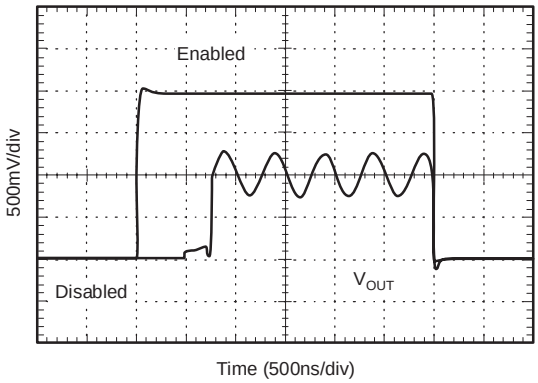
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, R_L = 150Ω connected to V_S/2, unless otherwise noted.

SMALL−SIGNAL TRANSIENT



ENABLE FUNCTION



APPLICATIONS INFORMATION

OPERATING VOLTAGE

The OPA358 is fully specified from +2.7V to +3.3V over a temperature range of −40°C to +85°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

Power-supply pins should be bypassed with a 100nF ceramic capacitor.

INPUT VOLTAGE

The input common-mode range of the OPA358 extends from (V−) − 0.1V to (V+) − 1.0V.

INPUT OVER-VOLTAGE PROTECTION

All OPA358 pins are static-protected with internal ESD protection diodes connected to the supplies. These diodes will provide input overdrive protection if the current is externally limited to 10mA.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For a 150Ω load, the output voltage swing is 100mV from the negative rail and 200mV from the positive rail when the load is connected to $V_S/2$. For lighter loads, the output swings significantly closer to the supply rails while maintaining high open-loop gain. If the load is connected to ground, the OPA358 output typically swings to within 5mV of ground. See the typical characteristic curve, *Output Voltage Swing vs Output Current*.

ENABLE/SHUTDOWN

The OPA358 has a shutdown feature that disables the output and reduces the quiescent current to less than 5μA. This feature is especially useful for portable video applications such as digital still cameras (DSCs) and camera phones, where the equipment is infrequently connected to a TV or other video device.

The Enable logic input voltage is referenced to the OPA358 GND pin. A logic level HIGH applied to the enable pin enables the op amp. A valid logic HIGH is defined as ≥ 1.6V above GND. A valid logic LOW is defined as ≤ 0.8V above GND. If the Enable pin is not connected, internal pull-up circuitry will enable the amplifier. Enable pin voltage levels are tested for a valid logic HIGH threshold of 1.6V minimum and a valid logic LOW threshold of 0.8V maximum.

The enable time is 1.5μs and the disable time is only 50ns. This allows the output of the OPA358 to be multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

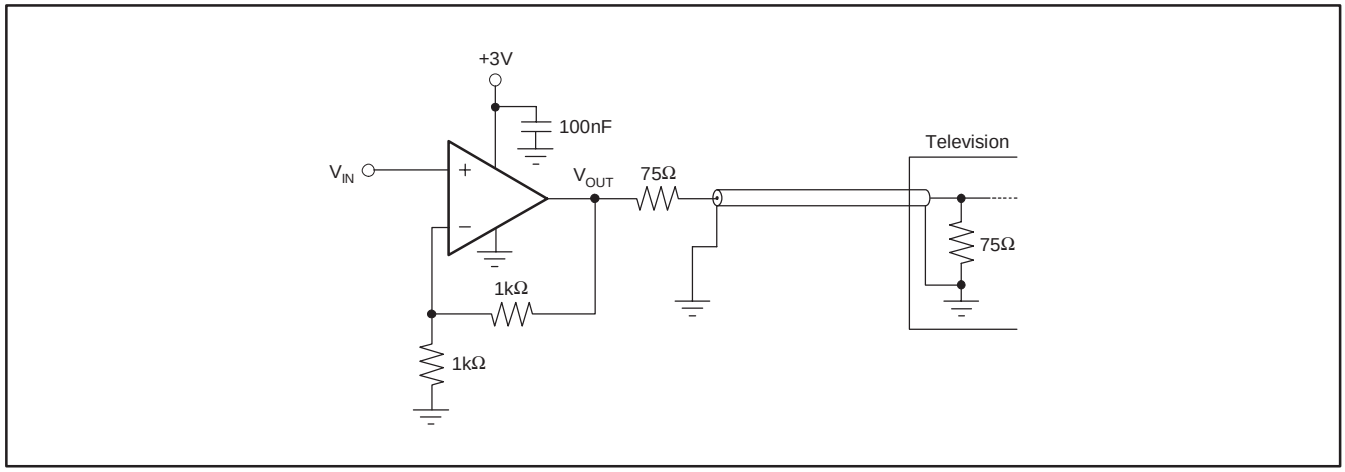


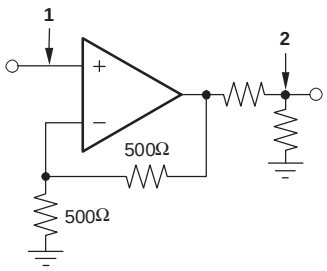
Figure 1. Typical Circuit Using the OPA358 in a Gain = 2 Configuration

VIDEO PERFORMANCE

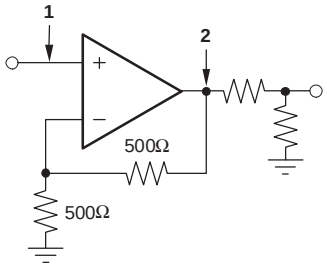
Industry standard video test patterns include:

- Multiburst—packets of different test frequencies to check for basic frequency response.
- Multipulse—pulses modulated at different frequencies to test for comprehensive measurement of amplitude and group delay errors across the video baseband.
- Chrominance-to-luminence (CCIR17) — tests amplitude, phase and some distortion

Figure 2 shows the test circuits for Figure 3 through Figure 13 and Figure 16. (NOTE: **1** and **2** indicate measurement points corresponding to the waveforms labeled **1** and **2** in the figures.)



a. Test circuit for Figure 3 through Figure 5.



b. Test circuit for Figure 6.

NOTE: **1** and **2** indicate measurement points corresponding to the waveforms labeled **1** and **2** in the figures.

Figure 2. Test Circuits Used for Figure 3 through Figure 6

FREQUENCY RESPONSE OF THE OPA358

Frequency response measurements evaluate the ability of a video system to uniformly transfer signal components of different frequencies without affecting their respective amplitudes. Figure 3 shows the multiburst test pattern; Figure 4 shows the multipulse. The top waveforms in these figures show the full test pattern. The middle and bottom waveform are a more detailed view of the critical portion of the full waveform. The middle waveform represents the input signal from the video generator; the bottom waveform is the OPA358 output to the line.

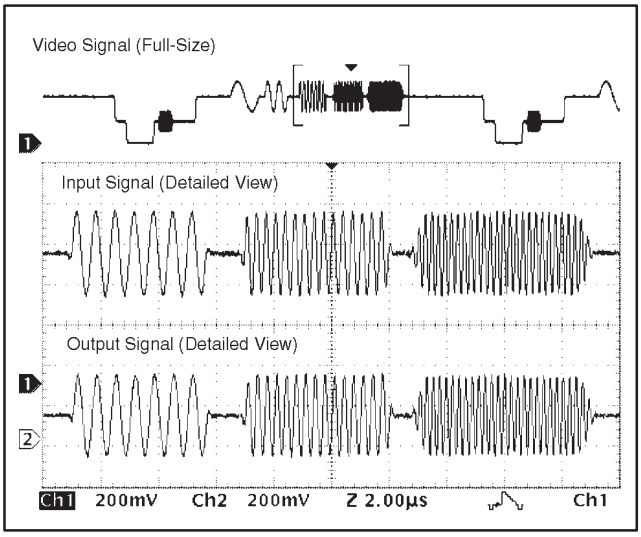


Figure 3. Multiburst (CCIR 18) Test Pattern (PAL)

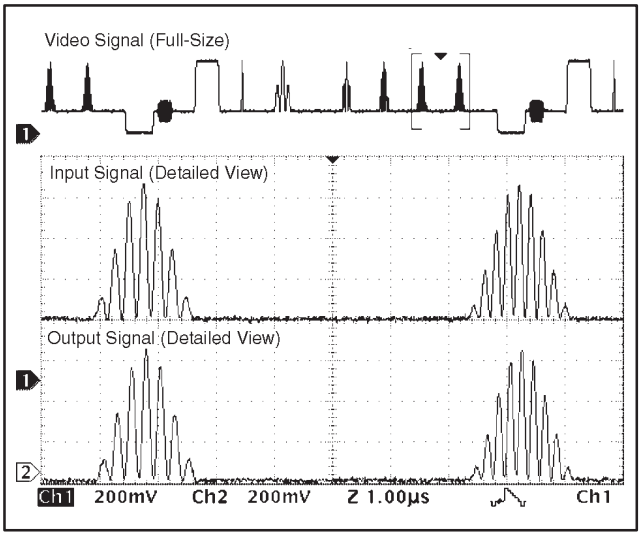


Figure 4. Multipulse Test Pattern (PAL)

Chrominance-to-luminence gain inequality (or relative chrominance level) is a change in the gain ratio of the chrominance and luminence components of a video signal, which are at different frequencies. A common test pattern is the pulse in test pattern CCIR 17, shown in Figure 5. As in Figure 3 and Figure 4, the top waveform shows the full test pattern. The middle and bottom waveform are a more detailed view of the critical portion of the full waveform, with the middle waveform representing the input signal from the video generator and the bottom waveform being the OPA358 output to the line.

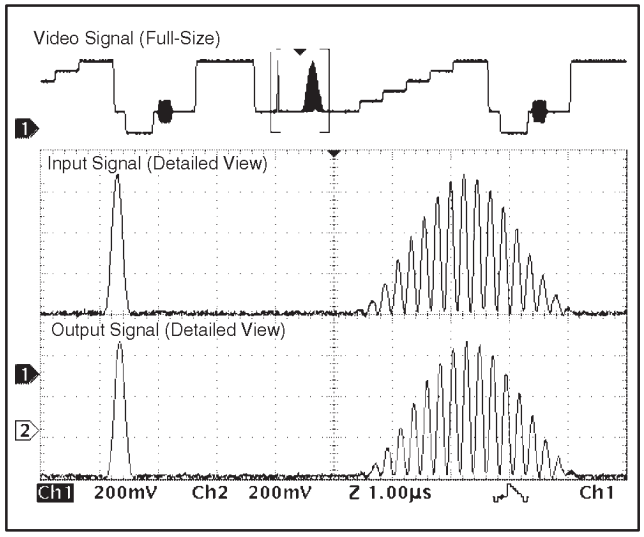


Figure 5. CCIR 17 Test Pattern (PAL)

Gain errors most commonly appear as attenuation or peaking of the chrominance information. This shows up in the picture as incorrect color saturation. Delay distortion will cause color smearing or bleeding, particularly at the edges of objects in the picture. It may also cause poor reproduction of sharp luminence transitions.

Figure 3 through Figure 5 show that the OPA358 causes no visible distortion or change in gain throughout the entire video frequency range.

OUTPUT SWING TO GND (SYNC PULSE)

Figure 6 shows the output swing capability of the OPA358 by driving the input with a sync level of 0V. The output of the OPA358 swings very close to 0V, typically to within less than 5mV with an 150Ω load connected to ground.

SAG CORRECTION

Sag correction provides excellent video performance with two small output coupling capacitors. It eliminates the traditional, large 220µF output capacitor. The traditional 220µF circuit (Figure 7a) creates a single low frequency pole (−3dB frequency) at 5Hz. If this capacitor is made much smaller, excessive phase shift in the critical 50Hz to 100Hz range produces *field tilt* which can interfere with proper recovery of synchronization signals in the television receiver.

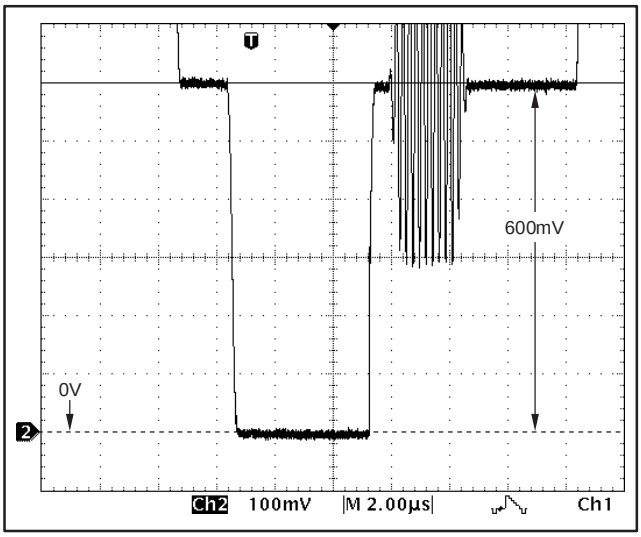


Figure 6. OPA358 Output Swing with Input Sync Level at 0V

The OPA358 with sag correction (Figure 7b) creates an amplitude response peak in the 20Hz region. This small amount of peaking (a few tenths of a dB) provides compensation of the phase response in the critical 50Hz to 100Hz range, greatly reducing field tilt. Note that two significantly smaller and lower-cost capacitors are required.

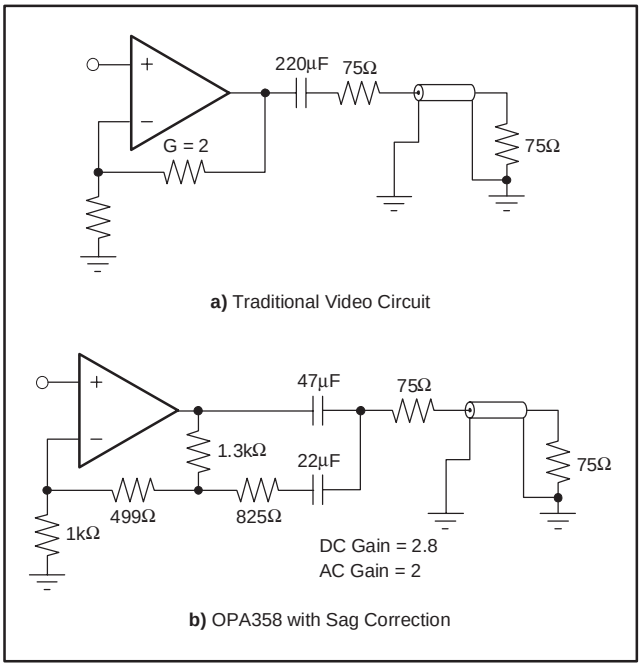


Figure 7. Traditional Video Circuit vs OPA358 with Sag Correction

The output voltage swing for the circuit with sag correction (see Figure 7b) is a function of the coupling capacitor value. The value of the sag correction capacitor has only a minor influence. The smaller the coupling capacitor, the greater the output swing. Therefore, to accommodate the large signal swing with very small coupling capacitors (22µF and 33µF), a higher supply voltage might be needed.

DC-COUPLED OUTPUT

Due to the excellent swing to ground, the OPA358 can also be DC- coupled to a video load. As shown in Figure 8, this eliminates the need for AC-coupling capacitors at the output. This is especially important in portable video applications where board space is restricted.

The DC-coupled output configuration also shows the best video performance. There is no line or field tilt—allowing use of the lowest power supply. In this mode, the OPA358 will safely operate down to 2.5V with no clipping of the signal.

The disadvantage with DC-coupled output is that it uses somewhat higher supply current.

WIDEBAND VIDEO MULTIPLEXING

One common application for video amplifiers which include an enable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple *Wired-OR Video Multiplexer* can be easily implemented using the OPA358, as shown in Figure 9.

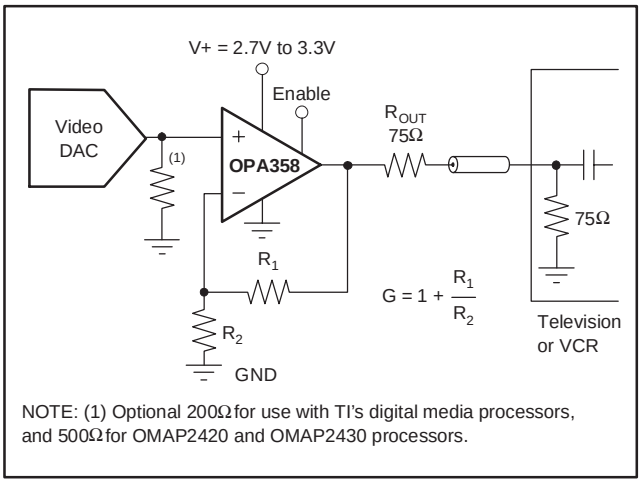


Figure 8. DC-Coupled Input/DC-Coupled Output

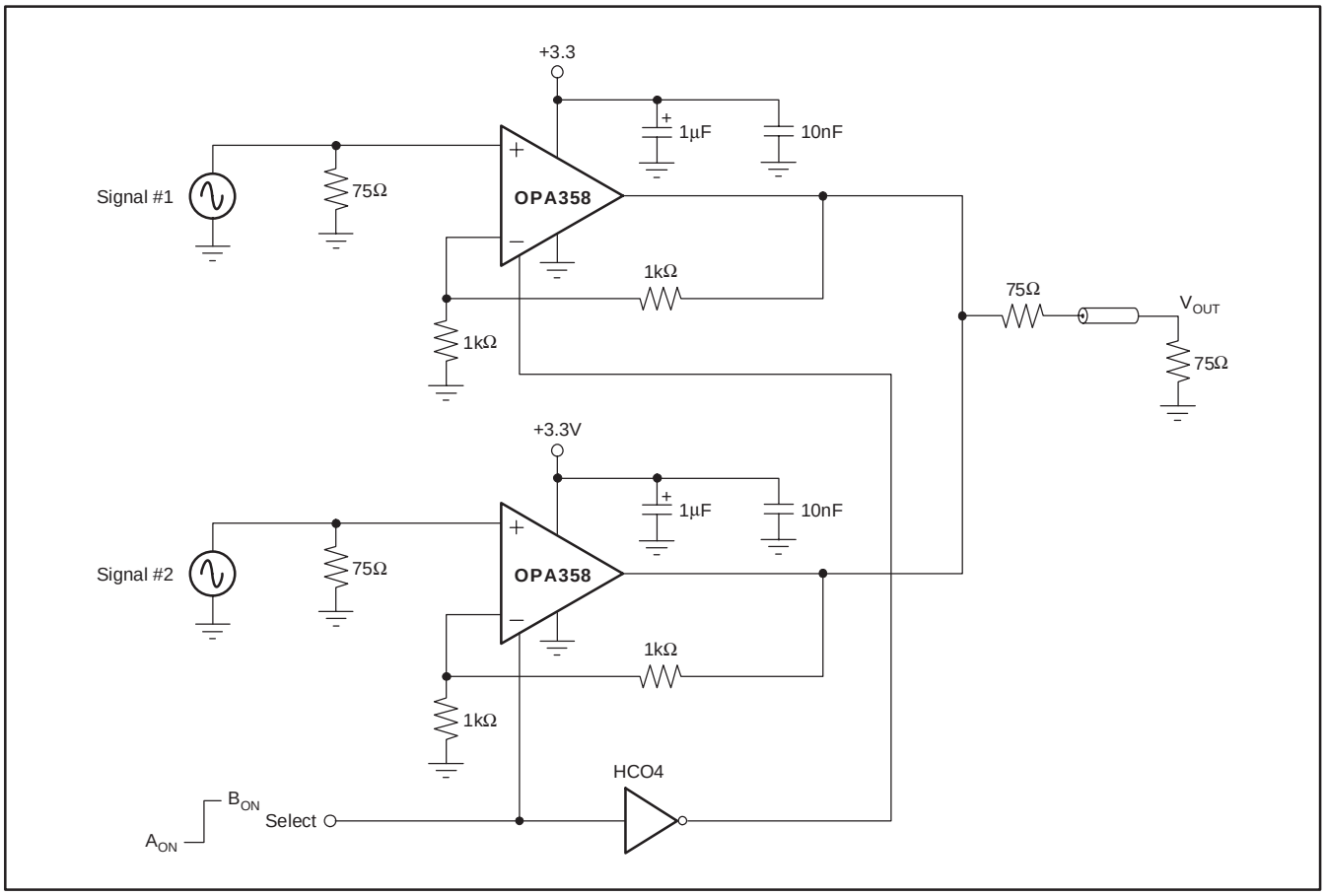


Figure 9. Multiplexed Output

CAPACITIVE LOAD AND STABILITY

The OPA358 can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor in series with the output, as shown in Figure 10. This significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10kΩ and R_S = 20Ω, there is only about a 0.2% error at the output.

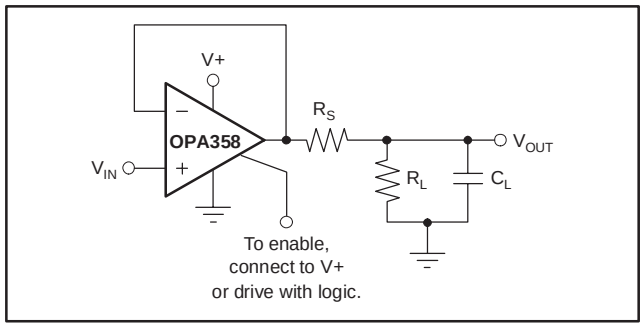


Figure 10. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

WIDEBAND TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA358 an ideal wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 11, are the expected diode capacitance (including the parasitic input common-mode and differential-mode input capacitance (1.5 + 1.5)pF for the OPA358), the desired transimpedance gain (R_F), and the Gain Bandwidth Product (GBW) for the OPA358 (80MHz). With these 3 variables set, the feedback capacitor value (C_F) may be set to control the frequency response.

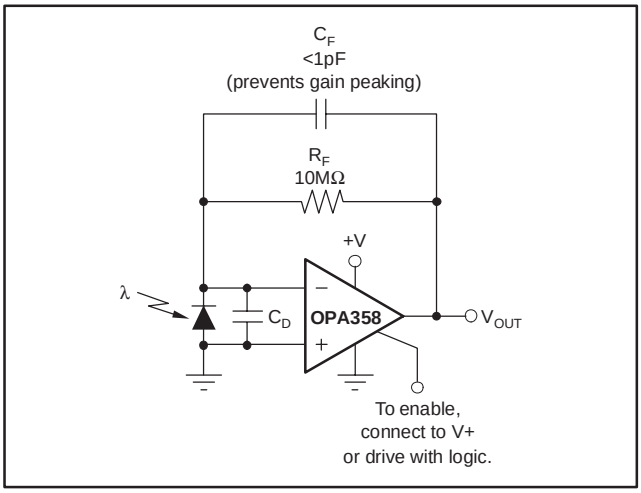


Figure 11. Transimpedance Amplifier

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of around 0.2pF that must be deducted from the calculated feedback capacitance value.

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the CMOS OPA380 (90MHz GBW), OPA355 (200MHz GBW), or the OPA655 (400MHz GBW) may be used.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA358AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AUS	Samples
OPA358AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AUS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

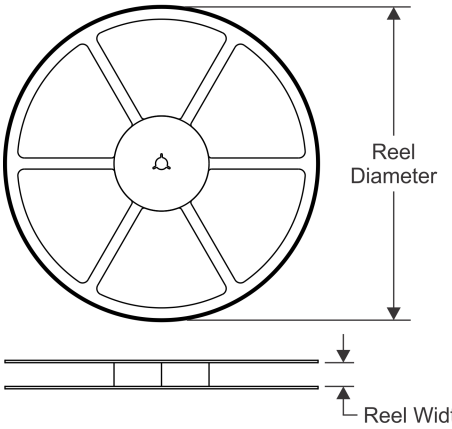
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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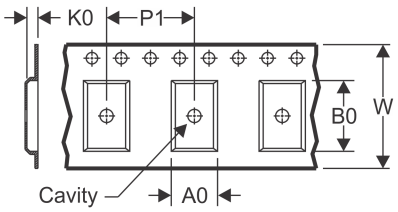
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

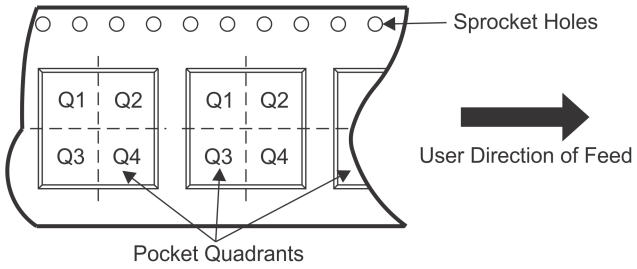


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

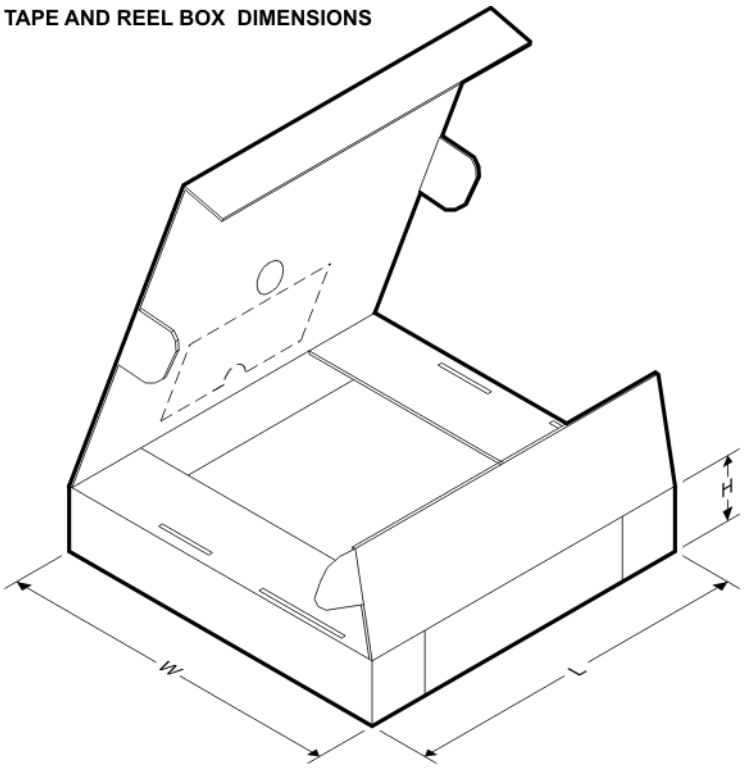
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA358AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA358AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA358AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

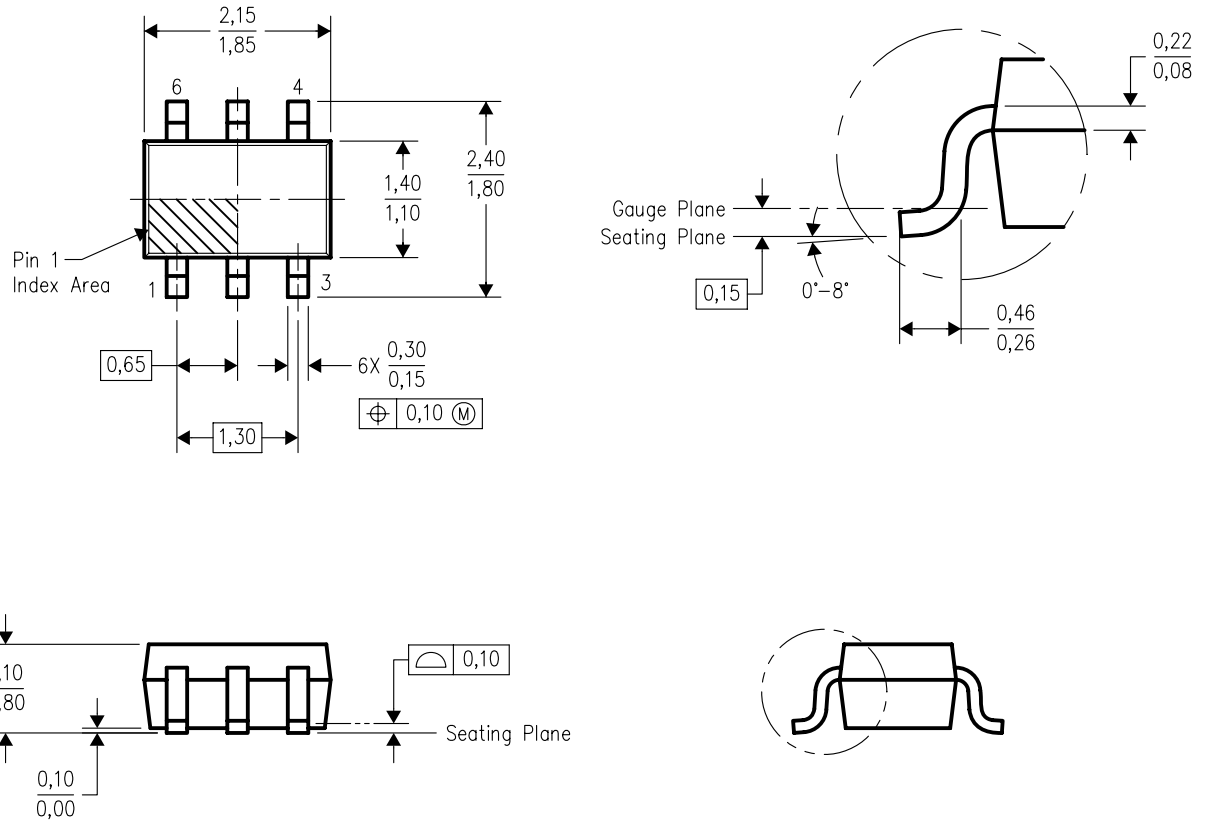
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA358AIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
OPA358AIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
OPA358AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0

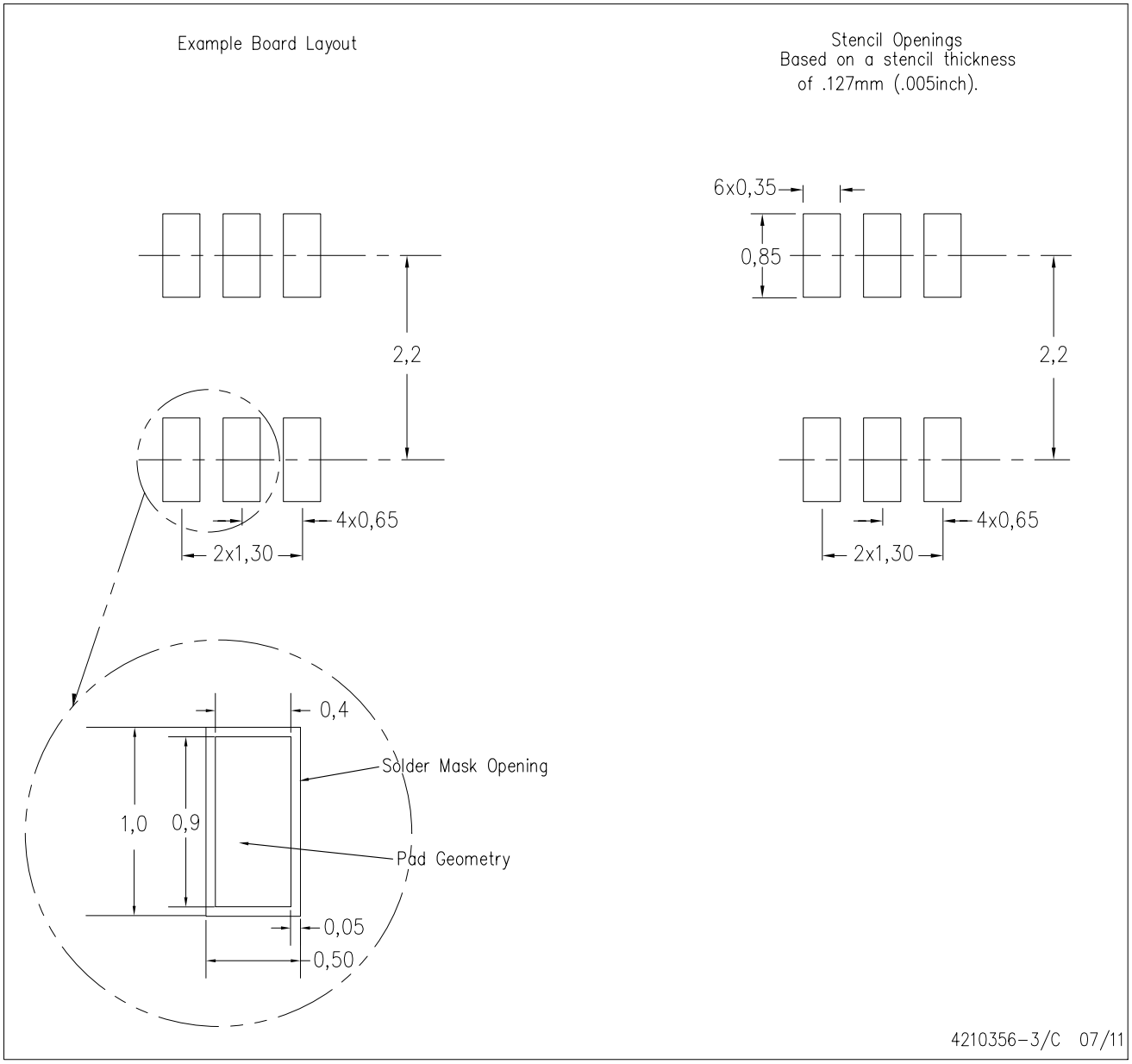
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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