

## 模拟输出电流分流和电压 即时功率监控器

 查询样品: **INA223**

### 特性

- 宽共模范围: **0V 至 26V**
- **$\pm 100\mu\text{V}$**  偏移 (最大, 增益 = **300 V/V**)
- 准确度
  - **$\pm 0.25\%$**  分流电压增益错误 (最大值)
  - **$\pm 0.15\%$**  总线电压增益错误 (最大值)
  - **1.25%** 功率错误 (最大值)
  - **$0.3\mu\text{V}/^\circ\text{C}$**  偏移漂移 (最大值)
  - **50 ppm/ $^\circ\text{C}$**  增益漂移 (最大值)
- 可编辑增益
  - 电流分流电压增益: **20, 128, 300**
  - 总线电压衰减: **1/10, 1/5, 2/5**
- 监控/测量/报告:
  - 即时功率
  - 总线电压
  - 负载电流间的关系
- 瞬态电流: **250 $\mu\text{A}$**  (最大值)
- 关断电流: **1 $\mu\text{A}$**  (最大值)

### 应用范围

- 笔记本电脑
- 手机
- 电信设备
- 电源管理

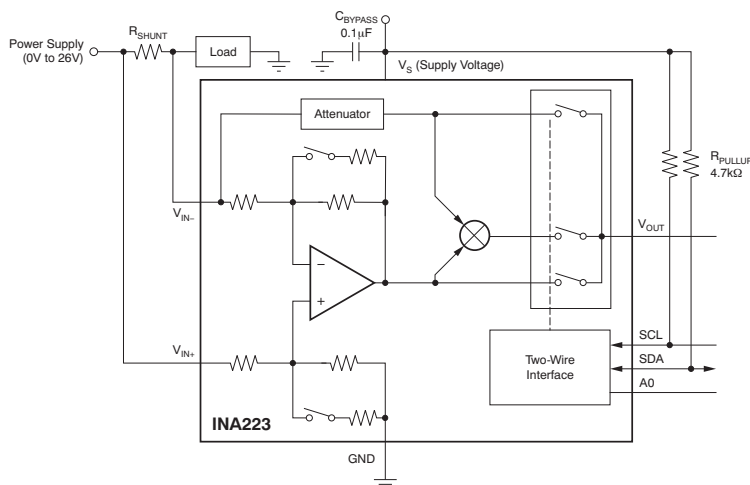
### 说明

INA223 是一款电压输出器件, 通过感测 0V 至 26V 的共模电压上分流的压降, 此器件监控电流、总线电压、和电源线的功率。共模电压范围与电源电压无关。零漂移架构的低偏移在整个分流中使得电流感测的最大压降低至 10mV 的量程。

INA223 包括一个用于调整此器件配置设置的两线制接口。此接口用于控制指向器件输出的信号 (电流分流电压、总线电压、或者功率)。多个增益和衰减设置可通过两线制进行设定以实现应用专用配置。可编辑增益特性也使得此器件可在更宽泛的动态电流负载范围内运行而无需切换到使用的感测元件。

提供了一个关断特性来禁用此器件并高效地从并联电阻器和电源电压上断开, 从而减少了对电池的消耗。

INA223 由单一 +2.7V 至 +5.5V 电源供电运行, 消耗的最大电源电流为 250 $\mu\text{A}$ 。此器件额定扩展温度范围介于  $-40^\circ\text{C}$  至  $+105^\circ\text{C}$  之间并采用小外形尺寸无引线 (SON)-10 封装。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TransZorb is a trademark of General Instruments, Inc.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE INFORMATION<sup>(1)</sup>

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---------|--------------|--------------------|-----------------|
| INA223  | SON-10       | DSK                | P223            |

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

|  |  | INA223             | UNIT |
|--|--|--------------------|------|
| Supply voltage   |  | +6                 | V    |
| Analog inputs,<br>$V_{IN+}$ , $V_{IN-}$ <sup>(2)</sup> | Differential ( $V_{IN+}$ ) – ( $V_{IN-}$ ) | –26 to +26         | V    |
|  | Common-mode <sup>(3)</sup>                 | (GND – 0.3) to +26 | V    |
| Input current into any pin <sup>(3)</sup>              |  | 5                  | mA   |
| Operating temperature                                  |  | –55 to +150        | °C   |
| Storage temperature                                    |  | –65 to +150        | °C   |
| Junction temperature                                   |  | +150               | °C   |
| Electrostatic<br>discharge<br>(ESD) ratings            | Human body model (HBM)                     | 2500               | V    |
|  | Charged-device model (CDM)                 | 1000               | V    |
|  | Machine model (MM)                         | 200                | V    |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2)  $V_{IN+}$  and  $V_{IN-}$  are the voltages at the +IN and –IN pins, respectively.
- (3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

**ELECTRICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SENSE}} = (V_{\text{IN}+}) - (V_{\text{IN}-}) = 10\text{ mV}$ ,  $V_S = 3.3\text{ V}$ , and  $V_{\text{IN}+} = 12\text{ V}$ , unless otherwise noted.

| PARAMETER           |  | TEST CONDITIONS   | INA223        |               |              | UNIT                         |
|---------------------|--|---|---------------|---------------|--------------|------------------------------|
|                     |  |   | MIN           | TYP           | MAX          |                              |
| <b>INPUT</b>        |  |   |               |               |              |                              |
| $V_{\text{CM}}$     | Common-mode input range                  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$   | 0             |               | 26           | V                            |
| CMR                 | Common-mode rejection                    | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{\text{IN}+} = 0\text{ V}$ to $+26\text{ V}$ ,<br>$V_{\text{SENSE}} = 0\text{ mV}$ , Current shunt voltage gain = 20 V/V             | 92            | 106           |              | dB                           |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{\text{IN}+} = 0\text{ V}$ to $+26\text{ V}$ ,<br>$V_{\text{SENSE}} = 0\text{ mV}$ , Current shunt voltage gain = 128 V/V,<br>300V/V | 100           | 120           |              | dB                           |
| $V_{\text{OS}}$     | Shunt offset voltage, RTI <sup>(1)</sup> | Current shunt voltage gain = 20 V/V   |               | $\pm 75$      | $\pm 300$    | $\mu\text{V}$                |
|                     |  | Current shunt voltage gain = 128 V/V  |               | $\pm 20$      | $\pm 150$    | $\mu\text{V}$                |
|                     |  | Current shunt voltage gain = 300 V/V  |               | $\pm 15$      | $\pm 100$    | $\mu\text{V}$                |
| $dV_{\text{OS}}/dT$ | vs temperature                           | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , current shunt voltage gain = 20 V/V   |               | 0.6           | 1            | $\mu\text{V}/^\circ\text{C}$ |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , current shunt voltage gain = 128 V/V,<br>300V/V   |               | 0.1           | 0.3          |                              |
| PSR                 | vs power supply                          | $V_S = +2.7\text{ V}$ to $+5.5\text{ V}$ , current shunt voltage gain = 20 V/V  |               | $\pm 15$      | $\pm 50$     | $\mu\text{V}/\text{V}$       |
|                     |  | $V_S = +2.7\text{ V}$ to $+5.5\text{ V}$ , current shunt voltage gain = 128 V/V   |               | $\pm 5$       | $\pm 25$     | $\mu\text{V}/\text{V}$       |
|                     |  | $V_S = +2.7\text{ V}$ to $+5.5\text{ V}$ , current shunt voltage gain = 300 V/V   |               | $\pm 2.5$     | $\pm 15$     | $\mu\text{V}/\text{V}$       |
| $V_{\text{OS}}$     | Bus offset voltage, RTI <sup>(1)</sup>   | Bus voltage gain = 0.1 V/V  |               | $\pm 2.5$     | $\pm 20$     | mV                           |
|                     |  | Bus voltage gain = 0.2 V/V  |               | $\pm 2.5$     | $\pm 15$     | mV                           |
|                     |  | Bus voltage gain = 0.4 V/V  |               | $\pm 1.5$     | $\pm 10$     | mV                           |
| $dV_{\text{OS}}/dT$ | vs temperature                           | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , bus voltage gain = 0.1 V/V  |               | 15            | 40           | $\mu\text{V}/^\circ\text{C}$ |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , bus voltage gain = 0.2 V/V, 0.4 V/V   |               | 10            | 30           | $\mu\text{V}/^\circ\text{C}$ |
| PSR                 | vs power supply                          | $V_S = +2.7\text{ V}$ to $+5.5\text{ V}$  |               | $\pm 9$       | $\pm 15$     | mV/V                         |
| $I_B$               | Input bias current                       | Enabled, $V_{\text{IN}+}$ , $V_{\text{IN}-}$  | 15            | 18            | 25           | $\mu\text{A}$                |
|                     |  | Disabled, $V_{\text{IN}+}$ , $V_{\text{IN}-}$   |               | 1             | 1.5          | $\mu\text{A}$                |
|                     | Input impedance, differential            |   |               | 2.5           |              | k $\Omega$                   |
| <b>OUTPUT</b>       |  |   |               |               |              |                              |
| $G_{\text{SV}}$     | Current shunt voltage gain               |   | 20, 128, 300  |               |              | V/V                          |
|                     | Current shunt voltage gain error         | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{\text{SENSE}} = 10\text{ mV}$ to $155\text{ mV}$ , current shunt voltage gain = 20 V/V  |               | $\pm 0.05\%$  | $\pm 0.25\%$ |                              |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{\text{SENSE}} = 1.5\text{ mV}$ to $24\text{ mV}$ , current shunt voltage gain = 128 V/V   |               | $\pm 0.05\%$  | $\pm 0.5\%$  |                              |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $V_{\text{SENSE}} = 1\text{ mV}$ to $9\text{ mV}$ , current shunt voltage gain = 300 V/V  |               | $\pm 0.2\%$   | $\pm 1\%$    |                              |
|                     | vs temperature                           | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , current shunt voltage gain = 20 V/V   |               |               | 50           | ppm/ $^\circ\text{C}$        |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , current shunt voltage gain = 128 V/V  |               |               | 75           | ppm/ $^\circ\text{C}$        |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , current shunt voltage gain = 300 V/V  |               |               | 125          | ppm/ $^\circ\text{C}$        |
|                     | Nonlinearity error                       | $V_{\text{SENSE}} = 1\text{ mV}$ to $10\text{ mV}$  |               | $\pm 0.01\%$  |              |                              |
| $G_{\text{BV}}$     | Bus voltage gain                         |   | 0.1, 0.2, 0.4 |               |              | V/V                          |
|                     | Bus voltage gain error                   | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , bus voltage gain = 0.1 V/V,<br>$V_{\text{CM}} = 0.5\text{ V}$ to $26\text{ V}$  |               | $\pm 0.05\%$  | $\pm 0.2\%$  |                              |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , bus voltage gain = 0.2 V/V,<br>$V_{\text{CM}} = 0.5\text{ V}$ to $12\text{ V}$  |               | $\pm 0.025\%$ | $\pm 0.15\%$ |                              |
|                     |  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , bus voltage gain = 0.4V/V,<br>$V_{\text{CM}} = 0.5\text{ V}$ to $6\text{ V}$  |               | $\pm 0.025\%$ | $\pm 0.15\%$ |                              |
|                     | vs temperature                           | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$   |               |               | 5            | ppm/ $^\circ\text{C}$        |
|                     | Nonlinearity error                       |   |               | $\pm 0.01\%$  |              |                              |

(1) RTI = referred-to-input.

## ELECTRICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SENSE}} = (V_{\text{IN}+}) - (V_{\text{IN}-}) = 10\text{ mV}$ ,  $V_S = 3.3\text{ V}$ , and  $V_{\text{IN}+} = 12\text{ V}$ , unless otherwise noted.

| PARAMETER                                     | TEST CONDITIONS   | INA223                                       |                        |                       | UNIT                   |
|---|---|--|------------------------|-----------------------|------------------------|
|   |   | MIN  | TYP                    | MAX                   |                        |
| Power measurement error                       | Current shunt voltage gain = 20 V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V   |  | ±0.35                  | ±1.25                 | %FSR                   |
|   | Current shunt voltage gain = 20 V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$           |  |                        | ±2                    | %FSR                   |
|   | Current shunt voltage gain = 128 V/V, 300V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V  |  | ±0.35                  | ±1.5                  | %FSR                   |
|   | Current shunt voltage gain = 128 V/V, 300V/V; bus voltage gain = 0.1 V/V, 0.2V/V, 0.4V/V; $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ |  |                        | ±2.25                 | %FSR                   |
| Output impedance                              |   |  | 4                      |                       | $\Omega$               |
| Maximum capacitive load                       | No sustained oscillation  |  | 1                      |                       | nF                     |
| <b>VOLTAGE OUTPUT<sup>(2)</sup></b>           |   |  |                        |                       |                        |
| Swing to VS power-supply rail                 | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $R_L = 10\text{ k}\Omega$ to GND  |  | $V_S - 0.015$          | $V_S - 0.035$         | V                      |
| Swing to GND                                  | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ , $R_L = 10\text{ k}\Omega$ to GND  |  | $V_{\text{GND}} + 2.5$ | $V_{\text{GND}} + 10$ | mV                     |
| <b>FREQUENCY RESPONSE</b>                     |   |  |                        |                       |                        |
| GBW   | Bandwidth   | Gain = 300, $C_{\text{LOAD}} = 10\text{ pF}$ |                        | 10                    | kHz                    |
|   |   | Gain = 128, $C_{\text{LOAD}} = 10\text{ pF}$ |                        | 20                    | kHz                    |
|   |   | Gain = 20, $C_{\text{LOAD}} = 10\text{ pF}$  |                        | 25                    | kHz                    |
| SR  | Slew rate   |  | 0.25                   |                       | V/ $\mu\text{s}$       |
| <b>NOISE, RTI<sup>(1)</sup></b>               |   |  |                        |                       |                        |
| Voltage noise density                         | 0.1 Hz to 10 Hz, current shunt voltage gain = 20 V/V  |  | 235                    |                       | nV/ $\sqrt{\text{Hz}}$ |
|   | 0.1 Hz to 10 Hz, current shunt voltage gain = 300 V/V   |  | 54                     |                       | nV/ $\sqrt{\text{Hz}}$ |
| <b>DIGITAL INPUTS (SDA as Input, SCL, A0)</b> |   |  |                        |                       |                        |
|   | Input capacitance   |  | 3                      |                       | pF                     |
| $V_{\text{IH}}$                               | High-level input voltage  |  | $0.7(V_S)$             | 6                     | V                      |
| $V_{\text{IL}}$                               | Low-level input voltage   |  | -0.3                   | $0.3(V_S)$            | V                      |
|   | Leakage input current   |  | 0.1                    | 1                     | $\mu\text{A}$          |
|   | Hysteresis  |  | 500                    |                       | mV                     |

(2) See Typical Characteristic curve, *Output Swing vs Output Current* (Figure 22).

**ELECTRICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SENSE}} = (V_{\text{IN}+}) - (V_{\text{IN}-}) = 10\text{ mV}$ ,  $V_S = 3.3\text{ V}$ , and  $V_{\text{IN}+} = 12\text{ V}$ , unless otherwise noted.

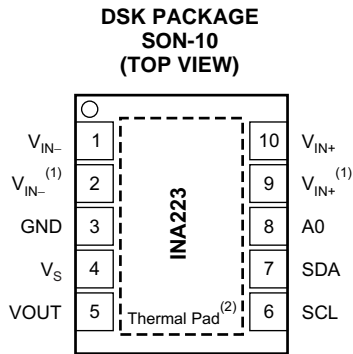
| PARAMETER           | TEST CONDITIONS          | INA223  |     |      | UNIT             |
|---------------------|--------------------------|---|-----|------|------------------|
|                     |                          | MIN   | TYP | MAX  |                  |
| <b>POWER SUPPLY</b> |                          |   |     |      |                  |
| $V_S$               | Operating range          | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ |     |      | V                |
| $I_Q$               | Quiescent current        | Enabled   | 200 | 250  | $\mu\text{A}$    |
|                     |                          | Disabled  | 0.1 | 1    | $\mu\text{A}$    |
|                     | Power-on reset threshold | 2   |     |      | V                |
| <b>TEMPERATURE</b>  |                          |   |     |      |                  |
|                     | Specified range          | -40   |     | +105 | $^\circ\text{C}$ |

**THERMAL INFORMATION**

| THERMAL METRIC <sup>(1)</sup> |  | INA223    | UNITS                     |
|-------------------------------|--|-----------|---------------------------|
|                               |  | DSK (SON) |                           |
|                               |  | 10 PINS   |                           |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 47.5      | $^\circ\text{C}/\text{W}$ |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance    | 57.9      |                           |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 21.5      |                           |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 0.8       |                           |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 21.8      |                           |
| $\theta_{JCbott}$             | Junction-to-case (bottom) thermal resistance | 4.6       |                           |

(1) 有关传统和全新热度的更多信息，请参阅 *IC 封装热度量* 应用报告 (文献号：SPRA953)。

### PIN CONFIGURATIONS



- (1) See [Application Information](#) section for a description of how to connect input pins to the shunt resistor.
- (2) Must be connected to ground.

### PIN DESCRIPTIONS

| PIN  |        | ANALOG/DIGITAL<br>INPUT/OUTPUT | DESCRIPTION   |
|------|--------|--------------------------------|---|
| NAME | NUMBER |                                |   |
| A0   | 8      | Digital input                  | Address pin. Connect to GND, SCL, SDA, or VS. <a href="#">Table 6</a> shows pin settings and corresponding address. |
| GND  | 3      | Analog                         | Ground  |
| SCL  | 6      | Digital input                  | Serial bus clock line   |
| SDA  | 7      | Digital I/O                    | Serial bus data line  |
| VIN+ | 9      | Analog input                   | Connect to supply side of shunt resistor. This pin can also be connected directly to pin 10.                        |
| VIN+ | 10     | Analog input                   | Connect to supply side of shunt resistor  |
| VIN- | 1      | Analog input                   | Connect to load side of shunt resistor  |
| VIN- | 2      | Analog input                   | Connect to load side of shunt resistor. This pin can also be connected directly to pin 1.                           |
| VOUT | 5      | Analog output                  | Output signal selected by multiplexer   |
| VS   | 4      | Analog                         | Power supply (2.7 V to 5.5 V)   |

**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +3.3\text{ V}$ ,  $V_{IN+} = 12\text{ V}$  unless otherwise noted.

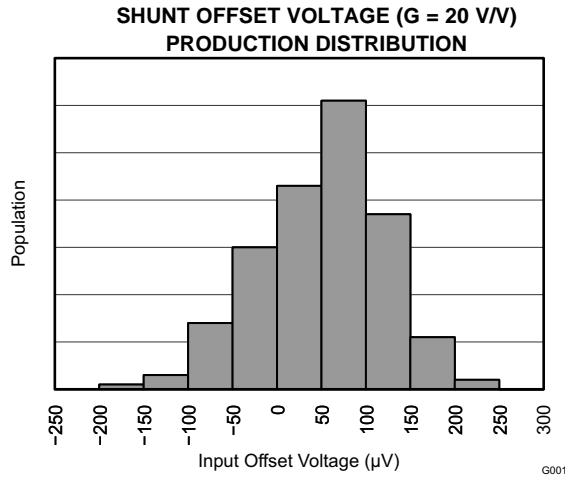


Figure 1.

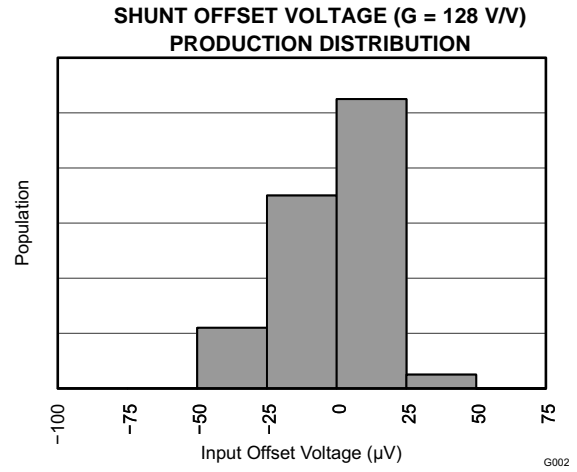


Figure 2.

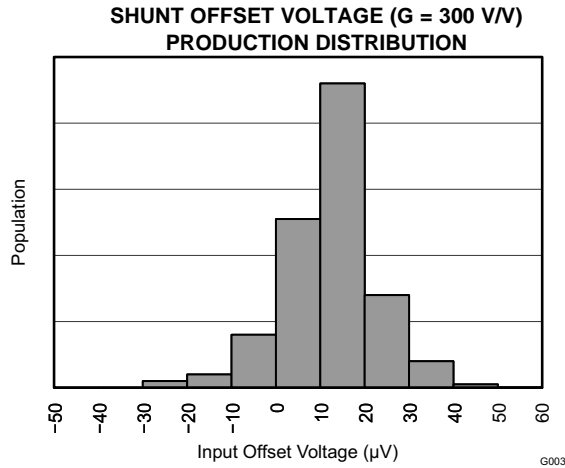


Figure 3.

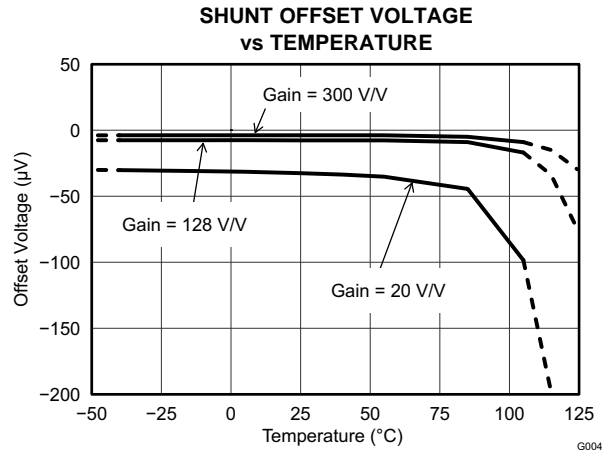


Figure 4.

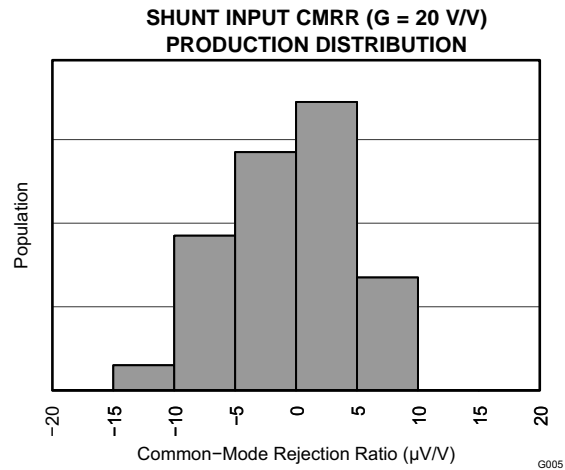


Figure 5.

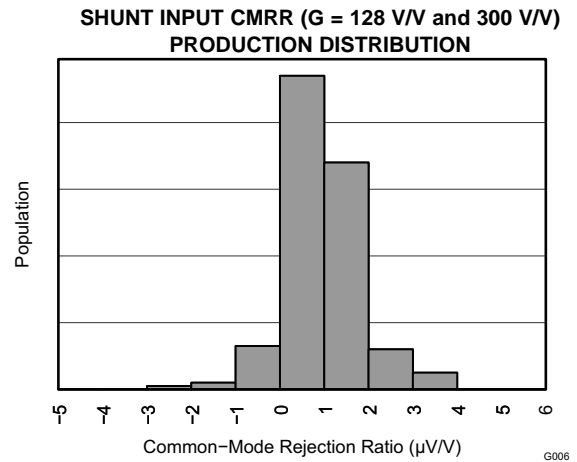


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +3.3\text{ V}$ ,  $V_{IN+} = 12\text{ V}$  unless otherwise noted.

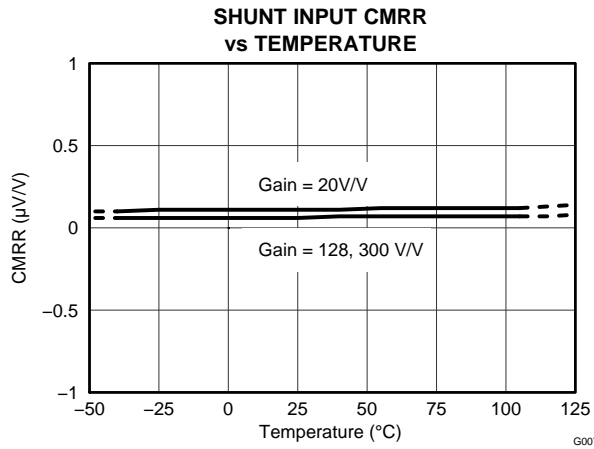


Figure 7.

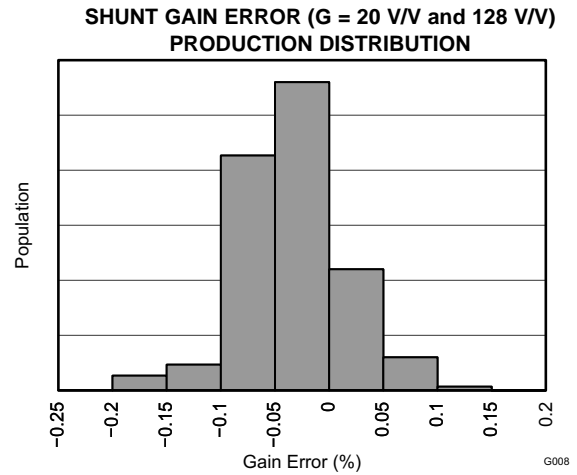


Figure 8.

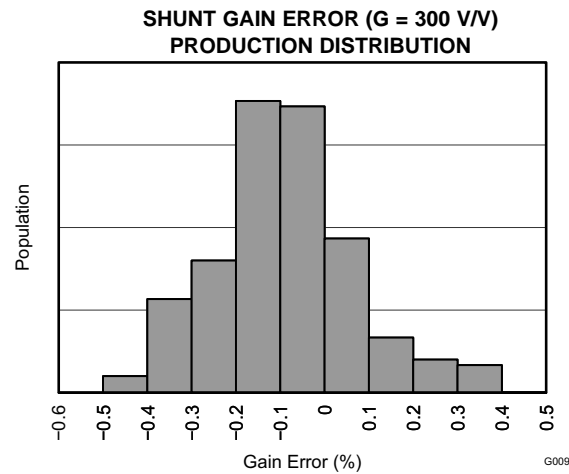


Figure 9.

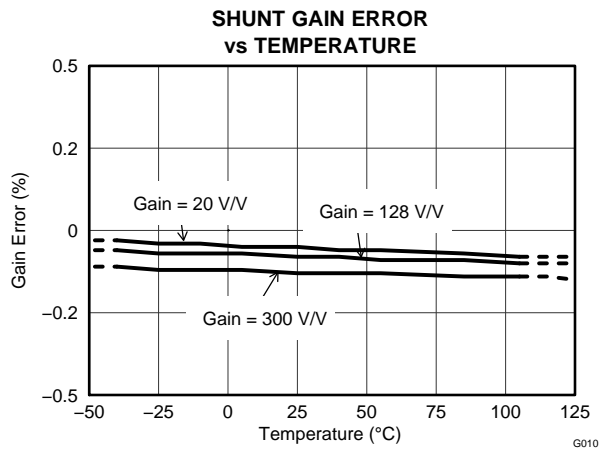


Figure 10.

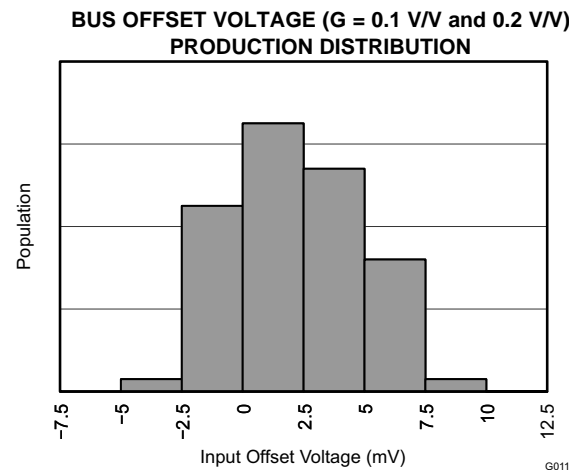


Figure 11.

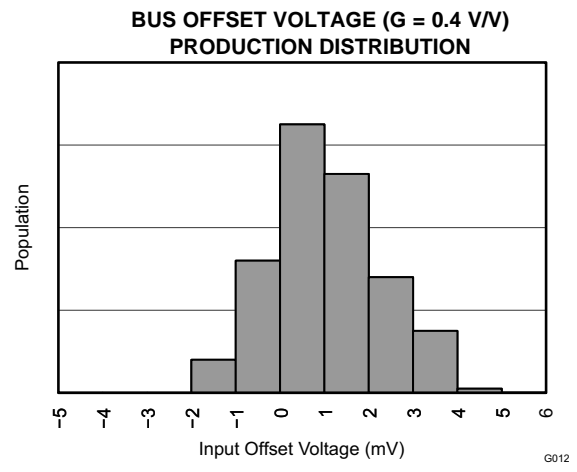


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +3.3\text{ V}$ ,  $V_{IN+} = 12\text{ V}$  unless otherwise noted.

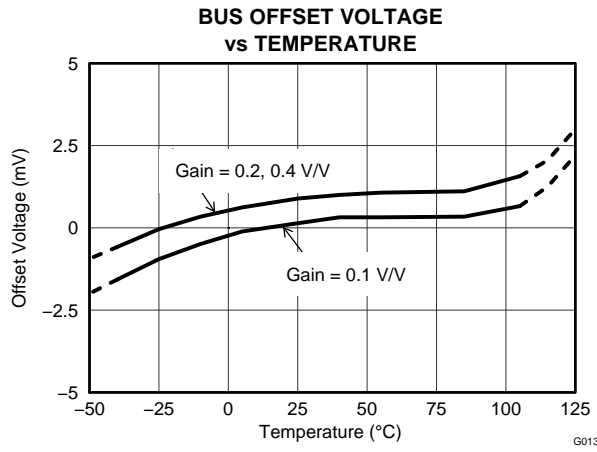


Figure 13.

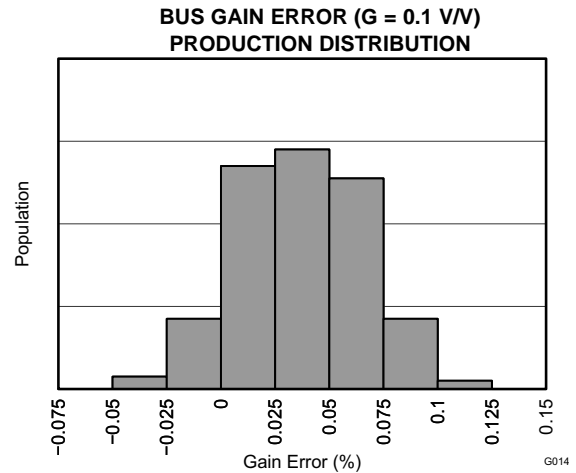


Figure 14.

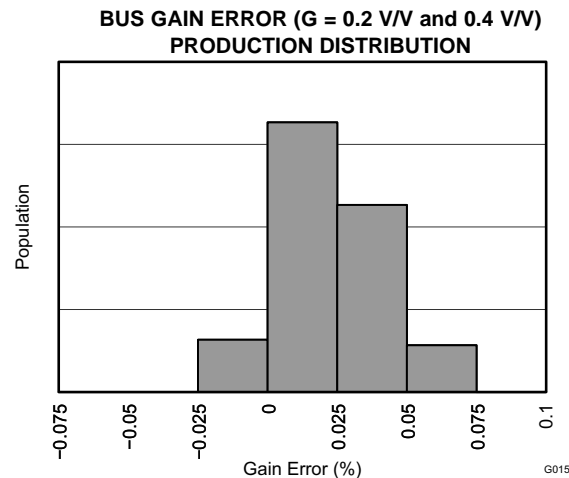


Figure 15.

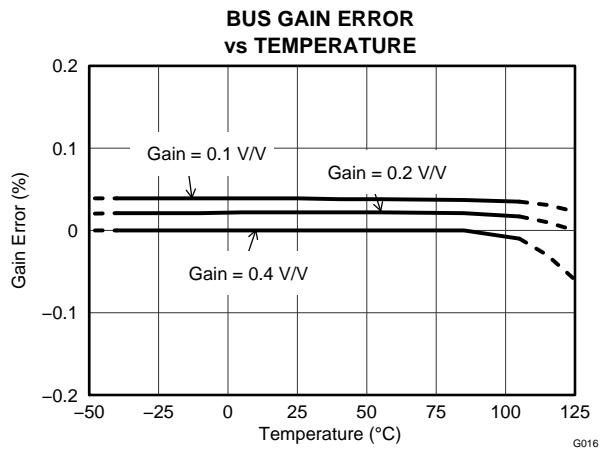


Figure 16.

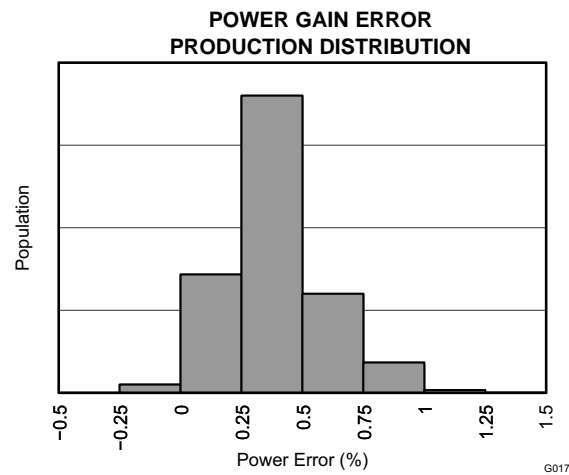


Figure 17.

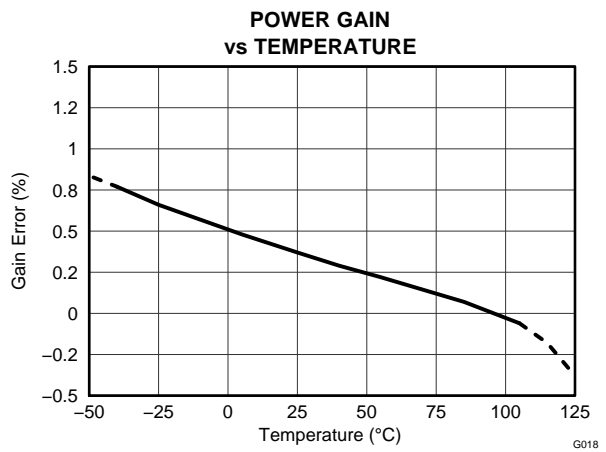


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +3.3\text{ V}$ ,  $V_{IN+} = 12\text{ V}$  unless otherwise noted.

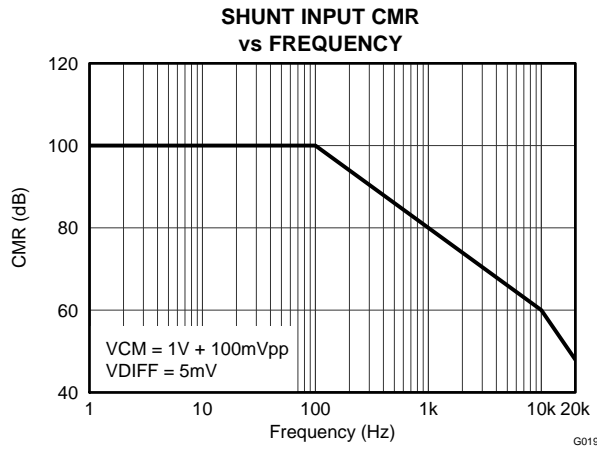


Figure 19.

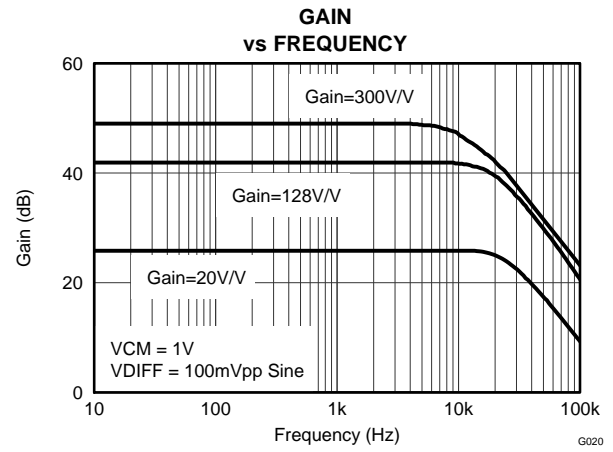


Figure 20.

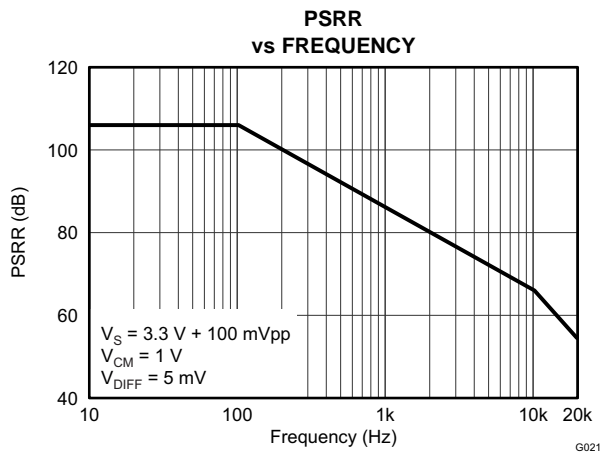


Figure 21.

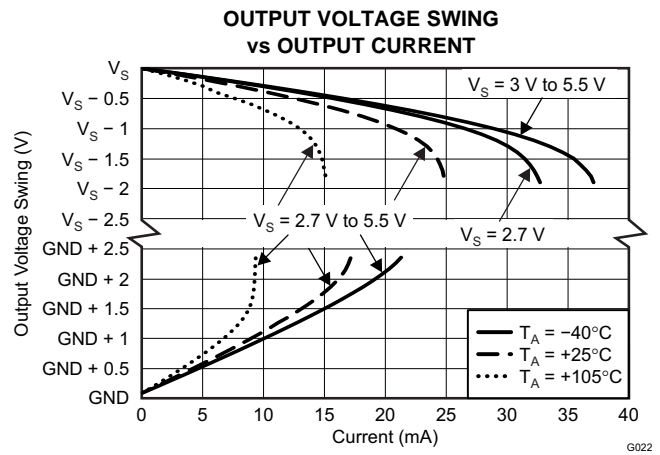


Figure 22.

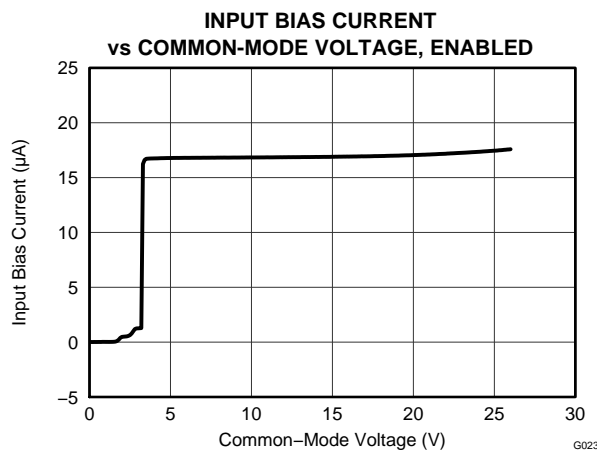


Figure 23.

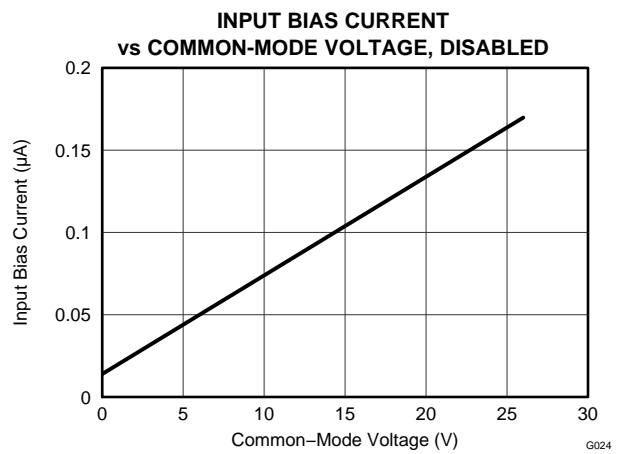
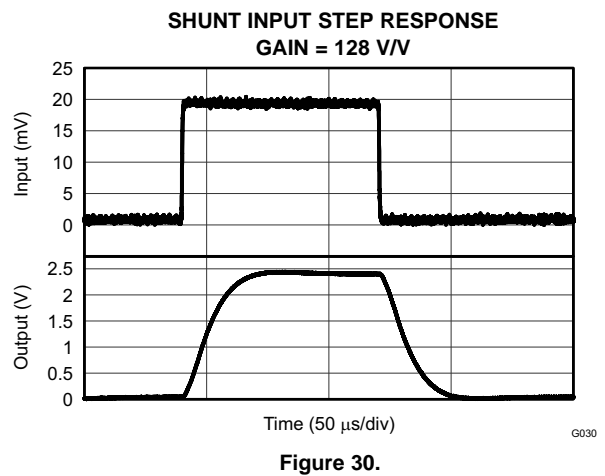
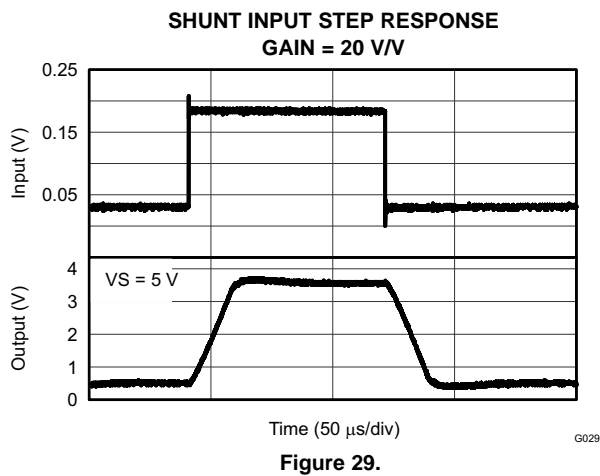
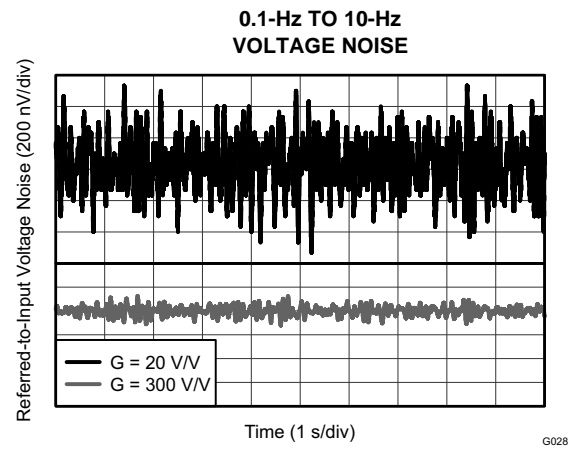
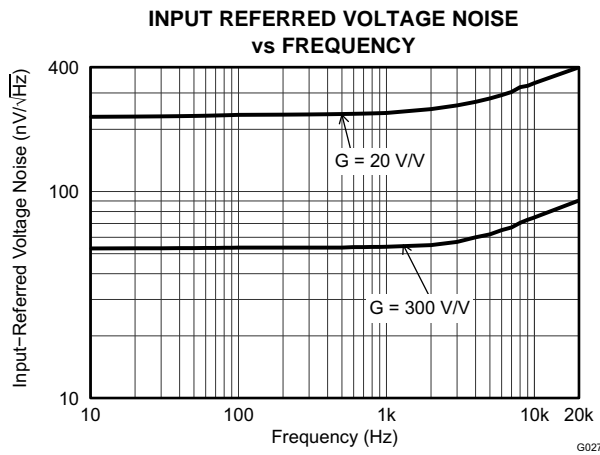
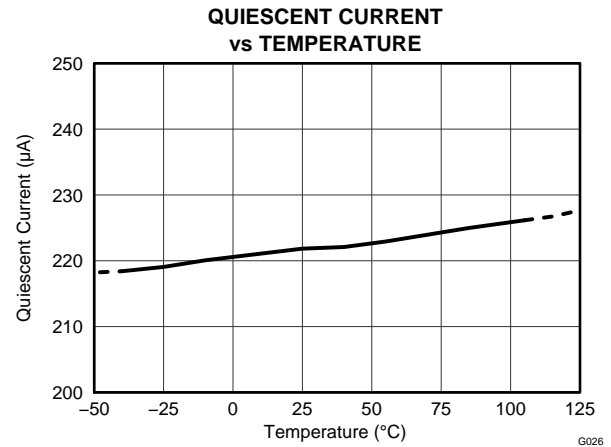
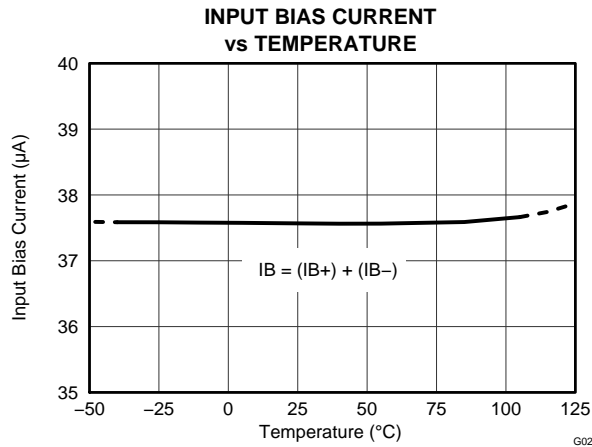


Figure 24.

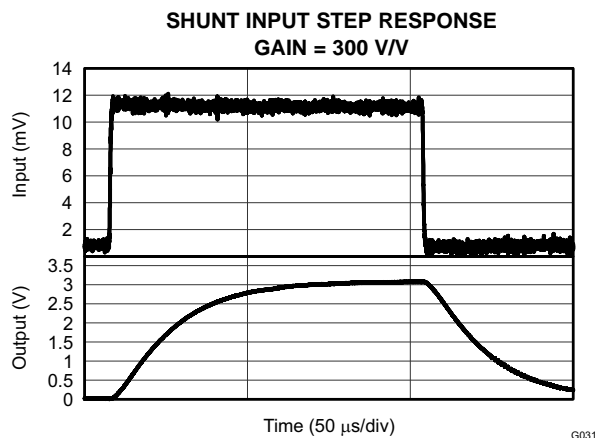
**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +3.3\text{ V}$ ,  $V_{IN+} = 12\text{ V}$  unless otherwise noted.

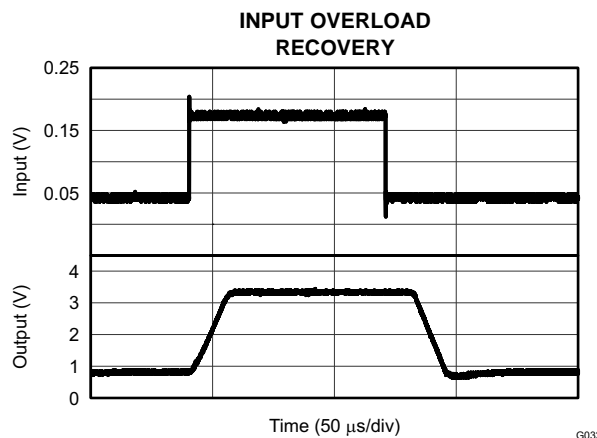


**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +3.3\text{ V}$ ,  $V_{IN+} = 12\text{ V}$  unless otherwise noted.



**Figure 31.**



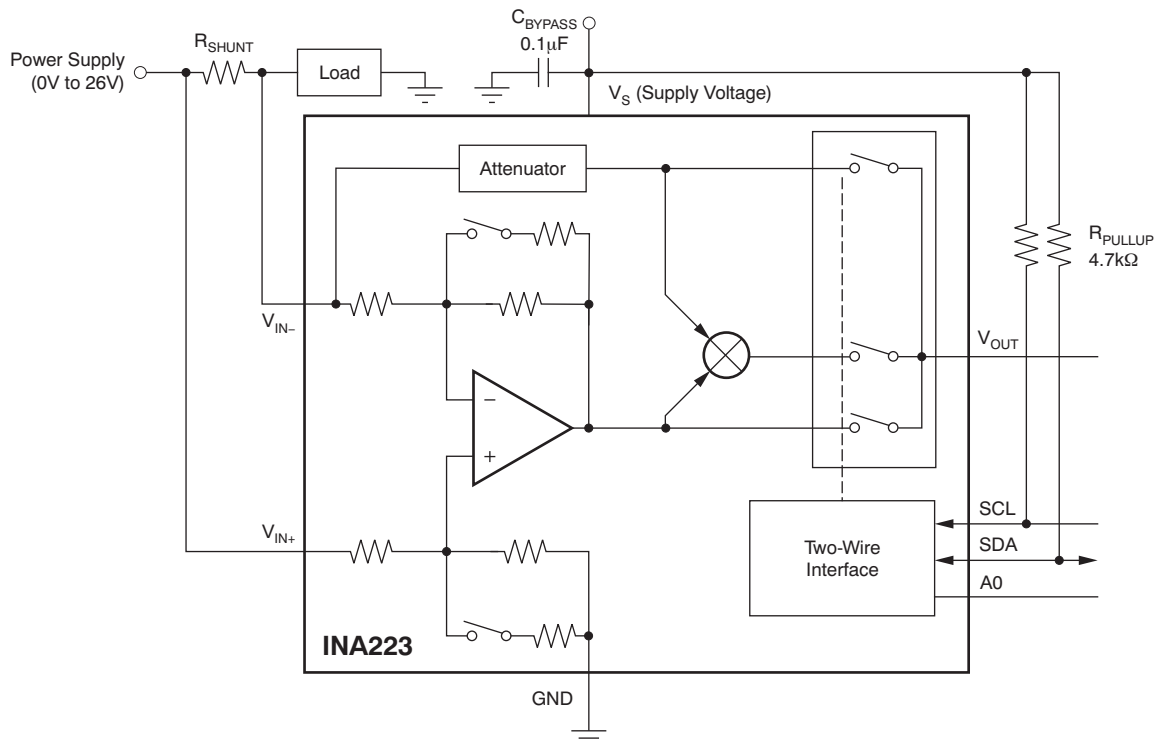
**Figure 32.**

## APPLICATION INFORMATION

The INA223 is an analog output current shunt monitor that incorporates an analog multiplier to provide instantaneous power measurement. The INA223 features a two-wire and SMBus-compatible interface allowing the configuration settings of the device to be adjusted and changed as needed, based on the specific application requirements. The configuration options include the selection of the desired signal to be available at the output pin, switching between multiple current shunt voltage gains and bus voltage attenuation factors, as well as being able to place the device into a disabled state.

### INA223 TYPICAL APPLICATION

Figure 33 shows the typical application circuit for the INA223. The input pins,  $V_{IN+}$  and  $V_{IN-}$ , should be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance. A power-supply bypass capacitor is required for stability. Use a 0.1- $\mu\text{F}$  ceramic capacitor for supply bypassing, placed as close as possible between the supply and ground pins.



**Figure 33. Typical Application**

### BASIC FUNCTIONS

The INA223 can be configured to monitor and report the differential voltage developed across a shunt resistor, the power supply bus voltage, or the power being delivered to the load. Through the two-wire interface, the output multiplexer (mux) can be configured to provide a proportional output signal to any one of these input signals at the output pin,  $V_{OUT}$ . The digital interface can also be used to switch between different current shunt voltage gains, bus voltage attenuation settings, as well as place the device into a disabled mode. The multiple settings available for the current shunt voltage gains and bus voltage attenuation factors allow the INA223 to operate over a wider input signal range than a single fixed-setting device would allow.

## Shunt Voltage

The INA223 has three available current shunt voltage gain options that can be selected using the two-wire interface. This allows for optimization of the output signal to maximize the available dynamic range. This flexibility provides a benefit over a fixed-gain current shunt monitor. A fixed-gain current shunt monitor has a finite range of current that can be monitored based on the limitations of the output stage of the device.

For example, in a typical application using a fixed-gain current shunt monitor, the shunt resistor is selected to achieve the maximum allowable full-scale output based on the maximum expected current to be monitored and the fixed gain value of the current shunt monitor. One limitation to a fixed gain approach is in the minimum current level that can be monitored. The minimum current that can be monitored is based on the ability of the output stage of the current shunt monitor to swing to ground. This minimum current level is calculated based on the maximum swing to ground specification (50 mV for the INA223), which is then divided by the fixed gain of the device. This calculation provides the minimum differential voltage that can be monitored and then divided by the shunt resistor to determine the minimum current that can be monitored. After the monitored current drops below this level, further decreases in the monitored current can no longer be detected at the output. The ability to switch the current shunt voltage gain to a higher gain setting brings the output level above this saturation point and enables lower currents to be monitored, thus extending the dynamic range of the device.

## Bus Voltage Range

The INA223 monitors bus voltages that can range from 0 V to 26 V. This voltage must be internally divided down to interface with the analog multiplier and output stage circuitry. The supply voltage for the INA223 can range from 2.7 V to 5.5 V; therefore, the bus voltage must be divided down so that it does not exceed the supply voltage. If this divider ratio or attenuation factor results in an internal voltage that exceeds the supply voltage, the measurement circuitry is saturated. The device will not be damaged, but the measurement result at the output will be invalid. Having multiple attenuation factors (0.1 V/V, 0.2 V/V, 0.4 V/V) allows for the optimization of the output range based on the specific common-mode voltage present. Having multiple values that can be selected provides a helpful advantage over a single fixed-attenuation device, given the wide common-mode range of the INA223. With a single attenuation factor, the maximum common-mode voltage (26 V) must be divided down to less than the minimum supply voltage (2.7 V). A bus voltage less than 26 V results in a significantly smaller output range. The ability to switch between different attenuation settings allows the device to be configured to maximize the dynamic output range at multiple common-mode voltage levels. Additionally, because the power calculation is based on the bus voltage measurement, the larger the corresponding representation of the common-mode voltage, the more accurate the power calculation.

## Output Range

The power calculation has two inputs: the current shunt voltage measurement, as well as the bus voltage measurement. Both of these measurements must be valid (within the linear range of the device) to achieve a valid power calculation. Set the gain setting for the current shunt voltage and attenuation setting for the bus voltage to allow each of these two measurements to remain within the linear range of the device, based on the input conditions. Saturating one of these two measurements may not result in the output being saturated based on the internal scaling of the analog multiplier; therefore, care should be taken to ensure that the two inputs to the multiplier are valid.

## Shutting Down the INA223

The INA223 includes a shutdown feature that is programmed through the serial interface. Setting the Enable bit in the Configuration Register to '0' places the INA223 into a disabled state. While in the disabled state, the input bias currents and device quiescent current drop below 1  $\mu$ A, thus reducing the power consumption of the system when this device is not in use. The device is placed back into the active mode by setting the Enable bit high. The time required for the INA223 output to be valid after enabling the device to come out of the shutdown state is typically 40  $\mu$ s.

In addition to responding to the Enable bit, the INA223 also responds to an Enable and Disable General Call as described in the [GENERAL CALL](#) section.

**CONFIGURATION REGISTER**

| BIT              | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5   | D4   | D3   | D2   | D1   | D0   |
|------------------|-----|-----|-----|-----|-----|-----|----|----|----|----|------|------|------|------|------|------|
| <b>BIT NAME</b>  | —   | —   | —   | —   | —   | —   | —  | —  | —  | EN | OUT1 | OUT0 | GSV1 | GSV0 | GBV1 | GBV0 |
| <b>POR VALUE</b> | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 1  | 1    | 0    | 0    | 0    | 0    | 1    |

**EN Enable/Disable Mode**

Bit 6 Setting this bit to '0' places the device into a disabled mode.

This mode drops the input bias current to 1  $\mu$ A for each of the analog inputs and reduces the quiescent current to 1  $\mu$ A.

**OUT Output Mode**

Bits 4, 5 Controls the setting of the output mux to select the signal that is available at the output pin. There are two different mode settings for selecting power at the output pin. The Supply Power output mode sets the bus voltage measurement to be taken at the  $V_{IN+}$  pin to calculate the power provided by the power supply. The Load Power output mode sets the bus voltage measurement to be taken at the  $V_{IN-}$  pin to calculate the power consumed by the load. Refer to [Table 1](#).

**Table 1. Output Mode Settings<sup>(1)</sup>**

| OUT1 | OUT0 | OUTPUT MODE               |
|------|------|---------------------------|
| D5   | D4   |                           |
| 0    | 0    | Bus Voltage Measurement   |
| 0    | 1    | Shunt Voltage Measurement |
| 1    | 0    | Supply Power              |
| 1    | 1    | Load Power                |

(1) Shaded cells indicate default value.

**GSV Current Shunt Voltage Gain**

Bits 2, 3 Sets the gain for the current shunt voltage measurement. [Table 2](#) summarizes the gain settings.

**Table 2. Current Shunt Voltage Gain Settings<sup>(1)</sup>**

| GSV1 | GSV0 | CURRENT SHUNT VOLTAGE GAIN |
|------|------|----------------------------|
| D3   | D2   |                            |
| 0    | 0    | 20 V/V                     |
| 0    | 1    | 128 V/V                    |
| 1    | 0    | 300 V/V                    |

(1) Shaded cells indicate default value.

**GBV Bus Voltage Gain**

Bits 0, 1 Sets the gain for the bus voltage measurement. Refer to [Table 3](#).

**Table 3. Bus Voltage Gain Settings<sup>(1)</sup>**

| GBV1 | GBV0 | BUS VOLTAGE GAIN |
|------|------|------------------|
| D1   | D0   |                  |
| 0    | 0    | 2/5 V/V          |
| 0    | 1    | 1/5 V/V          |
| 1    | 0    | 1/10 V/V         |

(1) Shaded cells indicate default value.

## OUTPUT

The signal available at the output pin is selected by the output mode setting programmed in the Configuration Register. The default setting for the output mux is the Supply Power mode. For the power value to be valid, both the shunt voltage measurement and the bus voltage measurement must both be valid (within the linear range of the device).

### Power Calculation

The output voltage for the two power output modes is calculated as shown in Equation 1. To convert the output voltage to the corresponding power representation, the output voltage must be divided by the product of the power gain shown in Table 4 and the value of the shunt resistor.

$$V_{OUT} = (V_{CM})(V_{SENSE})(POWER_{GAIN}) \tag{1}$$

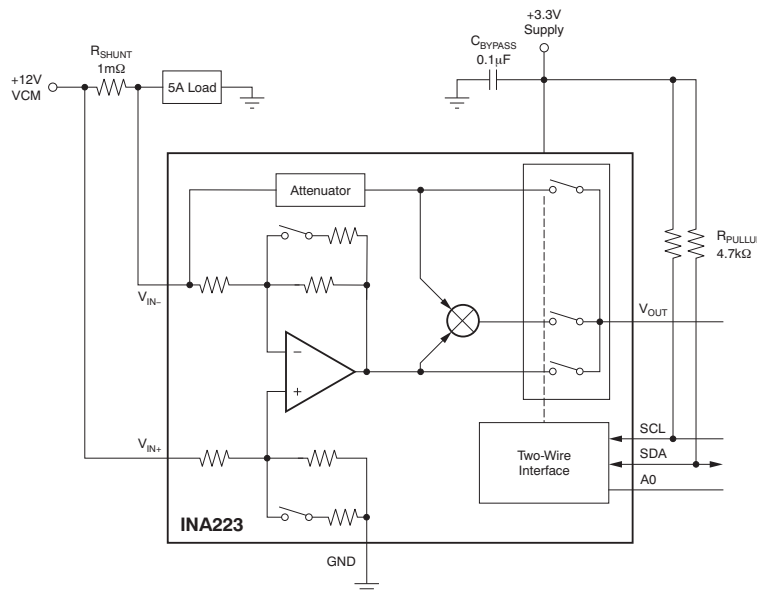
$$POWER = \frac{V_{OUT}}{(POWER_{GAIN})(R_{SHUNT})} \tag{2}$$

**Table 4. Power<sub>GAIN</sub> Values**

| GBV     | GSV     | POWER <sub>GAIN</sub> |
|---------|---------|-----------------------|
| 0.1 V/V | 20 V/V  | 0.667                 |
| 0.1 V/V | 128 V/V | 4.267                 |
| 0.1 V/V | 300 V/V | 10                    |
| 0.2 V/V | 20 V/V  | 1.333                 |
| 0.2 V/V | 128 V/V | 8.533                 |
| 0.2 V/V | 300 V/V | 20                    |
| 0.4 V/V | 20 V/V  | 2.667                 |
| 0.4 V/V | 128 V/V | 17.067                |
| 0.4 V/V | 300 V/V | 40                    |

### Power Calculation Example

The following example is based on Figure 34. In this example the system consists of a load current of 5 A and a common-mode voltage of 12 V. This 5-A current flowing through the 1-mΩ shunt resistor develops a differential voltage of 5 mV across the INA223 input pins. With the 3.3-V supply voltage shown here, a practical full-scale target for the output voltage is 3 V.



**Figure 34. Example Circuit**

### **Current Shunt Voltage Measurement Mode**

Based on the 5-mV differential voltage present at the input and the device set to Current Shunt Voltage mode, a current shunt voltage gain setting of 300 V/V is selected resulting in an output voltage of 1.5 V. A current shunt voltage gain setting less than 300 V/V could also be used in this example. The drawback of a lower gain setting is a smaller dynamic range present at the output as well as a less accurate input for the power measurement in the Power Output mode. A larger shunt resistor (2 m $\Omega$ ) could also be used to increase the full-scale drop to result. One drawback of increasing the impedance of the shunt resistor is the increased power dissipation requirement the component must be able to accommodate. A higher-accuracy power measurement is obtained with the largest possible input from the current shunt voltage, while remaining within the linear range of the device.

### **Bus Voltage Measurement Mode**

Assuming the same 3-V target as previously discussed, and with the device set to Bus Voltage mode, an attenuation factor of 0.2 V/V results in an output voltage of 2.4 V. An attenuation factor of 0.1 V/V could also be used, but results in a lower dynamic output range. An attenuation factor of 0.4 V/V cannot be used in this example because it results in an internal voltage of 4.8 V, exceeding the supply voltage of 3.3 V.

### **Power Modes**

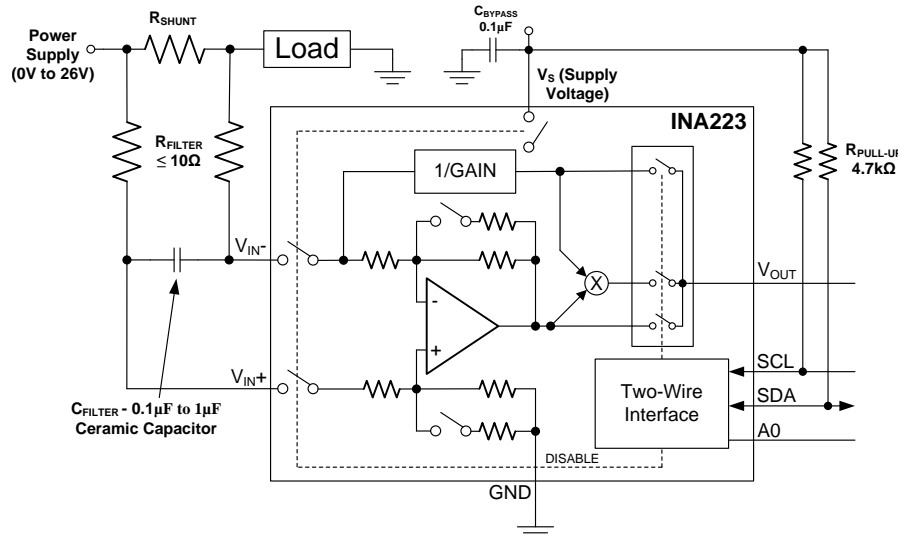
For the power output modes, the current shunt voltage and bus voltage measurements are multiplied by the Power Gain factor to yield a voltage output representing the calculated power. In this example, the 5 mV developed across the shunt resistor is multiplied by the 12-V bus voltage. This product is then multiplied by the Power Gain factor of 20 (GSV = 300 V/V, GBV = 0.2 V/V; See [Table 4](#)), and results in a 1.2-V output voltage representation of the power. Using [Equation 2](#) and the corresponding Power Gain of 20, the power being consumed by the load is calculated to be 60 W. This corresponds to the original 5-A load current and 12-V common-mode voltage conditions.

### **Bus Voltage Measurement Location for Power Output Modes**

For the power output mode, the bus voltage can be measured either at the  $V_{IN+}$  (supply side) or at the  $V_{IN-}$  (load side) pins when the current shunt voltage gain setting is 20. When the current shunt voltage gain setting is 128 or 300, this measurement assumes a relatively small differential voltage is being developed across the sense resistor. With a small drop across the sense resistor, the voltages at  $V_{IN+}$  and  $V_{IN-}$  are very close to one another, making the shunt voltage impact on the bus voltage measurement much less critical. When the device set to a gain of 20, it implies that a greater differential voltage is being developed across the sense resistor, causing the voltages at the  $V_{IN+}$  and  $V_{IN-}$  pins to be noticeably different. The power calculation can be configured to measure the bus voltage either at  $V_{IN+}$  (Supply Power) or at  $V_{IN-}$  (Load Power). If the power being supplied by the power supply is of interest, the Supply Power mode should be selected as the output mode setting. If the power being consumed by the load is of interest, the Load Power mode should be selected as the output mode setting. Note that the bus voltage measurement location is only available for the power calculation. For the Bus Voltage output mode, the bus voltage is always measured at the  $V_{IN+}$  pin.

### Input Filtering

An obvious and straightforward location for filtering is at the output of the INA223. However, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA223. [Figure 35](#) shows a filter placed at the inputs pins.



**Figure 35. Input Filter**

The addition of external series resistance, though, creates an additional error that is not present under normal operating conditions. An internal bias network at the input pins creates a mismatch in input bias currents when a differential voltage is applied to the device’s input pins. This results in a mismatch of voltage drops on the input lines due to the mismatch of input bias currents flowing through the additional external series filter resistors. This creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. The result is a reduced differential voltage at the device input pins relative to the expected shunt voltage created by the load current flowing through the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on the operation of the device.

The amount of variance in the differential voltage present directly at the input pins relative to the voltage developed at the shunt resistor is based both on values of external series resistance as well as the internal input resistors ( $R_{INT}$ ), which is based on the shunt voltage gain setting as shown in [Table 5](#). The reduction of the shunt voltage reaching the device input pins appears as a gain error when looking at the output voltage relative to the shunt voltage. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in [Equation 3](#).

$$\text{Gain Error Factor} = \frac{(1250 \cdot R_{INT})}{(1250 \cdot R_S) + (1250 \cdot R_{INT}) + (R_S \cdot R_{INT})}$$

Where

- $R_{INT}$  is the internal input resistance.
- $R_S$  is the external series resistance.

(3)

With the adjustment factor equation including the device internal input resistance, this factor will vary with each gain setting.

**Table 5. Internal Resistance Values**

| GAIN SETTING | $R_{INT}$ |
|--------------|-----------|
| 20           | 600 kΩ    |
| 128          | 93 kΩ     |
| 300          | 40 kΩ     |

### Using The INA223 with Common-Mode Transients Above 26 V

The INA223 is designed for a maximum common-mode voltage of 26 V. In applications that may be subjected to transients above 26 V, the INA223 inputs must be protected. Figure 36 is the recommended method for protecting the INA223 to these transients. Use only zener diodes or zener-type transient absorbers (also known as a TransZorb™). Most other types of transient absorbers have an unacceptable time delay. The input resistors shown in Figure 36 should be kept as small as possible (less than 10 Ω) to limit the effects this resistance has on the gain, as discussed in the Input Filtering section.

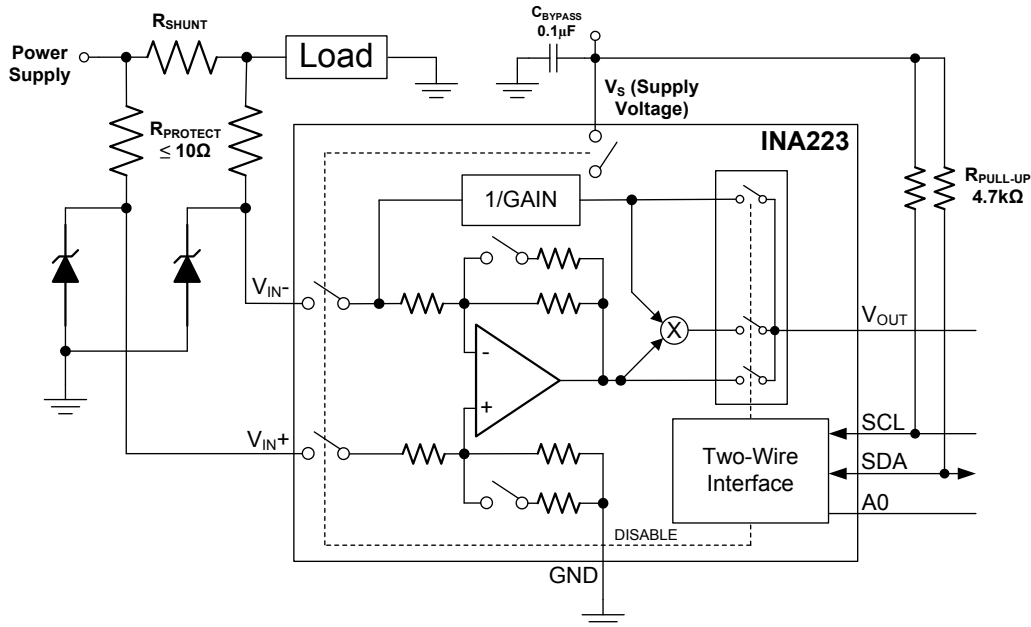


Figure 36. INA223 Transient Protection

### Low-Side Current Sensing

The bus voltage of the INA223 is measured internally at the  $V_{IN+}$  pin, making it a high-side-only power monitor. However, the INA223 can be used for low-side current sensing, as shown in Figure 37 (as the common-mode voltage ranges from 0 V to 26 V).

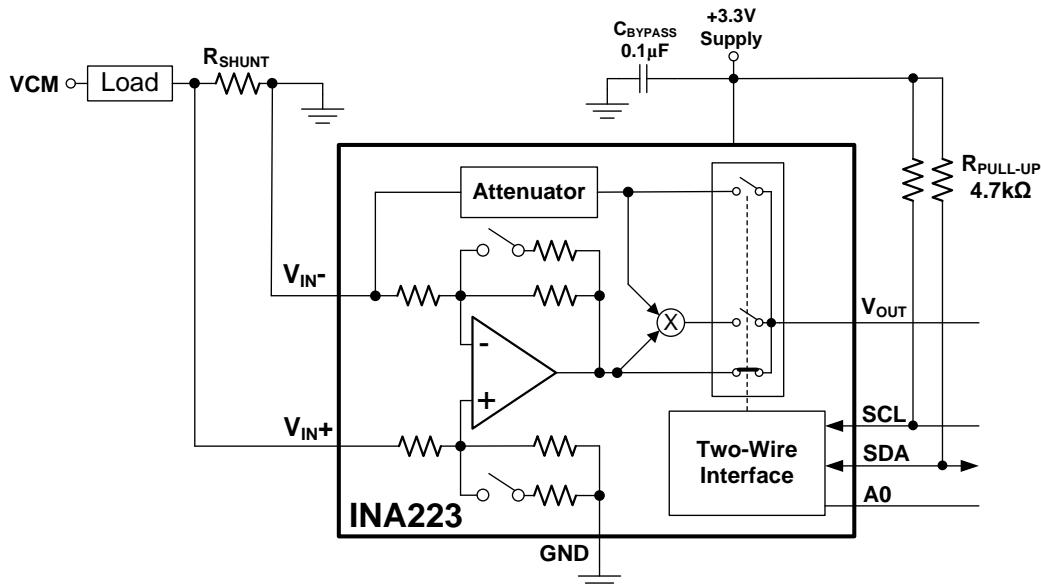
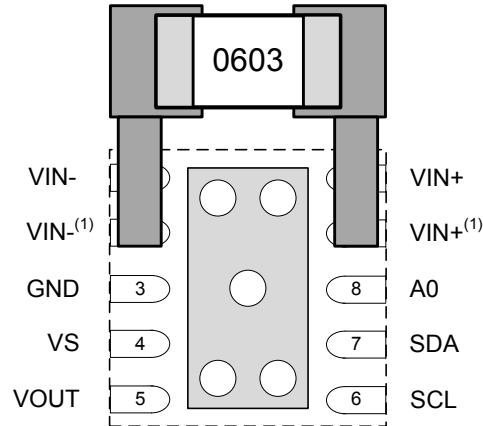


Figure 37. Low-Side Sensing with INA223

### INA223 Recommended Layout

The recommended layout is shown in [Figure 38](#). Pins 2 and 9 should be connected directly to Pins 1 and 10, respectively. The shunt resistor should be placed as closely to the input pins, VIN+ and VIN-, to minimize any parasitics or added resistance. Use a four-wire, or kelvin, connection to the shunt to achieve the most accurate measurement across the shunt.



(1) See [Application Information](#) section for a description of how to connect input pins to the shunt resistor.

**Figure 38. INA223 Recommended Layout**

## BUS OVERVIEW

The INA223 is compatible with both two-wire and SMBus interfaces. These protocols are essentially compatible with one another. The two-wire interface is used throughout this data sheet as the primary example, with the SMBus protocol specified only when a difference between the two systems is considered.

Two bidirectional lines, SCL and SDA, connect the INA223 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates *start* and *stop* conditions.

To address a specific device, the master initiates a *start* condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a *start* or *stop* condition.

After all data have been transferred, the master generates a *stop* condition, indicated by pulling SDA from low to high while SCL is high. The INA223 includes a 28-ms timeout on its interface to prevent locking up the bus.

### Serial Bus Address

To communicate with the INA223, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit that indicates the intent of executing a read or write operation.

The INA223 has one address pin, A0. [Table 6](#) describes the pin logic levels for each of the four possible addresses. The state of the A0 pin is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

**Table 6. INA223 Address Pins and Slave Addresses**

| A0             | ADDRESS |
|----------------|---------|
| GND            | 1000000 |
| V <sub>S</sub> | 1000001 |
| SDA            | 1000010 |
| SCL            | 1000011 |

### Serial Interface

The INA223 operates only as a slave device on both the two-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The INA223 supports the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted most significant byte first.

## GENERAL CALL

The INA223 responds to three unique two-wire general call commands. A response occurs to a general call address (0000000) if the eighth bit is '0'. The device acknowledges the general call address and responds to commands based on the second byte. The three commands that the INA223 responds to are:

- General Call Reset (06h)
- General Call Enable (81h)
- General Call Disable (82h)

The INA223 responds to the General Call Reset by resetting all of the Configuration Registers settings to the respective default power-on values. The INA223 responds to a General Call Enable or General Call Disable by entering into or exiting from a disabled state. The INA223 can also be enabled and disabled by setting or clearing the enable/disable mode (EN) bit in the Configuration Register. The General Call Enable and General Call Disable commands allow for a single command to place multiple connected INA223 devices into either an enabled or disabled state.

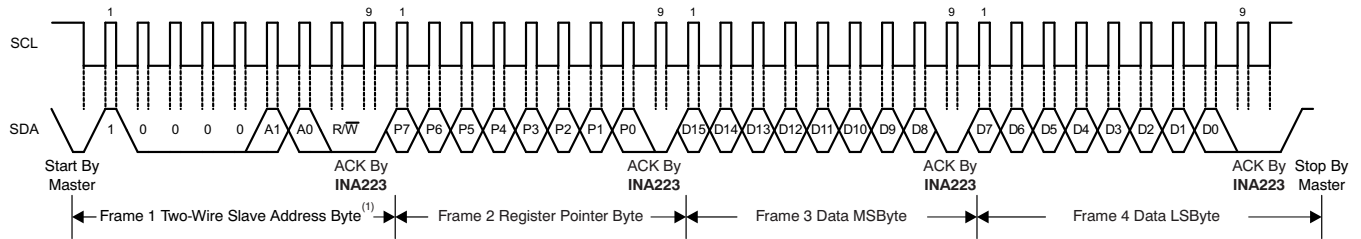
## WRITING TO AND READING FROM THE INA223

The INA223 has a single configuration register. This register is used to configure the INA223 based on how the device is to be used. This register can also be read to determine the register contents and the current device configuration.

Writing to the Configuration Register in the INA223 begins with the first byte transmitted by the master. This byte is the slave address, with the  $\overline{R/W}$  bit low. The INA223 then acknowledges receipt of a valid address. The next two bytes are written to the register addressed by the register pointer. The INA223 acknowledges receipt of each data byte. The master may terminate data transfer by generating a *start* or *stop* condition.

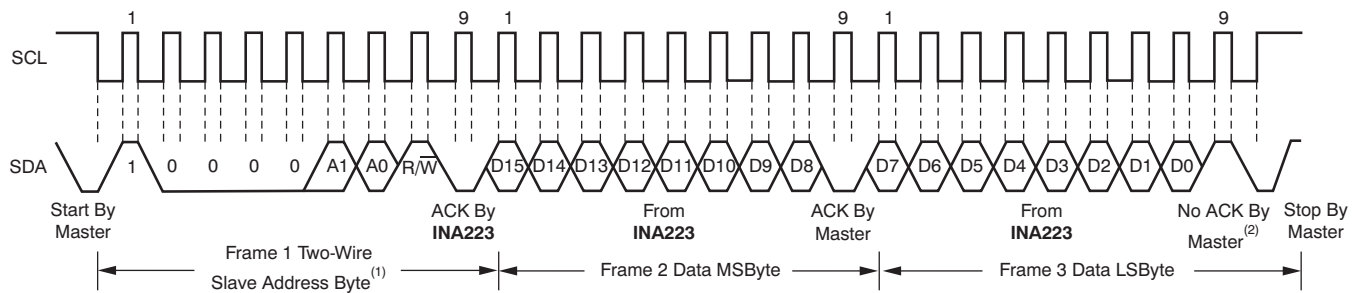
When reading the Configuration Register in the INA223, the communication sequence begins the same with the first byte being transmitted by the master. This byte is the slave address, with the  $R/\overline{W}$  bit high. The INA223 then acknowledges receipt of a valid address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an acknowledge bit from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a not-acknowledge bit after receiving any data byte, or by generating a *start* or *stop* condition.

Figure 39 and Figure 40 show read and write operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the Slave Address Byte is determined by the setting of the A0 pin. Refer to Table 1.

**Figure 39. Timing Diagram for Write Word Format**



(1) The value of the Slave Address Byte is determined by the setting of the A0 pin. Refer to Table 1.

(2) ACK by master can also be sent.

**Figure 40. Timing Diagram for Read Word Format**

### High-Speed Two-Wire Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a *start* condition followed by a valid serial byte containing high-speed (HS) master code 00001XXX. This transmission is made in either fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The INA223 does not acknowledge the HS master code, but recognizes it and switches its internal filters to support 3.4-MHz operation.

The master then generates a *repeated start* condition (a *repeated start* condition has the same timing as the *start* condition). After this *repeated start* condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 MHz are allowed. Instead of using a *stop* condition, *repeated start* conditions should be used to secure the bus in HS-mode. A *stop* condition ends the HS-mode and switches all the internal filters of the INA223 to support the F/S mode. Figure 41 illustrates the bus timing. Corresponding definitions are listed in Table 7.

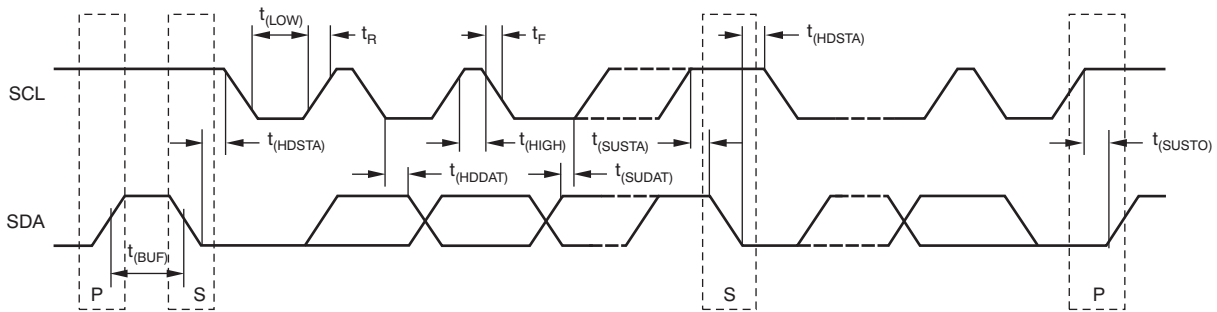


Figure 41. Bus Timing Diagram

Table 7. Bus Timing Diagram Definitions

| SYMBOL               | DESCRIPTION   | FAST MODE |      | HIGH-SPEED MODE |     | UNITS |
|----------------------|---|-----------|------|-----------------|-----|-------|
|                      |   | MIN       | MAX  | MIN             | MAX |       |
| f <sub>(SCL)</sub>   | SCL operating frequency   | 0.001     | 0.4  | 0.001           | 3.4 | MHz   |
| t <sub>(BUF)</sub>   | Bus free time between <i>stop</i> and <i>start</i> conditions                                     | 600       |      | 160             |     | ns    |
| t <sub>(HDSTA)</sub> | Hold time after <i>repeated start</i> condition. After this period, the first clock is generated. | 100       |      | 100             |     | ns    |
| t <sub>(SUSTA)</sub> | <i>Repeated start</i> condition setup time  | 100       |      | 100             |     | ns    |
| t <sub>(SUSTO)</sub> | <i>Stop</i> condition setup time  | 100       |      | 100             |     | ns    |
| t <sub>(HDDAT)</sub> | Data hold time  | 15        |      | 15              |     | ns    |
| t <sub>(SUDAT)</sub> | Data setup time   | 100       |      | 10              |     | ns    |
| t <sub>(LOW)</sub>   | SCL clock low period  | 1300      |      | 160             |     | ns    |
| t <sub>(HIGH)</sub>  | SCL clock high period   | 600       |      | 60              |     | ns    |
| t <sub>F</sub>       | Clock/Data fall time  |           | 300  |                 | 160 | ns    |
| t <sub>R</sub>       | Clock/Data rise time  |           | 300  |                 | 160 | ns    |
|                      | Clock/Data rise time for SCLK ≤ 100 kHz   |           | 1000 |                 |     | ns    |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| INA223AIDSKR     | ACTIVE        | SON          | DSK             | 10   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 105   | P223                    | <a href="#">Samples</a> |
| INA223AIDSKT     | ACTIVE        | SON          | DSK             | 10   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 105   | P223                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

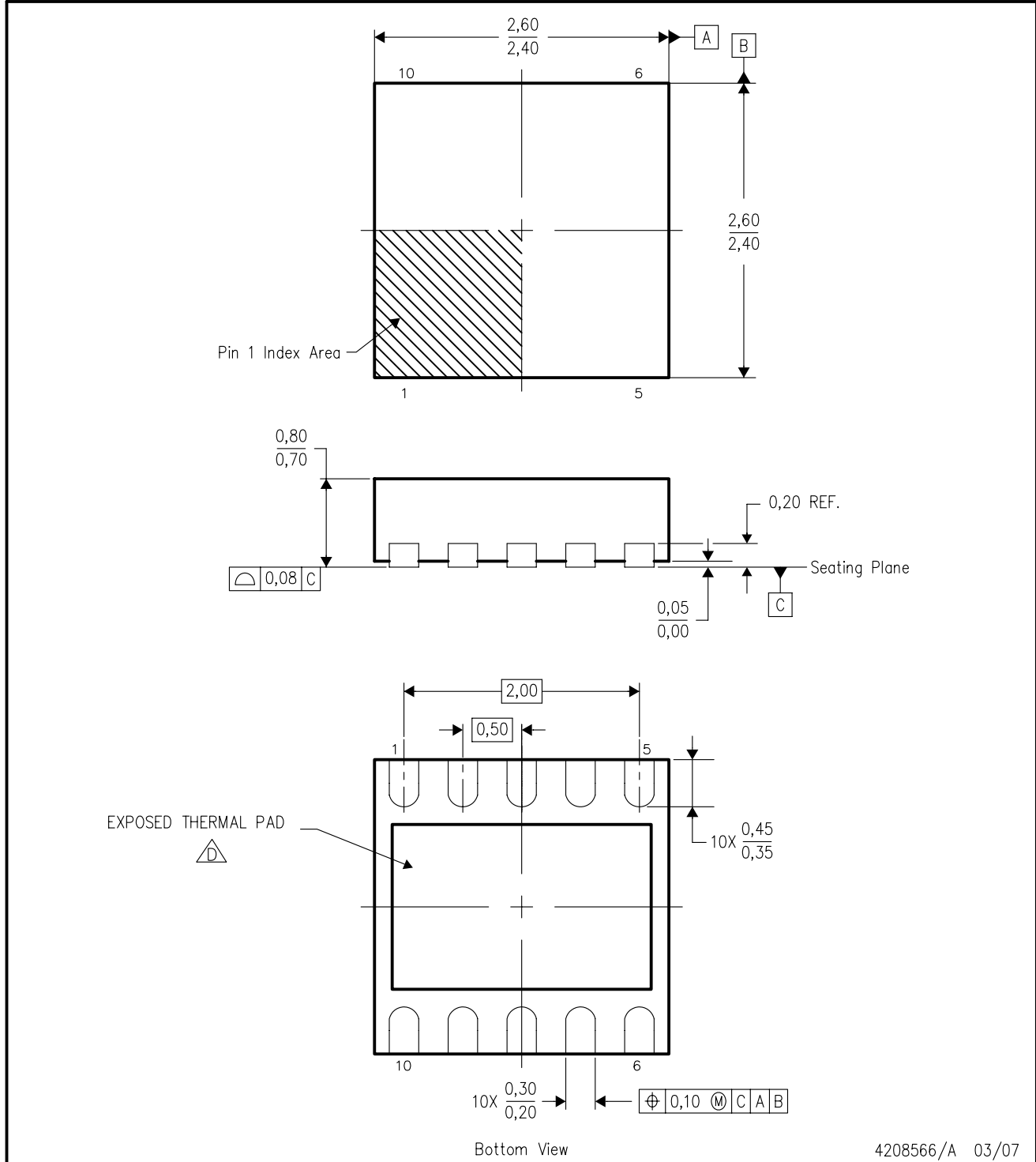
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.




DSK (S-PDSO-N10)

PLASTIC QUAD FLATPACK



4208566/A 03/07

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

## THERMAL PAD MECHANICAL DATA

DSK (R-PWSON-N10)

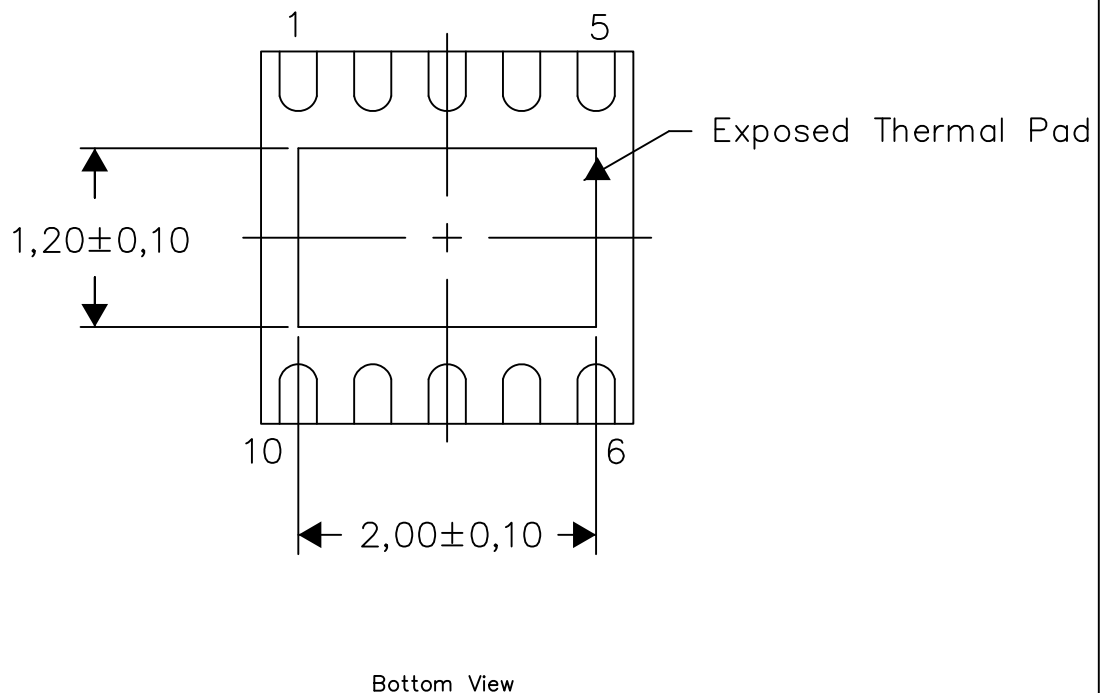
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



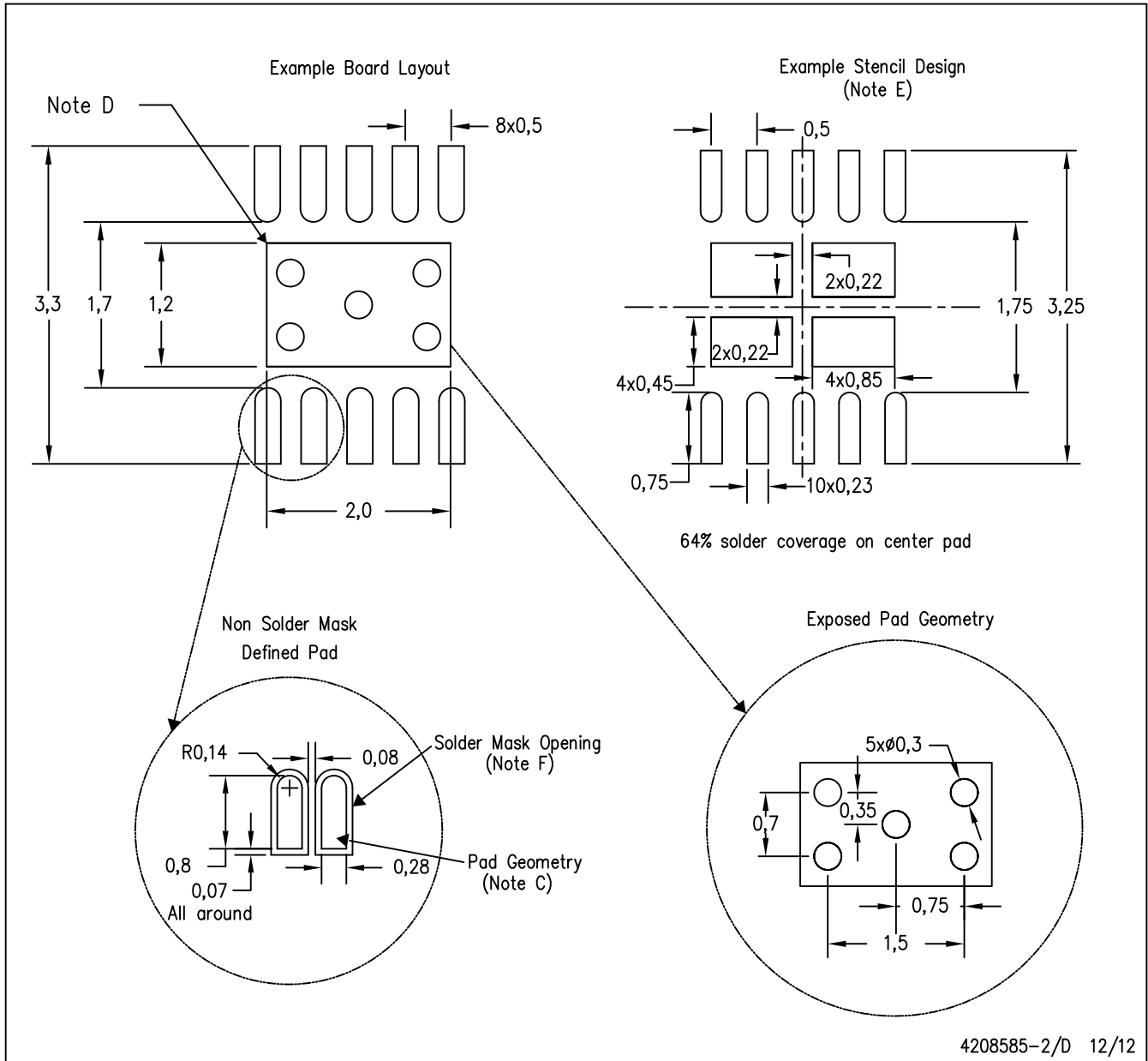
Exposed Thermal Pad Dimensions

4208579-2/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## 重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和和该等应用所用 TI 产品的功能而设计。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与应用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负任何责任，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准而设计。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2018 德州仪器半导体技术（上海）有限公司