

Excalibur™ 低噪声高速精确运算放大器

查询样品: [TLE2141-Q1](#)

特性

- 符合汽车应用要求
- 低噪声
 - 10 Hz ... 15 nV/√Hz
 - 1 kHz ... 10.5 nV/√Hz
- 10000-pF 负载能力
- 20-mA 最小短路输出电流
- 27-V/μs 转换率 (最小值)
- 高增益-带宽产品 ... 5.9 MHz
- 在 25°C 下, 低 V_{IO} ... 500 μV (最大值)
- 单一或分电源 ... 4 V 至 44 V
- 快速建立时间
 - 340 ns 达到 0.1%
 - 400 ns 达到 0.01%
- 饱和恢复 ... 150 ns
- 大输出摆幅 ... $V_{CC-} + 0.1 V$ 至 $V_{CC+} - 1 V$

说明

TLE2141-Q1 是一款高性能、内部补偿运算放大器, 此期间使用德州仪器互补双极 Excalibur™ 工艺制造。它是标准工业产品的引脚兼容升级产品。

这个设计包含一个输入级, 可同时实现含有一个 10-Hz 1/f 弯曲的 10.5 nV/√Hz 的低音频带噪声和典型负载高达 800 pF 的对称 40-V/μs 转换率。这引起的低失真和高功率带宽在高保真音频应用中非常重要。达到具有 2-kΩ/100-pF 负载的 10-V 阶跃 0.1% 的 340 ns 快速建立时间 在快速致动器/定位驱动器中十分有用。在相似的测试环境下, 达到 0.01% 的建立时间是 400 ns。

虽然 6-MHz 带宽减少至高负载电平时的 1.8 MHz, 此器件在电容负载高达 10 nF 时, 仍保持稳定。例如, TLE2141-Q1 用于低固定偏差采样保持电路和长电缆的直接缓冲, 包括 4-mA 至 20-mA 电流环路。

此特别设计也显示了一个改进了的对内在集成电路组件不匹配时的不敏感性, 这一点可由一个最大 500-μV 偏移电压和 1.7-μV/°C 典型电压漂移来得以证明。最小共模抑制比和电源电压抑制比分别为 85 dB 和 90 dB。

在电压范围为 ±2-V 至 ±22-V 时, 器件性能与电源电压无关。虽然过多的输入电流可能从每个超过较低共模输入范围的输入中流出, 输入可在不导致相位反转的情况下, 工作在 $V_{CC-} - 0.3 V$ 至 $V_{CC+} - 1.8 V$ 的电压范围内。在轻电流负载条件下, 该全-npn 输出级提供一个 $V_{CC-} - 0.1 V$ 至 $V_{CC+} - 1 V$ 的接近轨到轨的输出摆幅。由于输出电流是内部有限的, 此器件能够为任一电源保持短接, 但是必须小心以保证不超过最大封装功率耗散。

TLE2141-Q1 也可被用于比较器。在不对器件造成损害的情况下, V_{CC+} 的差分输入可被保持。含有 TTL 电源电平的开环传播延迟典型值为 200 ns。当该器件驱动电压超过建议输出电压摆幅限制的时候, 会给出一个正常指示来标示输出级饱和和恢复。

TLE2141-Q1 采用工业标准 8-引脚封装。该器件工作温度范围 -40°C 至 125°C。

订购信息⁽¹⁾

T_A	封装		可订购部件号	顶端标记
-40°C 至 125°C	SOIC – D (8 引脚)	卷盘 (2500 片)	TLE2141QDRQ1	2141Q

(1) 有关最新的封装和订购信息, 请参阅本文档结尾的“封装选项附录”, 或访问 TI 网站: www.ti.com。

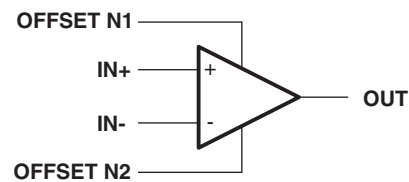
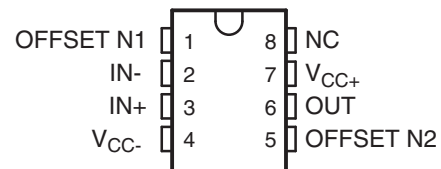


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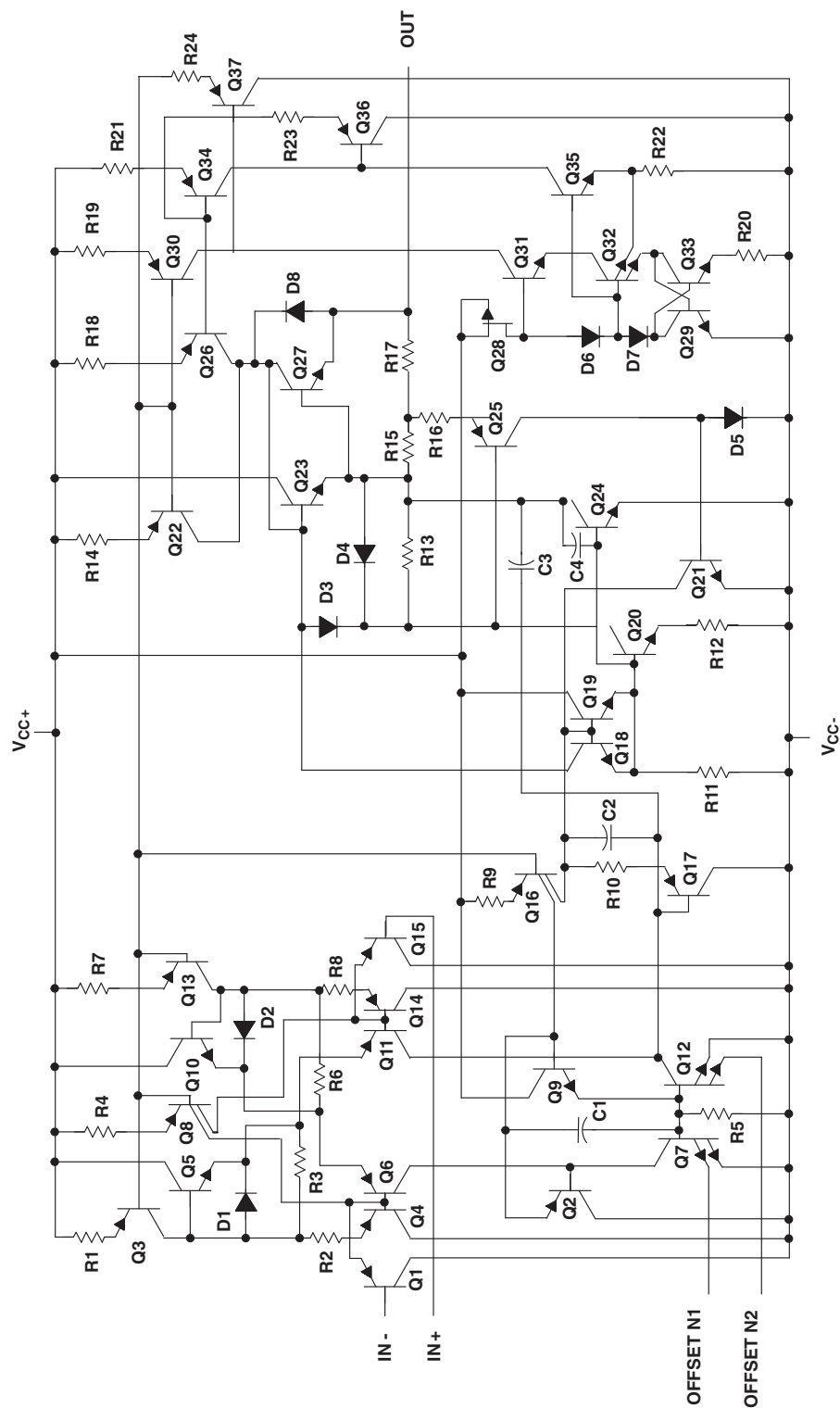
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English Data Sheet: [SLOS525](#)

SYMBOL**D PACKAGE
(TOP VIEW)**

NC – No internal connection

Figure 1. EQUIVALENT SCHEMATIC



DEVICE COMPONENT COUNT

COMPONENT	TLE2141-Q1
Transistors	46
Resistors	24
Diodes	8
Capacitors	4
Epi-FET	1

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT	
V _{CC+}	Supply voltage ⁽²⁾	22	V	
V _{CC-}	Supply voltage	−22	V	
V _{ID}	Differential input voltage ⁽³⁾	±44	V	
V _I	Input voltage range (any input)	V _{CC+} to (V _{CC-} − 0.3)	V	
I _I	Input current (each input)	±1	mA	
I _O	Output current	±80	mA	
	Total current into V _{CC+}	80	mA	
	Total current out of V _{CC-}	80	mA	
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾	Unlimited		
θ _{JA}	Package thermal impedance ⁽⁵⁾ ⁽⁶⁾	D package (8 pin)	97.1	°C/W
T _A	Operating free-air temperature range	−40 to 125	°C	
T _{stg}	Storage temperature range	−65 to 150	°C	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C	

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows, if input, are brought below $V_{CC-} - 0.3$ V.
- (4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- (5) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _{CC±}	Supply voltage		±2	±22	V
V _{IC}	Common-mode input voltage	V _{CC} = 5 V	0	2.7	V
		V _{CC±} = ±15 V	−15	12.7	
T _A	Operating free-air temperature		−40	125	°C

ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		225	1400	μV
		Full range			2100	
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		8	100	nA
		Full range			250	
I_{IB} Input bias current	$V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$, $V_{IC} = 2.5\text{ V}$	25°C		–0.8	–2	μA
		Full range			–2.3	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3	–0.3 to 3.2		V
		Full range	0 to 2.7	–0.3 to 2.9		
V_{OH} High-level output voltage	$I_{OH} = -150\ \mu\text{A}$	25°C		3.9	4.1	V
	$I_{OH} = -1.5\text{ mA}$			3.8	4	
	$I_{OH} = -15\text{ mA}$			3.2	3.7	
	$I_{OH} = -100\ \mu\text{A}$	Full range		3.75		
	$I_{OH} = -1\text{ mA}$			3.65		
	$I_{OH} = -10\text{ mA}$			3.25		
V_{OL} Low-level output voltage	$I_{OL} = 150\ \mu\text{A}$	25°C		75	125	mV
	$I_{OL} = 1.5\text{ mA}$			150	225	
	$I_{OL} = 15\text{ mA}$			1.2	1.4	V
	$I_{OL} = 100\ \mu\text{A}$	Full range			200	mV
	$I_{OL} = 1\text{ mA}$				250	
	$I_{OL} = 10\text{ mA}$				1.25	V
A_{VD} Large-signal differential voltage amplification	$V_{IC} = \pm 2.5\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1\text{ V to }1.5\text{ V}$	25°C	50	220		V/mV
		Full range	5			
r_i Input resistance		25°C		70		M Ω
c_i Input capacitance		25°C		2.5		pF
z_o Open-loop output impedance	$f = 1\text{ MHz}$	25°C		30		Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$, $R_S = 50\ \Omega$	25°C	85	118		dB
		Full range	80			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$, $R_S = 50\ \Omega$	25°C	90	106		dB
		Full range	85			
I_{CC} Supply current	$V_O = 2.5\text{ V}$, No load, $V_{IC} = 2.5\text{ V}$	25°C		3.4	4.4	mA
		Full range			4.6	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$		45		V/ μs
SR–	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 500\text{ pF}$		42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 2.5-V step	To 0.1%	0.16		μs
			To 0.01%	0.22		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 10\text{ Hz}$	15		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51		
I_n	Equivalent input noise current	$f = 10\text{ Hz}$		1.92		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.5		
THD+N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }3\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 2$, $f = 10\text{ kHz}$		0.0052		%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$		5.9		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$, $f = 100\text{ kHz}$		5.8		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 2\text{ k}\Omega^{(1)}$, $A_{VD} = 1$		660		kHz
Φ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^{(1)}$, $C_L = 100\text{ pF}^{(1)}$		57		°

(1) R_L and C_L terminated to 2.5 V.

ELECTRICAL CHARACTERISTICS

 $V_{CC} = \pm 15\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A ⁽¹⁾	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		200	900	μV
			Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$	Full range		1.7		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		7	100	nA
			Full range			250	
I_{IB}	Input bias current	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		–0.7	–1.5	μA
			Full range			–1.8	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	–15 to 13	–15.3 to 13.2		V
			Full range	–15 to 12.7	–15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	$I_O = -150\ \mu\text{A}$	25°C		13.8	14.1	V
		$I_O = -1.5\ \text{mA}$			13.7	14	
		$I_O = -15\ \text{mA}$			13.1	13.7	
		$I_O = -100\ \mu\text{A}$	Full range		13.7		
		$I_O = -1\ \text{mA}$			13.6		
		$I_O = -10\ \text{mA}$			13.1		
V_{OM-}	Maximum negative peak output voltage swing	$I_O = 150\ \mu\text{A}$	25°C		–14.7	–14.9	V
		$I_O = 1.5\ \text{mA}$			–14.5	–14.8	
		$I_O = 15\ \text{mA}$			–13.4	–13.8	
		$I_O = 100\ \mu\text{A}$	Full range		–14.6		
		$I_O = 1\ \text{mA}$			–14.5		
		$I_O = 10\ \text{mA}$			–13.4		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$, $R_L = 2\ \text{k}\Omega$	25°C		100	450	V/mV
			Full range		20		
r_i	Input resistance		25°C		65		M Ω
c_i	Input capacitance		25°C		2.5		pF
z_o	Open-loop output impedance	$f = 1\ \text{MHz}$	25°C		30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$, $R_S = 50\ \Omega$	25°C		85	108	dB
			Full range		80		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V}$ to $\pm 15\ \text{V}$, $R_S = 50\ \Omega$	25°C		90	106	dB
			Full range		85		
I_{OS}	Short-circuit output current	$V_O = 0$	25°C		–25	–50	mA
					20	31	
I_{CC}	Supply current	$V_O = 0$, No load, $V_{IC} = 2.5\ \text{V}$	25°C		3.5	4.5	mA
			Full range			4.7	

(1) Full range is -40°C to 125°C .

OPERATING CHARACTERISTICS

$V_{CC} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$	27	45		V/ μs
SR–	Negative slew rate	$A_{VD} = -1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$	27	42		V/ μs
t_s	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%	0.34		μs
			To 0.01%	0.4		
V_n	Equivalent input noise voltage	$R_S = 20\text{ }\Omega$	$f = 10\text{ Hz}$	15		$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51		
I_n	Equivalent input noise current	$f = 10\text{ Hz}$		1.89		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.47		
THD+N	Total harmonic distortion plus noise	$V_{O(PP)} = 20\text{ V}$, $R_L = 2\text{ k}\Omega$, $A_{VD} = 10$, $f = 10\text{ kHz}$		0.01		%
B_1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		6		MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$		5.9		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 20\text{ V}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		668		kHz
ϕ_m	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		58		°

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

V_{IO}	Input offset voltage	Distribution	Figure 2
I_{IO}	Input offset current	vs Free-air temperature	Figure 3
I_{IB}	Input bias current	vs Common-mode input voltage	Figure 4
		vs Free-air temperature	Figure 5
V_{OM+}	Maximum positive peak output voltage	vs Supply voltage	Figure 6
		vs Free-air temperature	Figure 7
		vs Output current	Figure 8
		vs Settling time	Figure 10
V_{OM-}	Maximum negative peak output voltage	vs Supply voltage	Figure 6
		vs Free-air temperature	Figure 7
		vs Output current	Figure 9
		vs Settling time	Figure 10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 11
V_{OH}	High-level output voltage	vs Output current	Figure 12
V_{OL}	Low-level output voltage	vs Output current	Figure 13
	Phase shift	vs Frequency	Figure 14
A_{VD}	Large-signal differential voltage amplification	vs Frequency	Figure 14
		vs Free-air temperature	Figure 15
z_o	Closed-loop output impedance	vs Frequency	Figure 16
I_{OS}	Short-circuit output current	vs Free-air temperature	Figure 17
CMRR	Common-mode rejection ratio	vs Frequency	Figure 18
		vs Free-air temperature	Figure 19
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	Figure 20
		vs Free-air temperature	Figure 21
I_{CC}	Supply current	vs Supply voltage	Figure 22
		vs Free-air temperature	Figure 23
V_n	Equivalent input noise voltage	vs Frequency	Figure 24
V_n	Input noise voltage	Over a 10-second period	Figure 25
I_n	Noise current	vs Frequency	Figure 26
THD+N	Total harmonic distortion plus noise	vs Frequency	Figure 27
SR	Slew rate	vs Free-air temperature	Figure 28
		vs Load capacitance	Figure 29
	Pulse response	Noninverting large signal	Figure 30
		Inverting large signal	Figure 31
		Small signal	Figure 32
B_1	Unity-gain bandwidth	vs Load capacitance	Figure 33
	Gain margin	vs Load capacitance	Figure 34
ϕ_m	Phase margin	vs Load capacitance	Figure 35

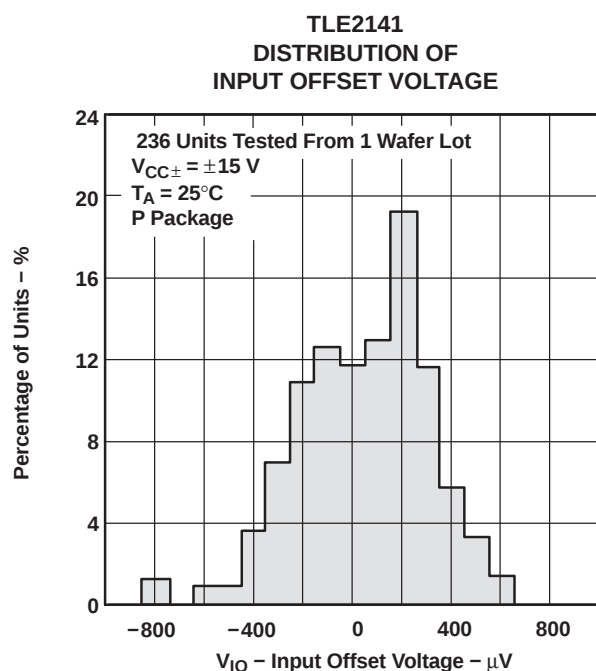


Figure 2.

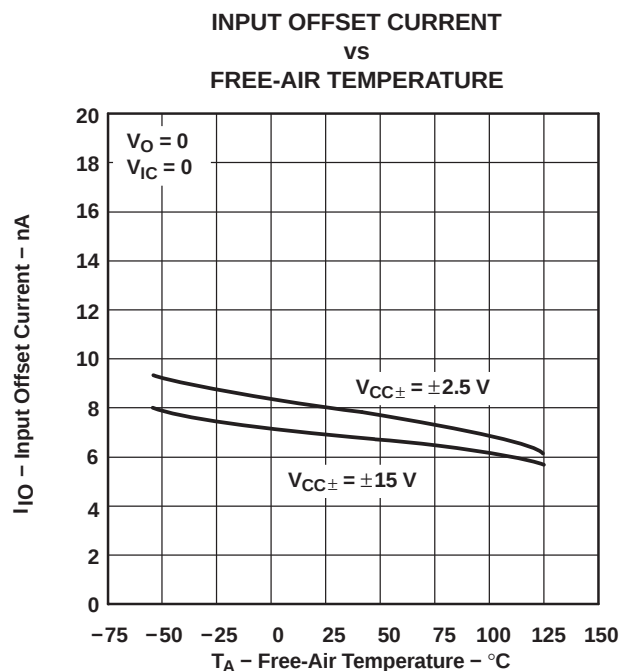


Figure 3.

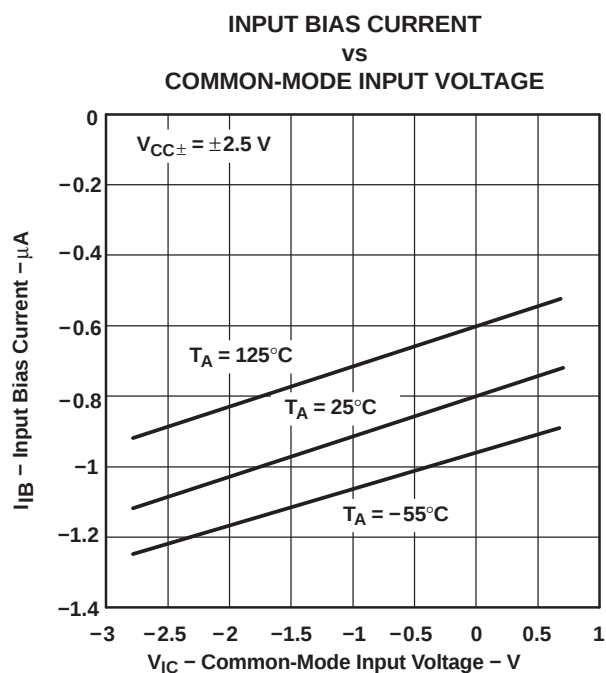


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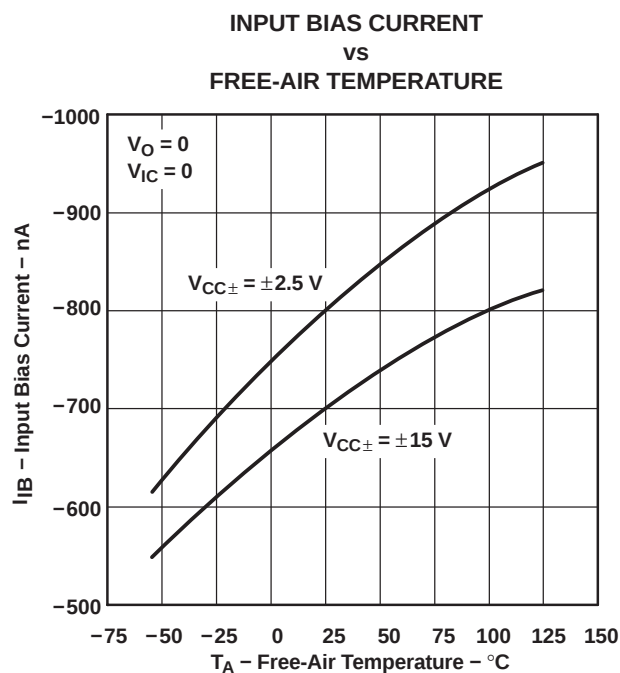


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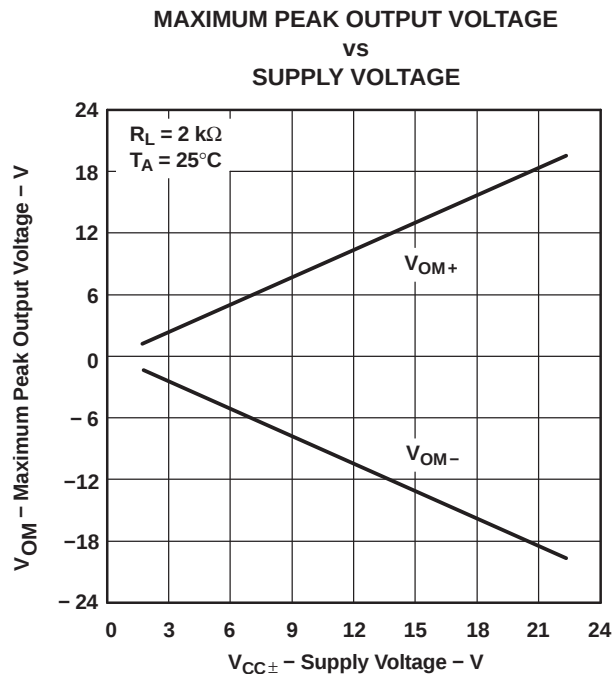


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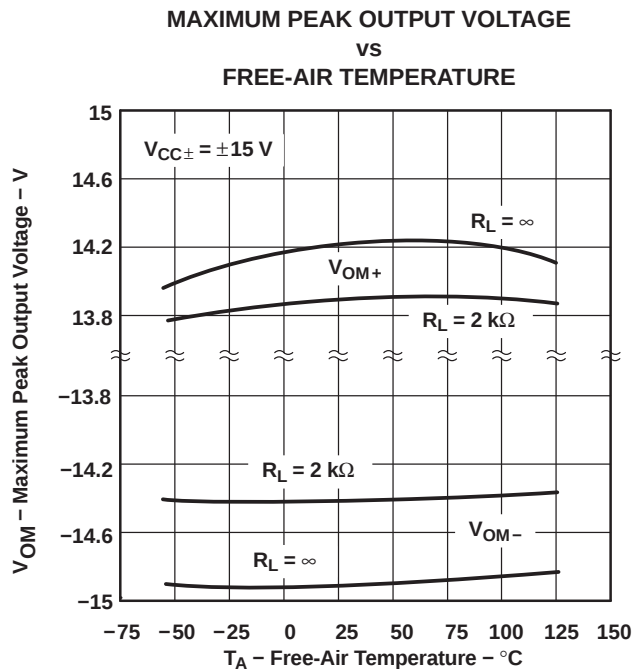


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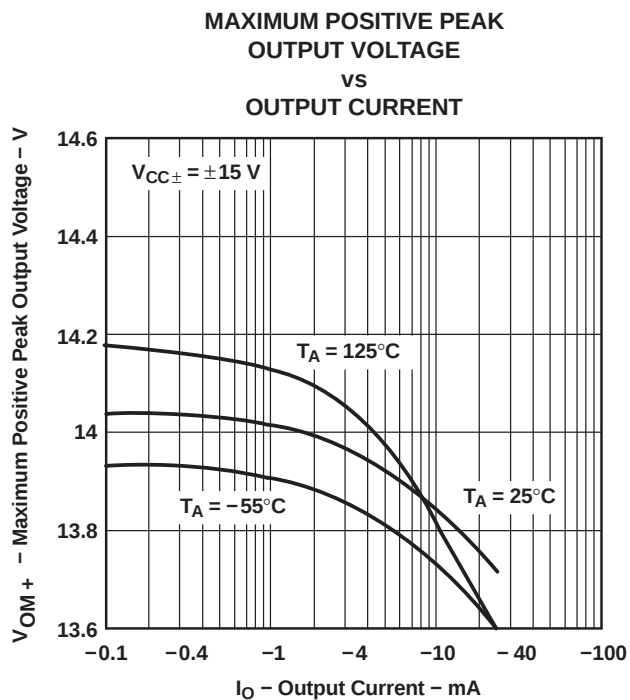


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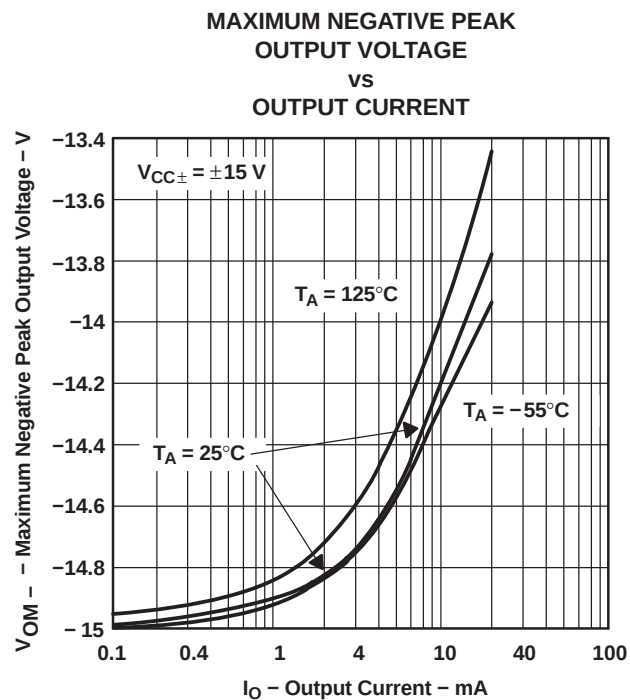


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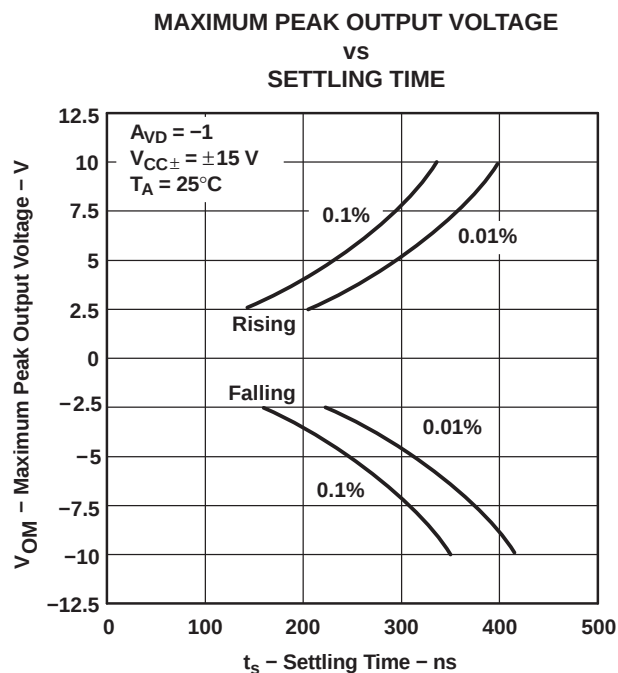


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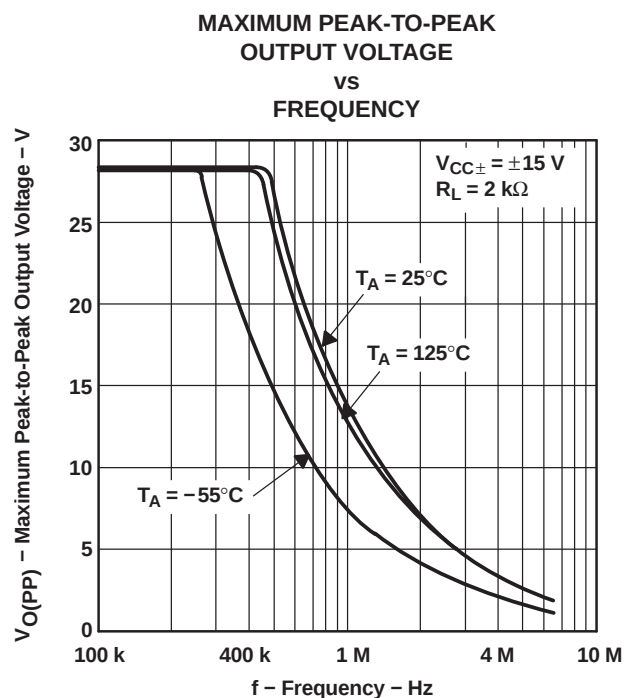


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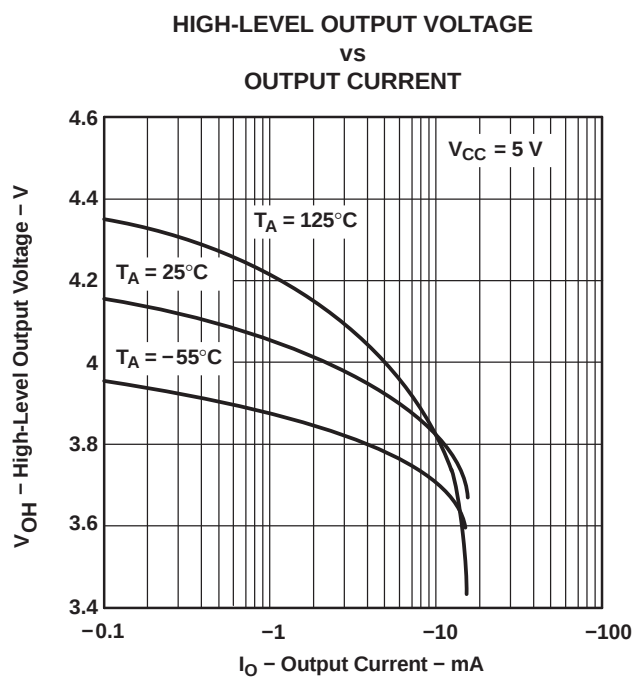


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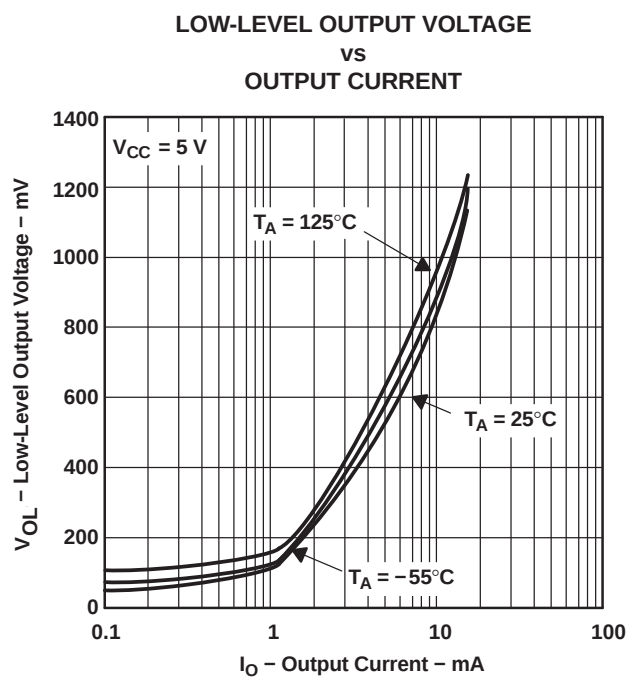


Figure 13.

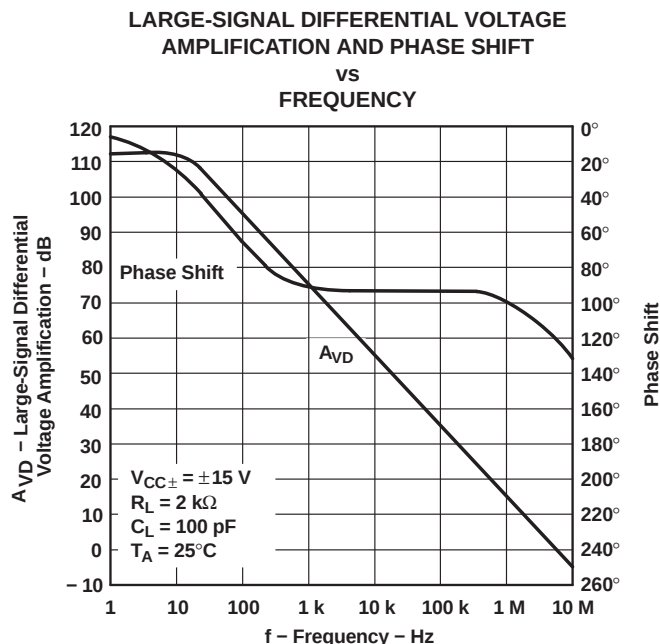


Figure 14.

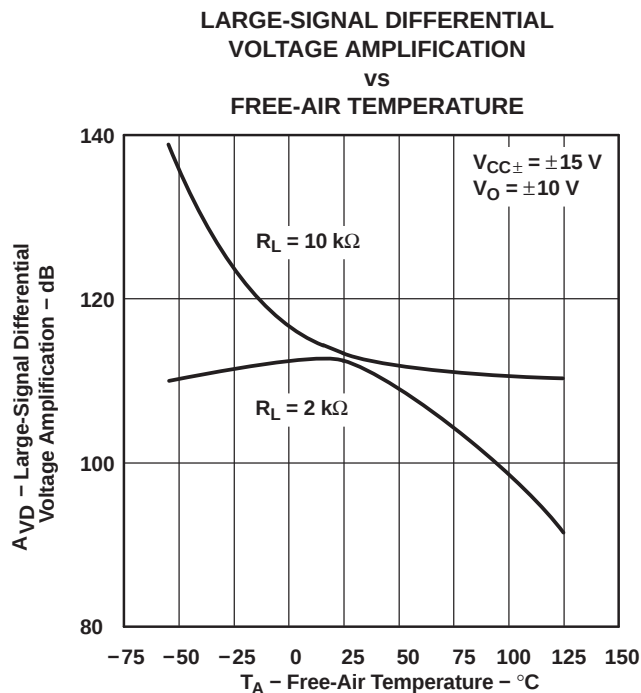


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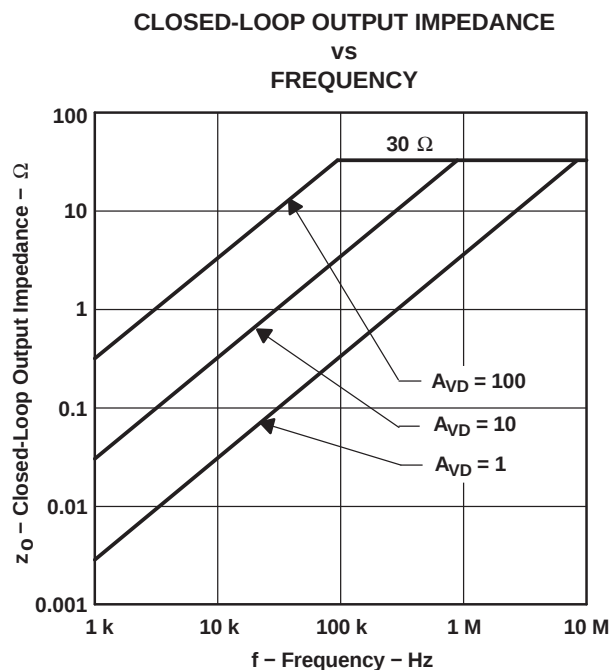


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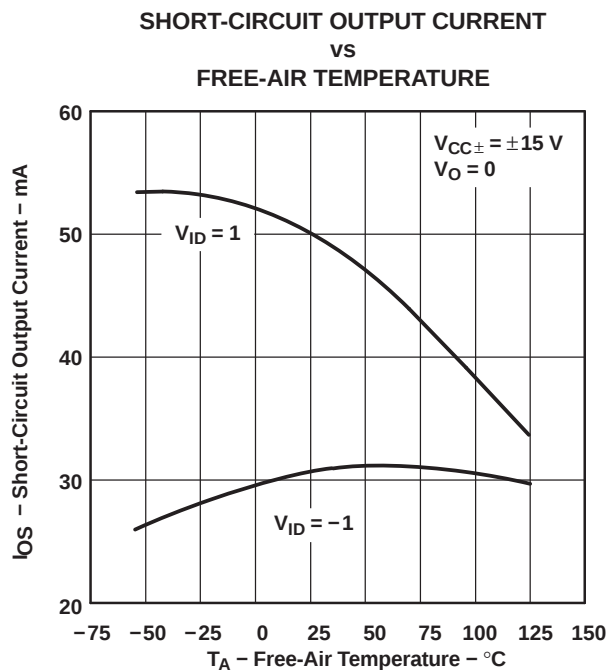


Figure 17.

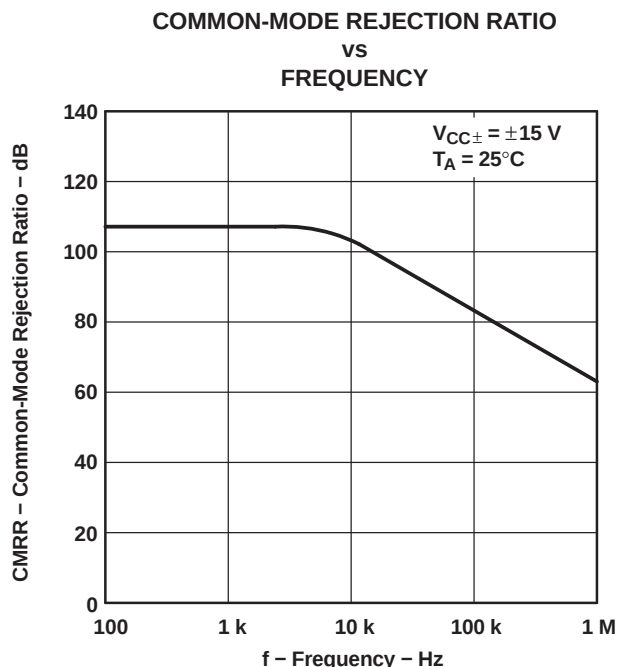


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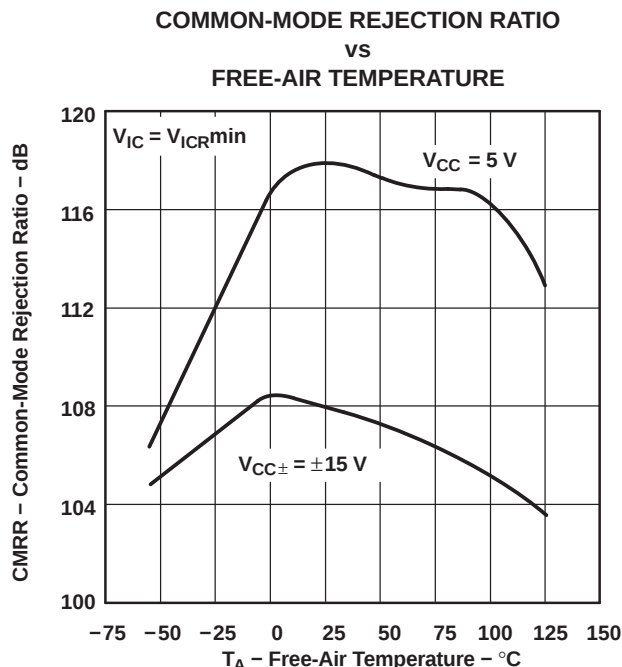


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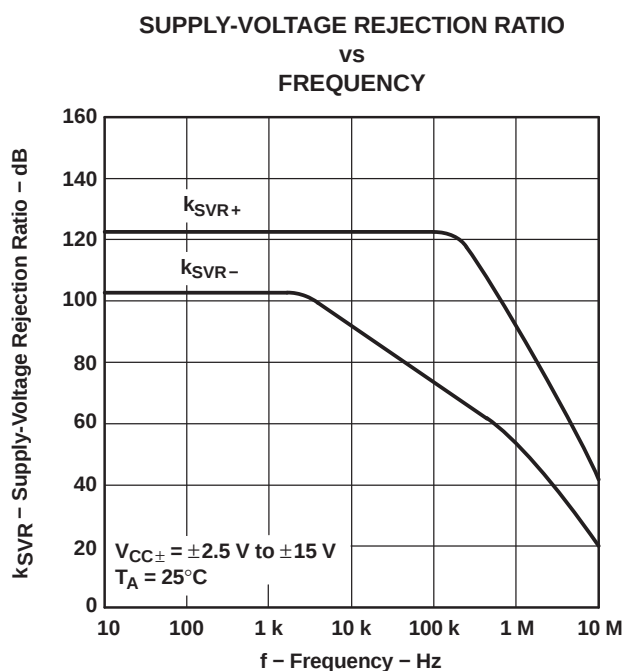


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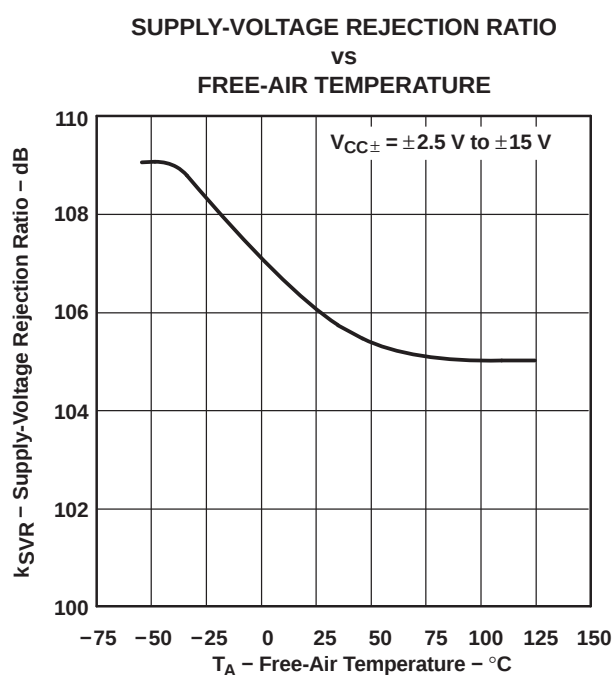


Figure 21.

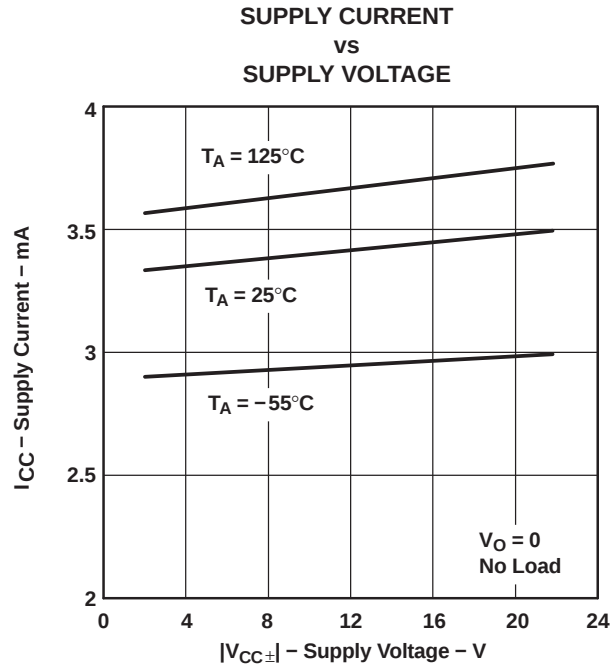


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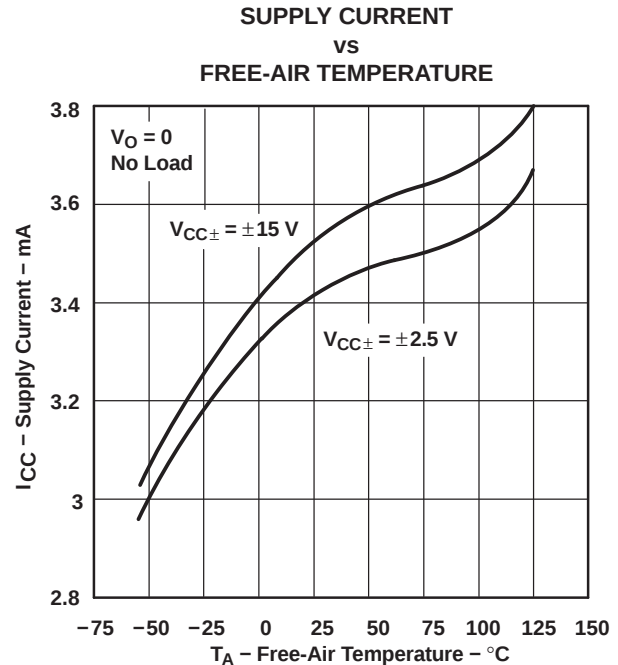


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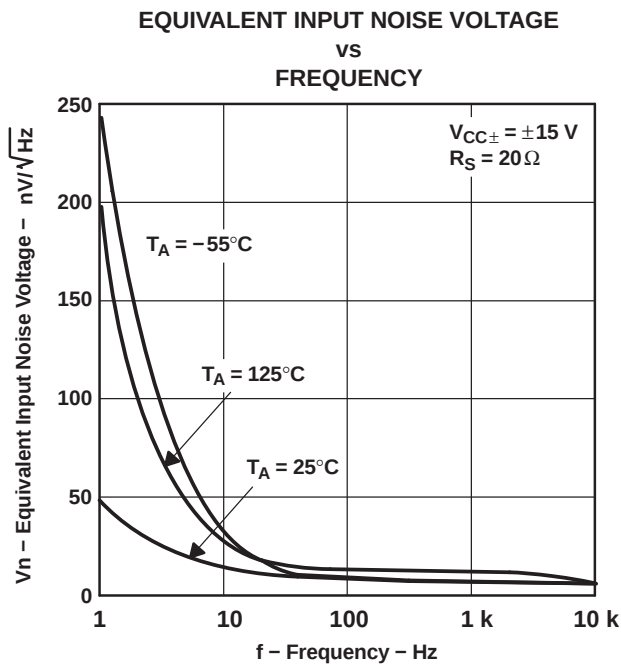


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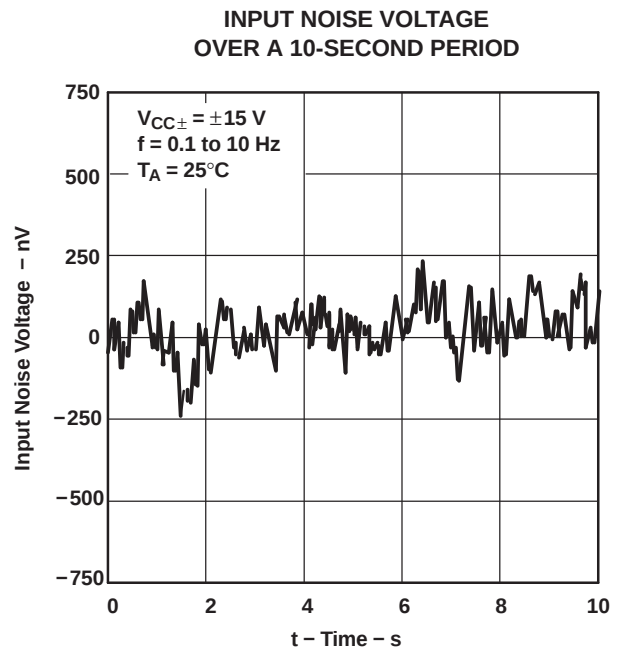


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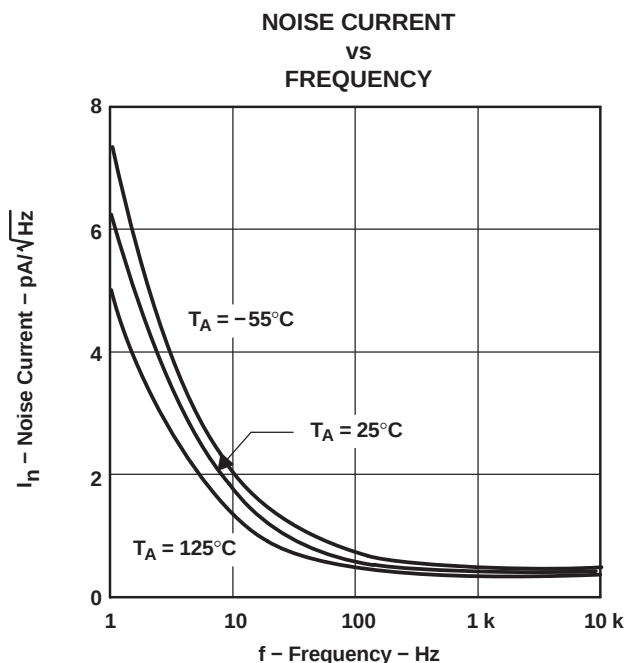


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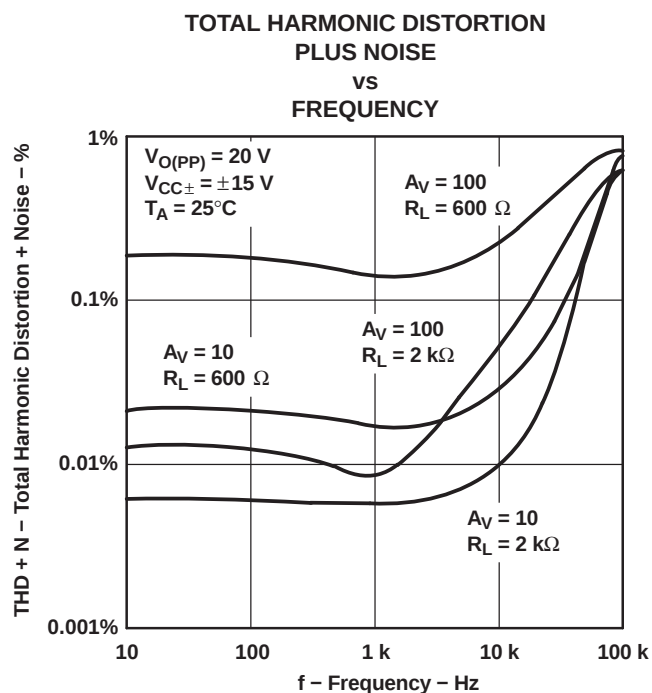


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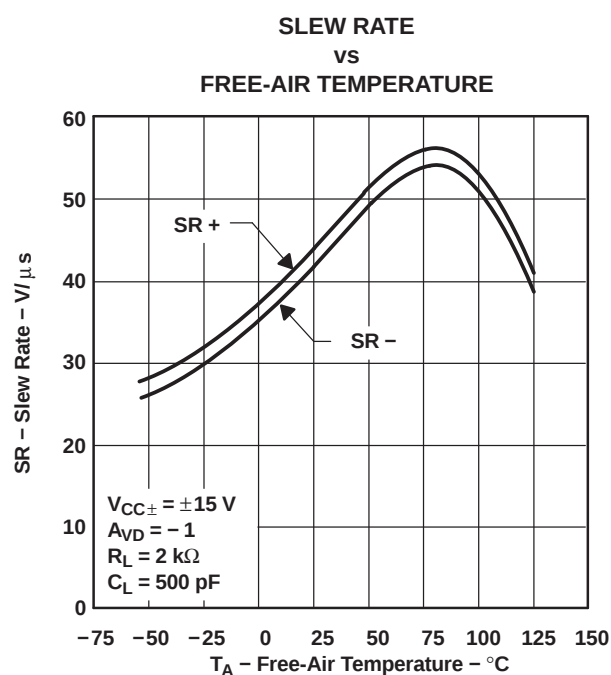


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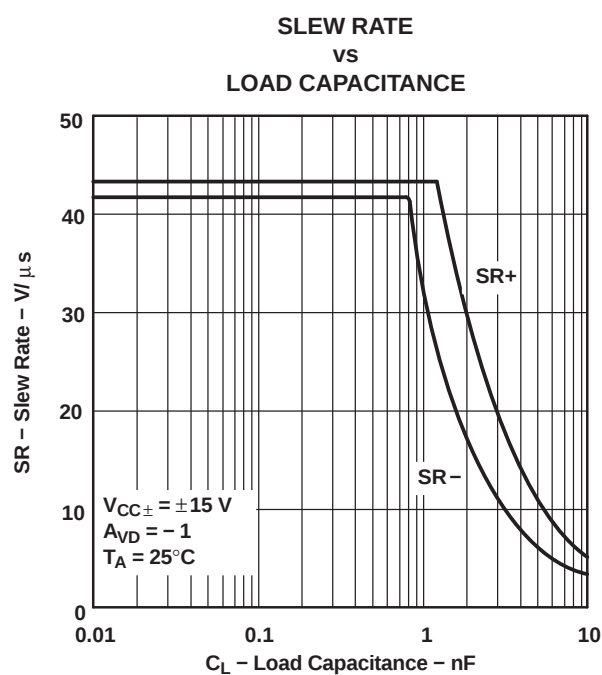
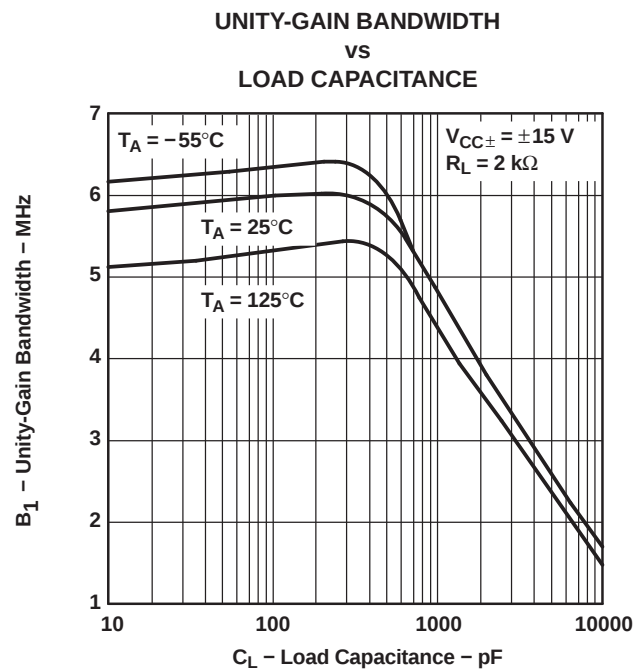
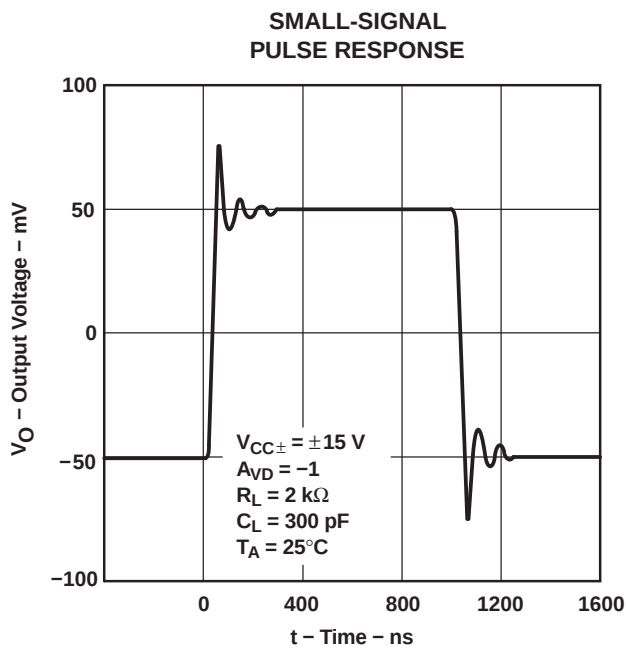
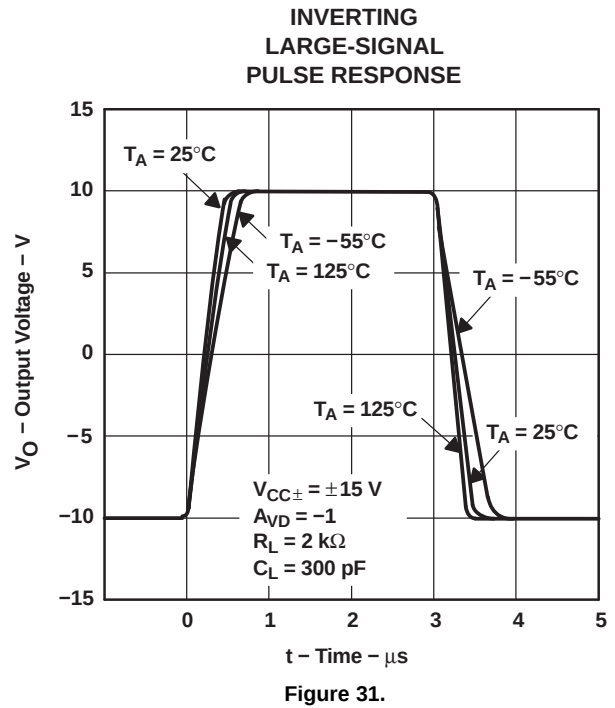
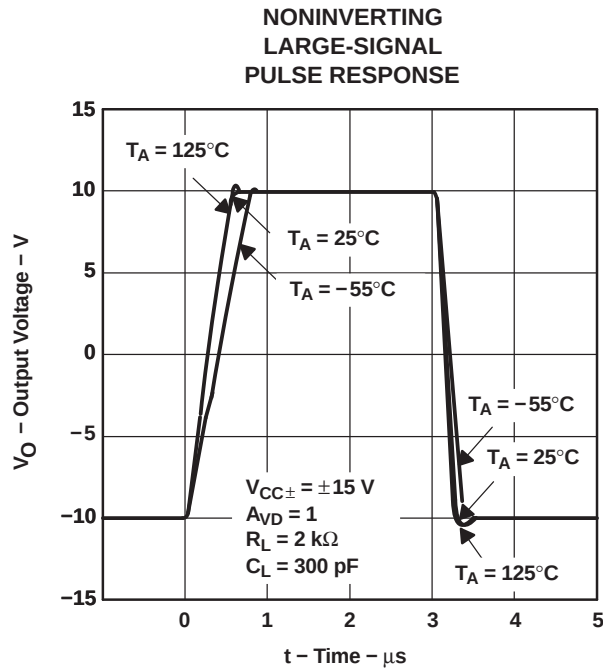


Figure 29.



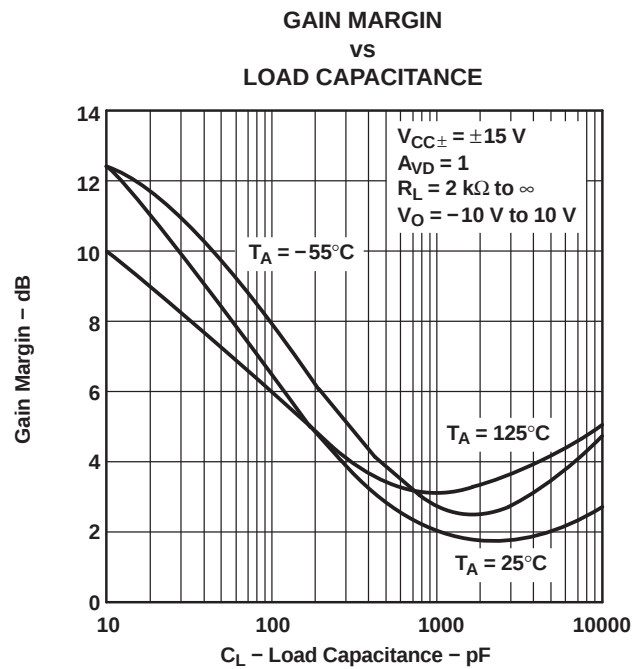


Figure 34.

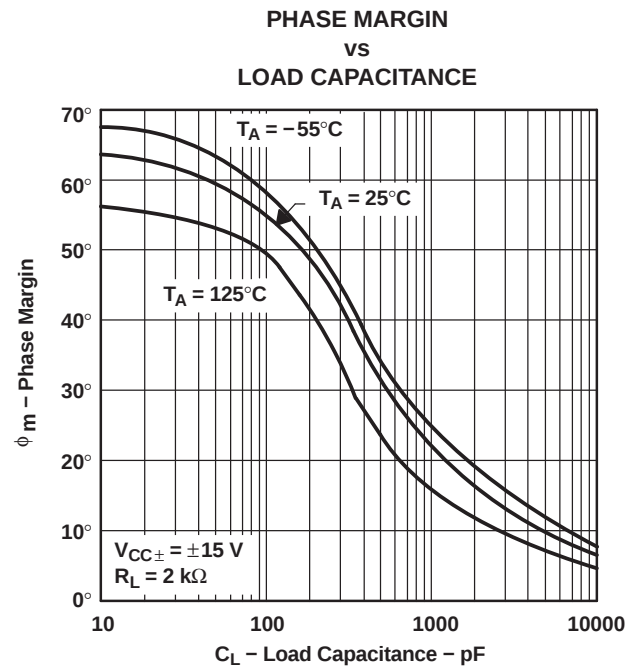


Figure 35.

APPLICATION INFORMATION

Input Offset Voltage Nulling

The TLE2141-Q1 offers external null pins that can be used to further reduce the input offset voltage. If this feature is desired, connect the circuit of [Figure 36](#) as shown. If external nulling is not needed, the null pins may be left unconnected.

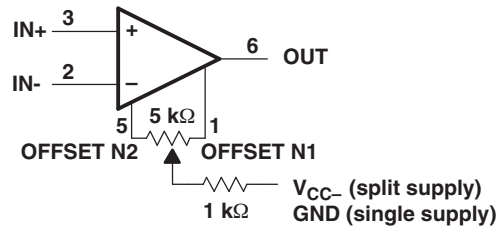


Figure 36. Input Offset Voltage Null Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLE2141QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2141Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TLE2141-Q1 :

- Catalog: [TLE2141](#)

- Enhanced Product: [TLE2141-EP](#)

- Military: [TLE2141M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



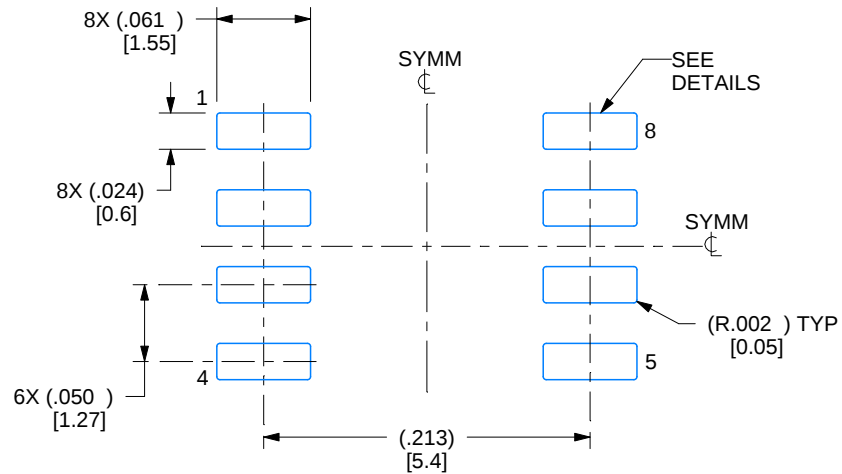
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

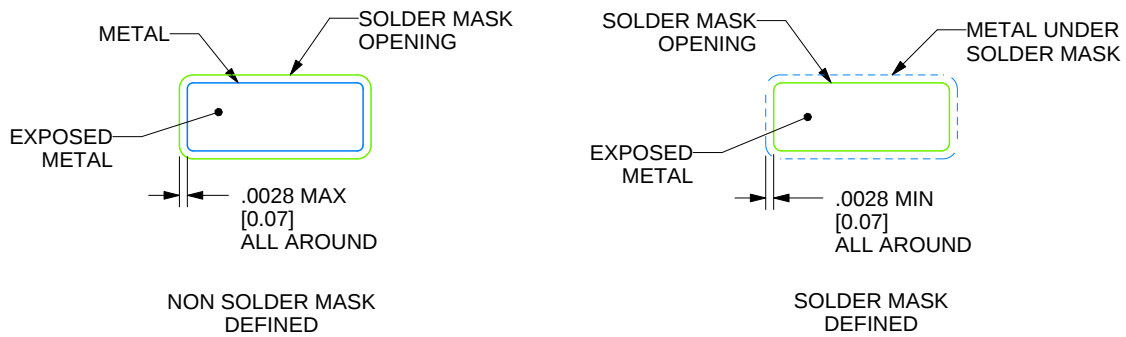
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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