

# 1.1nV/√Hz 噪声、低功耗、精密运算放大器

 查询样品: [OPA2211-HT](#)

## 特性

- 低电压噪声: **1kHz** 时为 **1.1nV/√Hz**
- 输入电压噪声:  
**80nV<sub>PP</sub>** (**0.1Hz** 至 **10Hz**)
- 总谐波失真 (THD)+N: **-136dB** (**G=1**, **f=1kHz**)
- 偏移电压: **350μV** (最大值)
- 偏移电压漂移: **0.35μV/°C** (典型值)
- 低电源电流: 每通道 **6mA** (最大值)
- 单位增益稳定
- 增益带宽产品:  
**80MHz** (**G= 100**)  
**45MHz** (**G= 1**)
- 转换速率: **27V/μs**
- **16** 位稳定时间: **700ns**
- 宽电源范围:  
**±2.25V** 至 **±18V**, 或者 **4.5V** 至 **36V**
- 轨至轨输出
- 输出电流: **30 mA**

## 应用范围

- 潜孔打钻
- 高温环境

## 支持极端温度环境下的应用

- 受控基线
- 一个组装/测试场所
- 一个制造场所
- 可在极端温度范围内 (**-55°C/150°C**) 工作 <sup>(1)</sup>
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性
- 德州仪器 (TI) 高温产品利用高度优化的硅 (芯片) 解决方案, 此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大大地提高性能。

(1) 可定制工作温度范围

## 说明

OPA2211 精密运算放大器用一个电流只有 **3.6mA** 的电源电流实现极低 **1.1nV/√Hz** 噪声密度。这个器件还提供轨到轨输出摆幅, 这大大增加了动态范围。

OPA2211 的极低电压和低电流噪声、高速度、和宽输出摆幅使得这些器件成为锁相环 (PLL) 应用中环路滤波放大器的理想选择。

在精准数据采集应用中, OPA2211 在整个 **10V** 输出摆幅内实现 **16** 位精度所需的稳定时间为 **700ns**。这个交流性能, 与温度范围内只有 **240μV** 的偏移和 **0.35μV/°C** 的漂移组合在一起, 使得 OPA2211 成为驱动高精度 **16** 位模数转换器 (ADC) 或者缓冲高分辨率数模转换器 (DAC) 输出的理想选择。

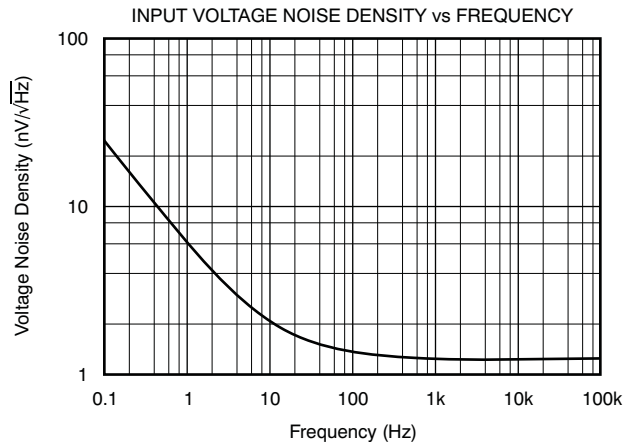
OPA2211 可在 **±2.25V** 至 **±18V** 的宽双电源范围, 或者 **4.5V** 至 **36V** 的单电源范围内运行。

这个运算放大器的额定温度范围  $T_A = -55^{\circ}\text{C}$  至  $150^{\circ}\text{C}$ 。



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**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

$T_J$	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 150°C	PWP	OPA2211SPWP	OP2211S

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

	VALUE	UNIT	
Supply Voltage	$V_S = (V+) - (V-)$	40	V
Input Voltage		$(V-) - 0.5$ to $(V+) + 0.5$	V
Input Current (Any pin except power-supply pins)		$\pm 10$	mA
Output Short-Circuit <sup>(2)</sup>		Continuous	
Storage Temperature, ( $T_S$ )		-65 to +165	°C
Junction Temperature, ( $T_J$ )		-55 to +165	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

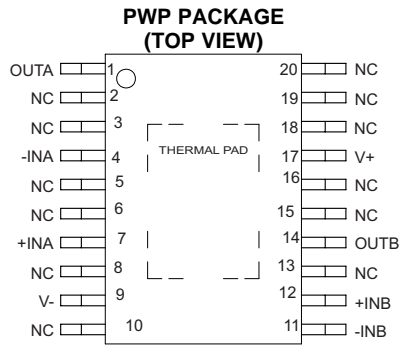
(2) Short-circuit to  $V_S/2$  (ground in symmetrical dual supply setups), one amplifier per package.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		OPA2211-HT		UNITS
		PWP		
		20 PINS		
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	41.2		°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	21.4		
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	23.9		
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	1.1		
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	23.7		
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	1.1		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

### PIN CONFIGURATION



**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 2.25V$  to  $\pm 18V$** 
**BOLDFACE** limits apply over the specified temperature range,  $T_J = -55^\circ\text{C}$  to  $+150^\circ\text{C}$ .

 At  $T_J = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted.

PARAMETER	CONDITIONS	Standard Grade OPA2211			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage	$V_{OS}$ $V_S = \pm 15V$		$\pm 50$	$\pm 175$	$\mu\text{V}$
<b>Over Temperature</b>				$\pm 350$	$\mu\text{V}$
<b>Drift</b>	$dV_{OS}/dT$		<b>0.35</b>		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR $V_S = \pm 2.25V$ to $\pm 18V$		0.1	1	$\mu\text{V}/\text{V}$
<b>Over Temperature</b>				<b>3</b>	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>					
Input Bias Current	$I_B$ $V_{CM} = 0V$		$\pm 60$	$\pm 215$	nA
<b>Over Temperature</b>				<b><math>\pm 350</math></b>	<b>nA</b>
Offset Current	$I_{OS}$ $V_{CM} = 0V$		$\pm 25$	$\pm 120$	nA
<b>Over Temperature</b>				<b><math>\pm 200</math></b>	<b>nA</b>
<b>NOISE</b>					
Input Voltage Noise	$e_n$ $f = 0.1\text{Hz}$ to $10\text{Hz}$		80		$\text{nV}_{PP}$
Input Voltage Noise Density	$f = 10\text{Hz}$		2		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 100\text{Hz}$		1.4		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{kHz}$		1.1		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density	$I_n$ $f = 10\text{Hz}$		3.2		$\text{pA}/\sqrt{\text{Hz}}$
	$f = 1\text{kHz}$		1.7		$\text{pA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range <sup>(1)</sup>	$V_{CM}$ $V_S \geq \pm 5V$	$(V-) + 1.8$		$(V+) - 1.4$	V
	$V_S < \pm 5V$	$(V-) + 2$		$(V+) - 1.4$	V
<b>Common-Mode Rejection Ratio</b>	<b>CMRR</b> $V_S \geq \pm 5V, (V-) + 2V \leq V_{CM} \leq (V+) - 2V$	<b>114</b>	<b>120</b>		<b>dB</b>
	$V_S < \pm 5V, (V-) + 2V \leq V_{CM} \leq (V+) - 2V$	<b>106</b>	<b>120</b>		<b>dB</b>
<b>INPUT IMPEDANCE</b>					
Differential			$20\text{k} \parallel 8$		$\Omega \parallel \text{pF}$
Common-Mode			$10^9 \parallel 2$		$\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>					
<b>Open-Loop Voltage Gain</b>	<b><math>A_{OL}</math></b> $(V-) + 0.2V \leq V_O \leq (V+) - 0.2V,$ $R_L = 10\text{k}\Omega$	<b>114</b>	<b>130</b>		<b>dB</b>
	$A_{OL}$ $(V-) + 0.6V \leq V_O \leq (V+) - 0.6V,$ $R_L = 600\Omega$	110	114		dB
<b>Over Temperature</b>	<b><math>A_{OL}</math></b> $(V-) + 0.6V \leq V_O \leq (V+) - 0.6V,$ $I_O \leq 15\text{mA}$	<b>100</b>			<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW $G = 100$		80		MHz
	$G = 1$		45		MHz
Slew Rate	SR		27		$\text{V}/\mu\text{s}$
Settling Time, 0.01%	$t_S$ $V_S = \pm 15V, G = -1, 10V$ Step, $C_L = 100\text{pF}$		400		ns
0.0015% (16-bit)	$V_S = \pm 15V, G = -1, 10V$ Step, $C_L = 100\text{pF}$		700		ns
Overload Recovery Time	$G = -10$		500		ns
Total Harmonic Distortion + Noise	THD+N $G = +1, f = 1\text{kHz},$ $V_O = 3V_{RMS}, R_L = 600\Omega$		0.000015		%
			-136		dB

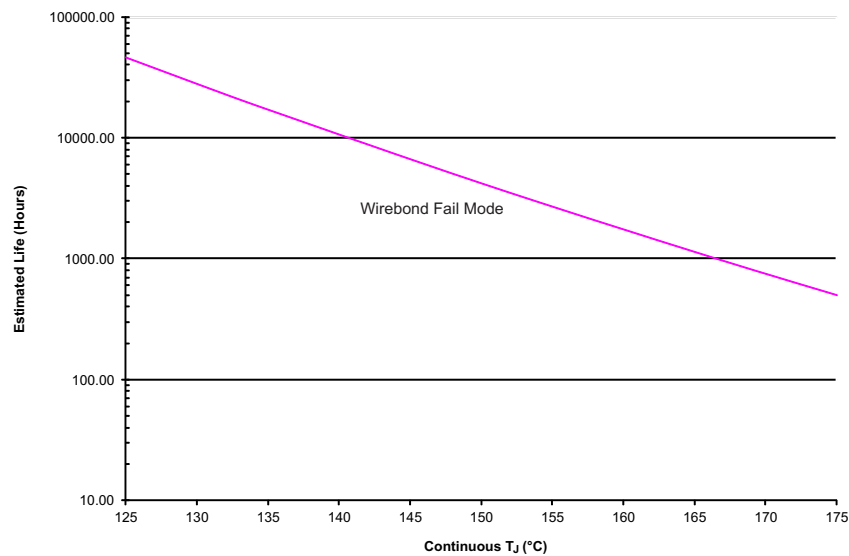
(1) The OPA2211-HT is not intended to be used as a comparator due to its limited differential input range capability. Refer to the [INPUT PROTECTION](#) section of this data sheet.

**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 2.25V$  to  $\pm 18V$  (continued)**

**BOLDFACE** limits apply over the specified temperature range,  $T_J = -55^\circ C$  to  $+150^\circ C$ .

At  $T_J = +25^\circ C$ ,  $R_L = 10k\Omega$  connected to midsupply,  $V_{CM} = V_{OUT} =$  midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	Standard Grade OPA2211			UNIT
		MIN	TYP	MAX	
<b>OUTPUT</b>					
Voltage Output	$V_{OUT}$ $R_L = 10k\Omega, A_{OL} \geq 114dB$ $R_L = 600\Omega, A_{OL} \geq 110dB$ $I_O < 15mA, A_{OL} \geq 100dB$	<b>(V-) + 0.2</b> (V-) + 0.6 <b>(V-) + 0.6</b>		<b>(V+) - 0.2</b> (V+) - 0.6 <b>(V+) - 0.6</b>	<b>V</b> V <b>V</b>
Short-Circuit Current	$I_{SC}$		+30/-45		mA
Capacitive Load Drive	$C_{LOAD}$	See <a href="#">Typical Characteristics</a>			pF
Open-Loop Output Impedance	$Z_O$ f = 1MHz		5		$\Omega$
<b>POWER SUPPLY</b>					
Specified Voltage	$V_S$	<b><math>\pm 2.25</math></b>		<b><math>\pm 18</math></b>	<b>V</b>
Quiescent Current (per channel)	$I_Q$ $I_{OUT} = 0A$		3.6	4.5	mA
<b>Over Temperature</b>				<b>6</b>	<b>mA</b>
<b>TEMPERATURE RANGE</b>					
Specified Range	$T_A$	-55		+150	$^\circ C$
Operating Range	$T_A$	-55		+150	$^\circ C$



- (1) See Datasheet for Absolute Maximum and Minimum Recommended Operating Conditions.
- (2) Silicon operating life design goal is 10 years at  $105^\circ C$  junction temperature (does not include package interconnect life).
- (3) The predicted operating lifetime vs. junction temperature is based on reliability modeling and available qualification data.
- (4) Device is qualified for 1000 hour operation at  $150^\circ C$ . Device is functional at  $175^\circ C$ , but at reduced operating life.

**Figure 1. OPA2211-HT Wirebond Life Derating Chart**

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

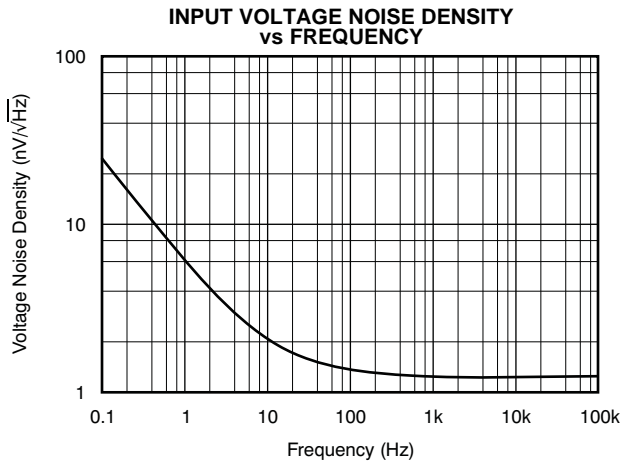


Figure 2.

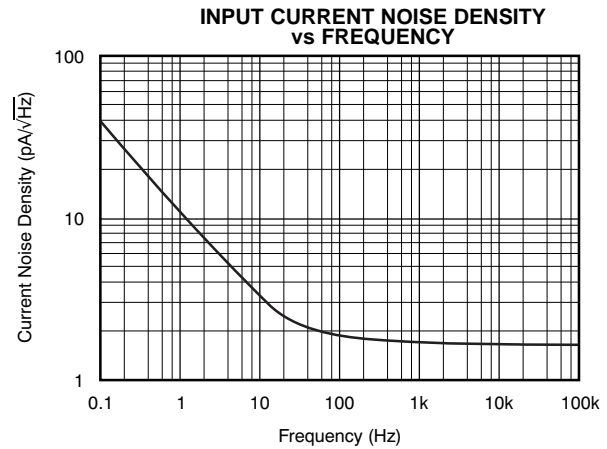


Figure 3.

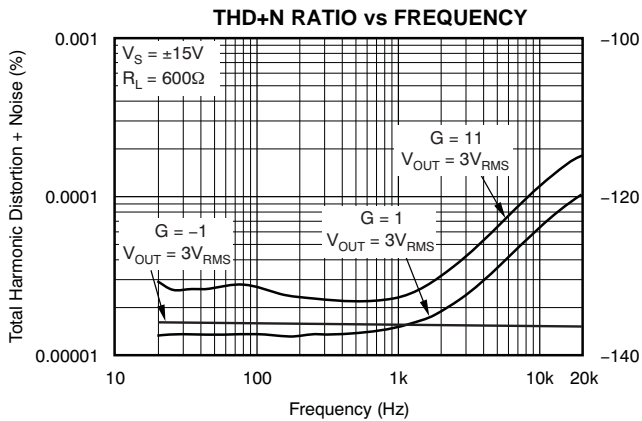


Figure 4.

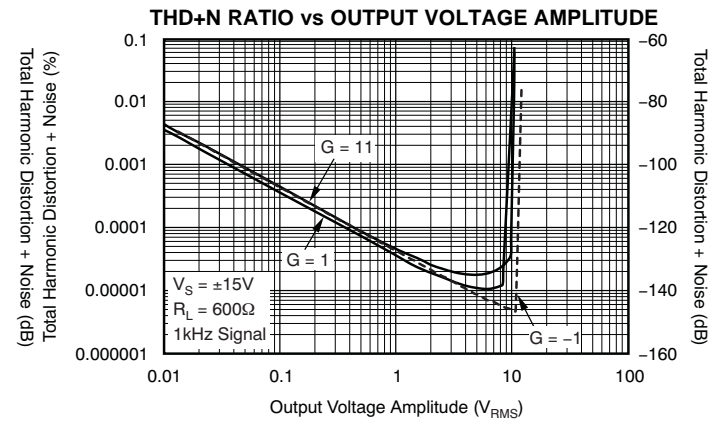


Figure 5.

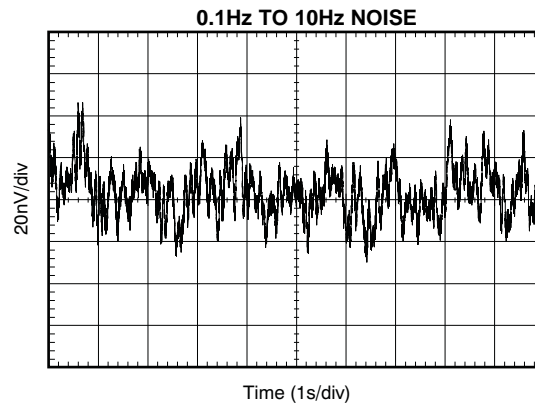
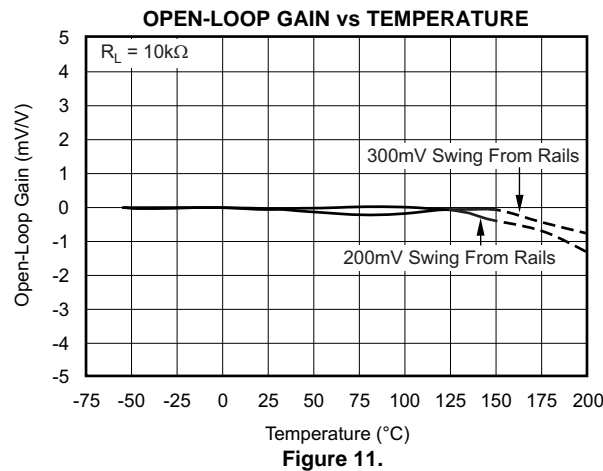
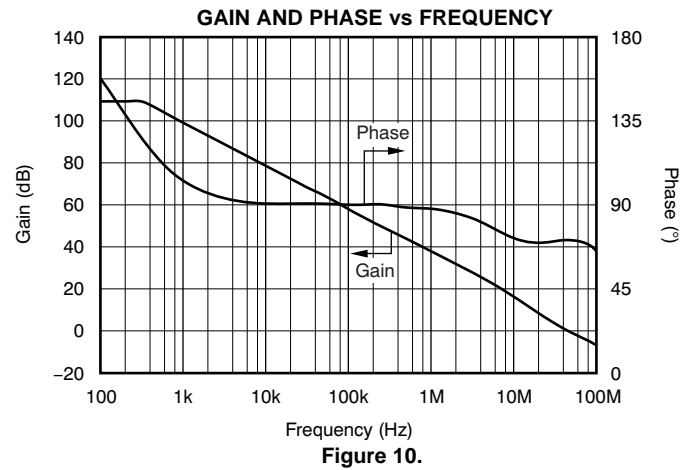
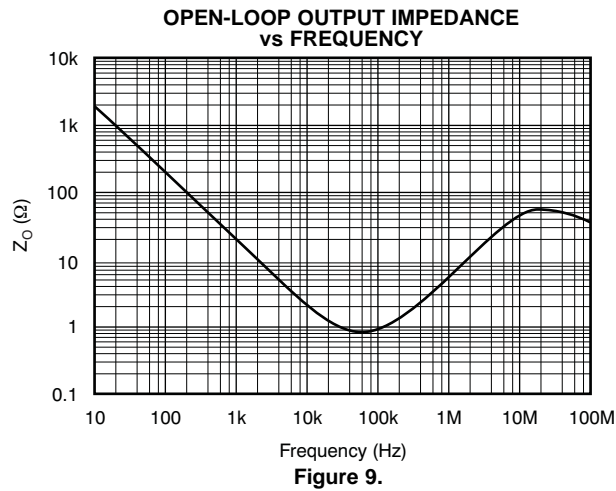
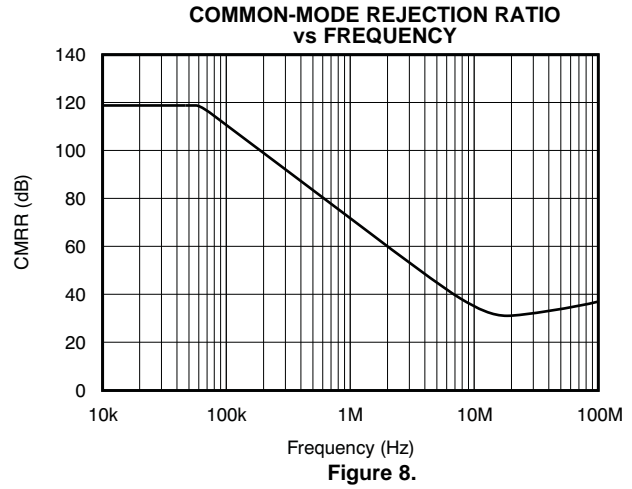
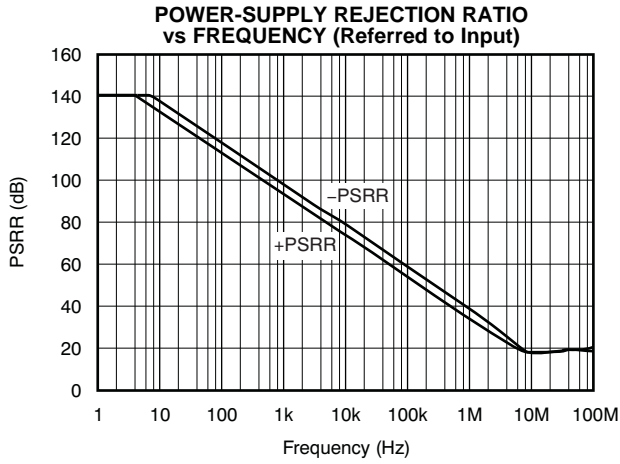


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

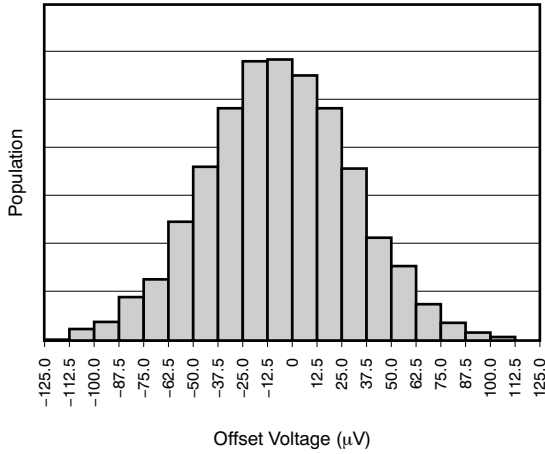
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**

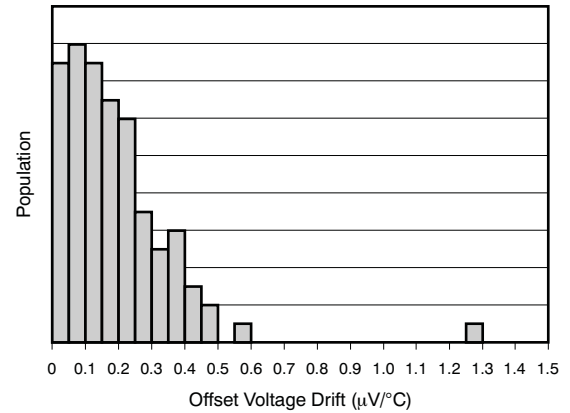
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

**OFFSET VOLTAGE PRODUCTION DISTRIBUTION**



Offset Voltage ( $\mu\text{V}$ )  
Figure 12.

**OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION**



Offset Voltage Drift ( $\mu\text{V}/^\circ\text{C}$ )  
Figure 13.

**$I_B$  AND  $I_{OS}$  CURRENT vs TEMPERATURE**

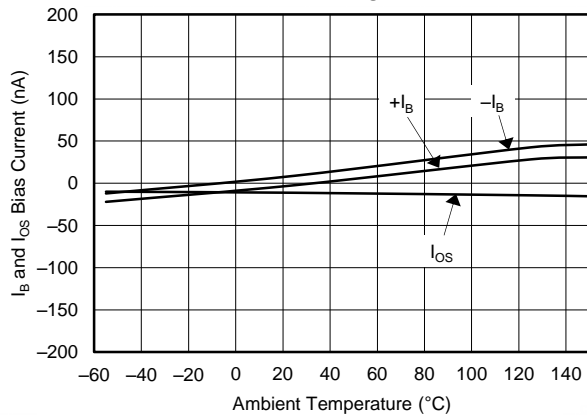


Figure 14.

**OFFSET VOLTAGE vs COMMON-MODE VOLTAGE**

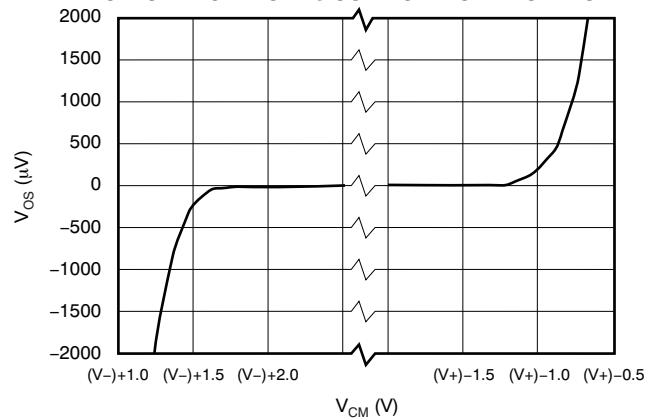


Figure 15.

**$V_{OS}$  WARMUP**

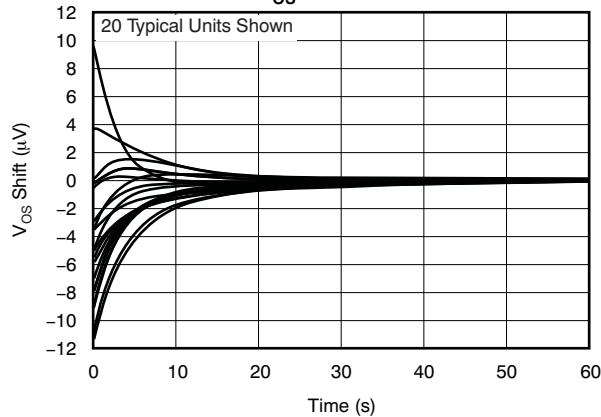


Figure 16.

**INPUT OFFSET CURRENT vs SUPPLY VOLTAGE**

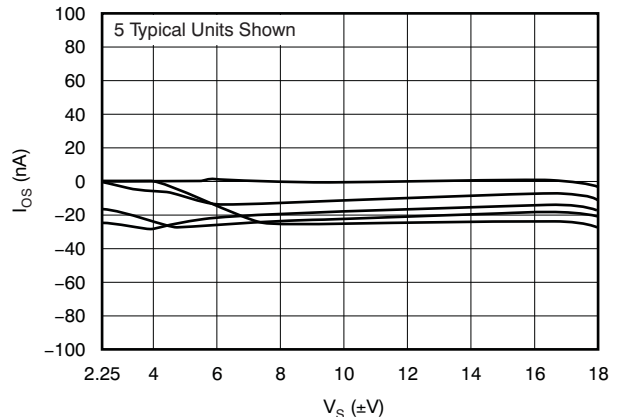


Figure 17.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

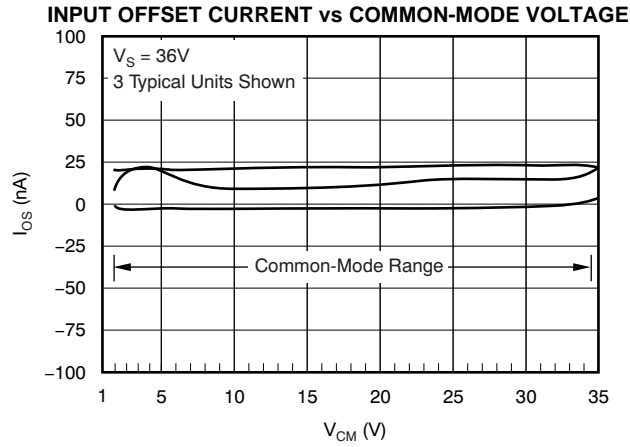


Figure 18.

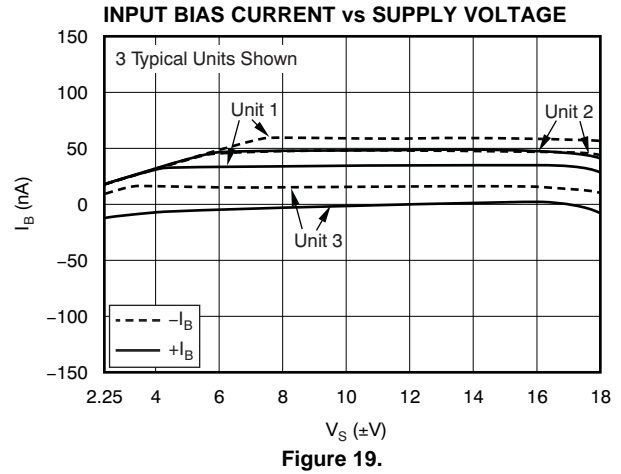


Figure 19.

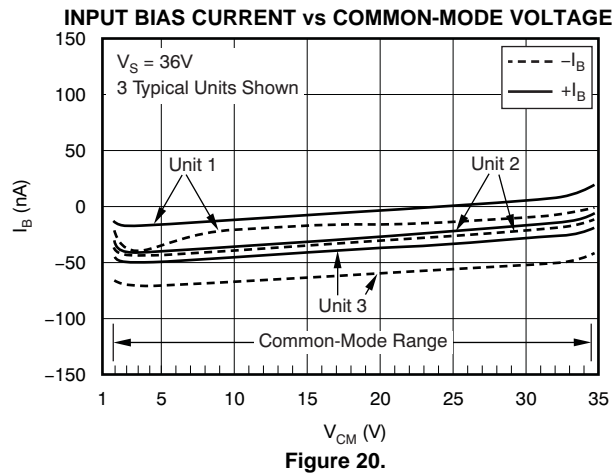


Figure 20.

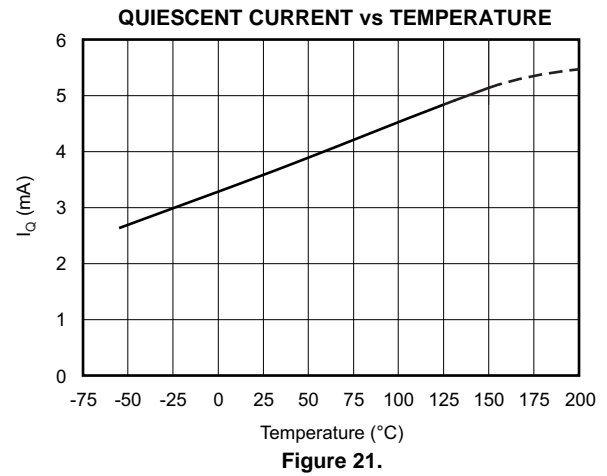


Figure 21.

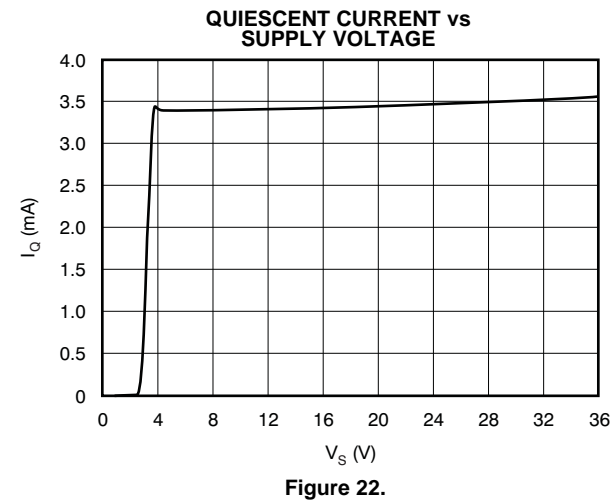


Figure 22.

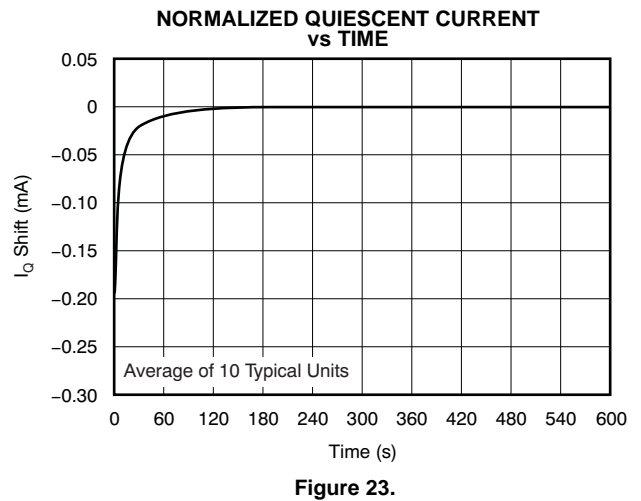
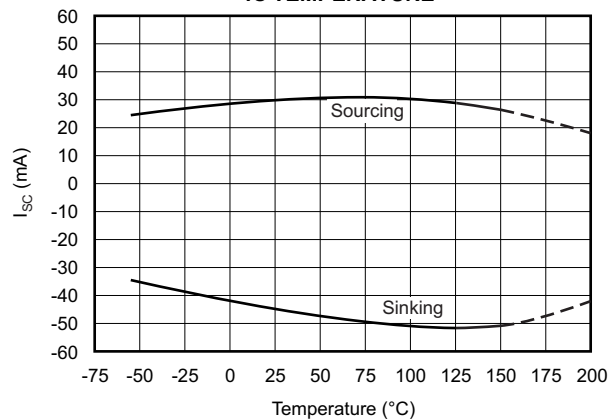


Figure 23.

**TYPICAL CHARACTERISTICS (continued)**

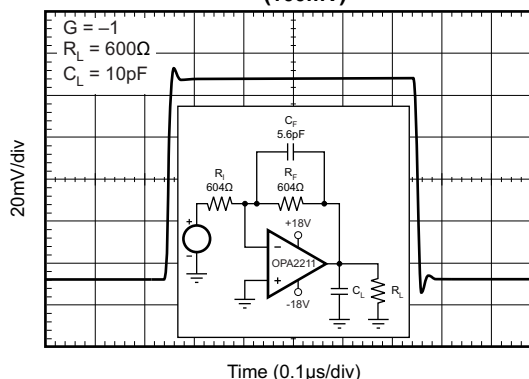
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**



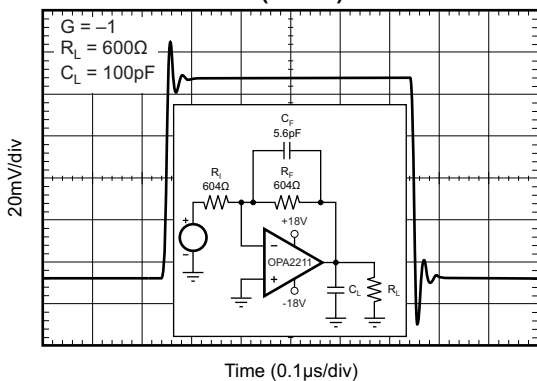
**Figure 24.**

**SMALL-SIGNAL STEP RESPONSE (100mV)**



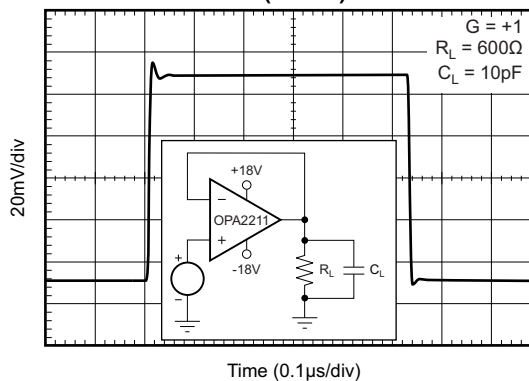
**Figure 25.**

**SMALL-SIGNAL STEP RESPONSE (100mV)**



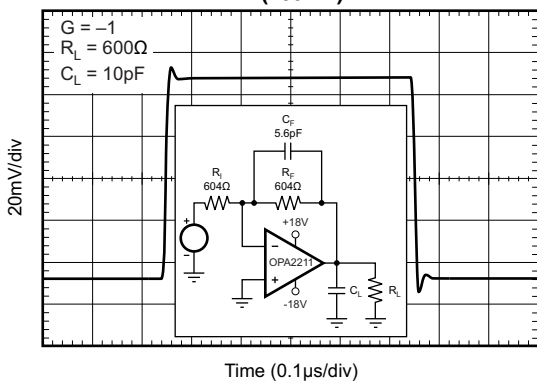
**Figure 26.**

**SMALL-SIGNAL STEP RESPONSE (100mV)**



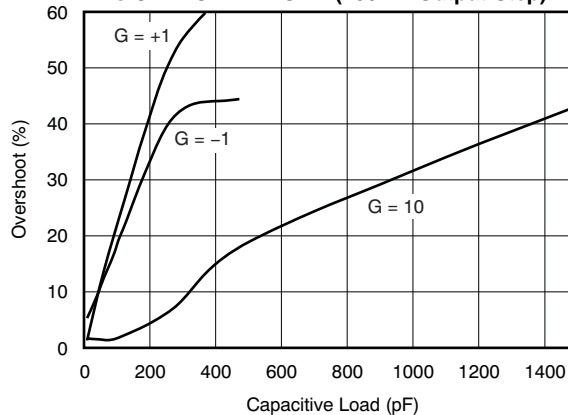
**Figure 27.**

**SMALL-SIGNAL STEP RESPONSE (100mV)**



**Figure 28.**

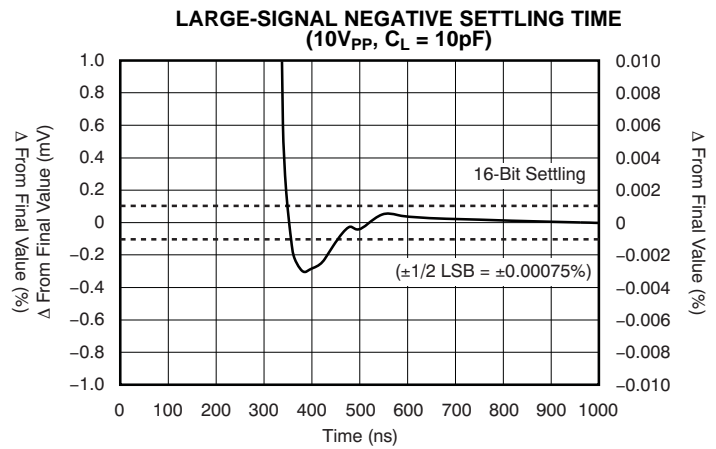
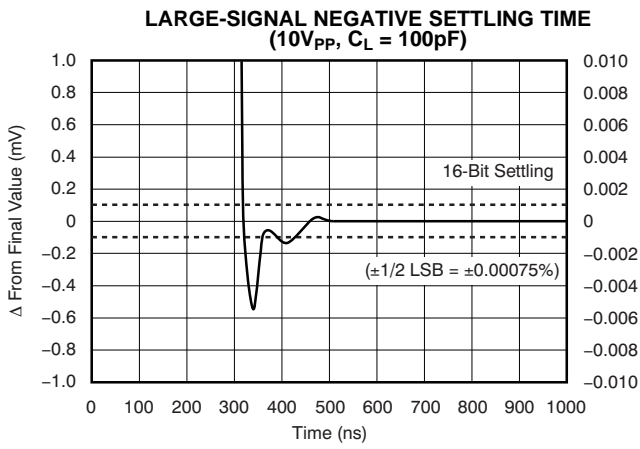
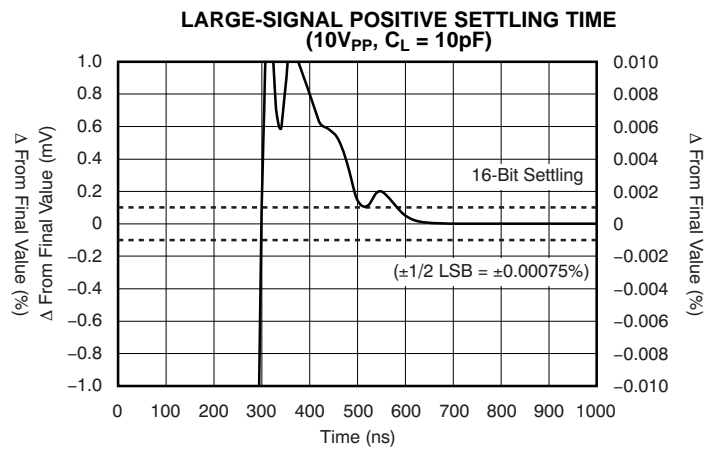
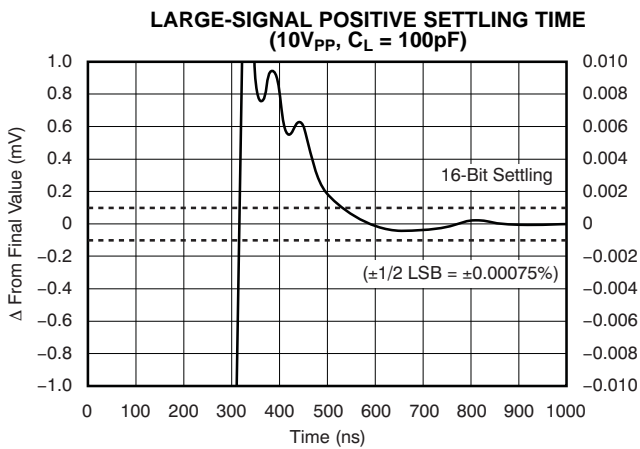
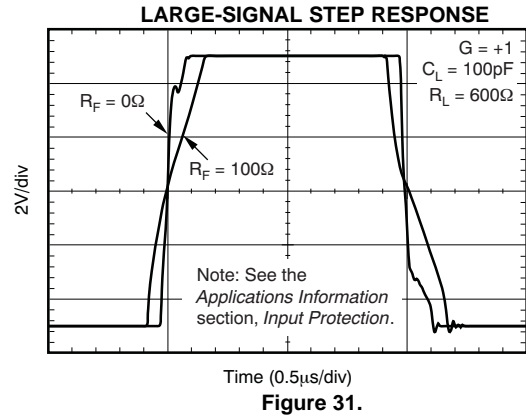
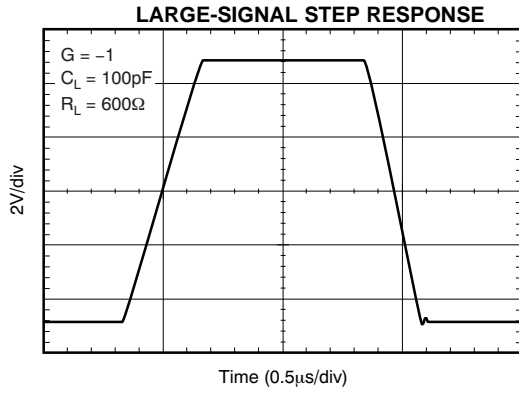
**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)**



**Figure 29.**

**TYPICAL CHARACTERISTICS (continued)**

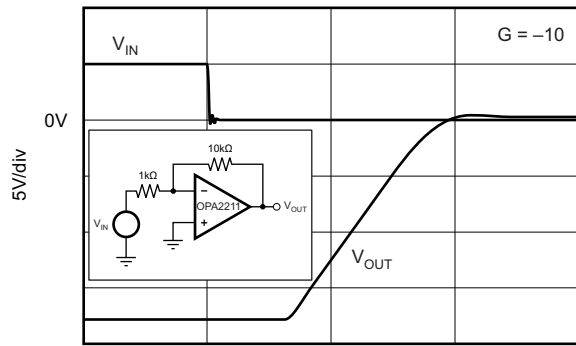
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**

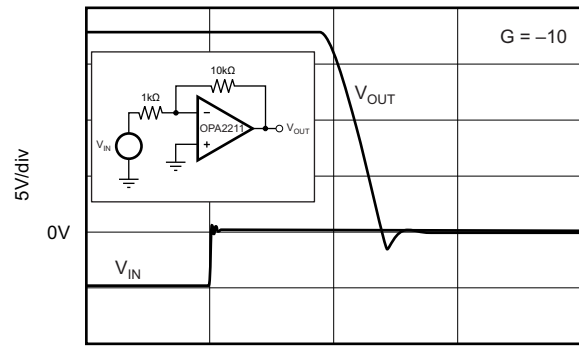
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

**NEGATIVE OVERLOAD RECOVERY**



Time (0.5μs/div)  
Figure 36.

**POSITIVE OVERLOAD RECOVERY**



Time (0.5μs/div)  
Figure 37.

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

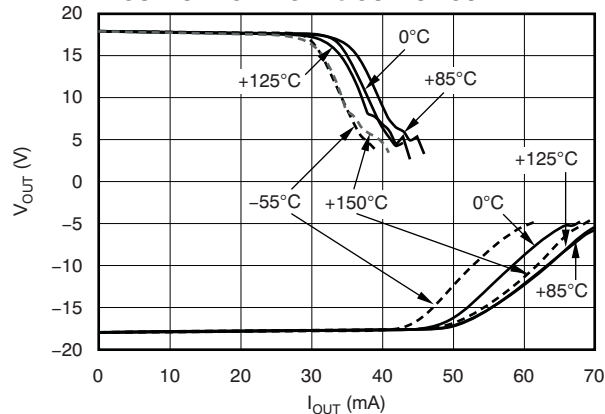


Figure 38.

**NO PHASE REVERSAL**

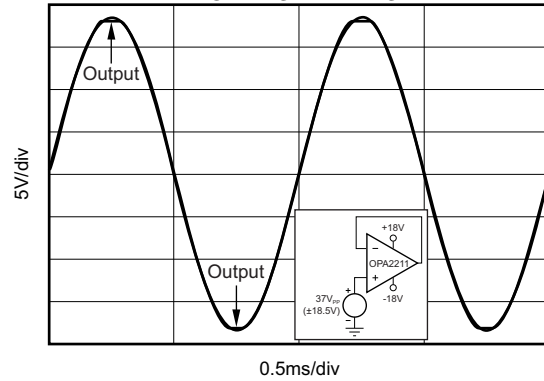


Figure 39.

## APPLICATION INFORMATION

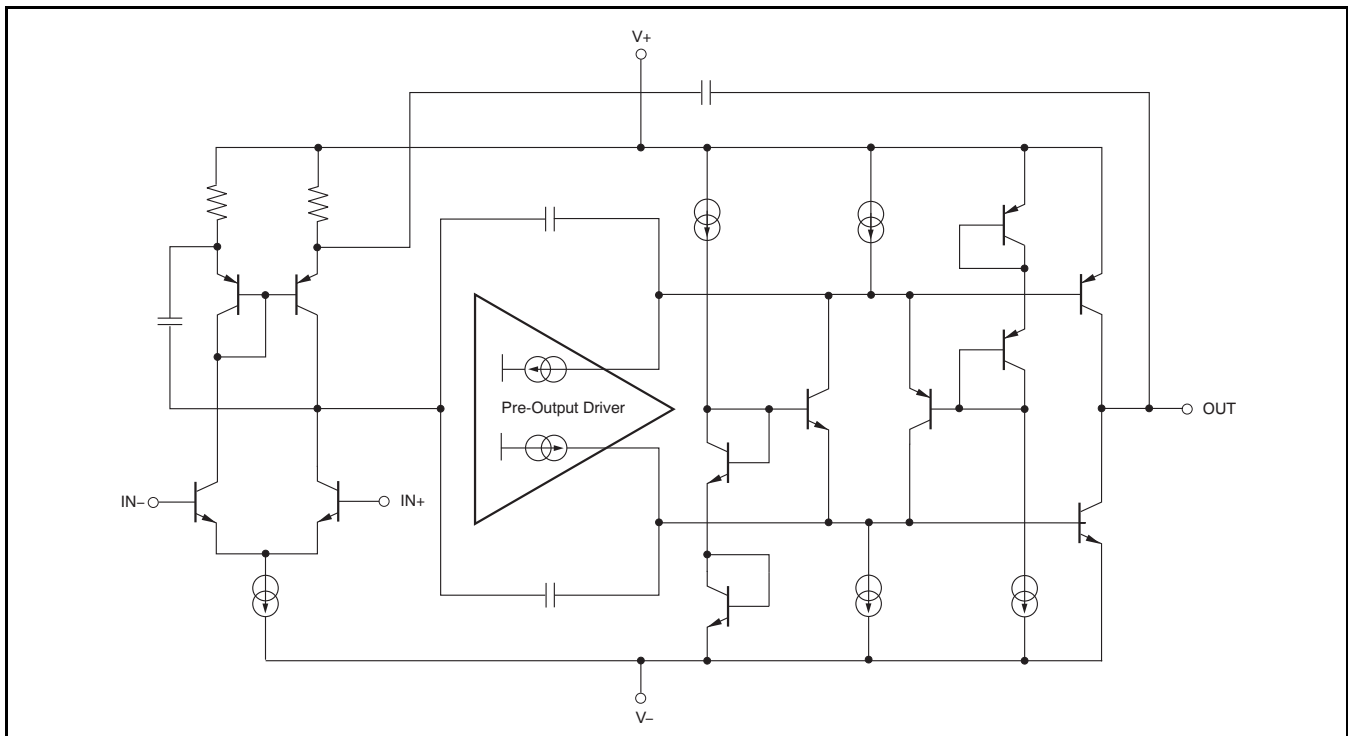
The OPA2211 is a unity-gain stable, precision op amp with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1 $\mu$ F capacitors are adequate. [Figure 40](#) shows a simplified schematic of the OPA2211. This die uses a SiGe bipolar process and contains 180 transistors.

### OPERATING VOLTAGE

OPA2211 series op amps operate from  $\pm 2.25$ V to  $\pm 18$ V supplies while maintaining excellent performance. The OPA2211 series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and

negative output voltage swing. With the OPA2211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at -5V or vice-versa.

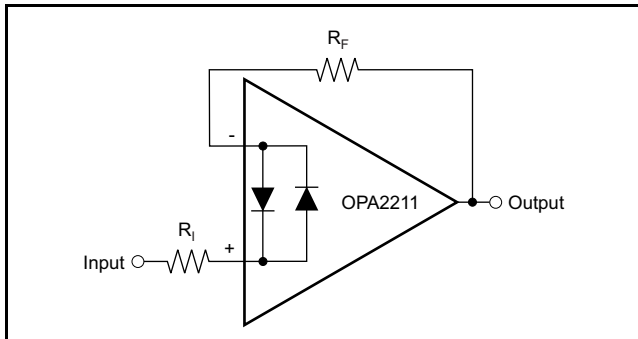
The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range,  $T_j = -55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ . Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#).



**Figure 40. OPA2211 Simplified Schematic**

## INPUT PROTECTION

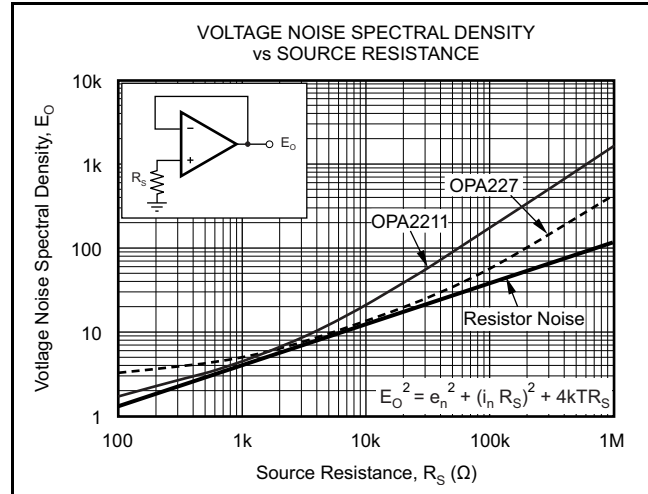
The input terminals of the OPA2211 are protected from excessive differential voltage with back-to-back diodes, as shown in [Figure 41](#). In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or  $G = 1$  circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in [Figure 31](#) of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA2211, and is discussed in the [Noise Performance](#) section of this data sheet. [Figure 41](#) shows an example implementing a current-limiting feedback resistor.



**Figure 41. Pulsed Operation**

## NOISE PERFORMANCE

[Figure 42](#) shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA2211 has very low voltage noise, making it ideal for low source impedances (less than 2k $\Omega$ ). A similar precision op amp, the [OPA227](#), has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10k $\Omega$  to 100k $\Omega$ ). Above 100k $\Omega$ , a FET-input op amp such as the [OPA132](#) (very low current noise) may provide improved performance. The equation in [Figure 42](#) is shown for the calculation of the total circuit noise. Note that  $e_n$  = voltage noise,  $i_n$  = current noise,  $R_S$  = source impedance,  $k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$  J/K, and  $T$  is temperature in K.



**Figure 42. Noise Performance of the OPA2211 and OPA227 in Unity-Gain Buffer Configuration**

## BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in [Figure 42](#). The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

[Figure 42](#) depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

## TOTAL HARMONIC DISTORTION MEASUREMENTS

OPA2211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% ( $G = +1$ ,  $V_O = 3V_{RMS}$ ) throughout the audio frequency range, 20Hz to 20kHz, with a 600Ω load.

The distortion produced by OPA2211 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in can be used to extend the measurement capabilities.

## ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. [Figure 43](#) illustrates the ESD circuits contained in the OPA2211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

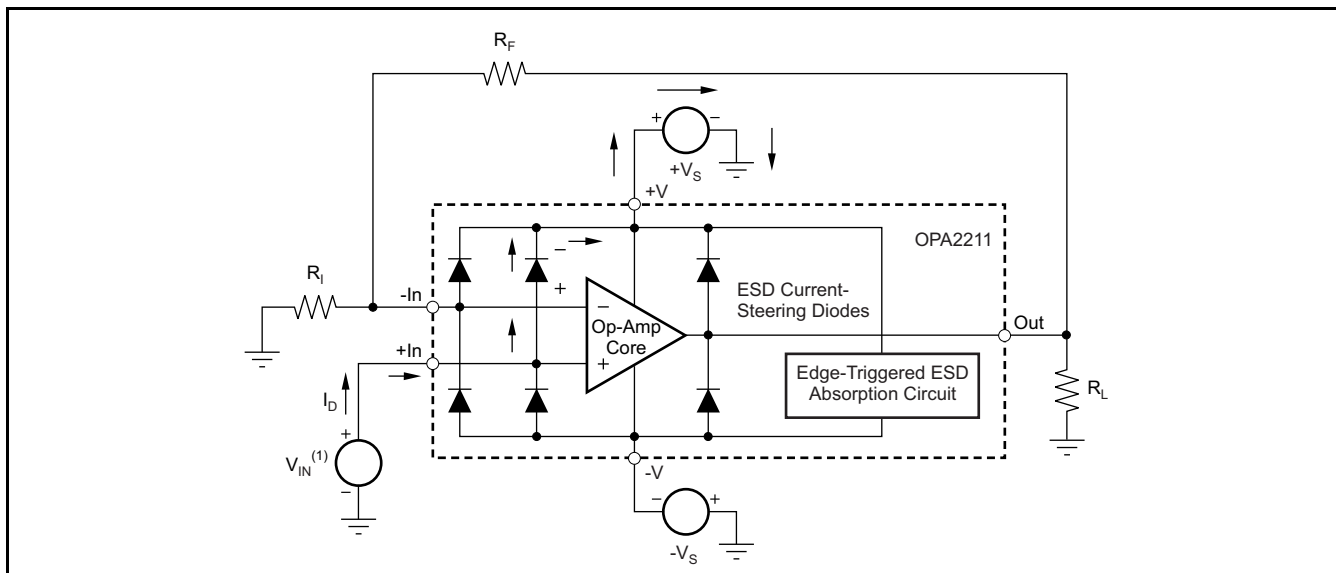
Op amp distortion can be considered an internal error source that can be referred to the input. shows a circuit that causes the op amp distortion to be 101 times greater than that normally produced by the op amp. The addition of  $R_3$  to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without  $R_3$ . The value of  $R_3$  should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in [Figure 43](#), the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1)  $V_{IN} = +V_S + 500\text{mV}$ .

**Figure 43. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application**

Figure 43 depicts a specific example where the input voltage,  $V_{IN}$ , exceeds the positive supply voltage ( $+V_S$ ) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $+V_S$  can sink the current, one of the upper input steering diodes conducts and directs current to  $+V_S$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current,  $V_{IN}$  may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while  $+V_S$  and  $-V_S$  are applied. If this event happens, a

direct current path is established between the  $+V_S$  and  $-V_S$  supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies  $+V_S$  and/or  $-V_S$  are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2211SPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 150	OP2211S	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

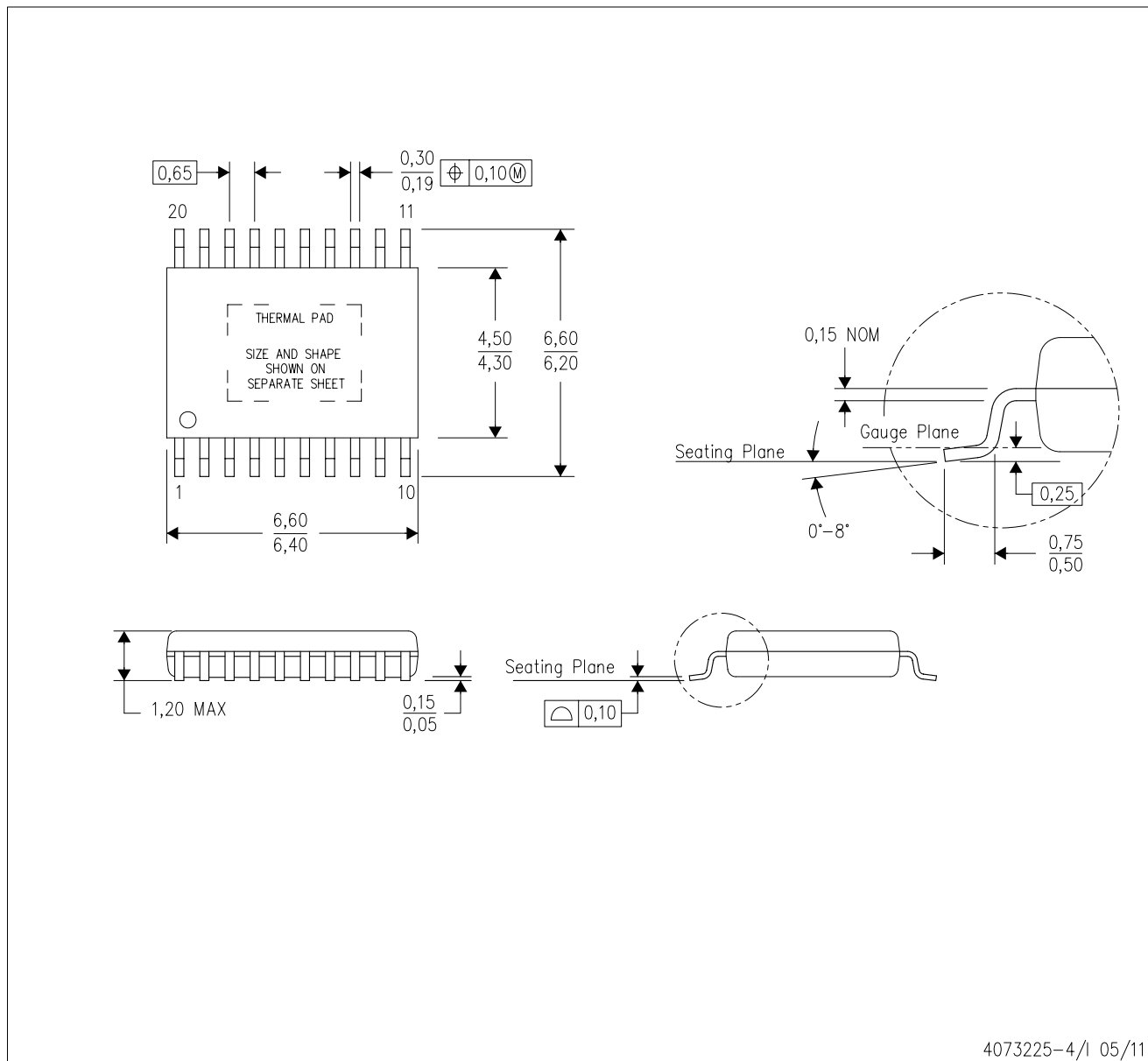
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# MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

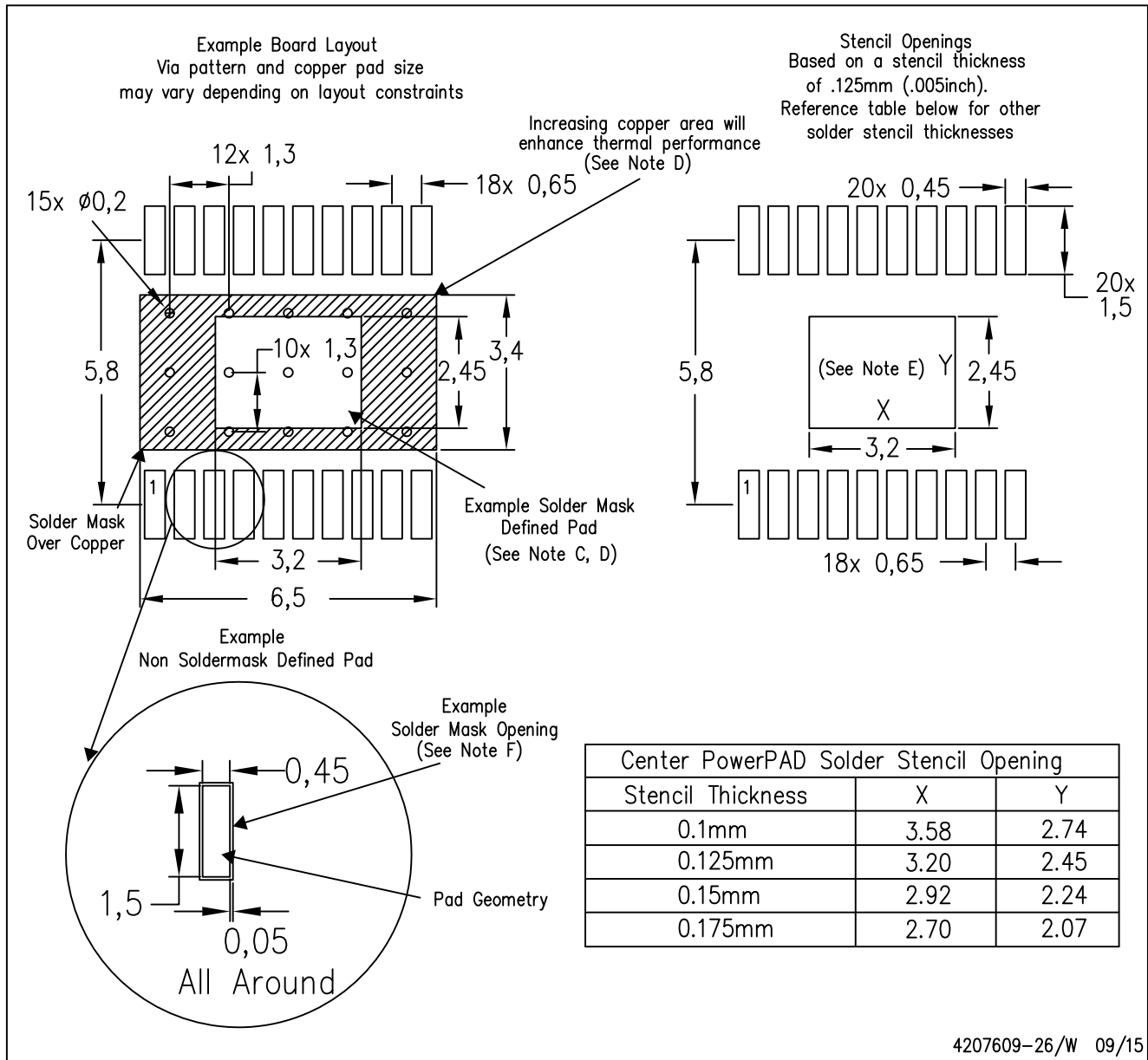
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
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电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com.cn/omap">www.ti.com.cn/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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