

OPA4277-EP 高精度运算放大器

1 特性

- 超低偏移电压：10 μ V
- 超低漂移： $\pm 0.1\mu$ V/ $^{\circ}$ C
- 高开环增益：134dB
- 高共模抑制比：140dB
- 高电源抑制比：130dB
- 低偏置电流：1nA（最大值）
- 宽电源电压范围： ± 2 V 至 ± 18 V
- 低静态电流：800 μ A/放大器
- 支持国防、航天和医疗应用
 - 受控基线
 - 同一组装和测试场所
 - 同一制造场所
 - 支持军用（-55 $^{\circ}$ C 至 125 $^{\circ}$ C）温度范围
 - 延长的产品生命周期
 - 延长的产品变更通知
 - 产品可追溯性

2 应用范围

- 换能器放大器
- 桥式放大器
- 温度测量
- 应变仪放大器
- 精密积分器
- 电池供电仪器
- 测试设备

3 说明

OPA4277-EP 高精度运算放大器取代了行业标准的 OP-177。此器件改进了噪声性能，具有更宽的输出电压摆幅，并且在使静态电流减半的同时将速度提升了一倍。其具有诸多特性，其中包括超低的偏移电压、超低漂移、低偏置电流、高共模抑制比及高电源抑制比。

OPA4277-EP 由 ± 2 V 至 ± 18 V 电源供电运行，性能出色。大多数运算放大器仅有一个指定的电源电压，而 OPA4277-EP 高精度运算放大器有所不同，其电源电压取决于实际应用；唯一的限制条件是电源电压在 ± 5 V 至 ± 15 V 范围内。当放大器输出摆幅达到指定限值时，可保持高性能。由于初始偏移电压非常低（最高 $\pm 20\mu$ V），因此通常无需用户调整。

OPA4277-EP 易于使用，而且不存在其他某些运算放大器中会出现的反相和过载问题。其单位增益稳定，在宽范围负载条件下可保持出色的动态性能。

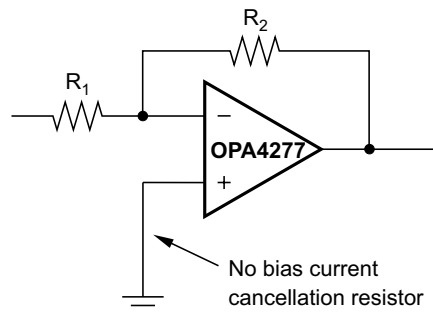
OPA4277-EP 具有完全独立的电路，即便在过驱或过载时也可以实现最低串扰和零交互。

器件信息⁽¹⁾

部件号	封装	封装尺寸（标称值）
OPA4277MDTEP	SOIC (14)	3.91mm \times 8.65mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



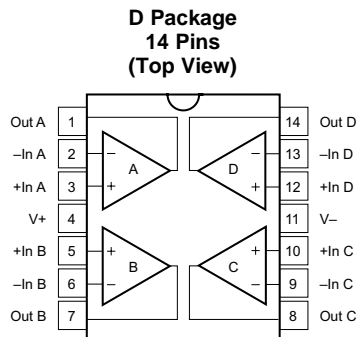
目录

1	特性	1	7.2	Functional Block Diagram	10
2	应用范围	1	7.3	Feature Description	10
3	说明	1	8	Application and Implementation	11
4	修订历史记录	2	8.1	Application Information	11
5	Pin Configuration and Functions	3	8.2	Typical Application	11
6	Specifications	4	9	Power Supply Recommendations	14
6.1	Absolute Maximum Ratings	4	10	Layout	14
6.2	Handling Ratings	4	10.1	Layout Guidelines	14
6.3	Recommended Operating Conditions	4	10.2	Layout Example	15
6.4	Thermal Information	4	11	器件和文档支持	16
6.5	Electrical Characteristics	5	11.1	商标	16
6.6	Typical Characteristics	6	11.2	静电放电警告	16
7	Detailed Description	10	11.3	术语表	16
7.1	Overview	10	12	机械封装和可订购信息	16

4 修订历史记录

日期	修订版本	注释
2014 年 11 月	*	最初发布。

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT A	1	O	Amplifier output A
-IN A	2	I	Inverting amplifier input A
+IN A	3	I	Noninverting amplifier input A
V+	4	P	Positive amplifier power supply input
+IN B	5	I	Noninverting amplifier input B
-IN B	6	I	Inverting amplifier input B
OUT B	7	O	Amplifier output B
OUT C	8	O	Amplifier output C
-IN C	9	I	Inverting amplifier input C
+IN C	10	I	Noninverting amplifier input C
V-	11	P	Negative amplifier power supply input
+IN D	12	I	Noninverting amplifier input D
-IN D	13	I	Inverting amplifier input D
OUT D	14	O	Amplifier output D

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage		36	V
Input voltage	(V-) - 0.7	(V+) + 0.7	V
Output short circuit	Continuous		
Operating temperature	-55	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

	MIN	MAX	UNIT
T _{stg} Storage temperature range	-55	125	°C
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
	Machine model (MM)		
	-2000	2000	
	-100	100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Dual supply voltage	±5	±15	V
T _J Operating junction temperature	-55	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA4277-EP	UNIT
		D (14 PINS)	
R _{θJA}	Junction-to-ambient thermal resistance	66.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	19.3	
R _{θJB}	Junction-to-board thermal resistance	26.8	
ψ _{JT}	Junction-to-top characterization parameter	2.1	
ψ _{JB}	Junction-to-board characterization parameter	26.2	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

At $T_J = 25^\circ\text{C}$, and $R_L = 2\text{ k}\Omega$, $V_S = \pm 5$ to $\pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			± 20	± 65	μV
	Input offset voltage over temperature	$T_J = -55^\circ\text{C}$ to 125°C			± 140	
dV_{OS}/dT	Input offset voltage drift			± 0.15		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage	vs time		0.2		$\mu\text{V}/\text{mo}$
		vs power supply, $V_S = \pm 2$ to $\pm 18\text{ V}$		± 0.3	± 1	$\mu\text{V}/\text{V}$
		$T_J = -55^\circ\text{C}$ to 125°C ; $V_S = \pm 2$ to $\pm 18\text{ V}$				± 1
	Channel separation	dc		0.1		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
I_B	Input bias current			± 0.5	± 2.8	nA
		$T_J = -55^\circ\text{C}$ to 125°C				
I_{OS}	Input offset current			± 0.5	± 2.8	nA
		$T_J = -55^\circ\text{C}$ to 125°C				
NOISE						
	Input voltage noise	$f = 0.1$ to 10 Hz		0.22		μV_{pp}
e_n	Input voltage noise density	$f = 10\text{ Hz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		8		
		$f = 1\text{ kHz}$		8		
		$f = 10\text{ kHz}$		8		
i_n	Current noise density	$f = 1\text{ kHz}$		0.2		$\text{pA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		$(V-) + 2$		$(V+) - 2$	V
CMRR	Common-mode rejection	$V_{CM} = (V-) + 2\text{ V}$ to $(V+) - 2\text{ V}$	115	140		dB
		$T_J = -55^\circ\text{C}$ to 125°C ; $V_{CM} = (V-) + 2\text{ V}$ to $(V+) - 2\text{ V}$	115			
INPUT IMPEDANCE						
	Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
	Common mode	$V_{CM} = (V-) + 2\text{ V}$ to $(V+) - 2\text{ V}$		$250 \parallel 3$		$\text{G}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_O = (V-) + 0.5\text{ V}$ to $(V+) - 1.2\text{ V}$, $R_L = 10\text{ k}\Omega$		140		dB
		$V_O = (V-) + 1.5\text{ V}$ to $(V+) - 1.5\text{ V}$, $R_L = 2\text{ k}\Omega$	126	134		
		$T_J = -55^\circ\text{C}$ to 125°C ; $V_O = (V-) + 1.5\text{ V}$ to $(V+) - 1.5\text{ V}$, $R_L = 2\text{ k}\Omega$	126			
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.8		$\text{V}/\mu\text{s}$
	Setting time	0.1%, $V_S = \pm 15\text{ V}$, $G = 1$, 10-V step		14		μs
		0.01%, $V_S = \pm 15\text{ V}$, $G = 1$, 10-V step		16		
THD + N	Total harmonic distortion + noise	1 kHz, $G = 1$, $V_O = 3.5\text{ V}_{rms}$		0.002%		

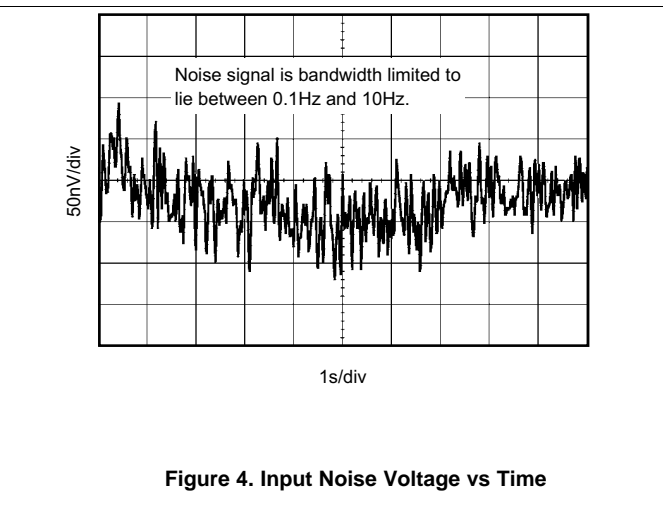
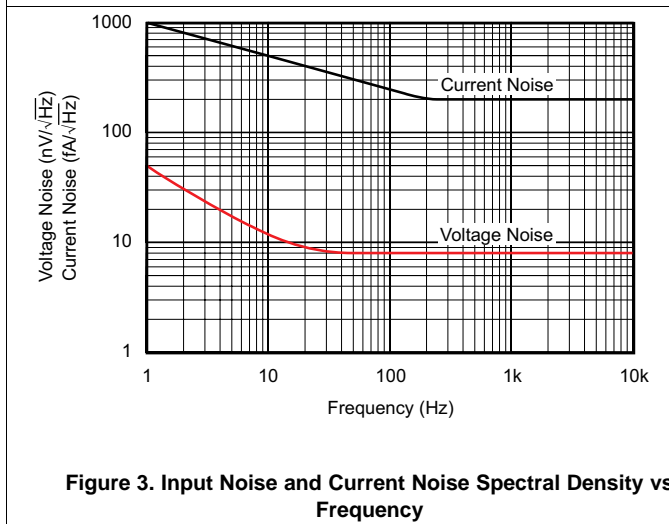
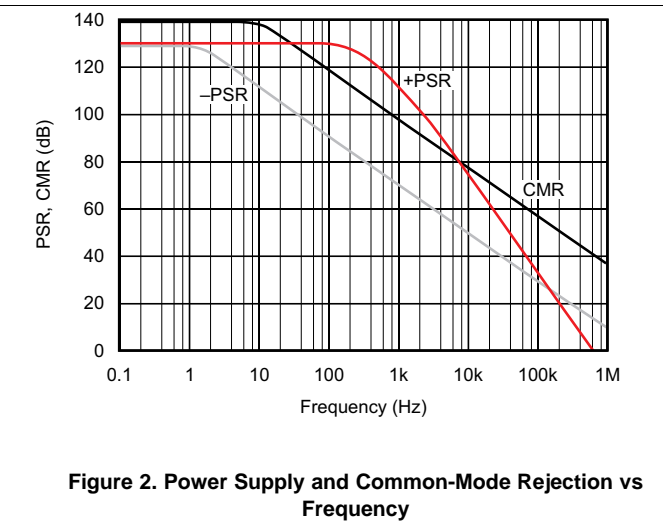
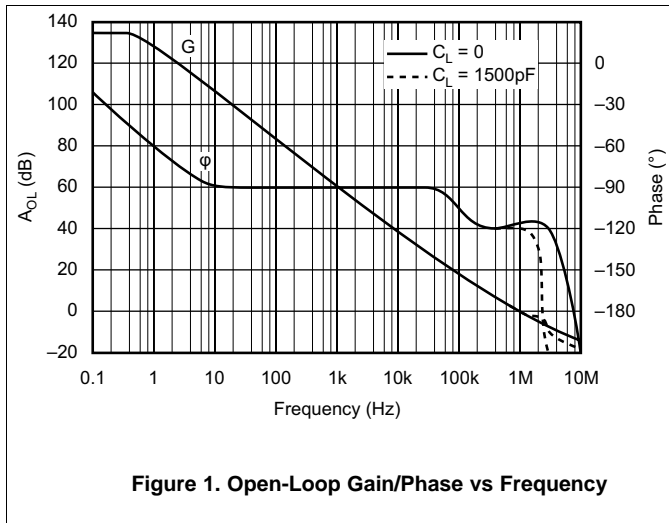
Electrical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, and $R_L = 2\text{ k}\Omega$, $V_S = \pm 5$ to $\pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output	$T_J = -55^\circ\text{C}$ to 125°C ; $R_L = 10\text{ k}\Omega$	$(V_-) + 0.5$		$(V_+) - 1.2$	V
		$T_J = -55^\circ\text{C}$ to 125°C ; $R_L = 2\text{ k}\Omega$	$(V_-) + 1.5$		$(V_+) - 1.5$	
I_{SC}	Short-circuit current			± 35		mA
C_{LOAD}	Capacitive load drive		See Typical Characteristics			
POWER SUPPLY						
V_S	Specified voltage		± 5		± 15	V
	Operating voltage		± 2		± 18	V
I_Q	Quiescent current (per amplifier)	$I_O = 0$		± 790	± 825	μA
		$T_J = -55^\circ\text{C}$ to 125°C ; $I_O = 0$			± 900	

6.6 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, unless otherwise noted.



Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, unless otherwise noted.

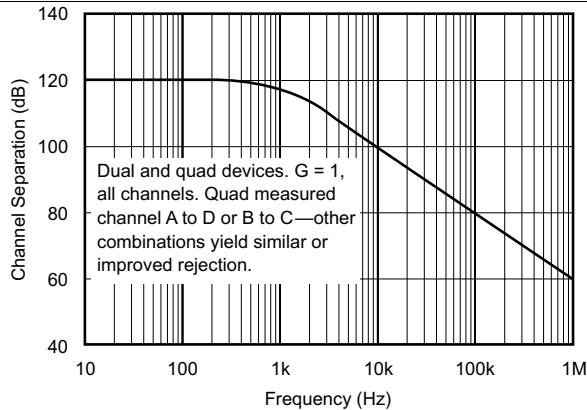
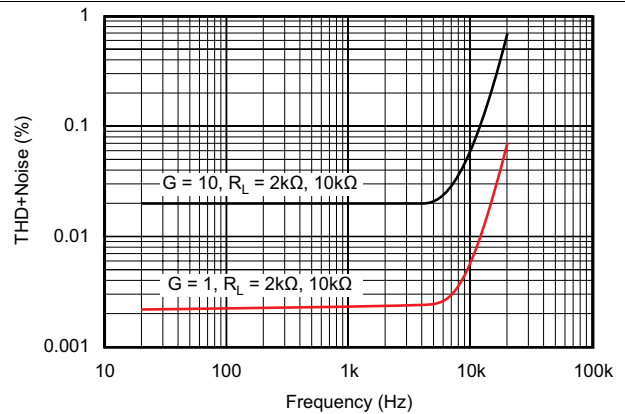


Figure 5. Channel Separation vs Frequency



$V_{OUT} = 3.5\text{ Vrms}$

Figure 6. Total Harmonic Distortion + Noise vs Frequency

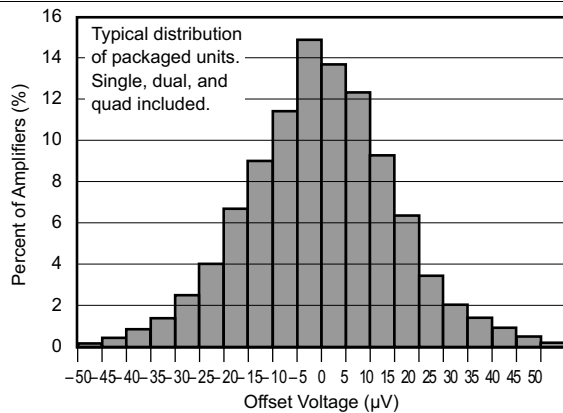


Figure 7. Offset Voltage Production Distribution

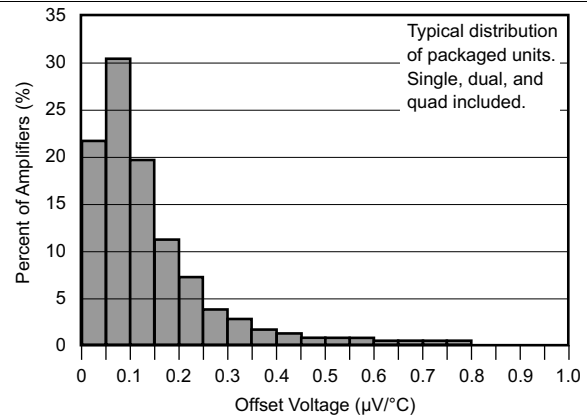


Figure 8. Offset Voltage Drift Production Distribution

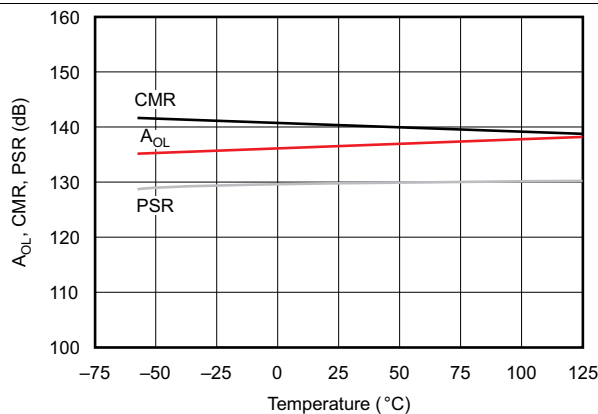


Figure 9. A_{OL} , CMR, PSR vs Temperature

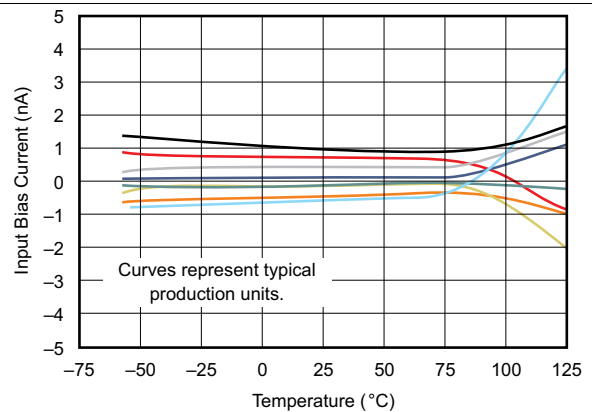


Figure 10. Input Bias Current vs Temperature

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, unless otherwise noted.

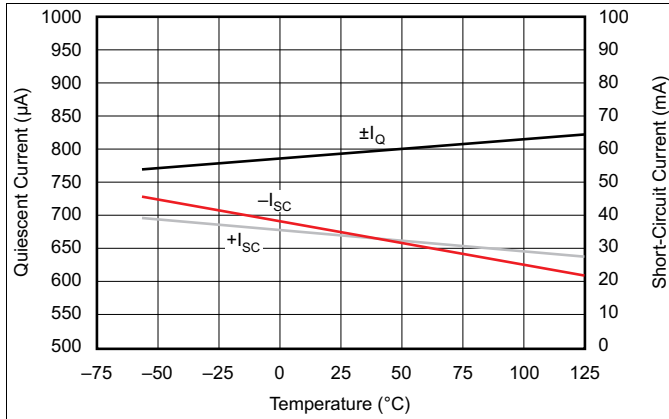


Figure 11. Quiescent Current and Short-Circuit Current vs Temperature

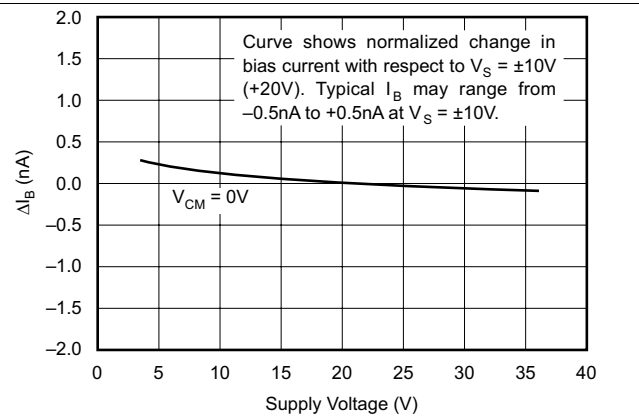


Figure 12. Change in Input Bias Current vs Power Supply Voltage

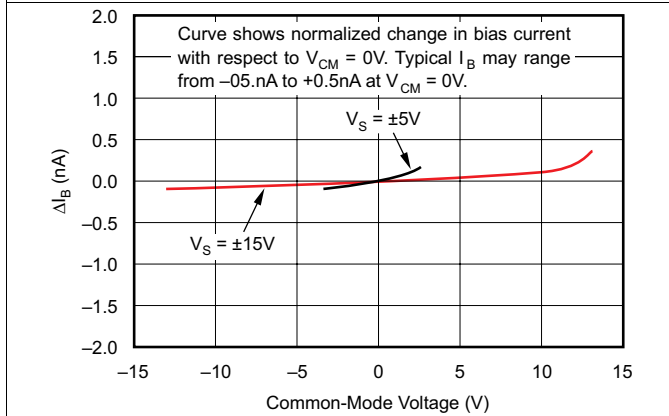


Figure 13. Change in Input Bias Current vs Common-Mode Voltage

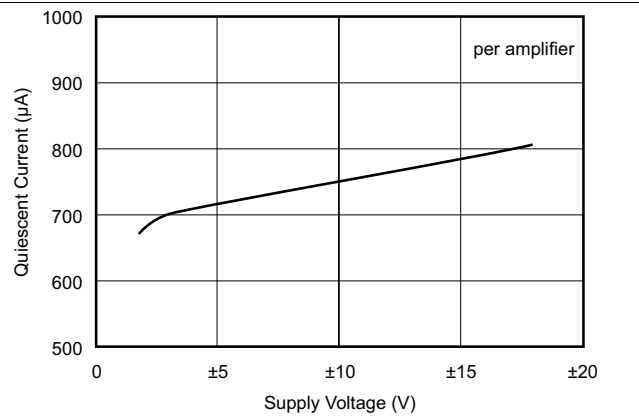


Figure 14. Quiescent Current vs Supply Voltage

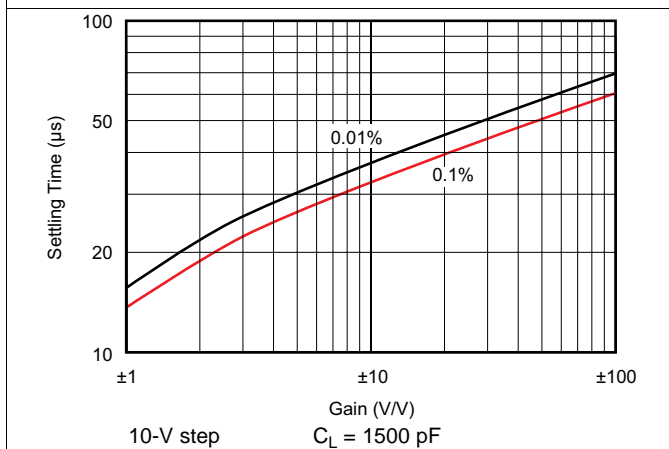


Figure 15. Settling Time vs Closed-Loop Gain

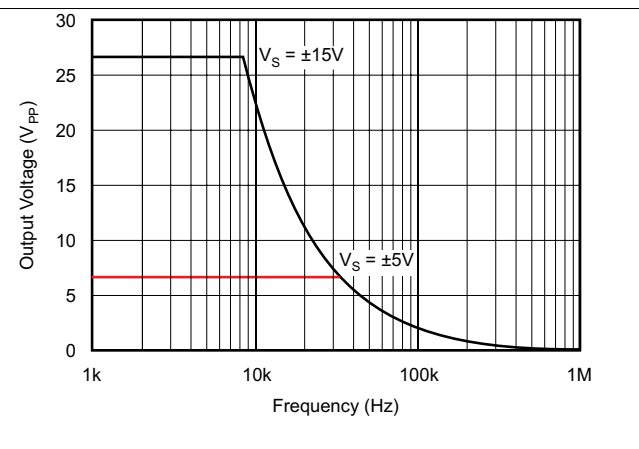


Figure 16. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, unless otherwise noted.

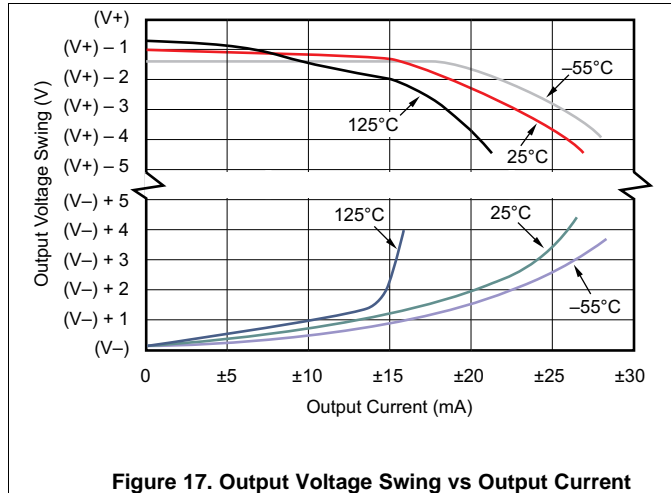


Figure 17. Output Voltage Swing vs Output Current

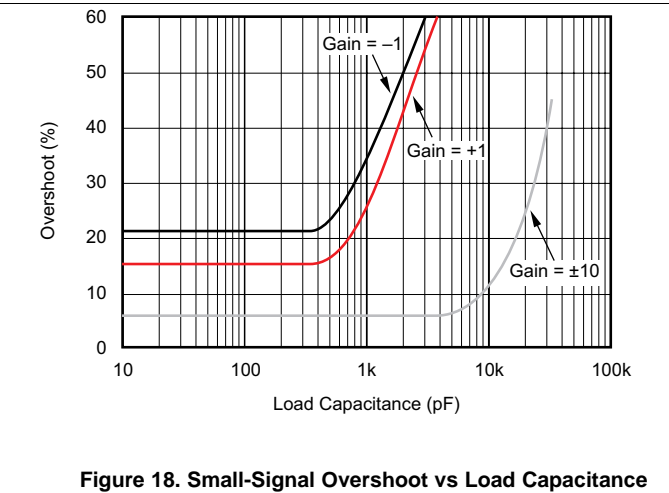


Figure 18. Small-Signal Overshoot vs Load Capacitance

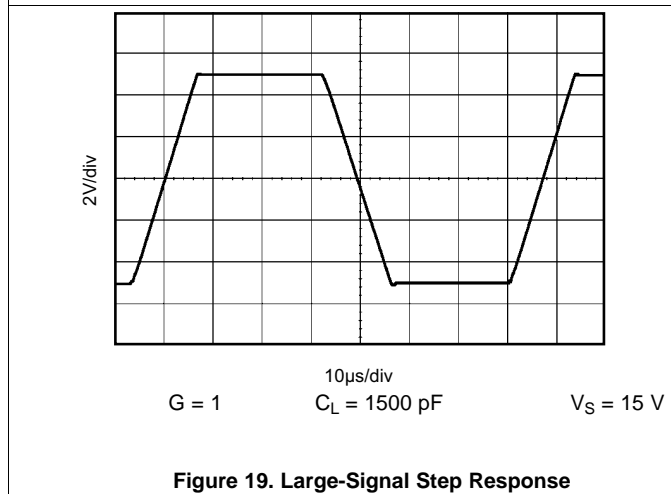


Figure 19. Large-Signal Step Response

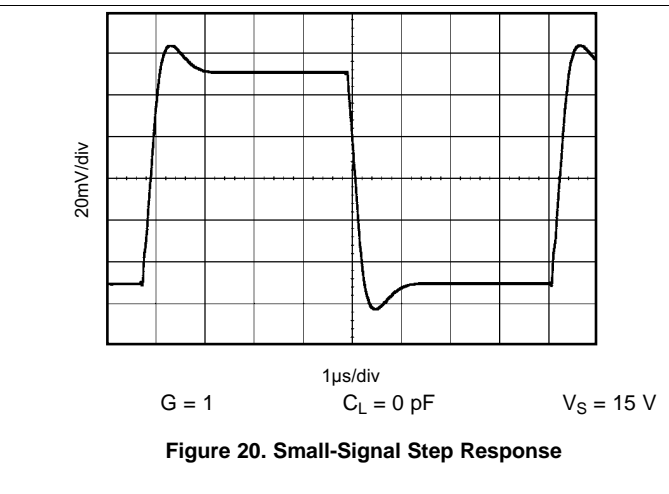


Figure 20. Small-Signal Step Response

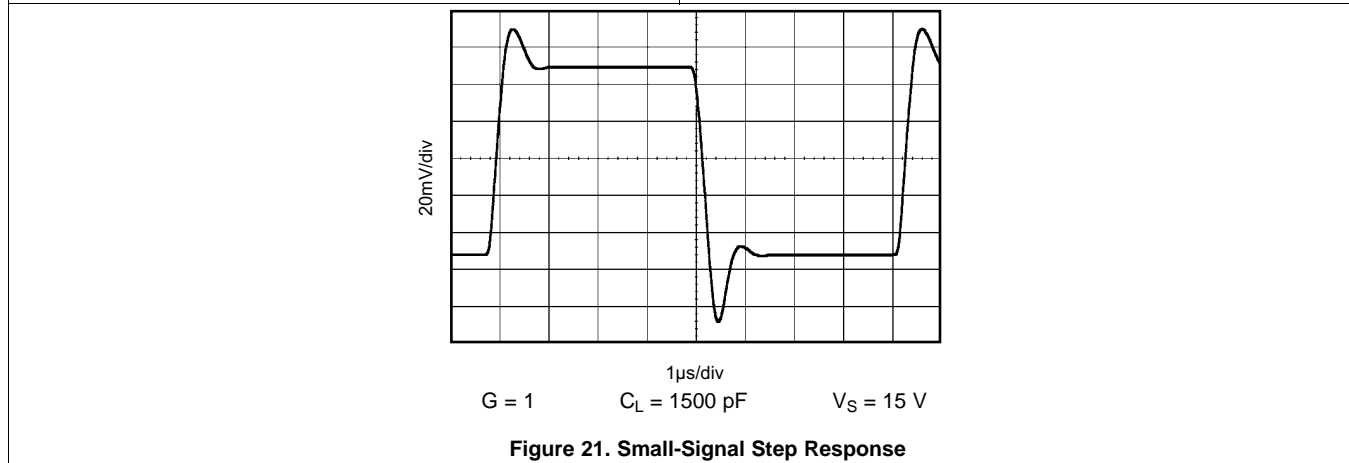


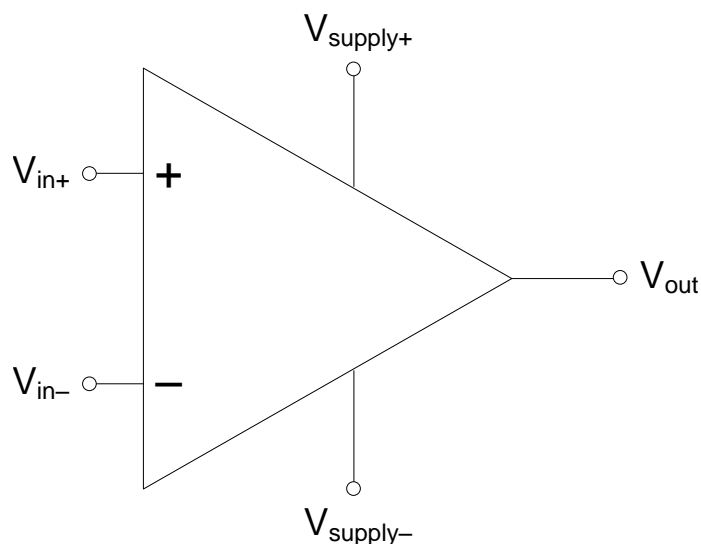
Figure 21. Small-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA4277-EP precision operational amplifier replaces the industry standard OP-177. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA4277-EP operates from ± 2 - to ± 18 -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-EP precision operational amplifier is specified for real-world applications; a single limit applies over the ± 5 - to ± 15 -V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage ($\pm 50 \mu\text{V}$ max) is so low, user adjustment is usually not required.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA4277 is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

8.2 Typical Application

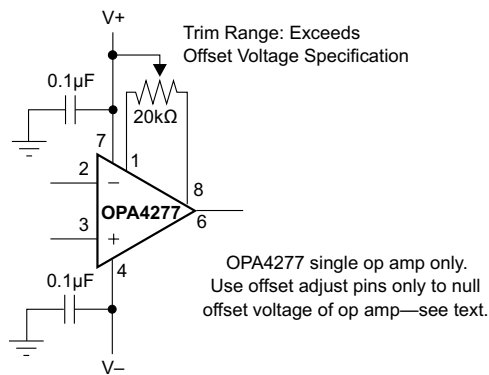


Figure 22. OPA4277 Offset Voltage Trim Circuit

8.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation (see Figure 25), Table 1 lists the design parameters needed with gain = 50.

$$G = 1 + \frac{2R_F}{R} = 50 \quad (1)$$

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_F	10 kΩ
R	412 Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Offset Voltage Adjustment

The OPA27 is laser-trimmed for very-low offset voltage and drift so most circuits do not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. The user can adjust offset voltage by connecting a potentiometer as shown in Figure 22. Only use this adjustment to null the offset of the operational amplifier. This adjustment should not be used to compensate for offsets created elsewhere in a system because this can introduce additional temperature drift.

8.2.2.2 Input Protection

The inputs of the OPA4277 are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

8.2.2.3 Input Bias Current Cancellation

The input stage base current of the OPA4277 is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see [Figure 23](#)). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

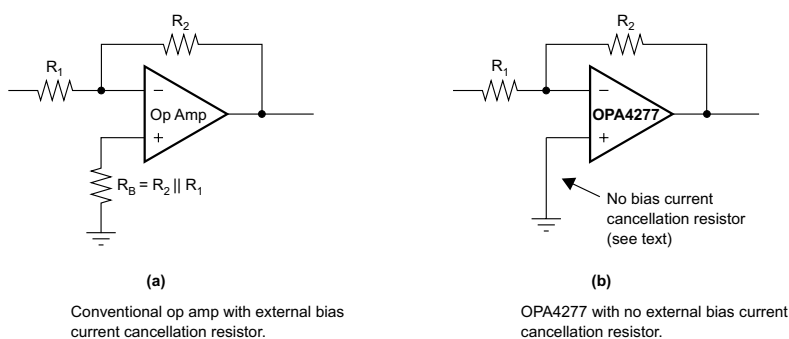
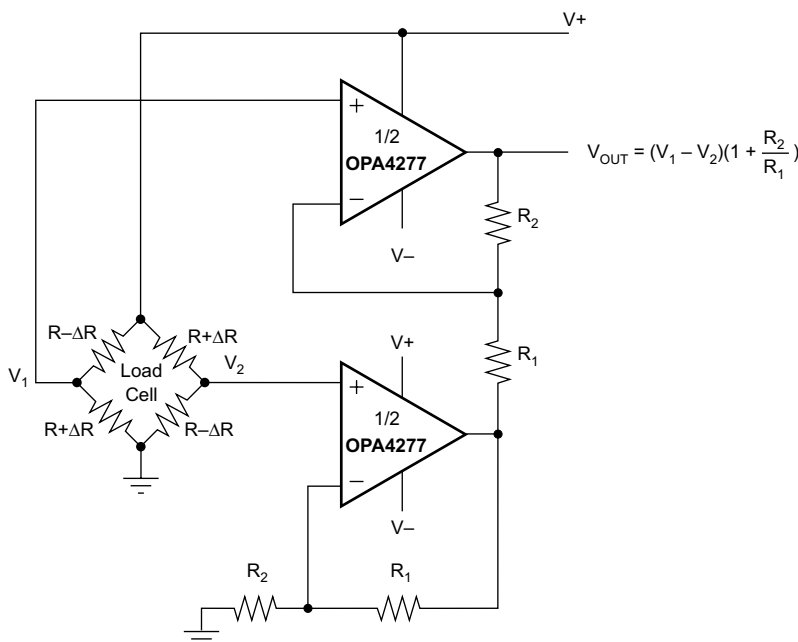


Figure 23. Input Bias Current Cancellation



For integrated solution see: INA126, INA2126 (dual)
 INA125 (on-board reference)
 INA122 (single-supply)

Figure 24. Load Cell Amplifier

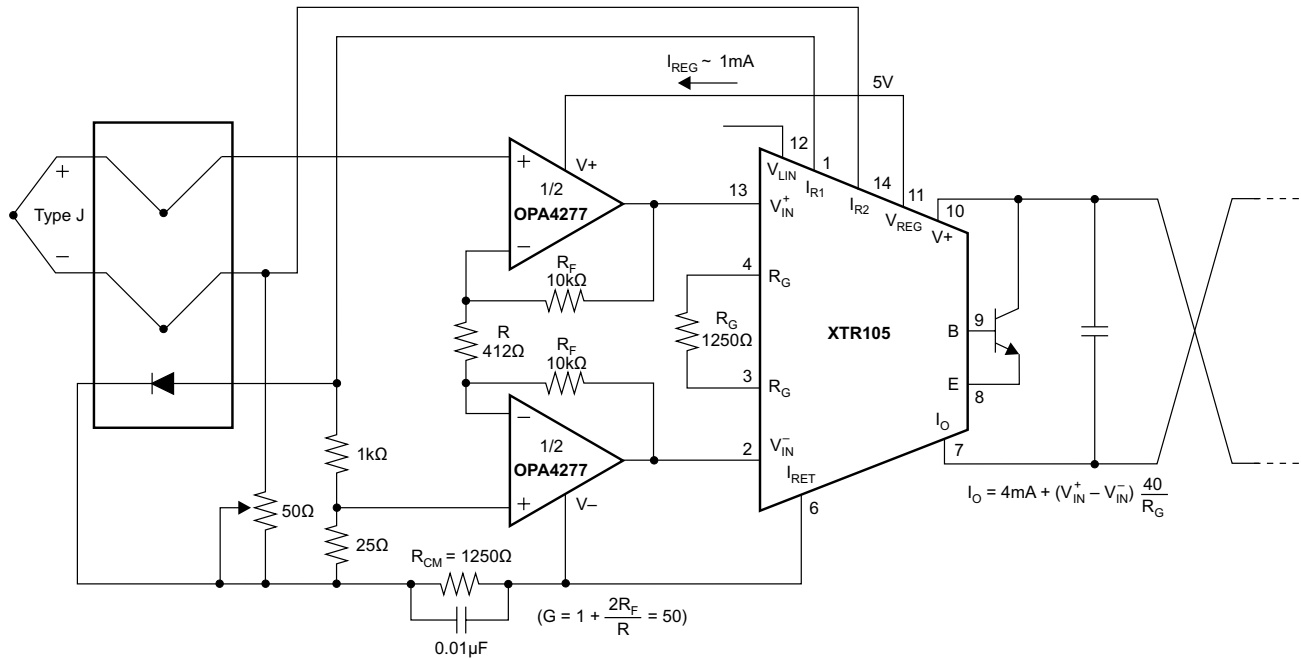


Figure 25. Thermocouple Low Offset, Low Drift Loop Measurement With Diode Cold Junction Compensation

8.2.3 Application Curve

At $T_J = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 2\text{ k}\Omega$, unless otherwise noted.

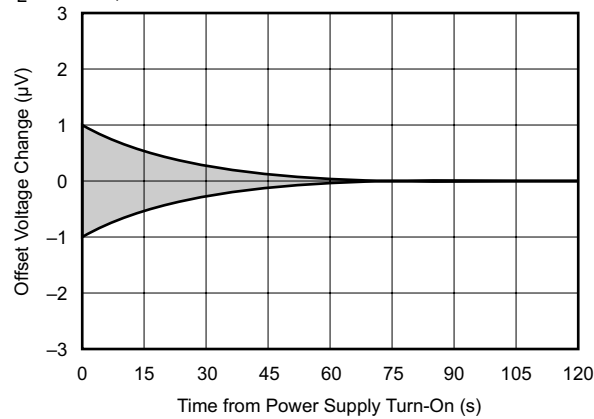


Figure 26. Warm-Up Offset Voltage Drift

9 Power Supply Recommendations

OPA4277 operates from ± 2 - to ± 18 -V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277 is specified for real-world applications; a single limit applies over the ± 5 - to ± 15 -V supply range. This allows a customer operating at $V_S = \pm 10$ V to have the same assured performance as a customer using ± 15 -V supplies. In addition, key parameters are assured over the specified temperature range, -55°C to 125°C . Most behavior remains unchanged through the full operating voltage range (± 2 to ± 18 V). Parameters which vary significantly with operating voltage or temperature are shown in the typical performance curves.

10 Layout

10.1 Layout Guidelines

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located in [机械封装和可订购信息](#) show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA4277 has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA4277. Cancel these thermal potentials by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

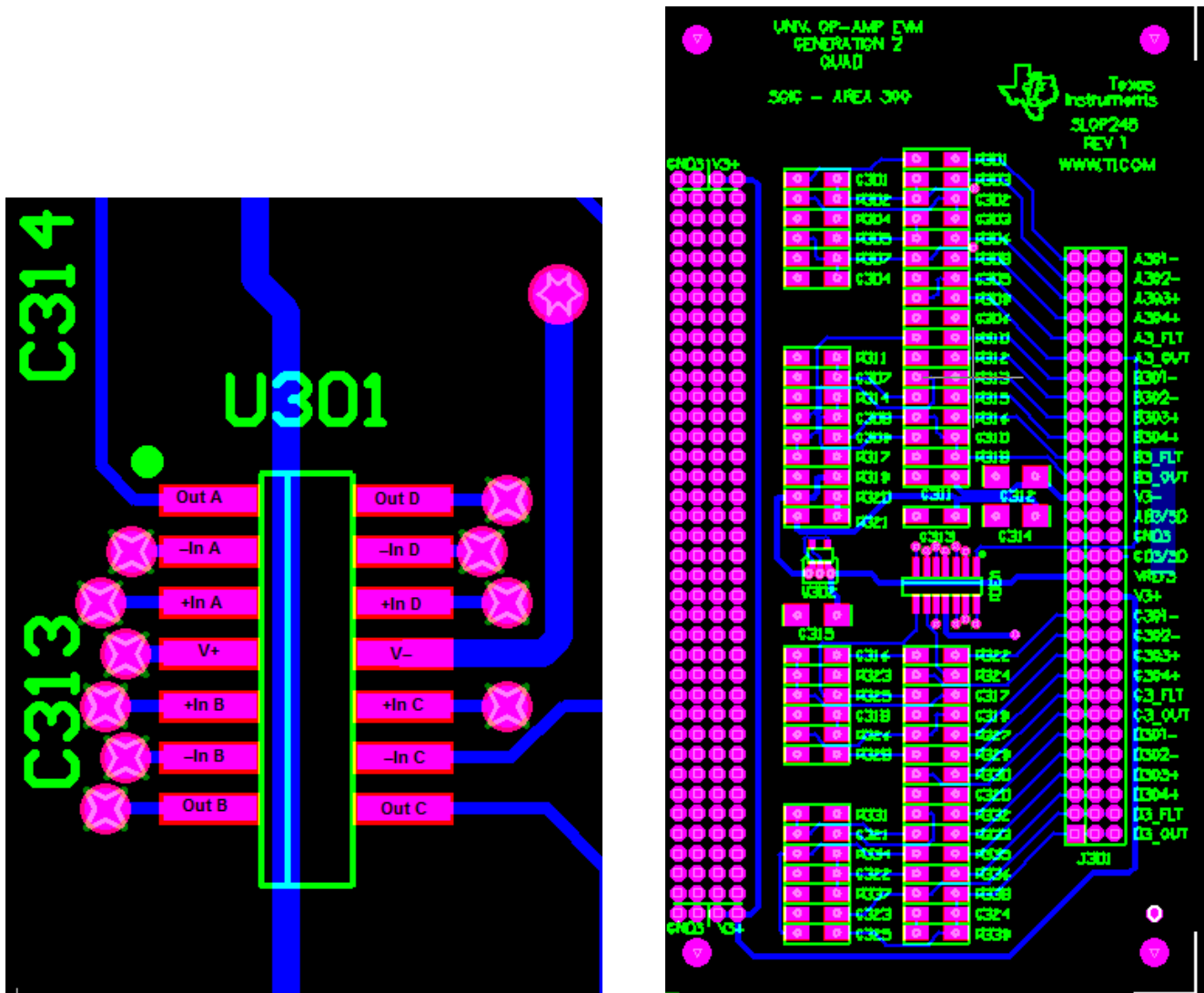


Figure 27. Board Layout Example

11 器件和文档支持

11.1 商标

All trademarks are the property of their respective owners.

11.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2014, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4277MDREP	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	OPA4277EP	
OPA4277MDTEP	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	OPA4277EP	Samples
V62/14625-01XE	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	OPA4277EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA4277-EP :

- Catalog: [OPA4277](#)

NOTE: Qualified Version Definitions:



- Catalog - TI's standard catalog product

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

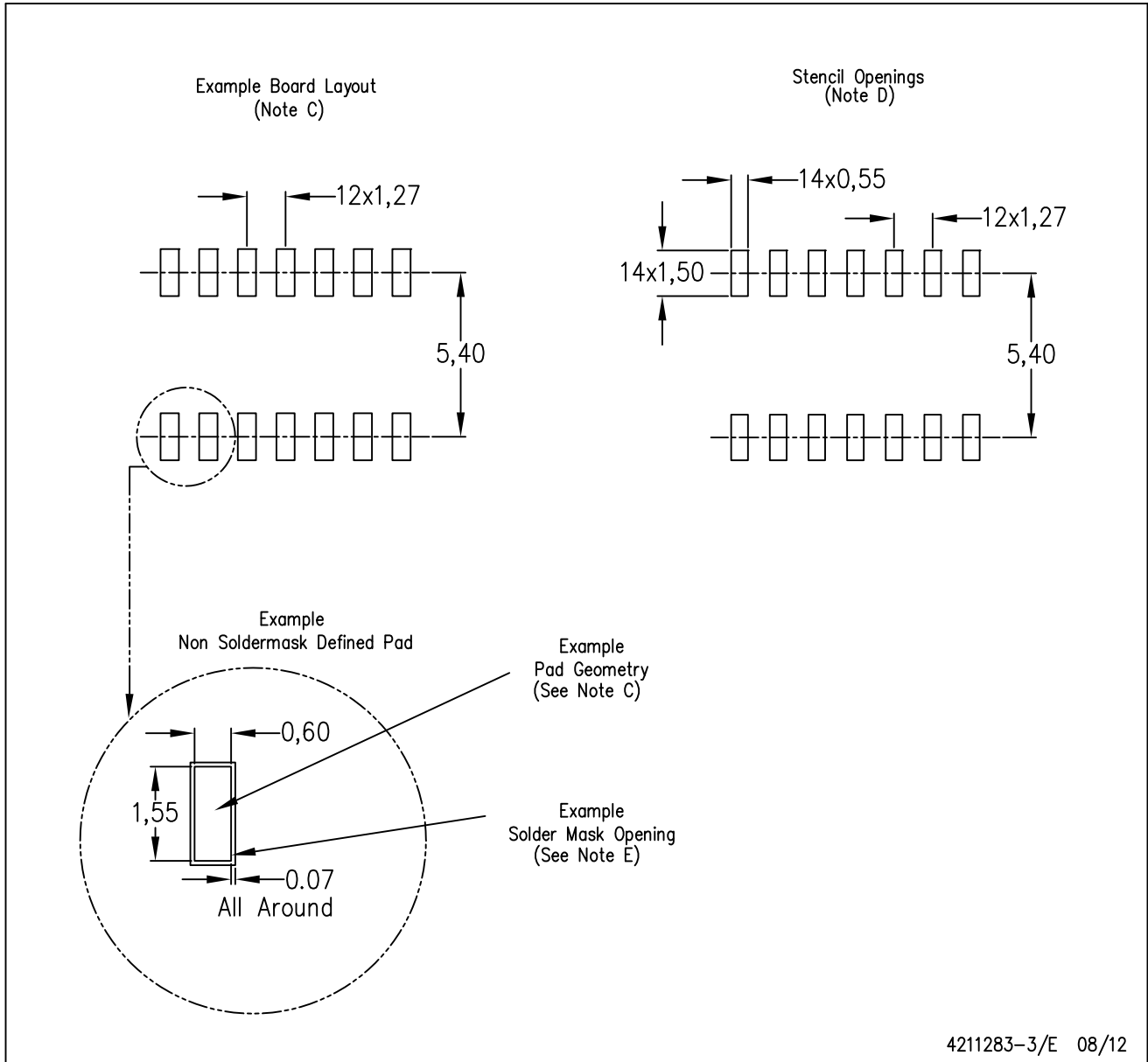


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或间接版权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独自负责满足与其产品及其应用中使用 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独自负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated