OPA1612-Q1 SoundPlus 高性能、双极输入音频运算放大器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体放电模式 (HBM) 分类等级 2
  - 器件组件充电模式 (CDM) 分类等级 C6
- 出色音质
- 超低噪声：1kHz 时为 1.1nV/√Hz
- 超低失真：
  1kHz 时为 0.000015%
- 高压摆率：27V/μs
- 高带宽：40MHz (G = +1)
- 高开环增益：130dB
- 单位增益稳定
- 低静态电流：
  每通道 3.6mA
- 轨到轨输出
- 宽电源电压范围：±2.25V 至 ±18V

2 应用

- 专业音频设备
- 麦克风前置放大器
- 模数混合控制台
- 播音室设备
- 音频测试和测量
- 高端 A/V 接收器

3 概述

OPA1612-Q1 器件是一款双通道、 SoundPlus™双极输入运算放大器，在 1kHz 频率下可实现很低的噪声密度 (1.1nV/√Hz) 以及超低失真 (0.000015%)。 OPA1612-Q1 器件可在 2kΩ 负载条件下提供摆幅在 600mV 以内的轨到轨输出，这有助于提高余量并实现动态范围的最大化。 此外，这些器件还具有 ±30mA 高输出驱动能力。

这些器件支持 ±2.25V 到 ±18V 的宽电源电压范围，每通道电源电流仅为 3.6mA。 OPA1612-Q1 运算放大器的单位增益稳定，在宽负载条件范围内可提供出色的动态性能。

双通道型号具有完全独立的电路，即使处于过驱或过载状态也可在通道间实现最低串扰和零交互。

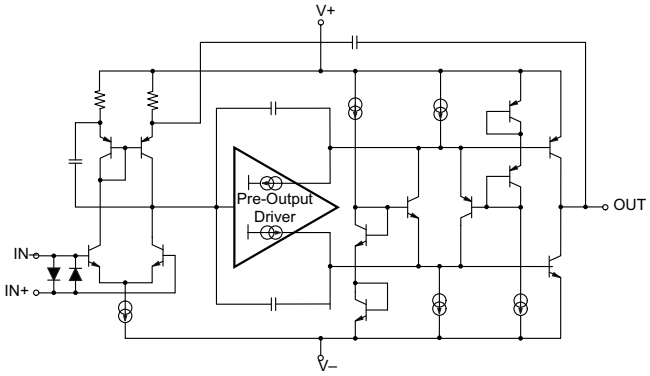
OPA1612-Q1 器件采用小外形尺寸集成电路 (SOIC)-8 封装 封装。 该器件的额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

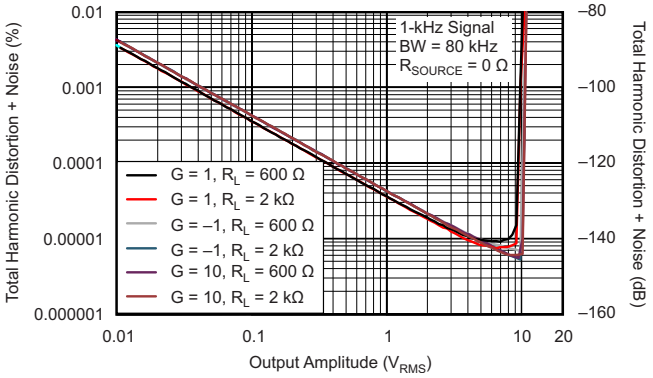
器件型号	封装	封装尺寸（标称值）
OPA1612-Q1	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

功能框图



THD+N 比与输出幅值间的关系



目录

4 修订历史记录

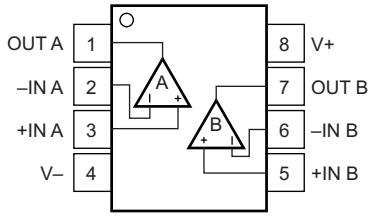
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (November 2015) to Revision A **Page**

- 已更改 器件状态“*产品预览*”至“*量产数据*” ... 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output, channel A
2	–IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
4	V–	—	Negative (lowest) power supply
5	+IN B	I	Inverting input, channel B
6	–IN B	I	Noninverting input, channel B
7	OUT B	O	Output, channel B
8	V+	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S(2)	Supply voltage		40	V
	Input voltage	(V–) – 0.5	(V+) + 0.5	V
	Input current (all pins except power-supply pins)		±10	mA
	Output short-circuit(2)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature		200	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2 (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA1612-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	0.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	1.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_S = ±2.25 V to ±18 V

At T_A = 25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3 V_{RMS}		0.000015%		
				–136		dB
IMD	Intermodulation distortion	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz), G = +1, V_O = 3 V_{RMS}		0.000015%		
				–136		dB
		DIM 30 (3-kHz square wave and 15-kHz sine wave), G = +1, V_O = 3 V_{RMS}		0.000012%		
				–138		dB
		CCIF twin-tone (19 kHz and 20 kHz), G = +1, V_O = 3 V_{RMS}		0.000008%		
				–142		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 100		80		MHz
		G = 1		40		MHz
SR	Slew rate	G = –1		27		V/µs
	Full-power bandwidth(1)	V_O = 1 V_{PP}		4		MHz
	Overload recovery time	G = –10		500		ns
	Channel separation (dual)	f = 1 kHz		–130		dB
NOISE						
	Input voltage noise	f = 20 Hz to 20 kHz		1.2		μV_{PP}
e_n	Input voltage noise density(2)	f = 10 Hz		2		nV/√Hz
		f = 100 Hz		1.5		nV/√Hz
		f = 1 kHz		1.1	1.5	nV/√Hz
I_n	Input current noise density	f = 10 Hz		3		pA/√Hz
		f = 1 kHz		1.7		pA/√Hz
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±15 V		±100	±500	µV
dV_{OS}/dT	V_{OS} over temperature(2)	T_A = –40°C to +125°C		1	4	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V		0.1	1	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = 0 V		±60	±250	nA
		VCM = 0 V, DRG package only		±60	±300	nA
	I_B over temperature(2)	T_A = –40°C to +125°C			350	nA
I_{OS}	Input offset current	V_{CM} = 0 V		±25	±175	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2 V ≤ V_{CM} ≤ (V+) – 2 V	110	120		dB
INPUT IMPEDANCE						
	Differential			20k || 8		Ω || pF
	Common-mode			10^9 || 2		Ω || pF

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.

Electrical Characteristics: V_S = ±2.25 V to ±18 V (continued)

At T_A = 25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 10 kΩ	114	130		dB
		(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 2 kΩ	110	114		dB
OUTPUT						
V_{OUT}	Voltage output	R_L = 10 kΩ, A_{OL} ≥ 114 dB	(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, A_{OL} ≥ 110 dB	(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current		See Figure 27			mA
Z_O	Open-loop output impedance		See Figure 28			Ω
I_{SC}	Short-circuit current	Source, V_S = ±18 V		55		mA
		Sink, V_S = ±18 V		–62		mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			pF
POWER SUPPLY						
V_S	Specified voltage		±2.25		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		3.6	4.5	mA
	I_Q over Temperature(2)	T_A = –40°C to +125°C			5.5	mA
TEMPERATURE RANGE						
	Specified range		–40		125	°C
	Operating range		–55		125	°C

6.6 Typical Characteristics

At T_A = 25°, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

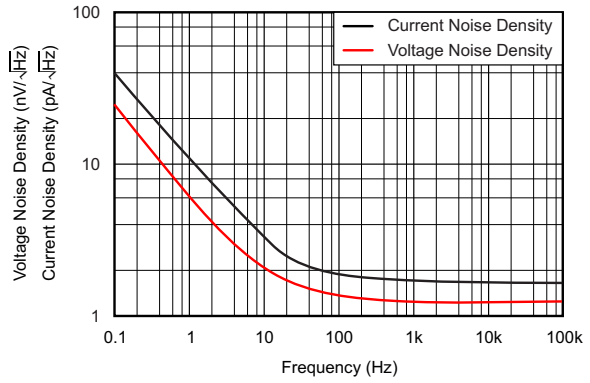


Figure 1. Input Voltage Noise Density and Input Current Noise Density vs Frequency

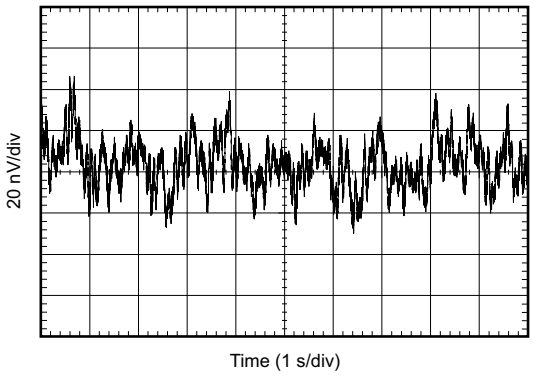
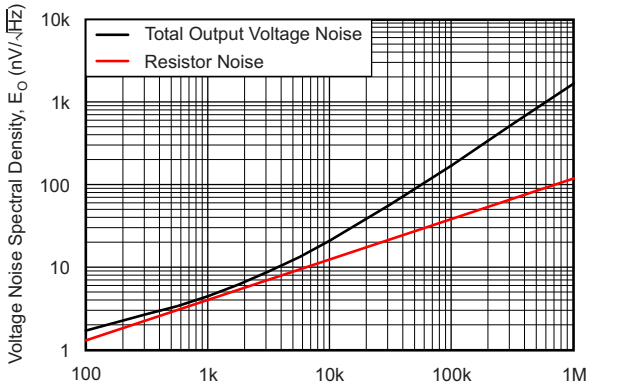


Figure 2. 0.1-Hz to 10-Hz Noise



$E_O^2 = e_n^2 + (i_n \times R_S)^2 + 4kRT_S$ See Figure 29

Figure 3. Voltage Noise vs Source Resistance

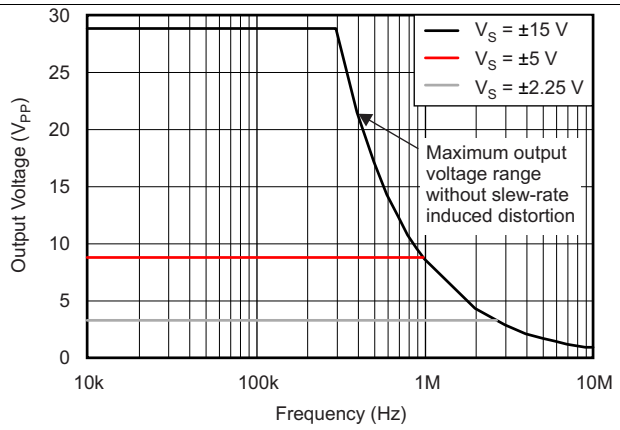


Figure 4. Maximum Output Voltage vs Frequency

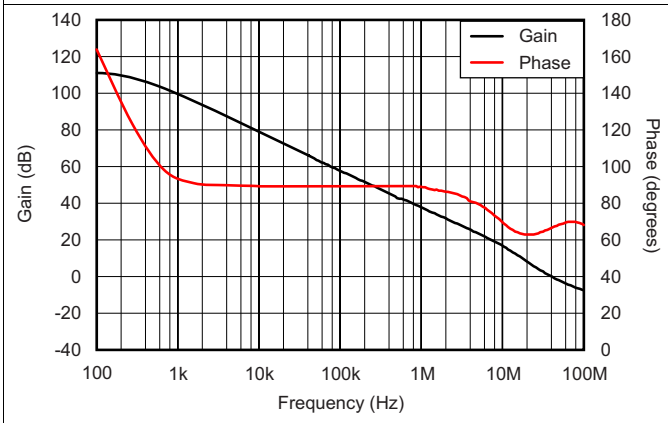


Figure 5. Gain and Phase vs Frequency

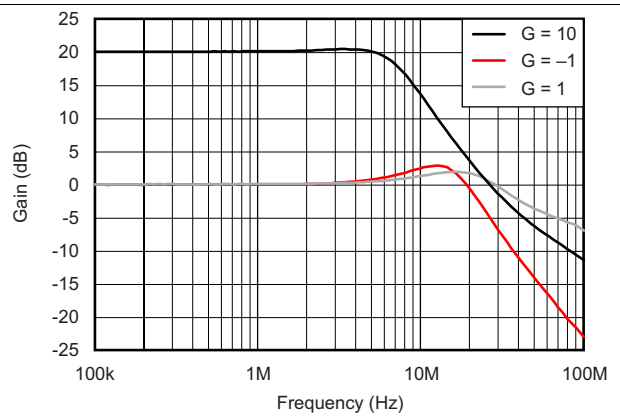
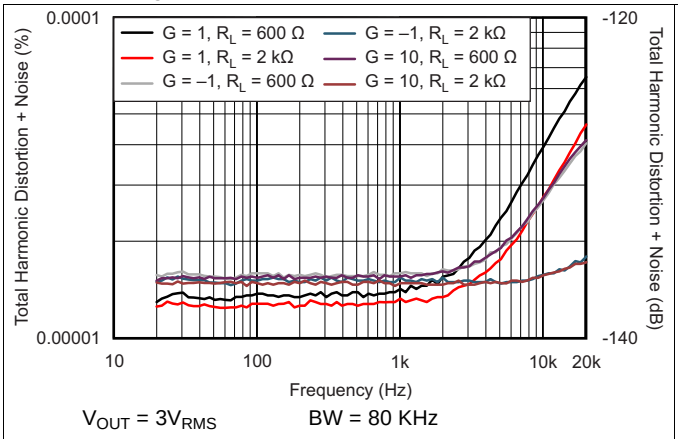


Figure 6. Closed-Loop Gain vs Frequency

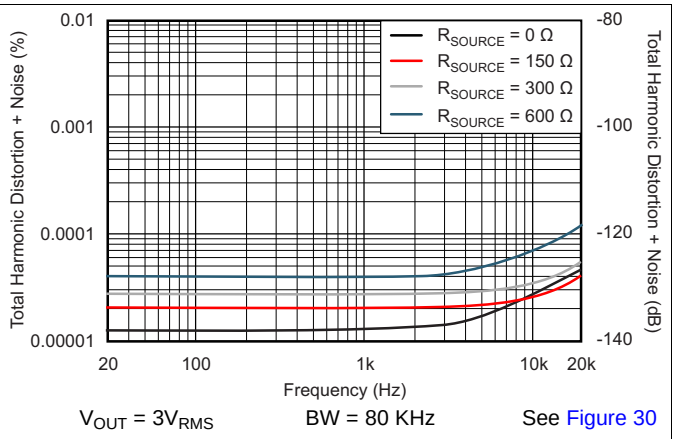
Typical Characteristics (continued)

At T_A = 25°, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



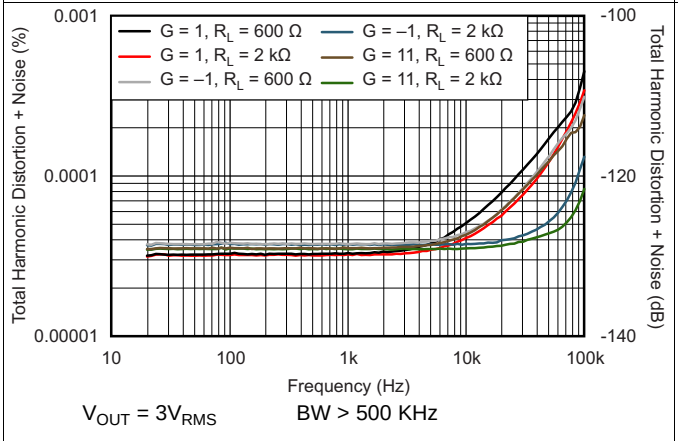
V_{OUT} = 3V_{RMS} BW = 80 KHz

Figure 7. THD+N Ratio vs Frequency



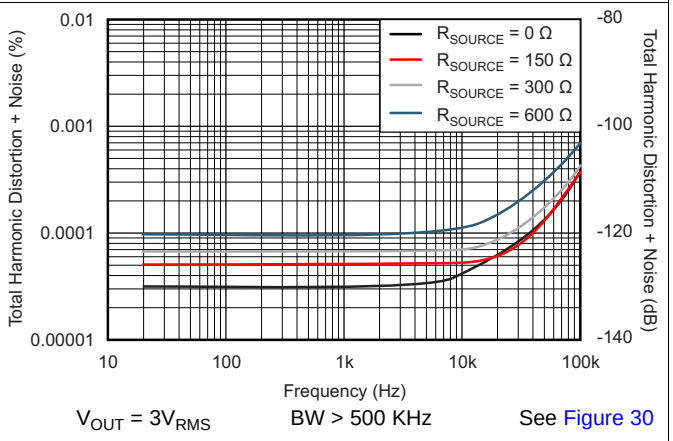
V_{OUT} = 3V_{RMS} BW = 80 KHz See Figure 30

Figure 8. THD+N Ratio vs Frequency



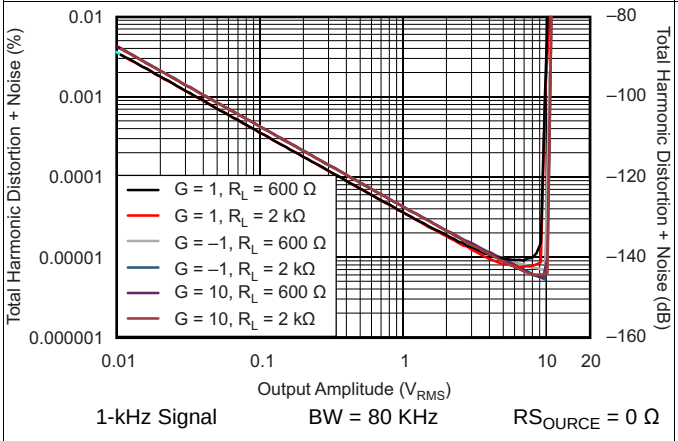
V_{OUT} = 3V_{RMS} BW > 500 KHz

Figure 9. THD+N Ratio vs Frequency



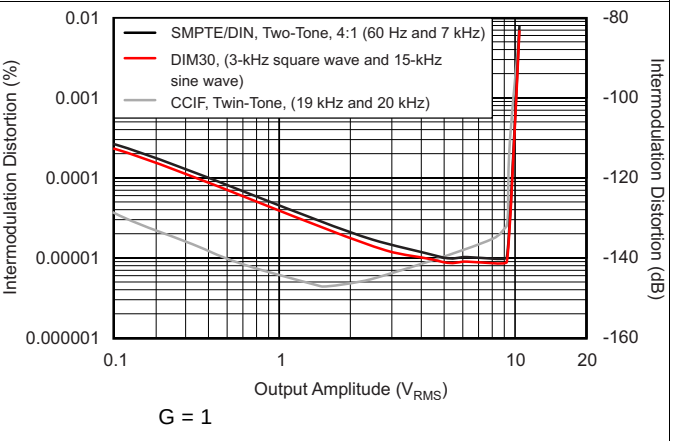
V_{OUT} = 3V_{RMS} BW > 500 KHz See Figure 30

Figure 10. THD+N Ratio vs Frequency



1-kHz Signal BW = 80 KHz RS_{OURCE} = 0 Ω

Figure 11. THD+N Ratio vs Output Amplitude

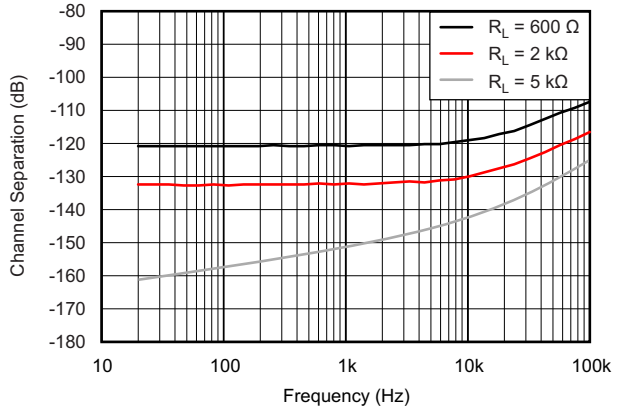


G = 1

Figure 12. Intermodulation Distortion vs Output Amplitude

Typical Characteristics (continued)

At T_A = 25°, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



VOUT = 3.5 V_{RMS} V_S = ±15 V G = 1

Figure 13. Channel Separation vs Frequency

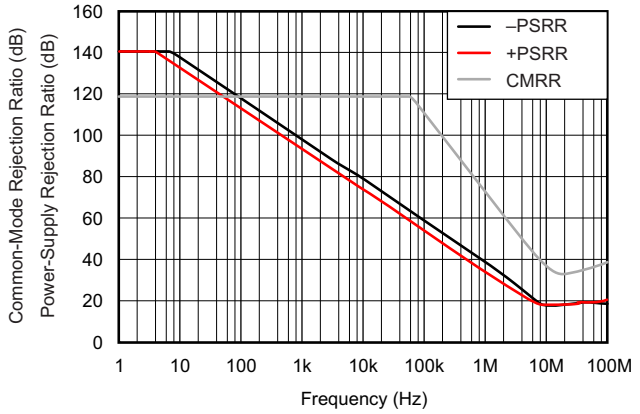
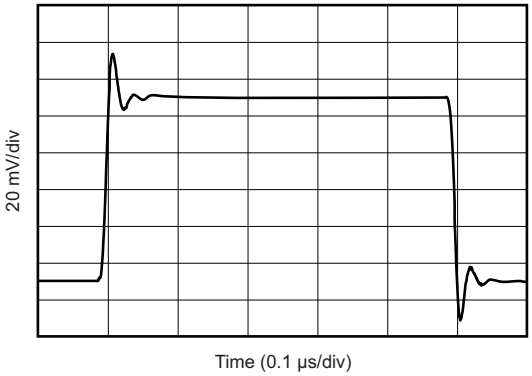
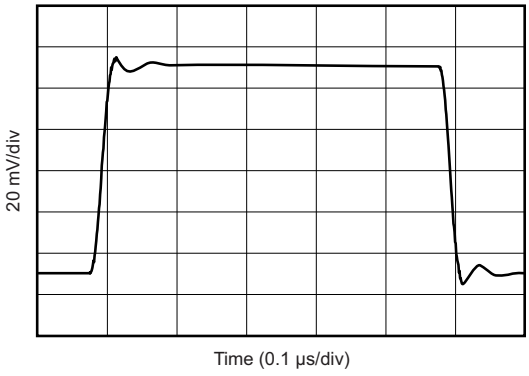


Figure 14. CMRR and PSRR vs Frequency (Referred to Input)



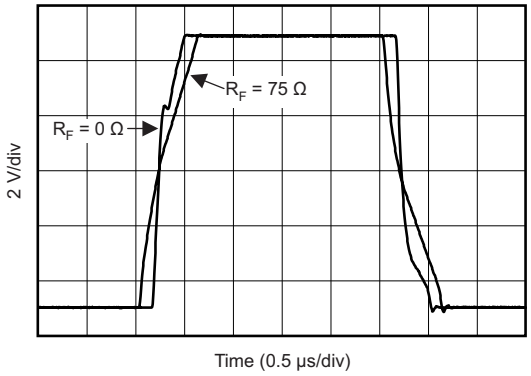
G = 1 C_L = 50 pF See Figure 31

Figure 15. Small-Signal Step Response (100 mV)



G = –1 C_L = 50 pF See Figure 32

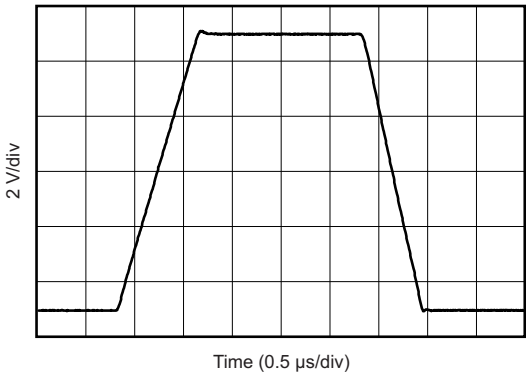
Figure 16. Small-Signal Step Response (100 mV)



G = 1 C_L = 50 pF RL = 2 kΩ

See the *Input Protection* section

Figure 17. Large-Signal Step Response

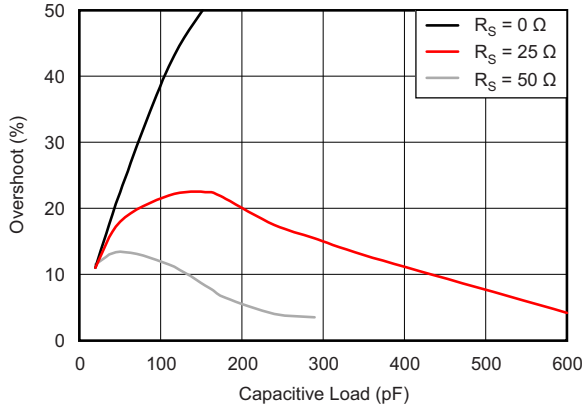


G = –1 C_L = 50 pF RL = 2 kΩ

Figure 18. Large-Signal Step Response

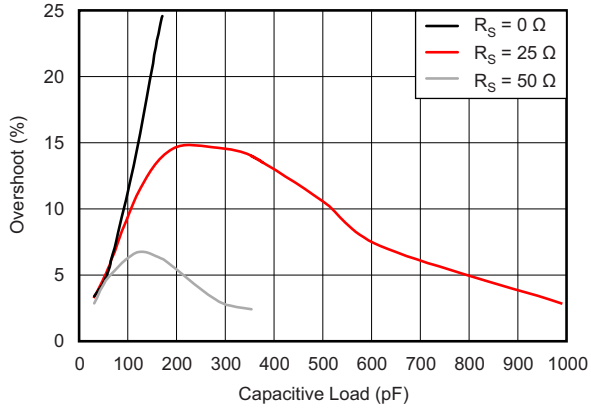
Typical Characteristics (continued)

At T_A = 25°, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



G = 1 See Figure 33

Figure 19. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



G = –1 See Figure 34

Figure 20. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

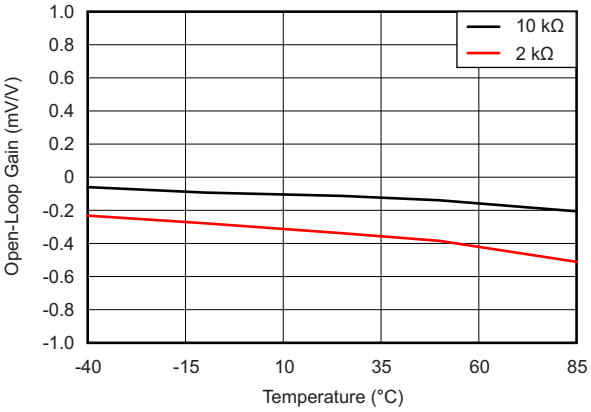


Figure 21. Open-Loop Gain vs Temperature

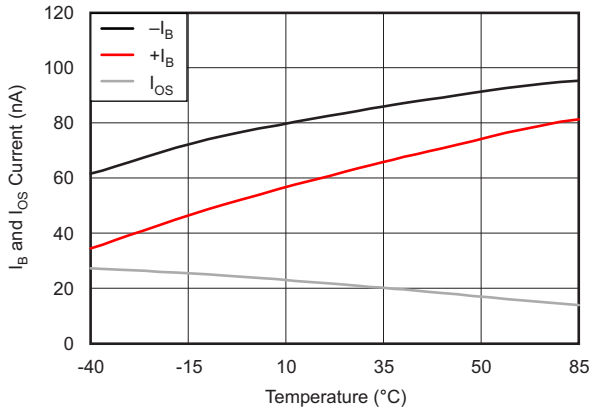
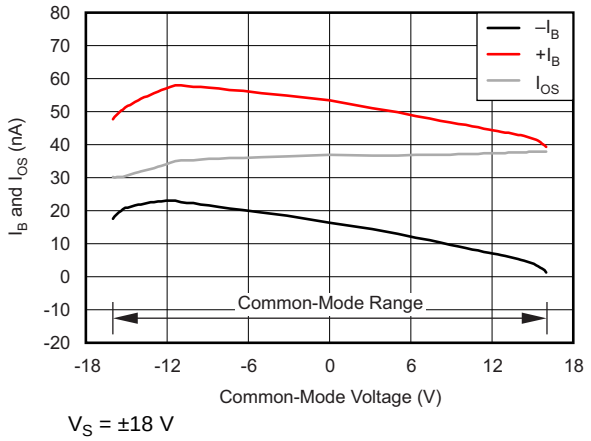


Figure 22. I_B and I_{OS} vs Temperature



V_S = ±18 V

Figure 23. I_B and I_{OS} vs Common-Mode Voltage

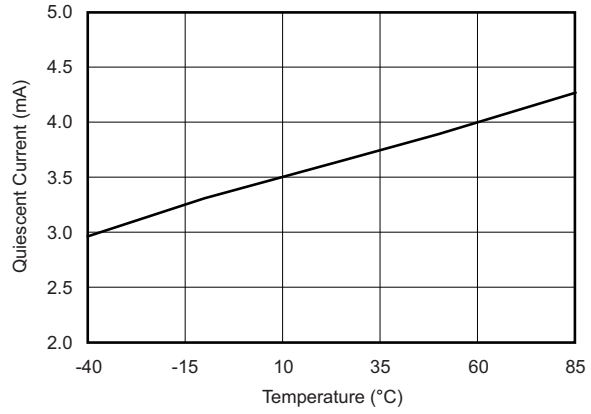


Figure 24. Quiescent Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

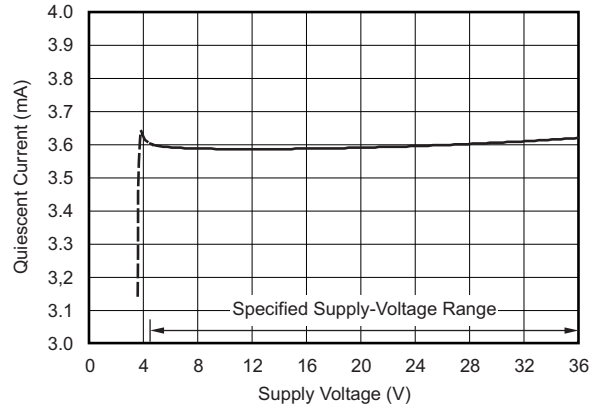


Figure 25. Quiescent Current vs Supply Voltage

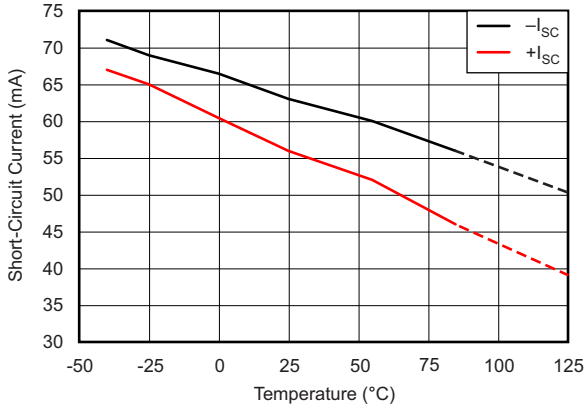
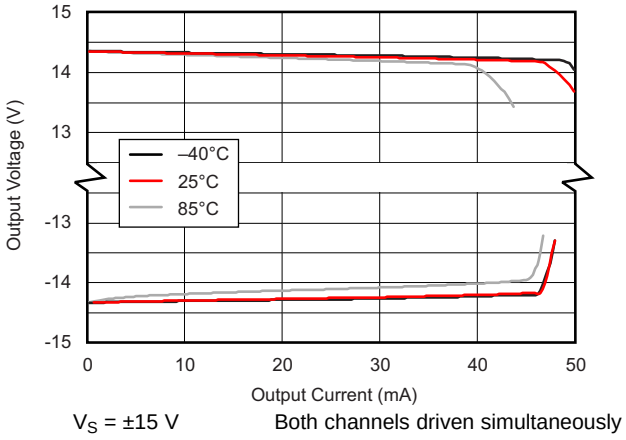


Figure 26. Short-Circuit Current vs Temperature



V_S = ±15 V Both channels driven simultaneously

Figure 27. Output Voltage vs Output Current

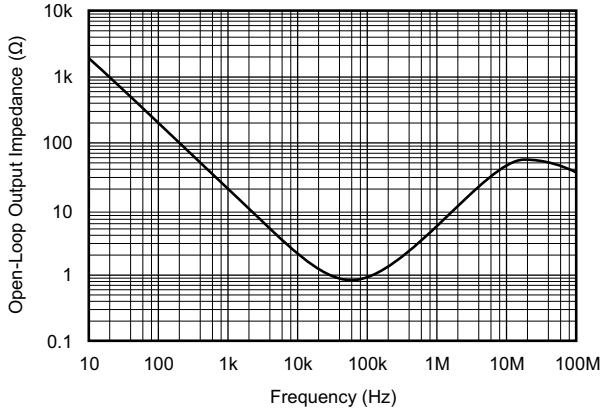


Figure 28. Open-Loop Output Impedance vs Frequency

7 Parameter Measurement Information

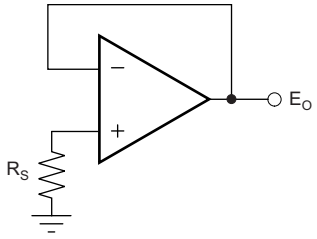


Figure 29. Circuit for Figure 3—Voltage Noise vs Source Resistance

Parameter Measurement Information (continued)

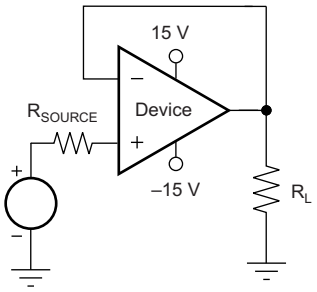


Figure 30. Circuit for Figure 8 and Figure 10—THD+N Ratio vs Frequency

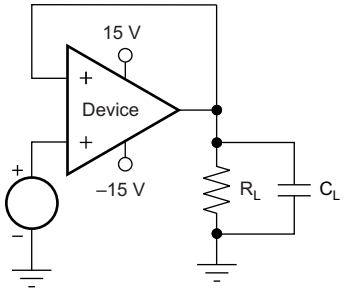


Figure 31. Circuit for Figure 15—Small-Signal Step Response (100 mV)

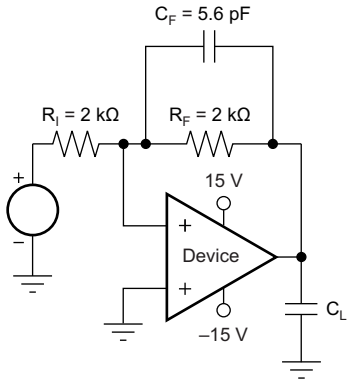


Figure 32. Circuit for Figure 16—Small-Signal Step Response (100 mV)

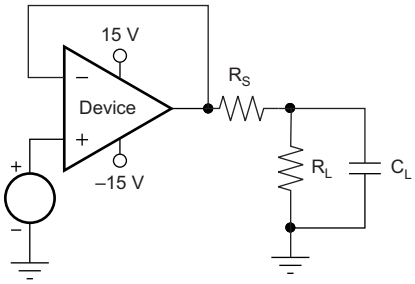


Figure 33. Circuit for Figure 19—Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Parameter Measurement Information (continued)

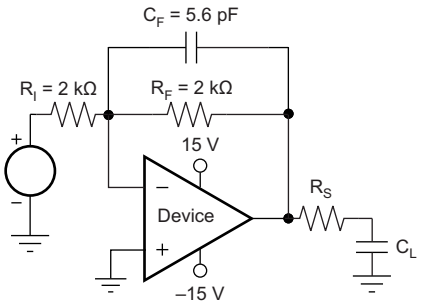


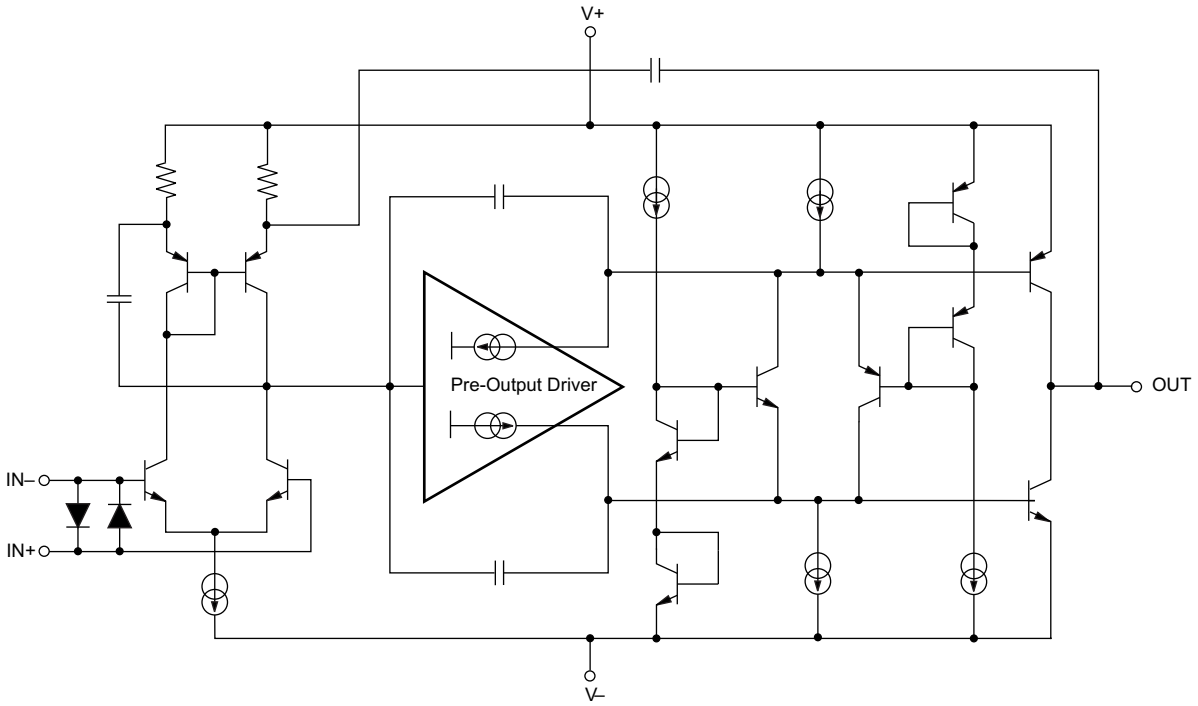
Figure 34. Circuit for Figure 20—Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8 Detailed Description

8.1 Overview

The OPA1612-Q1 bipolar-input operational amplifierachieves very low 1.1-nV/√Hz noise density with an ultralow distortion of 0.000015% at 1 kHz. The rail-to-rail output swing, within 600 mV with a 2-kΩ load, increases headroom and maximizes dynamic range. These devices also have a high output drive capability of ±40 mA. The wide supply range of ±2.25 V to ±18 V, on only 3.6 mA of supply current per channel, makes them applicable to both 5-V systems and 36-V audio applications. The OPA1612-Q1 op amp is unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Dissipation

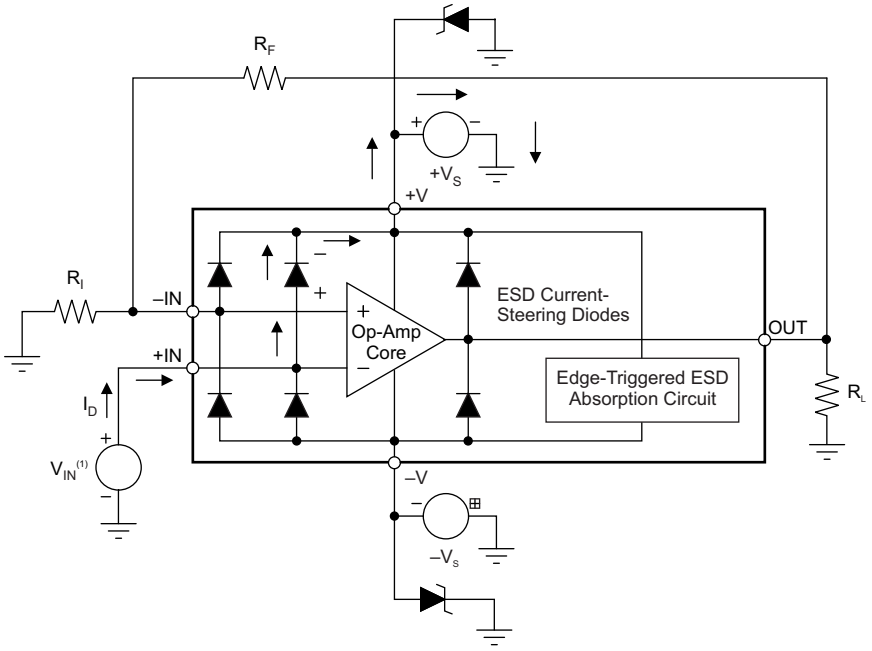
The OPA1612-Q1 op amp is capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA1612-Q1 op amp improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

8.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Feature Description (continued)

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 35 shows the ESD circuits contained in the OPA1612-Q1 device (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) $V_{IN} = +V_S + 500$ mV.

Figure 35. Equivalent Internal ESD Circuitry and its Relation to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse when discharged through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage to the core. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device internal to the OPA1612-Q1 device triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, the absorption device quickly activates and clamps the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as the one Figure 35 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, some of the internal ESD protection circuits may possibly be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 35 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

Feature Description (continued)

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, the result depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins; see Figure 35. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener diode voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.3.3 Operating Voltage

The OPA1612-Q1 op amp operates from ±2.25-V to ±18-V supplies while maintaining excellent performance. The OPA1612-Q1 device can operate with as little as +4.5 V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA1612-Q1 device, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary with operating voltage or temperature are shown in the *Typical Characteristics* section.

8.3.4 Input Protection

The input terminals of the OPA1612-Q1 device is protected from excessive differential voltage with back-to-back diodes, as Figure 36 shows. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 17 of the *Typical Characteristics* section. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) or a feedback resistor (R_F) can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA1612-Q1 device and is examined in the *Noise Performance* section. Figure 36 shows an example configuration when both current-limiting input and feedback resistors are used.

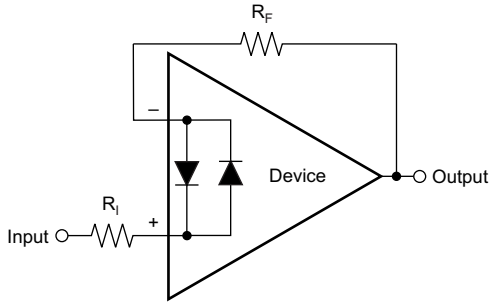


Figure 36. Pulsed Operation

8.4 Device Functional Modes

The OPA1612-Q1 device has a single functional mode. The device is powered on as long as the power supply voltage is between 4.5 V (±2.25 V) and 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA1612-Q1 device is unity-gain stable, precision op amp with very low noise; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-µF capacitors are adequate.

9.2 Typical Application

Figure 37 shows how to use the OPA1612-Q1 device as an amplifier for professional audio headphones. The circuit shows the left side stereo channel. An identical circuit is used to drive the right side stereo channel.

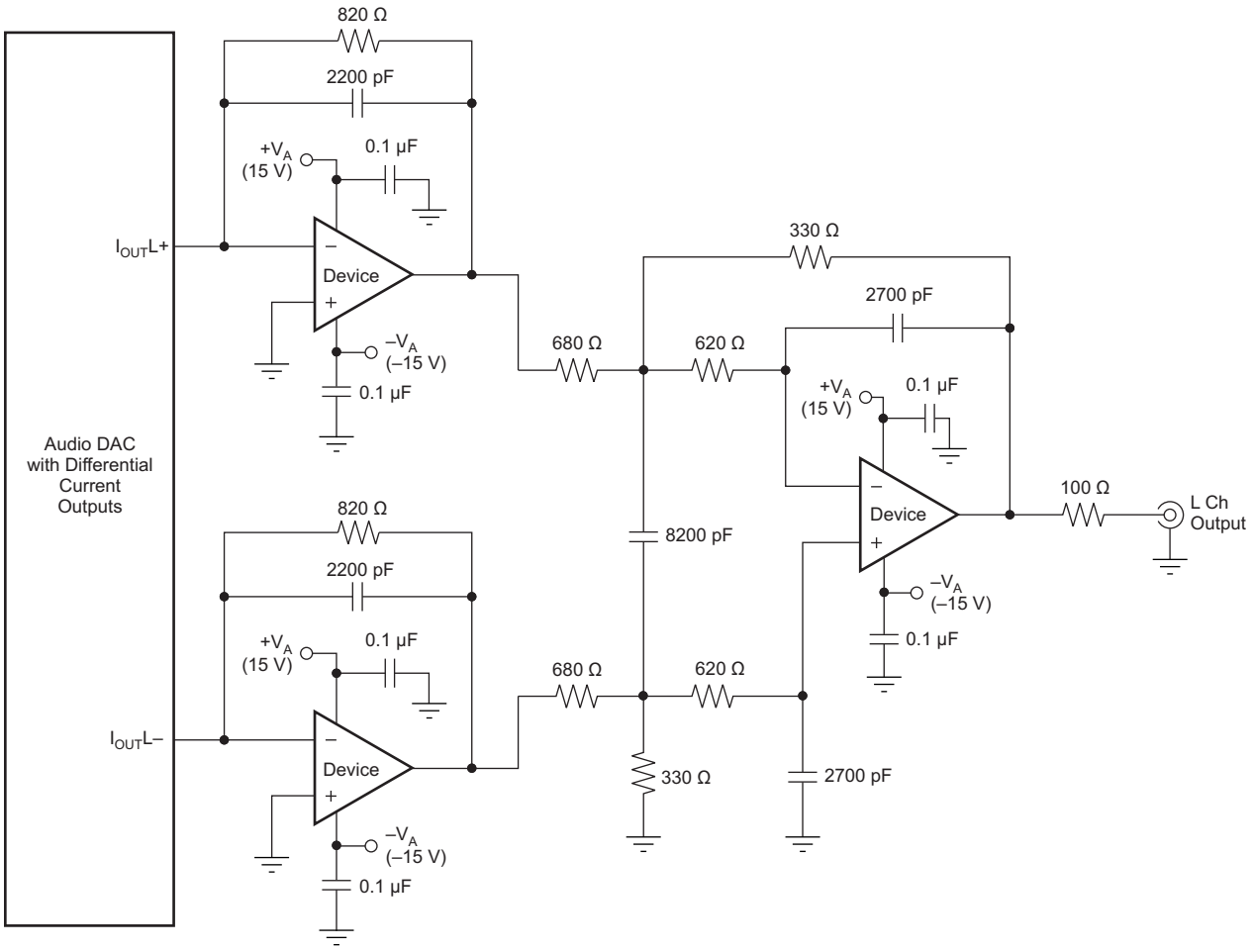


Figure 37. Audio DAC Post Filter (I/V Converter and Low-Pass Filter)

Typical Application (continued)

9.2.1 Design Requirements

Use Equation 1 to calculate the total circuit noise.

$$E_O^2 = e_n^2 + (i_n R_S)^2 + 4kTR_S \quad (1)$$

where

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

9.2.2 Detailed Design Procedure

9.2.2.1 Noise Performance

Figure 40 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA1612-Q1 device (GBW = 40 MHz, G = +1) is shown with total circuit noise calculated. The op amp contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA1612-Q1 device makes it a good choice for use in applications where the source impedance is less than 1 kΩ.

9.2.2.1.1 Basic Noise Calculations

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

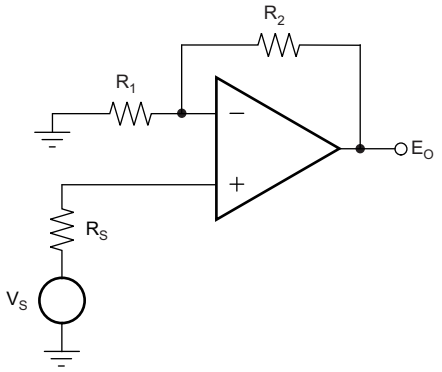
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 40 plots this function. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 38 shows both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise.

The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

Typical Application (continued)

Noise in Noninverting Gain Configuration



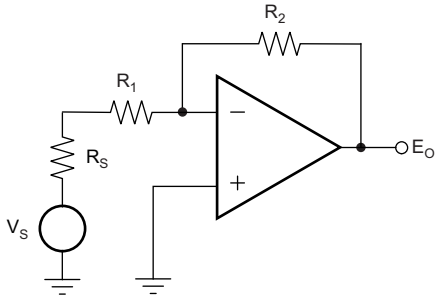
Noise at the output:

$$E_O^2 = \left[1+\frac{R_2}{R_1}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left[1+\frac{R_2}{R_1}\right]^2$$

where

- $e_S = \sqrt{4kTR_S} \times \left[1+\frac{R_2}{R_1}\right]$ = thermal noise of R_S
- $e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1}\right]$ = thermal noise of R_1
- $e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1+\frac{R_2}{R_1+R_S}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

where

- $e_S = \sqrt{4kTR_S} \times \left[\frac{R_2}{R_1+R_S}\right]$ = thermal noise of R_S
- $e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1+R_S}\right]$ = thermal noise of R_1
- $e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

At 1 kHz, e_n = 1.1 nV/$\sqrt{Hz}$ and i_n = 1.7 pA/$\sqrt{Hz}$.

Figure 38. Noise Calculation in Gain Configurations

9.2.2.2 Total Harmonic Distortion Measurements

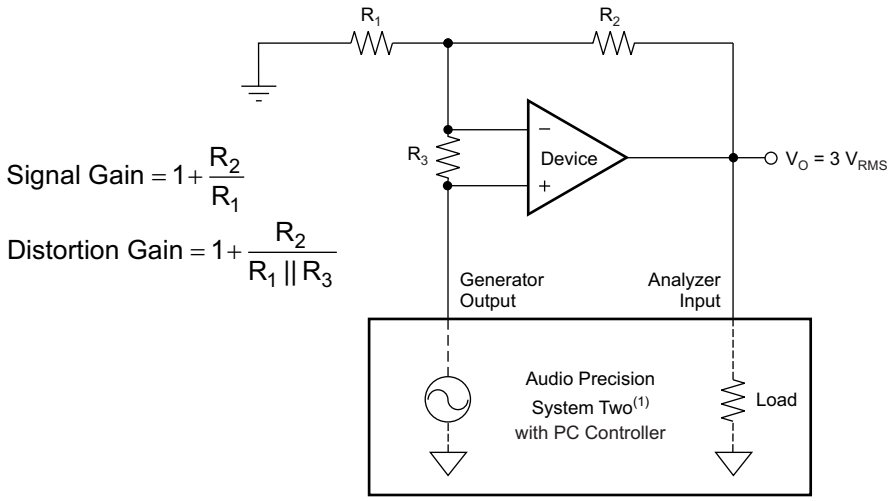
The OPA1612-Q1 op amp has excellent distortion characteristics. THD + noise is below 0.00008% (G = +1, V_O = 3 V_{RMS}, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7 for characteristic performance).

The distortion produced by OPA1612-Q1 op amp is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 39 shows) can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 39 shows a circuit that causes the op amp distortion to be 101 times (or approximately 40 dB) greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. Keep the value of R_3 small to minimize its effect on the distortion measurements.

Typical Application (continued)

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an audio precision system two distortion and noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.



(1) For measurement bandwidth, see Figure 7 through Figure 12.

SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
1	101	∞	1 kΩ	10 Ω
–1	101	4.99 kΩ	4.99 kΩ	49.9 kΩ
10	110	549 Ω	4.99 kΩ	49.9 kΩ

Figure 39. Distortion Test Circuit

9.2.2.3 Capacitive Loads

The dynamic characteristics of the OPA1612-Q1 device is optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. For details of analysis techniques and application circuits, refer to Applications Bulletin AB-028, *Feedback Plots Define Op Amp AC Performance* (SBOA015).

Typical Application (continued)

9.2.3 Application Curves

Equation 1 applies to Figure 40 and Figure 41.

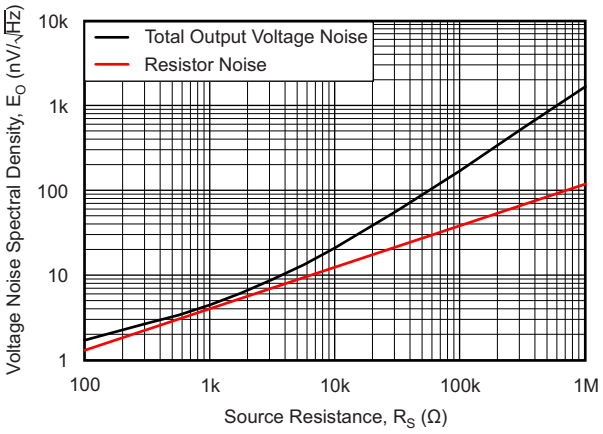


Figure 40. Noise Performance of the OPA1612-Q1 in Unity-Gain Buffer Configuration

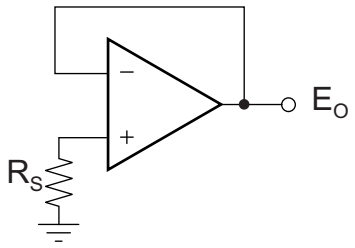


Figure 41. Circuit for Figure 40

10 Power-Supply Recommendations

The OPA1612-Q1 device is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

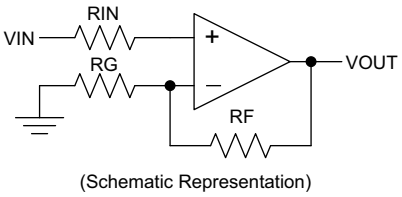
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds while paying attention to the flow of the ground current. For more detailed information, refer to the application report, *Circuit Board Layout Techniques* (SLOA089).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be keep them separate, crossing the sensitive trace perpendicular as

Layout Guidelines (continued)

opposed to in parallel with the noisy trace is the preferred method.

- Place the external components as close to the device as possible. As shown in Figure 42, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



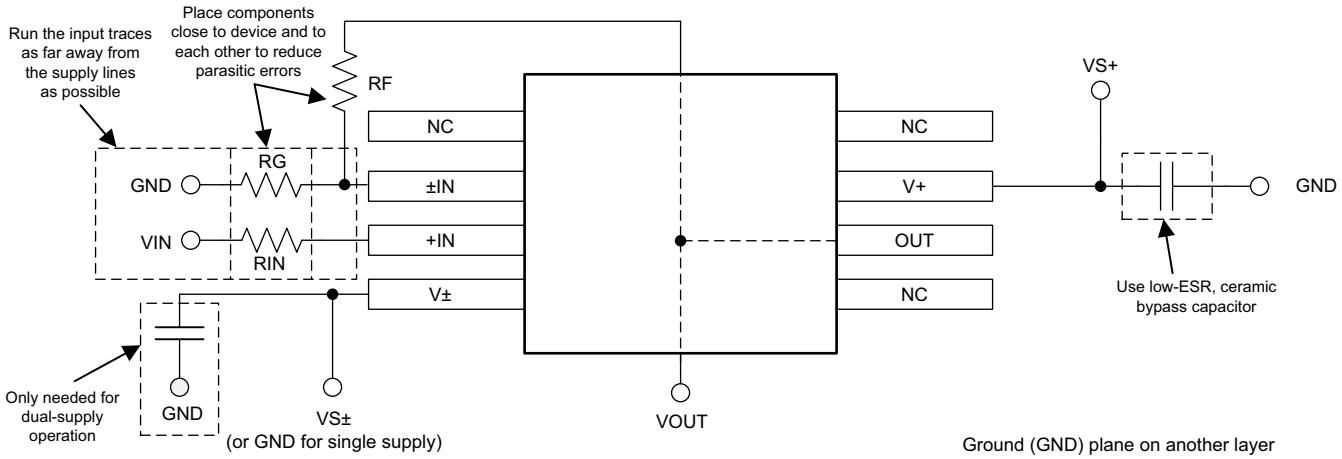


Figure 42. Operational Amplifier Board Layout for a Noninverting Configuration

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《反馈曲线图定义运算放大器交流性能》*，SBOA015
- *《电路板布局布线技巧》*，SLOA089

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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12.4 静电放电警告

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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DLP® 产品	www.dlp.com	能源	www.ti.com/energy
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1612AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1612Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

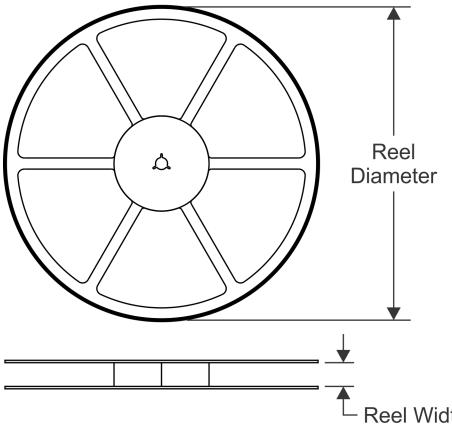
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

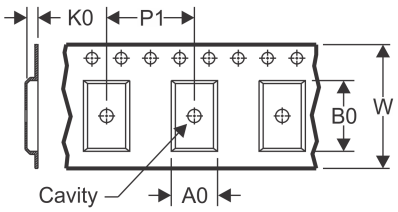
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

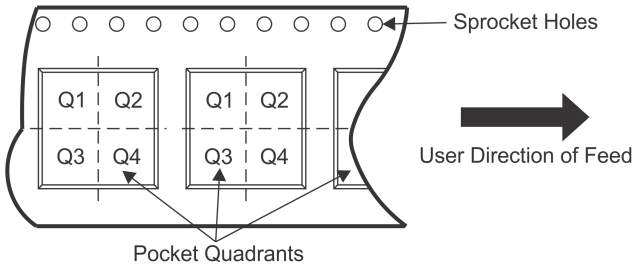


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

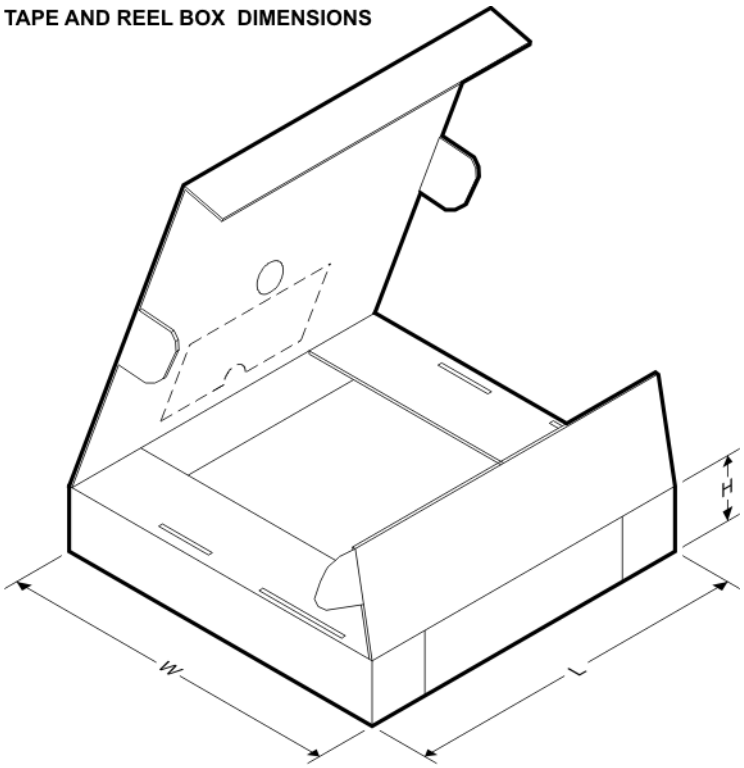
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

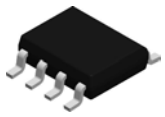
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1612AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1612AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

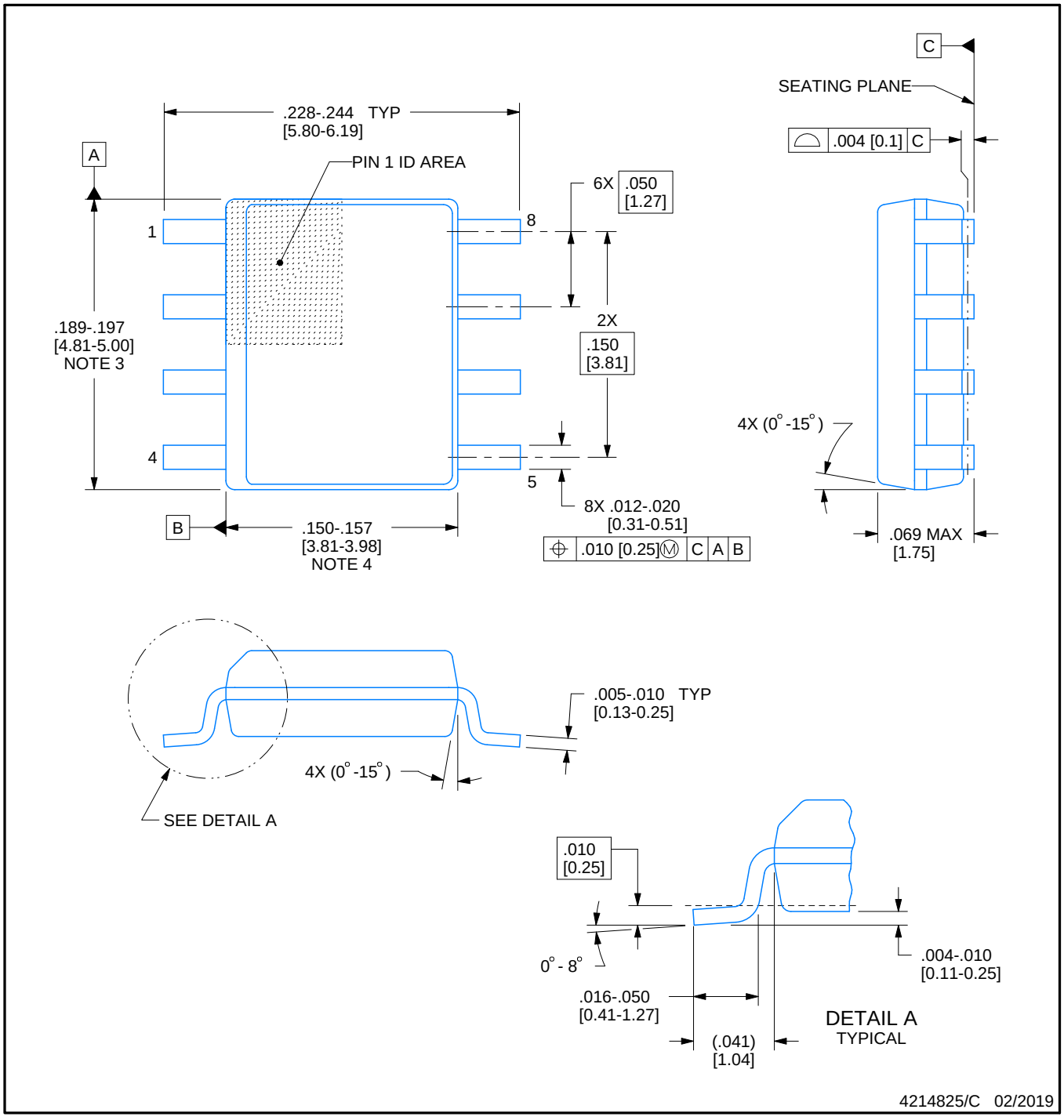


PACKAGE OUTLINE

D0008A

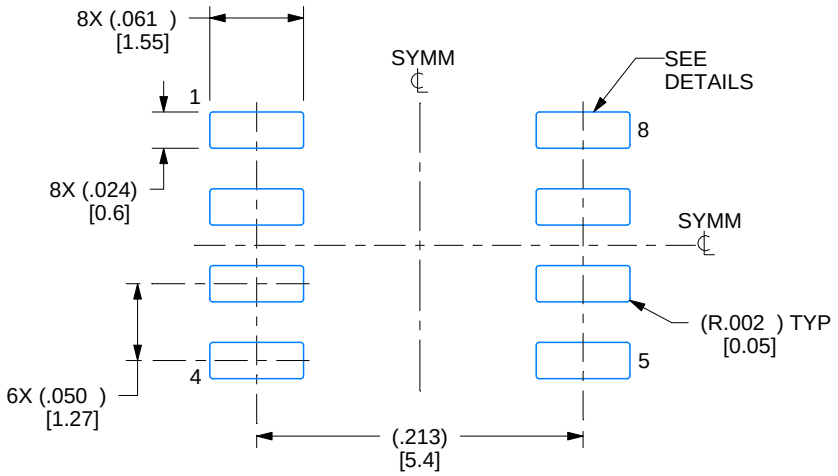
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

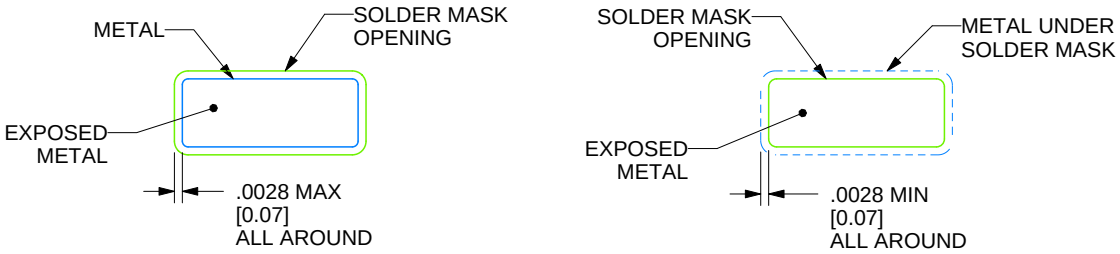


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

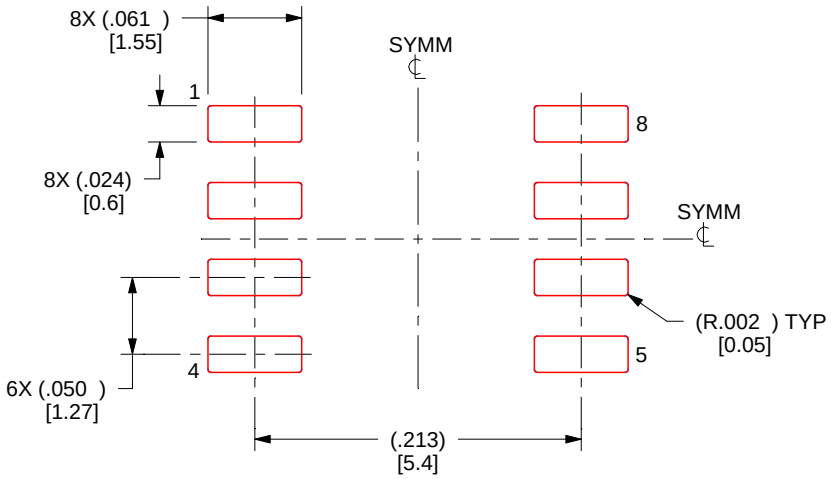
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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