OPA4277-SP 耐辐射高精度运算放大器

1 特性

- 符合 QMLV 标准：5962-16209
  - 抗辐射加固保障 (RHA) 高达 50krad(Si) 总电离剂量 (TID)
  - 无低剂量率辐射损伤增强 (ELDRS)（请参阅辐射报告）
  - 单粒子锁定 (SEL) 对于线性能量传输 (LET) 的抗扰度 = 85MeV-cm^2/mg
- 超低偏移电压：20µV
- 超低漂移：±0.15µV/°C
- 高开环增益：134dB
- 高共模抑制比：140dB
- 高电源抑制比：130dB
- 宽电源电压范围：±2V 至 ±18V
- 低静态电流：800µA/放大器
- 采用 14 引线 CFP，具有行业标准四路运算放大器引脚

2 应用

- 太空卫星温度和温度检测
- 高精度太空仪器
- 太空精密和科学设备 应用
  - 换能器放大器
  - 桥式放大器
  - 应变仪放大器
  - 精密积分器

3 说明

OPA4277-SP 高精度运算放大器取代了符合行业标准的 LM124-SP。该器件的噪声性能得到改善，可提供两种数量级的低输入偏移电压。该器件 具有诸多特性，其中包括超低的偏移电压、超低漂移、低偏置电流、高共模抑制比及高电源抑制比。

OPA4277-SP 由 ±2V 至 ±18V 电源供电运行，性能优异。多数运算放大器仅有一个指定的电源电压，OPA4277-SP 精密运算放大器则有所不同，该器件 适用于实际应用，额定工作电压范围为 ±5V 至 ±15V。当放大器输出摆幅达到指定限值时，可保持高性能。

OPA4277-SP 易于使用，而且不存在其他某些运算放大器中出现的反相和过载问题。其单位增益稳定，在宽负载范围内可保持优异动态性能。OPA4277-SP 配有完全独立的电路，即便在过驱或过载条件下也可以实现最低串扰和零交互。

器件信息(1)

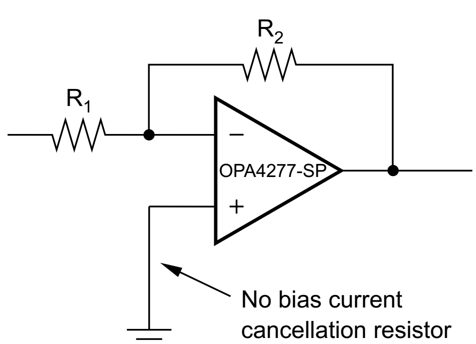
器件型号	等级	封装
5962L1620901VYC	50 krad(Si) 无低剂量率辐射损伤增强 (ELDRS)	14 引线 CFP (HFR)
5962L1620901VXA		28 引线 CDIP (JDJ)
5962L1620901V9A		KGD(2)
OPA4277HFR/EM	工程样片(3)	14 引线 CFP (HFR)

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

(2) KGD = 已知的合格芯片。

(3) 这些部件仅适用于工程评估。部件按照不合规的流程进行加工处理。这些部件不适用于质检、生产、辐射测试或飞行。无法保证器件在整个军用额定温度范围（-55°C 至 125°C）内或其使用寿命内性能无恙。

简化原理图



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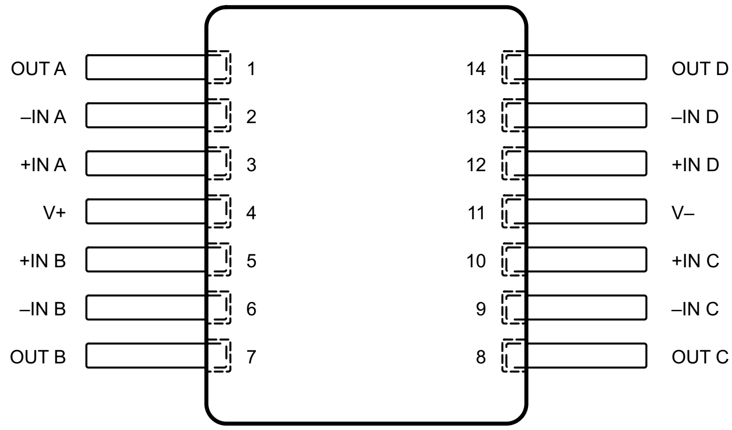
4 修订历史记录

Changes from Original (December 2016) to Revision A — **Page**

- 已更改 *更改了"特性"部分* ... 1
- 已添加 新器件封装 ... 1
- Updated *Pin Configurations and Functions* section ... 3
- Updated *Recommended Operating Conditions* table ... 6
- Updated Figure 3 ... 9

5 Pin Configuration and Functions

HFR Package
14-Pin CFP
Top View

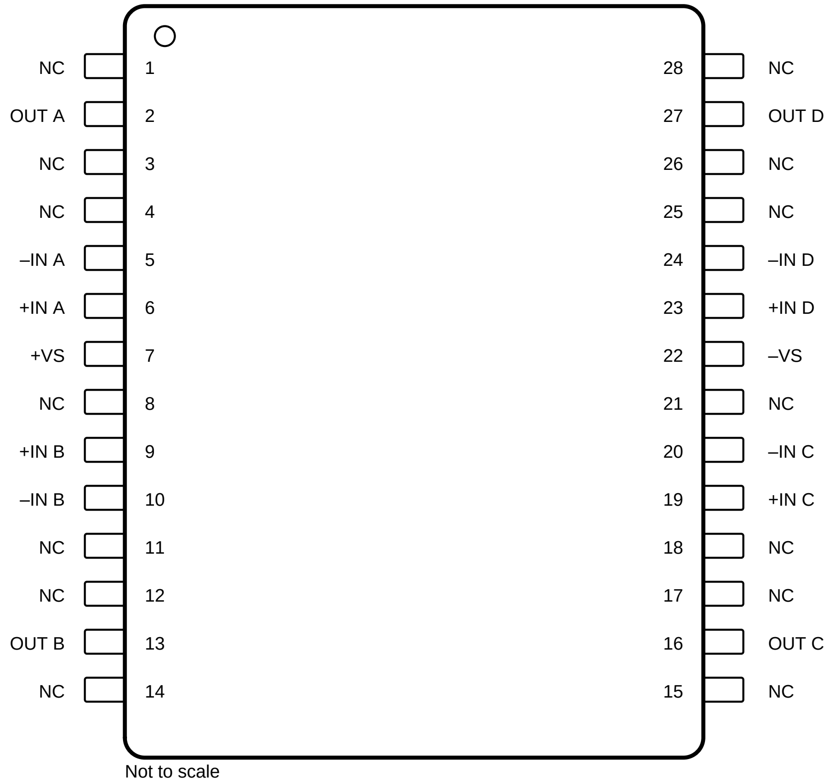


Not to scale

Pin Functions: CFP

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT A	O	Output channel A.
2	–IN A	I	Inverting input channel A.
3	+IN A	I	Noninverting input channel A.
4	V+	—	Positive (highest) power supply.
5	+IN B	I	Noninverting input channel B.
6	–IN B	I	Inverting input channel B.
7	OUT B	O	Output channel B.
8	OUT C	O	Output channel C.
9	–IN C	I	Inverting input channel C.
10	+IN C	I	Noninverting input channel C.
11	V–	—	Negative (lowest) power supply.
12	+IN D	I	Noninverting input channel D.
13	–IN D	I	Inverting input channel D.
14	OUT D	O	Output channel D.

JDJ Package
28-Pin CDIP
Top View



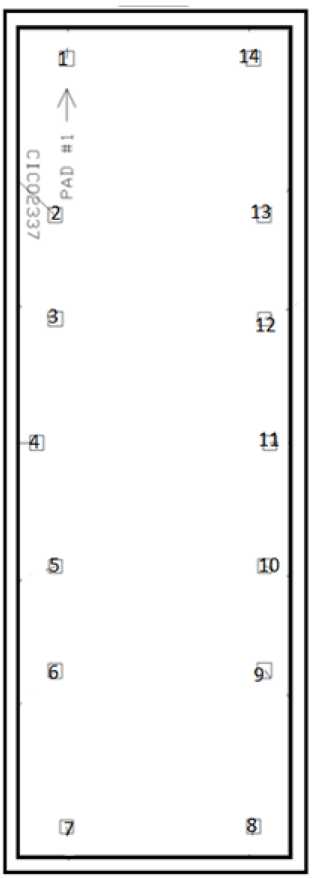
NC - no internal connection

Pin Functions: CDIP

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 3, 4, 8, 11, 12, 14, 15, 17, 18, 21, 25, 26, 28	NC	—	Not connected.
2	OUT A	O	Output (channel A).
5	–IN A	I	Inverting input (channel A).
6	+IN A	I	Noninverting input (channel A).
7	+VS	—	Positive (highest) power supply.
9	+IN B	I	Inverting input (channel B).
10	–IN B	I	Noninverting input (channel B).
13	OUT B	O	Output (channel B).
16	OUT C	O	Output (channel C).
19	+IN C	I	Inverting input (channel C).
20	–IN C	I	Noninverting input (channel C).
22	–VS	—	Negative (lowest) power supply.
23	+IN D	I	Inverting input (channel D).
24	–IN D	I	Noninverting input (channel D).
27	OUT D	O	Output (channel D).

5.1 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Negative (lower) Power Supply	AlCu (0.5%)	990 to 1210 nm



Bond Pad Coordinates in Microns(1)

PAD		I/O	DESCRIPTION	X MIN	Y MIN	X MAX	Y MAX
NO.	NAME						
1	OUT A	O	Output channel A.	1791.042	7290.340	1901.751	7401.049
2	–IN A	I	Inverting input channel A.	1701.719	6111.536	1807.397	6217.213
3	+IN A	I	Noninverting input channel A.	1701.719	5326.505	1812.429	5437.215
4	V+	—	Positive (higher) power supply.	1555.784	4390.507	1661.461	4498.700
5	+IN B	I	Noninverting input channel B.	1706.752	3462.057	1807.397	3562.702
6	–IN B	I	Inverting input channel B.	1701.719	2671.994	1807.397	2777.671
7	OUT B	O	Output channel B.	1796.074	1498.222	1896.719	1598.867
8	OUT C	O	Output channel C.	3278.071	1498.222	3383.748	1603.900
9	–IN C	I	Inverting input channel C.	3362.361	2671.994	3473.071	2782.704
10	+IN C	I	Noninverting input channel C.	3367.393	3462.057	3473.071	3567.734
11	V–	—	Negative (lower) power supply.	3407.651	4391.765	3513.329	4497.442
12	+IN D	I	Noninverting input channel D.	3367.393	5331.537	3468.038	5432.182
13	–IN D	I	Inverting input channel D.	3362.361	6111.536	3468.038	6217.213
14	OUT D	O	Output channel D.	3273.039	7290.340	3383.748	7401.049

(1) Substrate must be biased to V–, negative (lower) power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage = (V+) – (V–)		36	V
Input voltage	(V–) – 0.7	(V+) + 0.7	V
Output short circuit	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C
Storage temperature, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Dual supply voltage	±2	±18	V
	Tested supply voltage	±5	±15	V
T_J	Operating junction temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA4277-SP CDIP (JDJ) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = 25°C, V_S = ±5 V to ±15 V, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_J = 25°C, pre- and post-irradiated		±20	±65	µV
		T_J = –55°C to 125°C, pre-irradiated			±140	
dV_{OS}/d_T	Input offset voltage temperature drift	T_J = –55°C to 125°C, pre-irradiated		±0.15		µV/°C
PSRR	Input offset voltage	vs time		0.2		µV/mo
		vs power supply, V_S = ±2 V to ±18 V, T_J = 25°C, pre- and post-irradiated		±0.3	±1	µV/V
		V_S = ±2 V to ±18 V, T_J = –55°C to 125°C			±1	
	Channel separation	dc		0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_J = –55°C to 125°C			±17.5	nA
		T_J = 25°C, pre- and post-irradiated			±17.5	
I_{OS}	Input offset current	T_J = –55°C to 125°C			±17.5	nA
		T_J = 25°C, pre- and post-irradiated			±17.5	
NOISE						
	Input voltage noise	f = 0.1 to 10 Hz		0.22		$µV_{pp}$
	Input voltage noise density	f = 10 Hz		12		nV/√Hz
		f = 100 Hz		8		
		f = 1 kHz		8		
		f = 10 kHz		8		
i_n	Input noise current density	f = 1 kHz		0.2		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	T_J = 25°C, pre- and post-irradiated	(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2 V < V_{CM} < (V+) – 2 V, T_J = 25°C, post-irradiated	114	140		dB
		(V–) + 2 V < V_{CM} < (V+) – 2 V, T_J = –55°C to 125°C	114			
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common mode	(V–) + 2 V < V_{CM} < (V+) – 2 V		250 || 3		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_O = (V_O–) + 0.5 V to (V_O+) – 1.2 V, R_L = 10 kΩ		140		dB
		V_O = (V_O–) + 1.5 V to (V_O+) – 1.5 V, R_L = 2 kΩ, T_J = –55°C to 125°C	118	134		
		V_O = (V_O–) + 1.5 V to (V_O+) – 1.5 V, R_L = 2 kΩ, T_J = 25°C, pre- and post-irradiated	118	134		
		V_O = (V_O–) + 3.4 V to (V_O+) – 3.4 V, R_L = 600 Ω, V_S = ±7 V, T_J = –55°C to 125°C	118	134		
		V_O = (V_O–) + 3.4 V to (V_O+) – 3.4 V, R_L = 600 Ω, V_S = ±7 V, T_J = 25°C, pre- and post-irradiated	118	134		

Electrical Characteristics (continued)

At T_J = 25°C, V_S = ±5 V to ±15 V, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.8		V/µs
	Settling time	0.1%, 10-V step, V_S = ±15 V, G = 1		14		µs
		0.01%, 10-V step, V_S = ±15 V, G = 1		16		
THD + N	Total harmonic distortion + noise	1 kHz, G = 1, V_O = 3.5 Vrms		0.002%		
OUTPUT						
V_O	Output voltage	R_L = 10 kΩ, T_J = 25°C, pre- and post-irradiated	(V–) + 0.5		(V+) – 1.2	V
		R_L = 10 kΩ, T_J = –55°C to 125°C	(V–) + 0.5		(V+) – 1.2	
		R_L = 2 kΩ, T_J = 25°C, pre- and post-irradiated	(V–) + 1.5		(V+) – 1.5	
		R_L = 2 kΩ, T_J = –55°C to 125°C	(V–) + 1.5		(V+) – 1.5	
		T_J = 25°C, R_L = 600 Ω, pre- and post-irradiated	(V–) + 3.4		(V+) – 3.4	
		R_L = 600 Ω, V_S = ±7 V, T_J = –55°C to 125°C	(V–) + 3.4		(V+) – 3.4	
I_{SC}	Short-circuit current			±35		mA
C_{LOAD}	Capacitive load drive	f = 350 kHz, I_O = 0		See *Typical Characteristics*		
POWER SUPPLY						
V_S	Specified voltage	T_J = –55°C to 125°C	±5	±7	±15	V
		T_J = 25°C, pre- and post-irradiated	±5	±7	±15	
V_S	Operating voltage	T_J = –55°C to 125°C	±2	±7	±18	V
		T_J = 25°C, pre- and post-irradiated	±2	±7	±18	
I_Q	Quiescent current per amplifier	I_O = 0, T_J = 25°C, pre- and post-irradiated		±790	±850	µA
		I_O = 0, T_J = –55°C to 125°C			±900	

6.6 Typical Characteristics

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

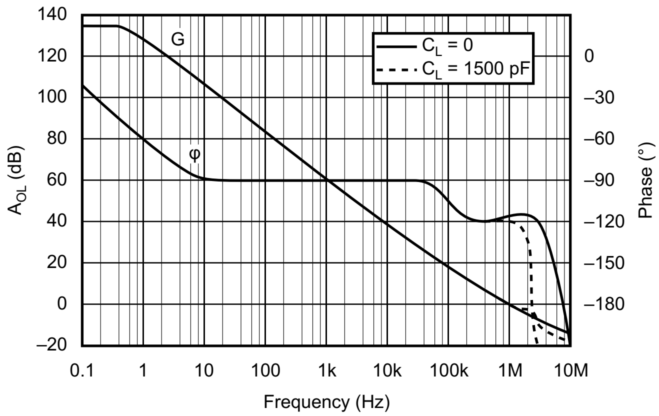


Figure 1. Open-Loop Gain/Phase vs Frequency

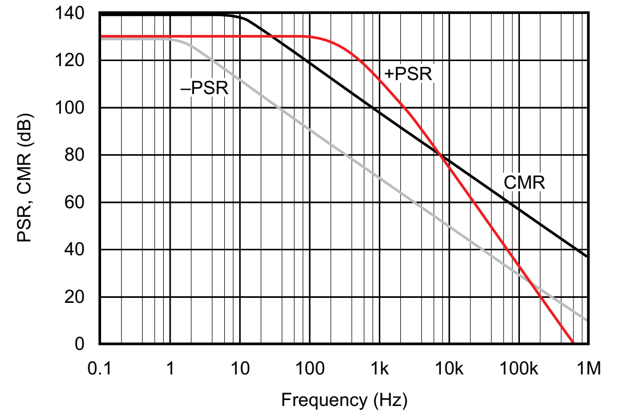


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

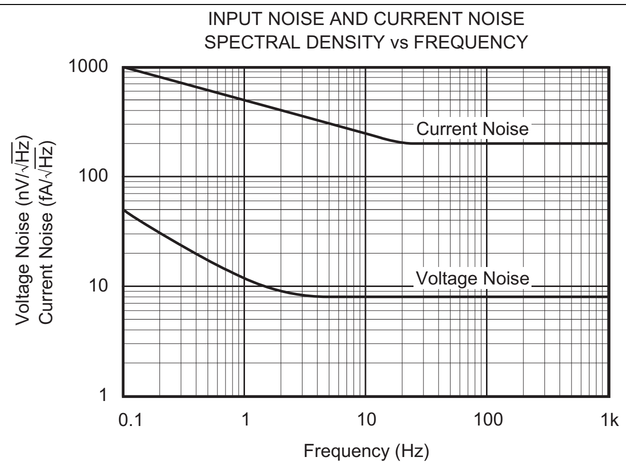
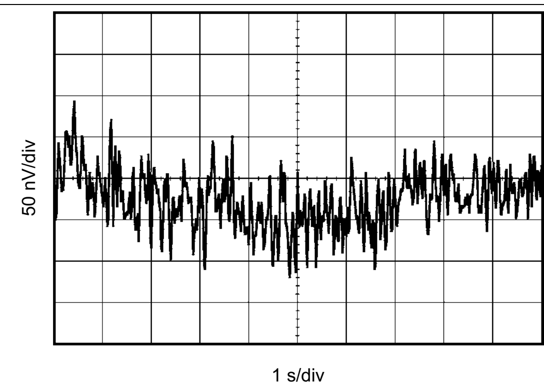
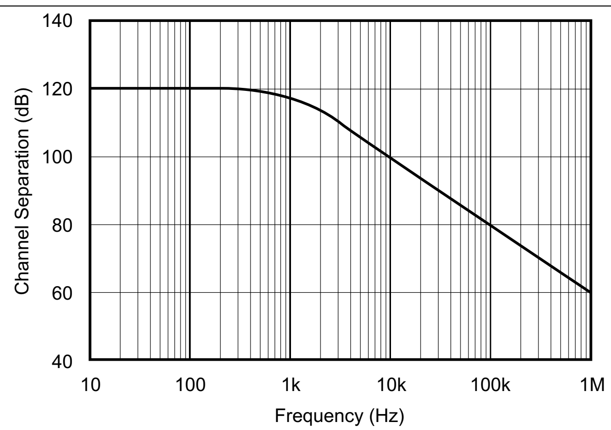


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency



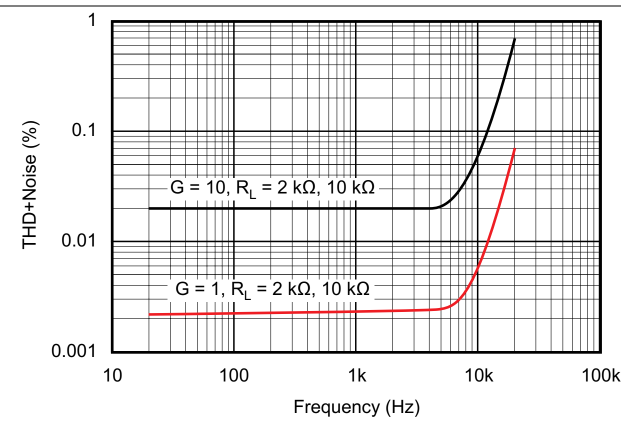
Noise signal is bandwidth limited to lie between 0.1 Hz and 10 Hz.

Figure 4. Input Noise Voltage vs Time



G = 1, measured channel A to D or B to C.
Other combinations yield similar or improved rejection.

Figure 5. Channel Separation vs Frequency



V_{OUT} = 3.5 Vrms

Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

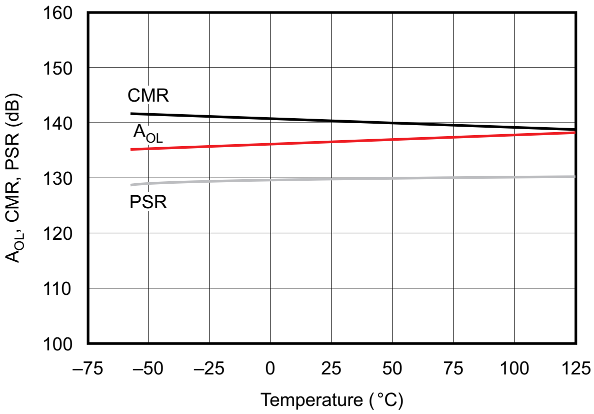
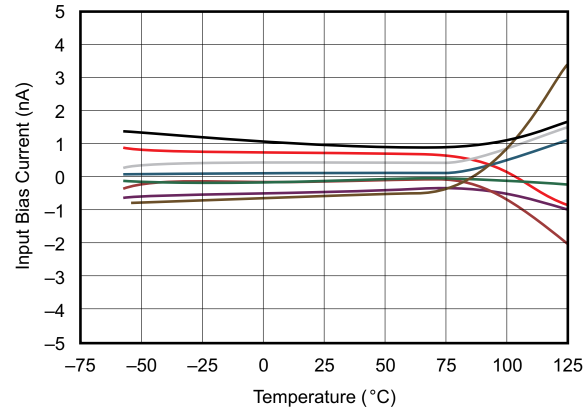


Figure 7. A_{OL}, CMR, PSR vs Temperature



Curves represent typical production units.

Figure 8. Input Bias Current vs Temperature

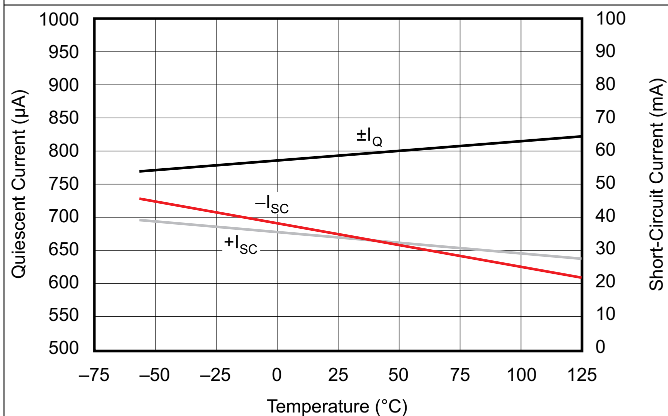
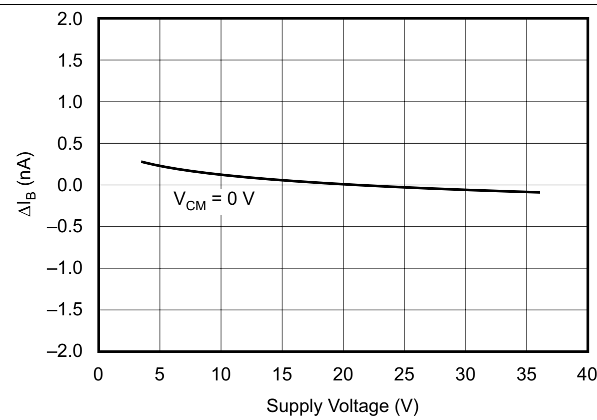
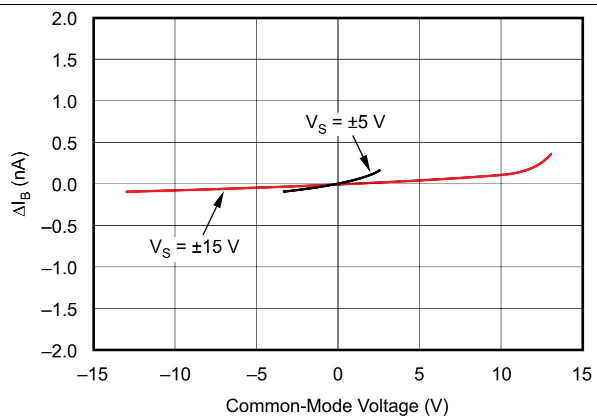


Figure 9. Quiescent Current and Short-Circuit Current vs Temperature



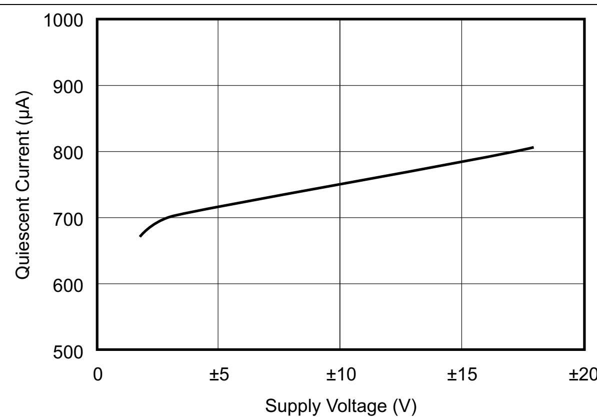
Curve shows normalized change in bias current with respect to V_S = ±10 V (+20 V). Typical I_B may range from –0.5 nA to 0.5 nA at V_S = ±10 V.

Figure 10. Change in Input Bias Current vs Power Supply Voltage



Curve shows normalized change in bias current with respect to V_{CM} = 0 V. Typical I_B may range from –0.5 nA to 0.5 nA at V_{CM} = 0 V.

Figure 11. Change in Input Bias Current vs Common-Mode Voltage



Per amplifier

Figure 12. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

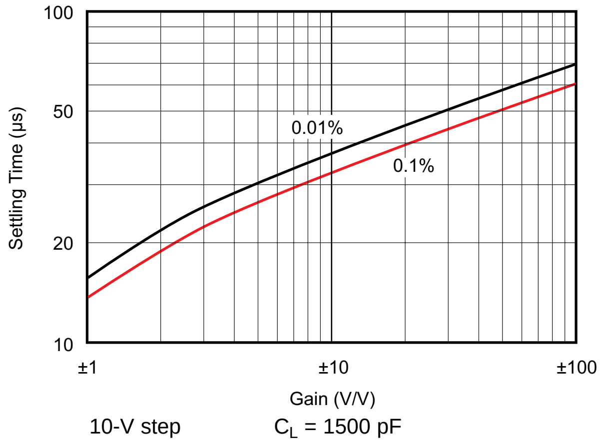


Figure 13. Settling Time vs Closed-Loop Gain

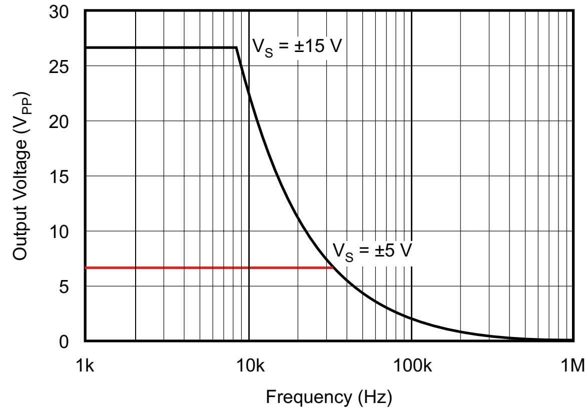


Figure 14. Maximum Output Voltage vs Frequency

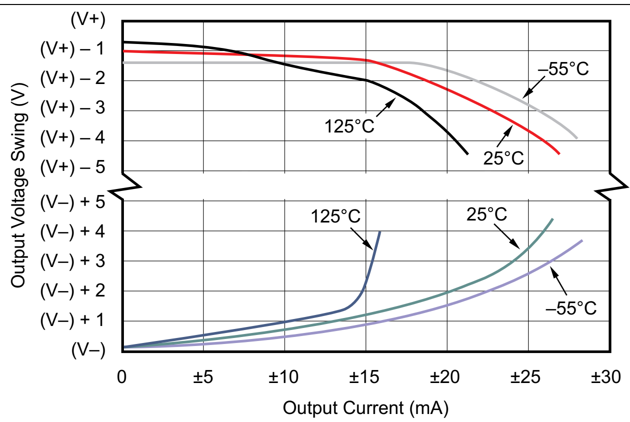


Figure 15. Output Voltage Swing vs Output Current

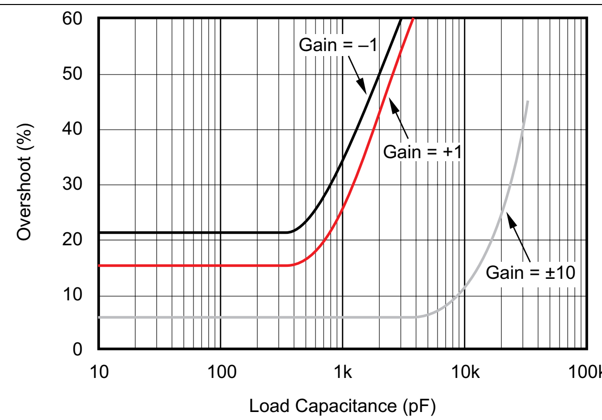


Figure 16. Small-Signal Overshoot vs Load Capacitance

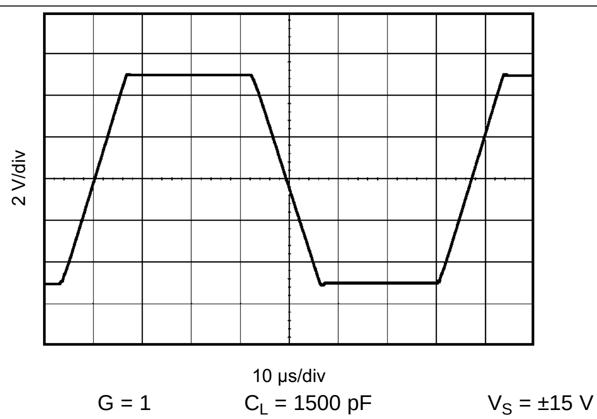


Figure 17. Large-Signal Step Response

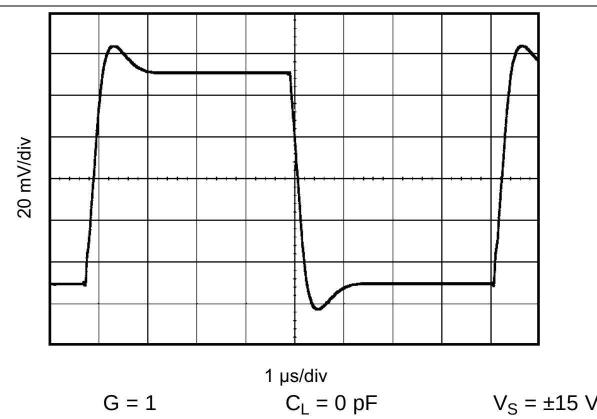


Figure 18. Small-Signal Step Response

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

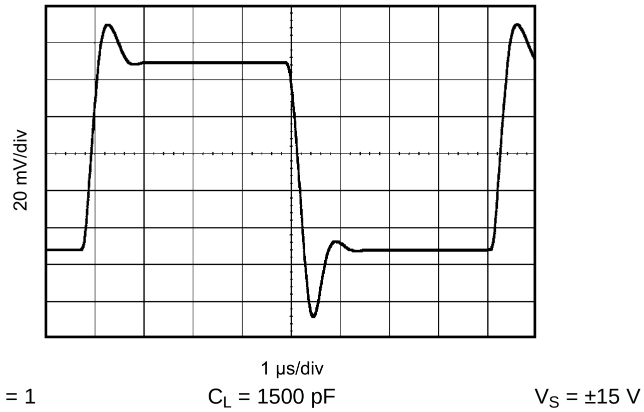


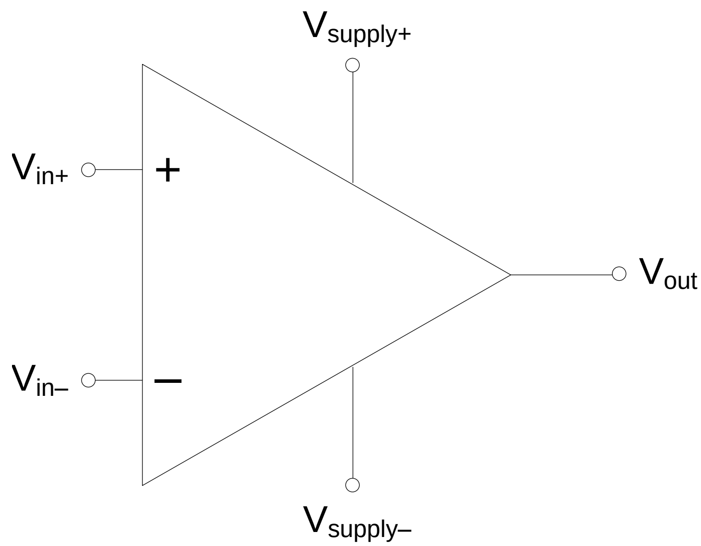
Figure 19. Small-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

7.2 Functional Block Diagram



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7.3 Feature Description

The OPA4277-SP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage (±50-µV max) is so low, user adjustment is usually not required.

7.3.1 Input Protection

The inputs of the OPA4277-SP are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

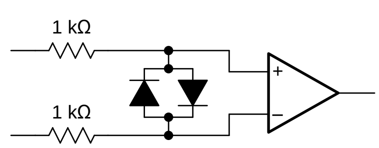


Figure 20. OPA4277-SP Input Protection

7.3.2 Input Bias Current Cancellation

The input stage base current of the OPA4277-SP is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

Feature Description (continued)

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see Figure 21). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

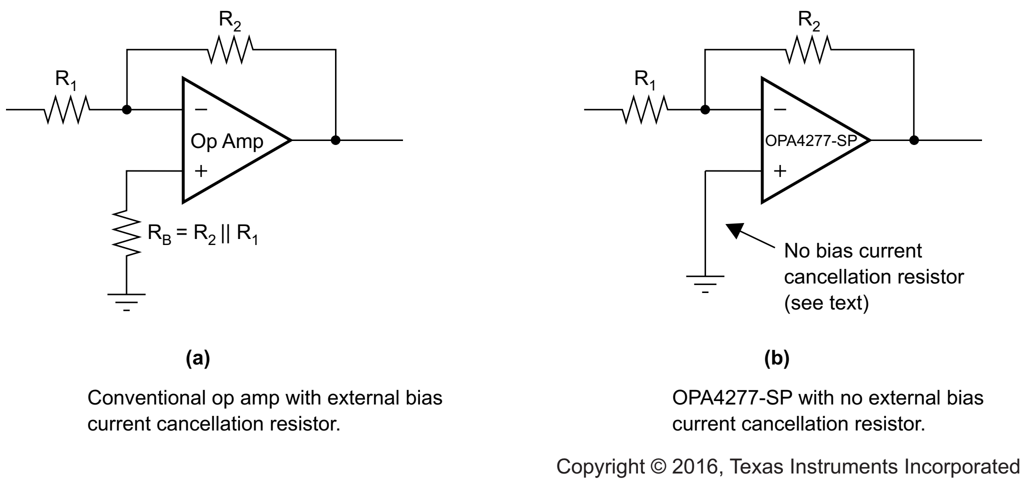


Figure 21. Input Bias Current Cancellation

7.4 Device Functional Modes

The OPA4277-SP has a single functional mode and is operational when the power-supply voltage, (V+) – (V–), is less than 36 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA4277-SP is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

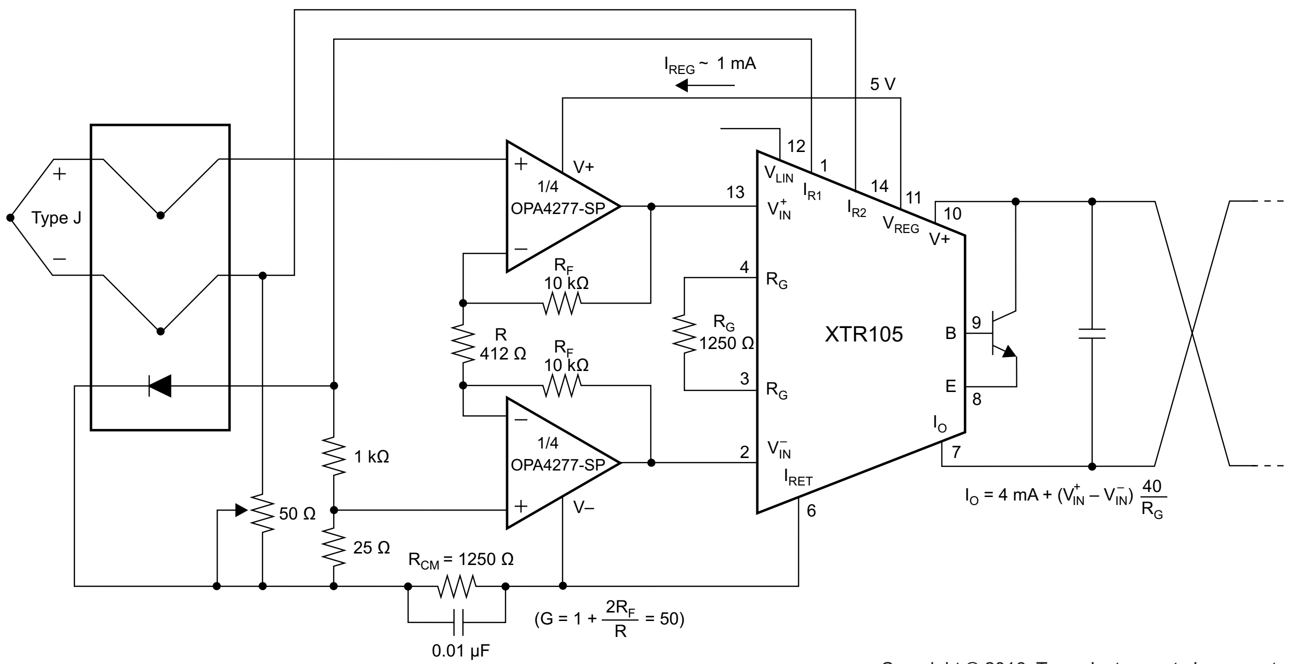


Figure 22. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

8.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation shown in Figure 22, a gain of 50 is desired.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Equation 1 shows the equation used to determine the resistor values needed for a gain of 50. Table 1 lists the design parameters.

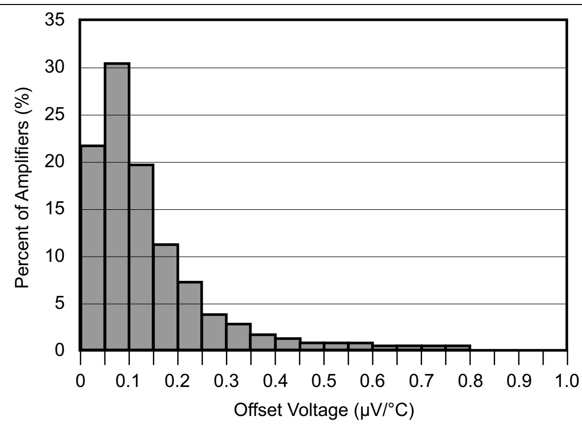
$$G = 1 + \frac{2R_F}{R} = 50 \quad (1)$$

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_F	10 kΩ
R	412 Ω

8.2.3 Application Curve

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



Typical distribution of packaged units. Single, dual, and quad included.

Figure 23. Warm-Up Offset Voltage Drift

9 Power Supply Recommendations

OPA4277-SP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. This allows a customer operating at V_S = ±10 V to have the same assured performance as a customer using ±15-V supplies. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Most behavior remains unchanged through the full operating voltage range (±2 to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in the typical performance curves.

10 Layout

10.1 Layout Guidelines

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located in *机械、封装和可订购信息* show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA4277-SP has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA4277-SP. Cancel these thermal potentials by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

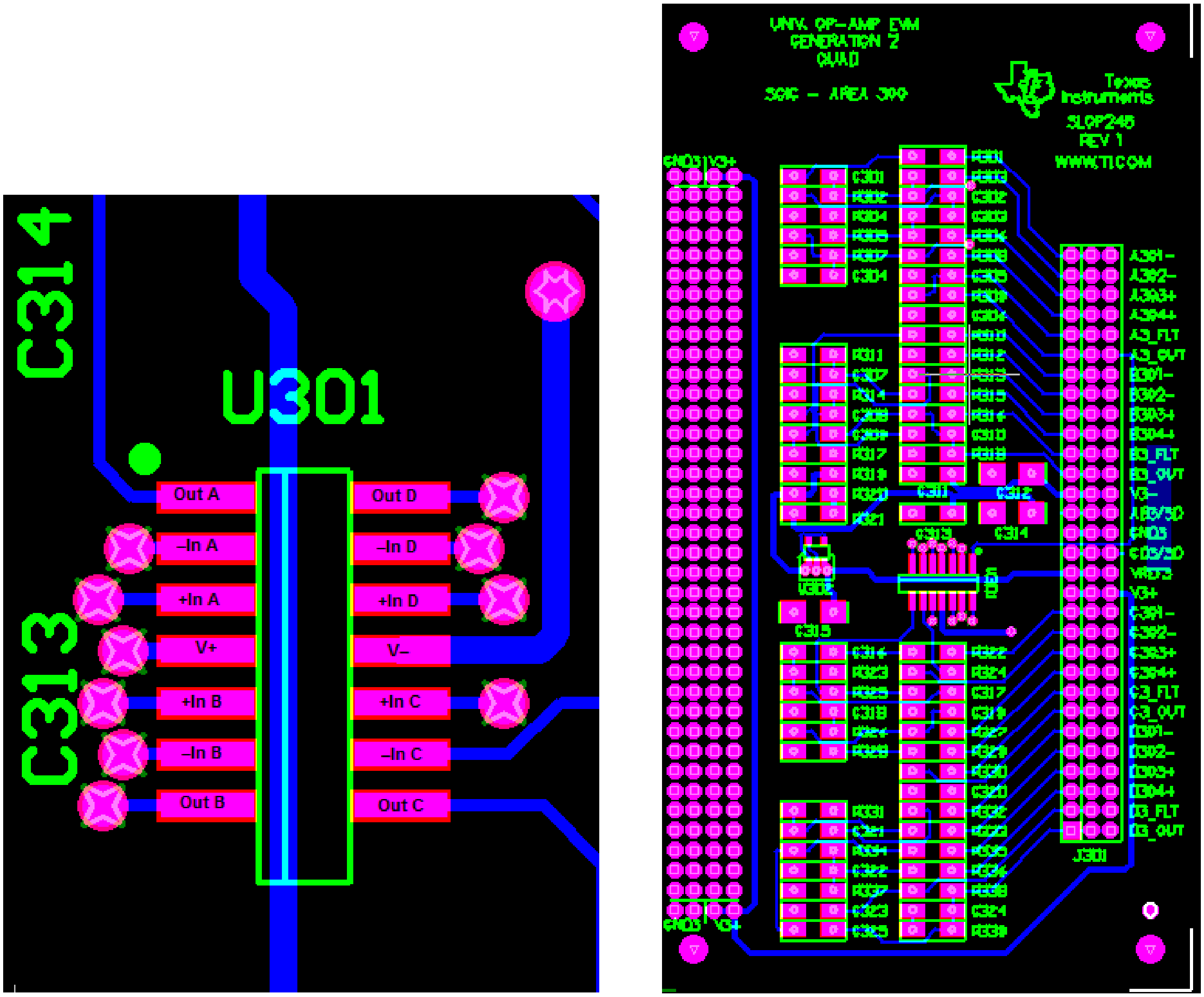


Figure 24. Board Layout Example

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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11.5 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962L1620901V9A	ACTIVE	XCEPT	KGD	0	50	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962L1620901VXA	ACTIVE	CDIP SB	JDJ	28	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962L1620901VX A OPA4277-SP	Samples
5962L1620901VYC	ACTIVE	CFP	HFR	14	1	TBD	AU	N / A for Pkg Type	-55 to 125	5962L1620901VYC OPA4277-SP	Samples
OPA4277HFR/EM	ACTIVE	CFP	HFR	14	1	TBD	AU	N / A for Pkg Type	25 to 25	OPA4277HFR/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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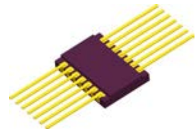
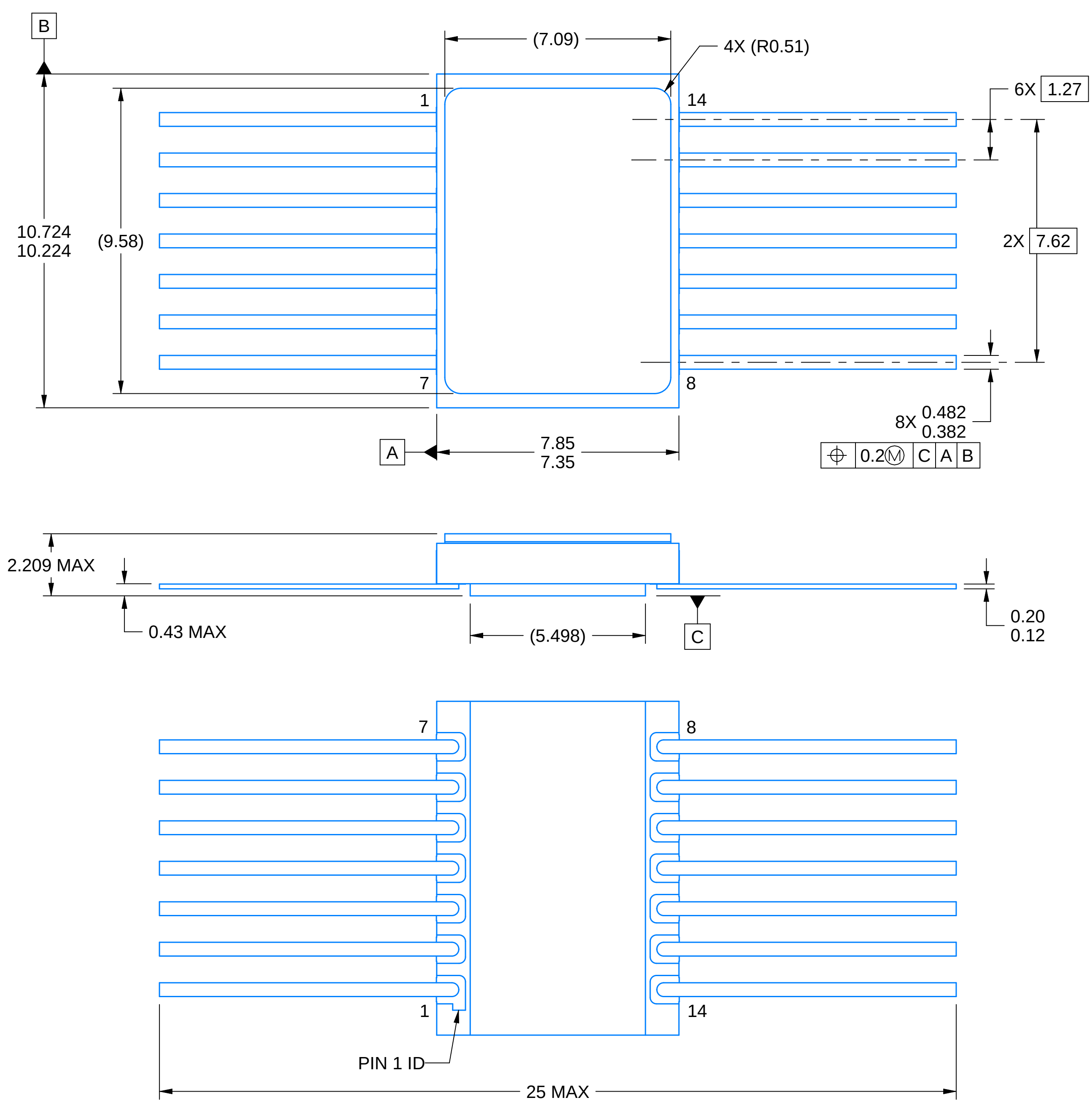


PACKAGE OUTLINE

CFP - 2.209 mm max height

CERAMIC FLATPACK

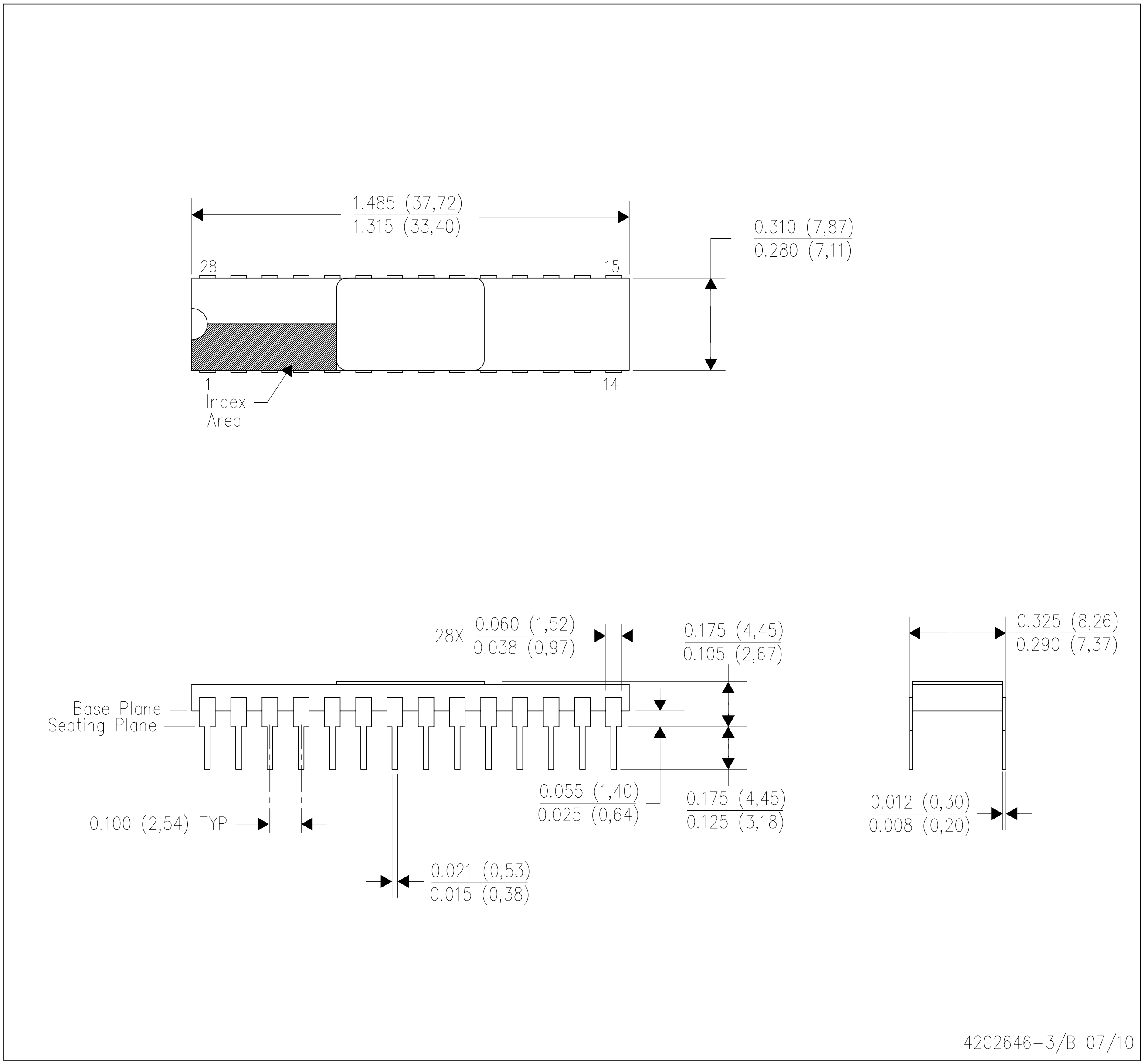


4224229/A 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.

JDJ (R–CDIP–T28) CERAMIC DUAL IN–LINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
- D. This package is hermetically sealed with a metal lid.
- E. The leads are gold plated and can be solderdipped.
- F. Leads not shown for clarity purposes.
- G. Lid and heat sink are connected to GND leads.

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