3-Channel SDTV Video Amplifier with 5th-Order Filters and 5.2-V/V Gain

FEATURES

- **Three SDTV Video Amplifiers for CVBS, S-Video, Y'P'$_B$P'$_R$ 480i/576i, Y'U'V', or G'B'R' (R'G'B')**
- **Integrated Low-Pass Filters:**
  - **5th-Order, 8.5-MHz (–3dB) Butterworth**
    - **–1dB Passband Bandwidth at 7 MHz**
    - **47 dB Attenuation at 27 MHz**
- **Versatile Input Biasing:**
  - **DC-Coupled with 230-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp**
  - **Allows AC-Coupled With DC-Biasing**
- **Built-in 5.2 V/V Gain (14.3 dB)**
- **+3-V to +5-V Single Supply Operation**
- **Rail-to-Rail Output:**
  - **Output Swings Within 100 mV of the Rails, Allowing AC- or DC-Output Coupling**
  - **Supports Driving Two Lines per Channel**
- **Low Total Quiescent Current: 15.6 mA at 3.3 V**
- **Low Differential Gain/Phase of 0.2%/0.3°**
- **Lead-free, Green SOIC-8 Package**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **PVR/DVDR Output Buffering**
- **USB/Portable Low-Power Video Buffering**

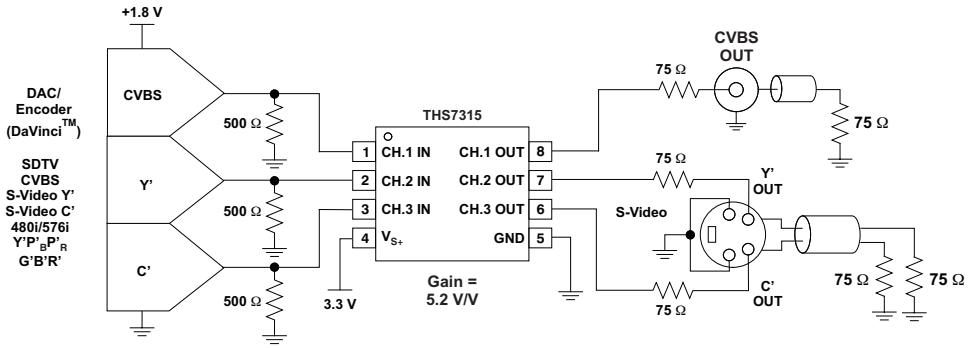
DESCRIPTION

Fabricated using the revolutionary complementary silicon-sermanium (SiGe) BiCom3 process, the THS7315 is a low-power, single-supply, 3-V to 5-V 3-channel integrated video buffer. It incorporates a 5th-order Butterworth filter that is useful as a digital-to-analog converter (DAC) reconstruction filter or an analog-to-digital converter (ADC) anti-aliasing filter. The 8.5-MHz filter is a perfect choice for SDTV video, including Composite Video Baseband Signals (CVBS), S-Video, Y'U'V', G'B'R' (R'G'B'), and Y'P'$_B$P'$_R$ 480i/576i.

The THS7315 inputs can be either ac- or dc-coupled. The 230-mV output level shift allows for a full sync dynamic range at the output with 0 V input. The ac-coupled modes include a transparent sync-tip clamp option for CVBS, Y', and G'B'R' signals with bottom-level sync. AC-coupled biasing for C'/P'$_B$/P'$_R$ channels can easily be achieved by adding an external resistor to V_{S+}.

The THS7315 is the perfect choice for all output buffer applications. Its rail-to-rail output stage with 5.2-V/V gain allows for both ac and dc line driving, making it a perfect choice for DaVinci™ processors. The ability for each channel to drive two video lines, or 75-Ω loading, allows for maximum flexibility as a video line driver. The 15.6-mA quiescent current at 3.3 V also makes it an excellent choice for USB-powered, portable, or other power-sensitive video applications

The THS7315 is available in a small SOIC-8 package that is lead-free and compliant with green requirements.



3.3-V Single-Supply DC-Input/DC-Output Coupled Video Line Driver

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS7315D	SOIC-8	Rails, 75
THS7315DR		Tape and reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

			THS7315	UNIT
	Supply voltage, V_{S+} to GND		5.5	V
V_I	Input voltage		–0.4 to V_{S+}	V
I_O	Output current		±90	mA
	Continuous power dissipation		See Dissipation Ratings Table	
T_J	Maximum junction temperature, any condition(2)		+150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		+125	°C
T_{stg}	Storage temperature range		–65 to +150	°C
	ESD ratings	HBM	2000	V
		CDM	1500	
		MM	200	

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J = +125°C)	
			T_A = +25°C	T_A = +85°C
SOIC-8 (D)	16.8	130(2)	769 mW	308 mW

(1) Power rating is determined with a junction temperature of +125°C. This temperature is the point where performance starts to degrade and long-term reliability starts to be reduced. Thermal management of the final printed circuit board (PCB) should strive to keep the junction temperature at or below +125°C for best performance and reliability.
(2) This data was taken with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is 196°C/W.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{S+}	Supply voltage	3		5	V
T_A	Ambient temperature	–40		+85	°C

ELECTRICAL CHARACTERISTICS: V_{S+} = 3.3 V

R_L = 150Ω to GND, unless otherwise noted. See Figure 1 and Figure 2.

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
AC PERFORMANCE								
Small-signal bandwidth (–3 dB)		V_O – 0.2 V_{PP} (1)	8.5	6.8/10.4	6.7/10.5	6.6/10.6	MHz	Min/Max
Large-signal bandwidth (–3 dB)		V_O – 2 V_{PP} (1)	8.5	6.8/10.4	6.7/10.5	6.6/10.6	MHz	Min/Max
Passband bandwidth (–1dB)			7.0				MHz	Typ
Attenuation (with respect to 100 kHz)		f = 6 MHz (2)	0.25	–0.3/2.4	–0.35/2.5	–0.4/2.6	dB	Min/Max
		f = 27 MHz (2)	47	36	35	34	dB	Min
Group delay		f = 100 kHz	61				ns	Typ
Group delay variation (with respect to 100 kHz)		f = 5.1 MHz	12				ns	Typ
Channel-to-channel delay			0.3				ns	Typ
Differential gain		NTSC/PAL	0.2/0.2				%	Typ
Differential phase		NTSC/PAL	0.25/0.35				degrees	Typ
Total harmonic distortion		f = 1 MHz, V_O = 2 V_{PP}, ac-coupled I/O	–62				dB	Typ
Signal-to-noise ratio		NTC-7 weighting, 100 kHz to 4.2 MHz	73				dB	Typ
Channel-to-channel crosstalk		f = 1 MHz, output-referred	–65				dB	Typ
AC gain, all channels			14.3	14/14.6	14/14.6	14/14.6	dB	Min/Max
Output impedance		f = 1 MHz	0.8				Ω	Typ
DC PERFORMANCE								
Biased output voltage		V_{IN} = 0 V	230	80/390	68/415	48/420	mV	Min/Max
Input voltage range		DC input, limited by output	–0.1/0.56				V	Typ
Sync tip clamp charge current		V_{IN} = –0.1 V	200				µA	Typ
Input resistance			800				kΩ	Typ
Input capacitance			2				pF	Typ
OUTPUT CHARACTERISTICS								
High output voltage swing		R_L = 150 Ω to 1.65 V	3.15				V	Typ
		R_L = 150 Ω to GND	3.10	2.85	2.75	2.75	V	Min
		R_L = 75 Ω to 1.65 V	3.10				V	Typ
		R_L = 75 Ω to GND	3.0				V	Typ
Low output voltage swing		R_L = 150 Ω to 1.65 V (V_{IN} = –0.15 V)	0.15				V	Typ
		R_L = 150 Ω to GND (V_{IN} = –0.15 V)	0.05	0.13	0.14	0.14	V	Max
		R_L = 75 Ω to 1.65 V (V_{IN} = –0.15 V)	0.26				V	Typ
		R_L = 75 Ω to GND (V_{IN} = –0.15 V)	0.1				V	Typ
Output current	Sourcing	R_L = 10 Ω to 1.65 V	80				mA	Typ
	Sinking		70				mA	Typ
POWER SUPPLY								
Maximum operating voltage			3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage			3.3	2.85	2.85	2.85	V	Min
Maximum quiescent current		V_{IN} = 0 V	15.6	20	22	24	mA	Max
Minimum quiescent current		V_{IN} = 0 V	15.6	12	11.6	11	mA	Min
Power supply rejection (+PSRR)			43				dB	Typ

(1) The Min/Max values listed for this specification are specified by design and characterization only.
(2) 3.3-V supply filter specifications are specified by 100% testing at 5-V supply along with design and characterization only.

ELECTRICAL CHARACTERISTICS: V_{S+} = 5 V

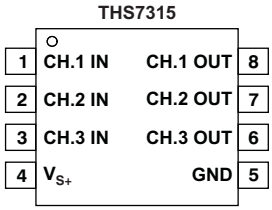
R_L = 150Ω to GND, unless otherwise noted. See Figure 1 and Figure 2.

PARAMETER		TEST CONDITIONS	TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNIT	MIN/MAX/ TYP
AC PERFORMANCE								
Small-signal bandwidth (–3 dB)		V_O – 0.2 V_{PP} (1)	8.5	6.8/10.4	6.7/10.5	6.6/10.6	MHz	Min/Max
Large-signal bandwidth (–3 dB)		V_O – 2 V_{PP} (1)	8.5	6.8/10.4	6.7/10.5	6.6/10.6	MHz	Min/Max
Passband bandwidth (–1dB)			7.0				MHz	Typ
Attenuation (with respect to 100 kHz)		f = 6 MHz	0.25	–0.3/2.4	–0.35/2.5	–0.4/2.6	dB	Min/Max
		f = 27 MHz	47	36	35	34	dB	Min
Group delay		f = 100 kHz	61				ns	Typ
Group delay variation (with respect to 100 kHz)		f = 5.1 MHz	11				ns	Typ
Channel-to-channel delay			0.3				ns	Typ
Differential gain		NTSC/PAL	0.2/0.2				%	Typ
Differential phase		NTSC/PAL	0.3/0.35				degrees	Typ
Total harmonic distortion		f = 1 MHz, V_O = 2 V_{PP}, ac-coupled I/O	–61				dB	Typ
Signal-to-noise ratio		NTC-7 weighting, 100 kHz to 4.2 MHz	73				dB	Typ
Channel-to-channel crosstalk		f = 1 MHz, output-referred	–65				dB	Typ
AC gain, all channels			14.3	14/14.6	14/14.6	14/14.6	dB	Min/Max
Output impedance		f = 1 MHz	0.8				Ω	Typ
DC PERFORMANCE								
Bias output voltage		V_{IN} = 0 V	235	80/390	68/415	48/420	mV	Min/Max
Input voltage range		Limited by output	–0.1/0.9				V	Typ
Sync tip clamp charge current		V_{IN} = –0.1 V	200				µA	Typ
Input resistance			800				kΩ	Typ
Input capacitance			2				pF	Typ
OUTPUT CHARACTERISTICS								
High output voltage swing		R_L = 150 Ω to 2.5 V	4.85				V	Typ
		R_L = 150 Ω to GND	4.7	4.4	4.3	4.25	V	Min
		R_L = 75 Ω to 2.5 V	4.8				V	Typ
		R_L = 75 Ω to GND	4.5				V	Typ
Low output voltage swing		R_L = 150 Ω to 2.5 V (V_{IN} = –0.15 V)	0.2				V	Typ
		R_L = 150 Ω to GND (V_{IN} = –0.15 V)	0.05	0.14	0.16	0.18	V	Max
		R_L = 75 Ω to 2.5 V (V_{IN} = –0.15 V)	0.35				V	Typ
		R_L = 75 Ω to GND (V_{IN} = –0.15 V)	0.07				V	Typ
Output current	Sourcing	R_L = 10 Ω to 2.5 V	90				mA	Typ
	Sinking		85				mA	Typ
POWER SUPPLY								
Maximum operating voltage			5	5.5	5.5	5.5	V	Max
Minimum operating voltage			5	2.85	2.85	2.85	V	Min
Maximum quiescent current		V_{IN} = 0 V	16.5	22	24	25	mA	Max
Minimum quiescent current		V_{IN} = 0 V	16.5	12.5	12	11.5	mA	Min
Power supply rejection (+PSRR)			44				dB	Typ

(1) The Min/Max values listed for this specification are specified by design and characterization only.

PIN CONFIGURATION

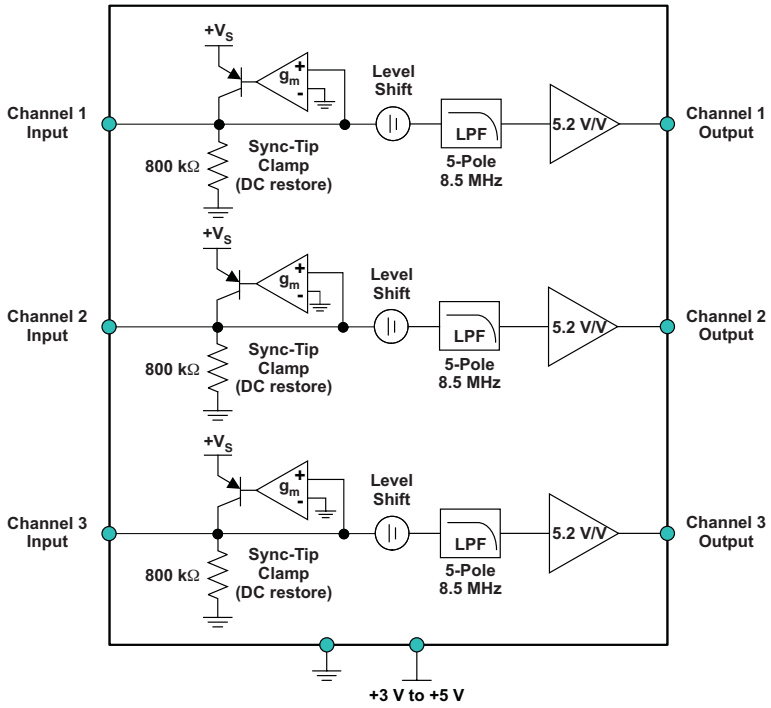
SOIC-8 (D)
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. (SOIC-8)		
CH. 1 IN	1	I	Video Input, Channel 1
CH. 2 IN	2	I	Video Input, Channel 2
CH. 3 IN	3	I	Video Input, Channel 3
V_{S+}	4	I	Positive Power Supply Pin. Connect to 3 V to 5 V.
GND	5	I	Ground pin for all internal circuitry.
CH. 3 OUT	6	O	Video Output, Channel 3
CH. 2 OUT	7	O	Video Output, Channel 2
CH. 1 OUT	8	O	Video Output, Channel 1

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

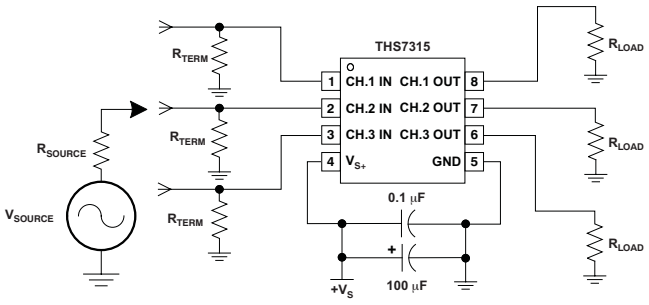


Figure 1. DC-Coupled Input and Output Test Circuit

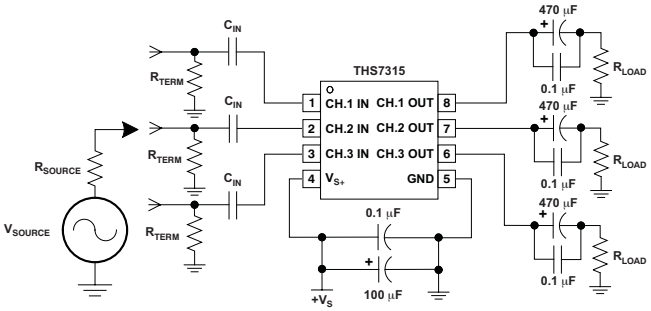


Figure 2. AC-Coupled Input and Output Test Circuit

APPLICATION INFORMATION

The THS7315 is targeted for standard definition (SD) video output buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7315. Built on the revolutionary complementary silicon-germanium (SiGe) BiCom3 process, the THS7315 incorporates many features not typically found in integrated video parts while consuming very low power.

The THS7315 has the following features:

- Single-supply 3-V to 5-V operation with low total quiescent current of 15.6 mA at 3.3 V and 16.5 mA at 5 V.
- Input configuration accepting dc + level-shift, ac sync-tip clamp, or ac bias selection; ac-biasing is accomplished with the use of an external pull-up resistor to the positive power supply.
- 5th-order low-pass filter for DAC reconstruction or ADC image rejection:
  - 8.5-MHz for NTSC, PAL, SECAM, Composite (CVBS), S-Video Y'C', 480i/576i $Y'P'_BP'_R$, and G'B'R' (R'G'B') signals.
- Internal fixed gain of 5.2 V/V (+14.3 dB) buffer that can drive up to two video lines per channel with dc coupling or traditional ac coupling.
- Signal flow-through configuration using an 8-pin SOIC package that complies with the latest lead-free (RoHS compatible) and green manufacturing requirements.

OPERATING VOLTAGE

The THS7315 is designed to operate from 3 V to 5 V over a –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible because of the implementation of thin film resistors and high-quality, low temperature coefficient capacitors. The design of the THS7315 allows operation down to 2.85 V, but for best results, the use of a 3 V or greater supply should be used to ensure there are no issues with headroom or clipping.

A 0.1-µF to 0.01-µF capacitor should be placed as close as possible to the power-supply pins. Failure to do so may result in the THS7315 outputs ringing or oscillating. Additionally, a large capacitor, such as 22 µF to 100 µF, should be placed on the power-supply line to minimize interference with 50-Hz/60-Hz line frequencies.

INPUT VOLTAGE

The THS7315 input range allows for an input signal range from –0.3 V to approximately (V_{S+} – 1.5V). However, because of the internal fixed gain of 5.2 V/V (+14.3 dB) and the internal level shift that shifts the output by 230 mV, the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.3 V to +3.5 V. As a result of the gain and level shift, the linear output range limits the allowable linear input range from about –0.1 V to +2.3 V.

APPLICATION INFORMATION (continued)

INPUT OVERVOLTAGE PROTECTION

The THS7315 is built using a very high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 3.

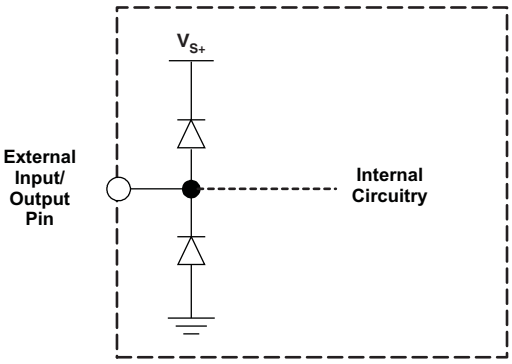


Figure 3. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

TYPICAL CONFIGURATION and VIDEO TERMINOLOGY

A typical application circuit using the THS7315 as a video buffer is shown in Figure 4. It shows a video DAC output, such as the DaVinci, driving the three input channels of the THS7315. Although the S-Video Y'/C' channels and the composite video (CVBS) channel of an SD video system are shown, these channels can easily be the $Y'P'_BP'_R$ (sometimes labeled Y'U'V' or incorrectly labeled $Y'C'_BC'_R$) signals of a 480i or 576i system. These signals can also be G'B'R' (R'G'B') signals or other variations. Note that for computer signals, the sync should be embedded within the signal for a system with only three outputs. This configuration is sometimes labeled as R'G'sB' (sync on green) or R'sG'sB's (sync on all signals).

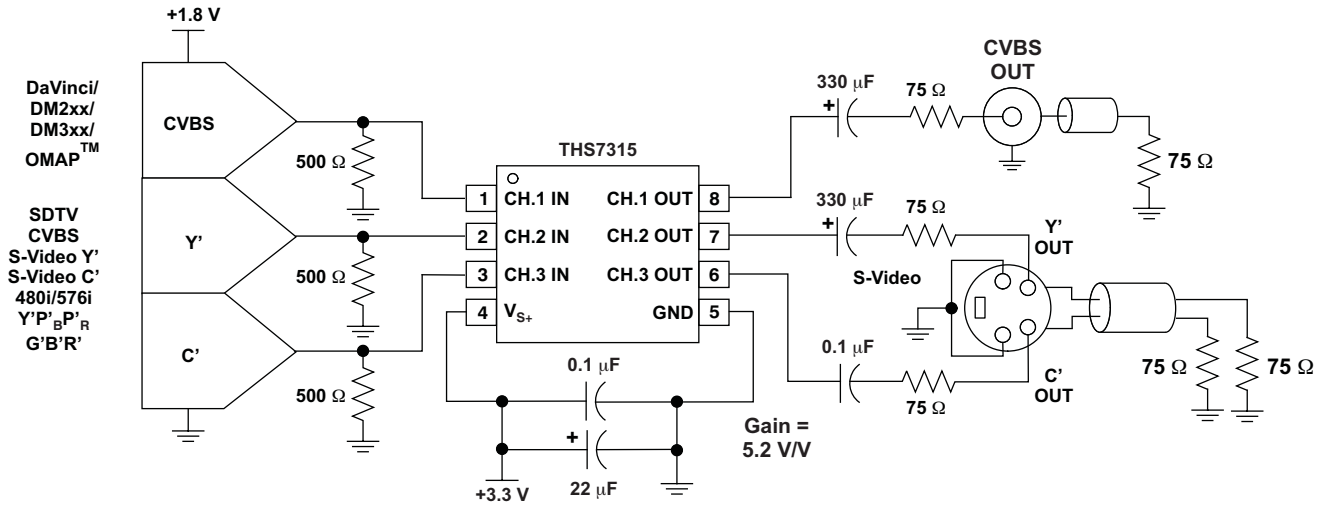


Figure 4. Typical SDTV CVBS/Y'/C' Inputs From DC-Coupled Encoder/DAC With AC-Coupled Line Driving

APPLICATION INFORMATION (continued)

Note that the Y' term is used for the luma channels throughout this document rather than the more common luminance (Y) term. The reason for this usage is to account for the definition of luminance as stipulated by the CIE (International Commission on Illumination). Video departs from true luminance because a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Therefore, true luminance (Y) is not maintained, and thus a difference in terminology arises.

This rationale is also used for the chroma (C') term. Chroma is derived from the nonlinear R'G'B' terms and therefore it is also nonlinear. True chominance (C) is derived from linear RGB, and thus the difference between chroma (C') and chrominance (C) exists. The color difference signals (P'_B/ P'_R/U'/V') are also referenced this way to denote the nonlinear (gamma-corrected) signals.

R'G'B' (commonly mislabeled RGB) is also called G'B'R' (again commonly mislabeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This approach is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectively. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels; this configuration may not always be the case for all systems.

INPUT MODE OF OPERATION—DC

The THS7315 allows for both ac-coupled and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7315. One of the drawbacks to dc-coupling, however, occurs when 0 V is applied to the input. Although the THS7315 allows for a 0-V input signal with no issues, the output swing of a traditional amplifier cannot yield a 0-V signal, resulting in possible clipping. This condition is true for any single-supply amplifier because of the output transistor limitations. Both CMOS and bipolar transistors cannot go to 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce both the horizontal and vertical sync amplitudes on the video signal. A problem occurs if the video signal receiver uses an AGC loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This effect may result in a picture with an overly bright display and too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control, and a reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation and/or clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other signal aberrations.

To eliminate saturation or clipping problems, the THS7315 has a 230 mV output level shift feature. This feature takes the input voltage and adds an internal level shift to the signal. The THS7315 rail-to-rail output stage can create this output level while connected to a typical video load. This process ensures that no saturation or clipping of the sync signal occurs. This level shift is constant, regardless of the input signal. For example, if a 0.5-V input is applied, the output is at (0.5 V $\times$ 5.2 V/V) + 0.23 V = 2.92 V.

The fixed internal gain of 5.2 V/V (14.3 dB) dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is about 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input will be [(3.1 V – 0.23 V) / 5.2 V/V)] = 0.55 V. This relationship holds true up to the maximum recommended 5 V power supply that allows an approximate input range of [(4.9 V – 0.23 V) / 5.2 V/V)] = 0.9 V while avoiding clipping on the output.

APPLICATION INFORMATION (continued)

The THS7315 input impedance in this operating mode is dictated by the internal 800-kΩ pull-down resistor, as shown in Figure 5. Note that the internal voltage shift does not appear at the input pin, but only at the output pin.

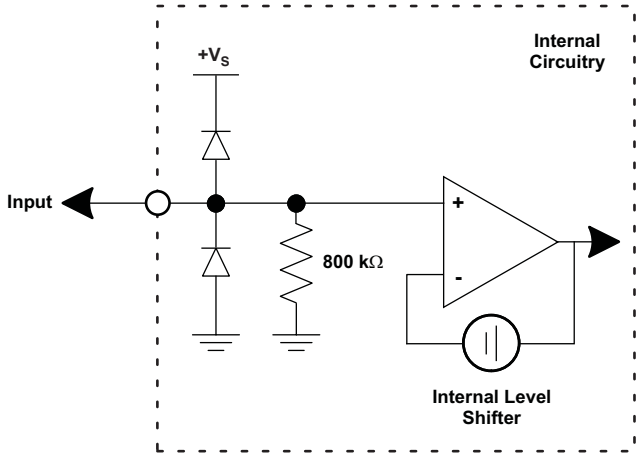


Figure 5. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION —AC SYNC-TIP CLAMP

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. These DACs typically only sink current, rather than the more traditional current-sourcing DAC where the resistor is referenced to ground. The resulting video signal voltages can be too high for a dc-coupled video buffer to function properly. To account for this scenario, the THS7315 incorporates a sync-tip clamp (STC) circuit. This function requires a capacitor (nominally 0.1 µF) to be placed in series with the input. Note that while the term *sync-tip clamp* or STC is used throughout this document, it should be noted that the THS7315 is better termed as a *dc-restoration circuit* based on how this function is performed. The STC circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7315 has an internal control loop that sets the lowest input-applied voltage to clamp at ground (0 V). By setting the reference at 0 V, the THS7315 allows a dc-coupled input to also function. Therefore, the STC is considered transparent because it does not operate unless the input signal goes below ground. The signal then goes through the same internal level shifter, resulting in an output voltage low level of 230 mV. If the input signal tries to go below 0 V, the internal control loop of the THS7315 will source up to 2 mA of current to increase the THS7315 input voltage level on the input side of the coupling capacitor. As soon as the voltage goes above 0 V, the loop will stop sourcing current and become very high impedance.

One of the concerns about the STC level is how the clamp reacts to a sync edge that has overshoot—a common effect in VCR signals or reflections found in poor PCB layouts. Ideally, the STC should not react to the overshoot voltage of the input signal. Otherwise, this effect could result in clipping on the rest of the video signal because it may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7315 has an internal low-pass filter as shown in Figure 6. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but generally, it is about a 100-ns delay. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage, but rather the flat portion of the sync signal.

APPLICATION INFORMATION (continued)

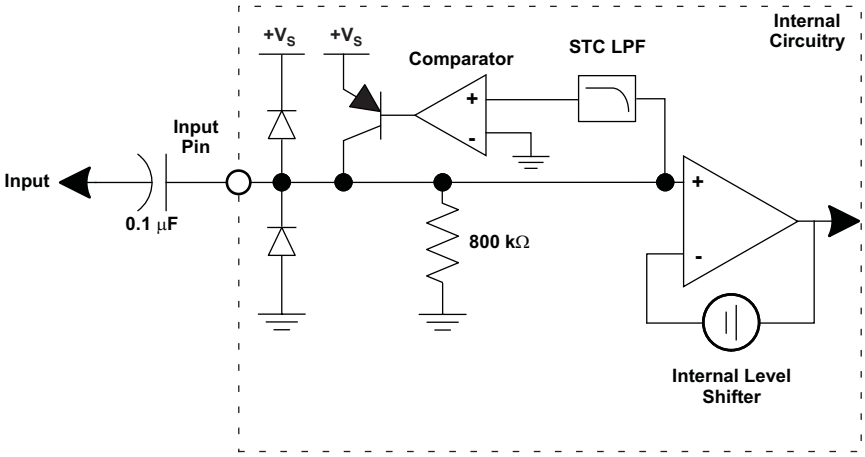


Figure 6. Equivalent AC Sync-Tip Clamp Input Circuit

As a result of the delay, the sync may have an apparent voltage shift. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because the sync is primarily for timing purposes—with syncs occurring on the edge of the sync signal—this shift is transparent in most systems.

While this feature may not fully eliminate overshoot issues on the input signal in cases of extreme overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional way to minimize this problem, an external capacitor (for example, 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that the STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage appearing at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line, ensuring a very robust STC system.

When using the ac sync-tip clamp operation, there must also be some finite amount of discharge bias current. As previously discussed, if the input signal goes below the 0 V clamp level, the THS7315 internal loop will source current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0 V reference level increases, the amount of source current increases proportionally—supplying up to 2 mA of current. As a result, the time to re-establish the proper STC voltage can be very short. If this difference is very small, then the source current will also be very small to account for minor voltage droop.

What happens if the input signal goes above the 0 V input level? The problem is that the video signal will always be above this level and must not be altered in any way. If the sync level of the input signal is above 0 V, however, then the internal discharge (sink) current will reduce the ac-coupled bias signal to the proper 0 V level.

This discharge current must not be large enough to significantly alter the video signal, or picture quality issues may arise. This effect is often seen by looking at the tilt (or *droop*) of a constant luma signal being applied and observing the resulting output level. The associated change in luma level from the beginning of the video line to the end of the video line is the amount of droop.

If the discharge current is very small, the amount of tilt (or droop) is very low, which is a generally a good thing. Unfortunately, the amount of time for the system to capture the sync signal could be too long. This effect is also termed *hum rejection*. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The values of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

APPLICATION INFORMATION (continued)

To allow for both dc-coupling and ac-coupling in the same part, the THS7315 incorporates an 800-kΩ resistor to ground. Although a true constant current sink is preferred over a resistor, there are significant issues when the voltage is near ground. (For example, voltage near ground can cause the current sink transistor to saturate and produce potential signal problems.) This resistor is large enough to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is utilized. If the video signal is 0.5 V, then there will be 0.5 V / 800 kΩ = 0.625 µA of discharge current. If more hum rejection is desired or there is a loss of sync occurring, simply decrease the 0.1 µF input coupling capacitor. A decrease from 0.1 µF to 0.047 µF increases the hum rejection by a factor of 2:1. Alternatively, an external pull-down resistor to ground may be added, decreasing the overall resistance and ultimately increasing the discharge current.

To ensure proper stability of the ac STC control loop, the source impedance must be less than 1 kΩ with the input capacitor in place. Otherwise, there is a possibility of the control loop ringing. This ringing may appear on the THS7315 output. Because most DACs or encoders use resistors that are typically ≤ 500 Ω to establish the voltage, meeting the < 1 kΩ requirement is easily done. However, if the source impedance looking from the THS7315 input is very high, then simply adding a 1-kΩ resistor to GND will ensure proper operation of the THS7315.

INPUT MODE OF OPERATION —AC BIAS

Sync-tip clamps work very well for signals that have horizontal and/or vertical syncs associated with them. Some video signals, on the other hand, do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then a dc bias is required to properly set the dc operating point within the THS7315. This function is easily accomplished with the THS7315 by simply adding an external pull-up resistor to the positive power supply, as shown in Figure 7.

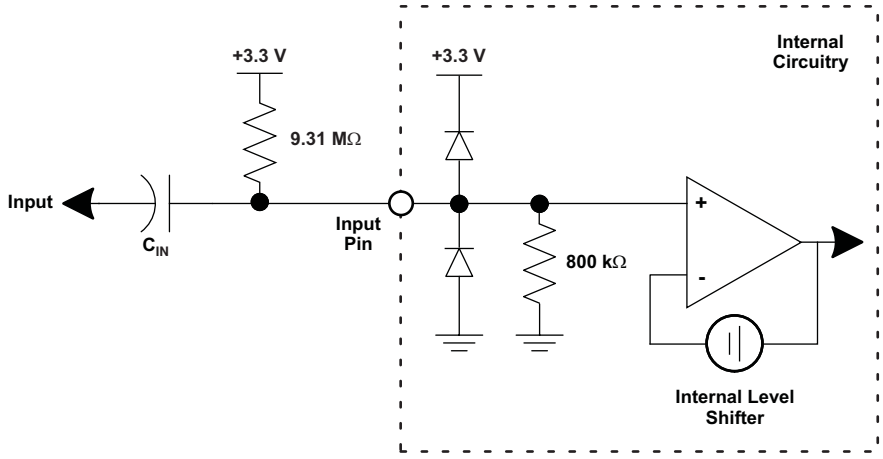


Figure 7. AC-Bias Input Mode Circuit Configuration

The dc voltage appearing at the input pin is approximately equal to:

$$V_{DC} = V_S\left(\frac{800k}{800k + R_{PU}}\right) \quad (1)$$

The allowable input range of the THS7315 is very wide: approximately ($+V_S$ – 1.5 V). The input range is limited by the allowable output voltage range and the internal gain. As such, the input dc bias point is very flexible, with the output dc bias point being the primary factor. For example, if the desired output dc bias point is 1.6 V on a 3.3-V supply, then the input dc bias point should be (1.6 V – 230 mV) / 5.2 = 0.263 V. Consequently, the pull-up resistor calculates to be about 9.31 MΩ, resulting in 0.261 V. If the desired input dc-bias point is 2.4 V with a 5-V power supply, then the pull-up resistor calculates to be about 8.66 MΩ.

Keep in mind that the internal 800-kΩ resistor has approximately a ±20% variance. As such, the calculations should account for this variance. For the 0.261 V example above, using an ideal 9.31-MΩ resistor, the input dc bias voltage is about 0.261 V ±0.05 V, which translates to an output bias voltage of about 1.64 V ±0.26 V.

APPLICATION INFORMATION (continued)

One other issue that must be taken into account is the dc-bias point. The dc-bias point is a function of the power supply. As such, there is as a low-pass filter. Additionally, the time to charge the capacitor to the final dc bias point is also a function of the pull-up resistor and the input capacitor. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. Generally, it is good to have this high-pass filter at about 3 Hz to minimize any potential droop on a P'_B, P'_R, or non-sync B' or R' signal. A 0.1-µF input capacitor with a 9.31-MΩ pull-up resistor equals about a 2.2-Hz high-pass corner frequency.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', V', and non-sync B' and/or R' signals.

OUTPUT MODE OF OPERATION—DC-COUPLED

The THS7315 incorporates a rail-to-rail output stage that can be utilized to drive the line directly without the need for large ac-coupling capacitors, as shown in Figure 8. This architecture offers the best line tilt and field tilt (or droop) performance because no ac coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt arising from the input ac coupling is still seen on the output, regardless of the output coupling. The 80-mA output current drive capability of the THS7315 was designed to drive two video lines per channel simultaneously—essentially, a 75-Ω load—while keeping the output dynamic range as wide as possible.

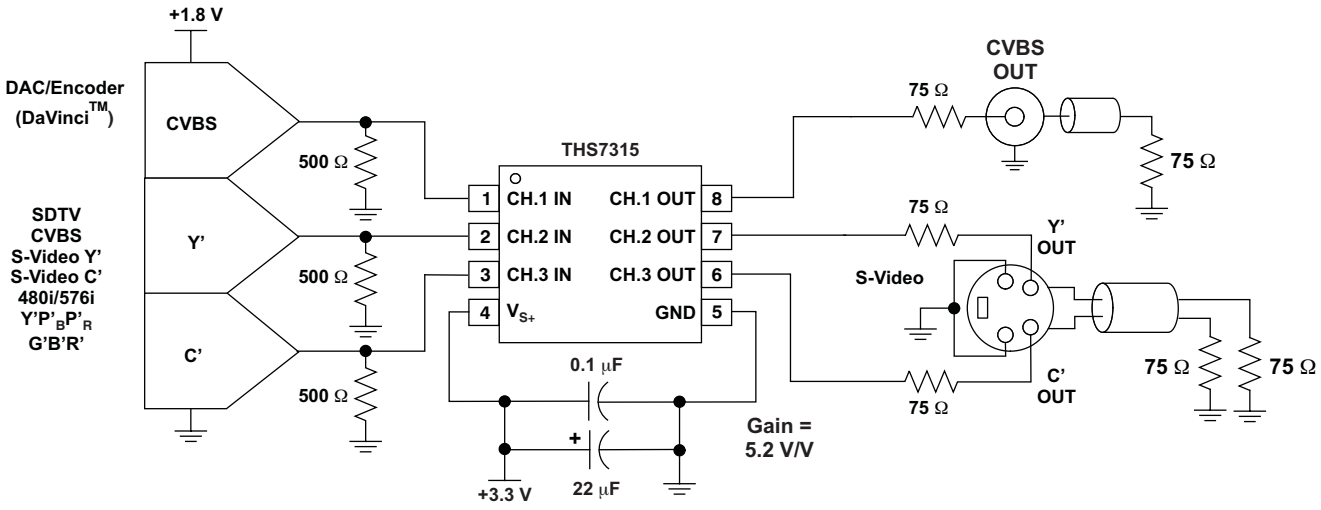


Figure 8. Typical SDTV CVBS/Y'/C' System with DC-Coupled Line Driving

One concern about dc coupling arises when the line is terminated to ground. If the ac-bias input configuration is used, the THS7315 output has a dc bias on the output. With two lines terminated to ground, this configuration creates a dc current path, resulting in a slightly decreased high output voltage swing as well as an increase in device power dissipation. While the THS7315 was designed to operate with junction temperatures of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level; otherwise, long-term reliability could suffer. Although this configuration only adds less than 10 mW of power dissipation per channel, the overall low power dissipation of the THS7315 design minimizes potential thermal issues even when using the SOIC package at high ambient temperatures.

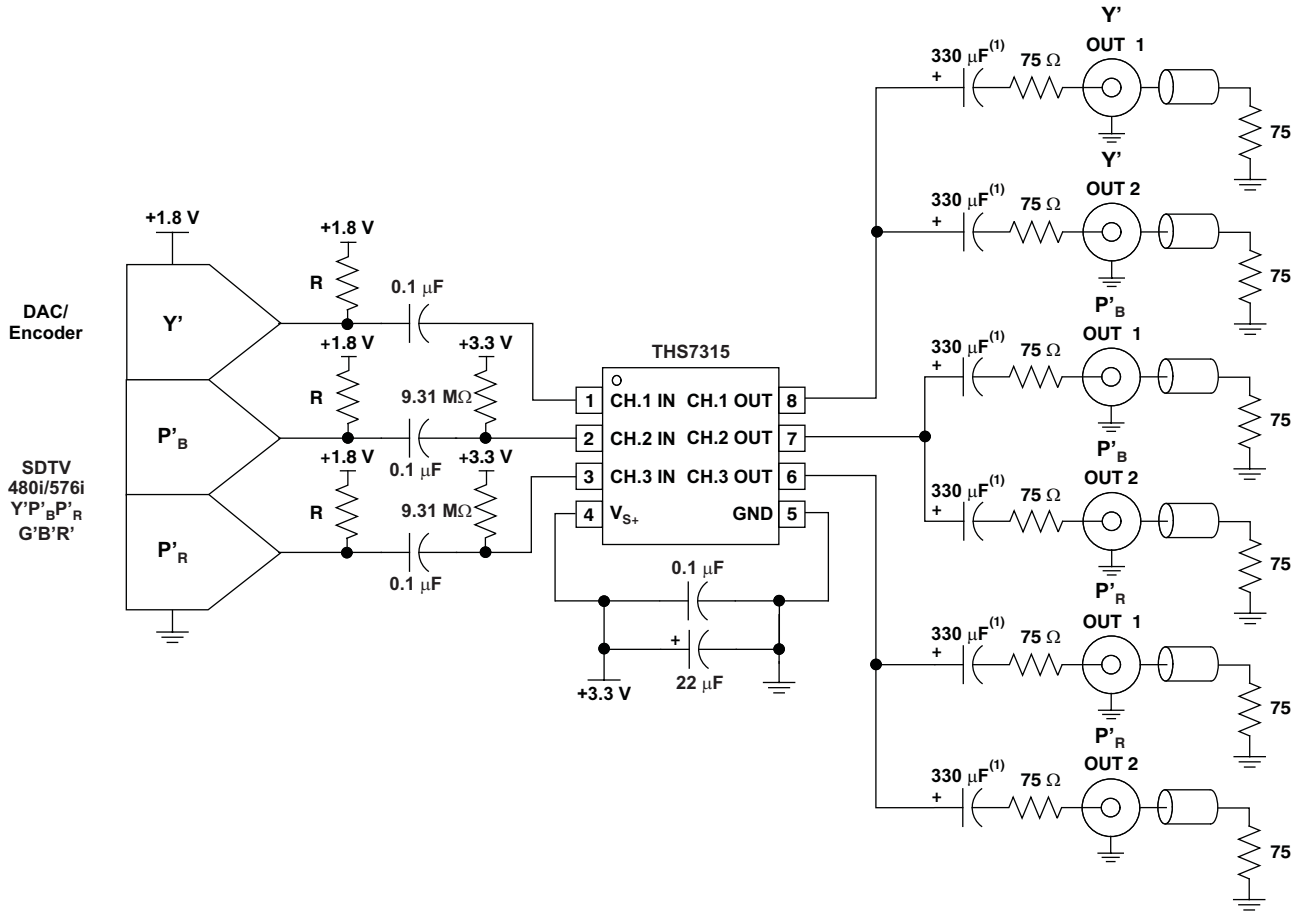
Note that the THS7315 can drive the line with dc coupling regardless of the input mode of operation. The only requirement is to verify that the video line has proper termination in series with the output (typically 75 Ω). This termination also helps isolate capacitive loading effects from the THS7315 output. Failure to isolate capacitive loads may result in instabilities with the output buffer, potentially causing ringing or oscillating to appear. The stray capacitance appearing directly at the THS7315 output pins should be kept below 25 pF.

APPLICATION INFORMATION (continued)

OUTPUT MODE OF OPERATION—AC-COUPLED

The most common method of coupling the video signal to the line is through the use of a large capacitor. This capacitor is typically between 220 µF and 1000 µF, although 330 µF is very common. The value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac coupling as discussed previously in this document. AC coupling is done for several reasons; generally, it is done to ensure full interoperability with the receiving video system. This coupling eliminates possible ground loops. It also ensures that regardless of the reference dc voltage used on the transmit side, the receive side will re-establish the dc reference voltage to its own requirements.

In the same way that the dc output mode of operation is configured (as discussed earlier), each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. If driving two lines, it is best to have each line use its own capacitor and resistor rather than sharing these components, as Figure 9 shows. This configuration helps ensure line-to-line dc isolation and avoids the potential problems discussed earlier. Using a single 1000-µF capacitor for two lines can be done, but there is a chance for ground loops and additional interference to be created between the two receivers.



(1) As a result of the high frequency content of the video signal, it is recommended, but not required, to add a 0.1-µF or 0.01-µF capacitor in parallel with these large capators.

(2) Current sinking DAC / Encoder shown. See the application notes.

Figure 9. Typical 480i/576i Y'P'$_B$P'$_R$ AC-Input System Driving Two AC-Coupled Video Lines

APPLICATION INFORMATION (continued)

Lastly, because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitor. These large-value capacitors are generally aluminum electrolytic. It is well-known that these types of capacitors have significantly large equivalent series resistance, or ESR, and the respective impedances at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-µF to 0.01-µF capacitors help to pass these high-frequency (greater than 1 MHz) signals with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in an S-Video system is not required to go to as low (or as high) a frequency as the luma channels. Therefore, the capacitor values of the chroma line(s) can be smaller, such as 0.1 µF.

LOW-PASS FILTER

Each channel of the THS7315 incorporates a 5th-order low-pass filter. These video reconstruction filters minimize DAC images from passing on to the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems that result from ADC aliasing. Another benefit of the filter is that it smooths out aberrations in the signal that some DACs can demonstrate if the internal filtering is not good. These benefits help with picture quality and ensure that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat, with a relatively steep initial attenuation at the corner frequency. The problem with the Butterworth filter, however, is that the group delay also rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time-domain pulse response that has overshoot (and possible ringing associated with the overshoot).

Other filter types (such as elliptic or chebyshev) are not recommended for video applications because of the very large group delay variations that occur near the corner frequency, also resulting in significant overshoot and ringing. While elliptic or chebyshev filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. Combined with the fact that video can switch from a white pixel to a black pixel over and over again, ringing can easily occur. Ringing typically causes a display to have ghosting or fuzziness on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Consequently, the Butterworth filter is a respectable compromise for both attenuation and group delay.

The THS7315 filters have a nominal corner (–3 dB) frequency at 8.5 MHz and a –1 dB passband, typically at 7 MHz. This 8.5-MHz filter is ideal for SDTV, NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'C'), 480i/576i $Y'P'_BP'_R$, Y'U'V', broadcast G'B'R' signals, and computer R'G'B' video signals. The 8.5-MHz, –3-dB corner frequency was designed to allow a maximally flat video signal while achieving 47 dB of attenuation at 27 MHz—a common sampling frequency between the DAC/ADC 2nd and 3rd Nyquist zones that is found in many video systems. This feature is important because any signal appearing around this frequency can appear in the baseband because of aliasing effects of an ADC found in a receiver.

Keep in mind that images do not stop at 27 MHz; they continue around the sampling frequencies of 54 MHz, 81 MHz, 108 MHz, and so forth. Because of these multiple images that an ADC can fold down into the baseband signal, the low-pass filter must also eliminate these higher-order images. The THS7315 has over 70-dB attenuation at 54 MHz and 81 MHz, along with over 65-dB attenuation at 108 MHz. Attenuation above 108 MHz is at least 55 dB, ensuring that images do not affect the desired video baseband signal.

The 8.5-MHz filter frequency was chosen to account for process variations in the THS7315. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other filter design consideration is the attenuation. It must be large enough to ensure that anti-aliasing/reconstruction filtering is enough to meet the system demands. Thus, the filter frequency selection was not arbitrary; it is a good compromise that should meet the demands of most systems.

APPLICATION INFORMATION (continued)

ADVANTAGES OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system such as the THS7315 over a passive system are PCB area and filter variations. For overall board area, the small SOIC-8 package for 3-video channels is much smaller over a passive RLC network, especially a 5-pole passive network. As for filter variations, consider that inductors generally have 10% tolerances (normally 15% to 20%) and capacitors typically have 10% tolerances. A Monte Carlo analysis shows that the desired filter corner frequency (–3 dB), flatness (–1 dB), Q-factor (or peaking), and channel-to-channel delay will have wide variations. These variations can lead to potential performance and quality issues in mass-production environments. The THS7315 solves most of these problems with the corner frequency being the only variable.

One concern about using an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature change. To minimize temperature effects, the THS7315 uses low temperature coefficient resistors and high quality/low temperature coefficient capacitors found in the BiCom3 process. The filters have been specified by design to account for process and temperature variations to maintain proper filter characteristics. This design guideline maintains a low channel-to-channel time delay that is required for proper video signal performance.

The input and output impedances are another benefit of the THS7315 over a passive RLC filter. The input impedance presented to the DAC varies significantly with a passive network and may cause voltage variations over frequency. The THS7315 input impedance is 800 kΩ; only the 2-pF input capacitance plus the PCB trace capacitance affect this value. As such, the voltage variation appearing at the DAC output is better controlled with the THS7315.

On the output side of the filter, a passive filter again has an impedance variation over frequency. The THS7315 is an operational amplifier that approximates an ideal voltage source. A voltage source is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss, this output impedance must maintain a 75-Ω impedance. A passive filter impedance variation cannot specify this condition, while the THS7315 has about 0.8 Ω of output impedance at 1 MHz. Thus, the system is matched much better with a THS7315 when compared to a passive filter.

One final benefit of the THS7315 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load—the receiver 75-Ω resistor and the 75-Ω impedance-matching resistor next to the DAC to maintain the source impedance requirement. This design requirement forces the DAC to drive at least 1.25 V_{PP} (100% saturation CVBS) / 37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when six channels are being driven. Using the THS7315, with a high input impedance and the capability to drive up to two video lines, can reduce the DAC power dissipation significantly. This reduction occurs because the resistance that the DAC is driving can be substantially increased. It is common to set this increase in a DAC by a current-setting resistor on the device. Thus, the resistance can be 300 Ω or more—significantly reducing the current drive demands from the DAC and saving a substantial amount of power. For example, a 3.3-V, six-channel DAC dissipates 660 mW just for the steering current capability (6 channels × 33.3 mA × 3.3 V) if it needs to drive 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 82.5 mW (6 channels × 4.16 mA × 3.3 V).

EVALUATION MODULE

To evaluate the THS7315, an evaluation module (EVM) is available. The EVM allows for testing the THS7315 in many different systems. Inputs and outputs include RCA connectors for consumer grade interconnections, or BNC connectors for higher-level lab grade connections. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user.

Figure 10 shows the THS7315EVM schematic. Figure 11 and Figure 12 illustrate the top layer and bottom layer (respectively) of the EVM PCB, incorporating standard high-speed layout practices. Table 1 lists the bill of materials as supplied from Texas Instruments.

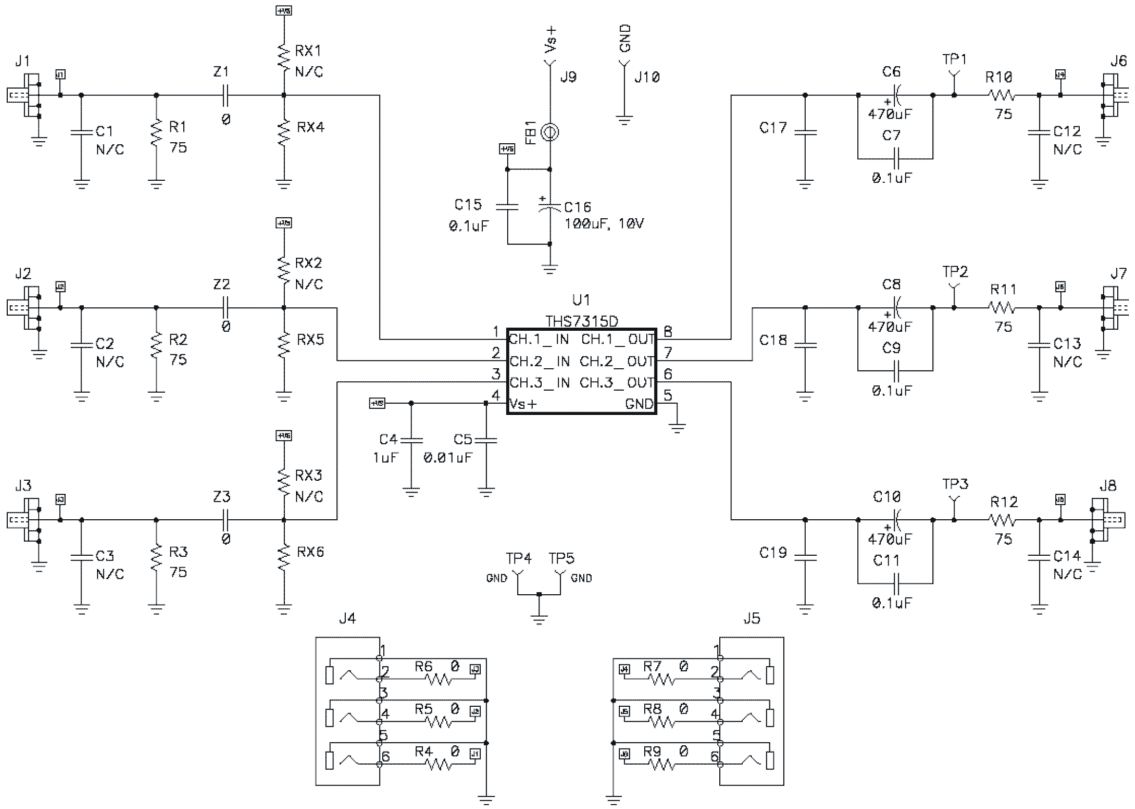


Figure 10. THS7315D EVM Schematic

EVALUATION MODULE (continued)

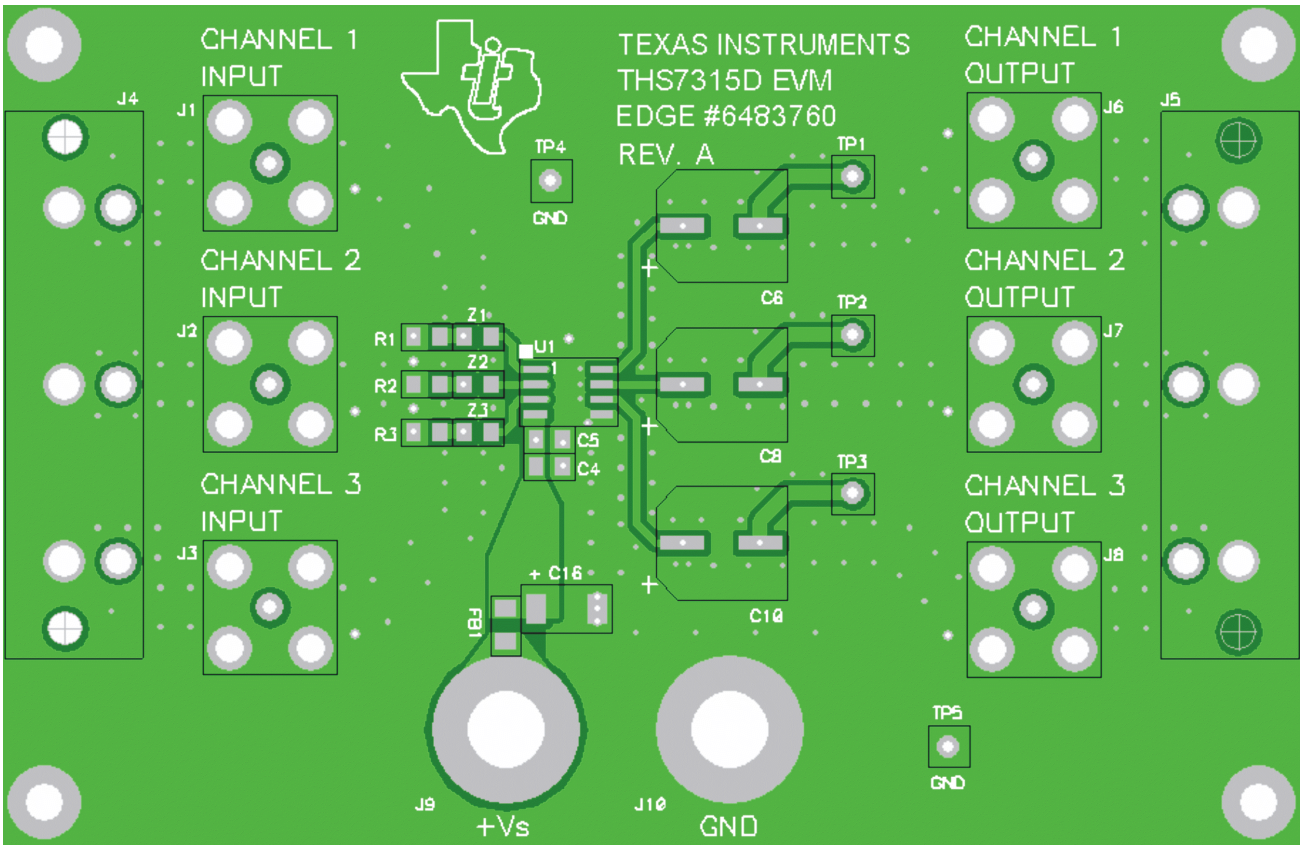


Figure 11. THS7315D EVM PCB Top Layer

EVALUATION MODULE (continued)

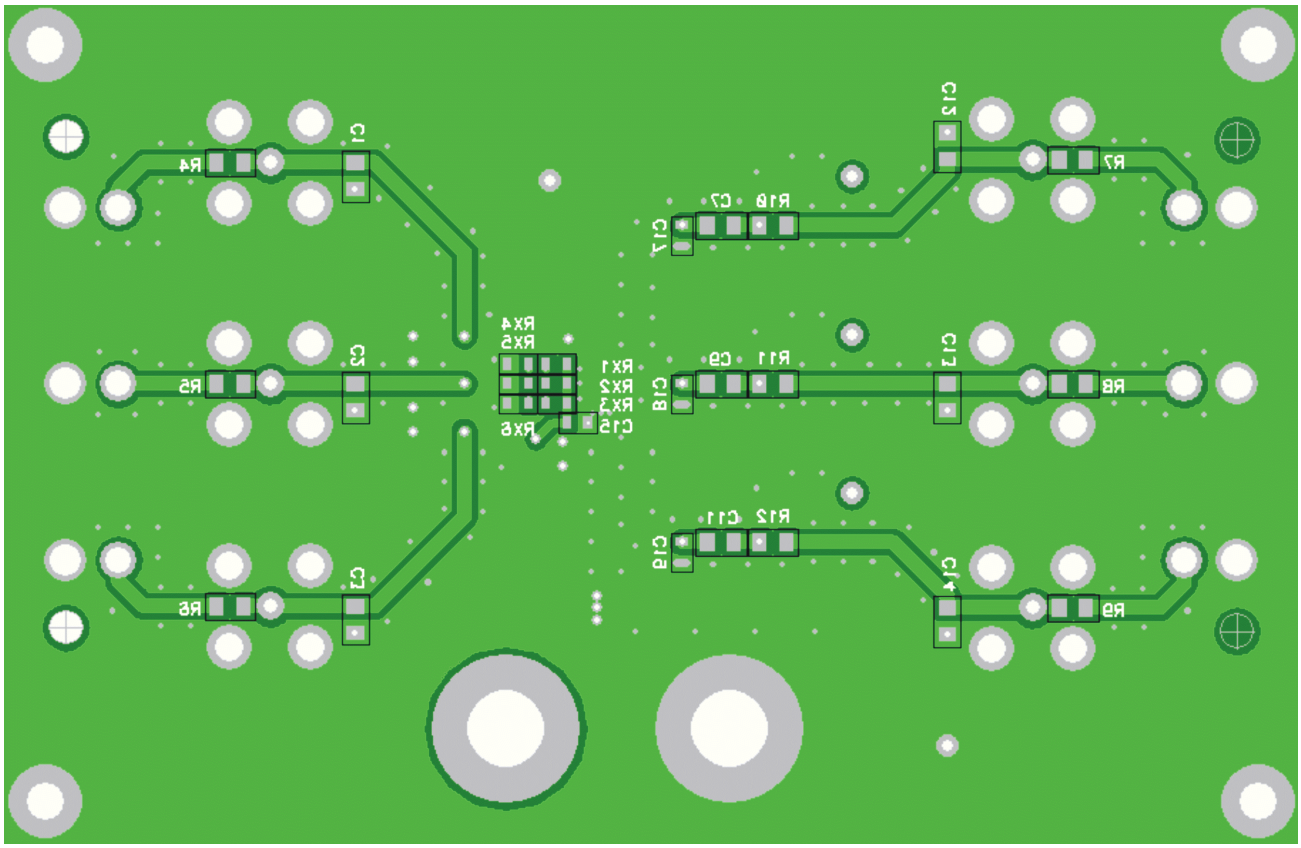


Figure 12. THS7315D EVM PCB Bottom Layer

EVALUATION MODULE (continued)

THS7315EVM Bill of Materials

Table 1. THS7315D EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1	1	Bead, Ferrite, 2.5A, 330 Ω	0805	(TDK) MPZ2012S331A	(Digi-Key) 445-1569-1-ND
2	C16	1	Capacitor, 100µF, Tantalum, 10V, 10%, Low-ESR	C	(AVX) TPSC107K010R0100	(Digi-Key) 478-1765-1-ND
3	C17, C18, C19	3	Open	0603		
4	C15	1	Capacitor, 0.1µF, Ceramic, 16V, X7R	0603	(AVX) 0603YC104KAT2A	(Garrett) 0603YC104KAT2A
5	C1, C2, C3, C12, C13, C14	6	OPEN	0805		
6	C5	1	Capacitor, 0.01µF, Ceramic, 100V, X7R	0805	(AVX) 08051C103KAT2A	(Digi-Key) 478-1358-1-ND
7	C7, C9, C11	3	Capacitor, 0.1µF, Ceramic, 50V, X7R	0805	(AVX) 08055C104KAT2A	(Digi-Key) 478-1395-1-ND
8	C4	1	Capacitor, 1µF, Ceramic, 16V, X7R	0805	(TDK) C2012X7R1C105K	(Digi-Key) 445-1358-1-ND
9	C6, C8, C10	3	Capacitor, Aluminum, 470µF, 10V, 20%	F	(Cornell) AFK477M10F24B	(Newark) 97C7597
10	RX1–RX6	6	Open	0603		
11	R4–R9, Z1, Z2, Z3	9	Resistor, 0 Ω	0805	(ROHM) MCR10EZHJ000	(Digi-Key) RHM0.0ACT-ND
12	R1, R2, R3, R10, R11, R12	6	Resistor, 75 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF75.0	(Digi-Key) RHM75.0CCT-ND
13	J9, J10	2	Jack, Banana Receptance, 0.25" dia. hole		(SPC) 813	(Newark) 39N867
14	J1, J2, J3, J6, J7, J8	6	Connector, BNC, Jack, 75 Ω		(Amphenol) 31-5329-72RFX	(Newark) 93F7554
15	J4, J5	2	Connector, RCA, Jack, R/A		(CUI) RCJ-32265	(Digi-Key) CP-1446-ND
16	TP1, TP2, TP3	3	Test Point, Red		(Keystone) 5000	(Digi-Key) 5000K-ND
17	TP4, TP5	2	Test Point, Black		(Keystone) 5001	(Digi-Key) 5001K-ND
18	U1	1	IC, THS7315	D	(TI) THS7315D	
19		4	Standoff, 4-40 Hex, 0.625" Length		(Keystone) 1808	(Newark) 89F1934
20		4	Screw, Phillips, 4-40, .250"		(BF) PMS 440 0031 PH	(Digi-Key) H343-ND
21		1	Printed circuit board		Edge # 6483760 REV. A	

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.85 V to 5.5 V single supply and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85 = C. The EVM is designed to operate properly with certain components above +85 = C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7315D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7315	Samples
THS7315DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7315	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

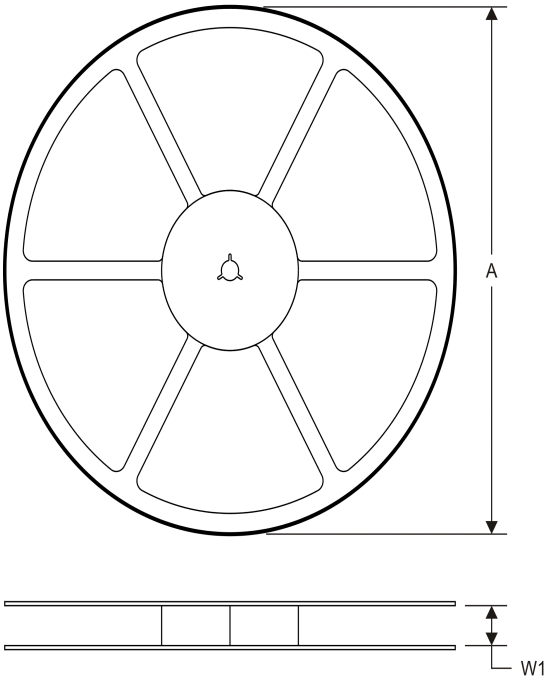
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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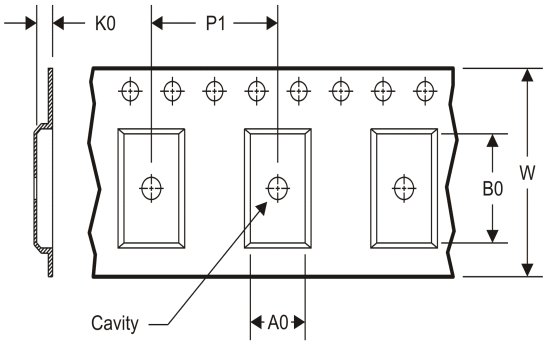
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



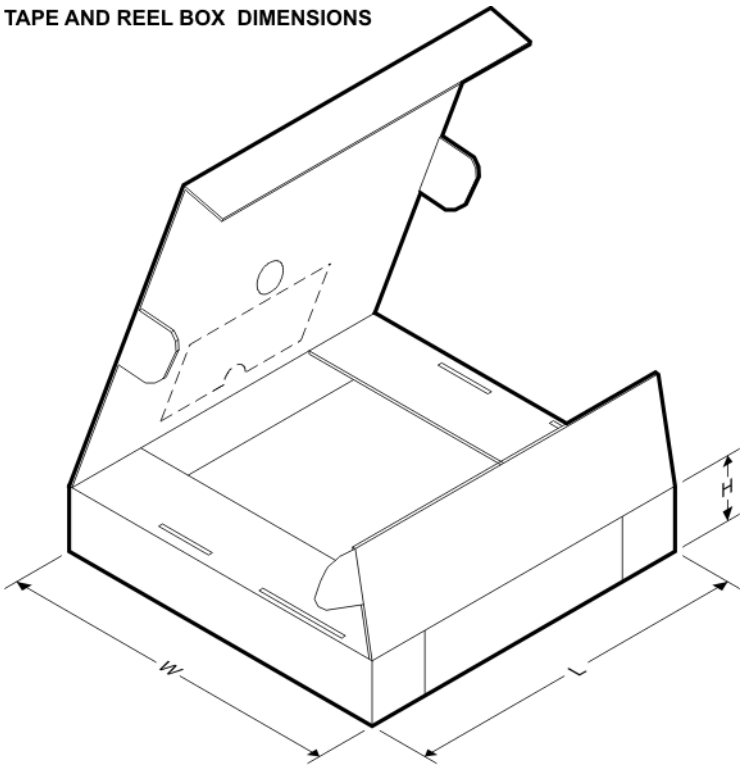
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

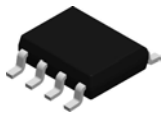
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7315DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7315DR	SOIC	D	8	2500	367.0	367.0	35.0

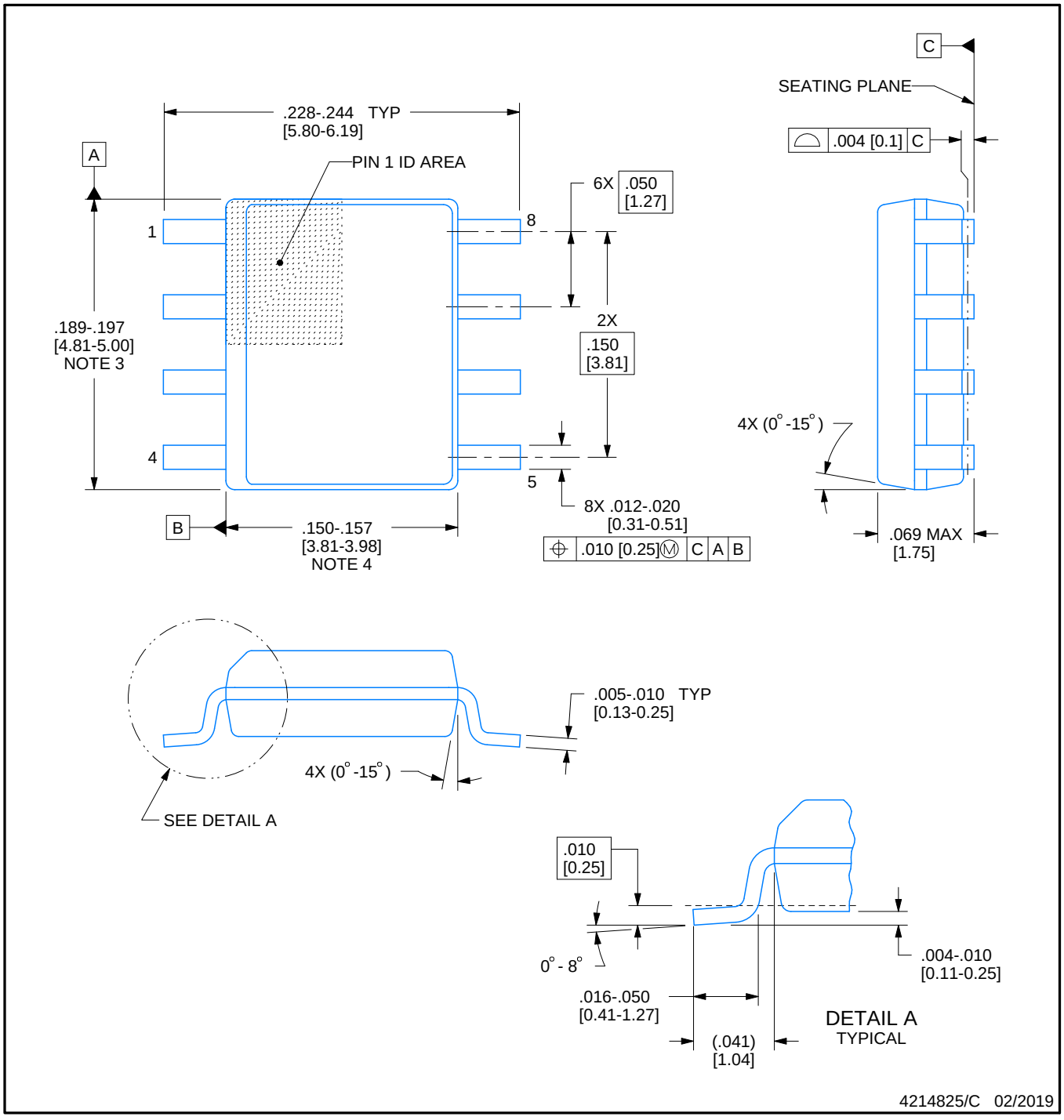


PACKAGE OUTLINE

D0008A

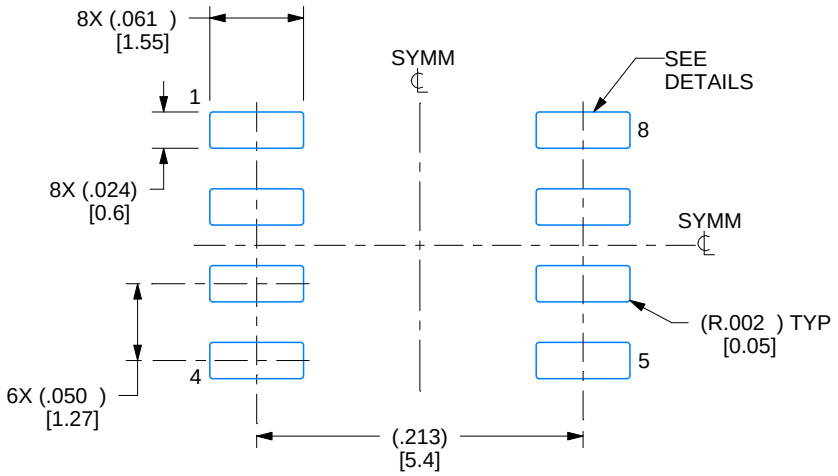
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

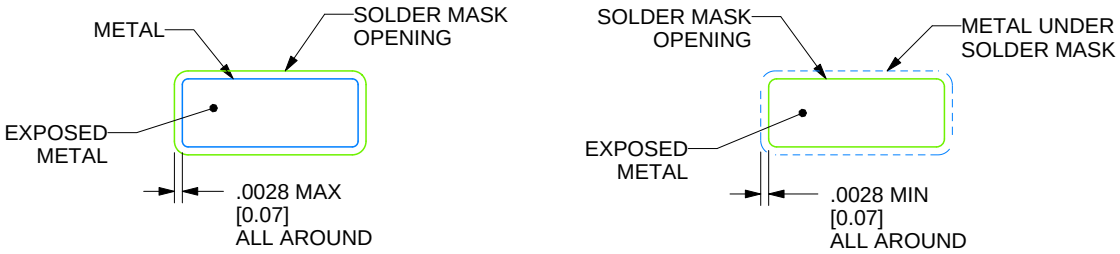


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

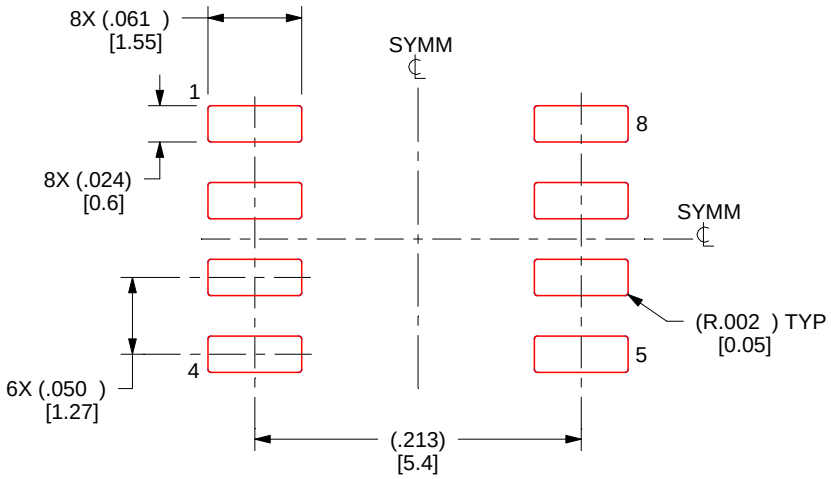
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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