

## OPAx376-Q1 低噪声、低静态电流、 高精度运算放大器 *e-trim* 系列

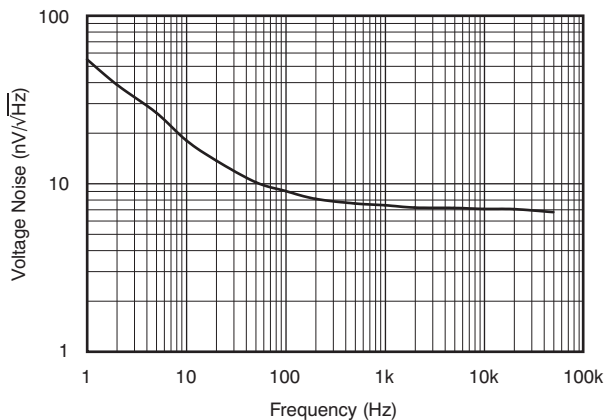
### 1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 3A
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 低噪声：1kHz 时为  $7.5\text{nV}/\sqrt{\text{Hz}}$
- 0.1Hz 至 10Hz 噪声： $0.8\ \mu\text{V}_{\text{PP}}$
- 静态电流：760 $\mu\text{A}$  (典型值)
- 低偏移电压：5 $\mu\text{V}$  (典型值)
- 增益带宽积：5.5MHz
- 轨到轨输入和输出
- 单电源供电
- 电源电压：2.2V 至 5.5V
- 小型封装：
  - SC70、小外形尺寸晶体管 (SOT)-23、超薄小外形尺寸 (VSSOP) 和薄型小外形尺寸 (TSSOP)

### 2 应用标准

- 主动巡航控制
- 停车辅助
- 轮胎气压监视
- 信息娱乐系统
- 有源滤波
- 传感器信号调节

输入电压噪声频谱密度



### 3 说明

OPA376-Q1 系列是采用 *e-trim*<sup>™</sup> 的新一代低噪声运算放大器的典型代表，同时拥有出色的直流精度和交流性能。该器件具有轨到轨输出、低偏移（最大值为 25 $\mu\text{V}$ ）、低噪声 ( $7.5\text{nV}/\sqrt{\text{Hz}}$ )、950 $\mu\text{A}$  的静态电流（最大值）和 5.5MHz 带宽，对于各类精密和便携式应用极具吸引力。此外，该器件的电源范围相当宽，电源抑制比 (PSRR) 优异，因此对于不经稳压而直接由电池供电运行的应用而言极具吸引力。

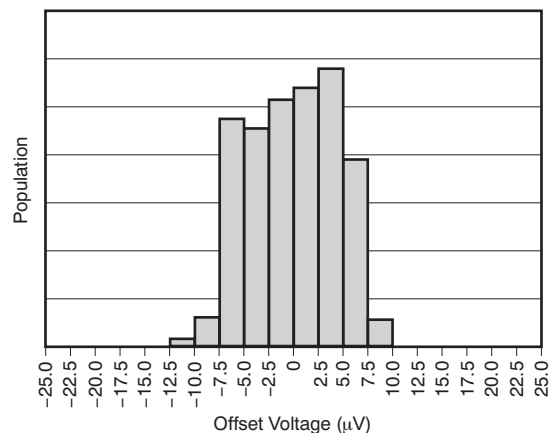
OPA376-Q1 (单通道) 采用 MicroSIZE Sc70-5、小外形尺寸晶体管 (SOT)-23-5 与小外形尺寸集成电路 (SOIC)-8 封装。OPA2376-Q1 (双通道) 采用 SOIC-8 和超薄小外形尺寸 (VSSOP)-8 封装。OPA4376-Q1 (四通道) 采用薄型小外形尺寸 (TSSOP)-14 封装。所有器件版本的额定工作温度范围均为 -40°C 至 +125°C。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
OPA376-Q1	SC70 (5)	2.00mm x 1.25mm
	SOT-23 (5)	2.90mm x 1.60mm
	SOIC (8)	4.90mm x 3.91mm
OPA2376-Q1	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm x 3.00mm
OPA4376-Q1	薄型小外形尺寸封装 (TSSOP) (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

偏移电压产品分布



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision A (January 2016) to Revision B

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•	已更新应用 示例 .....	1
•	Updated the <i>Pin Functions Table</i> for OPA4376-Q1 .....	5
•	Updated <i>HBM ESD Rating</i> .....	6
•	Changed units on <i>Channel Separation</i> .....	8
•	Deleted the temperature range parameters from the <i>Electrical Characteristics</i> table .....	9
•	Removed section regarding <i>WCSP photosensitivity</i> .....	23

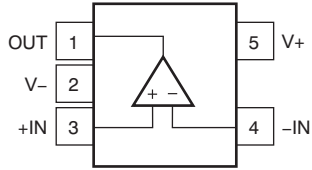
### Changes from Original (April 2011) to Revision A

Page

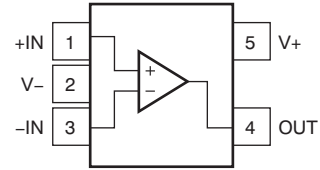
•	已添加 引脚功能表, ESD 额定值表, 建议运行条件表, 热性能信息表, 特性 描述部分, 器件功能模式, 应用和实施方案部分, 电源相关建议部分, 布局部分, 器件和文档支持部分, 以及机械、封装和可订购信息部分 .....	1
•	已将 OPA2376-Q1 器件发布为量产数据 .....	1
•	Added the <i>Input Offset Voltage and Input Offset Voltage Drift</i> section to the <i>Feature Description</i> .....	14

## 5 Pin Configuration and Functions

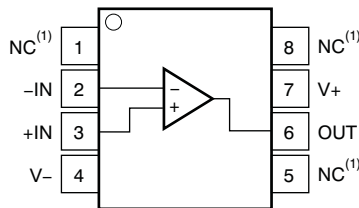
**OPA376-Q1: DBV Package  
5-Pin SOT-23  
Top View**



**OPA376-Q1: DCK Package  
5-Pin SC70  
Top View**



**OPA376-Q1: D Package  
8-Pin SOIC  
Top View**

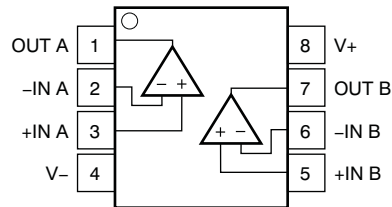


**Pin Functions: OPA376-Q1**

NAME	PIN NO.			I/O	DESCRIPTION
	SOT-23	SC70	SOIC		
+IN	3	1	3	I	Noninverting input <sup>+</sup>
-IN	4	3	2	I	Inverting input <sup>-</sup>
NC <sup>(1)</sup>	—	—	1	—	No connection
			5		
			8		
OUT	1	4	6	O	Output
V+	5	5	7	—	Positive (highest) power supply <sup>+</sup>
V-	2	2	4	—	Negative (lowest) power supply <sup>-</sup>

(1) NC denotes no internal connection.

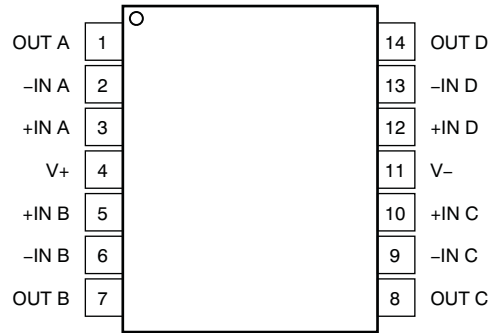
**OPA2376-Q1: D and DGK Packages  
8-Pin SOIC and VSSOP  
Top View**



**Pin Functions: OPA2376-Q1**

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A <sup>+</sup>
-IN A	2	I	Inverting input, channel A <sup>-</sup>
+IN B	5	I	Noninverting input, channel B <sup>+</sup>
-IN B	6	I	Inverting input, channel B <sup>-</sup>
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

**OPA4376-Q1: PW Package  
14-Pin TSSOP  
Top View**



**Pin Functions: OPA4376-Q1**

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A <sup>+</sup>
-IN A	2	I	Inverting input, channel A <sup>-</sup>
+IN B	5	I	Noninverting input, channel B <sup>+</sup>
-IN B	6	I	Inverting input, channel B <sup>-</sup>
+IN C	10	I	Noninverting input, channel C <sup>+</sup>
-IN C	9	I	Inverting input, channel C <sup>-</sup>
+IN D	12	I	Noninverting input, channel D <sup>+</sup>
-IN D	13	I	Inverting input, channel D <sup>-</sup>
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V-	11	—	Negative (lowest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_S = (V+) - (V-)$	Supply voltage		7	V
	Signal input pin voltage <sup>(2)</sup>	(V-) – 0.5	(V+) + 0.5	V
	Signal input pin current <sup>(2)</sup>	–10	10	mA
	Output short-circuit current <sup>(3)</sup>	Continuous		
$T_A$	Operating temperature	–40	125	°C
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_S = (V+) - (V-)$	Supply voltage	2.2 (±1.1)	5.5 (±2.75)	V
$T_A$	Operating temperature	–40	150	°C

#### 6.4 Thermal Information: OPA376-Q1

THERMAL METRIC <sup>(1)</sup>		OPA376-Q1			UNIT
		DCK (SC70)	DBV (SOT-23)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	267	273.8	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.9	126.8	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	85.9	41	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.2	10.9	4.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	54.1	84.9	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

#### 6.5 Thermal Information: OPA2376-Q1

THERMAL METRIC <sup>(1)</sup>		OPA2376-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	63.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	92.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	10.5	9.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	51.2	91.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

#### 6.6 Thermal Information: OPA4376-Q1

THERMAL METRIC <sup>(1)</sup>		OPA4376-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.7 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage			5	25	$\mu\text{V}$
$dV_{OS}/dT$	Input offset voltage versus temperature	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		0.26	1	$\mu\text{V}/^\circ\text{C}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.32	2	$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage versus power supply	$V_S = 2.2\text{ V}$ to $5.5\text{ V}$ , $V_{CM} < (V+) - 1.3\text{ V}$	$T_A = 25^\circ\text{C}$	5	20	$\mu\text{V}/\text{V}$
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	5		$\mu\text{V}/\text{V}$
	Channel separation, dc (dual, quad)			0.5		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$T_A = 25^\circ\text{C}$		0.2	10	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See <a href="#">Typical Characteristics</a>		pA
$I_{OS}$	Input offset current			0.2	10	pA
<b>NOISE</b>						
	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.8		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$		7.5		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise	$f = 1\text{ kHz}$		2		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE</b>						
$V_{CM}$	Common-mode voltage		$(V-) - 0.1$		$(V+) + 0.1$	V
CMRR	Common-mode rejection ratio	$(V-) < V_{CM} < (V+) - 1.3\text{ V}$	76	90		dB
<b>INPUT CAPACITANCE</b>						
	Differential			6.5		pF
	Common-mode			13		pF
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$50\text{ mV} < V_O < (V+) - 50\text{ mV}$ , $R_L = 10\text{ k}\Omega$	120	134		dB
		$100\text{ mV} < V_O < (V+) - 100\text{ mV}$ , $R_L = 2\text{ k}\Omega$	120	126		dB
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product	$C_L = 100\text{ pF}$ , $V_S = 5.5\text{ V}$		5.5		MHz
SR	Slew rate	$G = 1$ , $C_L = 100\text{ pF}$ , $V_S = 5.5\text{ V}$		2		$\text{V}/\mu\text{s}$
$t_S$	Settling time	0.1%, 2-V Step, $G = 1$ , $C_L = 100\text{ pF}$ , $V_S = 5.5\text{ V}$		1.6		$\mu\text{s}$
		0.01%, 2-V Step, $G = 1$ , $C_L = 100\text{ pF}$ , $V_S = 5.5\text{ V}$		2		$\mu\text{s}$
	Overload recovery time	$V_{IN} \times \text{Gain} > V_S$		0.33		$\mu\text{s}$
THD+N	THD + noise	$V_O = 1\text{ V}_{RMS}$ , $G = 1$ , $f = 1\text{ kHz}$ , $R_L = 10\text{ k}\Omega$		0.00027%		
<b>OUTPUT</b>						
	Voltage output swing from rail	$R_L = 10\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	10	20	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			40
		$R_L = 2\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	40	50	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			80
$I_{SC}$	Short-circuit current			30 / -50		mA
$C_{LOAD}$	Capacitive load drive			See <a href="#">Typical Characteristics</a>		
$R_O$	Open-loop output impedance			150		$\Omega$

**Electrical Characteristics (continued)**

 At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>							
$V_S$	Specified voltage			2.2		5.5	V
	Operating voltage				2 to 5.5		V
$I_Q$	Quiescent current per amplifier	$I_O = 0$ , $V_S = 5.5\text{ V}$ , $V_{CM} < (V+) - 1.3\text{ V}$	$T_A = 25^\circ\text{C}$		760	950	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			1	mA

### 6.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

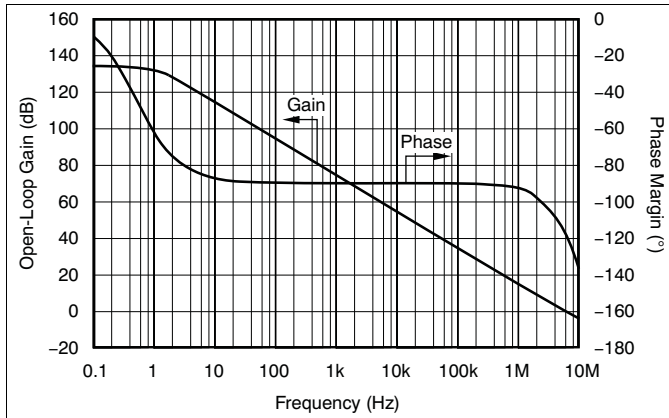


Figure 1. Open-Loop Gain and Phase vs Frequency

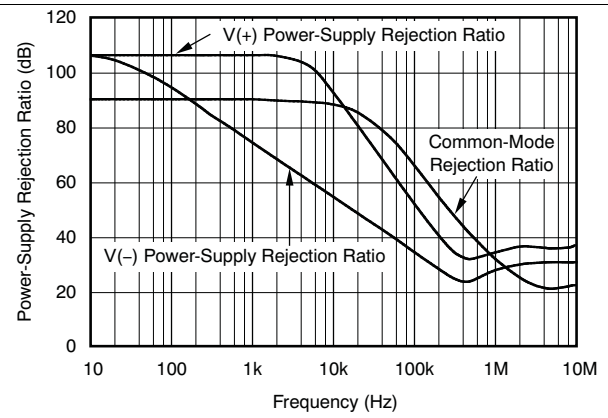


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

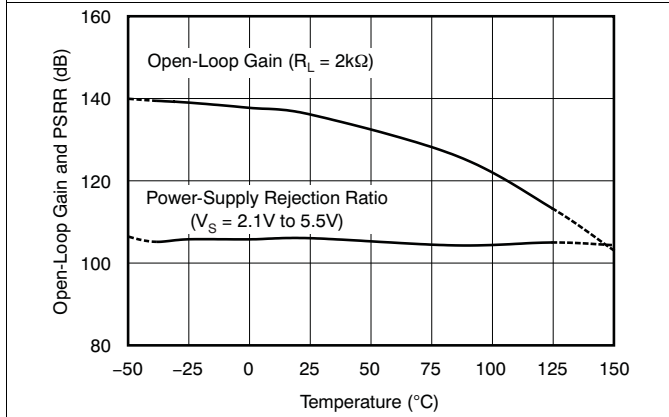


Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

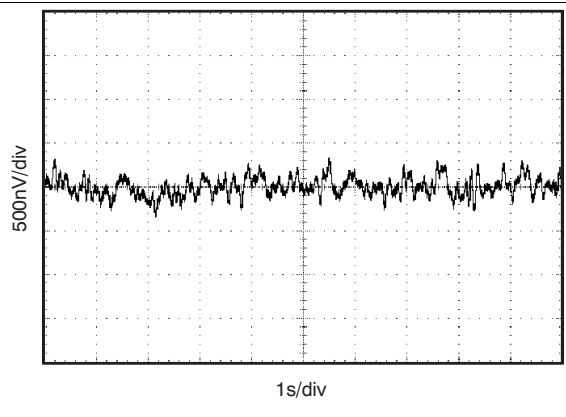


Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

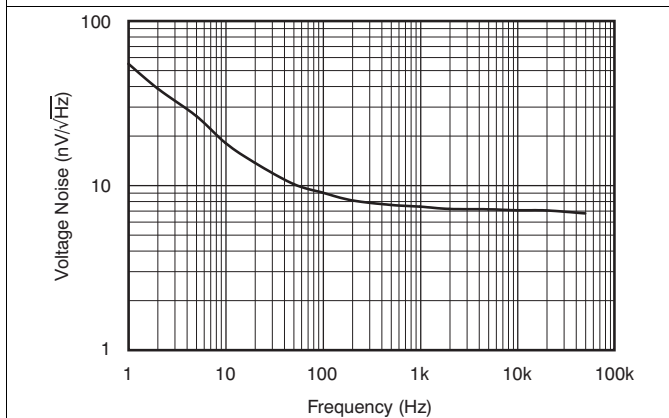


Figure 5. Input Voltage Noise Spectral Density

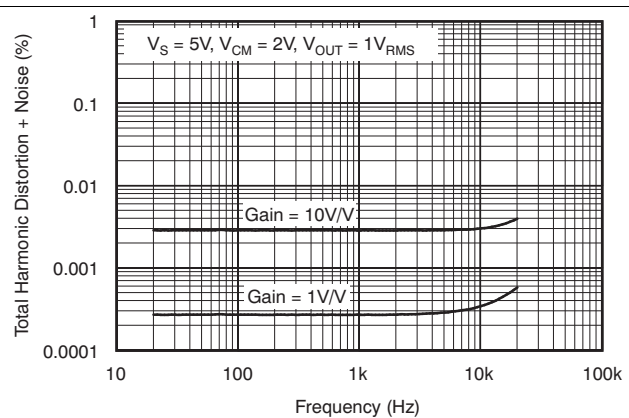


Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

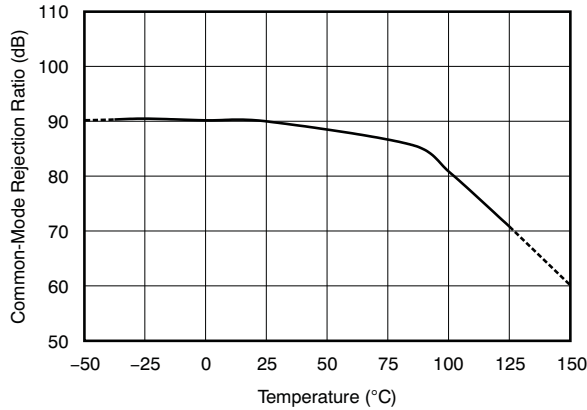


Figure 7. Common-Mode Rejection Ratio vs Temperature

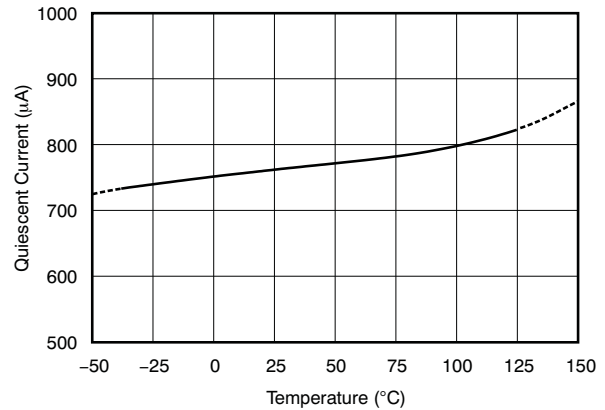


Figure 8. Quiescent Current vs Temperature

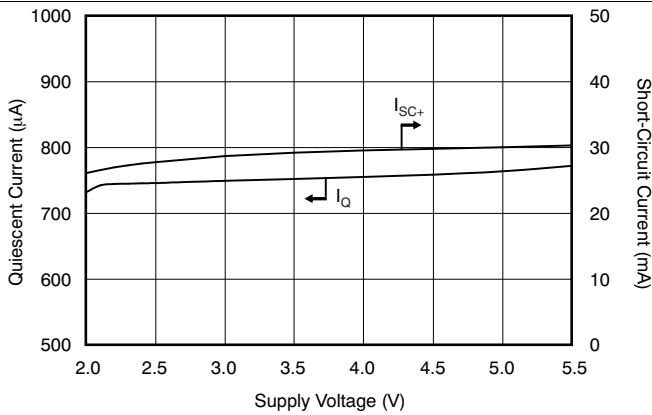


Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

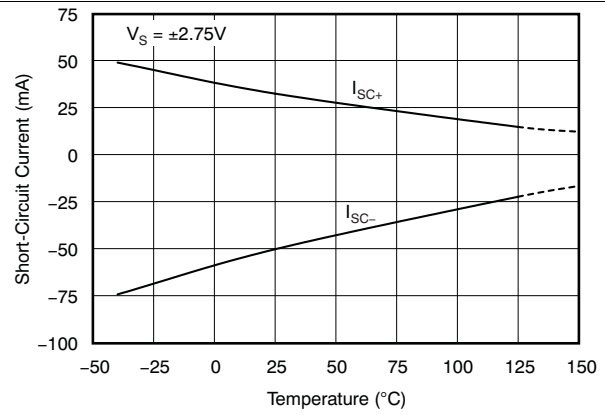


Figure 10. Short-Circuit Current vs Temperature

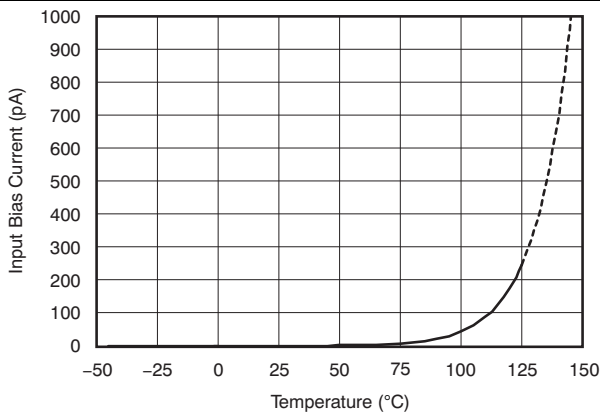


Figure 11. Input Bias Current vs Temperature

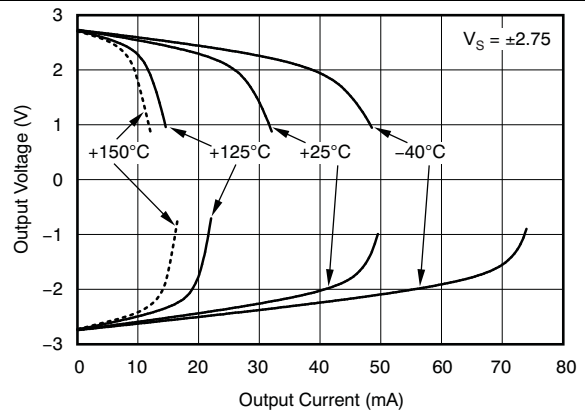


Figure 12. Output Voltage vs Output Current

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

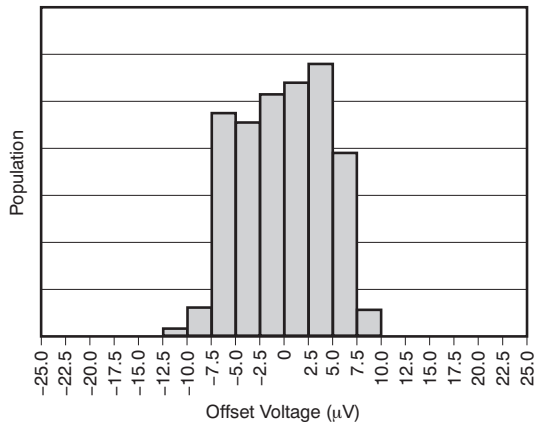


Figure 13. Offset Voltage Production Distribution

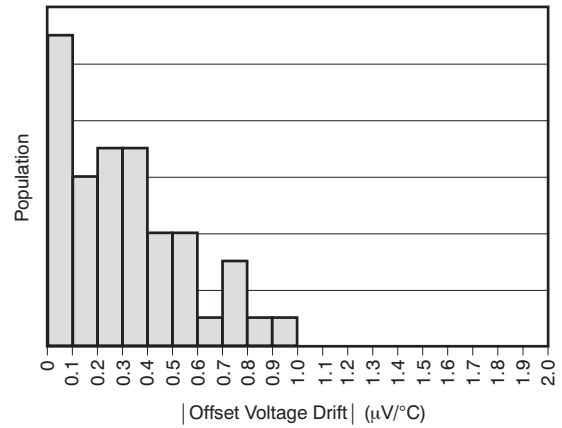


Figure 14. Offset Voltage Drift Production Distribution (-40°C to +125°C)

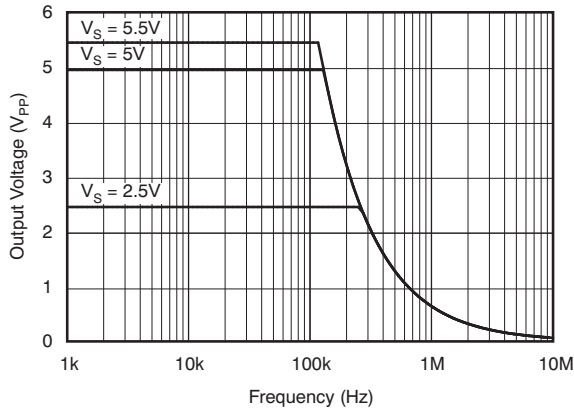


Figure 15. Maximum Output Voltage vs Frequency

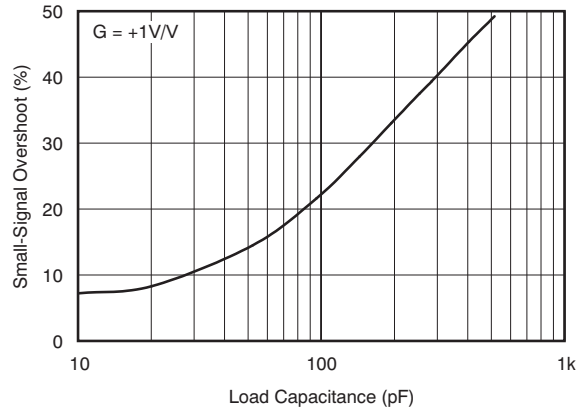


Figure 16. Small-Signal Overshoot vs Load Capacitance

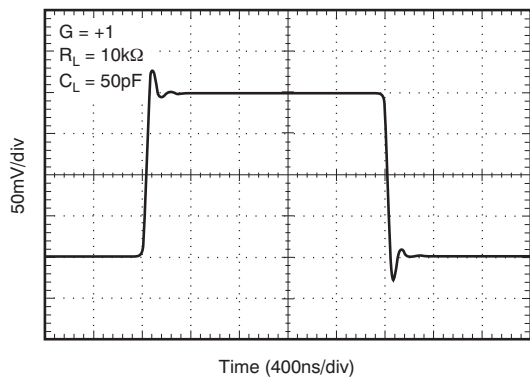


Figure 17. Small-Signal Pulse Response

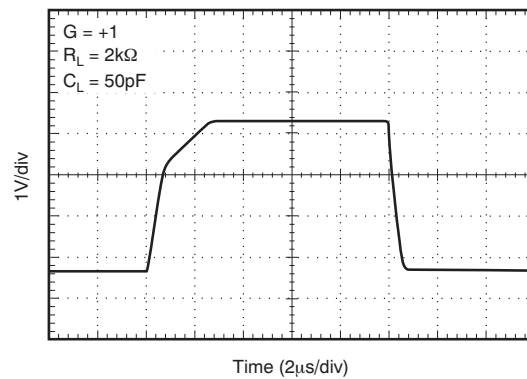
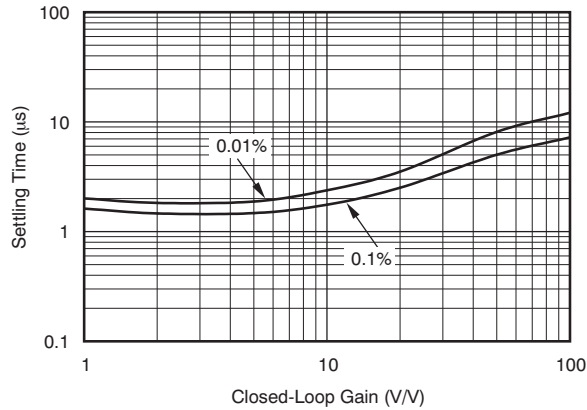


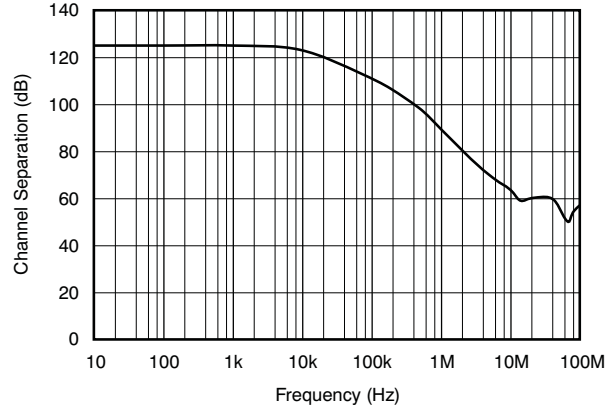
Figure 18. Large-Signal Pulse Response

**Typical Characteristics (continued)**

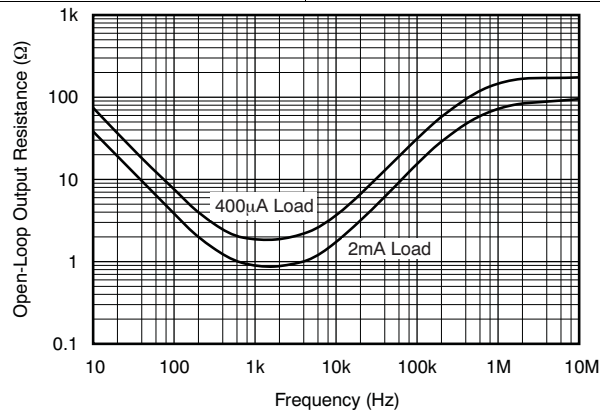
At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.



**Figure 19. Settling Time vs Closed-Loop Gain**



**Figure 20. Channel Separation vs Frequency**



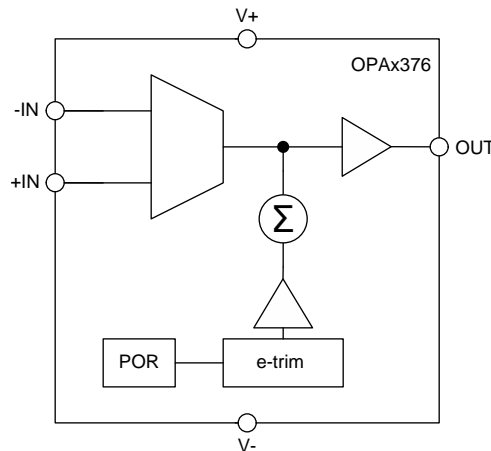
**Figure 21. Open-Loop Output Resistance vs Frequency**

## 7 Detailed Description

### 7.1 Overview

The OPA376-Q1 family belongs to a new generation of low-noise operational amplifiers with *e-trim*, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The OPAx376-Q1 family of precision amplifiers offers excellent dc performance as well as excellent ac performance. Operating from a single power-supply the OPAx376-Q1 is capable of driving large capacitive loads, has a wide input common-mode voltage range, and is well-suited to drive the inputs of successive-approximation response (SAR) analog-to-digital converters (ADCs) as well as 24-bit and higher resolution converters. Including internal ESD protection, the OPAx376-Q1 family is offered in a variety of industry-standard packages, including a wafer chip-scale package for applications that require space savings.

#### 7.3.1 Operating Voltage

The OPAx376-Q1 family of amplifiers operate over a power-supply range of 2.2 V to 5.5 V ( $\pm 1.1$  V to  $\pm 2.75$  V). Many of the specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

#### 7.3.2 Input Offset Voltage and Input Offset Voltage Drift

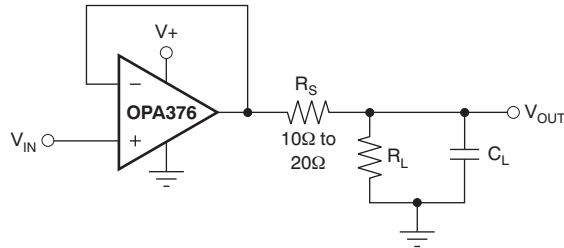
The OPAx376-Q1 family of operational amplifiers is manufactured using TI's *e-trim* technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The *e-trim* technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing.

#### 7.3.3 Capacitive Load and Stability

The OPAx376-Q1 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx376-Q1 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

## Feature Description (continued)

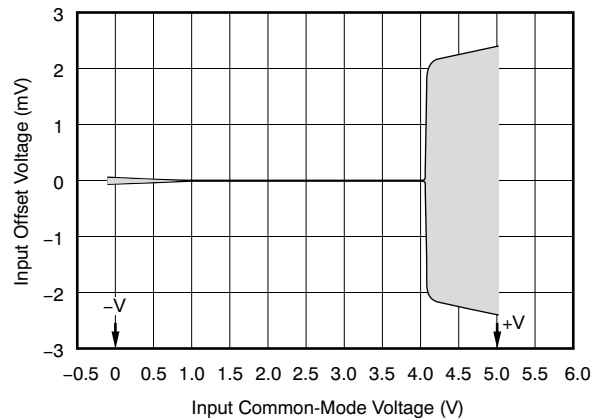
The OPAx376 in a unity-gain configuration can directly drive up to 250 pF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot [Figure 16](#), *Small-Signal Overshoot vs Load Capacitance*. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor,  $R_S$ , in series with the output, as shown in [Figure 22](#). This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_S / R_L$ , and is generally negligible at low output current levels.



**Figure 22. Improving Capacitive Load Drive**

### 7.3.4 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx376-Q1 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately  $(V_-)$  to  $(V_+) - 1$  V, as shown in [Figure 23](#). The offset voltage increases as common-mode voltage exceeds  $(V_+) - 1$  V. Common-mode rejection is specified from  $(V_-)$  to  $(V_+) - 1.3$  V.



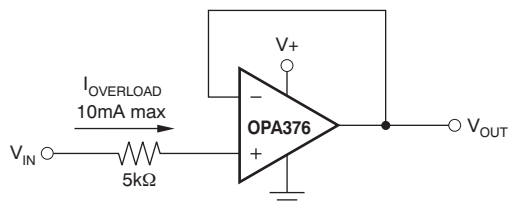
**Figure 23. Offset and Common-Mode Voltage**

## Feature Description (continued)

### 7.3.5 Input and ESD Protection

The OPAx376-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#) table.

[Figure 24](#) shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.



**Figure 24. Input Current Protection**

## 7.4 Device Functional Modes

The OPAx376-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V ( $\pm 1.1$  V). The maximum power supply voltage for the OPAx376-Q1 is 5.5 V ( $\pm 2.75$  V).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The OPAx376-Q1 family of operational amplifiers is built using *e-trim*, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through *e-trim*, the OPAx376-Q1 family delivers excellent offset voltage (5  $\mu$ V, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and  $A_{OL}$ . These 5.5-MHz CMOS op amps operate on 760  $\mu$ A (typical) quiescent current.

#### 8.1.1 Basic Amplifier Configurations

The OPA376-Q1 family is unity-gain stable. It does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 25. The OPA376-Q1 is configured as a basic inverting amplifier with a gain of  $-10$  V/V. This single-supply connection has an output centered on the common-mode voltage,  $V_{CM}$ . For the circuit shown in Figure 25, this voltage is 2.5 V, but may be any value within the common-mode input voltage range.

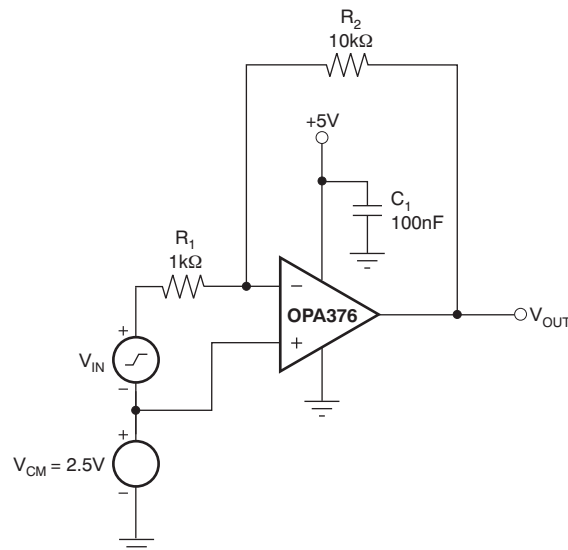
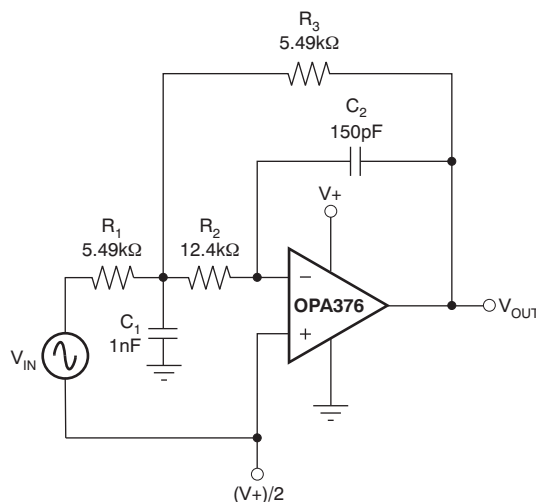


Figure 25. Basic Single-Supply Connection

## Application Information (continued)

### 8.1.2 Active Filtering

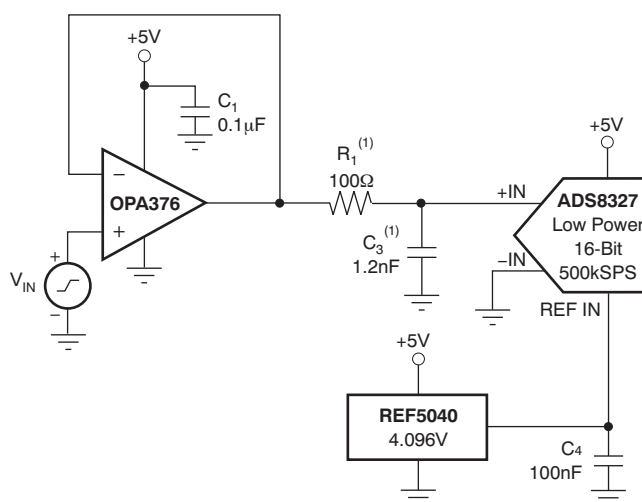
The OPA376-Q1 series is well-suited for filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 26 shows a 50-kHz, second-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is  $-40$  dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an ADC.



**Figure 26. Second-Order Butterworth, 50-kHz Low-Pass Filter**

### 8.1.3 Driving an Analog-to-Digital Converter

The low noise and wide gain bandwidth of the OPA376-Q1 family make it an ideal driver for ADCs. Figure 27 illustrates the OPA376-Q1 driving an ADS8327, 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer.



(1) Suggested value; may require adjustment based on specific application.

**Figure 27. Driving an ADS8327**

## Application Information (continued)

### 8.1.4 Phantom-Powered Microphone

The circuit shown in Figure 28 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

An OPA2376-Q1 serves as a single-ended input to a differential output amplifier with a 6-dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A 48-V phantom supply is reduced to 5.1 V by the series 6.8-k $\Omega$  resistors on the output side of the cable, and the 4.7-k $\Omega$  resistors and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable.

The INA163 gain may be set from 0 dB to 80 dB by selecting the  $R_G$  value. The INA163 circuit is typical of the input circuitry used in mixing consoles.

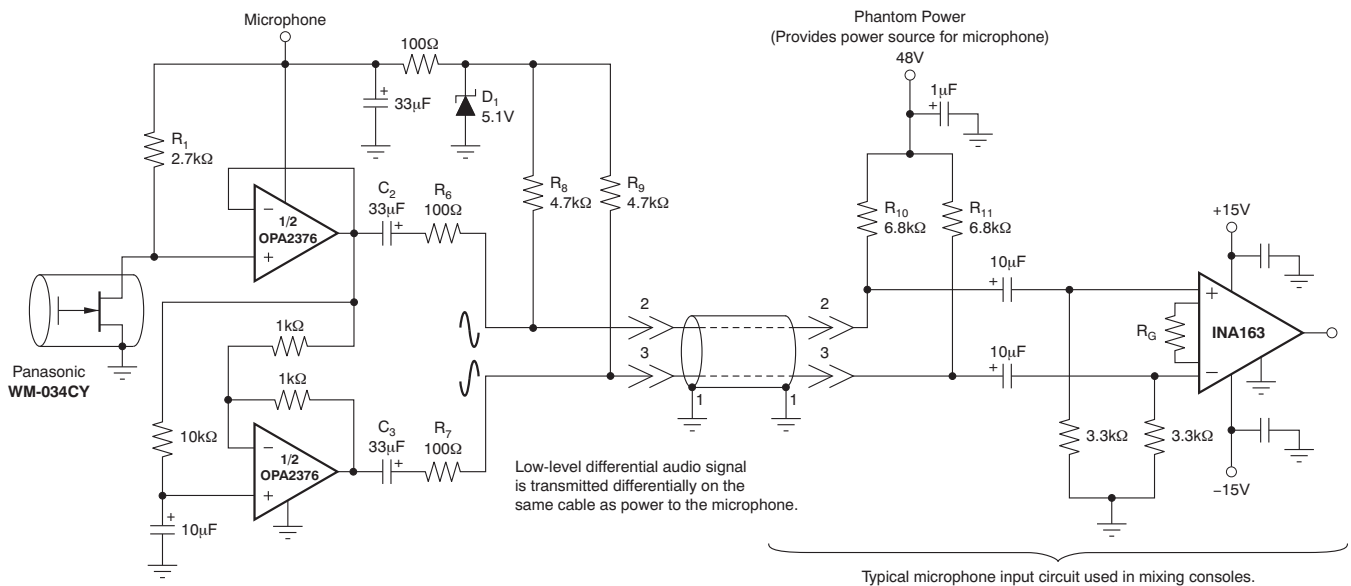
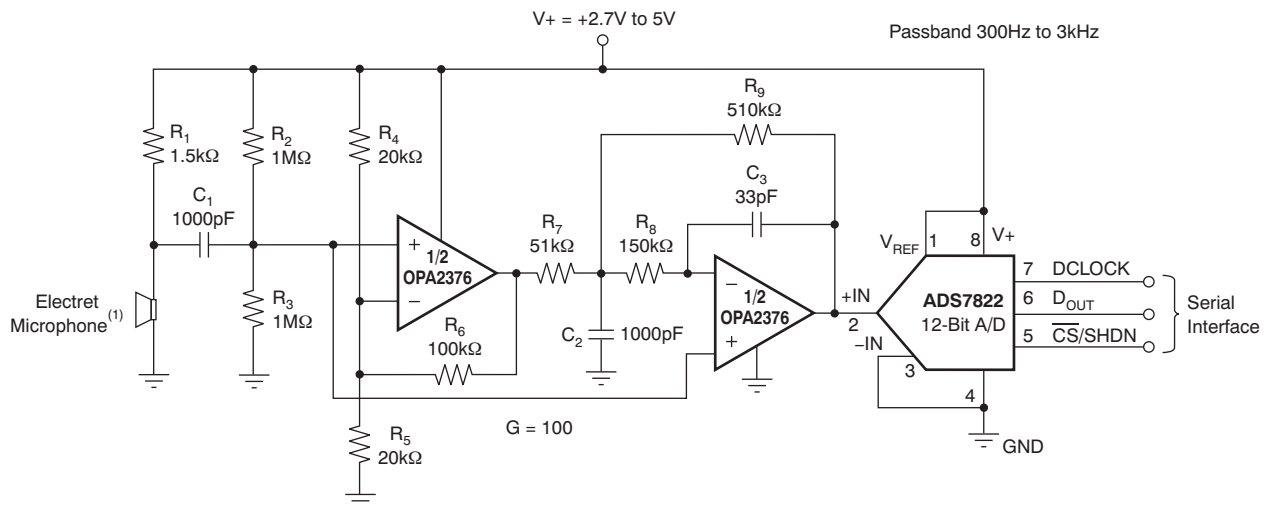


Figure 28. Phantom-Powered Electret Microphone

Figure 29 illustrates the OPA2376-Q1 driving a speech bandpass-filtered data acquisition system.

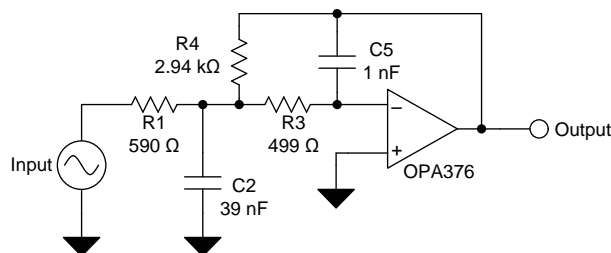


(1) Electret microphone powered by R<sub>1</sub>.

**Figure 29. OPA2376-Q1 as a Speech Bandpass-Filtered Data Acquisition System**

## 8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA376-Q1 is ideally suited to construct high-speed, high-precision active filters. Figure 30 shows a second-order, low-pass filter commonly encountered in signal processing applications.



**Figure 30. Typical Application Schematic**

## Typical Application (continued)

### 8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

#### 8.2.1.1 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in [Figure 30](#). Use [Equation 1](#) to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by [Equation 2](#):

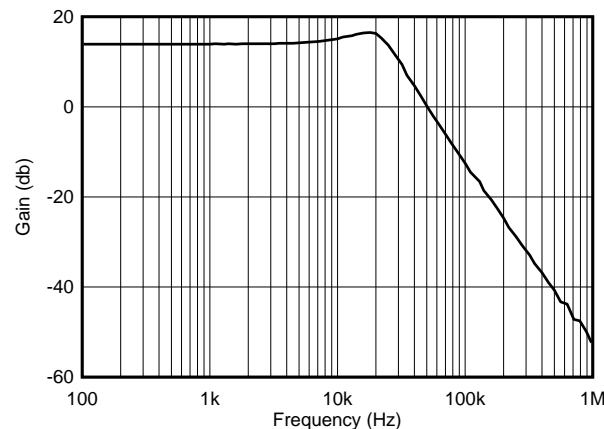
$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi} \sqrt{1/R_3 R_4 C_2 C_5} \quad (2)$$

Software tools are readily available to simplify filter design. [WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

### 8.2.2 Application Curve



**Figure 31. Low-Pass Filter Transfer Function**

## 9 Power Supply Recommendations

The OPAx376-Q1 family of devices is specified for operation from 2.2 V to 5.5 V ( $\pm 1.1$  V to  $\pm 2.75$  V); many specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

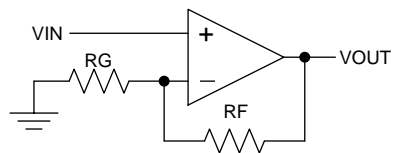
## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the application report, *Circuit Board Layout Techniques*, [SLOA089](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 32](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example



(Schematic Representation)

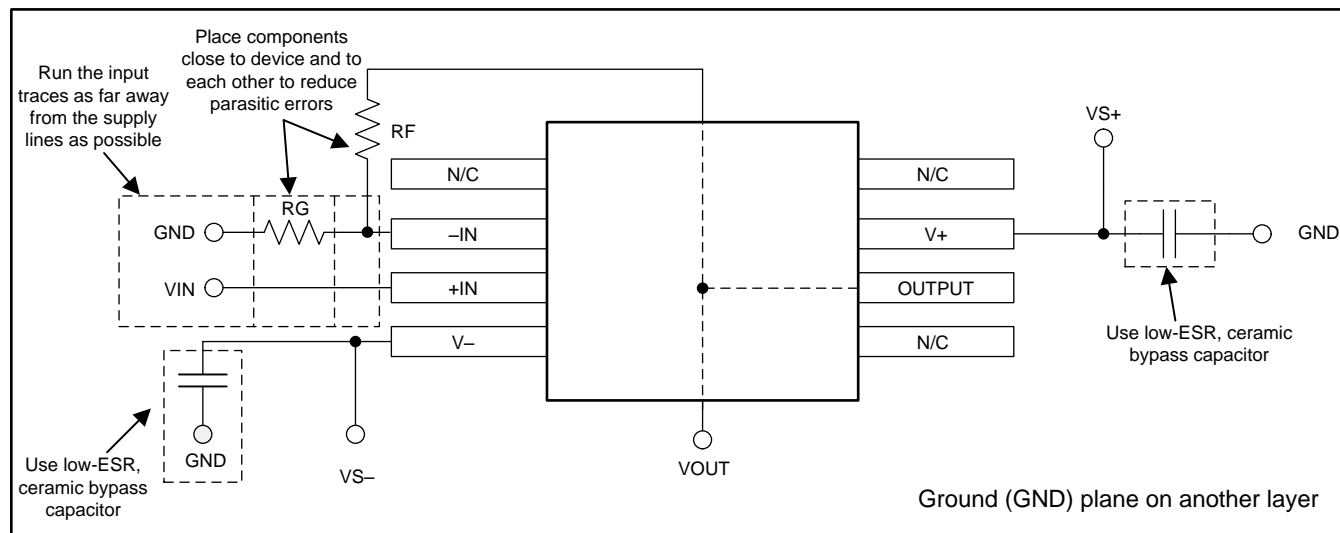


Figure 32. Layout Example

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 开发支持

##### 11.1.1.1 TINA-TI™ (免费下载)

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center (模拟电子实验室设计中心) [免费下载](#)，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

#### 注

这些文件需要安装 TINA 软件 (由 DesignSoft™提供) 或者 TINA-TI 软件。请从 [TINA-TI 文件夹](#) 中下载免费的 TINA-TI 软件。

##### 11.1.1.2 TI 高精度设计

TI 高精度设计是由 TI 公司的高精度模拟应用专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整 PCB 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 <http://www.ti.com.cn/www/analog/precision-designs/>。

##### 11.1.1.3 WEBENCH® Filter Designer

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。此 WEBENCH®滤波器设计器通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® Filter Designer。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

## 11.2 文档支持

### 11.2.1 相关文档

相关文档如下：

- 《电路板布局布线技巧》，[SLOA089](#)
- 《INA163: 低噪声、低失真仪表放大器》，[SBOS177](#)
- 《运算放大器增益稳定性，第 3 部分: 交流增益误差分析》，[SLYT383](#)
- 《运算放大器增益稳定性，第 2 部分: 直流增益误差分析》，[SLYT374](#)
- 《运算放大器性能分析》，[SBOS054](#)
- 《无铅组件涂层的保存期评估》，[SZZA046](#)
- 《运算放大器的单电源运行》，[SBOA059](#)
- 《调整放大器》，[SBOA067](#)
- 《在全差分有源滤波器中使用无限增益、MFB 滤波器拓扑》，[SLYT343](#)

### 11.3 相关链接

表 1 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
OPA376-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
OPA2376-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
OPA4376-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 商标

e-trim, E2E are trademarks of Texas Instruments.  
 TINA-TI is a trademark of Texas Instruments and DesignSoft, Inc.  
 WEBENCH is a registered trademark of Texas Instruments.  
 TINA, DesignSoft are trademarks of DesignSoft, Inc.  
 All other trademarks are the property of their respective owners.

### 11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

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	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2376AQRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2376Q1	<a href="#">Samples</a>
OPA2376QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2376	<a href="#">Samples</a>
OPA376AQBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUHQ	<a href="#">Samples</a>
OPA4376AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4376Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA376-Q1 :**

- Catalog: [OPA376](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2376AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2376QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA376AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA4376AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2376AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
OPA2376QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA376AQDBVRQ1	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA4376AQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

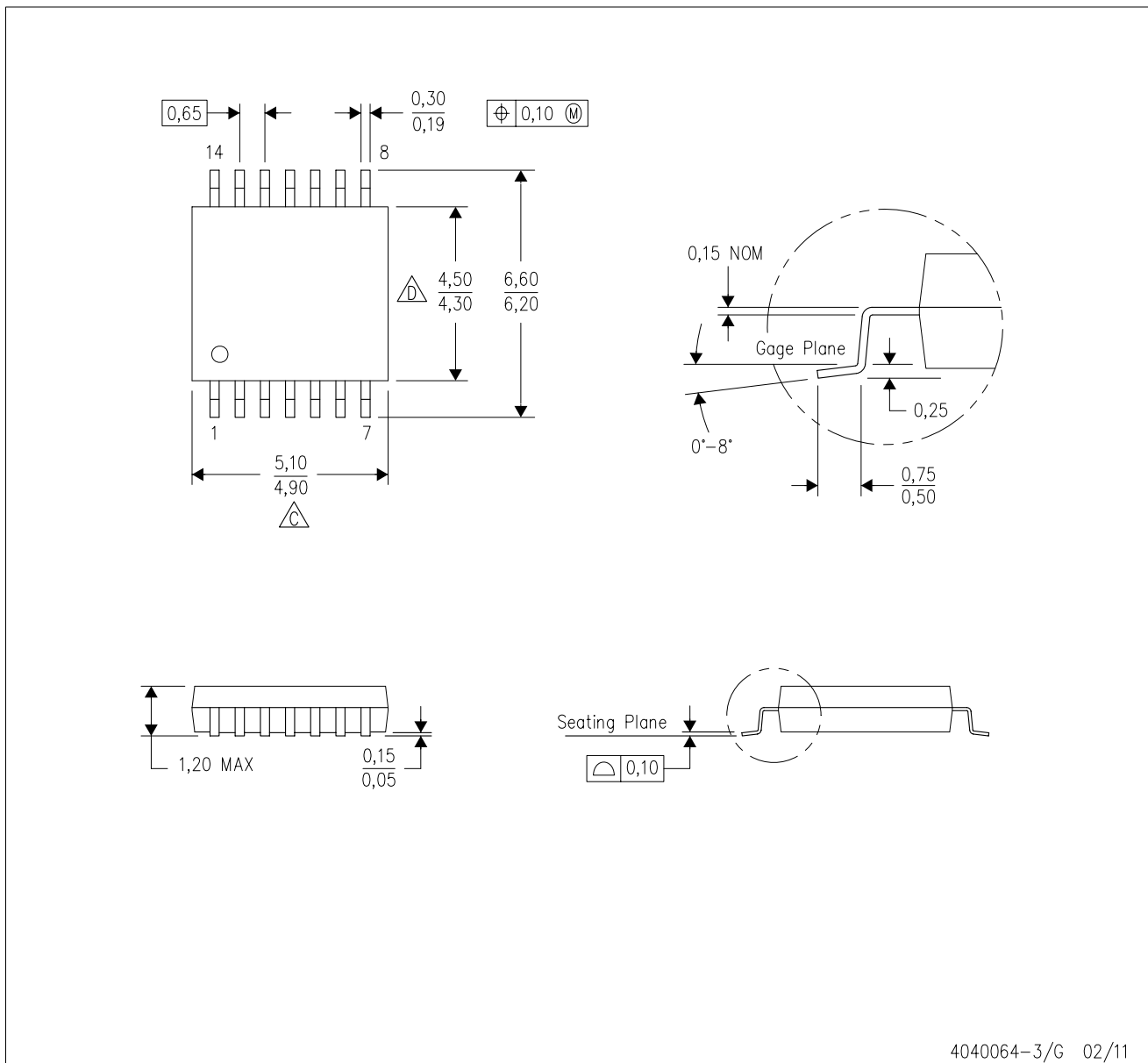




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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