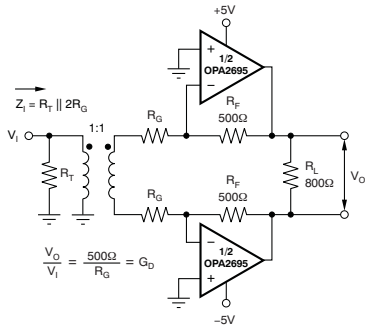
Dual, Ultra-Wideband, Current-Feedback OPERATIONAL AMPLIFIER with Disable

FEATURES

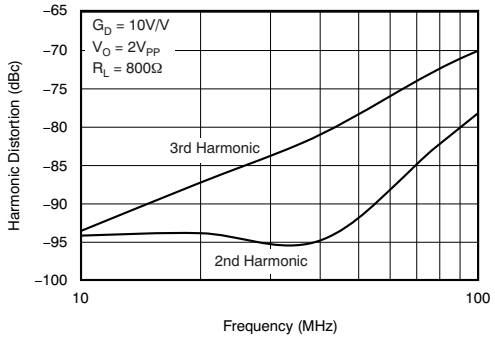
- GAIN = +2V/V BANDWIDTH (850MHz)
- GAIN = +8V/V BANDWIDTH (450MHz)
- OUTPUT VOLTAGE SWING: ±4.1V
- ULTRA-HIGH SLEW RATE: 2900V/µs
- DIFFERENTIAL 3RD-ORDER INTERCEPT: > 40dBm (f < 140MHz, 800Ω)
- LOW POWER: 129mW/channel
- LOW DISABLED POWER: 0.5mW/channel

APPLICATIONS

- VERY WIDEBAND ADC DRIVERS
- LOW-COST PRECISION IF AMPLIFIERS
- BROADBAND VIDEO LINE DRIVERS
- PORTABLE INSTRUMENTS
- ACTIVE FILTERS
- ARB WAVEFORM OUTPUT DRIVERS



Differential Driver Test Circuit



Differential Harmonic Distortion

DESCRIPTION

The OPA2695 is a dual, very high bandwidth, current-feedback op amp that combines exceptional 2900V/µs slew rate and low input voltage noise to deliver a precision, low-cost, high dynamic range intermediate frequency (IF) amplifier. The device has been optimized for high gain operation, and the pin outs of the two available packages (QFN-16, SO-8) have been optimized to provide symmetrical input and output paths. This architecture makes the OPA2695 an ideal choice as a differential driver, such as for a high-speed analog-to-digital converter (ADC).

The OPA2695 low 12.9mA/channel supply current is precisely trimmed at +25°C. This trim, along with a low temperature drift, gives low system power over temperature. System power may be further reduced with the optional disable control pin. Leaving this pin open, or holding it high, gives normal operation. If pulled low, the OPA2695 supply current drops to less than 200µA/channel. This power-saving feature, along with exceptional single +5V operation, makes the OPA2695 ideal for portable applications. The OPA2695 is available in an SO-8 (without disable) package or QFN-16 package (with disable).

OPA2695 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	COMMENTS
OPA695	—	OPA3695	Ultra-wideband current-feedback operational amplifier with disable
OPA691	OPA2691	OPA3691	Wideband, high output current, current-feedback operational amplifier with disable
OPA693	—	OPA3693	Ultra-wideband, fixed-gain operational amplifier
OPA694	OPA2694	—	Ultra-wideband, low-power, current-feedback operational amplifier

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2695	SO-8	D	–40°C to +85°C	OP2695	OPA2695ID	Rails, 75
					OPA2695IDR	Tape and Reel, 2500
OPA2695	QFN-16	RGT	–40°C to +85°C	2695	OPA2695IRGTT	Tape and Reel, 250
					OPA2695IRGTR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

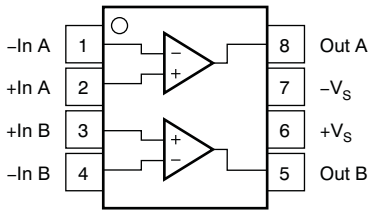
ABSOLUTE MAXIMUM RATINGS(1)

		OPA2695	UNITS
Power supply		±6.5	V_{DC}
Internal power dissipation		See Thermal Analysis	
Differential input voltage		±1.2	V
Input common-mode voltage range		$\pm V_S$	V
Storage temperature range: D, RGT		–65 to +125	°C
Lead temperature (soldering, 10s)		+300	°C
Junction temperature (T_J)		+150	°C
Junction temperature (T_J), continuous operation		+140	°C
ESD rating:	Human body model (HBM)(2)	1500	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	50	V

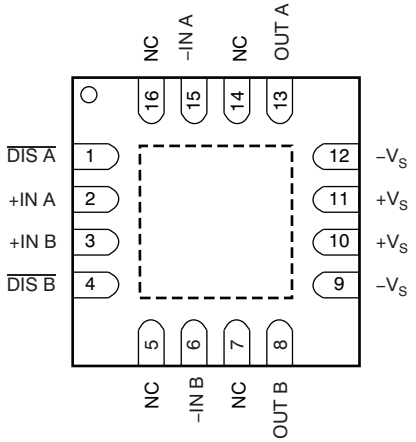
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these and any other conditions beyond those specified is not supported.
(2) Pins 1 and 4 on the SO-8 package and pins 6 and 15 on the QFN package are greater than 500V HBM.

PIN CONFIGURATIONS

SO-8 PACKAGE (TOP VIEW)



QFN-16 PACKAGE (TOP VIEW)



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω, and G = +8V/V, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2695ID, IRGT						TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 68)								
Small-signal bandwidth (V_O = 0.2V_{PP})	G = +1V/V, R_F = 523Ω	1100				MHz	typ	C
	G = +2V/V, R_F = 511Ω	850				MHz	typ	C
	G = +8V/V, R_F = 402Ω	450	400	380	350	MHz	min	B
	G = +16V/V, R_F = 249Ω	350				MHz	typ	C
Bandwidth for 0.2dB gain flatness	G = +2V/V, V_O = 0.2V_{PP}, R_F = 511Ω	300				MHz	min	B
Peaking at a gain of +1	R_F = 523Ω, V_O = 0.2V_{PP}	4.6	5.4	5.8	6.0	dB	max	B
Large-signal bandwidth	G = +8V/V, R_F = 402Ω, V_O = 4V_{PP}	400				MHz	typ	C
Slew rate	G = -8V/V, V_O = 4V step	2500	2000	1900	1800	V/µs	min	B
	G = +8V/V, V_O = 4V step	2900	2600	2500	2400	V/µs	min	B
Rise-and-fall time	G = +8V/V, V_O = 1V step	0.8				ns	typ	C
	G = +8V/V, V_O = 4V step	1.0				ns	typ	C
Settling time to 0.02%	G = +8V/V, V_O = 2V step	16				ns	typ	C
Settling time to 0.1%	G = +8V/V, V_O = 2V step	10				ns	typ	C
Harmonic distortion	G = +8V/V, f = 10MHz, V_O = 2V_{PP}							
2nd harmonic	R_L = 100Ω	–73	–62	–60	–59	dBc	max	B
	R_L ≥ 500Ω	–78	–76	–74	–73	dBc	max	B
3rd harmonic	R_L = 100Ω	–82	–80	–75	–72	dBc	max	B
	R_L ≥ 500Ω	–81	–80	–79	–78	dBc	max	B
Input voltage noise	f > 1MHz	1.8	2	2.7	2.9	nV/√Hz	max	B
Noninverting input current noise	f > 1MHz	18	19	21	22	pA/√Hz	max	B
Inverting input current noise	f > 1MHz	22	24	26	27	pA/√Hz	max	B
Differential gain	G = +2V/V, NTSC, V_O = 1.4V_{PP}, R_L = 150Ω	–0.01				%	typ	C
Differential phase	G = +2V/V, NTSC, V_O = 1.4V_{PP}, R_L = 150Ω	-0.05				°	typ	C
Crosstalk	f ≤ 10MHz	–50				dB	typ	C
DC PERFORMANCE(4)								
Open-loop transimpedance gain (Z_{OL})	V_O = 0V, R_L = 100Ω	85	**45**	43	41	kΩ	min	A
Input offset voltage	V_{CM} = 0V	±0.3	**±3.5**	±4.0	±4.5	mV	max	A
Average offset voltage drift	V_{CM} = 0V			±10	±15	µV/°C	max	B
Noninverting input bias current	V_{CM} = 0V	+13	**±30**	±37	±41	µA	max	A
Average noninverting input bias current drift	V_{CM} = 0V			+150	+180	nA/°C	max	B
Inverting input bias current	V_{CM} = 0V	±20	**±60**	±66	±70	µA	max	A
Average inverting input bias current drift	V_{CM} = 0V			±120	±160	nA/°C	max	B
INPUT								
Common-mode input voltage range (CMIR)(5)		±3.3	**±3.1**	±3.0	±3.0	V	min	A
Common-mode rejection ratio (CMRR)	V_{CM} = 0V	56	**51**	50	50	dB	min	A
Noninverting input Impedance		280 || 1.2				kΩ || pF	typ	C
Inverting input resistance (R_I)	Open-loop	29				Ω	typ	C
OUTPUT								
Voltage output swing	No load	±4.1	**±3.9**	±3.9	±3.9	V	min	A
	100Ω load	±3.9	**±3.7**	±3.7	±3.6	V	min	A
Current output, sourcing	V_O = 0	+120	**+90**	+80	+70	mA	min	A
Current output, sinking	V_O = 0	–120	**–90**	–80	–70	mA	min	A
Closed-loop output impedance	G = +8V/V, f = 100kHz	0.04				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +26°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω, and G = +8V/V, unless otherwise noted.

		OPA2695ID, IRGT						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
DISABLE (Disabled LOW)	QFN-16 (RGT) package only							
Power-down supply current (+V_S)	Both channels, $V_{\overline{DIS}}$ = 0	–200	**–340**	–375	–385	µA	typ	A
Disable time	V_{IN} = ±0.25V_{DC}	1				µs	typ	C
Enable time	V_{IN} = ±0.25V_{DC}	25				ns	typ	C
Off isolation	G = +8V/V, 10MHz	80				dB	typ	C
Output capacitance in disable		4				pF	typ	C
Turn-on glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0	±100				mV	typ	C
Turn-off glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0	±20				mV	typ	C
Enable voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control pin input bias current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	75	**130**	143	145	µA	max	A
POWER SUPPLY								
Specified operating voltage		±5				V	typ	C
Minimum operating voltage			±1.75	±1.8	±1.9	V	min	B
Maximum operating voltage			**±6**	±6	±6	V	max	A
Maximum quiescent current	Both channels, V_S = ±5V	25.8	**26.8**	27.6	28.6	mA	max	A
Minimum quiescent current	Both channels, V_S = ±5V	25.8	**25.2**	23.6	22	mA	min	A
Power-supply rejection ratio (+PSRR)	Input-referred	55	**51**	48	48	dB	typ	A
TEMPERATURE RANGE								
Specification: ID, IRGT		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
D SO-8		100				°C/W	typ	C
RGT QFN-16		55				°C/W	typ	C

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ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At R_F = 422Ω, R_L = 100Ω to V_S/2, and G = +8, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2695ID, IRGT						TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	
AC PERFORMANCE								
Small-signal bandwidth (V_O = 0.2V_{PP})	G = +1V/V, R_F = 511Ω	940				MHz	typ	C
	G = +2V/V, R_F = 487Ω	700				MHz	typ	C
	G = +8V/V, R_F = 348Ω	395	380	330	300	MHz	typ	B
	G = +16V/V, R_F = 162Ω	275				MHz	typ	C
Bandwidth for 0.2dB gain flatness	G = +2V/V, V_O < 0.2V_{PP}, R_F = 487Ω					MHz	min	B
Peaking at a gain of +1	R_F = 511Ω, V_O < 0.2V_{PP}	1.0	2.0	2.5	3.0	dB	max	B
Large-signal bandwidth	G = +8V/V, V_O = 2V_{PP}	363				MHz	typ	C
Slew rate	G = +8V/V, 2V step	1800	1300	1200	1100	V/µs	min	B
Rise-and-fall time	G = +8V/V, V_O = 2V step	1				ns	typ	C
Settling time to 0.02%	G = +8V/V, V_O = 2V step	16				ns	typ	C
Settling time to 0.1%	G = +8V/V, V_O = 2V step	10				ns	typ	C
Harmonic distortion	G = +8V/V, f = 10MHz, V_O = 2V_{PP}							
2nd harmonic	R_L = 100Ω to V_S/2	–67	–55	–55	–54	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–101	–64	–64	–63	dBc	max	B
3rd harmonic	R_L = 100Ω to V_S/2	–64	–62	–62	–63	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–92	–61	–61	–60	dBc	max	B
Input voltage noise	f > 1MHz	1.8	2	2.7	2.9	nV/√Hz	max	B
Noninverting input current noise	f > 1MHz	18	19	21	22	pA/√Hz	max	B
Inverting input current noise	f > 1MHz	22	24	26	27	pA/√Hz	max	B
DC PERFORMANCE(4)								
Open-loop transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 100Ω to V_S/2	70	**40**	38	36	kΩ	min	A
Input offset voltage	V_{CM} = V_S/2	±0.3	**±3.5**	±4.0	±4.5	mV	max	A
Average offset voltage drift	V_{CM} = V_S/2			±10	±15	µV/°C	max	B
Noninverting input bias current	V_{CM} = V_S/2	±5	**±40**	±45	±50	µA	max	A
Average noninverting input bias current drift	V_{CM} = V_S/2			±110	±170	nA/°C	max	B
Inverting input bias current	V_{CM} = V_S/2	±10	**±60**	±66	±70	µA	max	A
Average inverting input bias current drift	V_{CM} = V_S/2			±120	±160	nA/°C	max	B
INPUT								
Least positive input voltage(5)		1.7	**1.8**	1.9	1.9	V	max	A
Most positive input voltage(5)		3.3	**3.2**	3.1	3.1	V	min	A
Common-mode rejection ratio (CMRR)	V_{CM} = V_S/2	54	**51**	50	50	dB	min	A
Noninverting input impedance		280 || 1.2				kΩ || pF	typ	C
Inverting input resistance (R_I)	Open-loop	32				Ω	typ	C
OUTPUT								
Most positive output voltage	No load	4.2	**4.0**	3.9	3.8	V	min	A
	R_L = 100Ω load to V_S/2	4.0	**3.9**	3.8	3.7	V	min	A
Least positive output voltage	No load	0.8	**1.0**	1.1	1.2	V	max	A
	R_L = 100Ω load to V_S/2	1.0	**1.1**	1.2	1.3	V	max	A
Current output, sourcing	V_O = V_S/2	+90	**+70**	+67	+66	mA	min	A
Current output, sinking	V_O = V_S/2	–90	**–70**	–67	–66	mA	min	A
Closed-loop output impedance	G = +2V/V, f = 100kHz	0.05				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +12°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

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ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**

At R_F = 422Ω, R_L = 100Ω to V_S/2, and G = +8, unless otherwise noted.

		OPA2695ID, IRGT						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
DISABLE (Disabled LOW)	QFN-16 (RGT) package only							
Power-down supply current (+V_S)	Both channels, $V_{\overline{DIS}}$ = 0	–190	**–320**	–350	–360	µA	max	A
Disable time		1				µs	typ	C
Enable time		25				ns	typ	C
Off isolation	G = +8V/V, 10MHz	80				dB	typ	C
Output capacitance in disable		4				pF	typ	C
Turn-on glitch	G = +2V/V, R_L = 150Ω, V_{IN} = V_S/2	±100				mV	typ	C
Turn-off glitch	G = +2V/V, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control pin input bias current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	75	**130**	143	149	µA	max	A
POWER SUPPLY								
Specified single-supply operating voltage		5				V	typ	C
Minimum single-supply operating voltage		3.5	3.6	3.6	3.8	V	min	B
Maximum single-supply operating voltage			**12**	12	12	V	max	A
Maximum quiescent current	Both channels, V_S = +5V	22.8	**24.2**	25.2	26.0	mA	max	A
Minimum quiescent current	Both channels, V_S = +5V	22.8	**21.8**	18.8	18.2	mA	min	A
Power-supply rejection ratio (+PSRR)	Input-referred	56				dB	typ	C
TEMPERATURE RANGE								
Specification: ID, IRGT		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
D SO-8		100				°C/W	typ	C
RGT QFN-16		55				°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V

At G = +8V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

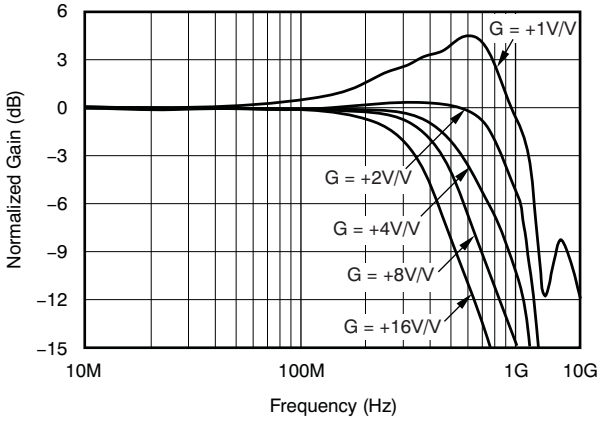


Figure 1.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

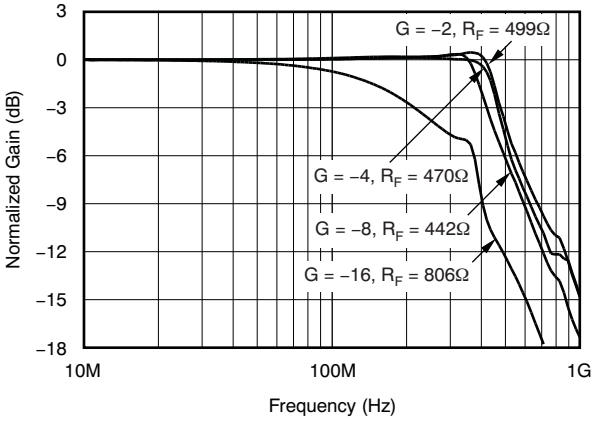


Figure 2.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

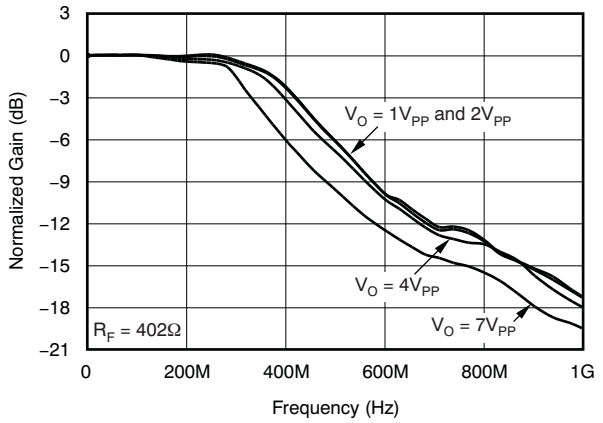


Figure 3.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

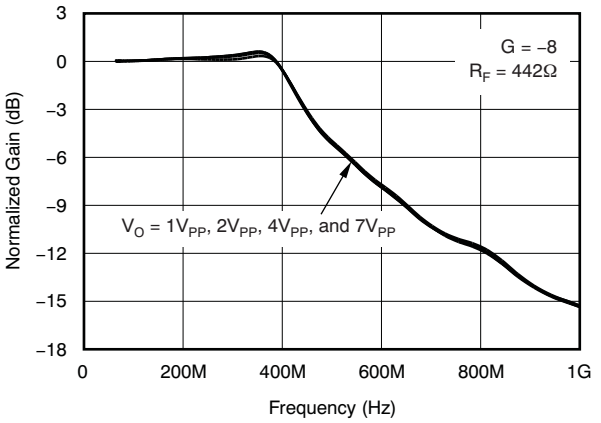


Figure 4.

NONINVERTING PULSE RESPONSE

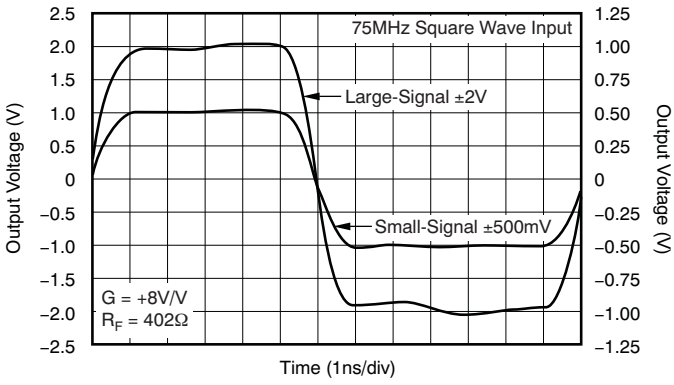


Figure 5.

INVERTING PULSE RESPONSE

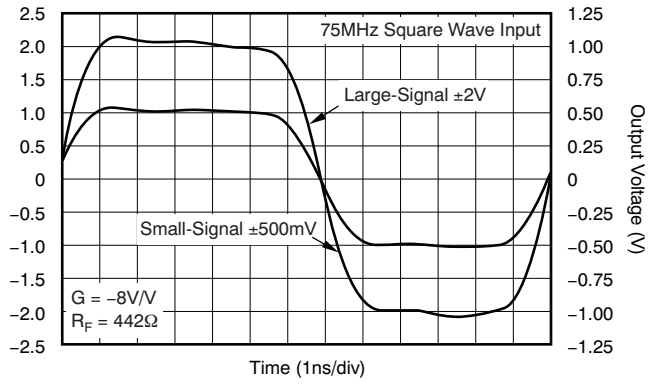


Figure 6.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +8V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

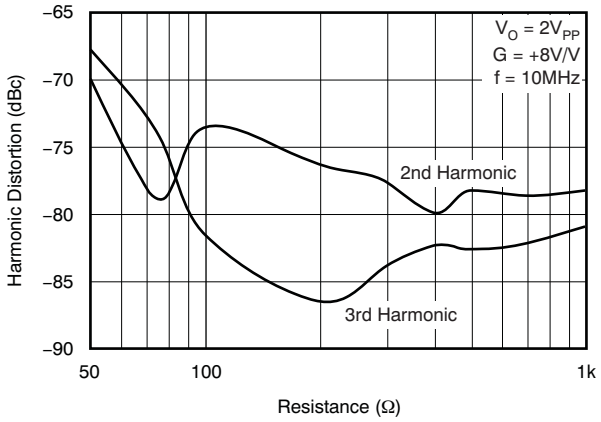


Figure 7.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

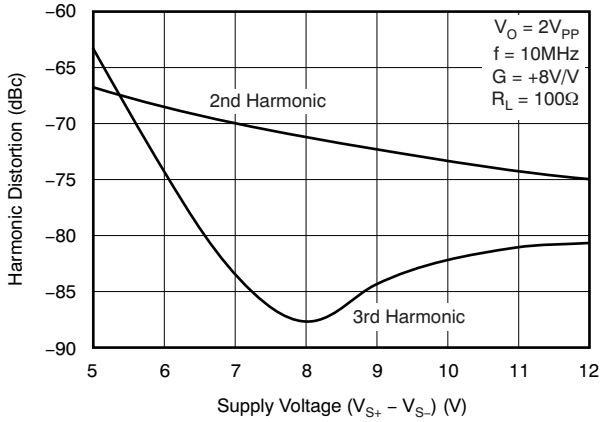


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

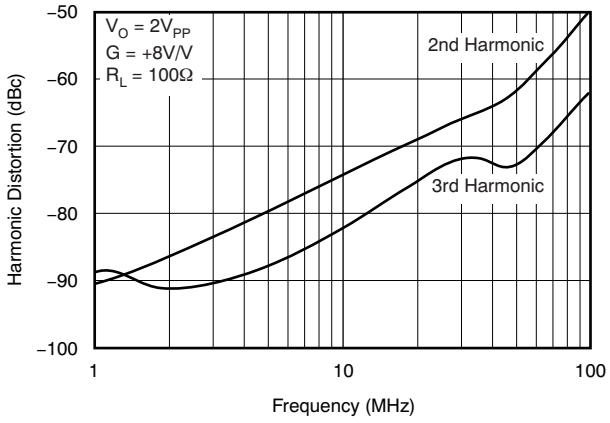


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

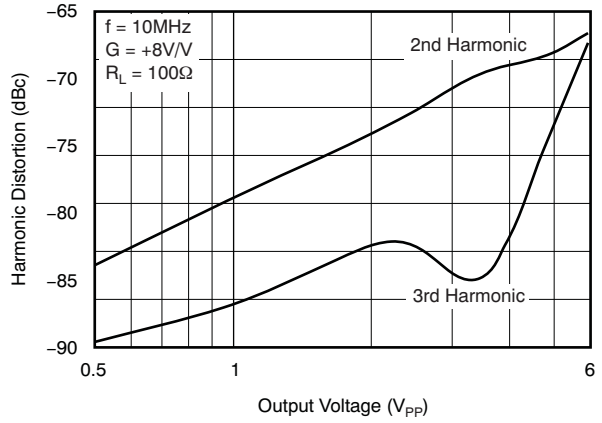


Figure 10.

HARMONIC DISTORTION vs NONINVERTING GAIN

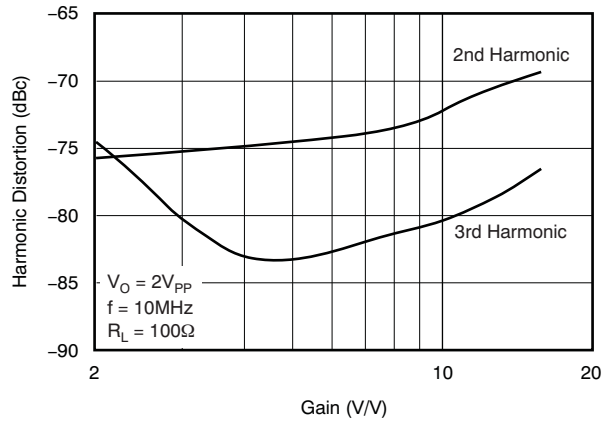


Figure 11.

HARMONIC DISTORTION vs INVERTING GAIN

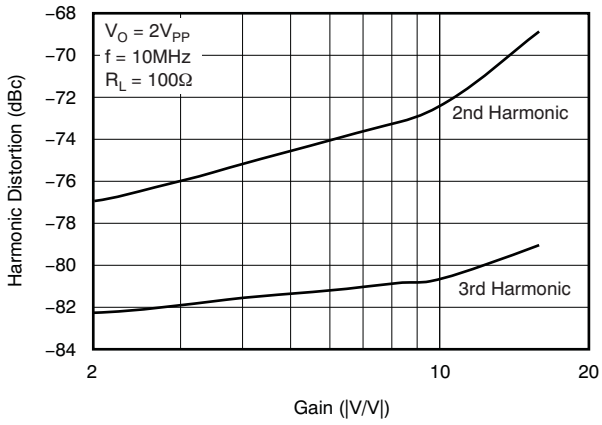


Figure 12.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +8V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

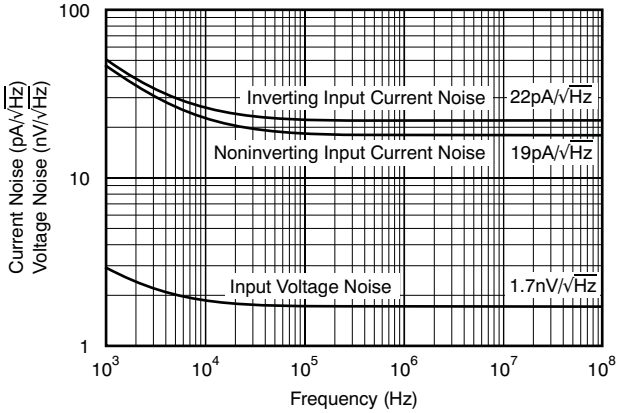


Figure 13.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

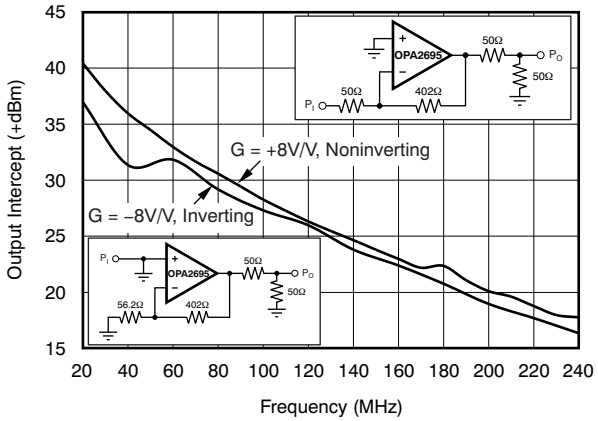


Figure 14.

INPUT RETURN LOSS vs FREQUENCY (S_{11})

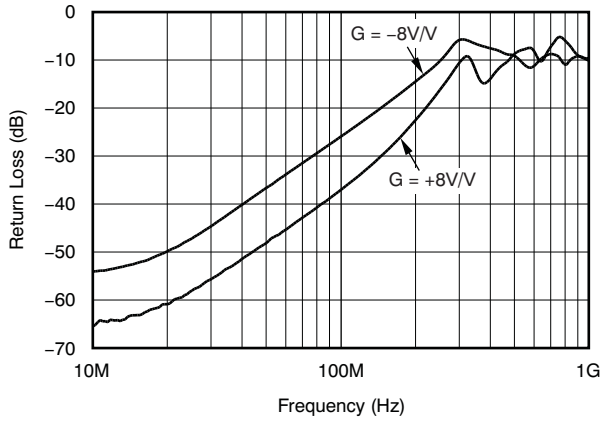


Figure 15.

OUTPUT RETURN LOSS vs FREQUENCY (S_{22})

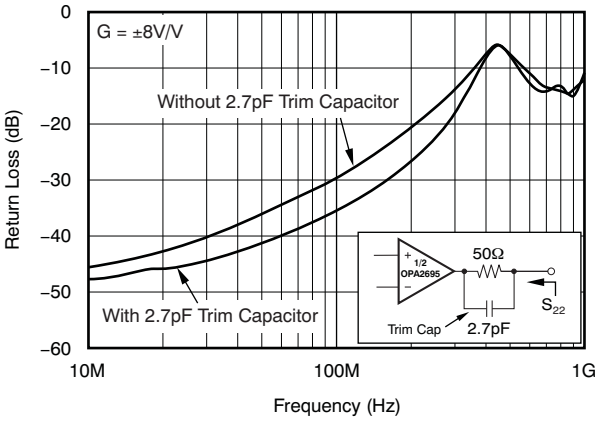


Figure 16.

RECOMMENDED R_S vs CAPACITIVE LOAD

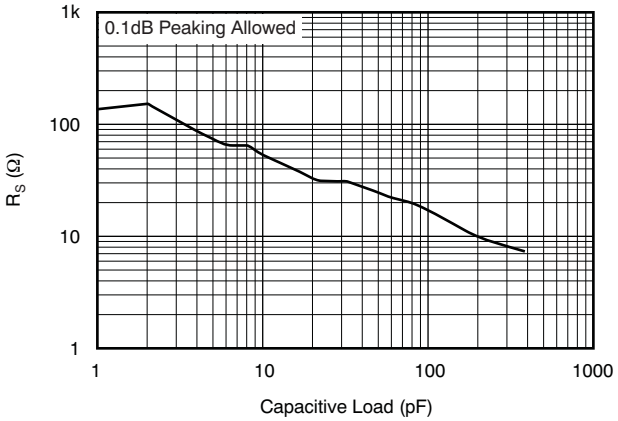


Figure 17.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOAD

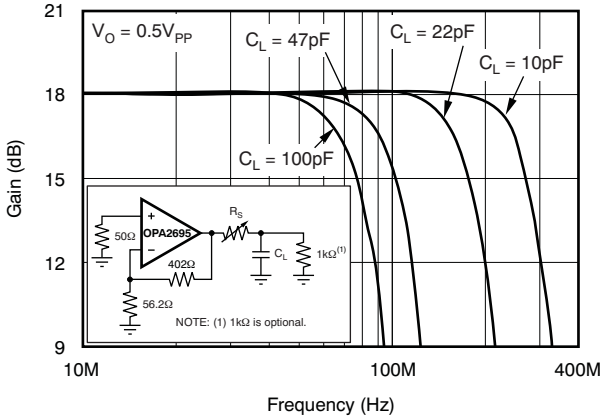


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +8V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

CMRR AND PSRR vs FREQUENCY

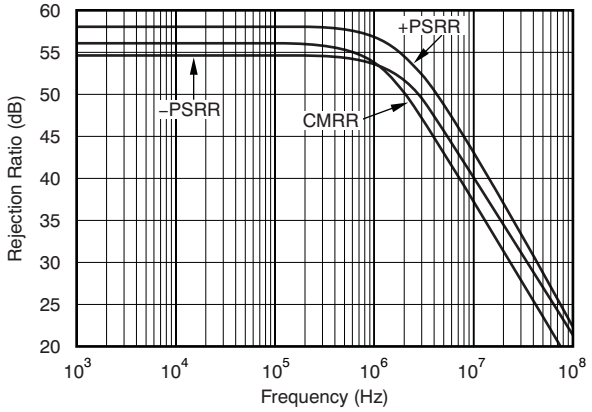


Figure 19.

OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE

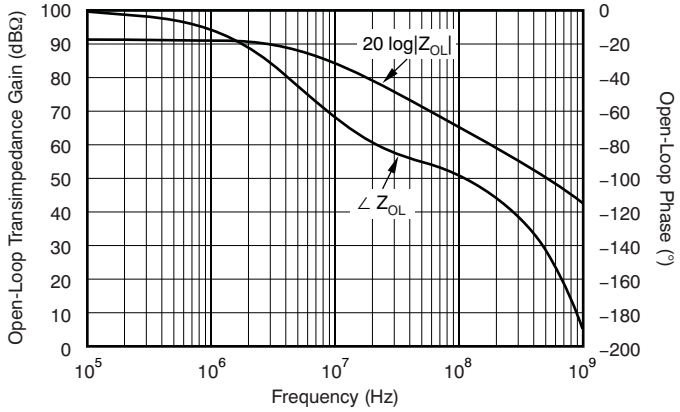


Figure 20.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

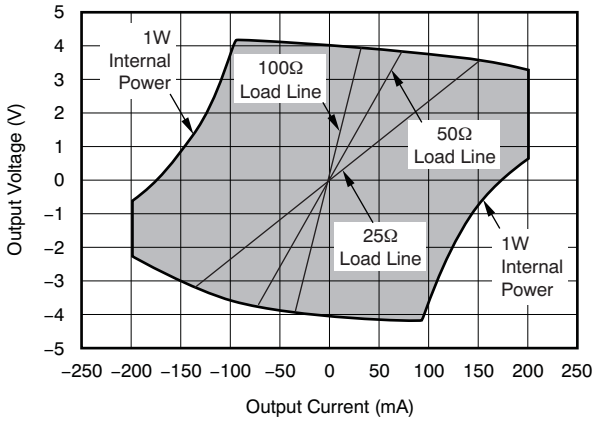


Figure 21.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

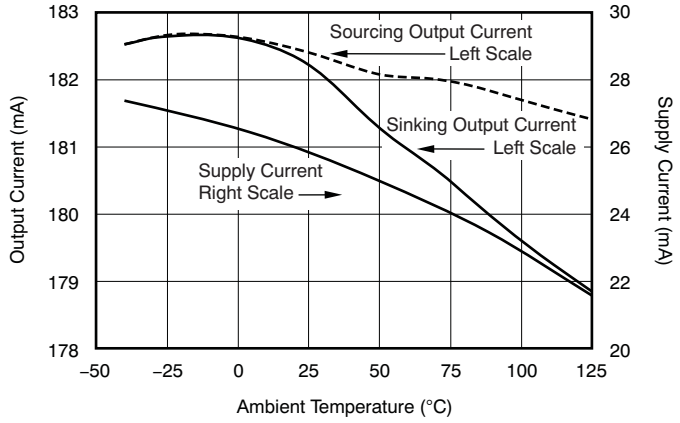


Figure 22.

NONINVERTING OVERDRIVE RECOVERY

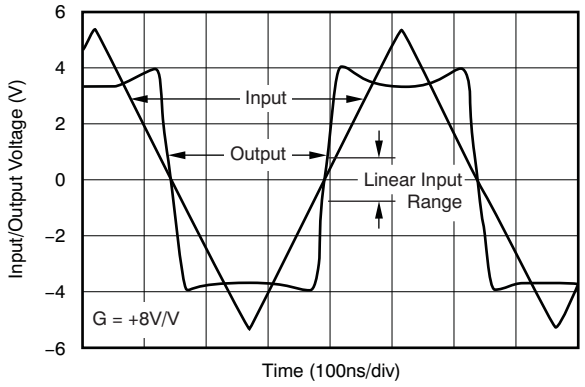


Figure 23.

INVERTING OVERDRIVE RECOVERY

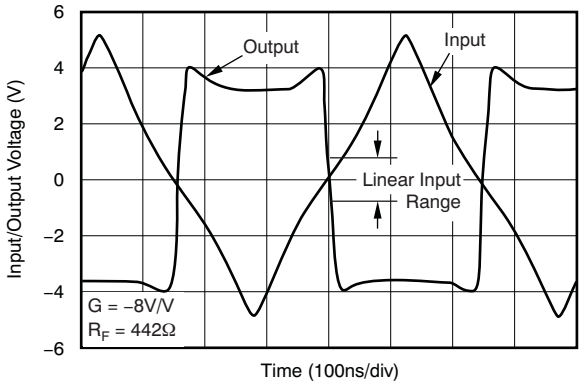


Figure 24.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +8V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

SETTLING TIME

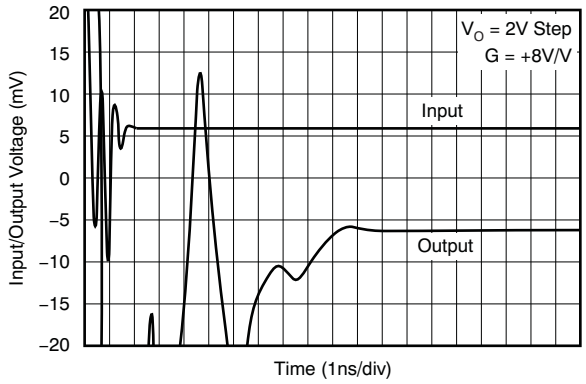


Figure 25.

DISABLE FEEDTHROUGH vs FREQUENCY

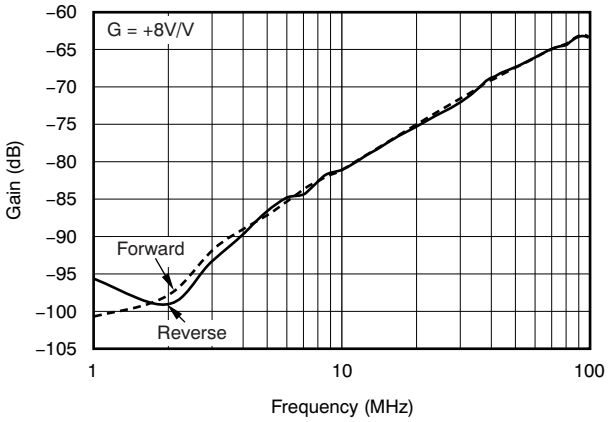


Figure 26.

COMPOSITE VIDEO (dG/dØ)

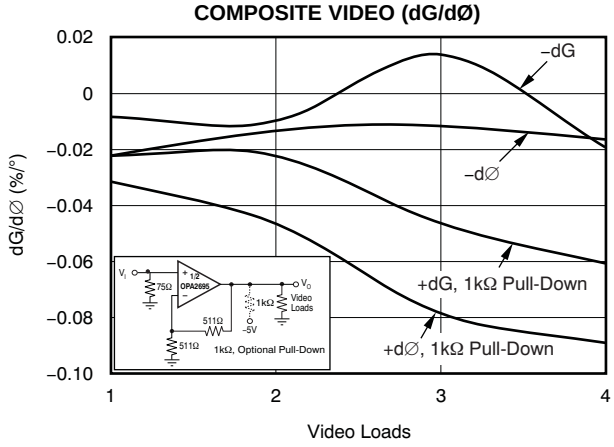


Figure 27.

TYPICAL DC DRIFT OVER TEMPERATURE

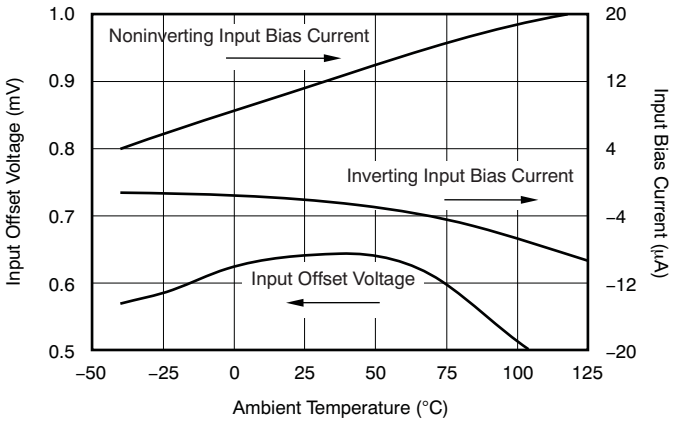


Figure 28.

COMMON-MODE INPUT AND OUTPUT SWING vs SUPPLY VOLTAGE

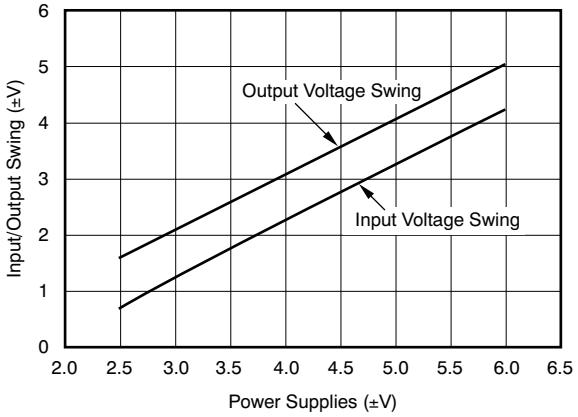


Figure 29.

LARGE-SIGNAL DISABLE/ENABLE RESPONSE

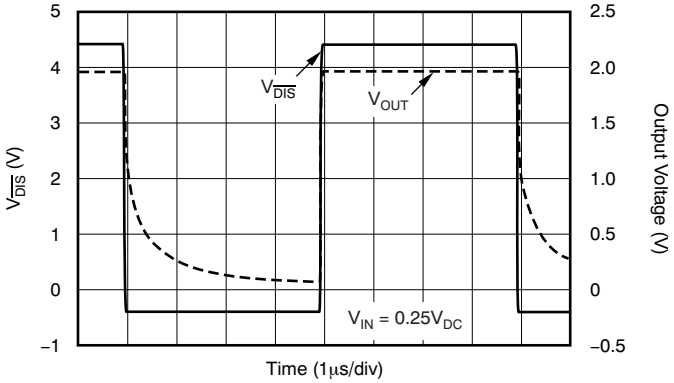


Figure 30.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +8V/V, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

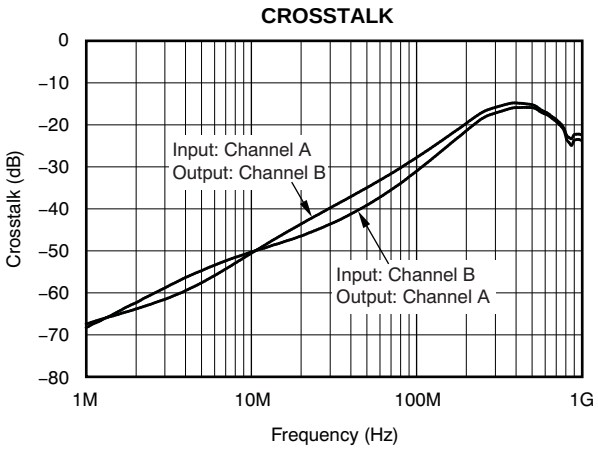


Figure 31.

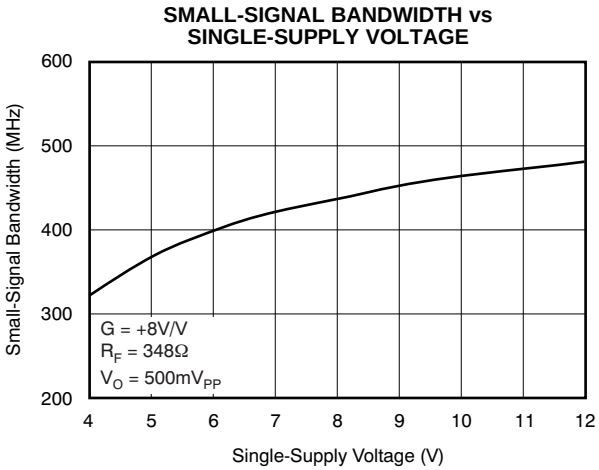


Figure 32.

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TYPICAL CHARACTERISTICS: V_S = ±5V, Differential Operation

At G_D = 10V/V, R_F = 500Ω, and R_L = 800Ω, unless otherwise noted.

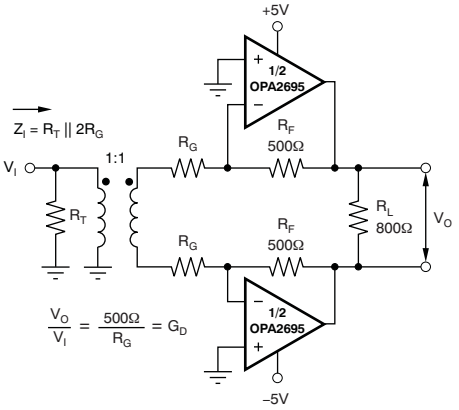


Figure 33.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

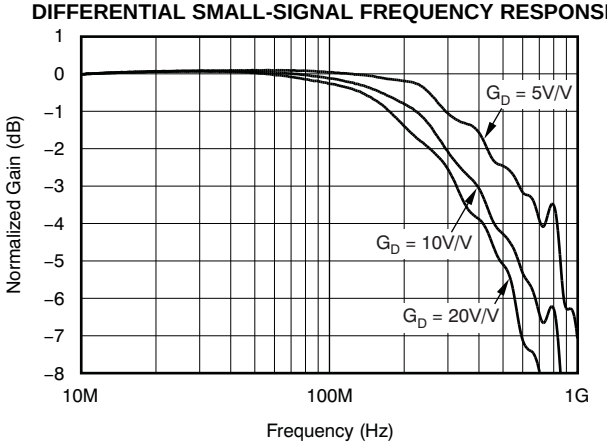


Figure 34.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

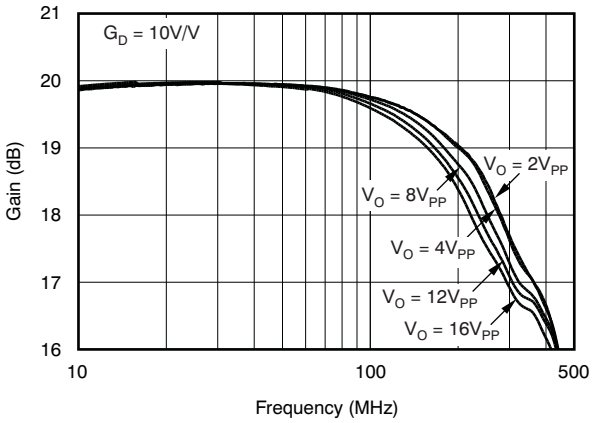


Figure 35.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY

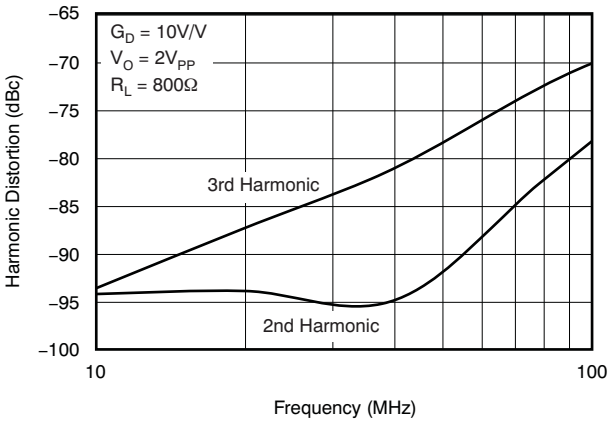


Figure 36.

RECOMMENDED R_S vs CAPACITIVE LOAD

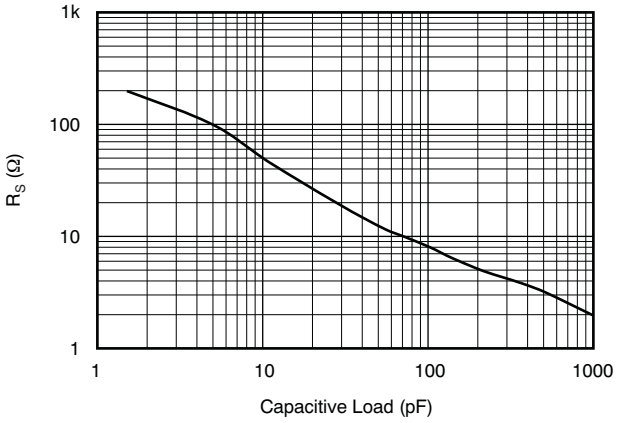


Figure 37.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

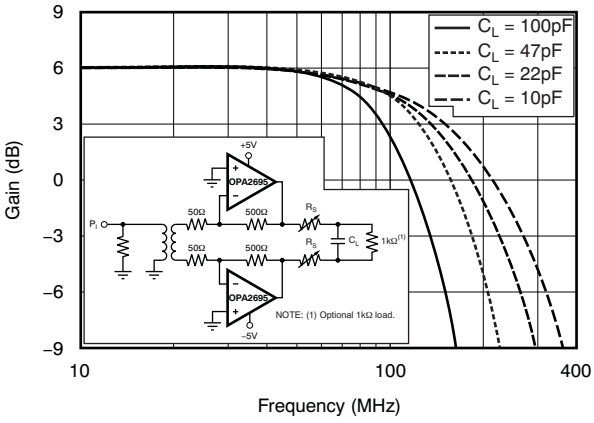


Figure 38.

TYPICAL CHARACTERISTICS: V_S = ±5V, Differential Operation (continued)

At G_D = 10V/V, R_F = 500Ω, and R_L = 800Ω, unless otherwise noted.

DIFFERENTIAL HARMONIC DISTORTION vs LOAD RESISTANCE

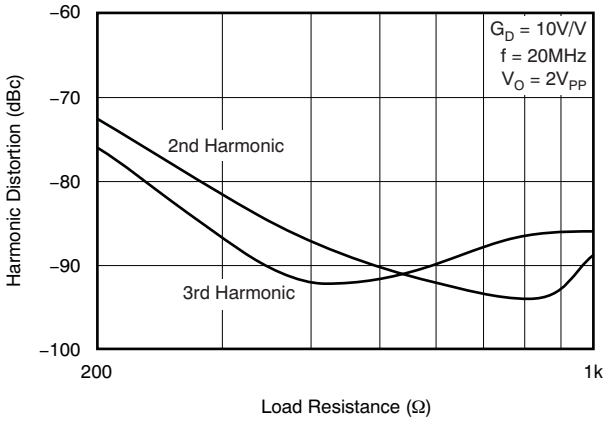


Figure 39.

DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT VOLTAGE

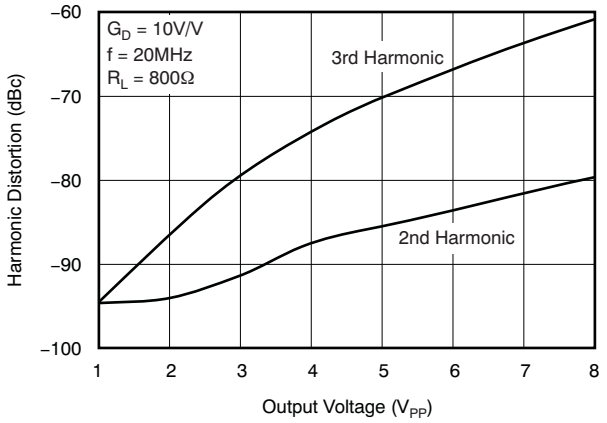


Figure 40.

DIFFERENTIAL HARMONIC DISTORTION vs NONINVERTING GAIN

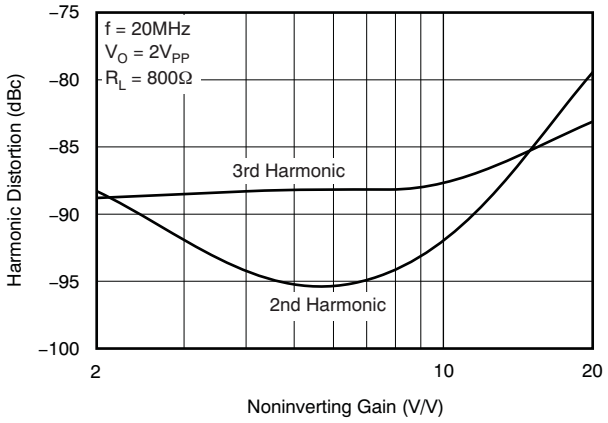


Figure 41.

DIFFERENTIAL HARMONIC DISTORTION vs INVERTING GAIN

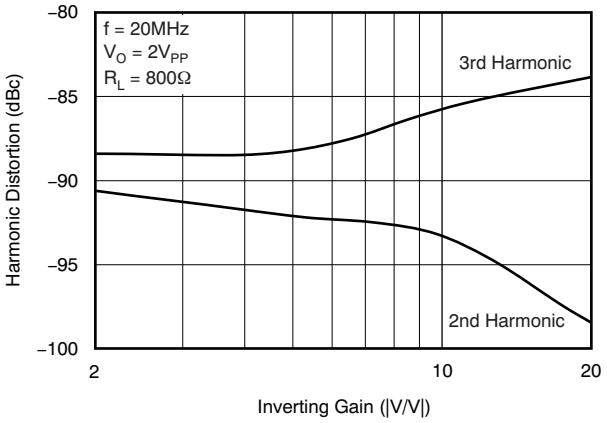


Figure 42.

DIFFERENTIAL HARMONIC DISTORTION vs SUPPLY VOLTAGE

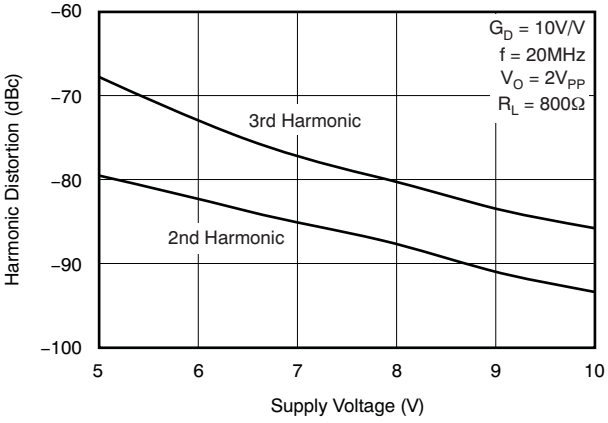


Figure 43.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

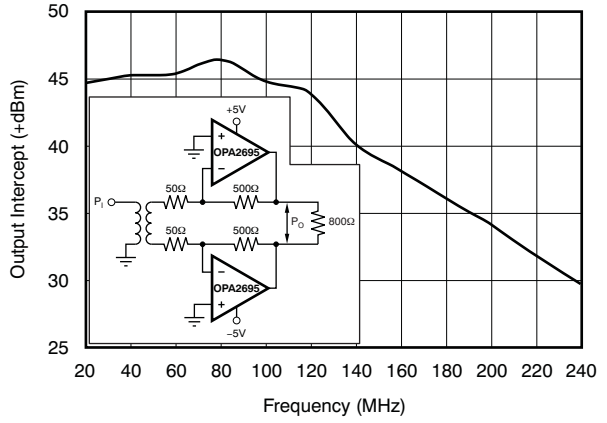


Figure 44.

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TYPICAL CHARACTERISTICS: V_S = 5V

At G = +8V/V, R_F = 348Ω, and R_L = 100Ω, unless otherwise noted.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

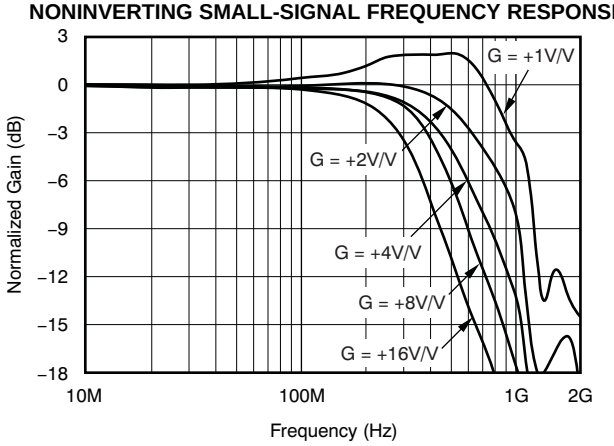


Figure 45.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

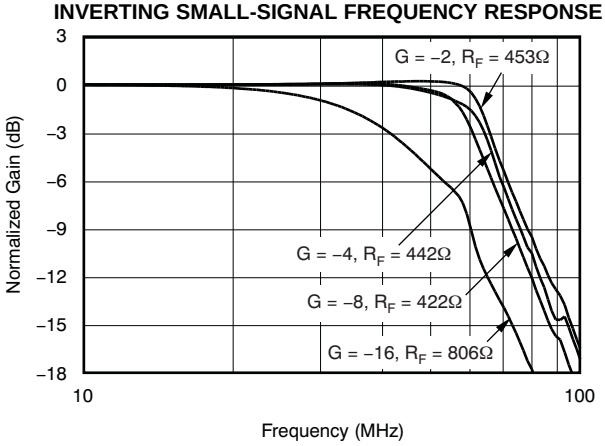


Figure 46.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

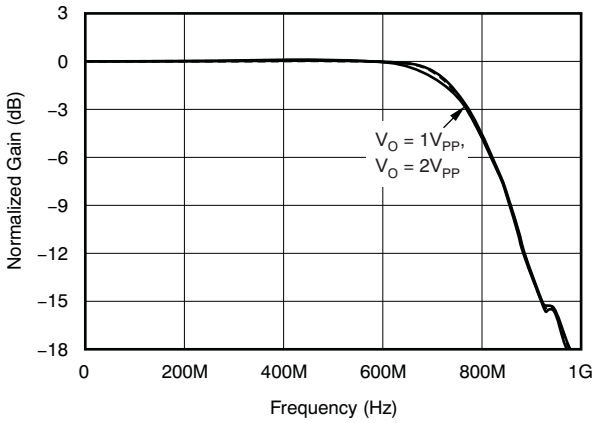


Figure 47.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

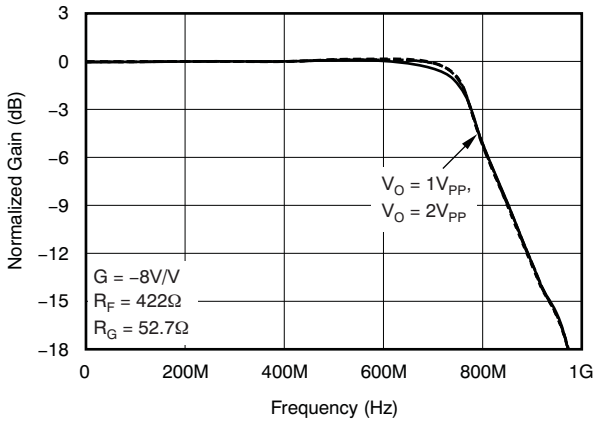


Figure 48.

NONINVERTING PULSE RESPONSE

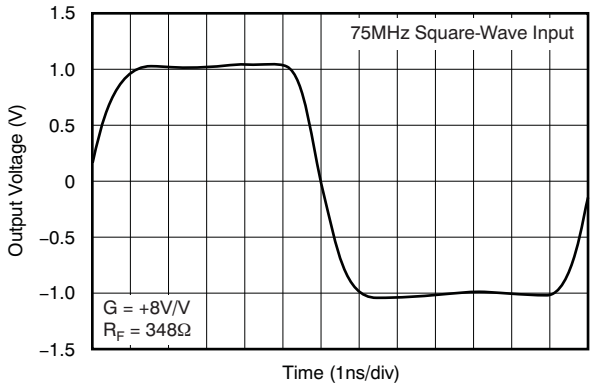


Figure 49.

INVERTING PULSE RESPONSE

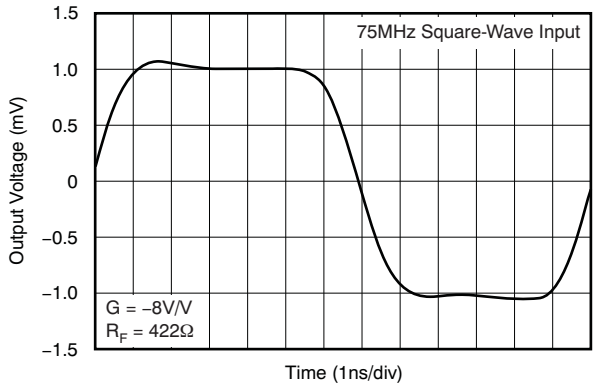


Figure 50.

TYPICAL CHARACTERISTICS: V_S = 5V (continued)

At G = +8V/V, R_F = 348Ω, and R_L = 100Ω, unless otherwise noted.

RECOMMENDED R_S vs CAPACITIVE LOAD

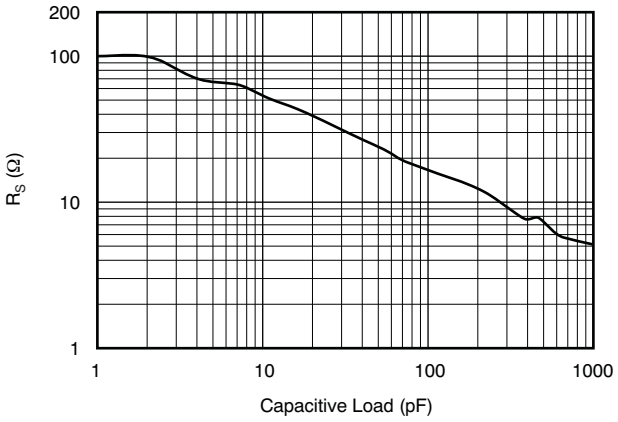


Figure 51.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

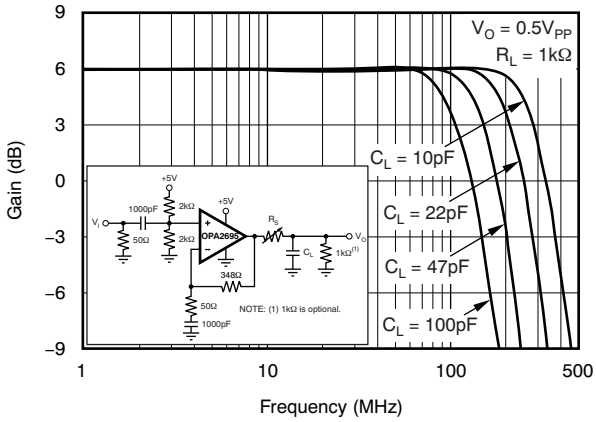


Figure 52.

HARMONIC DISTORTION vs FREQUENCY

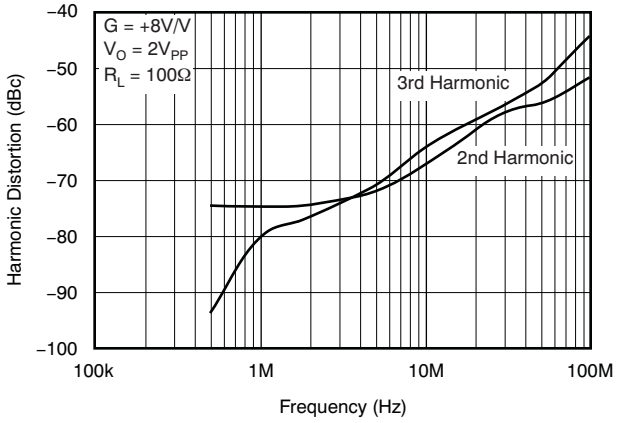


Figure 53.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

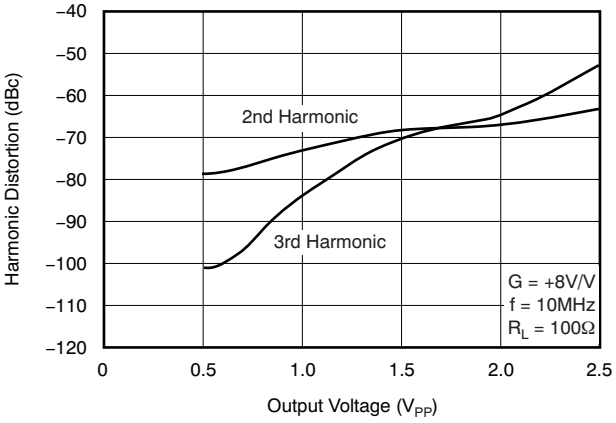


Figure 54.

HARMONIC DISTORTION vs LOAD RESISTANCE

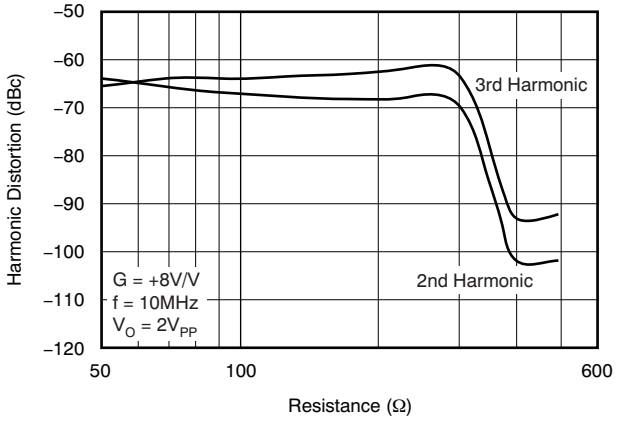


Figure 55.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

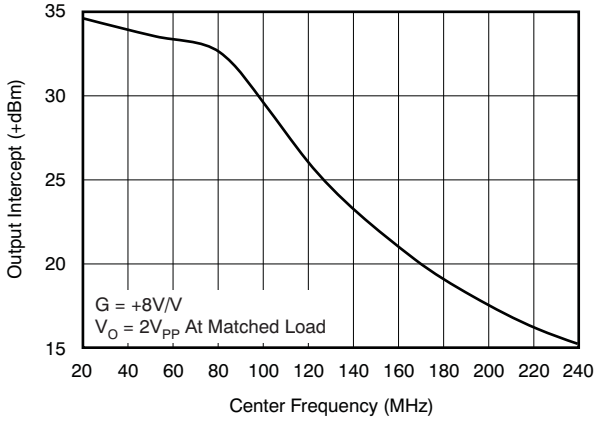


Figure 56.

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TYPICAL CHARCTERISTICS: V_S = 5V, Differential Operation

At G_D = 10V/V, R_F = 500Ω, and R_L = 800Ω, unless otherwise noted.

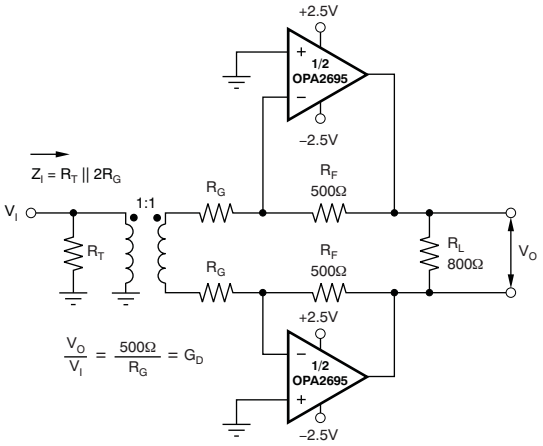


Figure 57.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

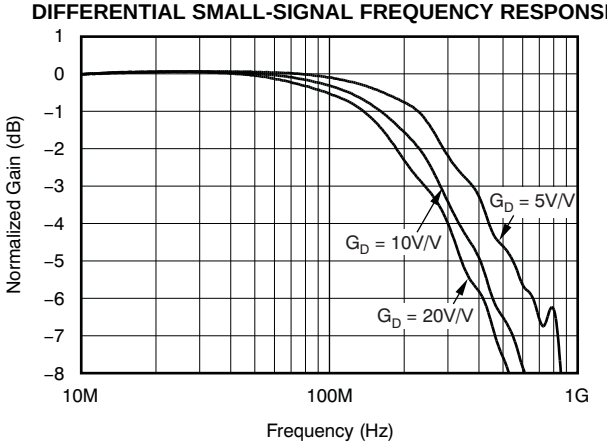


Figure 58.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

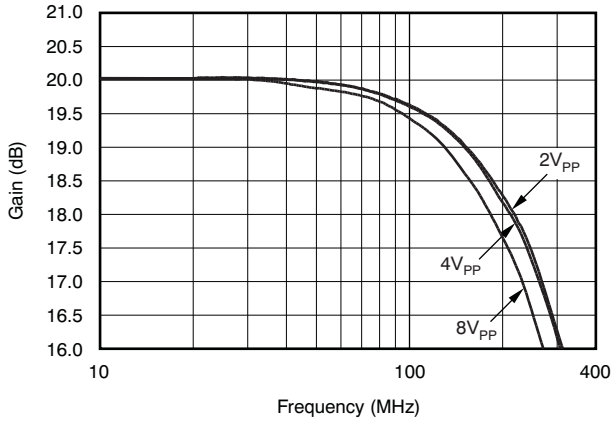


Figure 59.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

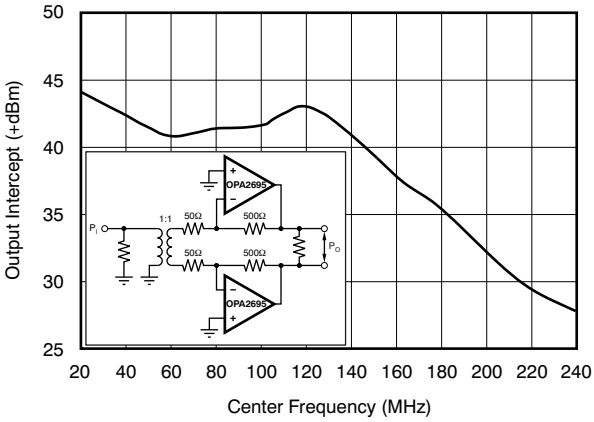


Figure 60.

RECOMMENDED R_S vs CAPACITIVE LOAD

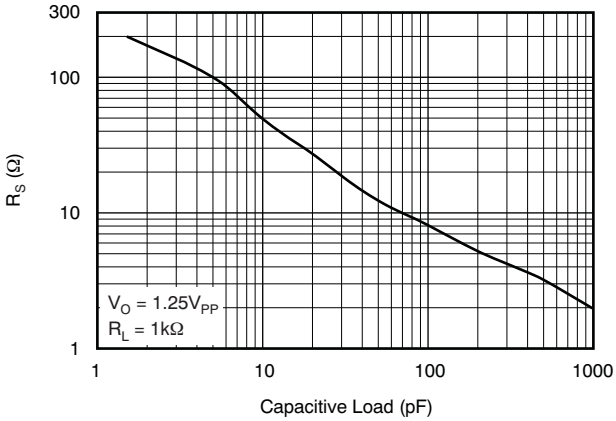


Figure 61.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

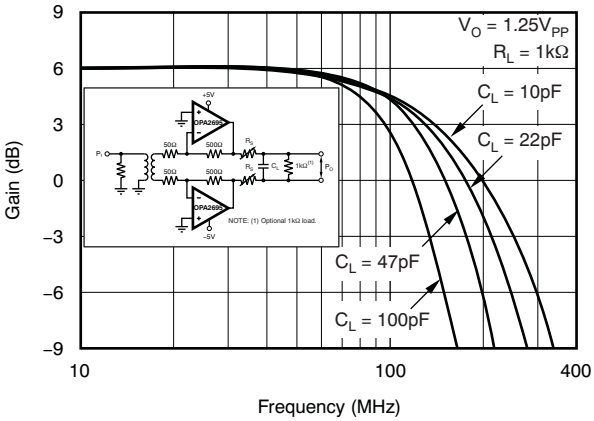


Figure 62.

TYPICAL CHARCTERISTICS: V_S = 5V, Differential Operation (continued)

At G_D = 10V/V, R_F = 500Ω, and R_L = 800Ω, unless otherwise noted.

DIFFERENTIAL HARMONIC DISTORTION vs LOAD RESISTANCE

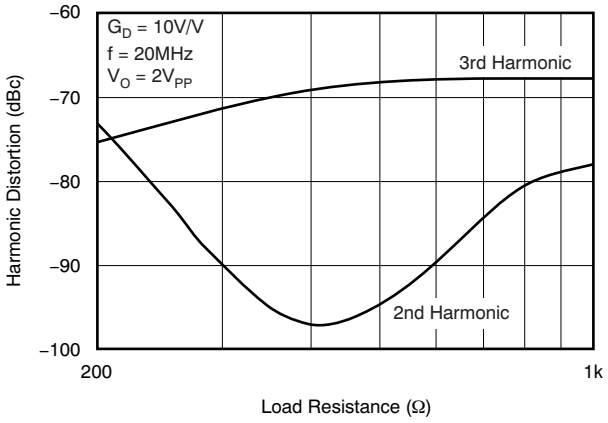


Figure 63.

DIFFERENTIAL HARMONIC DISTORTION vs OUTPUT VOLTAGE

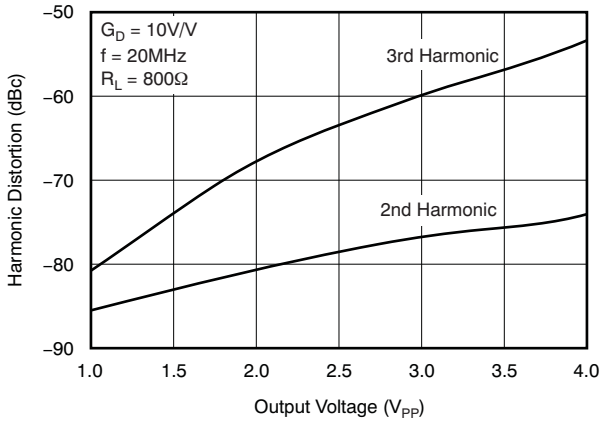


Figure 64.

DIFFERENTIAL HARMONIC DISTORTION vs NONINVERTING GAIN

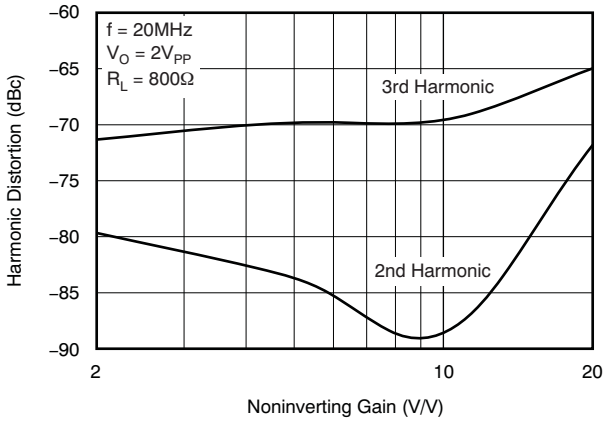


Figure 65.

DIFFERENTIAL HARMONIC DISTORTION vs INVERTING GAIN

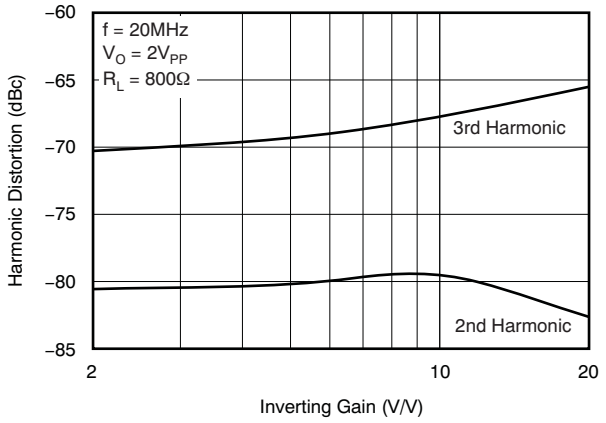


Figure 66.

DIFFERENTIAL HARMONIC DISTORTION vs FREQUENCY

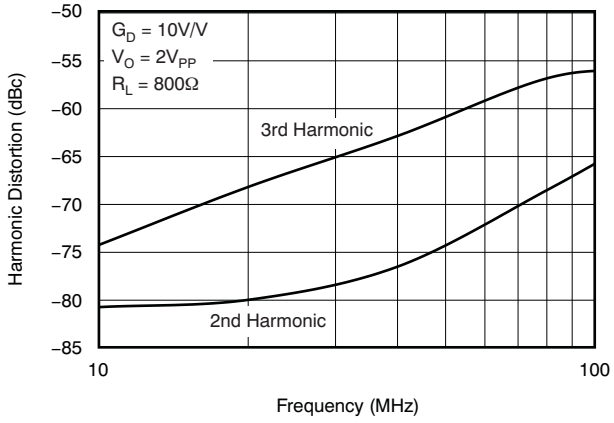


Figure 67.

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APPLICATIONS INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2695 gives a new level of performance in wideband current-feedback op amps. Nearly constant ac performance over a wide gain range, along with 2900V/µs slew rate, gives a lower power and cost solution for high-intercept IF amplifier requirements. While optimized at a gain of +8V/V (12dB to a matched 50Ω load) to give 450MHz bandwidth, applications from gains of 1 to 40 can be supported. At gains above 20, the signal bandwidth starts to decrease, but continues to exceed 180MHz up to a gain of 40V/V (26dB to a matched 50Ω load). Single +5V supply operation is also supported with similar bandwidths but reduced output power capability. For lower speed (< 250MHz) requirements with higher output power, consider the OPA2691.

Figure 68 shows the dc-coupled, gain of +8V/V, dual power-supply circuit used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 68, the total effective load is 100Ω || 458Ω = 82Ω. The disable control line ($\overline{DIS}$) is typically left open to get normal amplifier operation. The disable line must be asserted low to shut off the OPA2695. Figure 68 includes one optional component. In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional added capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB for bipolar supply operation.

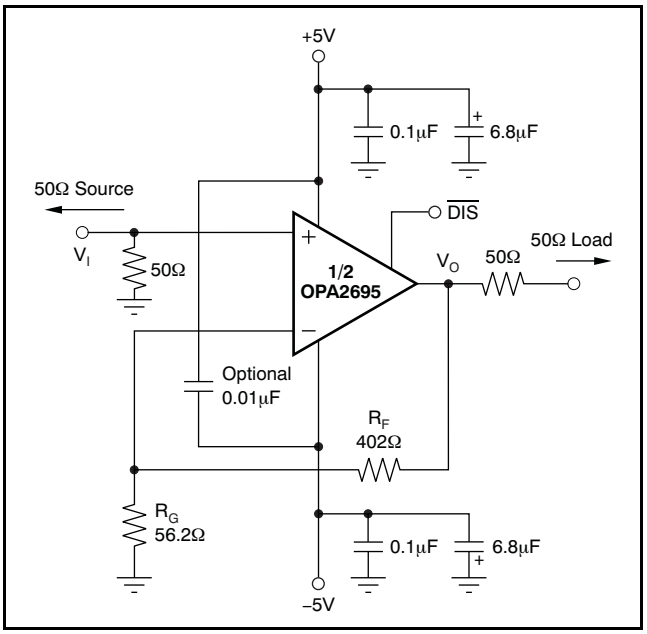


Figure 68. DC-Coupled, G = +8V/V, Bipolar Supply Specifications and Test Circuit

Figure 69 shows the dc-coupled, gain of –8V/V, dual power-supply circuit used as the basis of the Inverting Typical Characteristic curves. Inverting operation offers several performance benefits. Because there is no common-mode signal across the input stage, the slew rate for inverting operation is higher and the distortion performance is slightly improved. An additional input resistor, R_T, is included in Figure 69 to set the input impedance equal to 50Ω. The parallel combination of R_T and R_G set the input impedance. Both the noninverting and inverting applications of Figure 68 and Figure 69 benefit from optimizing the feedback resistor (R_F) value for bandwidth (see the discussion in *Setting Resistor Values to Optimize Bandwidth*). The typical design sequence is to select the R_F value for best bandwidth, set R_G for the gain, then set R_T for the desired input impedance. As the gain increases for the inverting configuration, a point is reached where R_G equals 50Ω, where R_T is removed and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, R_F is simply increased to increase gain. This increase, however, quickly reduces the achievable bandwidth, as shown by the inverting gain of –16V/V frequency response in the Typical Characteristic curves. For gains greater than 10V/V (14dB at the matched load), noninverting operation is recommended to maintain broader bandwidth.

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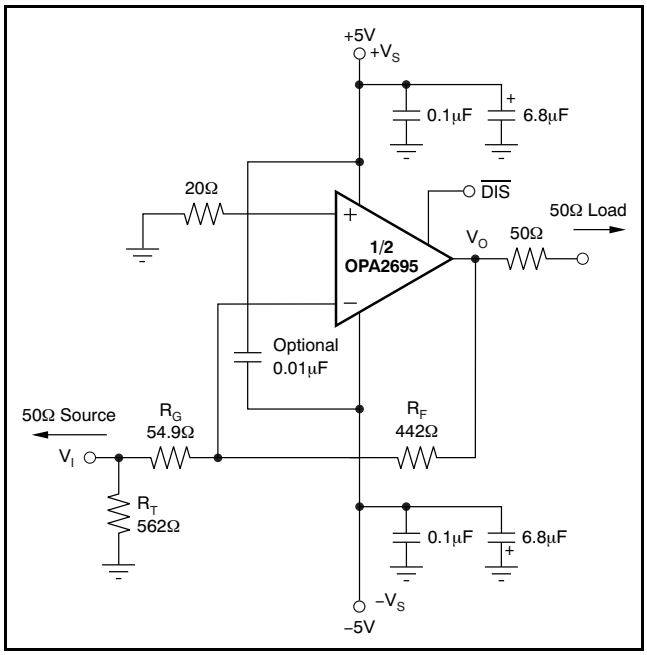


Figure 69. DC-Coupled, G = –8V/V, Bipolar Supply Specifications and Test Circuit

Figure 70 shows the ac-coupled, single +5V supply, gain of +8V/V circuit configuration used as a basis for the +5V only Electrical Characteristics and Typical Characteristics. The key requirement for broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 70 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors) to the noninverting input. The input signal is then ac-coupled into this midpoint voltage bias. The input voltage can swing to within 1.6V of either supply pin, giving a $1.8V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used in Figure 70 is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is ac-coupled, giving the circuit a dc gain of +1. This configuration puts the input dc bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V only, gain of +8 operation (see *Setting Resistor Values to Optimize Bandwidth*). On a single +5V supply, the output voltage can swing to within 1.0V of either supply pin while delivering more than 90mA output current, giving 3V output swing into 100Ω (7dBm maximum at the matched load). The circuit of Figure 70 shows a blocking capacitor driving into a 50Ω output resistor, then into a 50Ω load. Alternatively, the blocking capacitor could be removed with the load tied to a supply midpoint or to ground if the dc current required by this grounded load is acceptable.

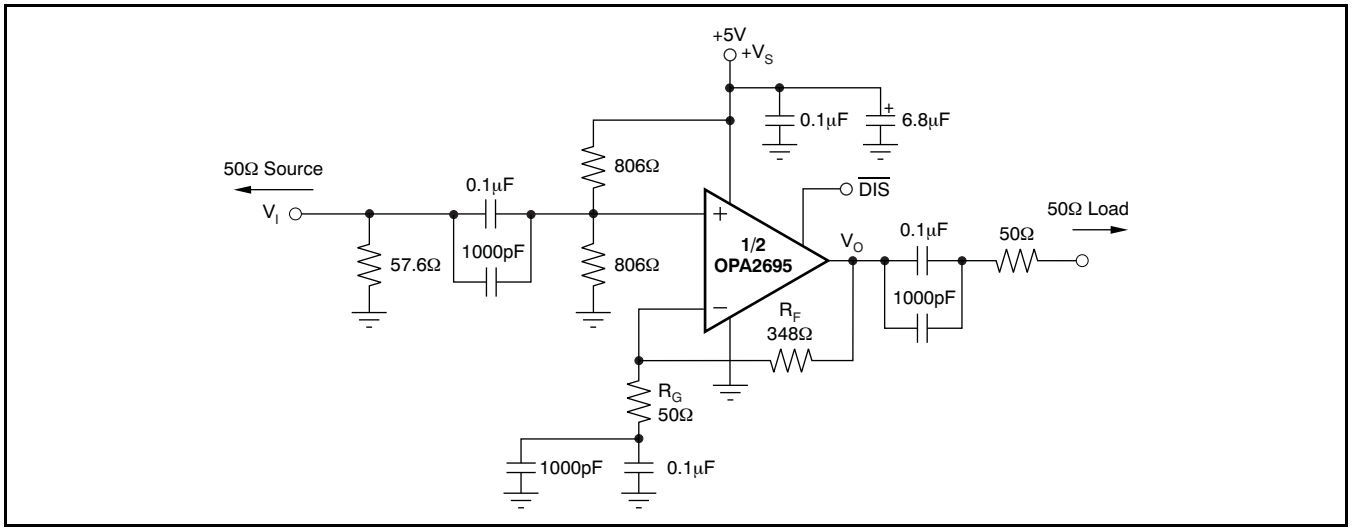


Figure 70. AC-Coupled, G = +8V/V, Single-Supply Specifications and Test Circuit

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Figure 71 shows the ac-coupled, single +5V supply, gain of –8V/V circuit configuration used as a basis for the +5V only Typical Characteristics. In this case, the midpoint dc bias on the noninverting input is also decoupled with an additional 0.1µF decoupling capacitor. This decoupling configuration reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, because R_G is dc blocked by the input capacitor, also appears at the output pin. One advantage to inverting operation is that because there is no signal swing across the input stage, higher slew rates and operation to even lower supply voltages are possible. To retain a $1V_{PP}$ output capability, operation down to a 3V supply is allowed. At a +3V supply, the input common-mode range is 0V. However, for the inverting configuration of a current-feedback amplifier, wideband operation is retained even with the input stage saturated.

The single-supply test circuits of Figure 70 and Figure 71 show +5V operation. These same circuits can be used over a single-supply range of +5V to +12V. Operating on a single +12V supply, with the absolute maximum supply voltage specification of +13V, gives adequate design margin for the typical ±5% supply tolerance.

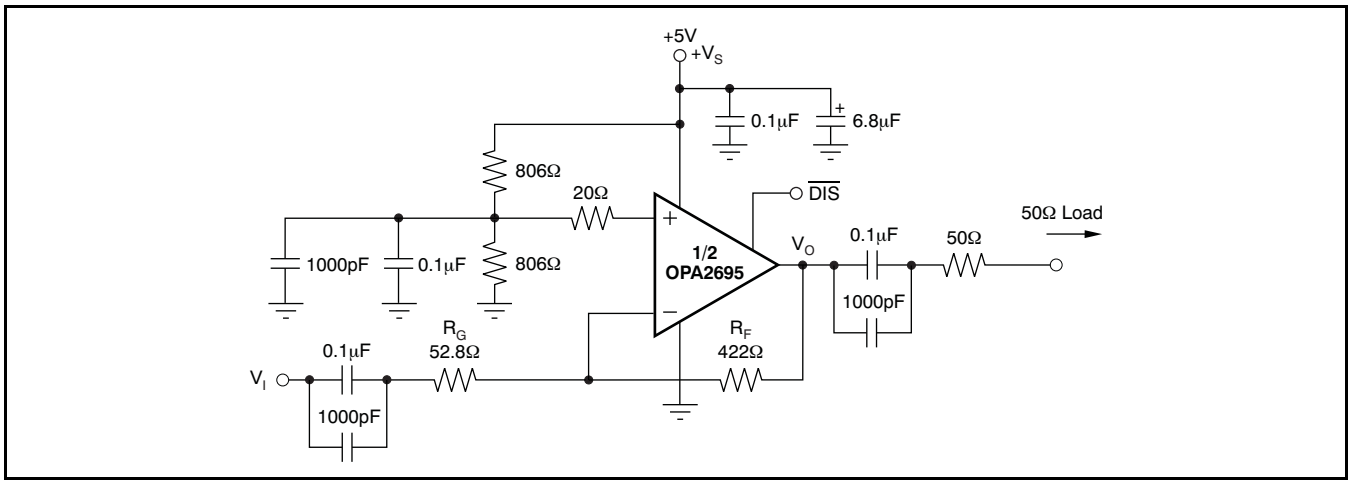


Figure 71. AC-Coupled, G = –8V/V, Single-Supply Specifications and Test Circuit

WIDEBAND VIDEO MULTIPLEXING (QFN-16 Package Only)

One common application for video speed amplifiers that include a disable pin is to wire multiple amplifier outputs together, then select one of several possible video inputs to source onto a single line. This simple *wired-OR video multiplexer* can be easily implemented using the OPA2695IRGT, as Figure 72 shows.

Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this time. The *make-before-break* disable characteristic of the OPA2695 ensures that there is always one amplifier controlling the line when using a wired-OR circuit such as the one presented in Figure 72. Because both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (82.5Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The gain and output matching resistors have been slightly increased to achieve a signal gain of +1V/V at the matched load and provide a 75Ω output impedance to the cable. The video multiplexer connection (as shown in Figure 72) also ensures that the maximum differential voltage across the inputs of the unselected channel does not exceed the rated ±1.2V maximum for standard video signal levels.

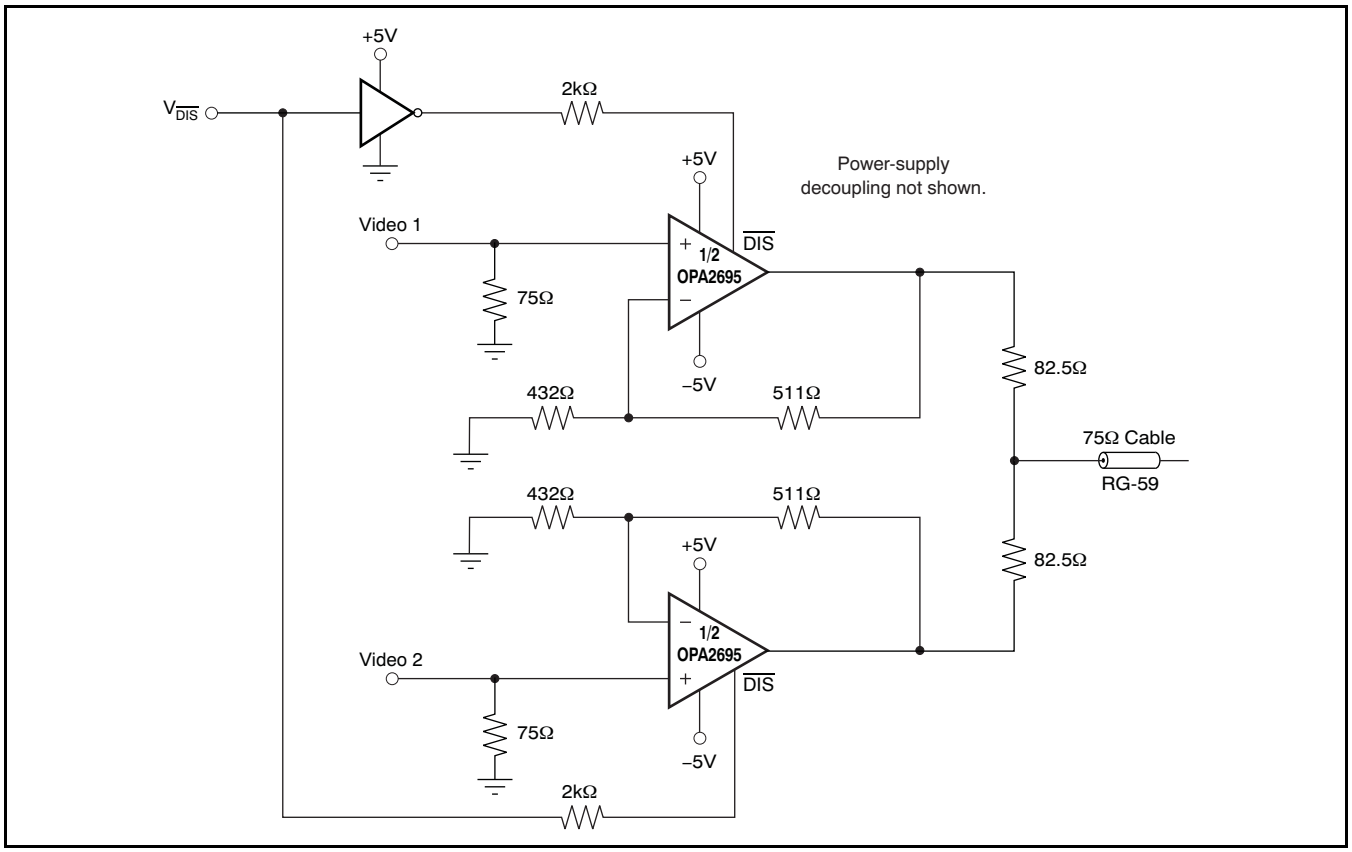


Figure 72. Two-Channel Video Multiplexer

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HIGH-SPEED ACTIVE FILTERS

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as a fixed gain block inside a passive RC circuit network. The relatively constant bandwidth versus gain provides low interaction between the actual filter poles and the required gain for the amplifier. Figure 73 shows a typical single-supply buffered filter application. In this case, one of the OPA2695 channels is used to set up the dc operating point and provide impedance isolation from the signal source into the 2nd-stage filter. That stage is set up to implement a 20MHz, maximally flat Butterworth frequency response and provide an ac gain of +4V/V.

The 51Ω input matching resistor is optional in this case. The input signal is ac-coupled to the 2.5V dc reference voltage developed through the resistor divider from the +5V power supply. This first stage acts as a gain of +1V/V voltage buffer for the signal where the 511Ω feedback resistor is required for stability. This first stage easily drives the low input resistors required at the input of this high-frequency filter. The second stage is set for a dc gain of +1V/V, carrying the 2.5V operating point through to the output pin and an ac gain of +4V/V. The feedback resistor has been adjusted to optimize bandwidth for the amplifier itself. As the single-supply frequency response plots show, the OPA2695 in this configuration gives greater than 400MHz small-signal bandwidth. The capacitor values were chosen to be as low as possible, but still large enough to overcome the effects of the parasitic input capacitance of the amplifier. The resistor values were slightly adjusted to give the desired filter frequency response while accounting for the approximate 1ns propagation delay through each channel of the OPA2695.

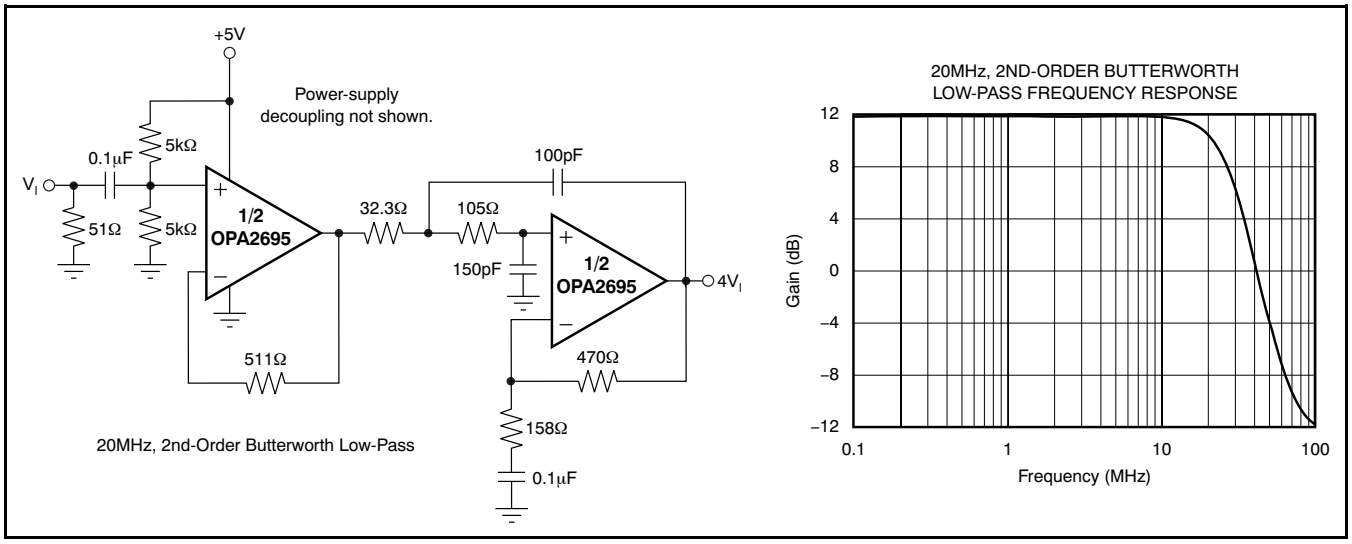


Figure 73. Buffered Single-Supply Active Filter

DIFFERENTIAL I/O APPLICATIONS

The OPA2695 offers very low third-order distortion terms with a dominant second-order distortion for the single amplifier operation. For the lowest distortion, particularly where differential outputs are needed, operating two OPA2695s in a differential I/O design suppresses these even-order terms, delivering extremely low harmonic distortion through high frequencies and powers. Differential outputs are often preferred for high performance ADCs, twisted-pair driving, and mixer interfaces. Two basic approaches to differential I/Os are the noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the two OPA2695s. Each approach has its advantages and disadvantages. Figure 74 shows a basic starting point for noninverting differential I/O applications.

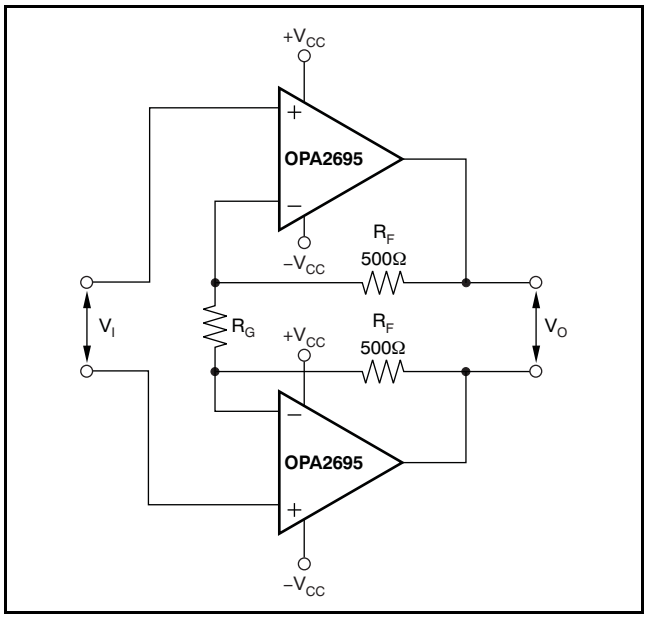


Figure 74. Noninverting Input Differential I/O Amplifier

This approach allows for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 74 is:

$A_D = 1 + 2 \times R_F/R_G$

Since the OPA2695 is a current-feedback amplifier, its bandwidth is principally controlled with the feedback resistor value—Figure 74 shows a typical value of 500Ω. However, the differential gain may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response. It is common for ac-coupled applications to include a blocking capacitor in series with R_G. This reduces the gain to 1 at low frequency, rising to the A_D expression shown above at higher frequencies. The noninverting input approach of Figure 74 can be used for higher gains than the inverting input approach. It does, however, have a reduced full-power bandwidth because of the lower slew rate of the OPA2695 running noninverting versus inverting input mode of operation.

Various combinations of single-supply or ac-coupled gain can also be delivered using the basic circuit of Figure 74. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1, since an equal dc voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output commonmode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also remove the common-mode signal at the secondary of the transformer.

Figure 75 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become part of the input resistance for the source. This provides a better noise performance than the non-inverting configuration, but does limit the flexibility in setting the input impedance separately from the gain.

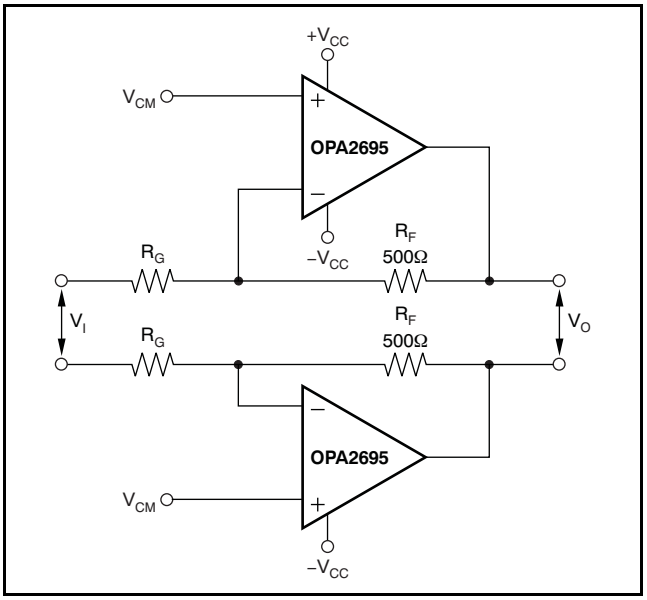


Figure 75. Inverting Input Differential I/O Amplifier

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The two noninverting inputs provide an easy common-mode control input. This is particularly easy if the source is ac-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving particularly easy common-mode control for single-supply operation. The OPA2695 used in this configuration does constrain the feedback to the 500Ω region for best frequency response. With R_F fixed, the input resistors may be adjusted to the desired gain, but also change the input impedance as well. The high-frequency common-mode gain for this circuit from input to output is the same as for the signal gain. Again, if the source might include an undesired common-mode signal, that could be rejected at the input using blocking caps (for low-frequency and dc common-mode) or a transformer coupling. The differential performance plots shown in the Typical Characteristics used the configuration of Figure 75 and an input 1:1 transformer. The differential signal gain in the circuit of Figure 75 is:

$A_D = R_F/R_G$

Using this configuration suppresses the second harmonics, leaving only third harmonic terms as the limit to output SFDR. The much higher slew rate of the inverting configuration also extends the full-power bandwidth and the range of very low intermodulation distortion over the performance bandwidth available from the circuit of Figure 74. The Typical Characteristics show that the circuit of Figure 75 operating at an A_D = 10 can deliver a $16V_{PP}$ signal with over 400MHz –3dB bandwidth. Using Equation 3, this implies a differential output slew of 18000V/µs, or 9000V/µs at each output. This output slew rate is far higher than specified, and probably due to the lighter load used in the differential tests.

$$F_{MAX} = \frac{\text{Slew Rate}}{2\pi V_P\ (0.707)} \quad (3)$$

This inverting input differential configuration is particularly suited to very high SFDR converter interfaces—specifically narrowband IF channels. The Typical Characteristics show the two-tone, third-order intermodulation intercept exceeding 45dBm through 90MHz. Although this data was taken with an 800Ω load, the intercept model appears to work for this circuit, simply treating the power level as if it were into 50Ω. For example, at 70MHz, the differential Typical Characteristic plots show a 48dBm intercept. To predict the two-tone intermodulation SFDR, assuming a –1dB below full-scale envelope to a $2V_{PP}$ maximum differential input converter, the test power level would be 9dBm – 6dBm = 3dBm for each tone. Putting this into the intercept equation, gives:

ΔdBc = 2 × (48 – 3) = 90dBc

The single-tone distortion data shows approximately 72dB SFDR at 70MHz for a $2V_{PP}$ output into this light 800Ω load. A modest post filter after the amplifier can reduce these harmonics (second at 140MHz, third at 210MHz) to the point where the full SFDR to a converter can be in the 85dB range for a 70MHz IF operation.

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DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2695 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2695ID	SO-8	DEM-OPA-SO-2E	SBOU064
OPA2695IRGT	QFN-16	DEM-OPA-QFN-2C	SBOU061

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2695 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This practice is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2695 is available through the TI web site (www.ti.com). This model does a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in the respective small-signal ac performance, nor do they attempt to simulate channel-to-channel coupling.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp such as the OPA2695 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This performance is shown in the Typical Characteristics. The small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor has been changed for each gain setting. The resistor *values* on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements while the *ratios* set the signal gain. Figure 76 shows the analysis circuit for the OPA2695 small-signal frequency response.

The key elements of this current-feedback op amp model are:

$\alpha \rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \rightarrow$ Buffer output impedance

$i_{ERR} \rightarrow$ Feedback error current signal

$Z_{(S)} \rightarrow$ Frequency-dependent, open-loop transimpedance gain from i_{ERR} to V_O

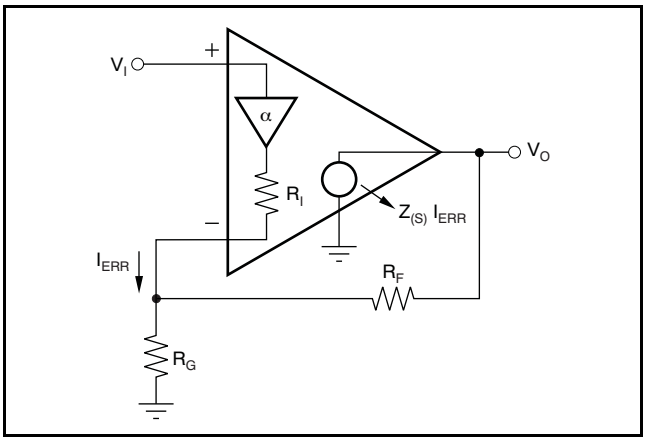


Figure 76. Current-Feedback Transfer Function Analysis Circuit

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It also, however, sets the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$, the CMRR = $-20 \times \log (1 - \alpha)$.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. For the OPA2695, it is typically about 29Ω for ±5V operation and 32Ω for single +5V operation.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this current on to the output through an internal frequency-dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This response is analogous to the open-loop voltage gain curve for a voltage-feedback op amp.

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Developing the transfer function for the circuit of Figure 79 gives Equation 5:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F+R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F+R_I\times NG}{Z_{(S)}}} \quad (5)$$

Where: NC = 1 + R_F/R_G = Noise Gain

This formula is written in a loop gain analysis format, where the errors arising from a non-infinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation 5 would reduce to 1, and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 5 determines the frequency response and also gives an expression for the loop gain:

$$\frac{Z_{(S)}}{R_F + R_I \times NG} = \text{Loop Gain} \quad (6)$$

If 20 × log (R_F + NG × R_I) were superimposed on the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation 6, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop frequency response given by Equation 5 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 6 may be controlled separately from the desired signal gain (or NG).

The OPA2695 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 8 on ±5V supplies. Evaluating the denominator of Equation 5 (the feedback transimpedance) gives an optimal target of 663Ω. As the signal gain changes, the contribution of the NG × R_I term in the feedback transimpedance changes, but the total can be held constant by adjusting R_F. Equation 7 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 663\Omega - NG \times R_I \quad (7)$$

As the desired signal gain increases, this equation eventually predicts a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 10Ω. Lower values load both the buffer stage at the input and the output stage if R_F goes too low, actually decreasing the bandwidth. Figure 77 shows the recommended R_F versus NG for both ±5V and a single +5V operation. The optimum target feedback impedance for +5V operation used in Equation 5 is 604Ω, while the typical buffer output impedance is 32Ω. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical Characteristic curves. In some cases, the values used differ slightly from that shown here, in that the values used in the Typical Characteristics are also correcting for board parasitics not considered in the simplified analysis leading to Equation 7. The values shown in Figure 77 give a good starting point for designs where bandwidth optimization is desired and a flat frequency response is needed.

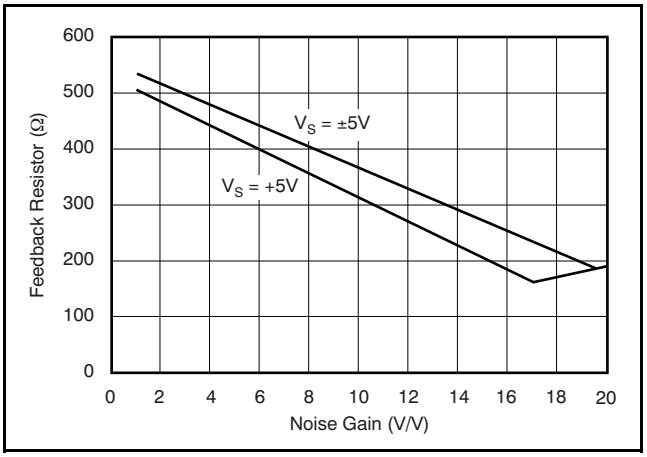


Figure 77. Recommended Feedback Resistor versus Noise Gain

The total impedance presented to the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (denominator of Equation 6) and decreases the bandwidth. The internal buffer output impedance for the OPA2695 is slightly influenced by the source impedance looking out of the noninverting input terminal. High source resistors have the effect of increasing R_I and decreasing the bandwidth. For those single-supply applications that develop a midpoint bias at the noninverting input through high-valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, noninverting input noise current shunting, and minimizing the high-frequency value for R_I in Figure 76.

OUTPUT CURRENT AND VOLTAGE

The OPA2695 provides output voltage and current capabilities that are consistent with driving doubly-terminated 50Ω lines. For a 100Ω load at a gain of +8V/V (see Figure 68), the total load is the parallel combination of the 100Ω load and the 458Ω

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total feedback network impedance. This 82Ω load requires no more than 45mA output current to support the ±3.7V minimum output voltage swing specified for 100Ω loads. This minimal requirement is well below the minimum ±90mA specifications.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or *V-I*, product that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 21) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants provide a more detailed view of the OPA2695 output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current overtemperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the specification tables. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current always are greater than that shown in the over-temperature specifications, because the output stage junction temperatures are greater than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output shortcircuit protection is provided. This lack of protection is normally a problem, because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin does, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. Under heavy output loads, this additional resistor reduces the available output voltage swing. A 5Ω series resistor in each power-supply lead limits the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. Always place the 0.1µF power-supply decoupling capacitors directly on the supply pins after these supply current-limiting resistors.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve analog-to-digital linearity. A high-speed, high open-loop gain amplifier such as the OPA2695 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This isolation resistor does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2695. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA2695 output pin (see the *Board Layout Guidelines* section).

DISTORTION PERFORMANCE

The OPA2695 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, the OPA2695 holds much lower distortion at higher frequencies (> 20MHz). Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network. In the noninverting configuration (Figure 68), this value is the sum of $R_F + R_G$, while in the inverting configuration, it is only R_F. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

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In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd harmonic increasing at a little less than the expected 2x rate, while the 3rd harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd harmonic decreases less than the expected 6dB, while the difference between it and the 3rd decreases by less than the expected 12dB.

The OPA2695 has extremely low third-order harmonic distortion. This also gives a high two-tone, third-order intermodulation intercept, as shown in the Typical Characteristics. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to R_F MMIC devices and is shown for both gains of ±8V/V. There is a slight improvement in third-order intercept by operating the OPA2695 in the inverting mode. The output matching resistor attenuates the voltage swing from the output pin to the load by 6dB. If the OPA2695 drives directly into the input of a high impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept increases by a minimum of 6dBm.

The third-order intercept is used to predict the intermodulation products for two closely-spaced frequencies. If the two test frequencies, F_1 and F_2, are specified in terms of average and delta frequency, $F_O = (F_1 + F_2)/2$ and $\Delta F = |F_2 - F_1|/2$, the two third-order, close-in spurious tones appear at $F_O \pm 3 \times \Delta F$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \times (OP_3 - P_O)$, where OP_3 is the intercept taken from the Typical Characteristic curves (see Figure 14, Figure 44, Figure 56, and Figure 60) and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For example, at 50MHz, gain of –8V/V, the OPA2695 has an intercept of 32dBm at a matched 50Ω load. If the full envelope of the two frequencies must be $2V_{PP}$, each tone must be 4dBm. The third-order intermodulation spurious tones are then 2 × (32 – 4) = 56dBc below the test-tone power level (–52dBm). If this same $2V_{PP}$ two-tone envelope were delivered directly into the input of an ADC without the matching loss or the loading of the 50Ω network, the intercept would increase to at least 38dBm. With the same signal and gain conditions, but now driving directly into a light load, the third-order spurious tones are then at least 2 × (38 – 4) = 68dBc below the 4dBm test-tone power levels centered on 50MHz. Tests have shown that, in reality, the third-order spurious levels are much lower as a result of the lighter loading presented by most ADCs.

NOISE PERFORMANCE

The OPA2695 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (22pA/√Hz) is lower than most other current-feedback op amps while the input voltage noise (1.8nV/√Hz) is lower than any unity-gain stable, wideband, voltage-feedback op amp. This low-input voltage noise was achieved at the price of a higher noninverting input current noise (18pA/√Hz). As long as the ac source impedance looking out of the noninverting node is less than 50Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 78 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

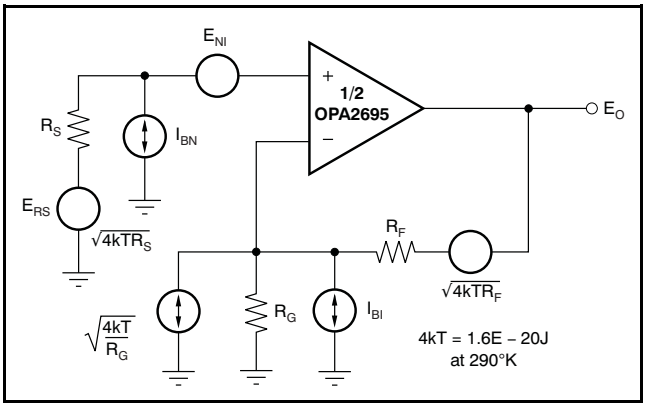


Figure 78. Op Amp Noise Analysis Model

The total output spot-noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 8 shows the general form for the output noise voltage using the terms shown in Figure 78.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)G_N^2 + (I_{BI}R_F)^2 + 4kTR_FG_N} \quad (8)$$

Dividing this expression by the noise gain ($NG = (1 + R_F/R_G)$) gives the equivalent input-referred spot-noise voltage at the noninverting input as shown in Equation 9:

$$E_O = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (9)$$

Evaluating these two equations for the OPA2695 circuit and component values shown in Figure 68 gives a total output spot-noise voltage of 18.7nV/√Hz and a total equivalent input spot-noise voltage of 2.3nV/√Hz. This total input-referred spot-noise

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voltage is higher than the 1.8nV/√Hz specification for the op amp voltage noise alone. This increased value reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input-referred voltage noise given by Equation 9 approaches the 1.8nV/√Hz of the op amp itself. For example, going to a gain of +20 (using R_F = 200Ω) gives a total input-referred noise of 2.0nV/√Hz.

For a more complete discussion of op amp noise calculation, see TI Application Note, SBOA066, *Noise Analysis for High Speed Op Amps*, available through the TI web site at www.ti.com.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA2695 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate dc accuracy. The typical specifications show an input offset voltage comparable to high-speed voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. Although bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce the respective error contribution to the output is ineffective. Evaluating the configuration of Figure 80, using a worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$\pm(NG \times V_{OS}) + (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$$

where NG = noninverting signal gain.

$$= \pm(8 \times 3.5mV) \pm (30\mu A \times 25\Omega \times 8) \pm (402\Omega \times 60\mu A)$$

$$= \pm 28mV \pm 8mV \pm 24mV$$

$$= \pm 60mV$$

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most simple adjustment techniques do not correct for temperature drift.

POWER SHUTDOWN OPERATION (QFN-16 Package Only)

The OPA2695IRGT provides an optional power shutdown feature that can be used to reduce system power. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA2695IRGT operates normally. This shutdown is intended only as a power-saving feature. Forward path isolation is very good for small signals. Large signal isolation is not ensured. Using this feature to multiplex two or more outputs together is not recommended. Large signals applied to the shutdown output stages can turn on parasitic devices, degrading signal linearity for the desired channel.

Turn-on time is very quick from the shutdown condition, typically less than 60ns. Turn-off time strongly depends on the external circuit configuration, but is typically 200ns for the circuit of Figure 68.

To shut down, the control pin must be asserted low. This logic control is referenced to the positive supply, as shown in the simplified circuit of Figure 79.

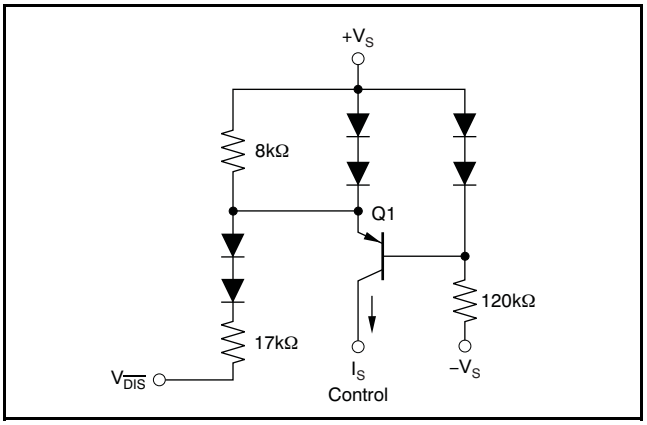


Figure 79. Simplified Shutdown Circuit

In normal operation, base current to Q1 is provided through the 120kΩ resistor, while the emitter current through the 8kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 8kΩ resistor, eventually turning on these two diodes (≈ 180μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This limitation shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 79.

When disabled, the output and input nodes go to a high-impedance state. If the OPA2695IRGT is operating in a gain of +1V/V, this configuration shows a very high impedance (3pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1V/V, the total feedback network resistance (R_F + R_G) appears as the impedance looking back into the output, but the circuit continues to show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output are connected through the feedback network resistance (R_F + R_G), giving relatively poor input to output isolation.

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THERMAL ANALYSIS

The OPA2695 does not require external heatsinking for most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load. However, for a grounded resistive load, P_{DL} would be at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA2695ID (SO package) in the circuit of Figure 68 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$$P_D = 10V \times 28.6mA + 5^2/\left(4 \times (100\Omega \parallel 458\Omega)\right) = 362mW \quad (10)$$

$$\text{Maximum } T_J = +85°C + (0.36W \times 100°C/W) = 121°C \quad (11)$$

A similar calculation for the device in a QFN package (OPA2695RGT) with a PowerPAD™ thermal connection results in an estimated junction temperature T_J = +105°C. These maximum operating junction temperatures are well below most system level targets. Most applications are lower because an absolute worst-case output stage power was assumed in this calculation.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA2695 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25", or 0.635cm) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply-decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserves the high-frequency performance of the OPA2695. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-sided component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value, as described previously. Increasing its value reduces the bandwidth, while decreasing it gives a more peaked frequency response. The 402Ω feedback resistor (used in the Typical Characteristics at a gain of +8 on ±5V supplies) is a good starting point for design. Note that a 523Ω feedback resistor, rather than a direct short, is required for the unity gain follower application. A current-feedback op amp requires a feedback resistor—even in the unity gain follower configuration—to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively

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wide traces (50mils to 100mils or 1.27mm to 2.54mm, respectively) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (Figure 17, Figure 37, Figure 61, and Figure 51). Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2695 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is usually not necessary on board. In fact, a higher impedance environment does improve distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2695 is used. A terminating shunt resistor at the input of the destination device is used as well. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2695 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S versus capacitive load. If the input impedance of the destination device is low, there will be some signal attenuation because of the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part such as the OPA2695 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2695 directly onto the board.

INPUT AND ESD PROTECTION

The OPA2695 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum ±6.5V supply is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 80.

These diodes also provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2695), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

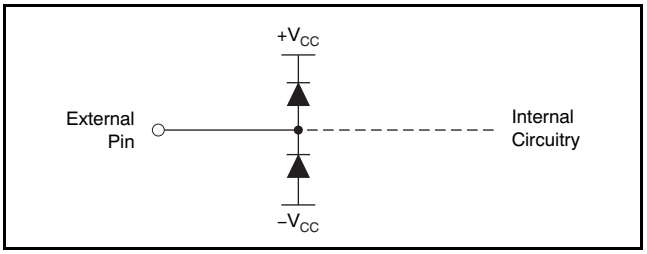


Figure 80. Internal ESD Protection

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Revision History

Changes from Original (April 2008) to Revision A **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2
- Changed ordering number for OPA2695IRGT in Table 1 26

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2695ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP2695	Samples
OPA2695IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP2695	Samples
OPA2695IRGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2695	Samples
OPA2695IRGTRG4	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2695	Samples
OPA2695IRGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2695	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

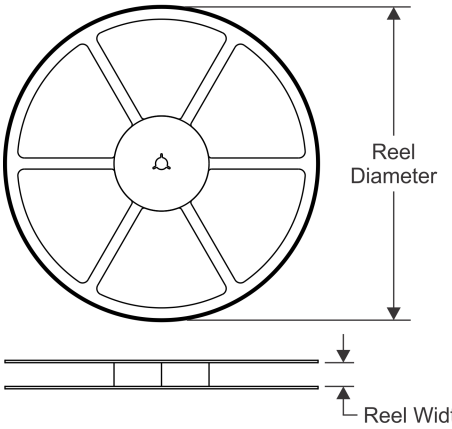
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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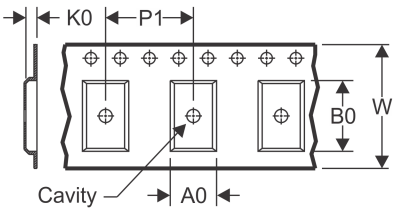
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

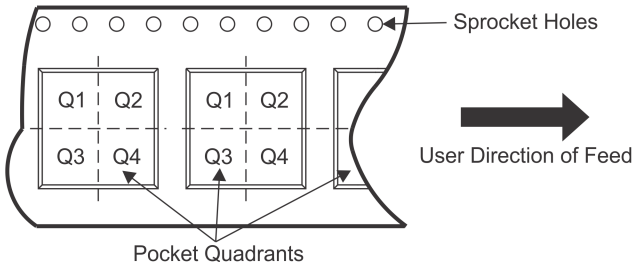


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

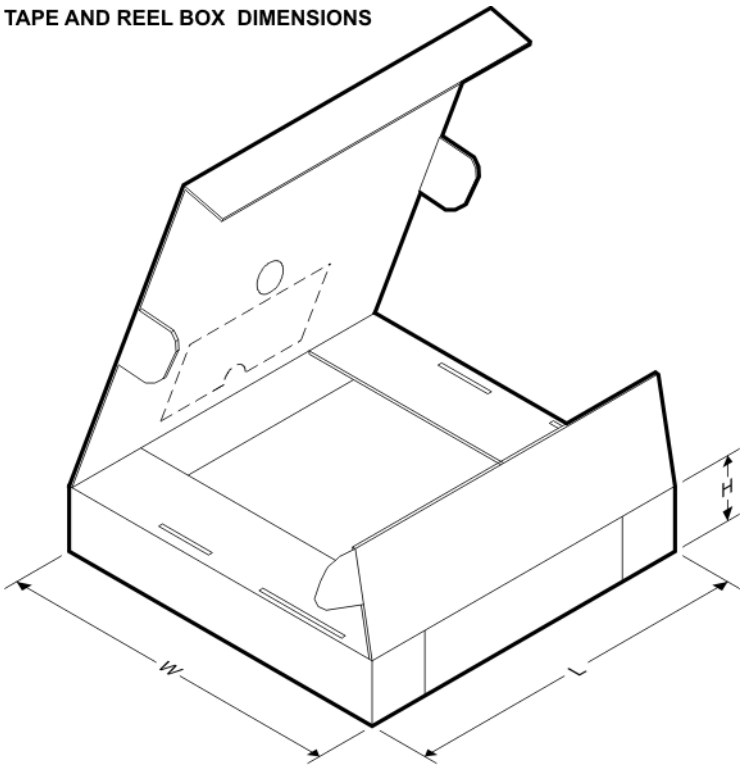
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2695IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2695IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2695IRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

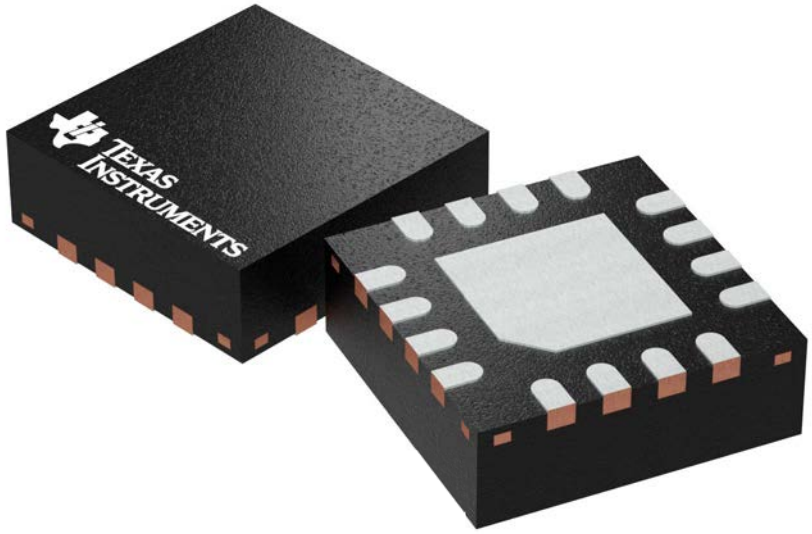


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2695IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2695IRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
OPA2695IRGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



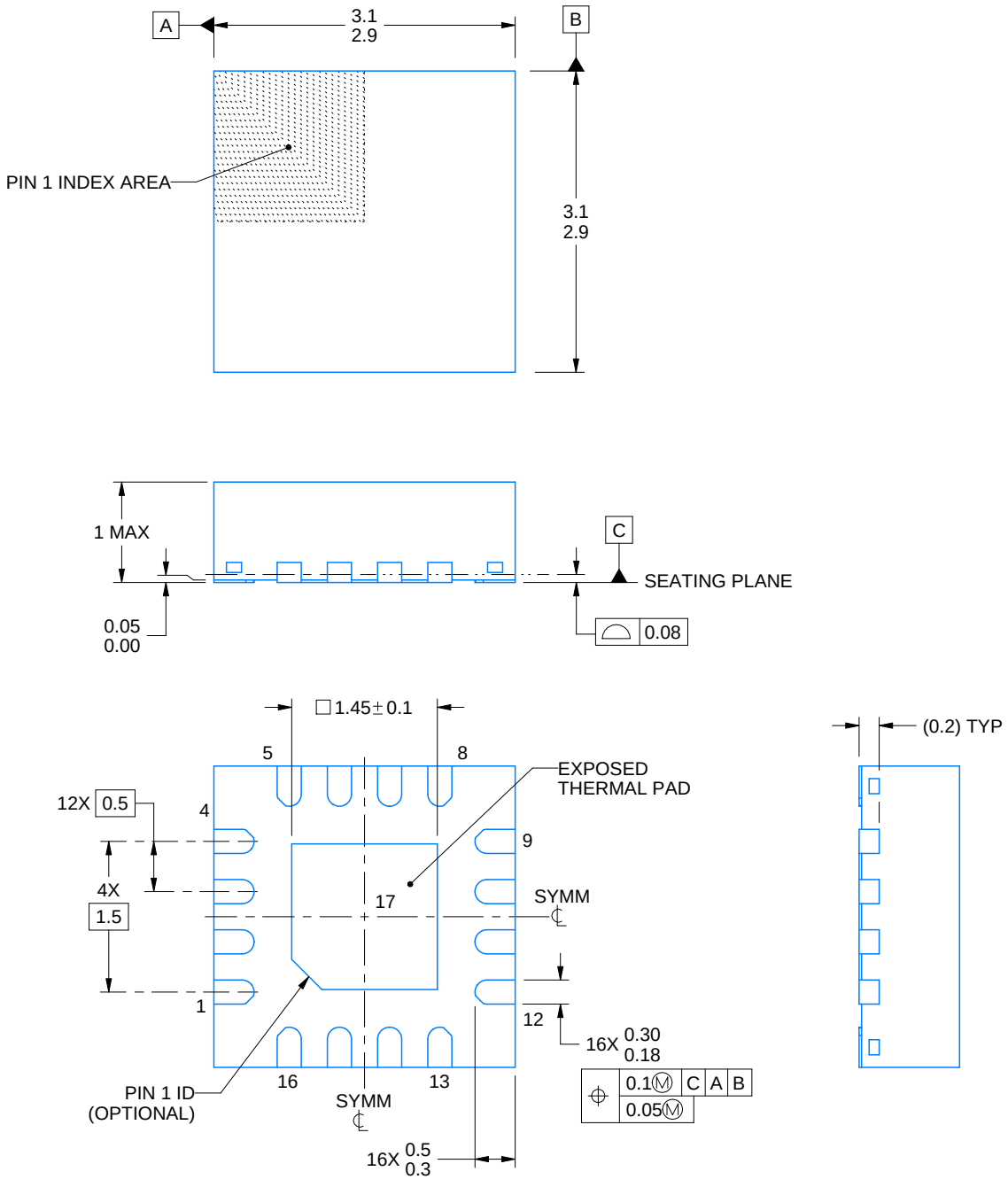
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

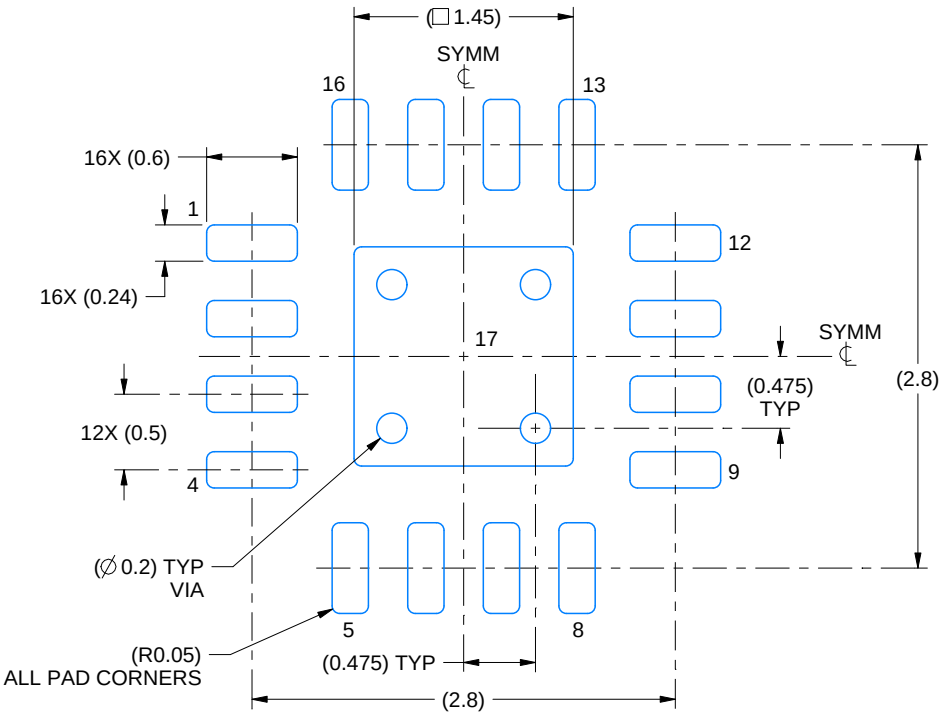
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

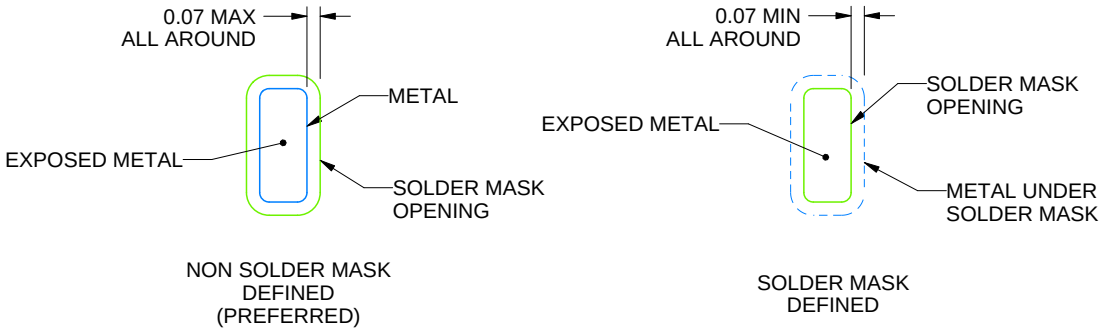


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

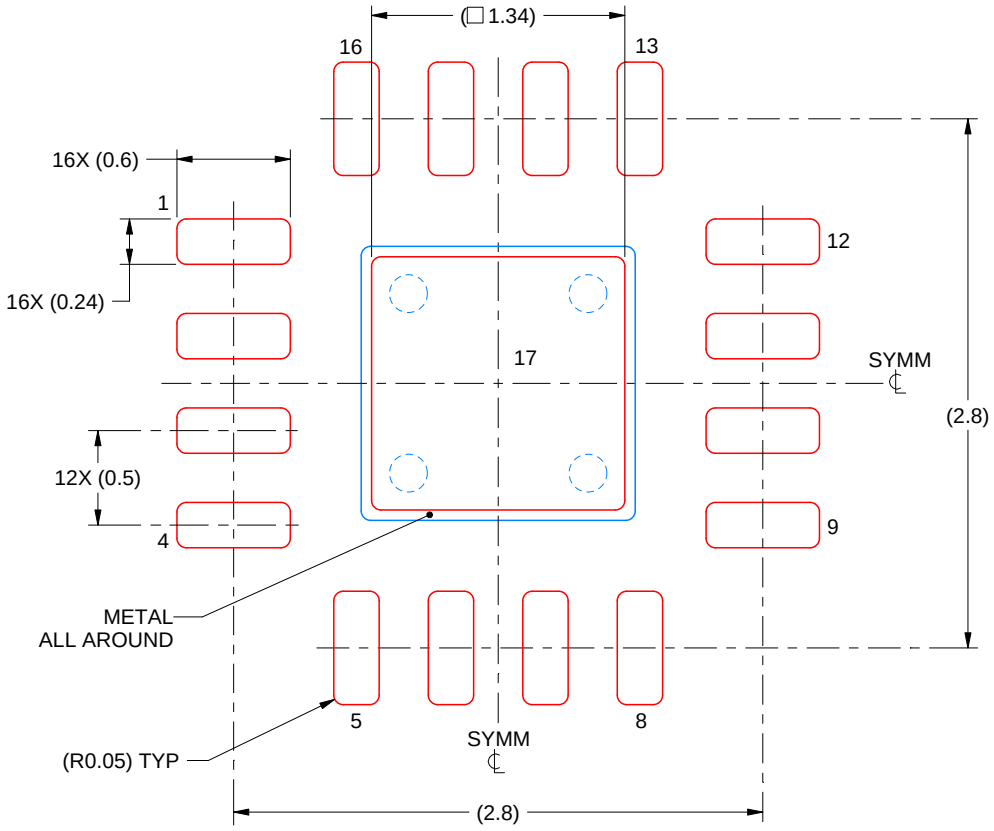


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



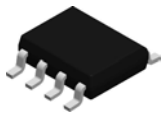
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

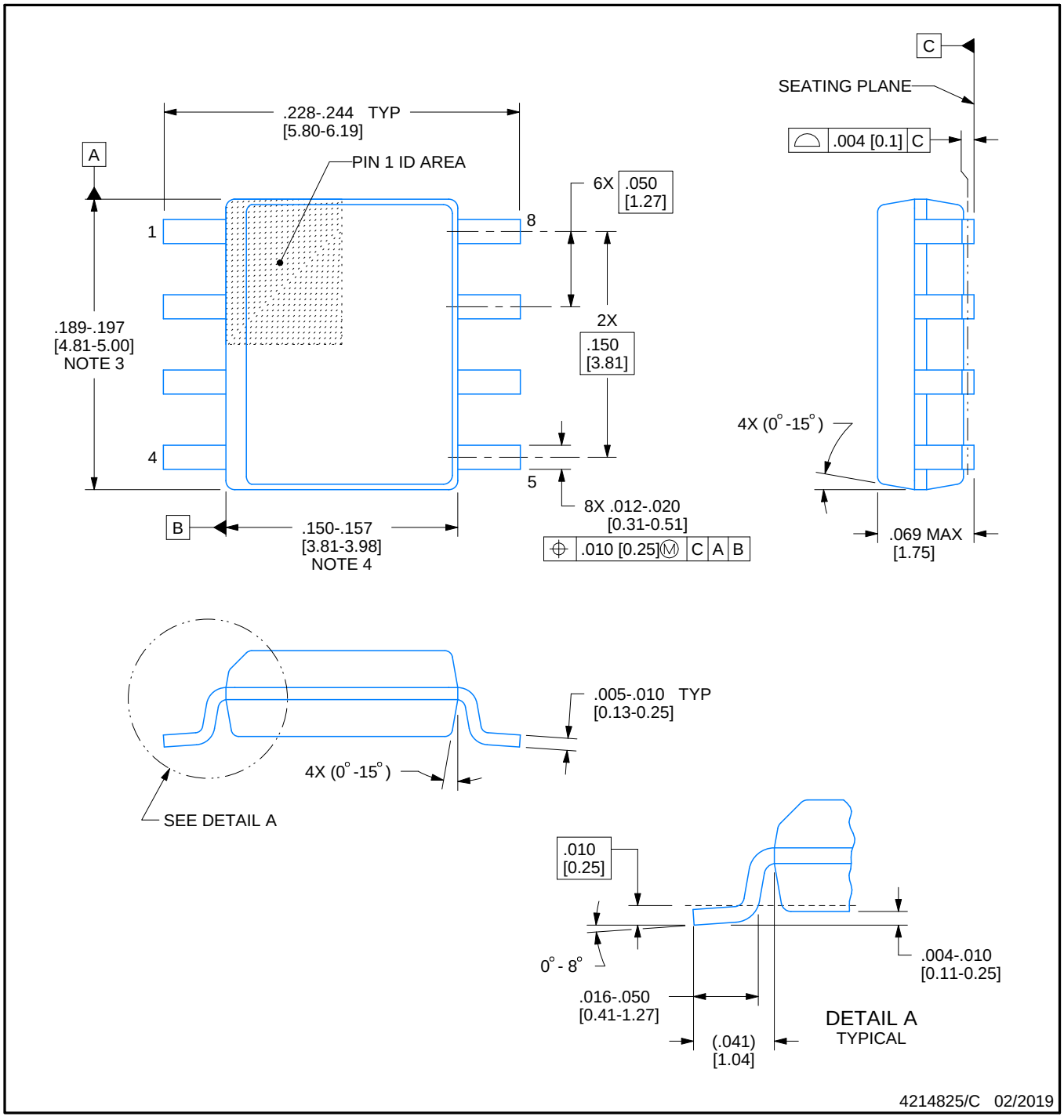


PACKAGE OUTLINE

D0008A

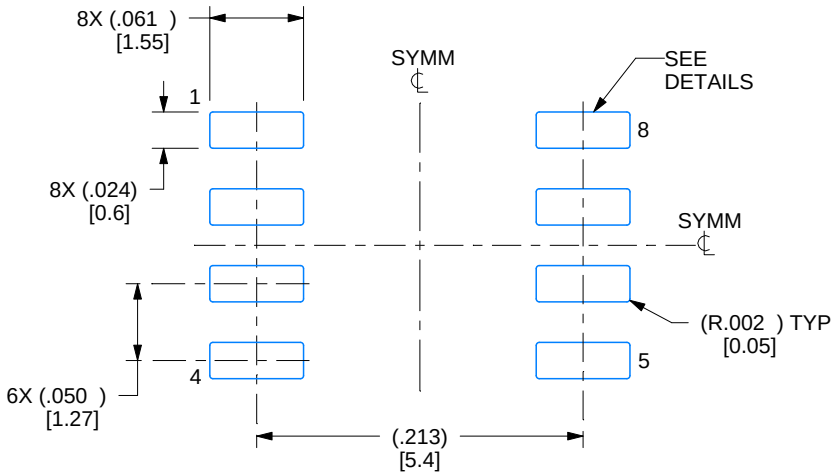
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

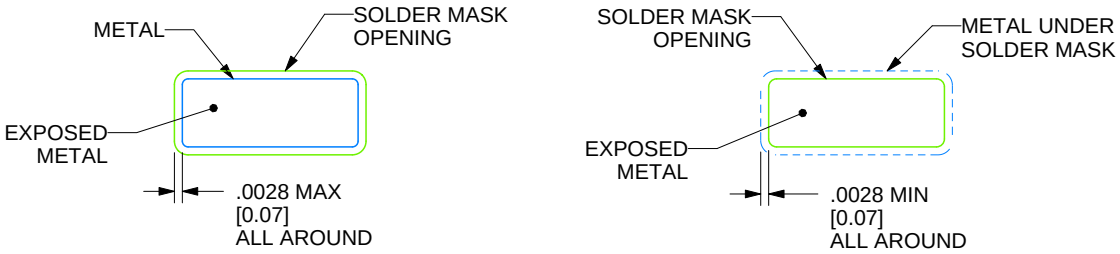


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

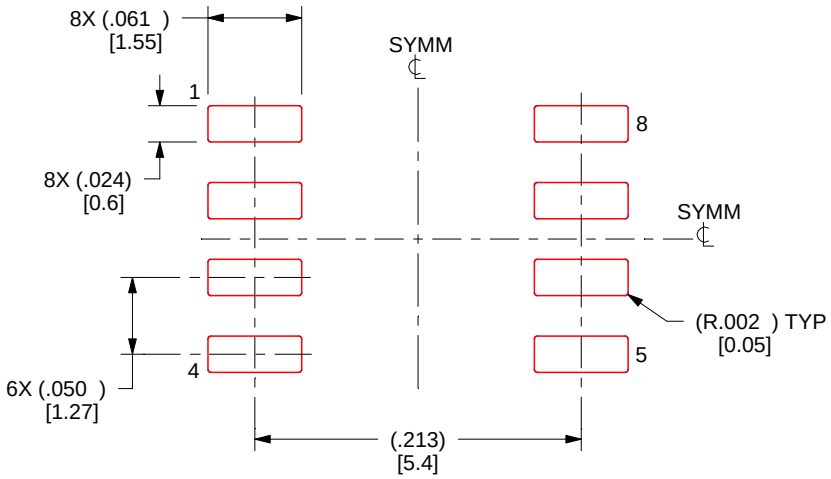
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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