Triple, Ultra-Wideband, Current-Feedback OPERATIONAL AMPLIFIER with Disable

FEATURES

- 900MHz BANDWIDTH, GAIN = +2V/V
- 450MHz BANDWIDTH, GAIN = +8V/V
- WIDE OUTPUT VOLTAGE SWING: ±4V
- ULTRA-HIGH SLEW RATE: 4300V/µs
- 3RD-ORDER INTERCEPT: > 35dBm (f < 40MHz)
- LOW 1.8nV/√Hz VOLTAGE NOISE
- ±120mA OUTPUT CURRENT DRIVE
- 12.9mA/Ch SUPPLY CURRENT (±5V)
- LOW 0.1mA/Ch DISABLE CURRENT
- 3.5V to 12V SINGLE-SUPPLY OPERATION
- ±1.75V to ±6V SPLIT-SUPPLY OPERATION

APPLICATIONS

- BROADBAND VIDEO LINE DRIVERS
- VERY WIDEBAND ADC DRIVERS
- HIGH BANDWIDTH INSTRUMENTATION AMPLIFIERS
- HIGH-SPEED IMAGING
- ACTIVE FILTERS
- ARB WAVEFORM OUTPUT DRIVERS

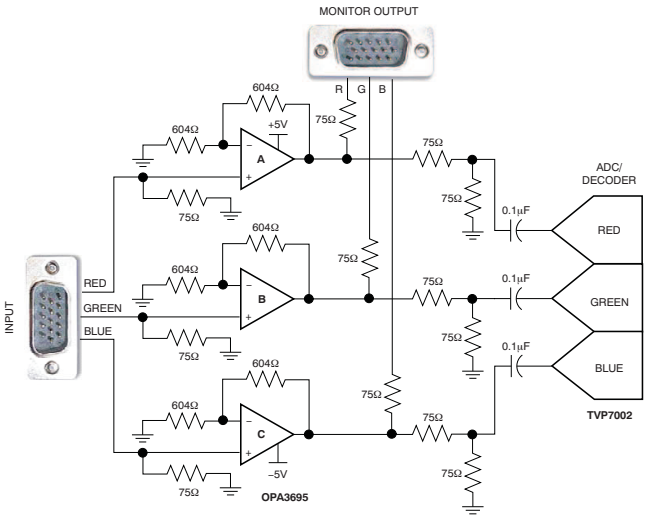


Figure 1. Typical RGB Input/Output Buffer Application

DESCRIPTION

The OPA3695 is a triple, very high bandwidth, current-feedback op amp that combines an exceptional 4300V/µs slew rate and a very high 900MHz bandwidth (G = +2V/V) to provide an amplifier that is ideal for the most demanding video applications. The device versatility is enhanced with a low 1.8nV/√Hz input voltage noise and an output stage that can swing within 1V from the supply rail to deliver a high dynamic range signal, making it well-suited for analog-to-digital converter (ADC) front-ends or digital-to-analog converter (DAC) output buffering. Optimized for high gain operation, the OPA3695 is also well-suited for buffering surface acoustic wave (SAW) filters in an intermediate frequency (IF) system.

The low 12.9mA/channel supply current is precisely trimmed at +25°C. This trim, along with a low temperature drift, gives low system power over temperature. System power may be further reduced using the Disable control pin. Leaving this pin open, or holding it high, gives normal operation. If pulled low, the OPA3695 supply current drops to 100µA/channel. This power-saving feature, along with exceptional single +5V operation, makes the OPA3695 a good fit for low-power applications that require very high performance. The OPA3695 is available in an SSOP-16 package.

OPA3695 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES
OPA695	OPA2695	OPA3695
OPA691	OPA2691	OPA3691
OPA692	THS3202	OPA3692
OPA693	—	OPA3693
OPA694	OPA2694	—

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3695	SSOP-16	DBQ	–40°C to +85°C	OPA3695	OPA3695IDBQ	Rails, 75
					OPA3695IDBQR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

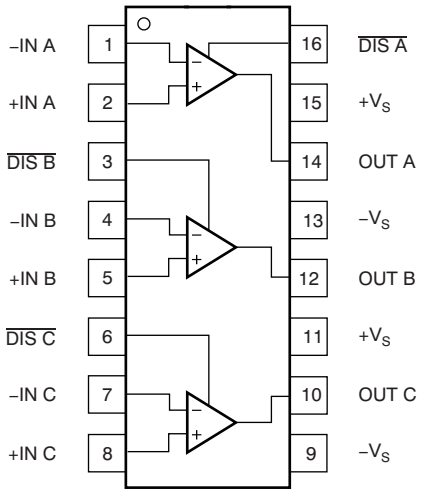
Over operating free-air temperature range (unless otherwise noted).

		OPA3695	UNIT
Power supply		±6.5	V_{DC}
Internal power dissipation		See Thermal Analysis	
Differential input voltage		±1.2	V
Input common-mode voltage range		$\pm V_S$	
Storage temperature range: DBQ		–65 to +125	°C
Lead temperature (soldering, 10s)		+300	°C
Junction temperature (T_J)		+125	°C
ESD rating	Human body model (HBM)	1500	V
	Charge device model (CDM)	1000	V
	Machine model (MM)	100	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these and any other conditions beyond those specified is not supported.

PARAMETER INFORMATION

SSOP-16
(TOP VIEW)



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω, and G = +8, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3695						TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 1)								
Small-signal bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 909Ω	1000				MHz	typ	C
	G = +2, R_F = 604Ω	900				MHz	typ	C
	G = +8, R_F = 402Ω	450	400			MHz	min	B
	G = +16, R_F = 249Ω	340				MHz	typ	C
Bandwidth for 0.2dB gain flatness	G = +2, V_O = 0.5V_{PP}, R_F = 604Ω	320				MHz	min	B
Peaking at a gain of +1	R_F = 523Ω, V_O = 0.5V_{PP}	4.6	5.4			dB	max	B
Large-signal bandwidth	G = +2, V_O = 2V_{PP}	600				MHz	typ	C
	G = +8, V_O = 4V_{PP}	450				MHz	typ	C
Slew rate	G = +2, V_O = 2V step	2400				V/µs	typ	C
	G = –8, V_O = 4V step	4300	3700			V/µs	min	B
	G = +8, V_O = 4V step	2900	2600			V/µs	min	B
Rise-and-fall time	G = +2, V_O = 4V step	1.0				ns	typ	C
	G = +8, V_O = 0.5V step	0.8				ns	typ	C
	G = +8, V_O = 4V step	1.0				ns	typ	C
Settling time to 0.02%	G = +8, V_O = 2V step	16				ns	typ	C
Settling time to 0.1%	G = +8, V_O = 2V step	10				ns	typ	C
Harmonic distortion	G = +8, f = 10MHz, V_O = 2V_{PP}							
2nd harmonic	R_L = 100Ω	–65	–62			dBc	max	B
	R_L ≥ 500Ω	–78	–76			dBc	max	B
3rd harmonic	R_L = 100Ω	–86	–84			dBc	max	B
	R_L ≥ 500Ω	–86	–82			dBc	max	B
2nd harmonic	G = +2, f = 10MHz, R_L = 100Ω	–74				dBc	typ	C
3rd harmonic	G = +2, f = 10MHz, R_L = 100Ω	–74				dBc	typ	C
Input voltage noise	f > 1MHz	1.8	2			nV/√Hz	max	B
Noninverting input current noise	f > 1MHz	18	19			pA/√Hz	max	B
Inverting input current noise	f > 1MHz	22	24			pA/√Hz	max	B
Differential gain	G = +2, NTSC, V_O = 1.4V_{PP}, R_L = 150Ω	0.04				%	typ	C
Differential phase	G = +2, NTSC, V_O = 1.4V_{PP}, R_L = 150Ω	0.007				degrees	typ	C
Crosstalk	All hostile, G = +8, f = 10MHz, V_O = 2V_{PP}	–55				dB	typ	C
DC PERFORMANCE(4)								
Open-loop transimpedance gain (Z_{OL})	V_O = 0V, R_L = 100Ω	85	**45**	43	41	kΩ	min	A
Input offset voltage	V_{CM} = 0V	±0.3	**±3.5**	±4.0	±4.5	mV	max	A
Average offset voltage drift	V_{CM} = 0V			±10	±15	µV/°C	max	B
Noninverting input bias current	V_{CM} = 0V	+13	**±30**	±37	±41	µA	max	A
Average noninverting input bias current drift	V_{CM} = 0V			150	180	nA/°C	max	B
Inverting input bias current	V_{CM} = 0V	±20	**±60**	±66	±70	µA	max	A
Average inverting input bias current drift	V_{CM} = 0V			±120	±160	nA/°C	max	B
INPUT								
Common-mode input voltage range (CMIR)(5)		±3.3	**±3.1**	±3.0	±3.0	V	min	A
Common-mode rejection ratio (CMRR)	V_{CM} = 0V	56	**51**	50	50	dB	min	A
Noninverting input impedance		280 || 1.2				kΩ || pF	typ	C
Inverting input resistance (R_I)	Open-loop	33				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +48°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω, and G = +8, unless otherwise noted.

		OPA3695						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
OUTPUT								
Voltage output swing	No load	±4.0	**±3.9**	±3.8	±3.8	V	min	A
	100Ω load	±3.9	**±3.7**	±3.7	±3.6	V	min	A
Current output, sourcing	V_O = 0V	+120	**+90**	+80	+70	mA	min	A
Current output, sinking	V_O = 0V	–120	**–90**	–80	–70	mA	min	A
Closed-loop output impedance	G = +2, f = 10MHz	0.3				Ω	typ	C
DISABLE (Disabled LOW)								
Power-down supply current (+V_S)	Per channel, $V_{\overline{DIS}}$ = 0V	–100	**–170**	–187	–194	µA	max	A
Disable time	V_{IN} = ±0.25V_{DC}	1				µs	typ	C
Enable time	V_{IN} = ±0.25V_{DC}	25				ns	typ	C
Off isolation	G = +8, 10MHz	77				dB	typ	C
Output capacitance in disable		4				pF	typ	C
Turn-on glitch	G = +2, R_L = 150Ω, V_{IN} = 0V	±100				mV	typ	C
Turn-off glitch	G = +2, R_L = 150Ω, V_{IN} = 0V	±20				mV	typ	C
Enable voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control pin input bias current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V	75	**130**	143	150	µA	max	A
POWER SUPPLY								
Specified operating voltage		±5				V	typ	C
Maximum operating voltage range			**±6**			V	max	A
Minimum operating voltage range			**±1.75**	±1.8	±1.9	V	min	B
Maximum quiescent current	Per channel, V_S = ±5V	12.9	**13.4**	13.8	14.2	mA	max	A
Minimum quiescent current	Per channel, V_S = ±5V	12.9	**12.1**	11.4	10.6	mA	min	A
Power-supply rejection ratio (–PSRR)	Input-referred	55	**51**	48	48	dB	min	A
TEMPERATURE RANGE								
Specification: IDBQ		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
DBQ SSOP-16		80				°C/W	typ	C

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ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At R_F = 348Ω, R_L = 100Ω to 2.5V, and G = +8, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3695 TYP +25°C	OPA3695 MIN/MAX OVER TEMPERATURE +25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/MAX	TEST LEVEL(1)
AC PERFORMANCE (see Figure 3)								
Small-signal bandwidth (V_O = 0.5V_{PP})	G = +1, R_F = 750Ω	850				MHz	typ	C
	G = +2, R_F = 487Ω	725				MHz	typ	C
	G = +8, R_F = 348Ω	395	380			MHz	typ	B
	G = +16, R_F = 162Ω	275				MHz	typ	C
Bandwidth for 0.2dB gain flatness	G = +2, V_O < 0.5V_{PP}, R_F = 487Ω	230	180			MHz	min	B
Peaking at a gain of +1	R_F = 511Ω, V_O < 0.5V_{PP}	1.0	2.0			dB	max	B
Large-signal bandwidth	G = +2, V_O = 2V_{PP}	440				MHz	typ	C
	G = +8, V_O = 2V_{PP}	330				MHz	typ	C
Slew rate	G = +2, V_O = 2V step	1700				V/µs	typ	C
	G = +8, V_O = 2V step	1700	1300			V/µs	min	B
Rise-and-fall time	G = +2, V_O = 2V step	1.0				ns	typ	C
	G = +8, V_O = 0.5V step	1.0				ns	typ	C
	G = +8, V_O = 2V step	1.0				ns	typ	C
Settling time to 0.02%	G = +8, V_O = 2V step	16				ns	typ	C
Settling time to 0.1%	G = +8, V_O = 2V step	10				ns	typ	C
Harmonic distortion	G = +8, f = 10MHz, V_O = 2V_{PP}							
2nd harmonic	R_L = 100Ω to 2.5V	–62	–58			dBc	max	B
	R_L ≥ 500Ω to 2.5V	–70	–66			dBc	max	B
3rd harmonic	R_L = 100Ω to 2.5V	–66	–64			dBc	max	B
	R_L ≥ 500Ω to 2.5V	–65	–63			dBc	max	B
2nd harmonic	G = +2, f = 10MHz, R_L = 100Ω	–68				dBc	typ	C
3rd harmonic	G = +2, f = 10MHz, R_L = 100Ω	–68				dBc	typ	C
Input voltage noise	f > 1MHz	1.8	2			nV/√Hz	max	B
Noninverting input current noise	f > 1MHz	18	19			pA/√Hz	max	B
Inverting input current noise	f > 1MHz	22	24			pA/√Hz	max	B
DC PERFORMANCE(4)								
Open-loop transimpedance gain (Z_{OL})	V_O = 2.5V, R_L = 100Ω to 2.5V	70	**40**	38	36	kΩ	min	A
Input offset voltage	V_{CM} = 2.5V	±0.3	**±3.5**	±4.0	±4.5	mV	max	A
Average offset voltage drift	V_{CM} = 2.5V			±10	±15	µV/°C	max	B
Noninverting input bias current	V_{CM} = 2.5V	±5	**±40**	±45	±50	µA	max	A
Average noninverting input bias current drift	V_{CM} = 2.5V			±110	±170	nA/°C	max	B
Inverting input bias current	V_{CM} = 2.5V	±5	**±60**	±70	±75	µA	max	A
Average inverting input bias current drift	V_{CM} = 2.5V			±120	±160	nA/°C	max	B
INPUT								
Least positive input voltage(5)		1.7	**1.8**	1.9	1.9	V	max	A
Most positive input voltage(5)		3.3	**3.2**	3.1	3.1	V	min	A
Common-mode rejection ratio (CMRR)	V_{CM} = 2.5V	54	**51**	50	50	dB	min	A
Noninverting input impedance		280 || 1.2				kΩ || pF	typ	C
Inverting input resistance (R_I)	Open-loop	37				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +21°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

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ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**

At R_F = 348Ω, R_L = 100Ω to 2.5V, and G = +8, unless otherwise noted.

		OPA3695						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
OUTPUT								
Most positive output voltage	No load	4.2	**4.0**	3.9	3.8	V	min	A
	R_L = 100Ω load to 2.5V	4.0	**3.9**	3.8	3.7	V	min	A
Least positive output voltage	No load	0.9	**1.0**	1.1	1.2	V	max	A
	R_L = 100Ω load to 2.5V	1.0	**1.1**	1.2	1.3	V	max	A
Current output, sourcing	V_O = 2.5V	+90	**+70**	+67	+66	mA	min	A
Current output, sinking	V_O = 2.5V	–90	**–70**	–67	–66	mA	min	A
Closed-loop output impedance	G = +2, f = 100kHz	0.05				Ω	typ	C
DISABLE (Disabled LOW)								
Power-down supply current (+V_S)	Per channel, $V_{\overline{DIS}}$ = 0V	–100	–160	–177	–180	µA	max	C
Disable time		1				µs	typ	C
Enable time		25				ns	typ	C
Off isolation	G = +8, 10MHz	70				dB	typ	C
Output capacitance in disable		4				pF	typ	C
Turn-on glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±100				mV	typ	C
Turn-off glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±20				mV	typ	C
Enable voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control pin input bias current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V	75	130	143	149	µA	max	C
POWER SUPPLY								
Specified single-supply operating voltage		5				V	typ	C
Maximum single-supply operating voltage range			**12**			V	max	A
Minimum operating voltage range			**3.5**	3.6	3.8	V	min	B
Maximum quiescent current	Per channel, V_S = +5V	11.4	**12.1**	12.6	13.0	mA	max	A
Minimum quiescent current	Per channel, V_S = +5V	11.4	**10.6**	9.1	8.8	mA	min	A
Power-supply rejection ratio (–PSRR)	Input-referred	56				dB	typ	C
TEMPERATURE RANGE								
Specification: IDBQ		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
DBQ SSOP-16		80				°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V

At R_F = 402Ω, R_L = 100Ω, and G = +8, unless otherwise noted.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

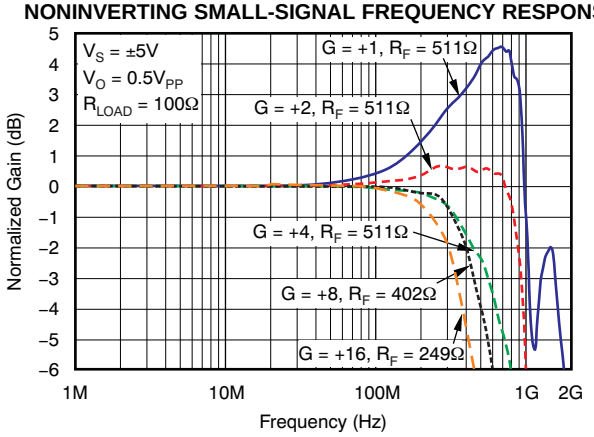


Figure 2.

GAIN OF +2, LARGE-SIGNAL FREQUENCY RESPONSE

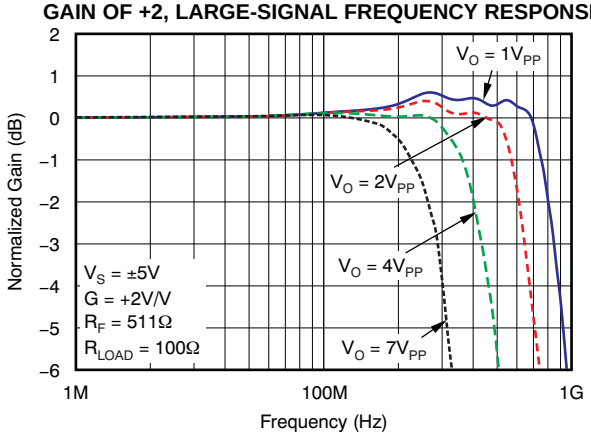


Figure 3.

GAIN OF +8, LARGE-SIGNAL FREQUENCY RESPONSE

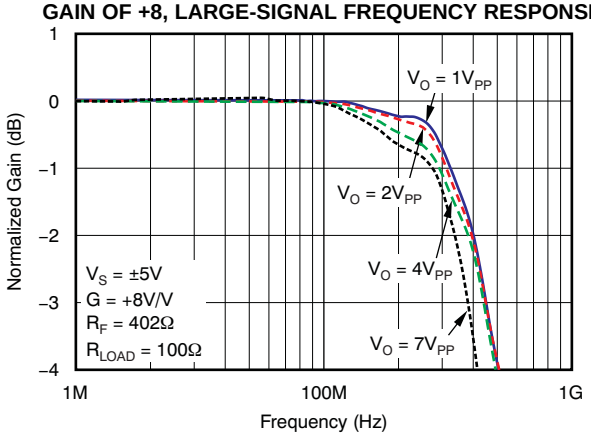


Figure 4.

NONINVERTING SMALL-SIGNAL PULSE RESPONSE

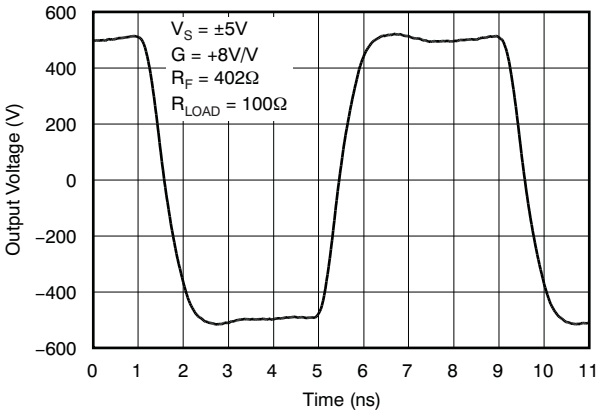


Figure 5.

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

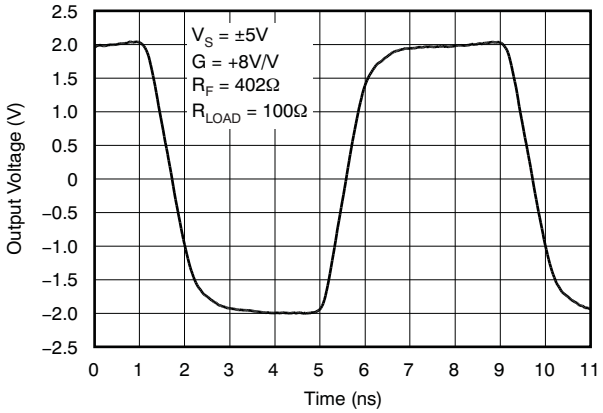


Figure 6.

10MHz HARMONIC DISTORTION vs LOAD RESISTANCE

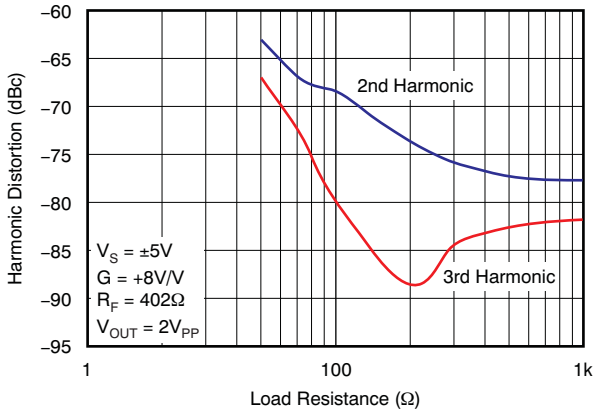


Figure 7.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At R_F = 402Ω, R_L = 100Ω, and G = +8, unless otherwise noted.

10MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

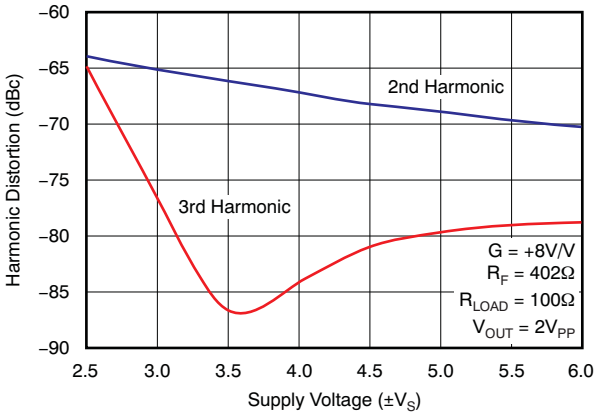


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

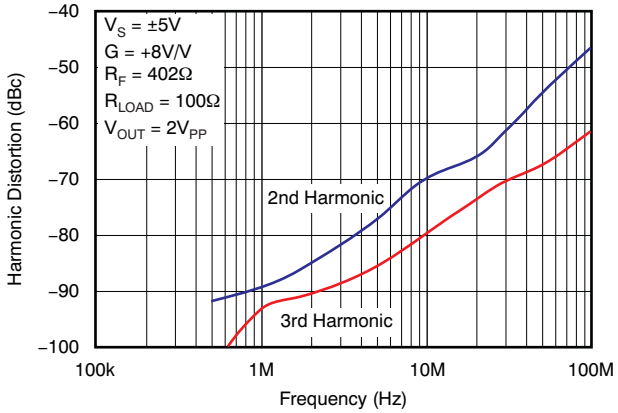


Figure 9.

10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

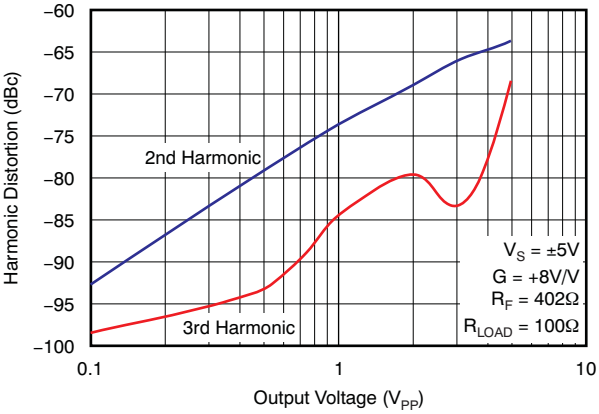


Figure 10.

10MHz HARMONIC DISTORTION vs NONINVERTING GAIN

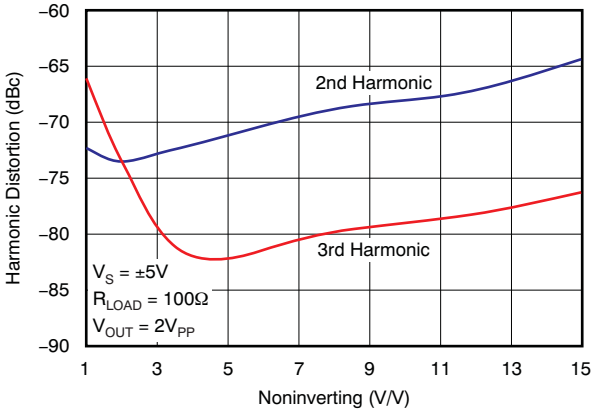


Figure 11.

10MHz HARMONIC DISTORTION vs LOAD RESISTANCE

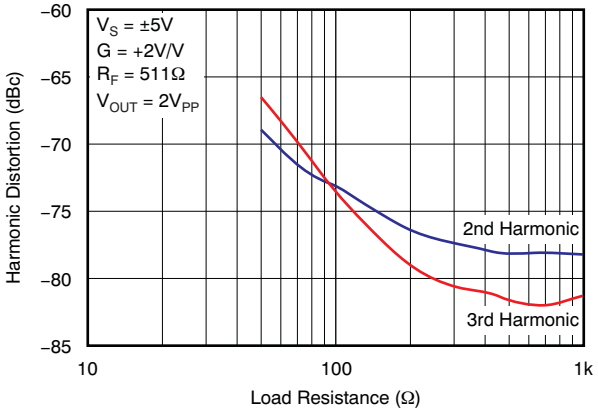


Figure 12.

10MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

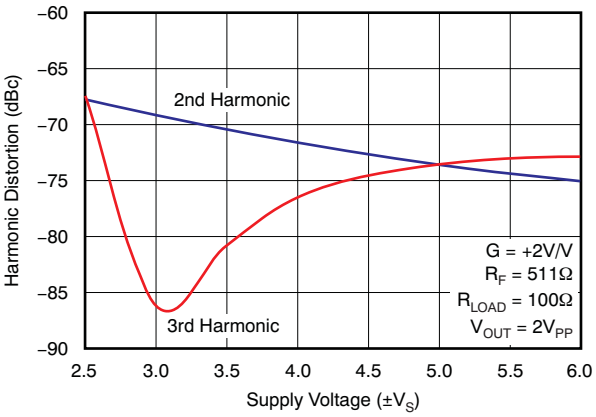


Figure 13.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At R_F = 402Ω, R_L = 100Ω, and G = +8, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

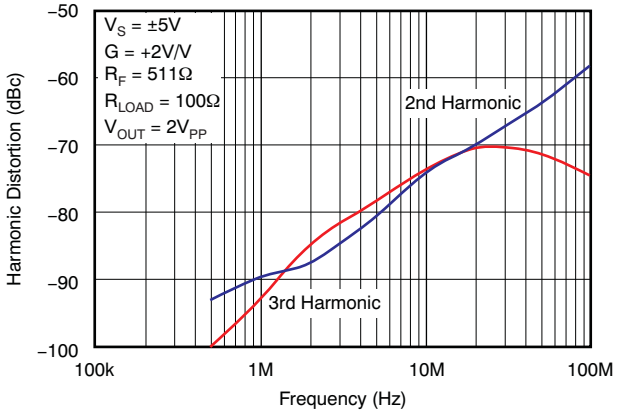


Figure 14.

10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

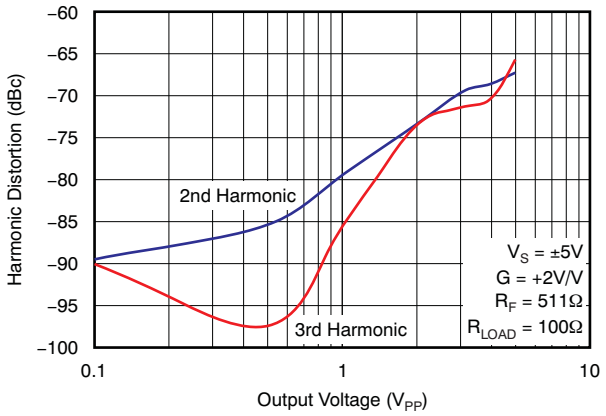


Figure 15.

10MHz HARMONIC DISTORTION vs INVERTING GAIN

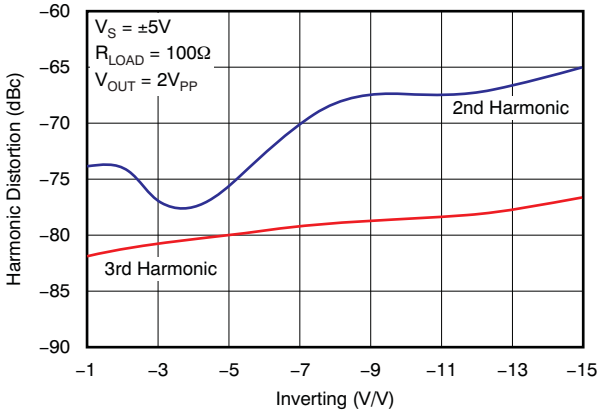


Figure 16.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

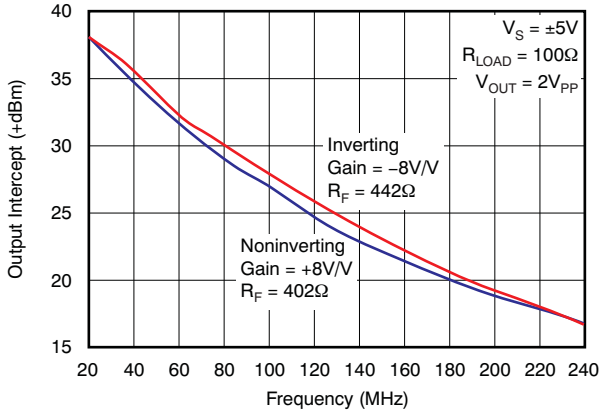


Figure 17.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

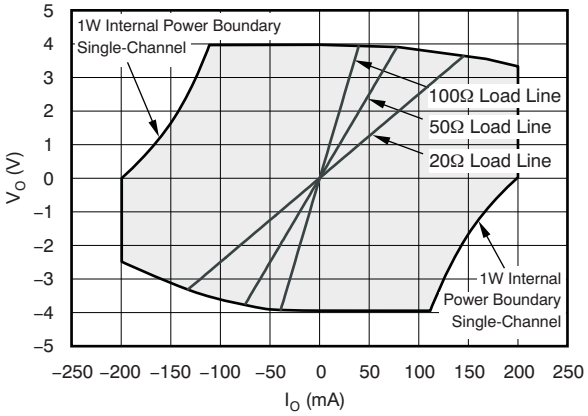


Figure 18.

DISABLE FEEDTHROUGH vs FREQUENCY

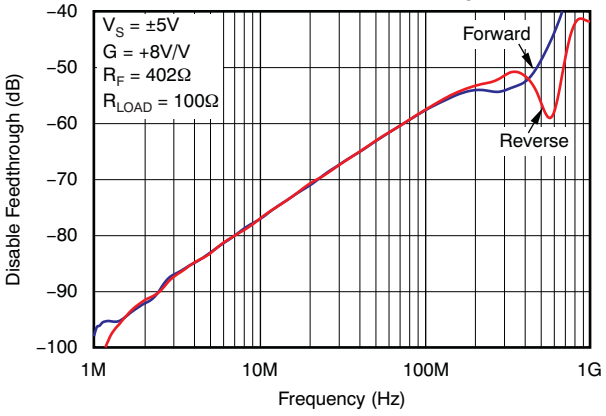


Figure 19.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At R_F = 402Ω, R_L = 100Ω, and G = +8, unless otherwise noted.

CROSSTALK vs FREQUENCY

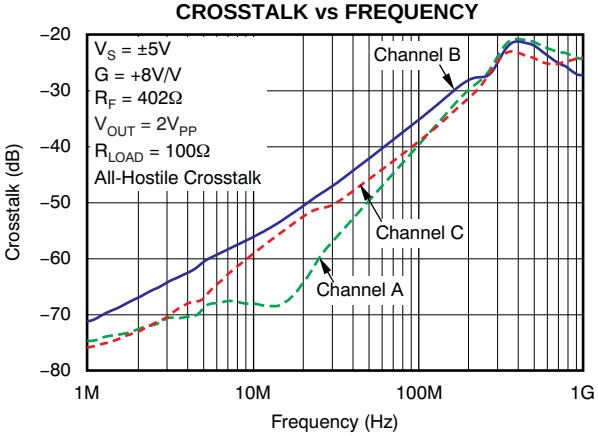


Figure 20.

DIFFERENTIAL GAIN AND PHASE vs NUMBER OF PARALLEL VIDEO LOADS

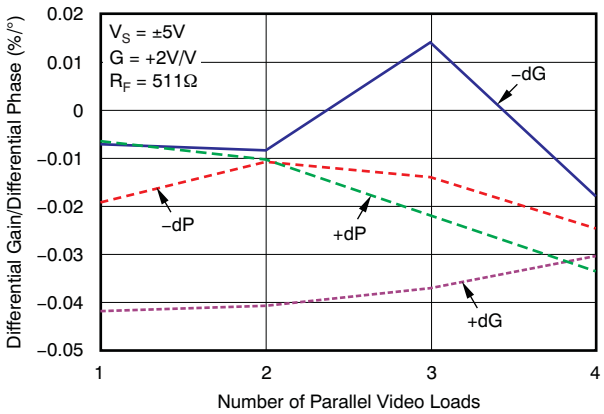


Figure 21.

DISABLE/ENABLE RESPONSE

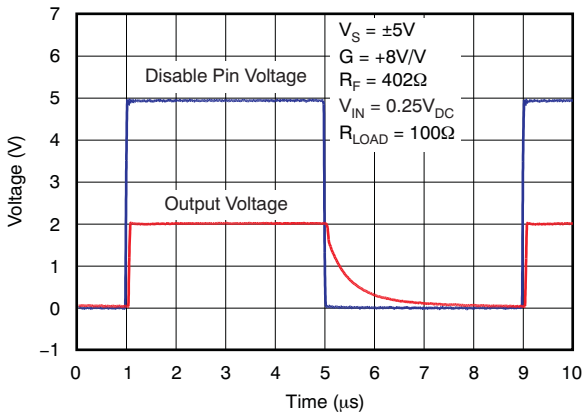


Figure 22.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

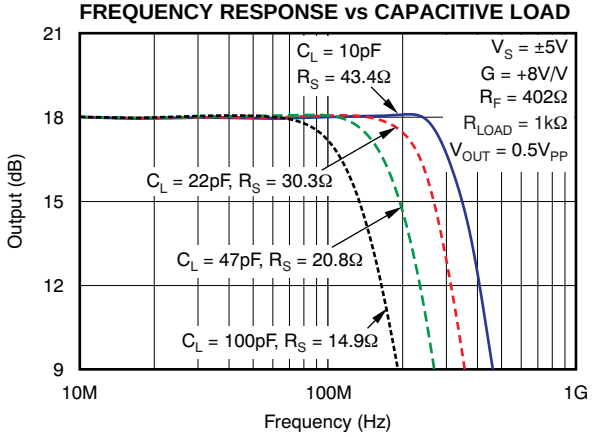


Figure 23.

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TYPICAL CHARACTERISTICS: V_S = +5V

At R_F = 348Ω, R_L = 100Ω to 2.5V, and G = +8, unless otherwise noted.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

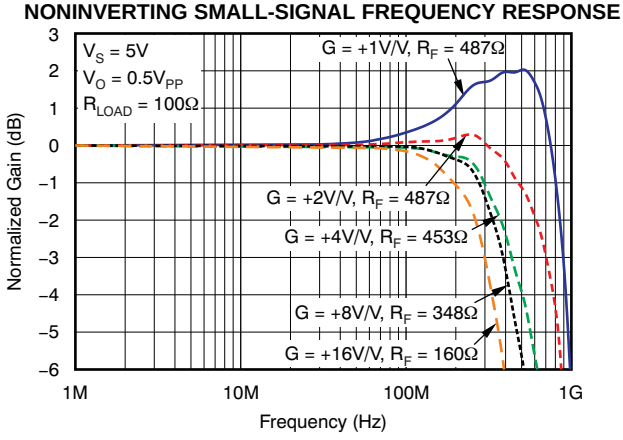


Figure 24.

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

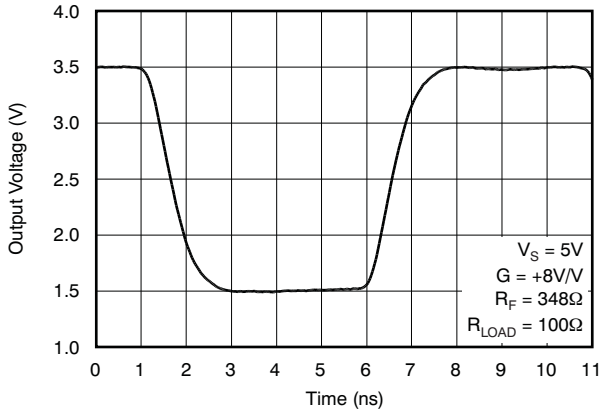


Figure 25.

HARMONIC DISTORTION vs FREQUENCY

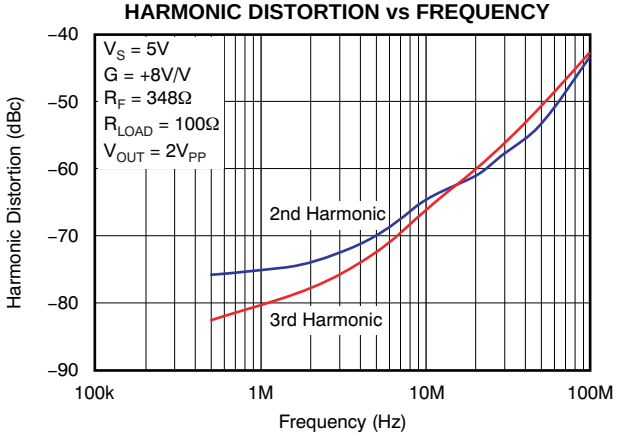


Figure 26.

10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

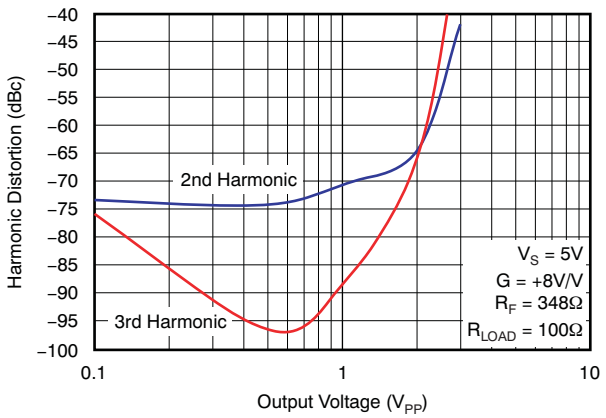


Figure 27.

10MHz HARMONIC DISTORTION vs LOAD RESISTANCE

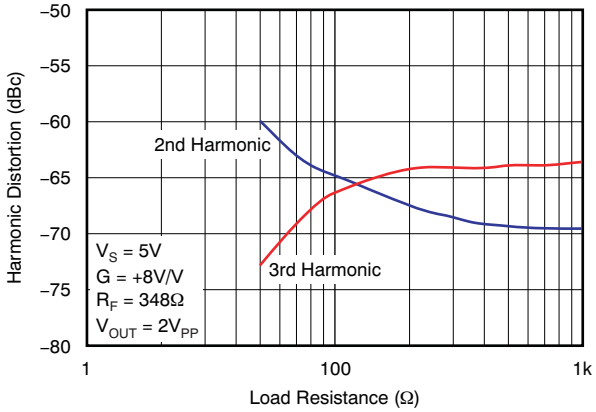


Figure 28.

HARMONIC DISTORTION vs FREQUENCY

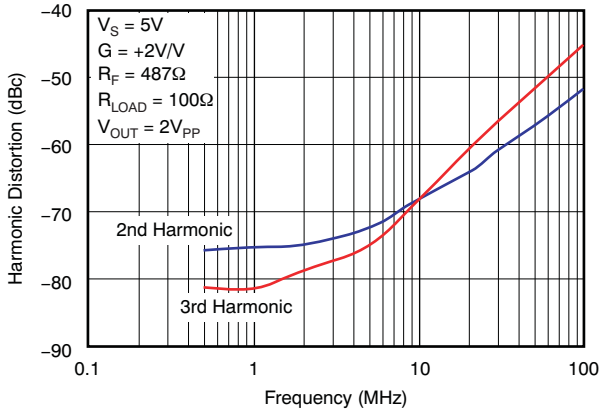


Figure 29.

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TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At R_F = 348Ω, R_L = 100Ω to 2.5V, and G = +8, unless otherwise noted.

10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

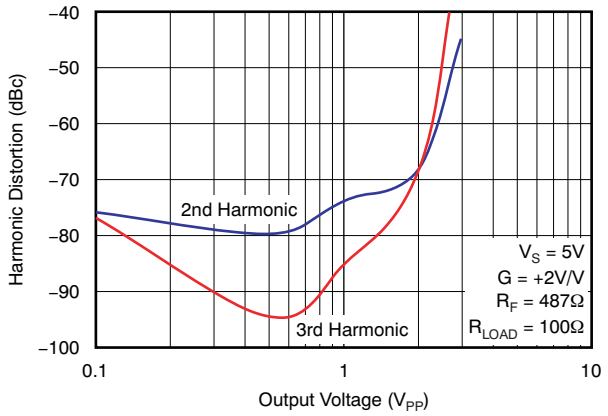


Figure 30.

10MHz HARMONIC DISTORTION vs LOAD RESISTANCE

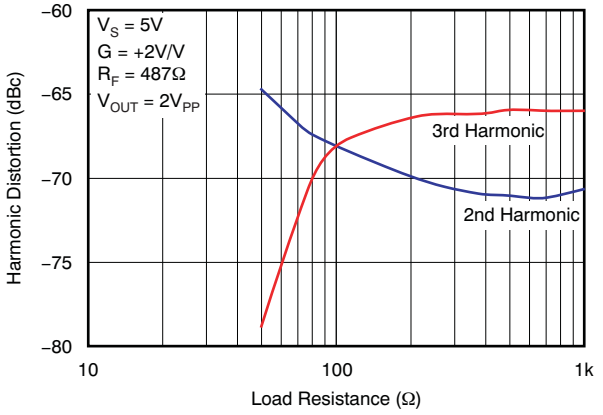


Figure 31.

TWO-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

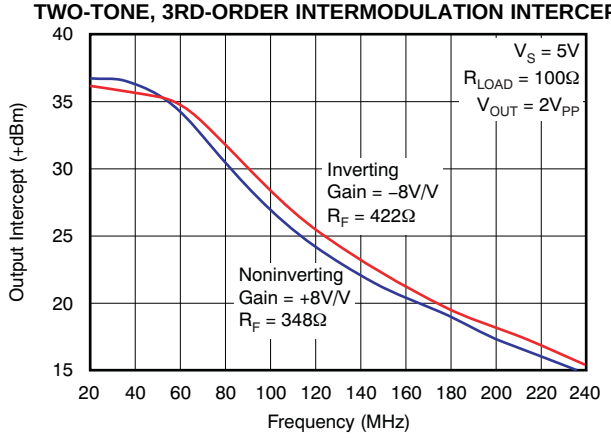


Figure 32.

RECOMMENDED R_S vs CAPACITIVE LOAD

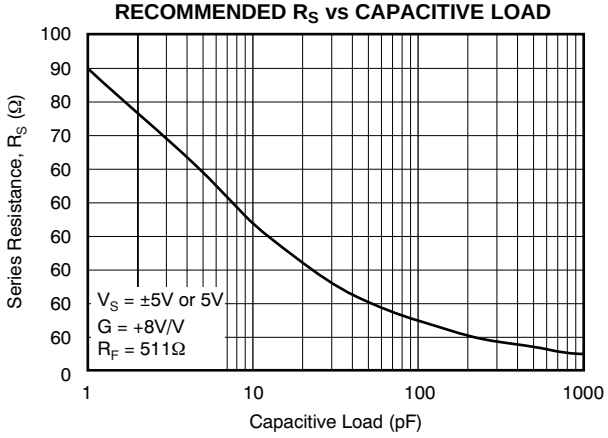


Figure 33.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

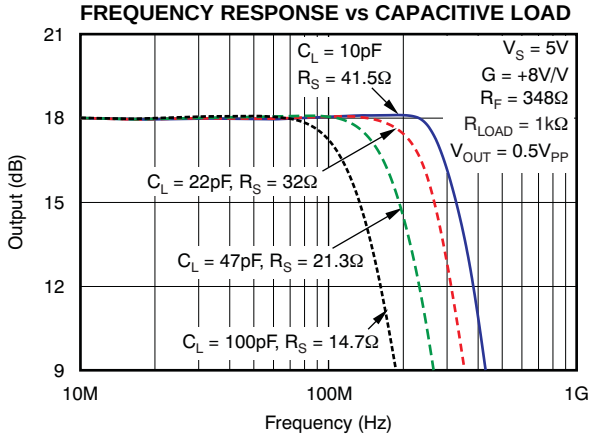


Figure 34.

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APPLICATION INFORMATION

WIDEBAND BUFFER OPERATION

The OPA3695 gives the exceptional ac performance of a wideband current-feedback op amp with a highly linear output stage. Requiring only 12.9mA/channel supply current, the OPA3695 achieves a 900MHz small-signal bandwidth (G = +2V/V); the high slew rate capability of up to 4300V/µs supports a 600MHz $2V_{PP}$ large signal into a 100Ω load. The low output headroom of 1V from either supply in a very high-speed amplifier gives very good single +5V operation. The OPA3695 delivers a $2V_{PP}$ swing with greater than 400MHz bandwidth operating on a single +5V supply. The primary advantage of a current-feedback video buffer (as opposed to a slew-enhanced, low-gain, stable voltage-feedback implementation) is a higher slew rate with lower quiescent power and output noise.

Figure 35 shows the dc-coupled, noninverting, dual power-supply circuit configuration used as the basis for the ±5V Electrical Characteristics table and Typical Characteristics curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground; the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 35, the total effective amplifier loading is 100Ω || (R_F + R_G) . For example, with a gain of +2V/V with R_F and R_G equal to 604Ω, the equivalent amplifier loading is 100Ω || 1208Ω = 92.3Ω. The disable control line ($\overline{DIS}$) is typically left open to ensure normal amplifier operation. Note that while most of the information presented in this data sheet was characterized with 100Ω loading, performance with a standard video loading of 150Ω has negligible impact on performance. Any changes in performance are typically improved over 100Ω loading because of lower output current demands.

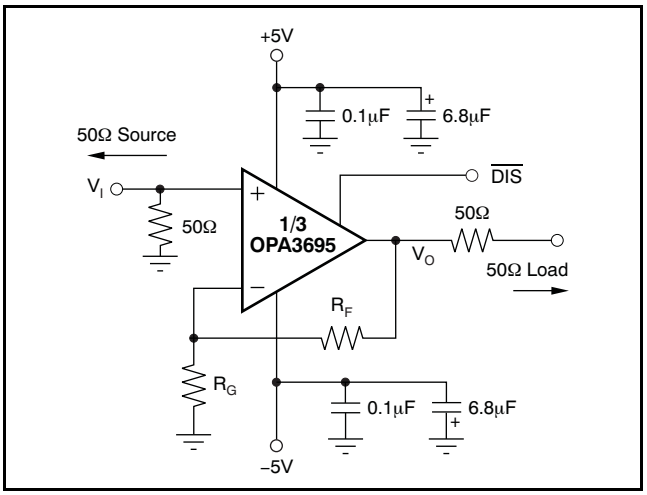


Figure 35. DC-Coupled, Noninverting, Bipolar-Supply, Specification and Test Circuit

Figure 36 illustrates the dc-coupled, inverting configuration used as the basis of the Inverting Typical Characteristic curves. Inverting operation offers several performance benefits. Since there is no common-mode signal across the input stage, the slew rate for inverting operation is higher and the distortion performance is slightly improved. An additional input resistor, R_M, is included in Figure 36 to set the input impedance equal to 50Ω. The parallel combination of R_M and R_G sets the input impedance. Both the noninverting and inverting applications of Figure 35 and Figure 36 benefit from optimizing the feedback resistor (R_F) value for bandwidth (see the discussion in the *Gain Setting* section). The typical design sequence is to select the R_F value for best bandwidth, set R_G for the gain, and then set R_M for the desired input impedance. As the gain increases for the inverting configuration, a point is reached where R_G equals 50Ω and R_M is removed; thus, the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, R_F is simply increased to increase gain. This approach, however, quickly reduces the achievable bandwidth at such high gains. For gains greater than 10V/V, noninverting operation is recommended to maintain broader bandwidth.

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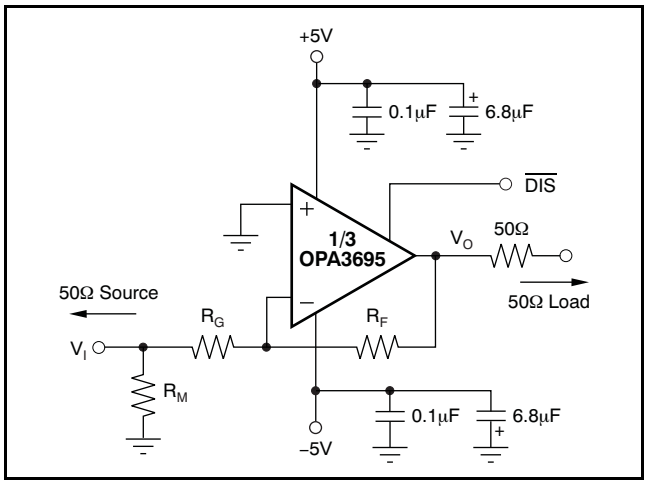


Figure 36. DC-Coupled, Inverting, Bipolar-Supply, Specification and Test Circuit

Notice that in this configuration (shown in Figure 36), the noninverting input is tied directly to ground. Because the internal design for the OPA3695 is current-feedback, trying to achieve improved dc accuracy by including a resistor on the noninverting input to ground is ineffective. Using a direct short to ground on the noninverting input reduces both the contribution of the dc bias current and the noise current to the output error. While the external R_M is used here to match with the 50Ω source from the test equipment, the input impedance in this configuration is limited to the R_G resistor. Removing R_M does not strongly impact the dc operating point because the short on the noninverting input of Figure 36 provides the dc operating voltage. This application of the OPA3695 provides a very broadband, high-output signal inverter.

SINGLE-SUPPLY OPERATION

The OPA3695 may be used over a single-supply range of +3.5V to +12V. Though not a rail-to-rail output design, the OPA3695 requires minimal input and output voltage headroom compared to other very-wideband video buffer amplifiers. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output.

The circuit of Figure 37 shows the single-supply ac-coupled, gain of +8V/V, video buffer circuit used as the basis for the Electrical Characteristics table and Typical Characteristics curves. The circuit of Figure 37 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 604Ω resistors). The input signal is then ac-coupled into this midpoint voltage bias. The input voltage can swing to within 1.6V of either supply pin, giving a $1.8V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (60.4Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is ac-coupled, giving the circuit a dc gain of +1V/V, which puts the input dc bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering ±90mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA3695 can deliver large bipolar output current into this midpoint load with minimal crossover distortion, as illustrated by the +5V supply, third-harmonic distortion plots.

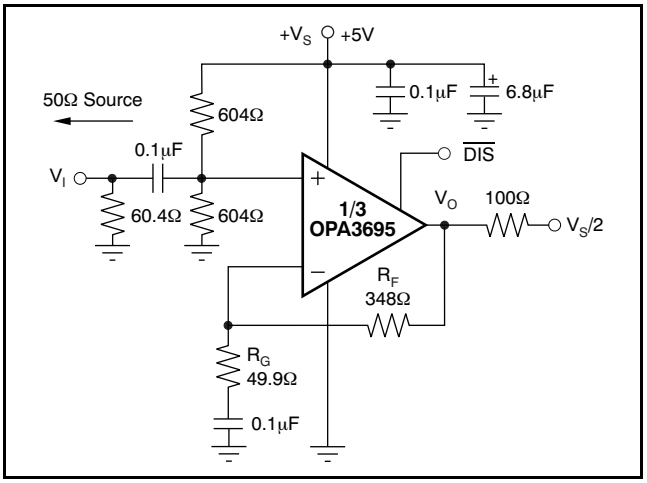


Figure 37. AC-Coupled, G = +8V/V, Single-Supply Specification and Test Circuit

While the circuit of Figure 37 shows +5V single-supply operation, this same circuit may be used for single supplies that range as high as +12V nominal. The noninverting input bias resistors are relatively low in Figure 37 to minimize output dc offset as a result of noninverting input bias current. At higher signal-supply voltages, these resistors should be increased in order to limit the added supply current drawn through this path.

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Figure 38 shows the ac-coupled, G = +2V/V, single-supply specification and test circuit. Once again, the noninverting input is dc-biased at midsupply to put that same $V_S/2$ at the output pin.

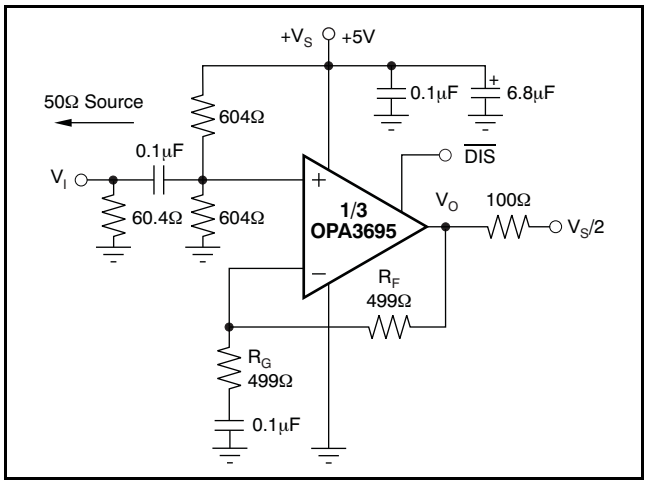


Figure 38. AC-Coupled, G = +2V/V, Single-Supply Specification and Test Circuit

HIGH-FREQUENCY ACTIVE FILTERS

The extremely wide bandwidth of the OPA3695 allows an extensive range of active filter topologies to be implemented with minimal amplifier bandwidth interaction in the filter shape. While Sallen-Key filters work very well with current-feedback amplifiers, the use of multiple feedback (MFB) filters is not recommended because an MFB filter places a capacitor in the feedback path which in turn eliminates compensation and results in an oscillator. In general, given a desired filter ω_O, the amplifier should have a minimum of 10X ω_O to minimize filter interaction with the amplifier frequency response. Figure 39 illustrates an example gain of +2 line driver using the OPA3695 that incorporates a 40MHz low-pass Butterworth response with only a few external components. The filter resistor values have been adjusted slightly here from an ideal filter analysis to account for parasitic effects.

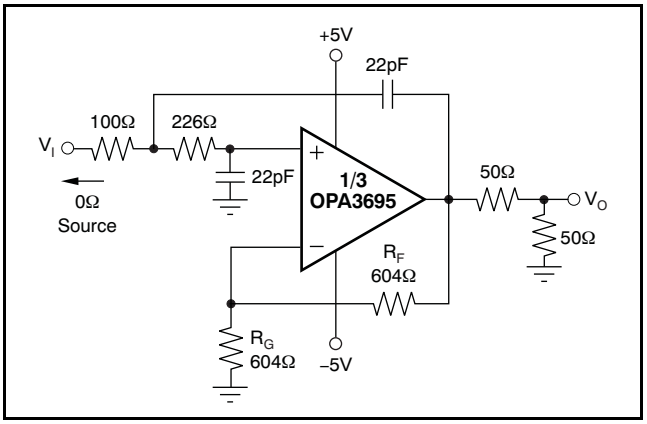


Figure 39. Line Driver with 40MHz Low-Pass Active Filter

This type of filter depends on a low output impedance from the amplifier through very high frequencies to continue to provide an increasing attenuation with frequency. As the amplifier output impedance rises with frequency, any input signal or noise starts to feed directly through to the output via the feedback capacitor. Because the OPA3695 used in Figure 39 has a 900MHz bandwidth, the active filter continues to roll-off through frequencies that exceed 200MHz. Figure 40 shows the frequency response for the filter of Figure 39, where the desired 40MHz cutoff is achieved and a 40dB/dec roll-off is held through very high frequencies.

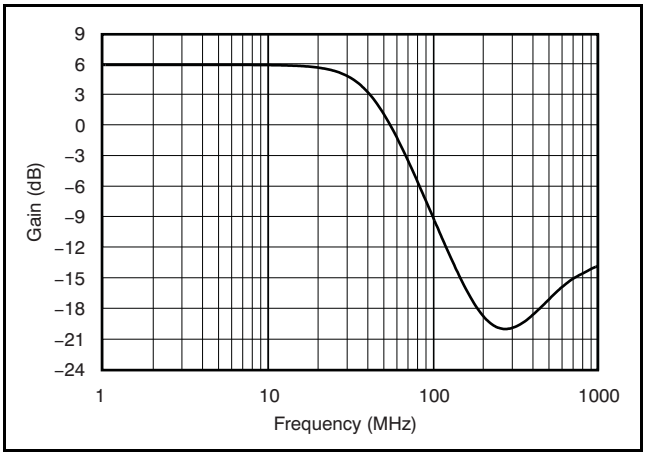


Figure 40. 40MHz Low-Pass Active Filter Response

HIGH-SPEED INSTRUMENTATION AMPLIFIER

Figure 41 shows an instrumentation amplifier circuit based on the OPA3695. Because all three amplifiers are on the same silicon die, the offset matching between inputs makes this configuration an attractive input stage for this application. The differential-to-single-ended gain for this circuit is 2V/V. The inputs are high-impedance, with only 1.2pF to ground at each input. The loads on the OPA3695 outputs are equal for the best harmonic distortion possible.

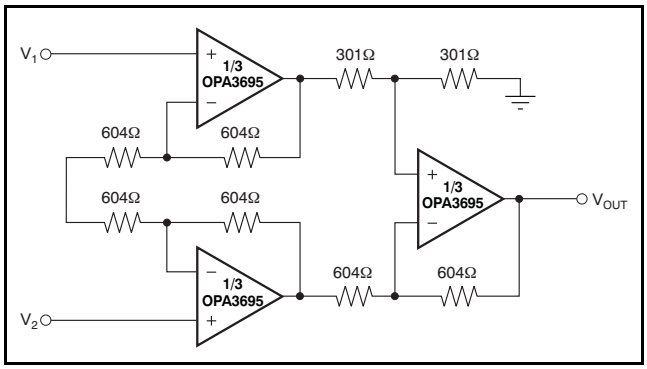


Figure 41. High-Speed Instrumentation Amplifier

MULTIPLEXED CONVERTER DRIVER

The converter driver in Figure 42 multiplexes among the three input signals with gains of +2V/V, +4V/V, and +8V/V. The OPA3695 enable and disable times support multiplexing among video signals. The *make-before-break* disable characteristic of the OPA3695 ensures that the output is always under control. To avoid large switching glitches, it is best to switch when the signal on the amplifier inputs are very close to each other.

The voltage difference appearing between the inverting node and the noninverting node should not exceed ±1.2V. This difference can occur when the individual amplifier is disabled and a voltage is applied at the summing node of the three amplifiers. The resulting inverting node voltage of the disabled amplifier is easily calculated by using simple resistor voltage divider methods. In general, as the gain of the amplifier increases, the less impact this issue has on the system because of the increased R_F/R_G ratio.

The output resistors isolate the outputs from each other when switching between channels. The feedback network of the disabled channels forms part of the load seen by the enabled amplifier, attenuating the signal slightly.

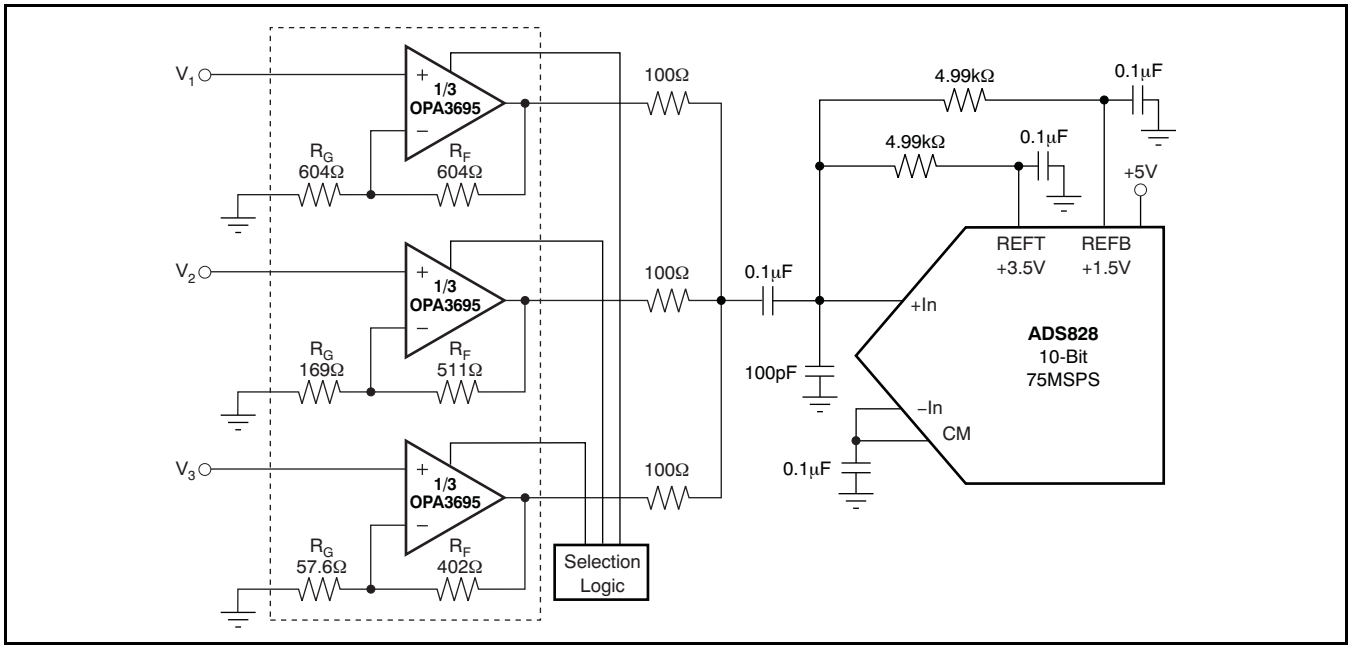


Figure 42. Multiplexed Converter Driver

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DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA3695. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 1.

Table 1. Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3695IDBQ, noninverting	SSOP-16	DEM-OPA-SSOP-3C	SBOU047
OPA3695IDBQ, inverting	SSOP-16	DEM-OPA-SSOP-3D	SBOU046

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA3695 product folder.

OPERATING SUGGESTIONS

GAIN SETTING

Similar to other current-feedback amplifiers, the OPA3695 compensation is dictated by the feedback resistor—R_F. As the resistance increases, more compensation is added to the amplifier. It is important to realize that increasing the resistance too far is not recommended because this increase causes a zero to form on the inverting input as a result of stray capacitance. In general, R_F should not exceed 1.5kΩ to 2kΩ, or else stability is a concern. Table 2 shows the recommended feedback values for common gain settings. These values are a good starting point; fine tuning of the resistor value(s) should be done to account for individual PCB designs and other factors.

Table 2. Recommended Feedback Resistor—R_F

GAIN (V/V)	±5V OR 10V SUPPLY	±2.5V OR 5V SUPPLY
+1	909Ω	750Ω
+2, –1	604Ω	499Ω
+4	511Ω	453Ω
+8	402Ω	348Ω
+16	249Ω	162Ω

OUTPUT CURRENT AND VOLTAGE

The OPA3695 provides output voltage and current capabilities that can easily support multiple video loads and/or 100Ω loads with very low distortion. Under no-load conditions at +25°C, the output voltage typically swings to 1V of either supply rail. Into a 15Ω load (the minimum tested load), it is tested to deliver ±120mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or *V-I product*, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 18) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA3695 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA3695 can drive ±3.4V into 20Ω or ±3.7V into 50Ω without exceeding either the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test-circuit load) shows full ±3.8V output swing capability, as shown in the Typical Characteristics.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the over-temperature min/max specifications. As the output transistors deliver power, the junction temperatures increase, which decreases the V_{BE}s (increasing the available output voltage swing) and increases the current gains (increasing the available output current). In steady-state operation, the available output voltage and current are always greater than that shown in the over-temperature characteristics since the output stage junction temperatures are higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This configuration is not normally a problem, because most applications include a series matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to an adjacent positive power-supply pin, in most cases, destroys the amplifier. If additional protection to a power-supply short is required, consider a small series resistor in the power-supply leads. Under heavy output loads, this resistor reduces the available output voltage swing. A 5Ω series resistor in each supply lead, for example, limits the internal power

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dissipation to < 1W for an output short while decreasing the available output voltage swing only 0.5V, for up to 100mA desired load currents. Always place the 0.1µF power-supply decoupling capacitors after these supply-current limiting resistors directly on the device supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance, which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA3695 can be very susceptible to decreased stability and may give closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path, resulting in a feedback path zero that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. The isolation acts to reduce the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show a *Recommended R_S vs Capacitive Load* curve (Figure 33) to help the designer pick a value to give < 0.5dB peaking to the load. The resulting frequency response curves show a 0.5dB peaked response for several selected capacitive loads and recommended R_S combinations.

Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3695. Long PCB traces, unmatched cables, and connections to other amplifier inputs can easily exceed this value. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA3695 output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load (< 0.5dB peaking). For the OPA3695 operating at a gain of +2V/V, the frequency response at the output pin is flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads.

DISTORTION PERFORMANCE

The OPA3695 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, the OPA3695 holds much lower distortion at higher frequencies (> 20MHz) than alternative solutions. Generally, until the fundamental signal reaches very high-frequency or power levels, the second harmonic dominates the distortion with a negligible third-harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 35), this value is the sum of $R_F + R_G$, while in the inverting configuration it is only R_F (see Figure 36). Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the second-order distortion slightly (3dB to 6dB).

The OPA3695 has very low third-order harmonic distortion—especially with high gains. This feature also produces a high two-tone, third-order intermodulation intercept. Two graphs for this intercept are given in the in the Typical Characteristics; one for ±5V and one for +5V. The curves shown in each graph is defined at the 50Ω load when driven through a 50Ω matching resistor, to allow direct comparisons to RF MMIC devices.

The intercept is used to predict the intermodulation spurious levels for two closely-spaced frequencies. If the two test frequencies (f_1 and f_2) are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta f = |f_2 - f_1|/2$, then the two, 3rd-order, close-in spurious tones appear at $f_O \pm 3 \times \Delta f$. The difference between two equal test tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \times (IM_3 - P_O)$, where IM_3 is the intercept taken from the Typical Characteristics and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For instance, at 40MHz, the OPA3695 at a gain of +8V/V has an intercept of 35dBm at a matched 50Ω load. If the full envelope of the two frequencies must be $2V_{PP}$ at this load, this requires each tone to be 4dBm ($1V_{PP}$). The third-order intermodulation spurious tones is then 2 × (35 – 4) = 62dBc below the test tone power level (–79dBm).

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NOISE PERFORMANCE

The OPA3695 offers an excellent balance between voltage and current noise terms to achieve a low output noise under a variety of operating conditions. The input noise voltage (1.8nV/√Hz) is very low for a unity-gain stable amplifier. This low input voltage noise was achieved at the price of higher noninverting input current noise (18pA/√Hz). As long as the ac source impedance looking out of the noninverting input is less than 100Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise using the OPA3695. Figure 43 shows the op amp noise analysis model with all of the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

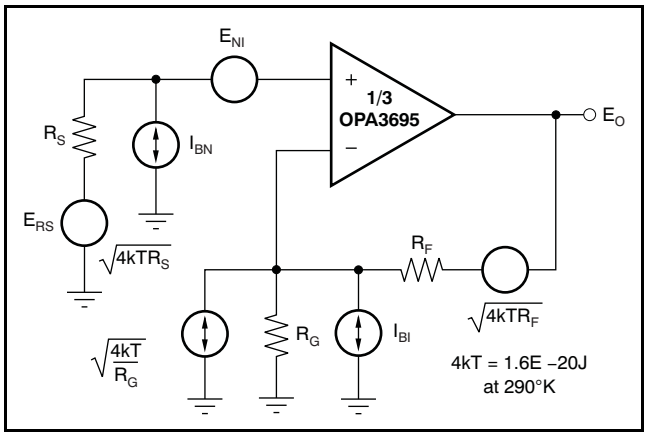


Figure 43. Op Amp Noise Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 43.

$$E_O = \sqrt{\left[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right]NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression through by noise gain (NG = 1 + R_F/R_G) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 2.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA3695 provides exceptional bandwidth and slew rate, giving fast pulse settling but only moderate dc accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce the error contributions to the output is ineffective. Evaluating the configuration of Figure 35 using a gain of +2V/V, using worst-case +25°C input offset voltage, and the two input bias currents, gives a worst-case output offset range equal to:

$$V_{OS} = \pm(NG \times V_{OS}) \pm (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$$
$$= \pm(2 \times 3.5mV) \pm (30\mu A \times 25\Omega \times 2) \pm (60\mu A \times 604\Omega)$$
$$= \pm 7mV \pm 1.5mV \pm 36.2mV$$
$$= \pm 44.7mV$$

where NG = noninverting signal gain.

Minimizing the resistance seen by the noninverting input also minimizes the output dc error. For improved dc precision in a wideband low-gain amplifier, consider the OPA842 where a bipolar input is acceptable (low source resistance) or the OPA656 where a JFET input is required.

DISABLE OPERATION

The OPA3695 provides an optional disable feature that can be used to reduce system power. If the $\overline{V_{DIS}}$ control pin is left unconnected, the OPA3695 operates normally. This shutdown is intended only as a power-savings feature. Forward path isolation when disabled is very good for small signals when configured for low gains. However, large-signal isolation is not ensured because of the ±1.2V limitation between the inverting node and the noninverting node. Failure to properly account for this voltage may cause undesirable responses in the output signal when multiplexed. Configuring the amplifier for high gains helps minimize this impact, but it is not ensured; proper analysis should be done by the designer.

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Turn-on time is very quick from the shutdown condition (typically < 25ns). Turn-off time strongly depends on the selected gain configuration and load, but is typically 1µs for the circuit of Figure 35. To shut down, the control pin must be asserted low. This logic control is referenced to the positive supply, as the simplified circuit of Figure 44 shows.

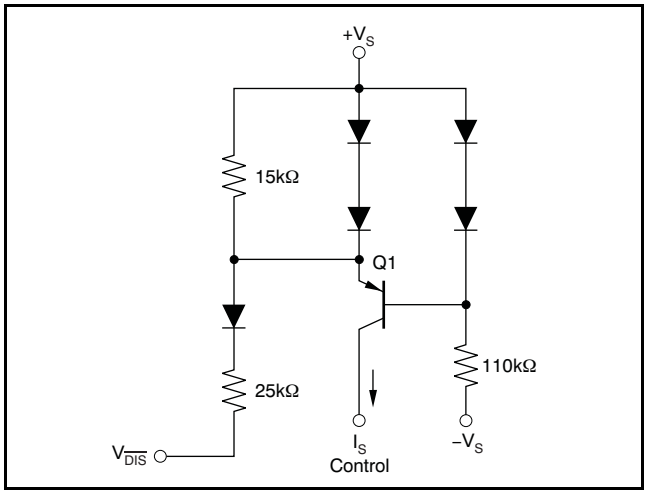


Figure 44. Simplified Disable Control Circuit

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 15kΩ resistor, eventually turning on these two diodes (≈ 80µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes, holding the emitter-base voltage of Q1 at approximately 0V. This sequence shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 44.

The shutdown feature for the OPA3695 is a positive-supply-referenced, current-controlled interface. Open-collector (or drain) interfaces are most effective, as long as the controlling logic can sustain the resulting voltage (in the open mode) that appears at the $V_{\overline{DIS}}$ pin. That voltage is one diode below the positive supply voltage applied to the OPA3695. For voltage output logic interfaces, the on/off voltage levels described in the Electrical Characteristics apply only for a +5V positive supply on the OPA3695. An open-drain interface is recommended for shutdown operation using a higher positive supply for the OPA3695 and/or logic families with inadequate high-level voltage swings.

THERMAL ANALYSIS

The OPA3695 does not require heatsinking or airflow in most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described here. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading. This value is the absolute highest power that can be dissipated for a given R_L. All actual applications dissipate less power in the output stage.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3695IDBQ (SSOP-16 package) in the circuit of Figure 35 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load at $V_S/2$. Maximum internal power is:

$$P_D = 10V \times 42.6mA + 3 \times 5^2/(4 \times (100\Omega \parallel 1.2k\Omega)) = 629mW$$

$$\text{Maximum } T_J = +85°C + (0.629W \times 80°C/W) = 135°C$$

Actual applications operate at a lower junction temperature than the +135°C computed above. This condition is because the RMS voltage of the output signals vary, along with the fact that part of the quiescent current is steered to the output, thus reducing the 10V × 42.6mA dominant term. Compute the actual output stage power to get an accurate estimate of maximum junction temperature, or use the results shown here as an absolute worst case maximum scenario.

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BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA3695 requires careful attention to PCB layout parasitics and external component types. Recommendations that optimize OPA3695 performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, create a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25” or 6,35mm) from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA3695. Use resistors that have low reactance at high frequencies. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value, as described previously. Increasing its value reduces the bandwidth, while decreasing it gives a more peaked frequency response. The 604Ω feedback resistor (used in the typical performance specifications at a gain of +2V/V on ±5V supplies) is a good starting point for design. Note that a 909Ω feedback resistor, rather than a direct short, is required for the unity-gain follower application. A current-feedback op amp requires a feedback resistor—even in the unity-gain follower configuration—to control stability. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values greater than 2.0kΩ, this parasitic capacitance can add a pole and/or zero below 400MHz that can affect circuit operation. Keep resistor values as low as possible consistent with load driving considerations.

d) Connections to other wideband devices on the PCB may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils, or 1,27mm to 2,54mm) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (Figure 33). Low parasitic capacitive loads (< 4pF) may not need an R_S because the OPA3695 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA3695 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as illustrated in the plot of Figure 33. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

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e) Socketing a high-speed part such as the OPA3695 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3695 directly onto the board.

INPUT AND ESD PROTECTION

The OPA3695 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 45.

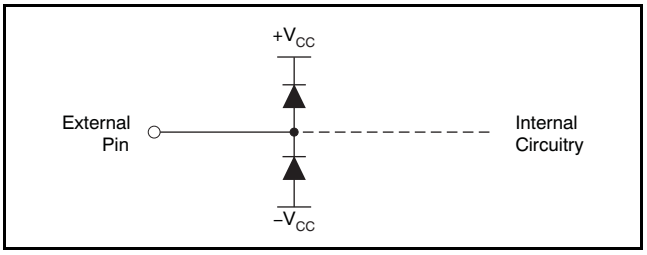


Figure 45. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA3695), current limiting series resistors may be added on the noninverting input. Keep this resistor value as low as possible; high values degrade both noise performance and frequency response.

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EVALUATION MODULE

To evaluate the OPA3695, an evaluation module (EVM) is available. This EVM allows for testing the OPA3695 in many different systems. Inputs and outputs include SMA connectors commonly found in high-frequency systems along with 50Ω characteristic impedance traces. Because the traces are very short, changing the input and output terminations resistors from 49.9Ω to 75Ω has essentially no impact when evaluating video signals. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user.

By default, all channels of the EVM are configured for a noninverting gain of +2V/V. If inverting configuration or differential input configuration is desired, then simply replacing R1, R4, and R7 with desired resistors allows these configurations to be set up quite easily. Also, the feedback and gain resistors can be easily replaced to allow for any gain desired.

Note that even though the default gain of the OPA3695 is +2V/V, or 6dB, the output 49.9Ω source termination resistors (R13, R14, and R15) and the user-applied 50Ω end-termination resistance commonly found in test systems makes the overall system gain appear as 0dB.

Each channel's disable control is independently configured. By default, the use of jumpers JP1, JP2, and JP3 allows for a quick and easy method to evaluate the disable function of the OPA3695. However, if this control must be externally controlled, then using the SMA connectors J10, J11, and J12 is recommended. The termination resistors R19, R20, and R21 should to be changed to match the source impedance, but it is not required. Attention to the voltage appearing at each disable pin is required to ensure proper operation of this feature. The voltage at the disable pin is shown in the Electrical Characteristics section of this data sheet.

This EVM is designed to be primarily used with split supplies from ±2.5V up to ±6V. This EVM can be used with a 5V single-supply up to 12V, but care must be taken to account for the input termination resistor connections to ground. Adiitionally, the 100uF bypass capcitors C1 and C2 are rate at 10V. If single supply is used with more than 10V applied, these capacitors should be changed to accomodate the increased supply voltage. The OPA3695 allowable input range is defined in the Electrical Characteristics section of this datasheet and must be adhered to for proper operation. Also note that the gain setting resistors are also connected to ground. Thus, any dc offset is increased proportionally by the gain. As such, using the EVM as a split supply is recommended even if the final use is single-supply. Example: if the final usage is to be 12V single-supply, then using ±6V supplies simplifies the dc reference voltage to mid-rail—or an equivalent 6V for a single-supply configuration.

Figure 46 shows the OPA3695EVM schematic. Figure 47 to Figure 50 illustrate the four layers of the EVM PCB, incorporating standard high-speed layout practices. Table 3 lists the Bill of Materials for the EVM as supplied from Texas Instruments.

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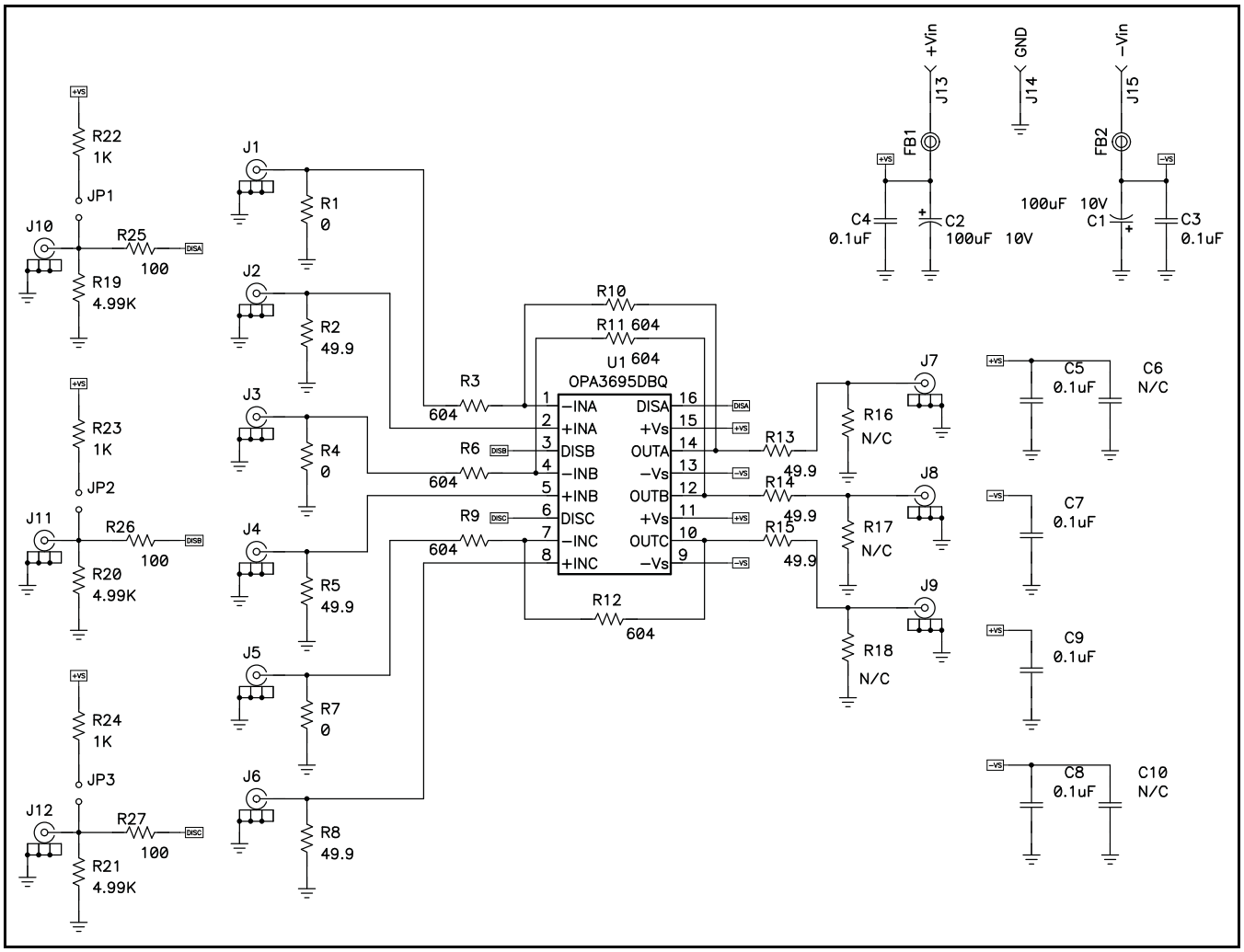


Figure 46. OPA3695D EVM Schematic

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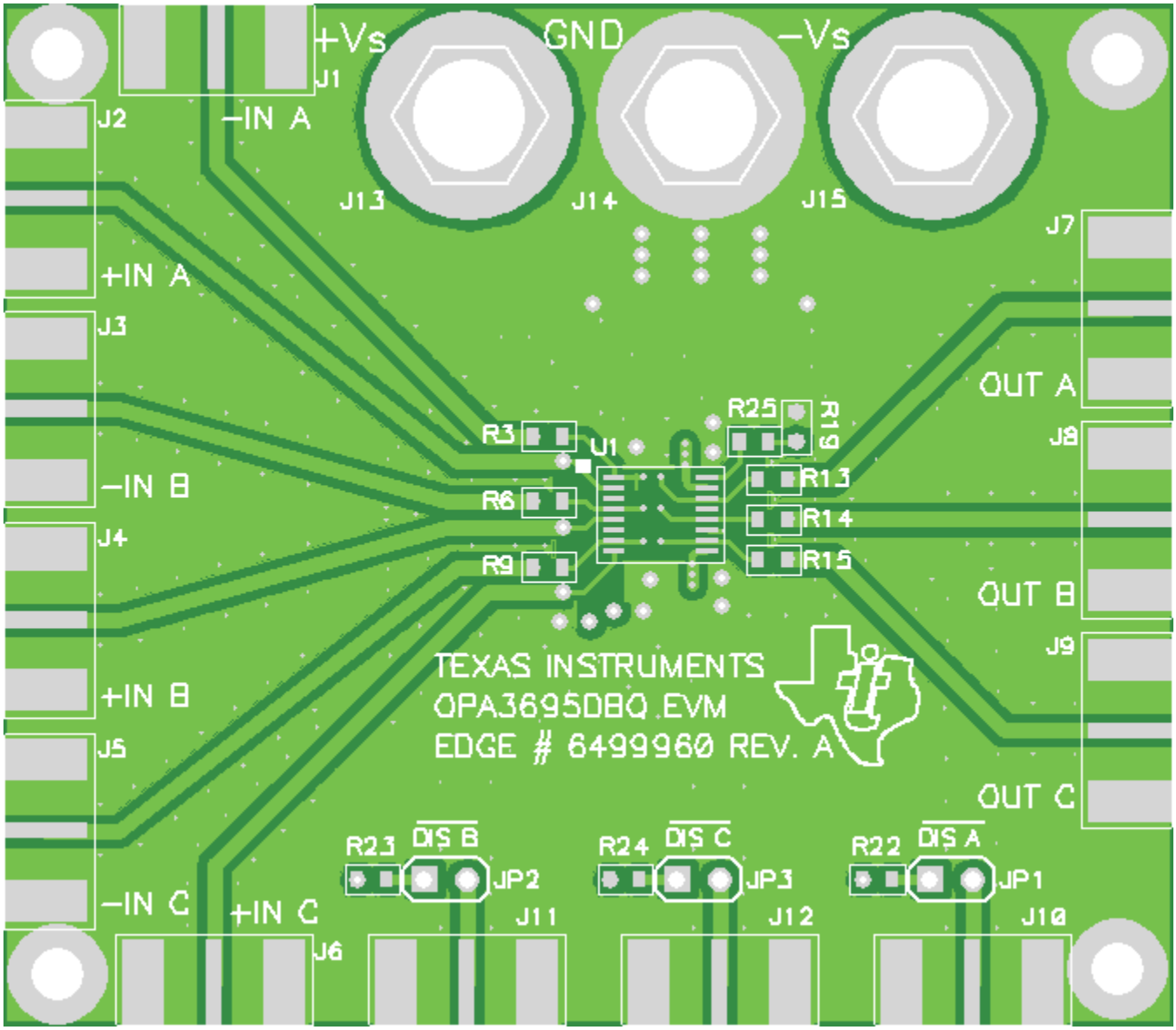


Figure 47. OPA3695D EVM PCB: Top Layer

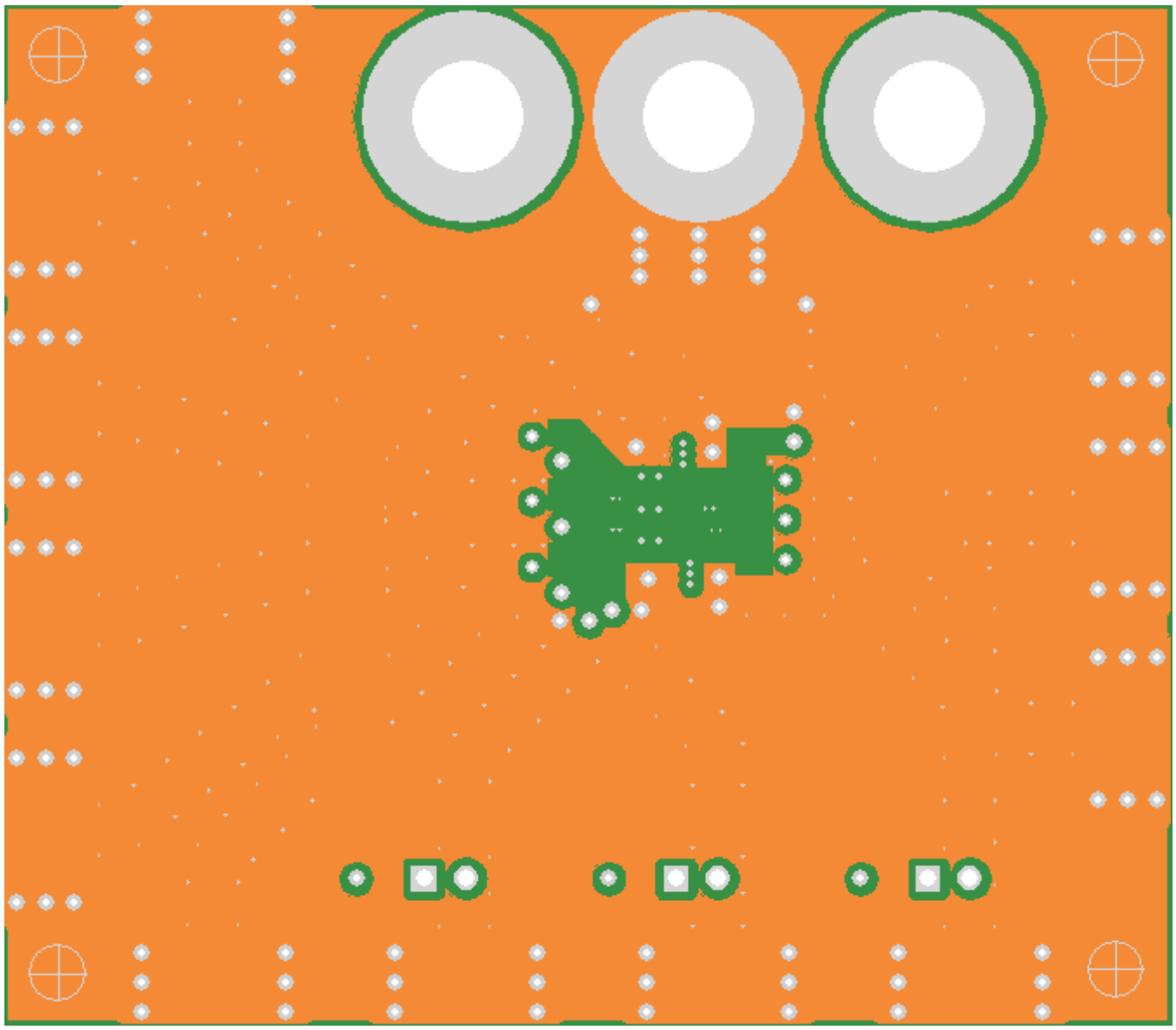


Figure 48. OPA3695D EVM PCB: Layer 2

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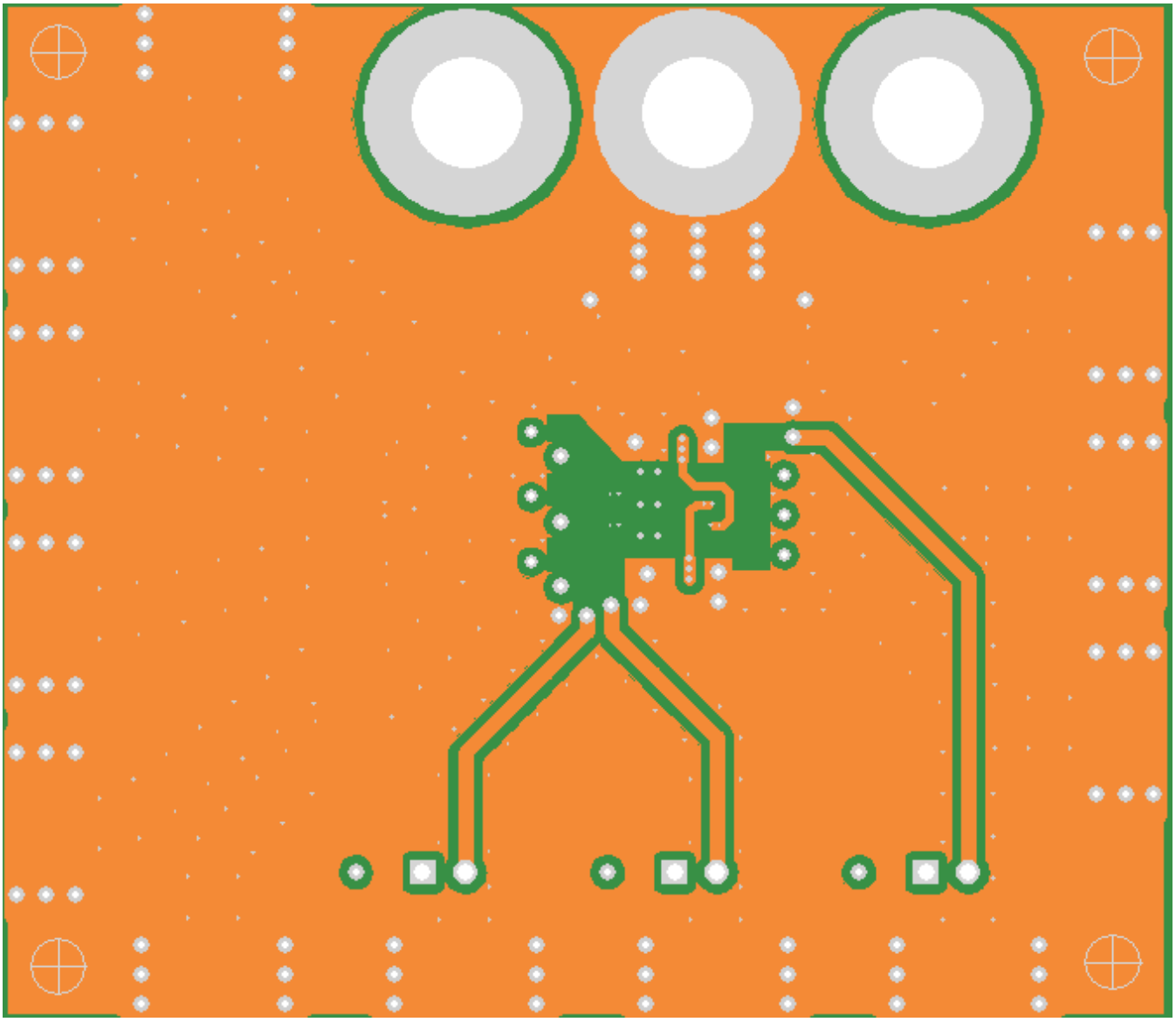


Figure 49. OPA3695D EVM PCB: Layer 3

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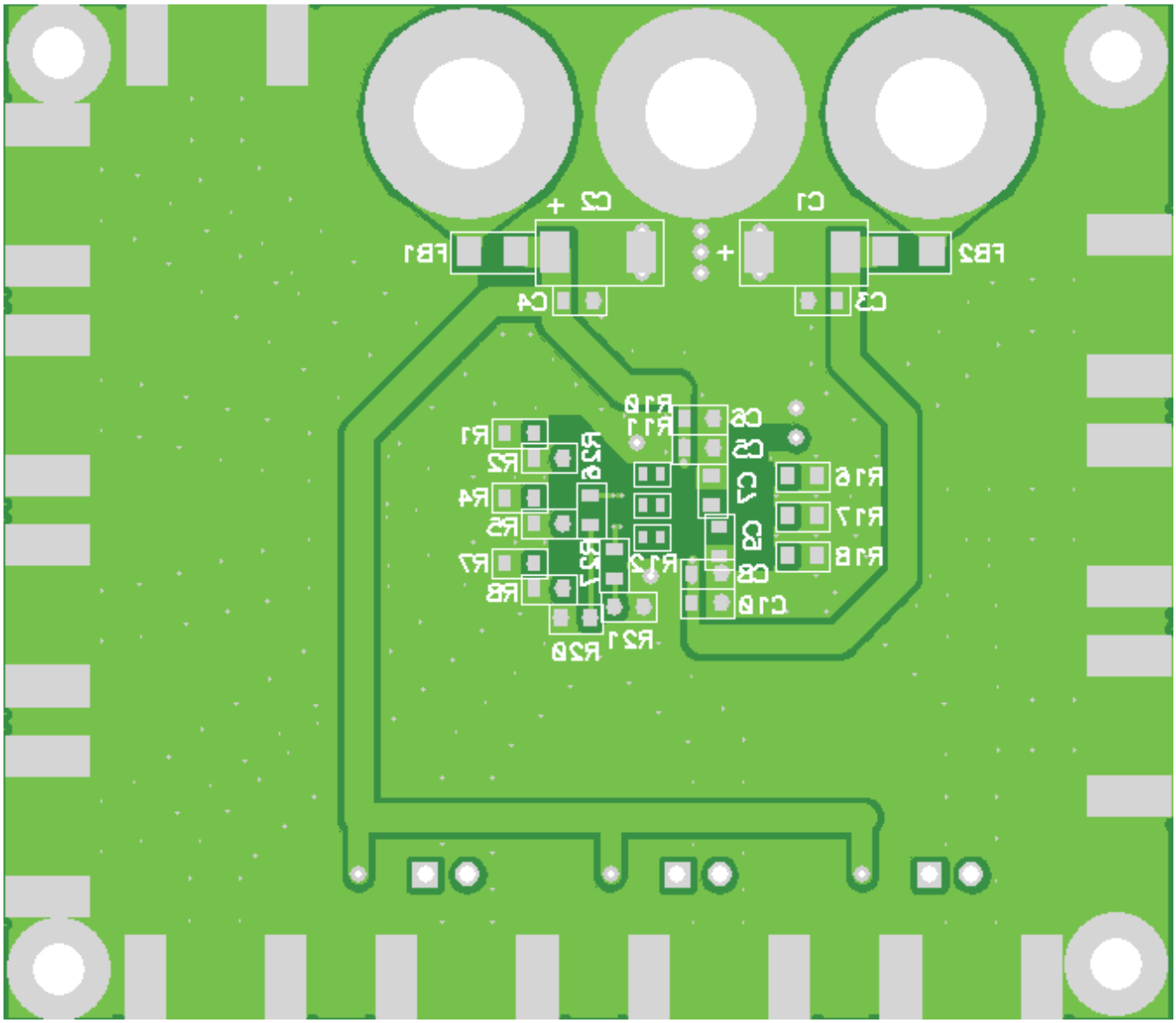


Figure 50. OPA3695D EVM PCB: Bottom Layer

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OPA3695EVM Bill of Materials

Table 3. OPA3695D EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1, FB2	2	Bead, Ferrite, 3A, 80Ω	1206	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	C1, C2	2	Capacitor, 100µF, Tantalum, 10V, 10%, Low-ESR	C	(AVX) TPSC107K010R0100	(Digi-Key) 478-1765-1-ND
3	C6, C10	2	Open	0603		
4	C3–C5, C7–C9	6	Capacitor, 0.1µF, Ceramic, 16V, X7R	0603	(AVX) 0603YC104KAT2A	(Digi-Key) 478-1239-1-ND
5	R10–R12	3	Resistor, 604Ω, 1/16W, 1%	0402	(KOA) RK73H1ETTP6040F	(Garrett) RK73H1ETTP6040F
6	R16–R18	3	Open	0603		
7	R1, R4, R7	3	Resistor, 0Ω, 1/10W	0603	(ROHM) MCR03EZPJ000	(Digi-Key) RHM0.0GCT-ND
8	R2, R5, R8, R13–R15	6	Resistor, 49.9Ω, 1/10W, 1%	0603	(ROHM) MCR03EZPFX49R9	(Digi-Key) RHM49.9HCT-ND
9	R25–R27	3	Resistor, 100Ω, 1/10W, 1%	0603	(ROHM) MCR03EZPFX1000	(Digi-Key) RHM100HCT-ND
10	R3, R6, R9	3	Resistor, 604Ω, 1/10W, 1%	0603	(ROHM) MCR03EZPFX6040	(Digi-Key) RHM604HCT-ND
11	R22–R24	3	Resistor, 1kΩ, 1/10W, 1%	0603	(ROHM) MCR03EZPFX1001	(Digi-Key) RHM1.00KHCT-ND
12	R19–R21	3	Resistor, 4.99kΩ, 1/10W, 1%	0603	(ROHM) MCR03EZPFX4991	(Digi-Key) RHM4.99KHCT-ND
13	J13–J15	3	Jack, Banana Receptance, 0.25" dia. hole		(SPC) 813	(Newark) 39N867
14	J1–J12	12	Connector, edge, SMA PCB Jack		(Johnson) 142-0701-801	(Newark) 90F2624
15	JP1–JP3	3	Header, 0.1" CTRS, 0.025" square pins	2 possible	(Sullins) PCB36SAAN	(Digi-Key) S1011E-36-ND
16	JP1–JP3	3	Shunts		(Sullins) SSC02SYAN	(Digi-Key) S9002-ND
17		4	Standoff, 4-40 hex, 0.625" length		(Keystone) 1808	(Digi-Key) 1808K-ND
18		4	Screw, Phillips, 4-40, .250"		(BF) PMS 440 0031 PH	(Digi-Key) H343-ND
19	U1	1	IC, OPA3695DBQ		(TI) OPA3695DBQ	
20		1	Printed circuit board		(TI) Edge# 6499960 Rev. A	

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Revision History

Changes from Original (April 2008) to Revision A **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2
- Added *Evaluation Module* section 23

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±1.7V to ±6.5V dual supply and the output voltage range of 0V to ±6.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3695IDBQ	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3695	Samples
OPA3695IDBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3695	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

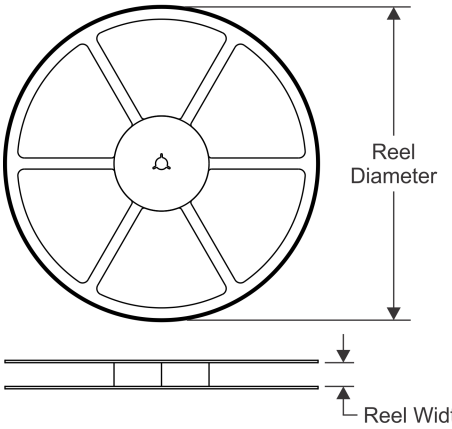
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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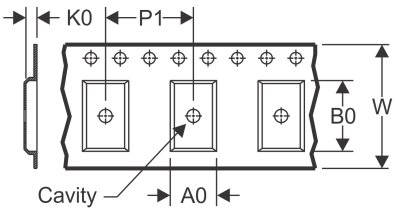
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

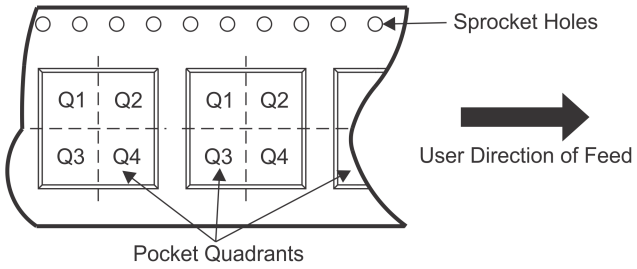


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

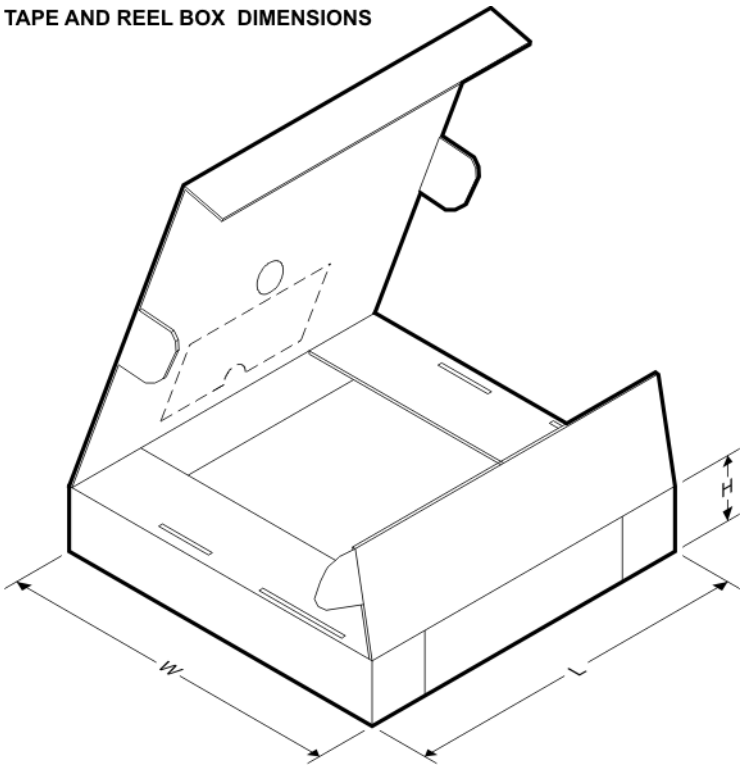
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3695IDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



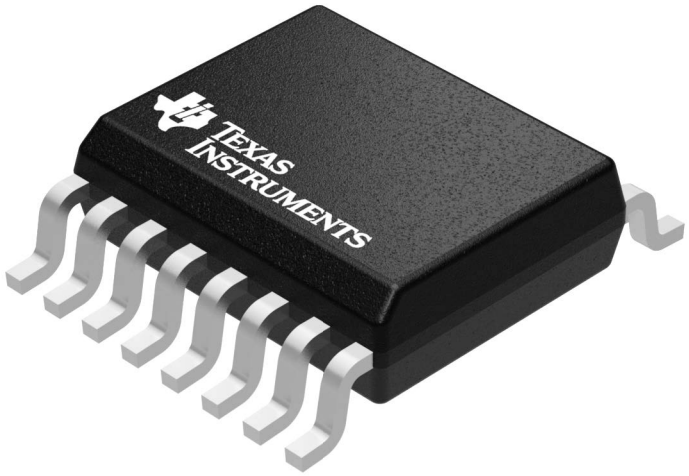
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3695IDBQR	SSOP	DBQ	16	2500	367.0	367.0	35.0

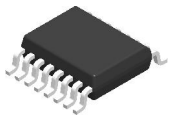
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

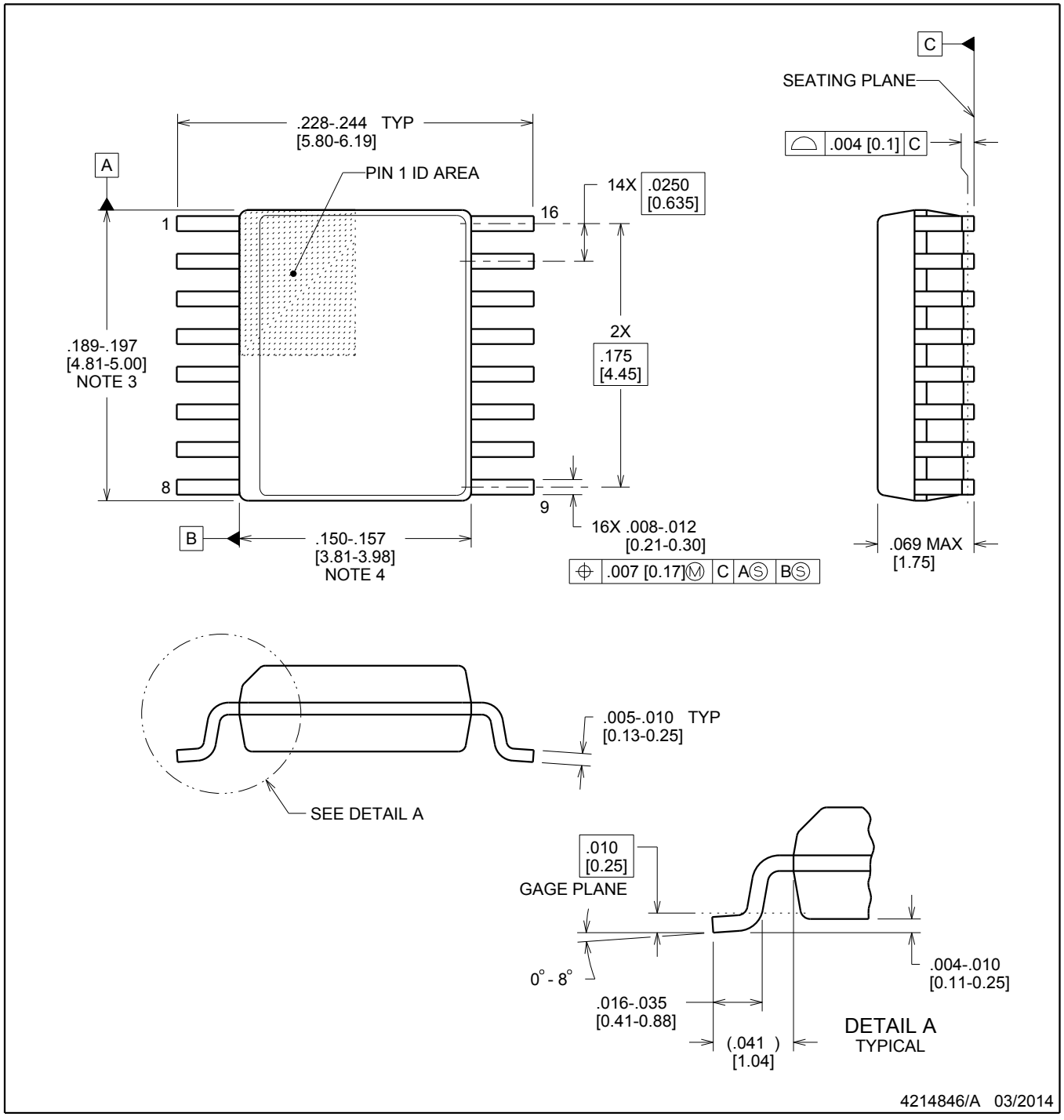


PACKAGE OUTLINE

DBQ0016A

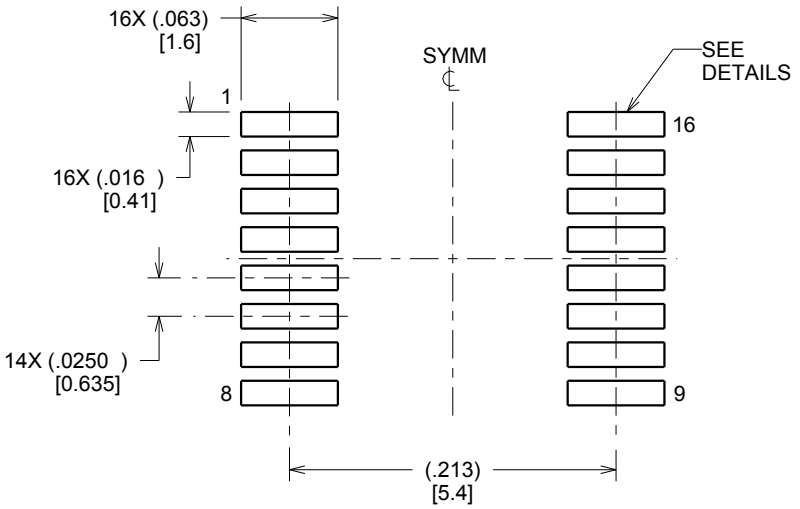
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

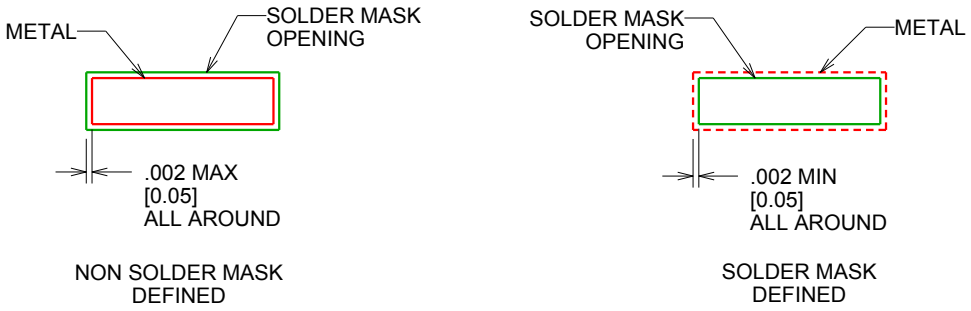


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

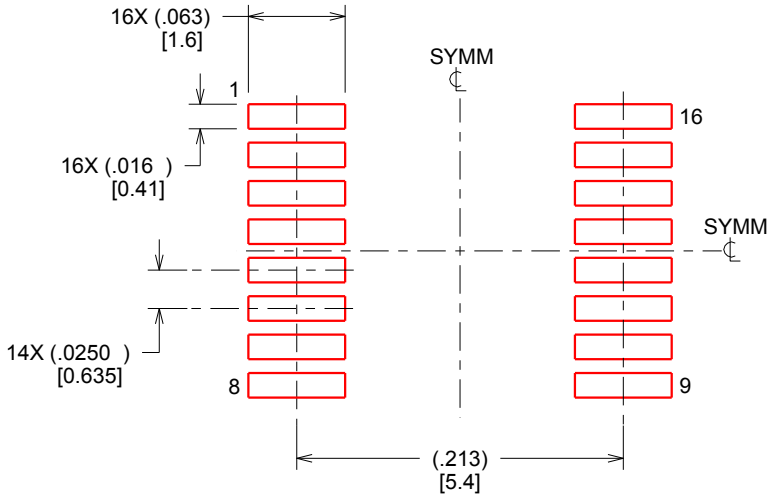
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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