OPA1671 13MHz、低噪声、轨至轨、音频运算放大器

1 特性

- 低噪声：
  10kHz 下为 4nV/√Hz
  1kHz 下为 4.7fA/√Hz
- 低失真：-109dB (0.00035%)
- 宽增益带宽：13MHz
- 轨至轨输入和输出
- 低电源电压范围：1.7V 至 5.5V
- 低输入电容
  - 差动：6pF
  - 共模：2.5pF
- 低输入偏置电流：10pA
- 低功耗电源电流：940µA
- 行业标准封装：SC-70

2 应用

- 麦克风前置放大器
- 辅助线路输入/输出
- 有源滤波器电路
- 跨阻放大器
- 电压缓冲器

3 说明

OPA1671 是一款宽带宽、低噪声、低失真音频运算放大器，可提供轨至轨输入和输出操作。这些器件可提供低压噪声、电流噪声和输入电容的完美组合，从而能够在各种音频和工业应用中提供高 应用中运行。
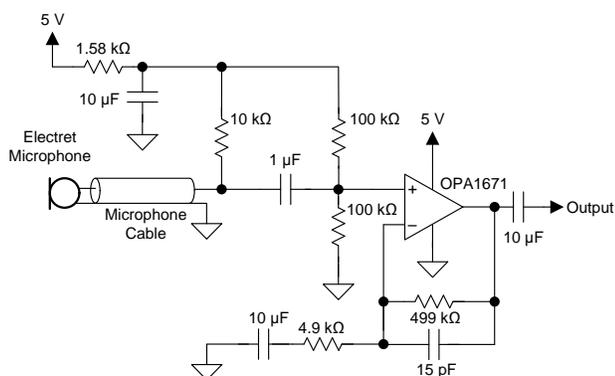
OPA1671 的独特内部拓扑可提供极低的失真 (-109dB)，同时仅消耗 940µA 的电源电流。OPA1671 的宽带宽 (13MHz) 和高压摆率 (5V/µs) 使其成为高增益音频和工业信号调节的绝佳选择。OPA1671 采用 SC-70 封装，可以在扩展工业温度范围（-40°C 至 +125°C）内正常工作。
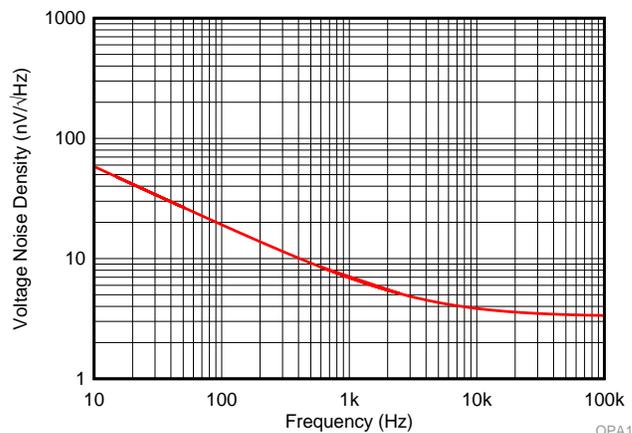
器件信息[1]

器件型号	封装	封装尺寸（标称值）
OPA1671	SC-70 (5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

驻极体麦克风前置放大器

OPA1671 电压噪声密度

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (November 2018) to Revision A   **Page**

- 首次发布生产数据数据表 1

5 Pin Configuration and Functions

DCK Package
5-Pin SC-70
Top View

Not to scale
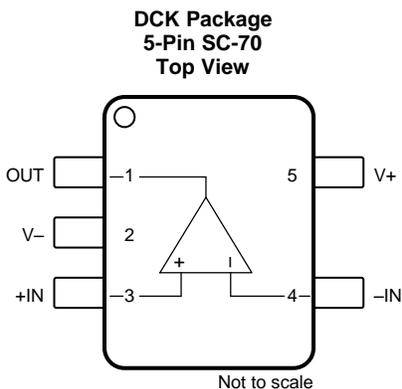
Pin Functions

PIN		I/O	DESCRIPTION
NAME	SC-70		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)			6	V
Input voltage		(V–) –0.3	(V+) +0.3	V
Output short-circuit[2]			Continuous	
Operating temperature		–55	150	°C
Specified temperature		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)	1.7 (±0.85)		5.5 (±2.75)	V
Specified temperature	–40		125	°C

6.4 Thermal Information

	THERMAL METRIC[1]	OPA1671 DCK (SC-70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics:V_S = ±0.85 V to ±2.75 V (V_S = 1.7 V to 5.5 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}, V_S = 5.5 V			0.00035%		
					−109		dB
IMD	Intermodulation distortion	G = 1, V_O = 1 V_{RMS}, V_S = 5.5 V	SMPTE/DIN Two-Tone, 4:1, (60 Hz and 7 kHz)		0.00158		
					-96		dB
			CCIF Two-Tone (19 kHz and 20 kHz)		0.0005		
					-106		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				13		MHz
SR	Slew rate	4-V step, G = 1			5		V/μs
t_S	Settling time	To 0.1%, 2-V step , G = 1			0.75		μs
		To 0.01%, 2-V step , G = 1			1		μs
	Overload recovery time	V_{IN} × gain > V_S			0.35		μs
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.4		$μV_{PP}$
e_N	Input voltage noise density	f = 10 Hz			45		nV/√Hz
		f = 1 kHz			7		
		f = 10 kHz			4.0		
i_N	Input current noise	f = 1 kHz			4.7		fA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.25	±1.25	mV
		T_A = −40°C to 125°C			±0.25		
dV_{OS}/dT	Input offset voltage drift	T_A = −40°C to 125°C			±0.3	±2.2	μV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = (V⁻)			±30	±130	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			V⁻		V⁺	V
CMRR	Common-mode rejection ratio	Vs = 1.7 V, (V⁻) < V_{CM} < (V⁺) − 1.25 V		74	91		dB
		Vs = 5.5 V, (V⁻) < V_{CM} < (V⁺) − 1.25 V		80	96		dB
		Vs = 1.7 V, V_{CM} = 0 V to 1.7 V		60	88		dB
		Vs = 5.5 V, V_{CM} = 0 V to 5.5 V		68	102		dB
INPUT CAPACITANCE							
Z_{ID}	Differential				10^{13} ‖ 6		MΩ ‖ pF
Z_{ICM}	Common-mode				10^{13} ‖ 2.5		GΩ ‖ pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V⁻) + 50 mV < V_O < (V⁺) − 50 mV, R_L = 10 kΩ		97	113		dB
		(V⁻) + 50 mV < V_O < (V⁺) − 50 mV, R_L = 10 kΩ	T_A = −40°C to 125°C		106		dB
		(V⁻) + 200 mV < V_O < (V⁺) − 200 mV, R_L = 2 kΩ		97	112		dB
		(V⁻) + 200 mV < V_O < (V⁺) − 200 mV, R_L = 2 kΩ	T_A = −40°C to 125°C		105		dB
OUTPUT							
	Voltage output swing from rail	V_S = 5.5 V, R_L = 10 kΩ			10	20	mV
I_{SC}	Short-circuit current	Sinking, V_S = 5.5 V			−57		mA
		Sourcing, V_S = 5.5 V			66		

Electrical Characteristics:V_S = ±0.85 V to ±2.75 V (V_S = 1.7 V to 5.5 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		0.94	1.3	mA
		I_O = 0 mA, T_A = −40°C to 125°C			1.4	

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

N = 9904 V_S = ±2.75 V   VOSH

图 1. Offset Voltage Production Distribution

N = 9904 V_S = ±0.85 V   VOSL
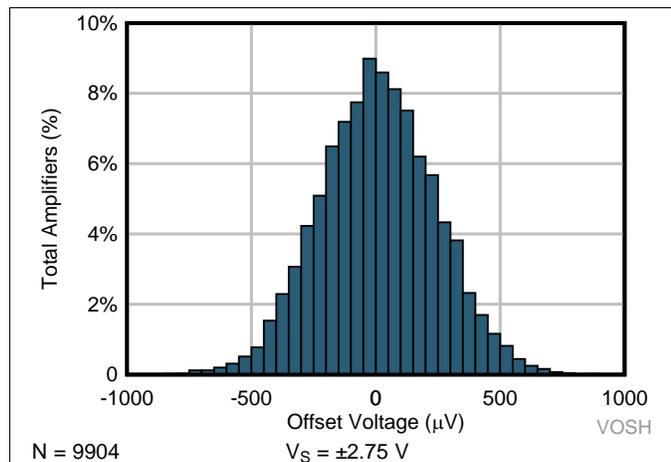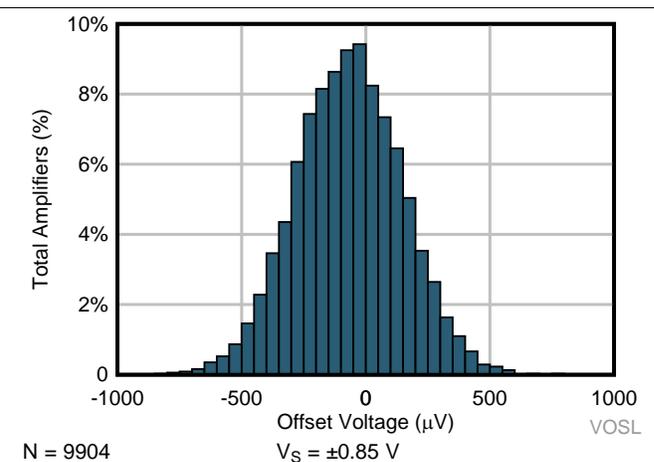
图 2. Offset Voltage Production Distribution

N = 65   vosd
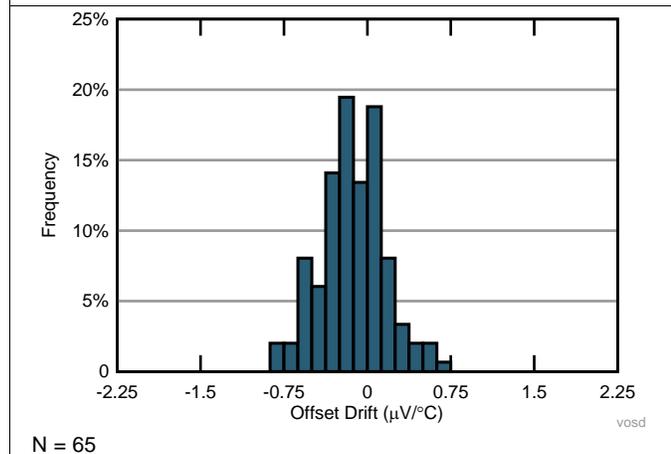
图 3. Offset Voltage Drift Distribution

N = 5   vosv
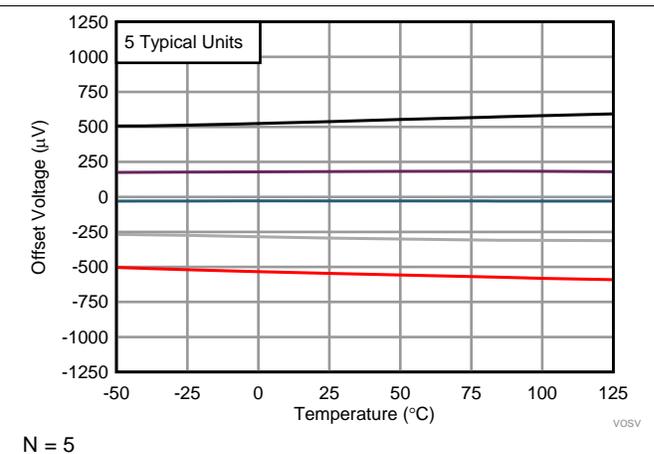
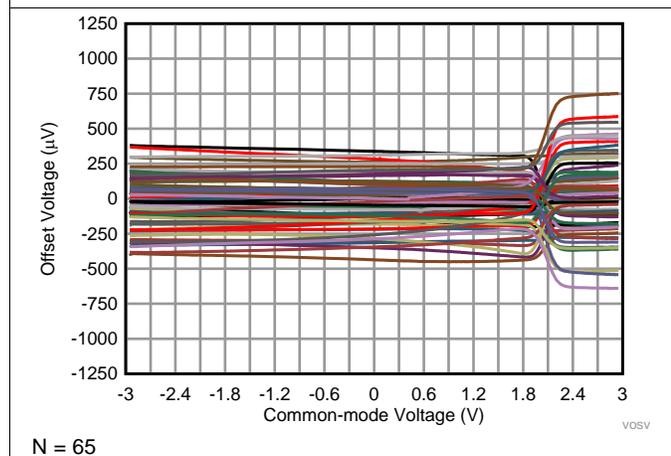图 4. Offset Voltage vs. Temperature

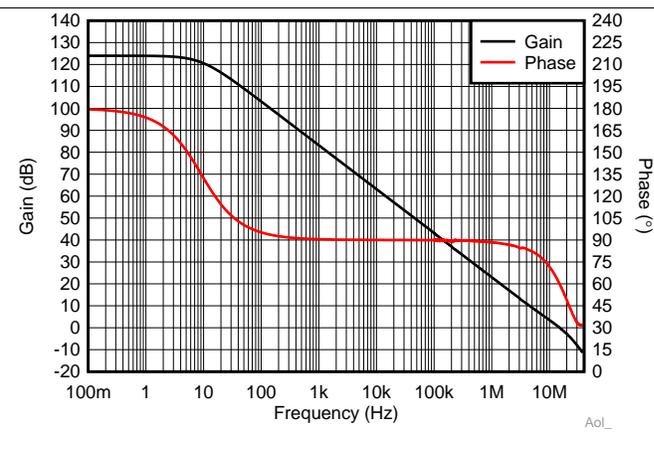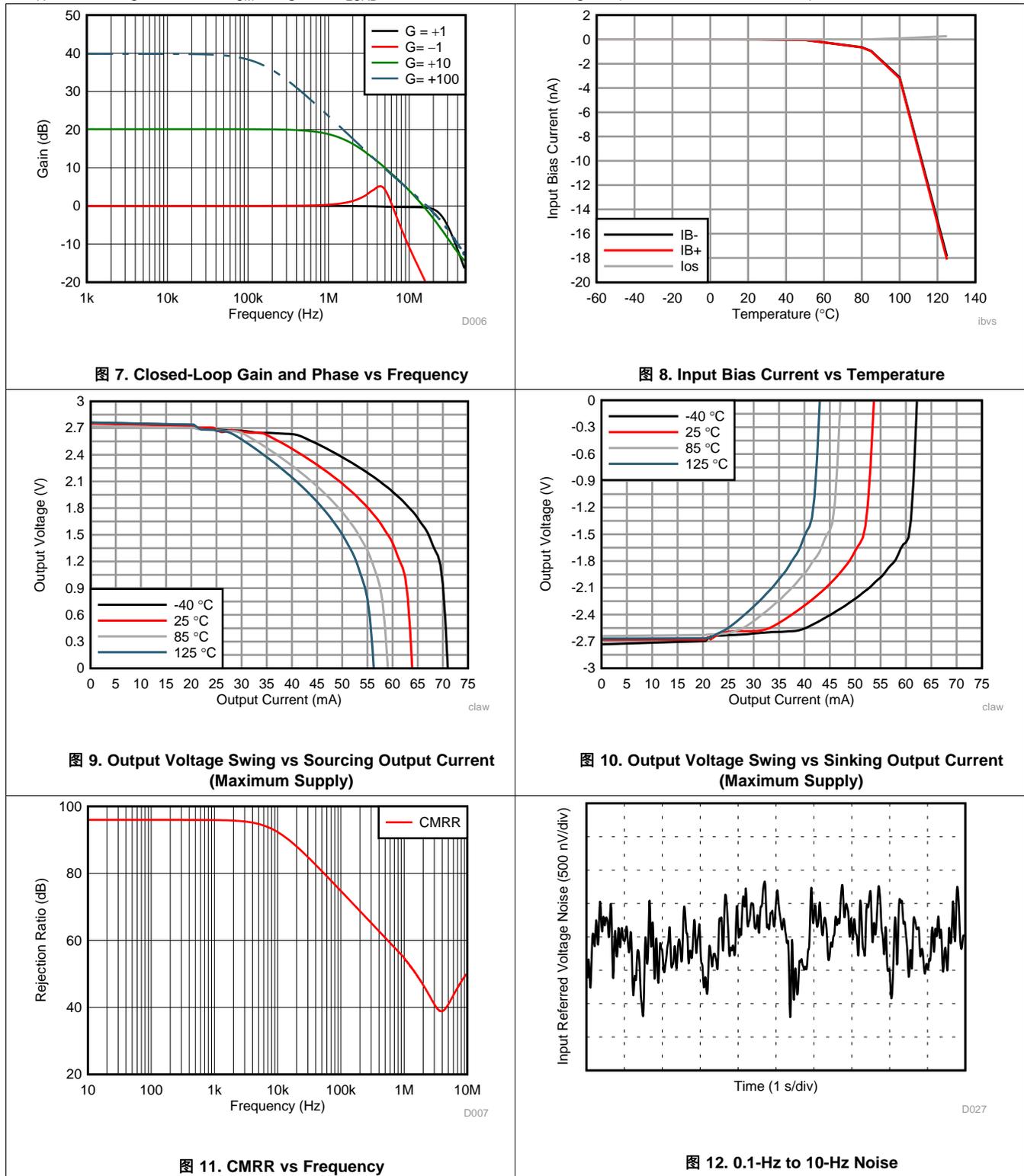

N = 65   vosv

图 5. Offset Voltage vs. Common Mode Voltage

Aol_

图 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (接下页)

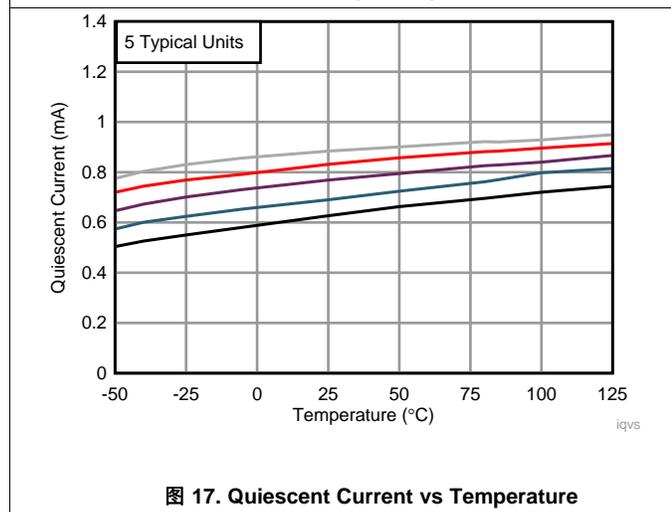at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

图 7. Closed-Loop Gain and Phase vs Frequency

图 8. Input Bias Current vs Temperature

图 9. Output Voltage Swing vs Sourcing Output Current
(Maximum Supply)

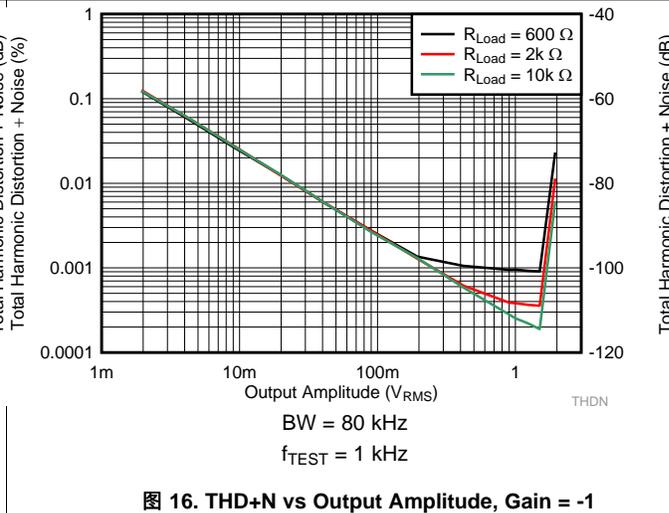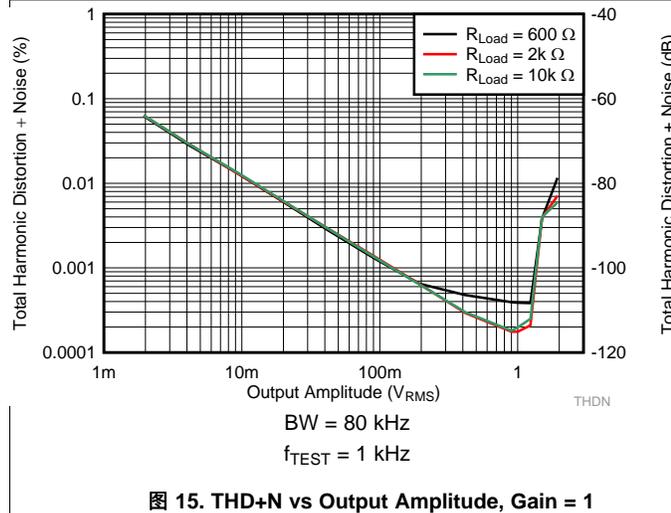图 10. Output Voltage Swing vs Sinking Output Current
(Maximum Supply)

图 11. CMRR vs Frequency

图 12. 0.1-Hz to 10-Hz Noise

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

图 13. Input Voltage Noise Spectral Density vs Frequency

图 14. THD+N Ratio vs Frequency

BW = 80 kHz

V_O = 1 V_{RMS}

图 15. THD+N vs Output Amplitude, Gain = 1

BW = 80 kHz

f_{TEST} = 1 kHz

图 16. THD+N vs Output Amplitude, Gain = -1

BW = 80 kHz

f_{TEST} = 1 kHz

图 17. Quiescent Current vs Temperature

图 18. Quiescent Current vs Supply

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

图 19. Open-Loop Gain vs Temperature

图 20. Open-Loop Output Impedance vs Frequency

图 21. Small-Signal Overshoot vs Capacitive Load
(10-mV Step)

图 22. No Phase Reversal

图 23. Positive Overload Recovery

图 24. Negative Overload Recovery

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

G = +1

图 25. Small-Signal Step Response (10-mV Step)
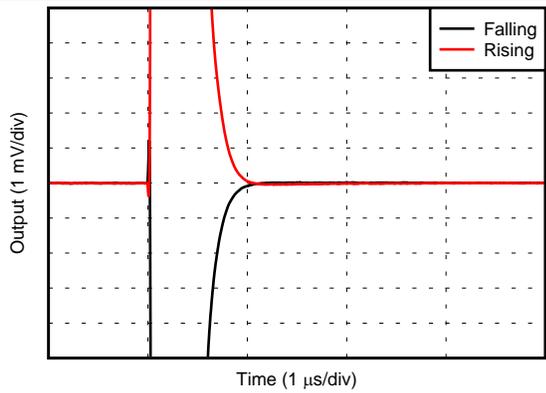

G = −1

图 26. Small-Signal Step Response (10-mV Step)
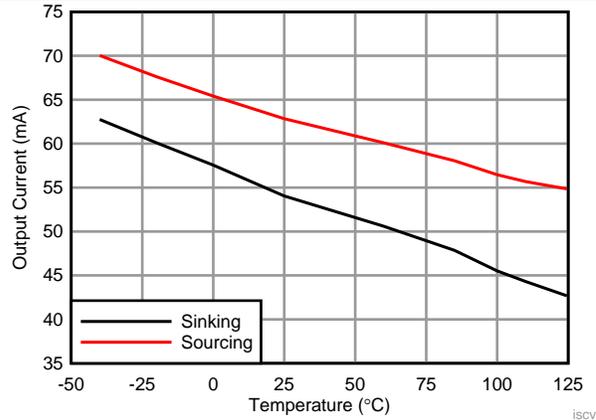

图 27. Settling Time (2-V Step)

图 28. Short-Circuit Current vs Temperature
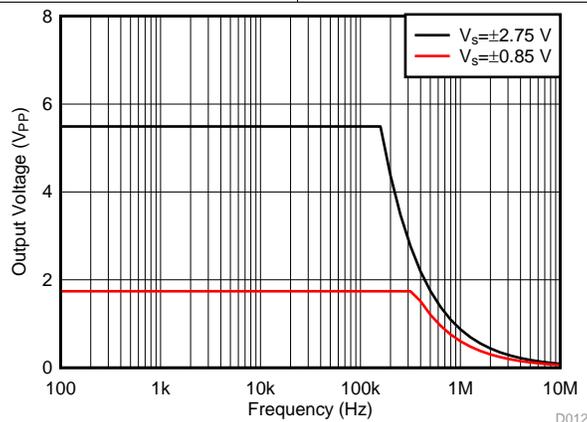
图 29. Maximum Output Voltage vs Frequency

7 Detailed Description

7.1 Overview

The OPA1671 is a rail-to-rail input, very low noise operational amplifier (op amp). The OPA1671 operates from 1.7 V to 5.5 V, is unity-gain stable, and is suitable for a wide range of audio and general-purpose applications. The OPA1671 strengths also include 13-MHz bandwidth, 4.0-nV/√Hz noise spectral density, with very low input bias current (10 pA), making the OPA1671 optimal for a preamplifier in microphone circuits, sensor modules and buffering high-fidelity, digital-to-analog converters (DACs).

7.2 Functional Block Diagram
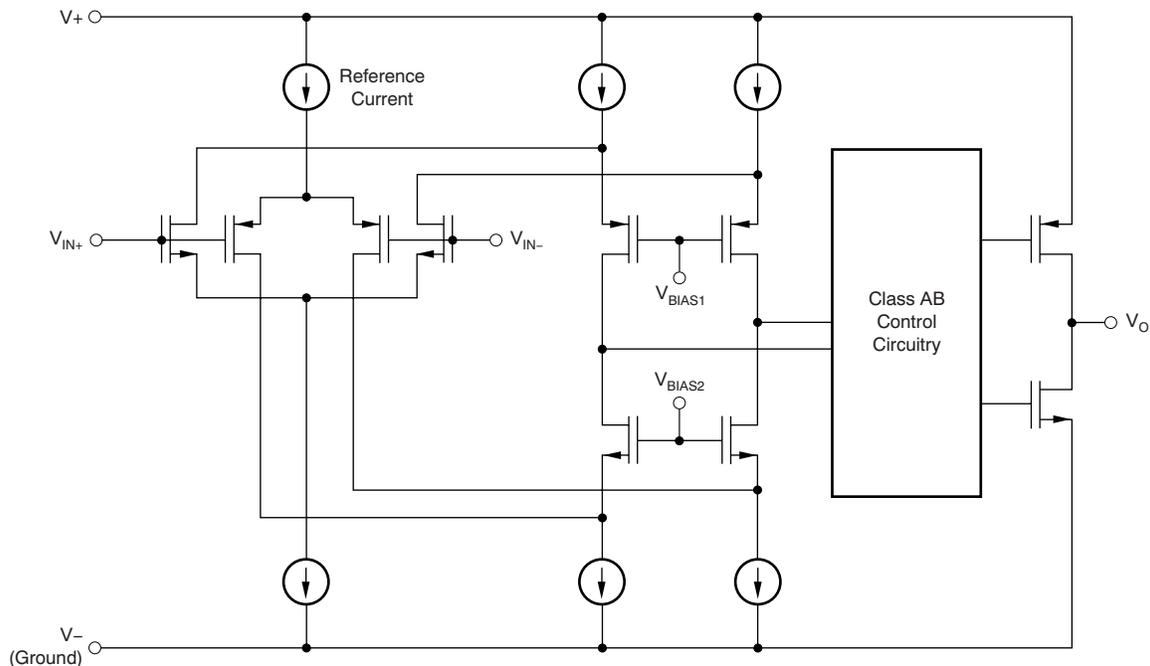
7.3 Feature Description

7.3.1 Operating Voltage

The OPA1671 op amp can be used with single or dual supplies from an operating range of V_S = 1.7 V (±0.85 V) up to 5.5 V (±2.75 V). Supply voltages greater than 6 V can permanently damage the device (see *Absolute Maximum Ratings*). Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section.

Feature Description (接下页)

7.3.2 Input Bias Current

Typically, input bias current is approximately ±10 pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in 图 30.

Unlike many operational amplifiers, there are no diodes connected between the positive and negative input terminals. As a result, differential voltages up to the full supply voltage will not cause any significantly higher current flow into the inputs.
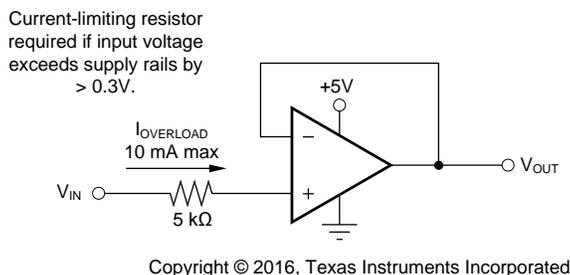
Current-limiting resistor required if input voltage exceeds supply rails by > 0.3V.

$I_{OVERLOAD}$ 10 mA max

V_{IN}

+5V

V_{OUT}

5 kΩ

Copyright © 2016, Texas Instruments Incorporated

图 30. Input Current Protection

7.3.3 Common-Mode Voltage Range

The OPA1671 features true rail-to-rail inputs, allowing full common mode operation from the negative supply voltage to the positive supply voltage. This is achieved with complimentary N-channel and P-channel differential input pairs. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.25 V to (V+) The P-channel is active for common-mode inputs from (V-) to (V+) – 1.25 V. There is a small transition region, typically from (V+) – 1.25 V to (V+) – 1 V. In this region, the offset voltage will transition between the P-channel and N-channel offset values. The difference between offset in the P and N regions can be seen in 图 5.

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA1671 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz (–3 dB), with a rolloff of 20 dB per decade.
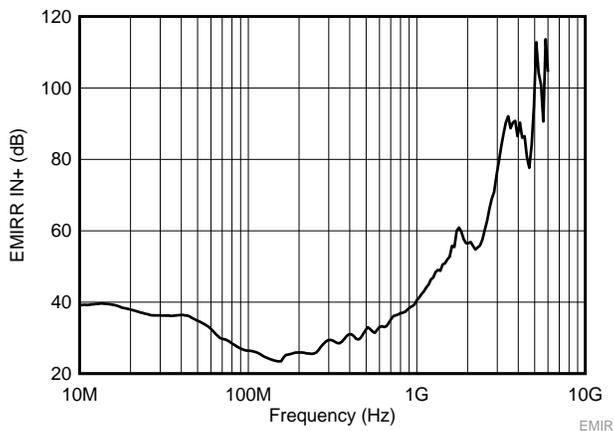
图 31. OPA1671 EMIRR vs. Frequency

Feature Description (接下页)

表 1. OPA1671 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	30 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	38 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	60 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	59 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	90 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100 dB

7.4 Device Functional Modes

The OPA1671 has a single functional mode and is operational when the power-supply voltage is greater than 1.7 V (±0.85 V). The maximum specified power-supply voltage for the OPA1671 is 5.5 V (±2.75 V).

8   Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1   Application Information

The OPA1671 is a low-noise, rail-to-rail input and output operational amplifier specifically designed for portable applications. The device operates from 1.7 V to 5.5 V, is unity-gain stable, and suitable for a wide range of audio and general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA1671 device to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving sampling analog-to-digital converters (ADCs)..

8.1.1   Capacitive Loads

The dynamic characteristics of the OPA1671 amplifiers are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. Add a small resistor (R_S equal to 50 Ω, for example) in series with the output to isolate heavier capacitive loads.

8.1.2   Noise Performance

图 31 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The op amp itself contributes a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. For a CMOS-input device, the noise resulting from the input current is negligible, therefore the total noise is dominated by the voltage noise of the OPA1671 at low source resistance, and the resistor noise above 1 kΩ.

图 31 shows the calculation of the total circuit noise, with these parameters:

* e_n = voltage noise
* R_S = source impedance
* k = Boltzmann's constant = 1.38×10^{-23} J/K
* T = temperature in degrees Kelvin (K)

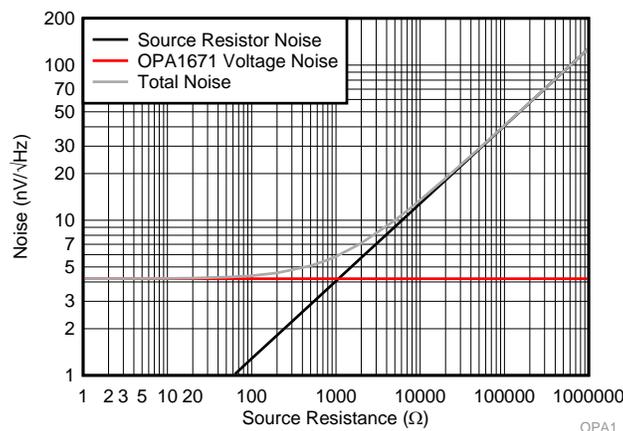For more details on calculating noise, see *Basic Noise Calculations*.

图 32. Noise Performance of the OPA1671 in a Unity-Gain Buffer Configuration

Application Information (接下页)

8.1.3 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in 图 31. The source impedance is typically fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

图 33 shows noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components.

The selected feedback resistor values make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration

Noise at the output is given as E_O, where
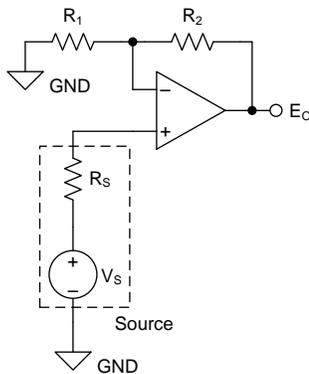
(1) $E_O = \left(1 + \dfrac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\dfrac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2}$ $[\,V_{RMS}\,]$

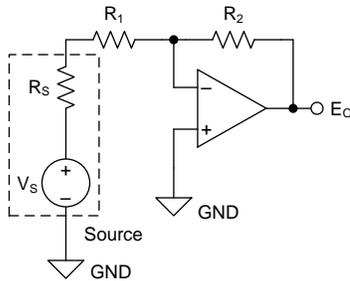(2) $e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S}$ $\left[\dfrac{V}{\sqrt{Hz}}\right]$ Thermal noise of R_S

(3) $e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\dfrac{R_1 \cdot R_2}{R_1 + R_2}\right]}$ $\left[\dfrac{V}{\sqrt{Hz}}\right]$ Thermal noise of $R_1 \| R_2$

(4) $k_B = 1.38065 \cdot 10^{-23}$ $\left[\dfrac{J}{K}\right]$ Boltzmann Constant

(5) $T(K) = 237.15 + T(°C)$ $[\,K\,]$ Temperature in kelvins

(B) Noise in Inverting Gain Configuration

Noise at the output is given as E_O, where

(6) $E_O = \left(1 + \dfrac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\dfrac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2}$ $[\,V_{RMS}\,]$

(7) $e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\dfrac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]}$ $\left[\dfrac{V}{\sqrt{Hz}}\right]$ Thermal noise of $(R_1 + R_S) \| R_2$

(8) $k_B = 1.38065 \cdot 10^{-23}$ $\left[\dfrac{J}{K}\right]$ Boltzmann Constant

(9) $T(K) = 237.15 + T(°C)$ $[\,K\,]$ Temperature in kelvins

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(1) e_N is the voltage noise of the amplifier. For the OPA1671 series of operational amplifiers, e_N = 4.0 nV/√Hz at 10 kHz.

(2) i_N is the current noise of the amplifier. For the OPA1671 series of operational amplifiers, i_N = 4.5 fA/√Hz at 1 kHz.

(3) For additional resources on noise calculations, see *TI's Precision Labs Series*.

图 33. Noise Calculation in Gain Configurations

8.2 Typical Application

This design uses an OPA1671 as a pre-amplifier for an electret microphone. Electret microphone types are common in many audio applications of varying performance levels. The OPA1671 offers very low noise in a tiny package, and is well-suited for use in electret pre-amplifier circuits.
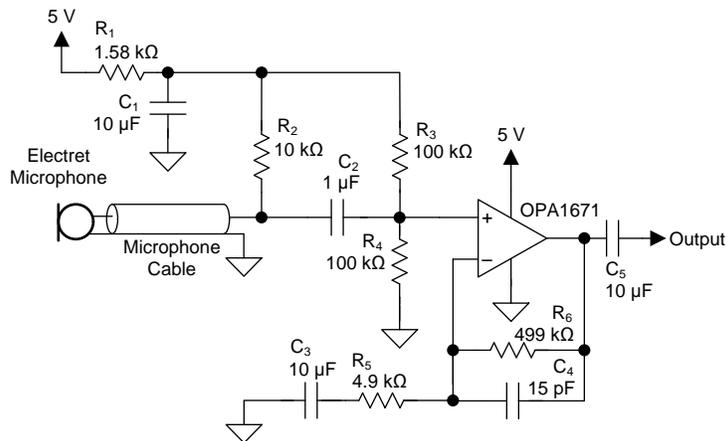
图 34 shows the solution.

图 34. Electret Pre-Amplifier Schematic

8.2.1 Design Requirements

This solution has the following requirements:
- Supply voltage: 5 V
- Gain: 100 V/V
- Frequency response: 3 dB from 20 Hz to 20 kHz
- Output: 2.5 V ±1 V
- Output noise density: <1 µV/Rt(Hz) at 10 kHz

Typical Application (接下页)

8.2.2 Detailed Design Procedure

The preamplifier circuit uses a non-inverting gain configuration to allow for high input impedance, with independent gain-setting resistor values. DC bypass is accomplished with C_2 and C_3 µF capacitors, with the low frequency poles set by C_2, R_4, C_3 and R_5, see equations 公式 1 and 公式 2.

$$p_{L1} = \frac{1}{2\pi \cdot (R_3 \| R_4) \cdot C_2} = 3.18 \text{ Hz}$$

(1)

$$p_{L2} = \frac{1}{2\pi \cdot R_5 \cdot C_3} = 3.23 \text{ Hz}$$

(2)

The filter cutoff frequency is determined by a higher frequency pole, set by R_5 and C_4.

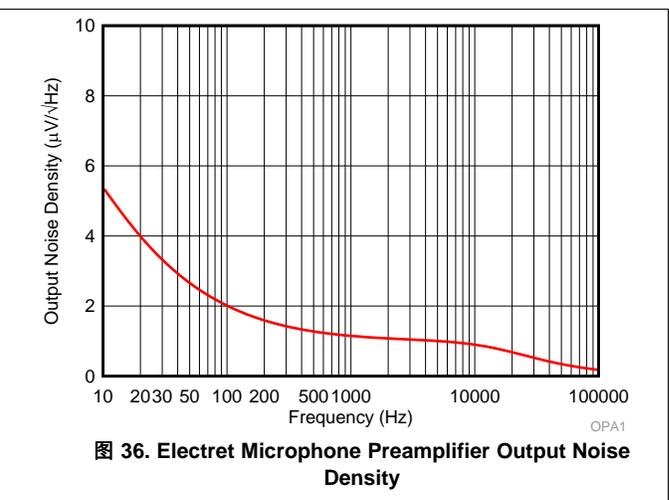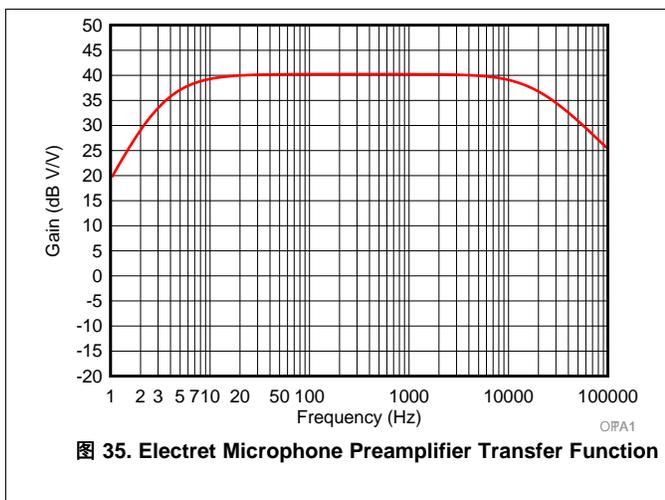$$p_H = \frac{1}{2\pi \cdot R_6 \cdot C_4} = 21.3 \text{ kHz}$$

(3)

The gain of the circuit in the passband is set by R_5 and R_6.

$$A \text{ (V/V)} = \frac{R_6}{R_5} = 100 \text{ (40 dB)}$$

(4)

The ouput noise of the circuit (ignoring the electret microphone intrinsic noise and impedance) will be the RSS average noise contribution from R_5 and the input voltage noise of OPA1671. R_5 was selected for minimal noise contribution without requiring a DC blocking cap. (C3) larger than 10 µF. See 公式 5 for the output noise density calculation at 10 kHz.

$$e_{N\_OUT} = \text{Input Referred Noise} \cdot \text{Gain} = \sqrt{(4kTR_5)^2 + V_{N\_10k}^2} \cdot 100 = 0.96 \text{ µV/}\sqrt{\text{Hz}}$$

(5)

8.2.3 Application Curves

图 35. Electret Microphone Preamplifier Transfer Function

图 36. Electret Microphone Preamplifier Output Noise Density

9 Power Supply Recommendations

The OPA1671 device is specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.75 V).

10 Layout

10.1 Layout Guidelines

Paying attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.
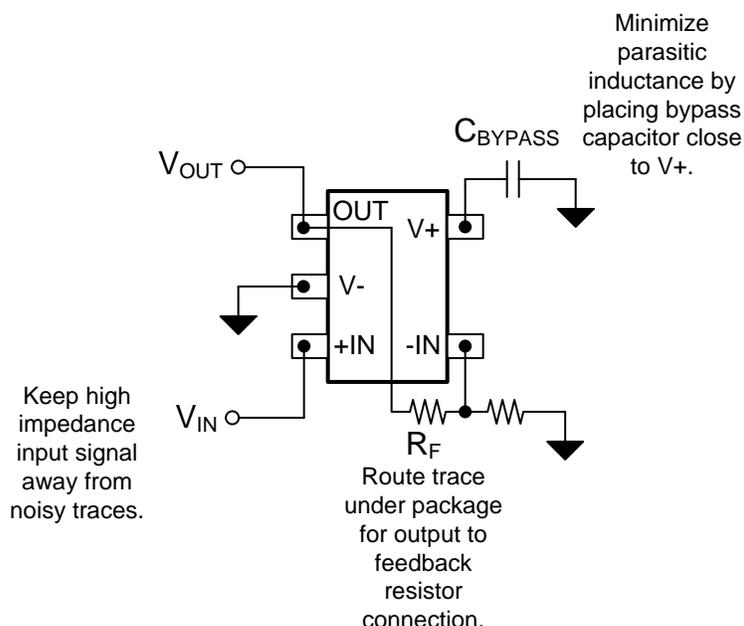
10.2 Layout Example

图 **37. OPA1671 Layout Example**

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 *TINA-TI™*（免费软件下载）

TINA-TI™ 是一款基于 SPICE 引擎的电路仿真程序，简单易用并且功能强大。TINA-TI™ 是 TINA™软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI™ 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI™ 提供全面的后处理能力，便于用户以多种方式获得结果，用户可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的功能，从而构建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI™ 软件。请下载 TINA-TI™ 文件夹中的免费 TINA-TI™ 软件。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：
* 《电路板布局布线技巧》
* 《模拟工程师电路设计指导手册》

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表。*

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1671IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1D3	Samples
OPA1671IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1D3	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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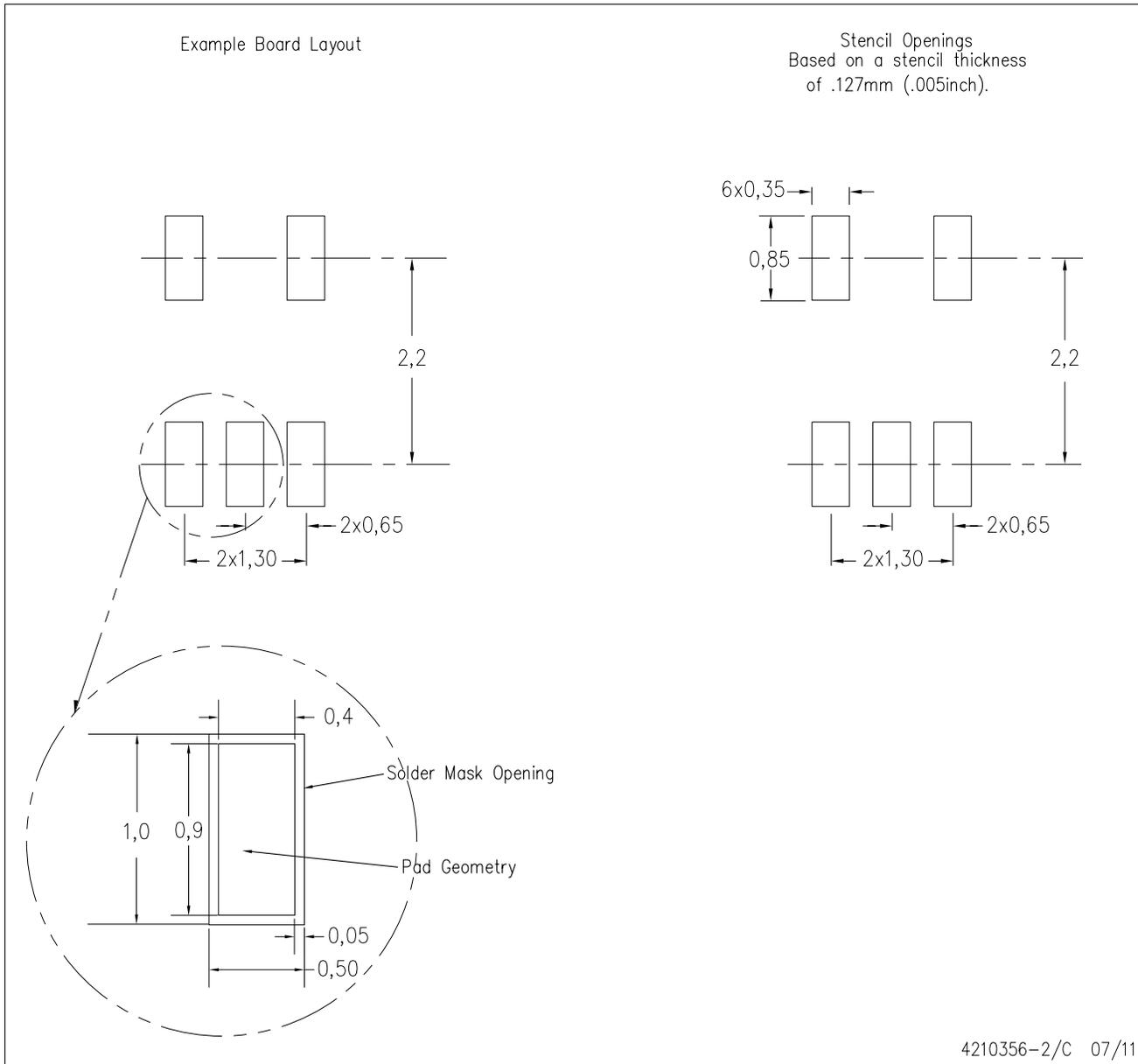
DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE
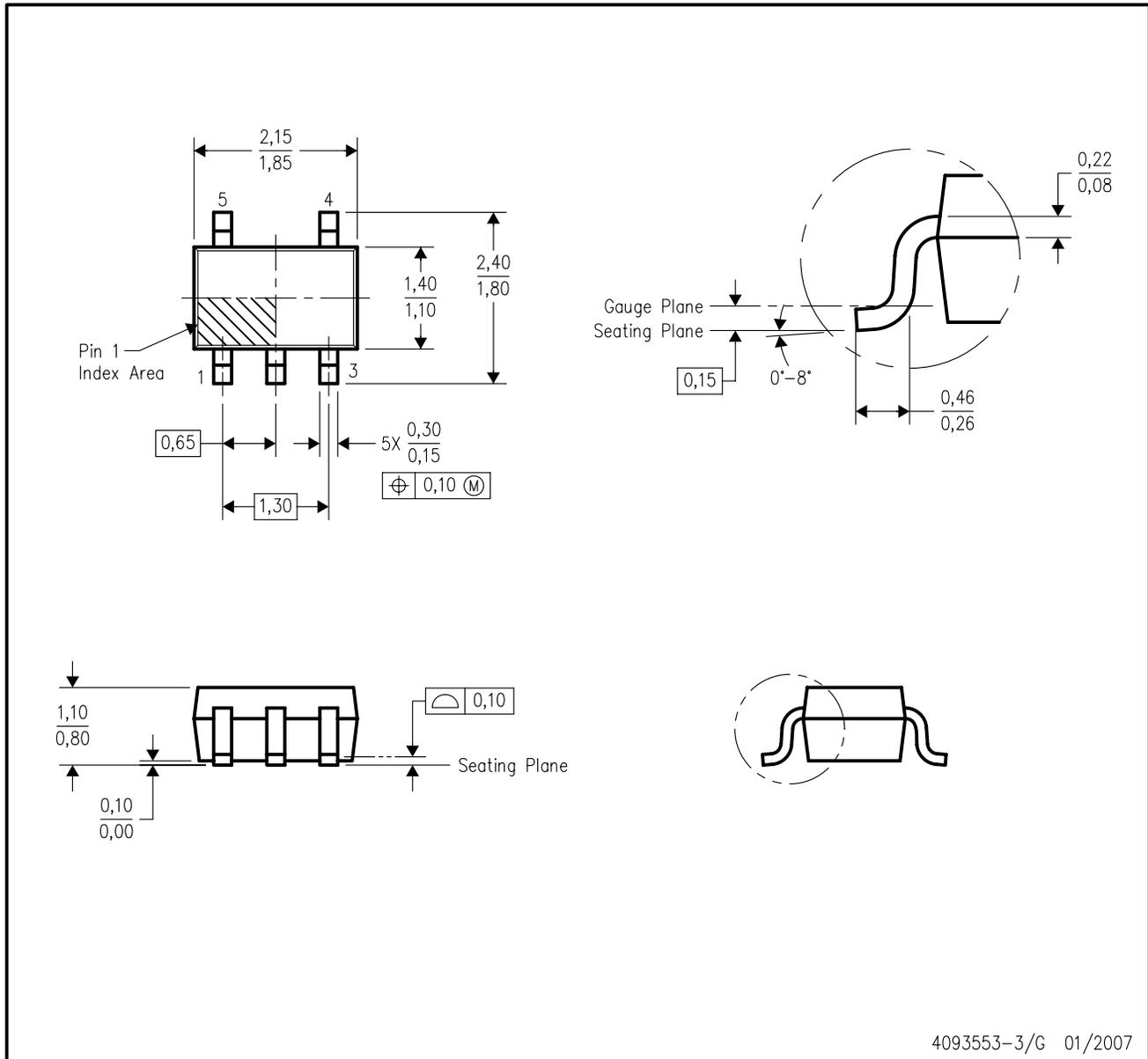
4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

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DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x1,30

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.