OPA2210 2.2nV/√Hz 精密、低功耗、36V 运算放大器

1 特性

- 精密超级 ß 性能：
  - 低失调电压：5μV（典型值）
  - 超低漂移：0.1μV/°C（典型值）
  - 低输入偏置电流：0.3nA（典型值）
- 超低噪声：
  - 0.1Hz 至 10Hz 低噪声：90nV$_{PP}$
  - 低电压噪声：1kHz 时为 2.2nV/√Hz
- 高 CMRR：132dB（最小值）
- 增益带宽积：18MHz
- 压摆率：6.4V/μs
- 低静态电流：2.5mA/通道（最大值）
- 短路电流：±65mA
- 宽电源范围：±2.25V 至 ±18V
- 无相位反转
- 轨至轨输出

2 应用

- 超声波扫描仪
- 医疗器械
- 商用网络和服务器 PSU
- 半导体测试设备
- PLL 回路滤波器
- 实验室仪表
- 高性能 ADC 驱动器
- 高性能 DAC 输出放大器
- 专业音频前置放大器

3 说明

OPA2210 是 OPA2209 运算放大器的下一代产品。OPA2210 精密运算放大器基于 TI 的精密超级 ß 互补双极半导体工艺进行构建，从而可提供超低闪烁噪声、低失调电压和低失调电压温漂。

OPA2210 可实现极低的电压噪声密度 (2.2nV/√Hz)，同时每个放大器仅消耗 2.5mA（最大值）的电流。该器件还提供轨至轨输出摆幅，从而有助于最大限度地扩大动态范围。

在精密数据采集 应用中，OPA2210 可实现精度达 16 位的快速建立时间，即使对于 10V 输出摆幅也是如此。出色的交流性能以及仅 35μV（最大值）的失调和 0.6μV/°C（最大值）的温漂使 OPA2210 非常适合高速、高精度 应用。

OPA2210 可在 ±2.25V 至 ±18V 的宽双电源电压范围或 4.5V 至 36V 的宽单电源电压范围内运行，并且具有 –40°C 至 125°C 的额定工作温度范围。

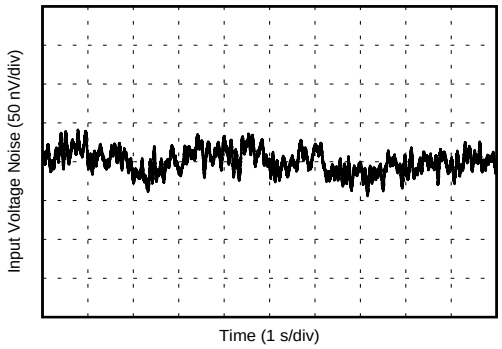
OPA2210 采用 8 引脚 VSSOP 封装。

器件信息(1)

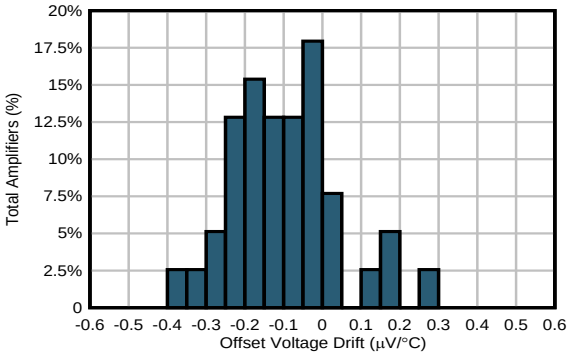
器件型号	封装	封装尺寸（标称值）
OPA2210	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

OPA2210 0.1Hz 至 10Hz 噪声



OPA2210 失调电压漂移分布图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2018) to Revision B **Page**

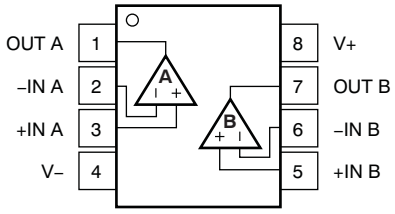
- 已更改 "OPAx145" to "OPA2210" 16
- Fixed link to TIDA-01427 21

Changes from Original (September 2018) to Revision A **Page**

- 首次发布生产数据数据表 1

5 Pin Configuration and Functions

OPA2210: DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2210

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)			40	V
	Signal input pins(2)		(V–) – 0.5	(V+) + 0.5	V
	Signal input pins	Differential		1	V
Current	Signal input pins(2)		–10	10	mA
	Output short circuit(3)		Continuous		
Temperature	Junction, T_J			150	°C
	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the de vice. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) For input voltages beyond the power-supply rails, voltage orcurrent must be limited.
(3) Short circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Specified voltage, V_S	±2.25	±18	V
Specified temperature	–40	125	°C
Operating temperature, T_A	–55	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2210 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_S = ±15 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±15 V, V_{CM} = 0 V			±5	±35	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			±0.1	±0.6	µV/°C
$V_{OS\text{-matching}}$	Input offset voltage matching				±5	±35	µV
PSRR	vs power supply	V_S = ±2.25 V to ±18 V	T_A = 25°C		0.05	0.5	µV/V
			T_A = –40°C to 125°C			±1	
	Channel separation	DC			±0.1		µV/V
INPUT BIAS OPERATION							
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		±0.3	±2	nA
			T_A = –40°C to 85°C			±4	
			T_A = –40°C to 125°C			±7	
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		±0.1	±2	nA
			T_A = –40°C to 85°C			±4	
			T_A = –40°C to 125°C			±7	
NOISE							
$e_{n\ p\text{-}p}$	Input voltage noise	f = 0.1 Hz to 10 Hz			0.09		μV_{PP}
e_n	Noise density	f = 10 Hz			2.5		nV/√Hz
		f = 100 Hz			2.25		nV/√Hz
		f = 1 kHz			2.2		nV/√Hz
I_n	Input current noise density	f = 1 kHz			400		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.5		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V		132	140		dB
		(V–) + 1.5 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to 125°C		120	130		dB
INPUT IMPEDANCE							
	Differential				400 || 9		kΩ || pF
	Common-mode				10^9 || 0.5		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ	T_A = 25°C	126	132		dB
			T_A = –40°C to 125°C	120			
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_L = 600 Ω(1)	T_A = 25°C	114	120		
			T_A = –40°C to 85°C	110			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				18		MHz
SR	Slew rate				6.4		V/µs
	Phase margin (Φm)	R_L = 10 kΩ, C_L = 25 pF			80		degrees
t_S	Settling time	0.1%, G = –1, 10-V step, C_L = 100 pF			2.1		µs
		0.0015% (16-bit), G = –1, 10-V step, C_L = 100 pF			2.6		
	Overload recovery time	G = –10			0.5		µs
	Total harmonic distortion + noise (THD+N)	G = +1, f = 1 kHz, V_O = 20 V_{PP}, 600 Ω			.000025		%

(1) Temperature range limited by thermal performance of the package.

Electrical Characteristics (continued)

at V_S = ±15 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing	R_L = 10 kΩ, A_{OL} > 130 dB		(V–) + 0.2		(V+) – 0.2	V
		R_L = 600 Ω, A_{OL} > 114 dB		(V–) + 0.6		(V+) – 0.6	
		R_L = 10 kΩ, A_{OL} > 120 dB, T_A = –40°C to 125°C		(V–) + 0.2		(V+) – 0.2	
I_{SC}	Short-circuit current	V_S = ±18 V			±65		mA
C_{LOAD}	Capacitive load drive (stable operation)			See *Typical Characteristics*			
Z_O	Open-loop output impedance			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0 A	T_A = 25°C		2.2	2.5	mA
			T_A = –40°C to 125°C			3.25	

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

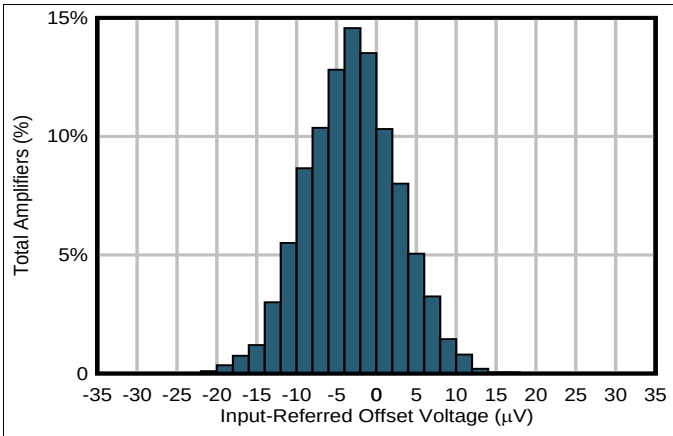


图 1. Offset Voltage Production Distribution

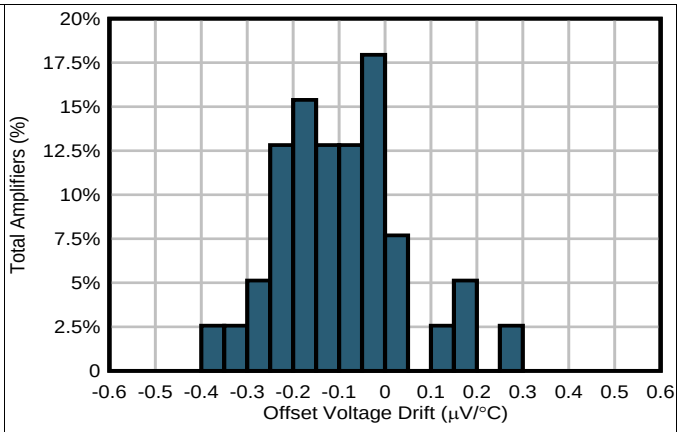


图 2. Offset Voltage Drift Distribution

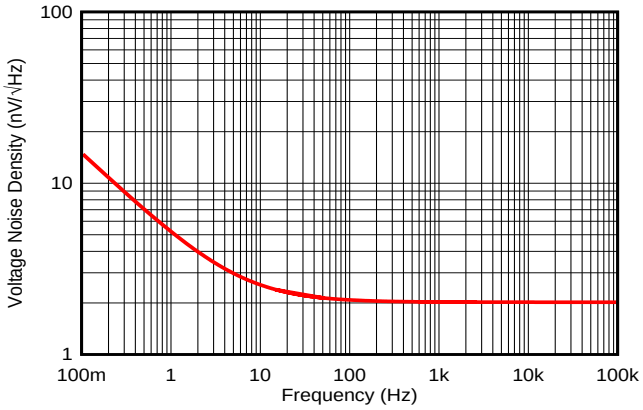


图 3. Input Voltage Noise Spectral Density vs Frequency

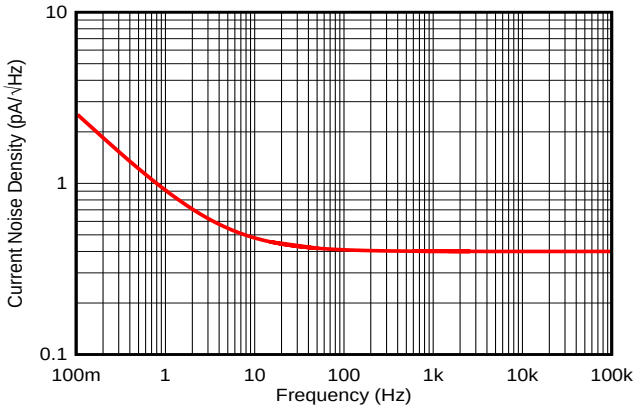


图 4. Input Current Noise Spectral Density vs Frequency

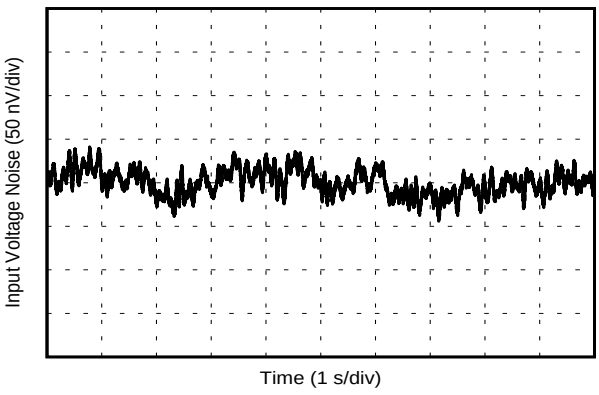
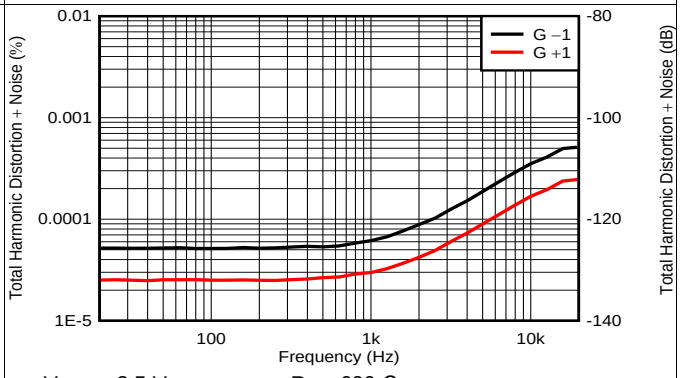


图 5. 0.1-Hz to 10-Hz Voltage Noise



V_{OUT} = 3.5 V_{RMS} R_L = 600 Ω

图 6. THD+N Ratio vs Frequency

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

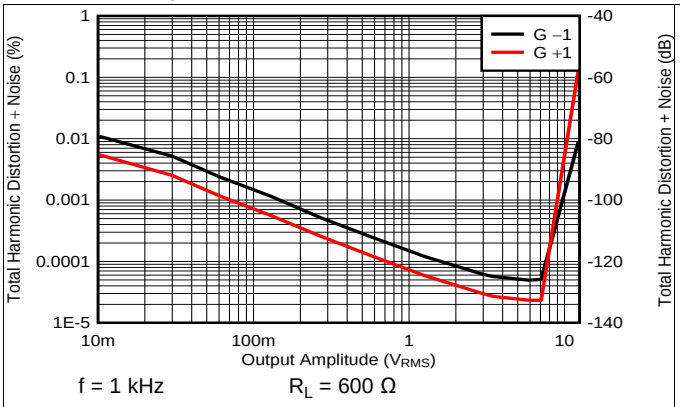


图 7. THD+N vs Output Amplitude

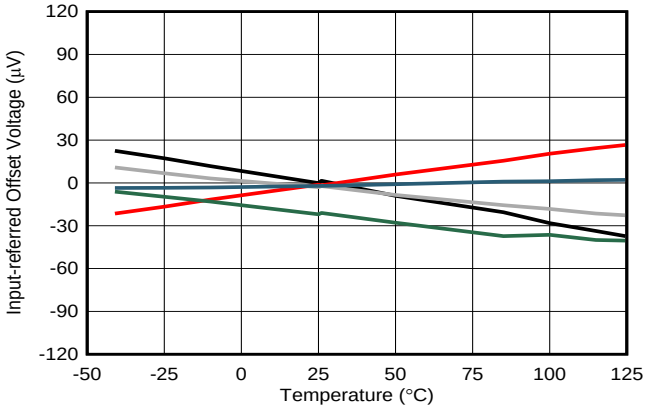


图 8. Input Offset Voltage vs Temperature

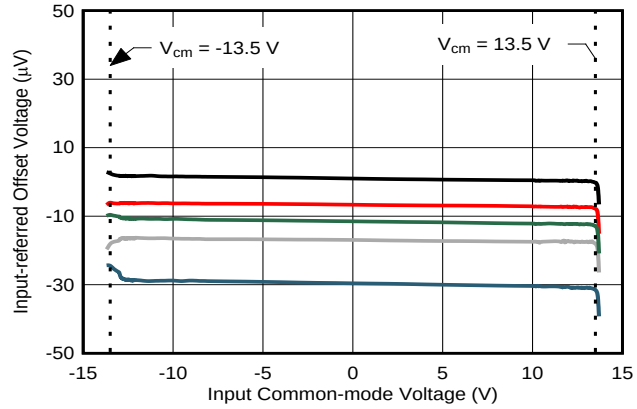


图 9. Offset Voltage vs Common-Mode Voltage

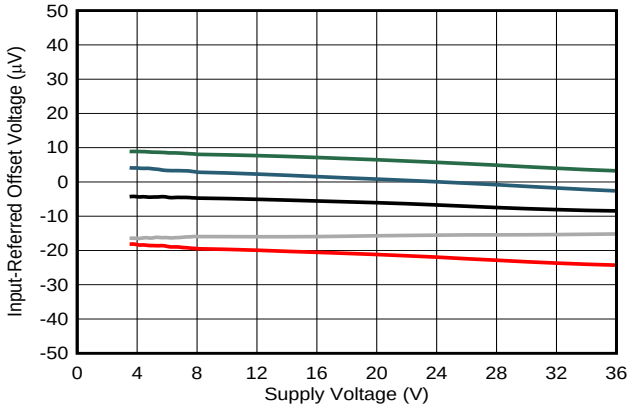


图 10. Offset Voltage vs Supply Voltage

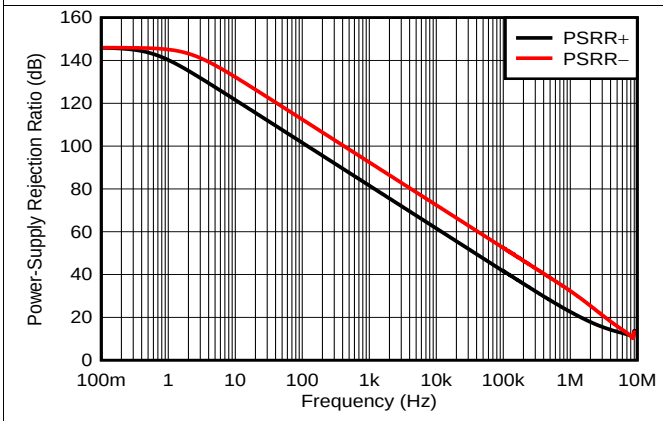


图 11. PSSR vs Frequency

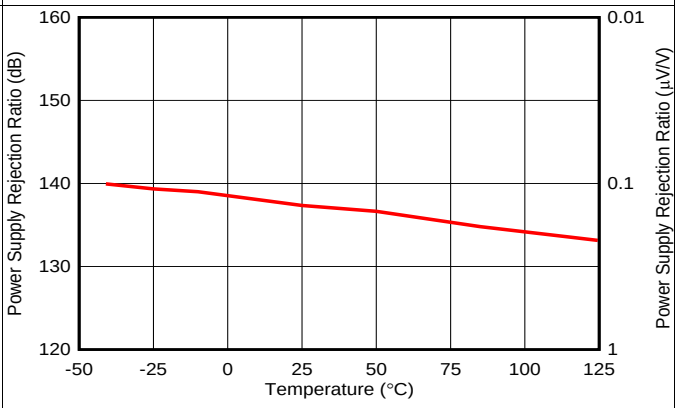


图 12. PSRR vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

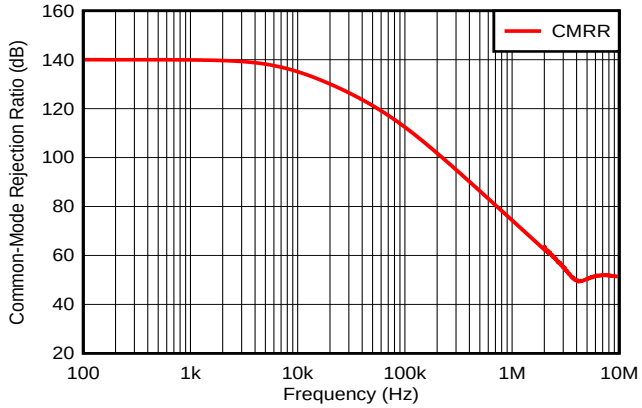


图 13. CMRR vs Frequency

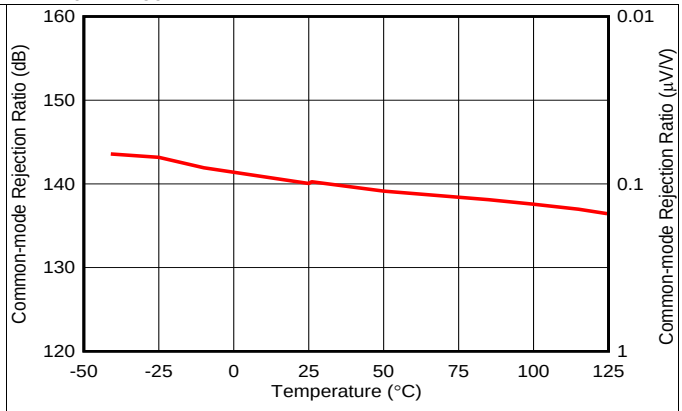


图 14. CMRR vs Temperature

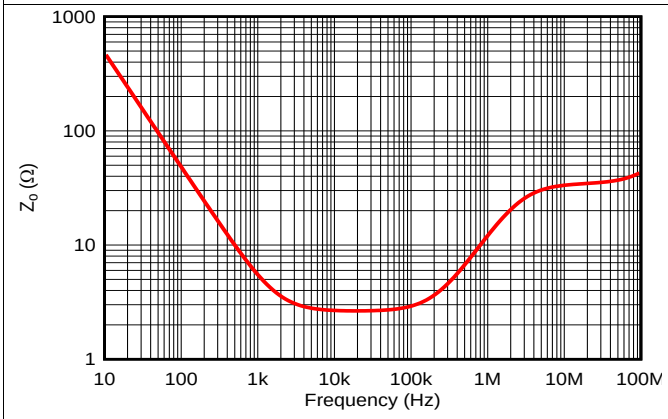


图 15. Open-Loop Output Impedance vs Frequency

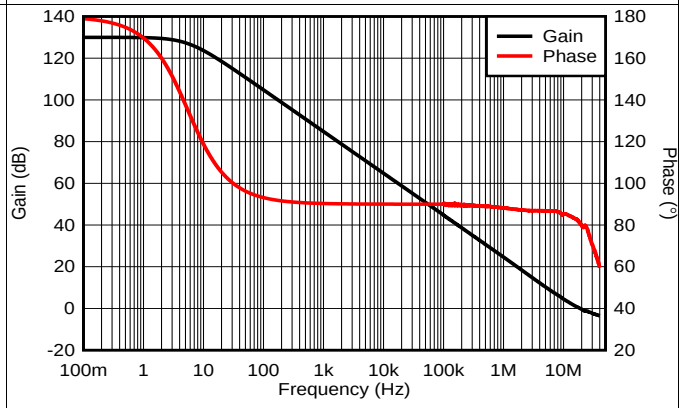


图 16. Open-Loop Gain and Phase vs Frequency

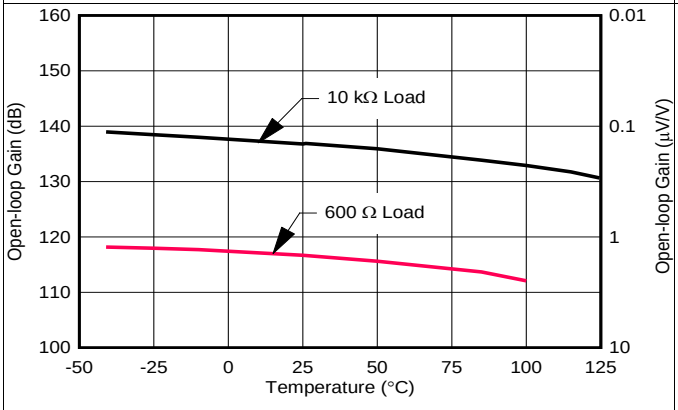


图 17. Open-Loop Gain vs Temperature

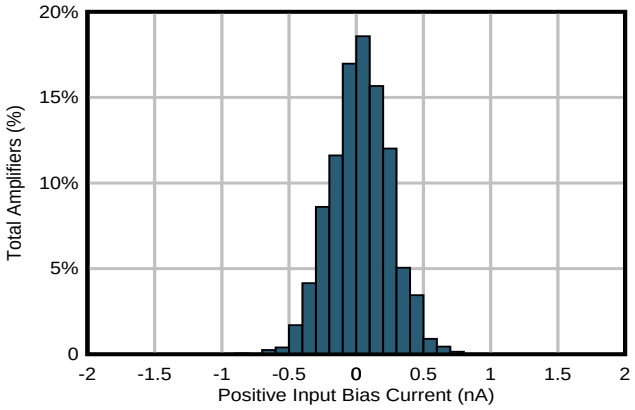


图 18. Positive Input Bias Current Production Distribution

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

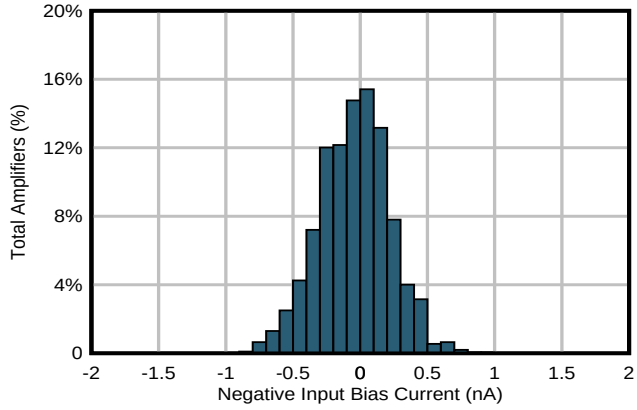


图 19. Negative Input Bias Current Production Distribution

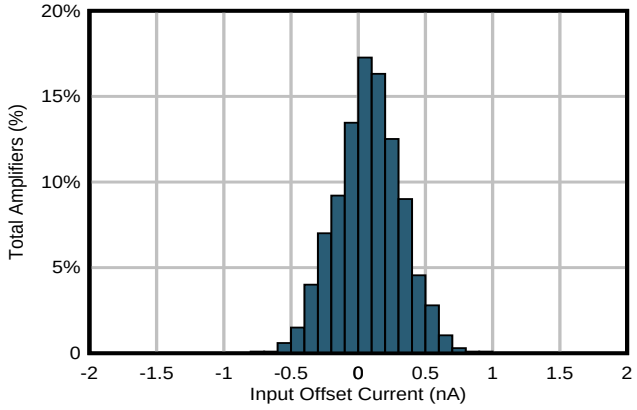


图 20. Input Offset Current Production Distribution

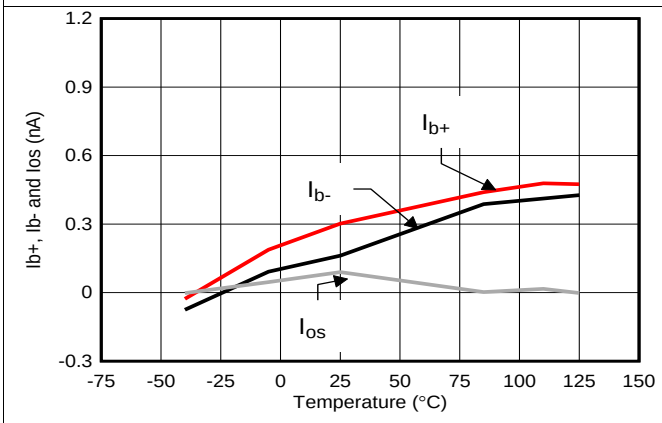


图 21. Input Bias and Input Offset Currents vs Temperature

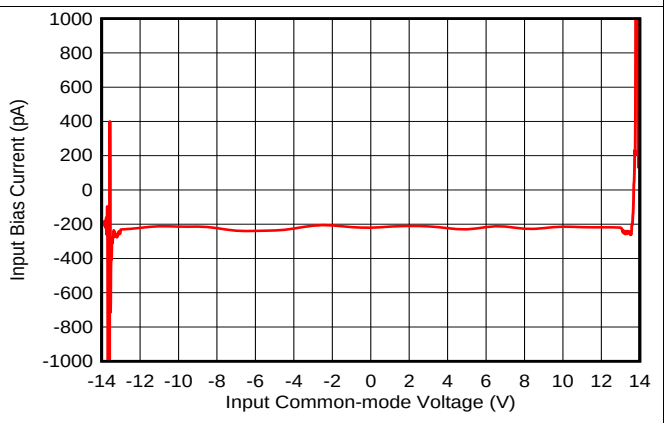


图 22. Positive Input Bias Current vs Common-Mode Voltage

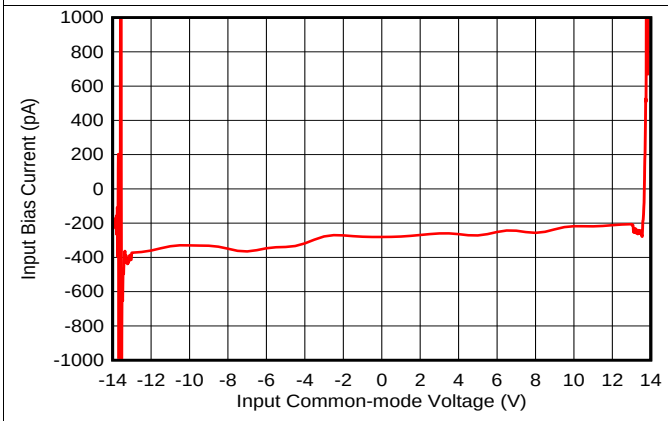


图 23. Negative Input Bias Current vs Common-Mode Voltage

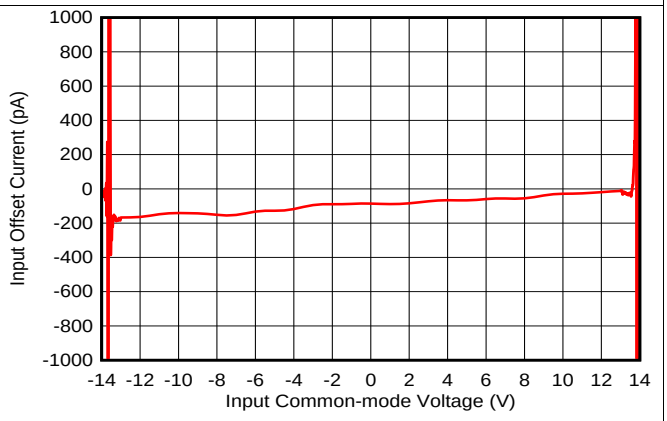


图 24. Input Offset Current vs Common-Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

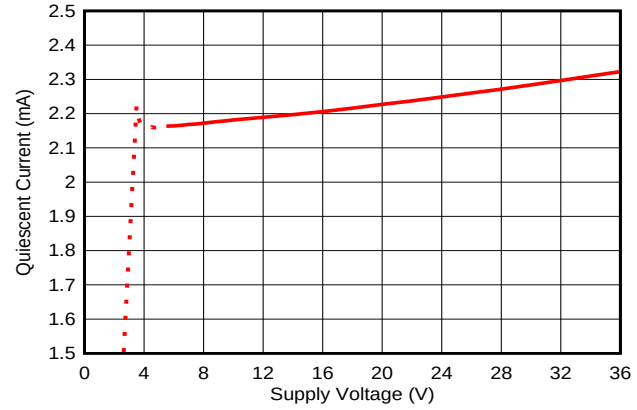


图 25. Quiescent Current vs Supply Voltage

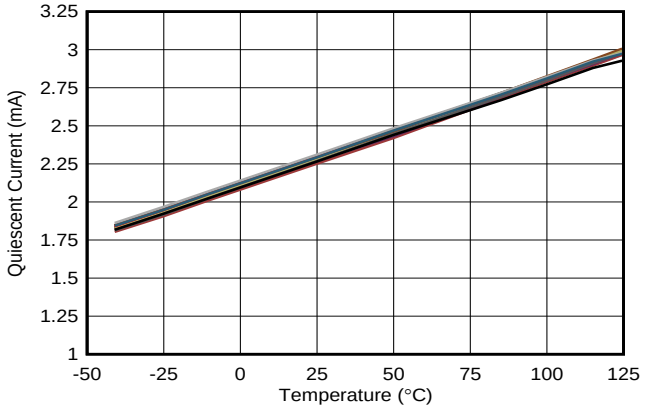


图 26. Quiescent Current vs Temperature

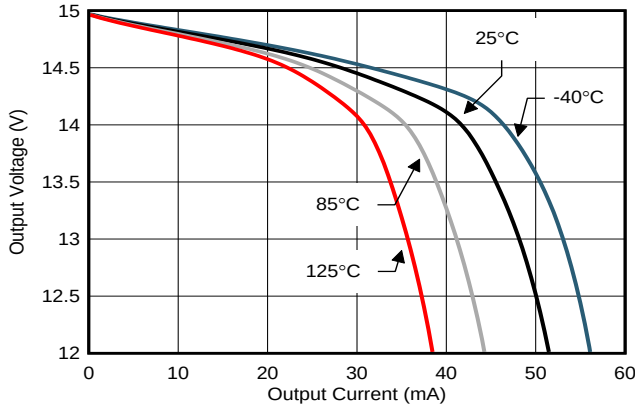


图 27. Output Voltage vs Output Current (Sourcing)

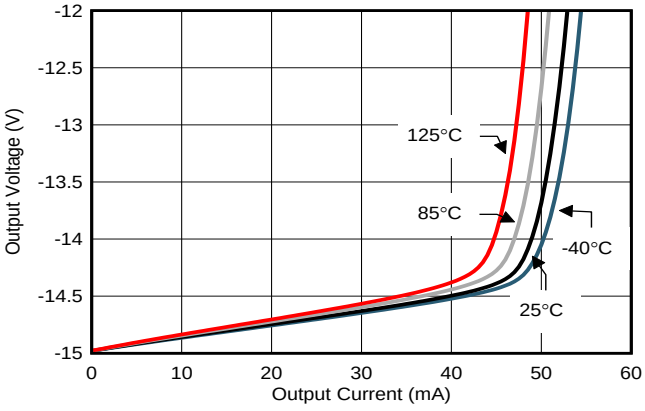


图 28. Output Voltage vs Output Current (Sinking)

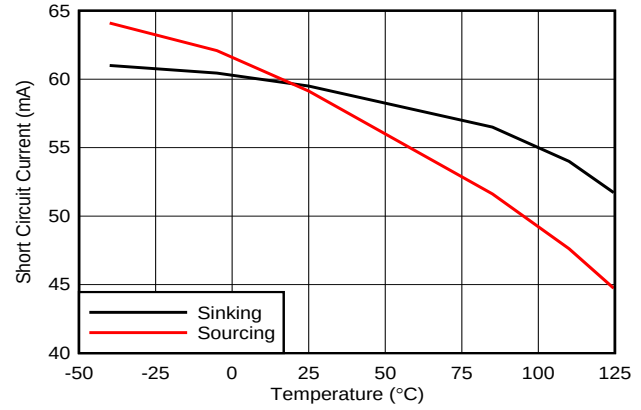


图 29. Short-Circuit Current vs Temperature

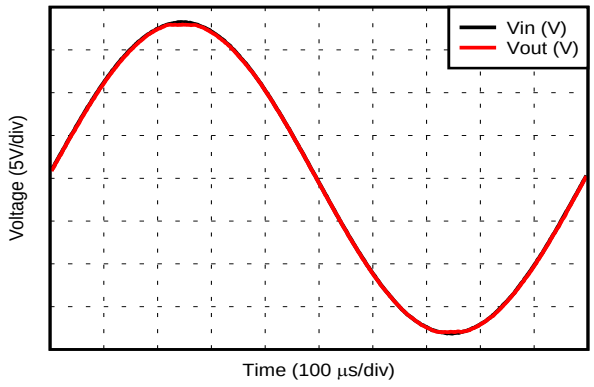
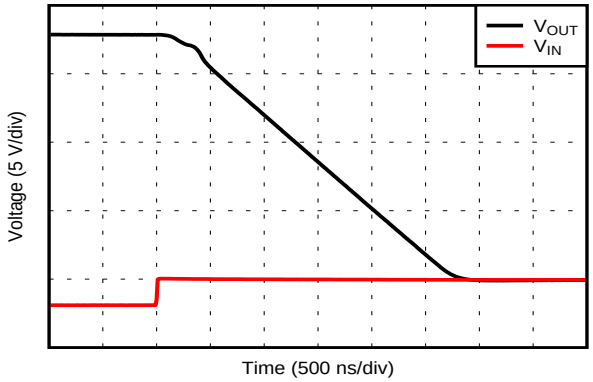


图 30. No Phase Reversal

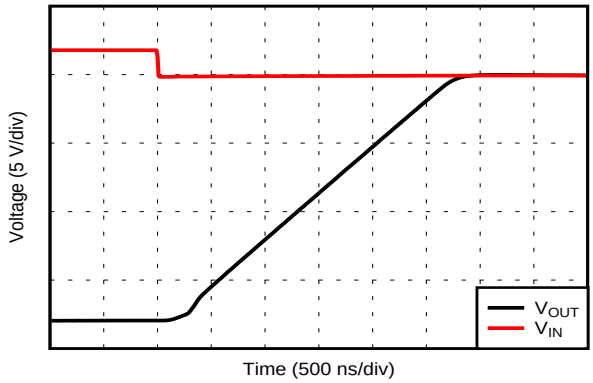
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)



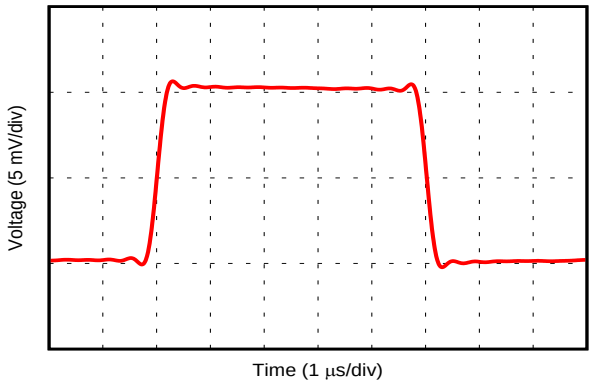
G = -10

图 31. Positive Overload Recovery



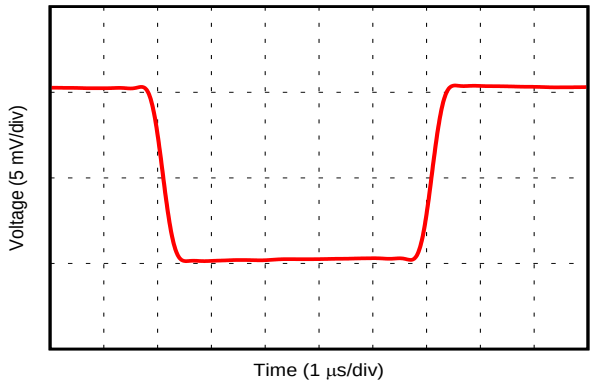
G = -10

图 32. Negative Overload Recovery



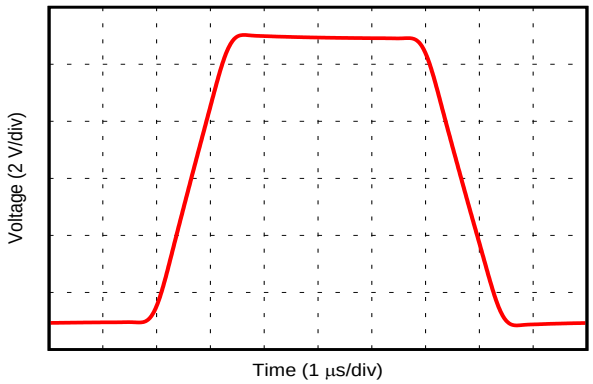
G = +1 10-mV step, C_L = 100 pF, R_L = 600 Ω

图 33. Small-Signal Step Response



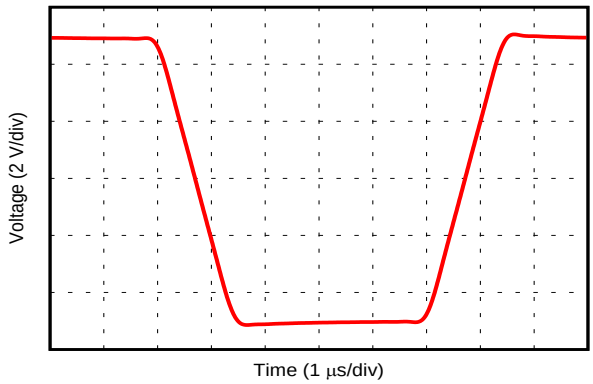
G = –1 10-mV step, C_L = 100 pF, R_L = 600 Ω

图 34. Small-Signal Step Response



G = +1 10-V step, C_L = 100 pF, R_L = 600 Ω

图 35. Large-Signal Step Response



G = –1 10-V step, C_L = 100 pF, R_L = 600 Ω

图 36. Large-Signal Step Response

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

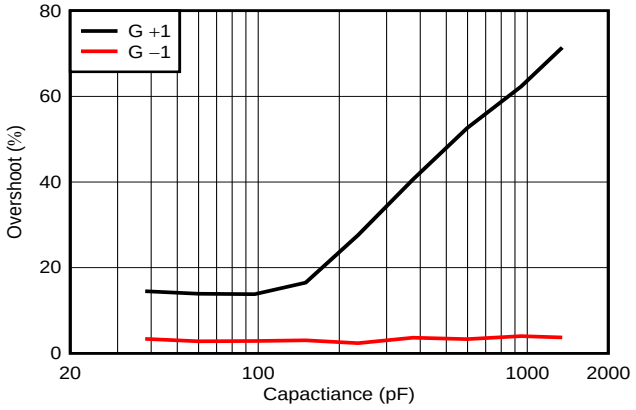
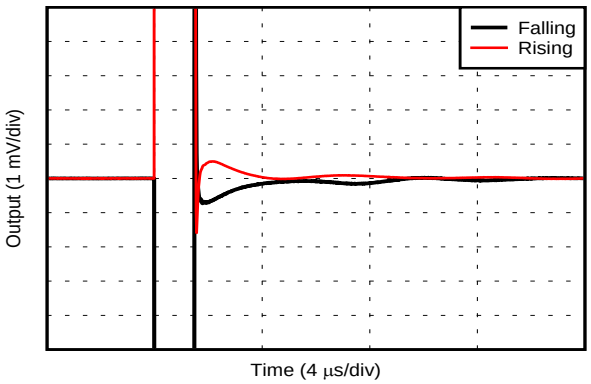
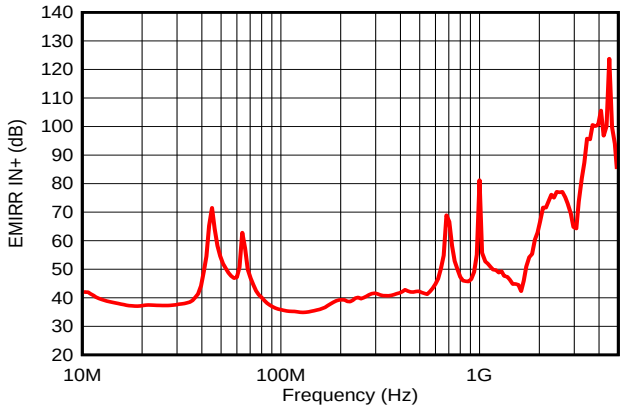


图 37. Small-Signal Overshoot vs Capacitive Load



10-V step

图 38. Settling Time



P_{RF} = –10 dBm

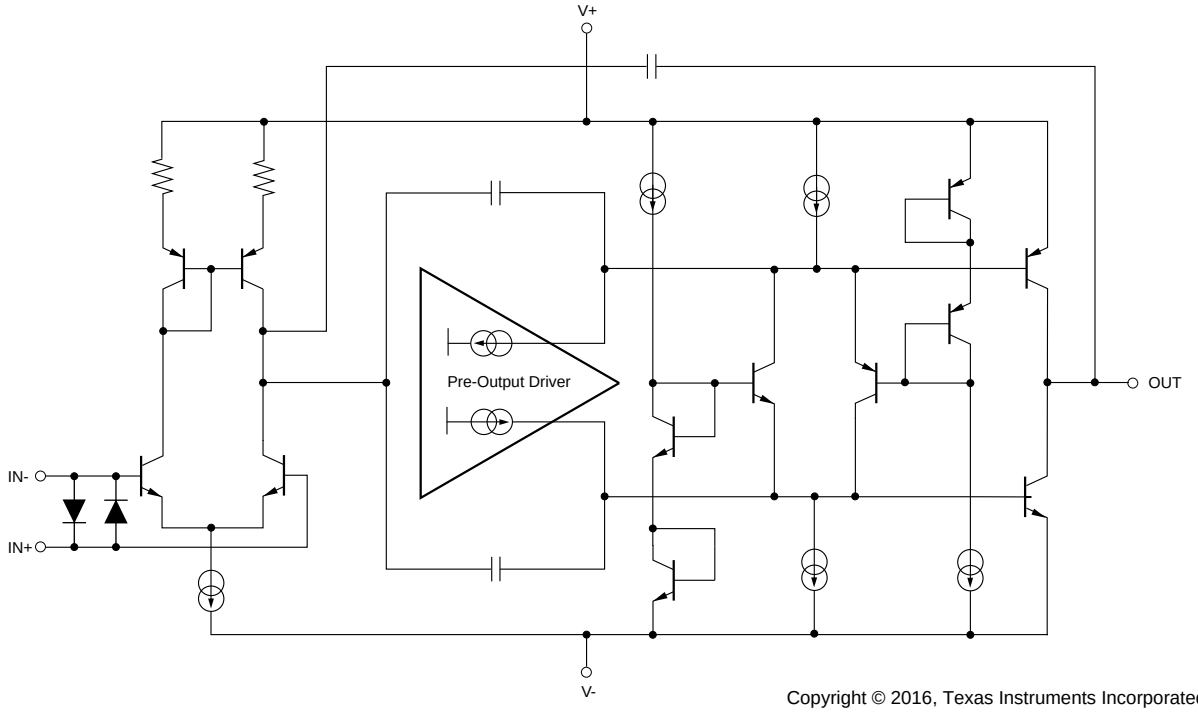
图 39. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The OPA2210 is the next generation of OPA2209 operational amplifier. The OPA2210 offers improved input offset voltage, offset voltage temperature drift, input bias current and lower 1/f noise corner frequency. In addition, this device offers excellent overall performance with high CMRR, PSRR, and A_{OL}.The OPA2210 precision operational amplifier is unity-gain stable and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. The *Functional Block Diagram* shows a simplified schematic of the OPA2210. This die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA2210 op amp can be used with single or dual supplies within an operating range of V_S = 4.5 V (±2.25 V) up to 36 V (±18 V). Supply voltages higher than 40 V total can permanently damage the device.

In addition, key parameters are assured over the specified temperature range, T_A = –40°C to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

7.3.2 Input Protection

The input terminals of the OPA2210 are protected from excessive differential voltage with back-to-back diodes, as shown in 图 40. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in and in *Typical Characteristics*. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA2210. See *Noise Performance* for further information on noise performance.

图 40 shows an example configuration that implements a current-limiting feedback resistor.

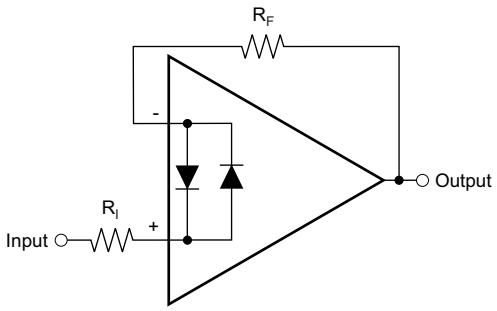


图 40. Pulsed Operation

7.3.3 Noise Performance

图 41 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPA2210 has very low voltage noise, making it ideal for low source impedances (less than 2 kΩ). As a comparable precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. It provides excellent noise performance at moderate to high source impedance (10 kΩ and up). For source impedance lower than 300 Ω, the OPA211 may provide lower noise.

The equation in 图 41 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise,
- i_n = current noise,
- R_S = source impedance,
- k = Boltzmann's constant = 1.38 × 10^{-23} J/K, and
- T = temperature in Kelvins

For more details on calculating noise, see *Basic Noise Calculations*.

Feature Description (接下页)

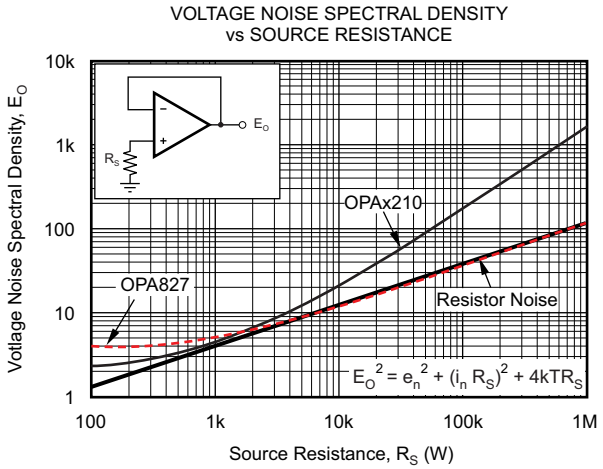


图 41. Noise Performance of the OPA2210 and OPA827 in Unity-Gain Buffer Configuration

7.3.4 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

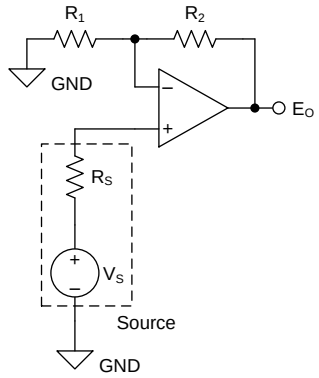
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in 图 41. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

图 42 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPA2210 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

Feature Description (接下页)

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

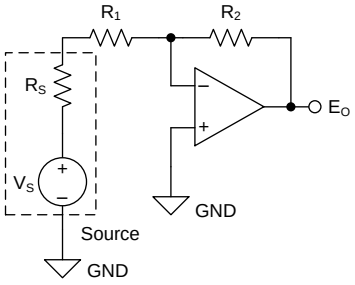
$$(2)\quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \qquad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \qquad \text{Thermal noise of } R_1 \| R_2$$

$$(4)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \qquad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \qquad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \qquad \text{Thermal noise of } (R_1 + R_S) \| R_2$$

$$(8)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \qquad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \qquad \text{Temperature in kelvins}$$

(1) e_N is the voltage noise of the amplifier. For the OPA2210 operational amplifier, e_N = 2.2 nV/√Hz at 1 kHz.
(2) i_N is the current noise of the amplifier. For the OPA2210 operational amplifier, i_N = 400 fA/√Hz at 1 kHz.
(3) For additional resources on noise calculations visit *TI's Precision Labs Series*.

图 42. Noise Calculation in Gain Configurations

7.3.5 Phase-Reversal Protection

The OPA2210 device has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA2210 device prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see 图 30).

7.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Feature Description (接下页)

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See 图 43 for an illustration of the ESD circuits contained in the OPA2210 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2210 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one 图 43 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

图 43 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

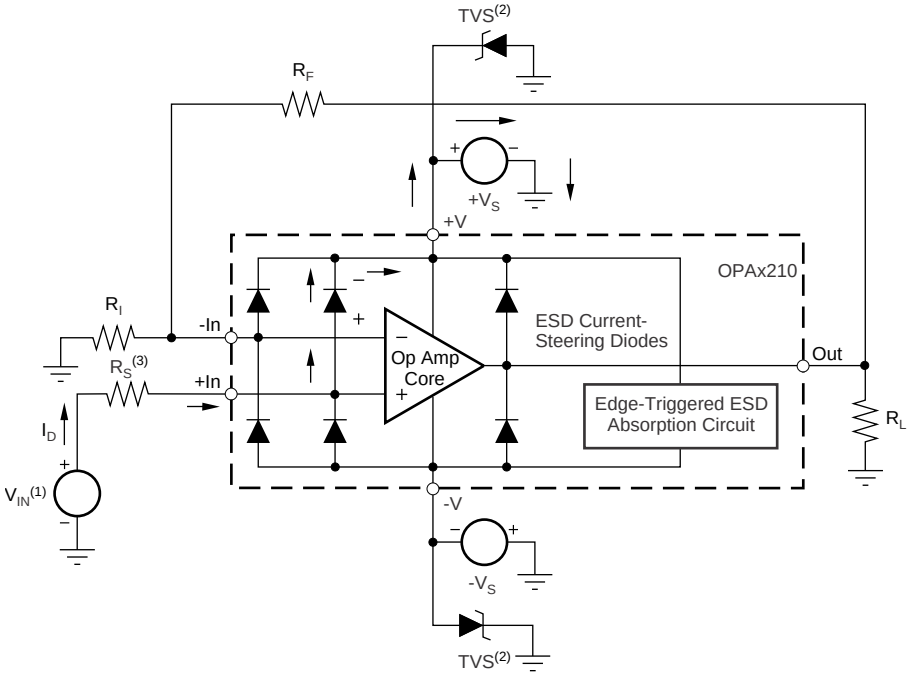
Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0 V.

Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Transient Voltage Suppressor (TVS) diodes may be added to the supply pins as shown in 图 43. The breakdown voltage must be selected such that the diode does not turn on during normal operation.

However, its breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

Feature Description (接下页)



(1) $V_{IN} = +V_S + 500$ mV

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (Min)} > +V_S$

(3) Suggested value approximately 1 kΩ

图 43. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

7.4 Device Functional Modes

The OPA2210 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the OPA2210 is 36 V (±18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2210 is a unity-gain stable, precision operational amplifier with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

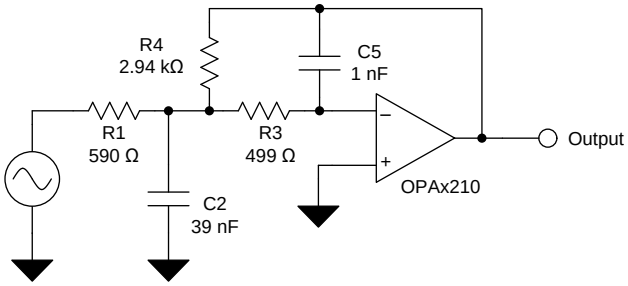


图 44. Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA2210 are ideally suited to construct high-speed, high-precision active filters. 图 44 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 图 44. Use 公式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by 公式 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Typical Application (接下页)

8.2.3 Application Curve

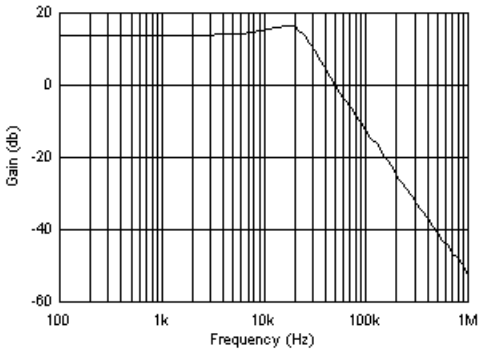


图 45. OPA2210 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

8.3 System Example

8.3.1 Time Gain Control System for Ultrasound Applications

During an ultrasound send-receive cycle, the magnitude of reflected signal depends on the depth of penetration. The ultrasound signal incident on the receiver decreases in amplitude as a function of the time elapsed since transmission, and the TGC helps achieve the best possible signal-to-noise ratio (SNR), even with the decreasing signal amplitude. When the image is displayed, similar material must have similar brightness, regardless of depth; this is achieved by *Linear-in-dB* gain, which means the decibel gain is a linear function of the control voltage (V_{CNTL}).

There are multiple approaches for a TGC control circuit that are based on the type of DAC. 图 46 shows a high level block diagram for the topology using a current-output multiplying DAC (MDAC) to generate the drive for V_{CNTL}. The op amp used for current-to-voltage (I-to-V) conversion must have low-voltage noise as well as low-current noise density. The current density helps in reducing the overall noise performance because of the DAC output configuration. Because the DAC output can go up to ±10 V, the op amp must have bipolar operation. The OPA2210 is employed here due to its low voltage-noise density of 2.2 nV/√Hz, low current-noise density of 500 fA/√Hz, rail-to-rail output and its ability to accept a wide supply range of ±2.25 to ±18 V and provide rail-to-rail output. The low offset voltage and offset drift of the OPA2210 facilitate excellent dc accuracy for the circuit.

The OPA2210 is used to filter and buffer the 10-V reference voltage generated by the REF5010. This serves as the reference voltage for the DAC8802, which generates a current output on I_{OUT} corresponding to the digital input code. The I_{OUT} pin of the DAC8802 is connected to the virtual ground (negative terminal) of the OPA2210; the feedback resistor (R_{FB} is internal to the DAC8802) is connected to the output of the OPA2210, resulting in a current-to-voltage conversion. The output of the OPA2210 has a range of –10 V to 0 V, and it is input to the THS4130, which is configured as a Sallen-Key filter. Finally, the 10-V range is attenuated down to a 1.5-V range, with common mode of 0.75 V using a resistive attenuator. See *2.3-nV/√Hz, Differential, Time Gain Control DAC Reference Design for Ultrasound* for an in-depth analysis of 图 46.

System Example (接下页)

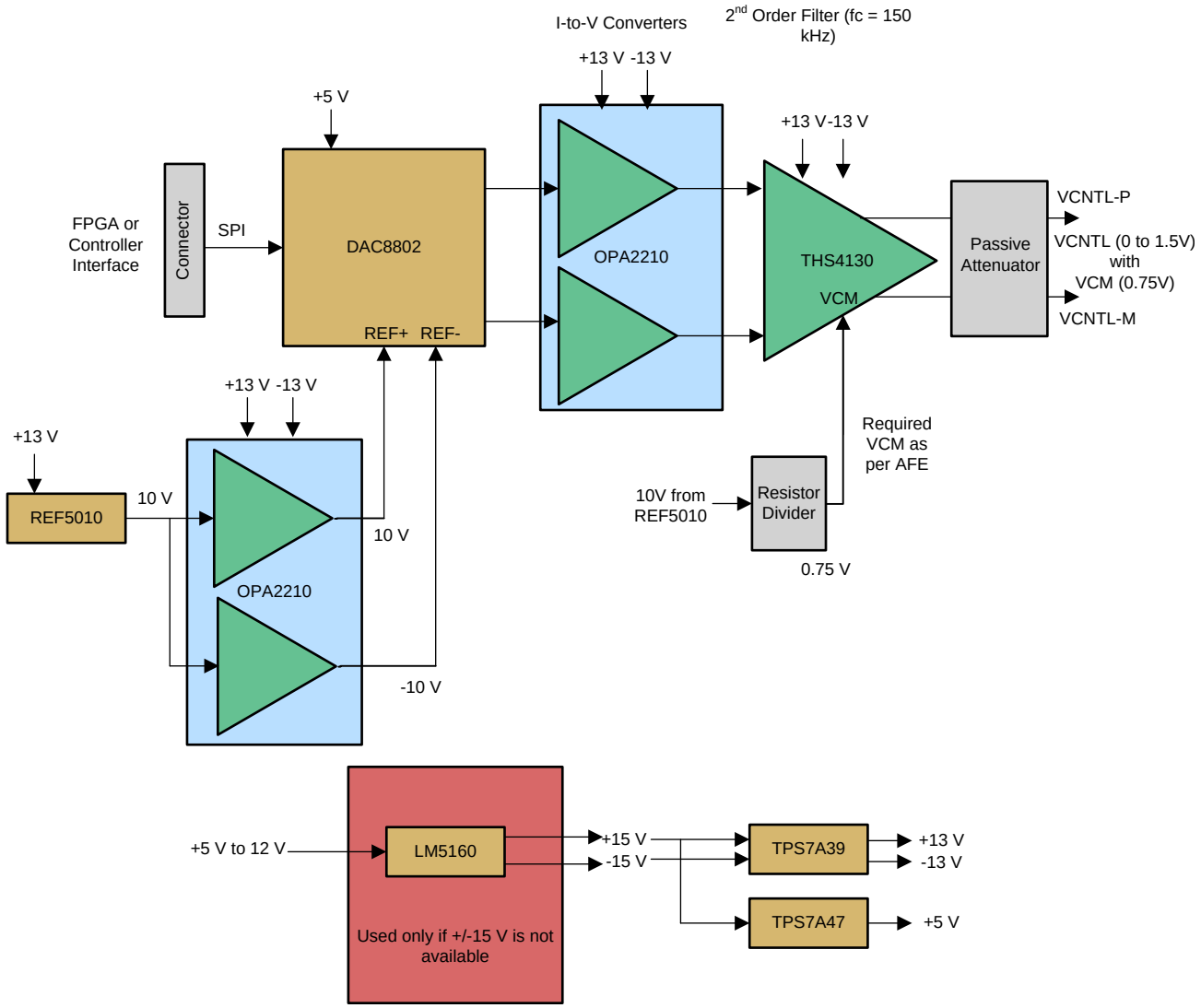


图 46. Block Diagram for Time Gain Control System for Ultrasound

9 Power Supply Recommendations

The OPA2210 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

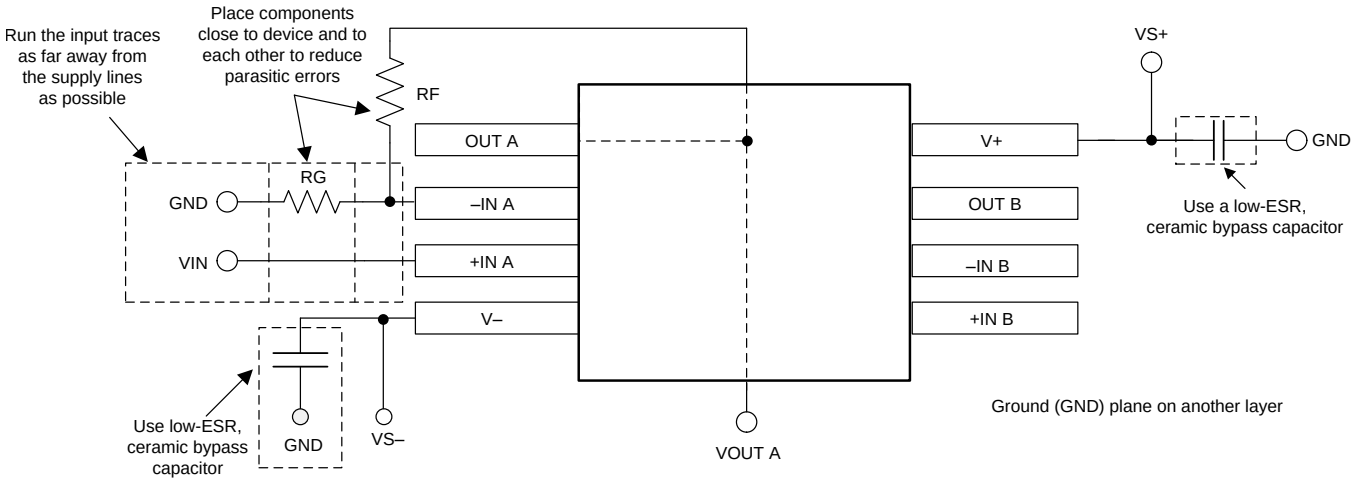


图 47. OPA2210 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种简单而低成本的方式来针对小型表面贴装 IC 进行原型设计。评估工具适用于以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV（SOT23-6、SOT23-5 和 SOT23-3）、DCK（SC70-6 和 SC70-5）以及 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

11.1.1.3 通用运算放大器评估模块 (EVM)

通用运放 EVM 是一系列通用空白电路板，可简化采用各种 IC 封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、VSSOP、TSSOP 和 SOT-23 封装。

注

这些电路板均为空白电路板，用户必须自行提供 IC。TI 建议您在订购通用运放 EVM 时申请几个运放器件样品。

11.1.1.4 TI 高精度设计

TI 高精度设计的模拟设计方案是由 TI 公司高精度模拟实验室设计 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

11.1.1.5 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。借助 WEBENCH 滤波器设计器，用户可使用精选 TI 运算放大器和 TI 供应商合作伙伴提供的无源组件来构建最佳滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在数分钟内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

使用 OPA2210 时，建议参考下列相关文档。所有这些文档都可从 www.ti.com.cn 下载（除非另外说明）：

- *《OPA827 低噪声、高精度 JFET 输入运算放大器》*(SBOS376)
- *《OPA2x11 1.1nv/√Hz 噪声、低功耗、精密运算放大器》*(SBOS377)
- *《OPA210、OPA2210、OPA4210 EMI 抗干扰性能》*(SBOZ020)
- *《OPAx209 2.2nV/√Hz、低功耗、36V 运算放大器》*(SBOS426)

文档支持 (continued)

- *《微控制器 PWM 到 12 位模拟输出》*(TIDU027)
- *《采用隔离电阻器的电容式负载驱动器解决方案》*(TIDU032)
- *《噪声测量后置放大器》*(TIDU016)
- *《诊断、患者监护及治疗指南》*(SLYB147)

11.3 接收文档更新通知

如需接收文档更新通知，请访问 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2210IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OHQ	Samples
OPA2210IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OHQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

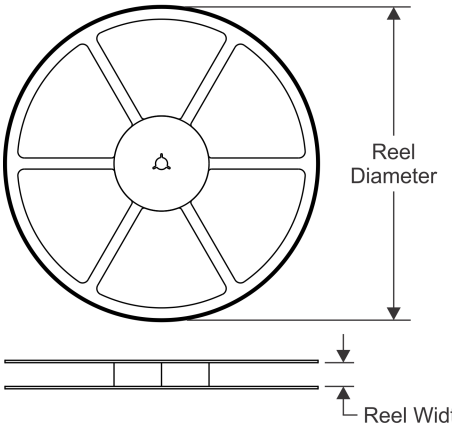
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

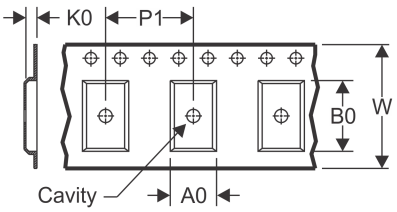
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

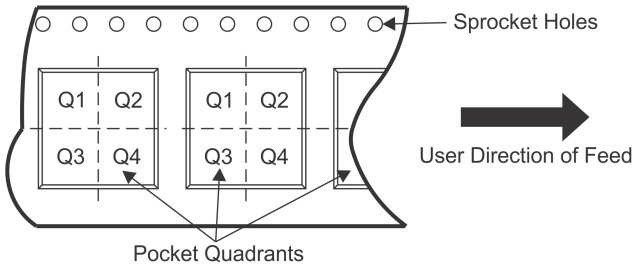


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

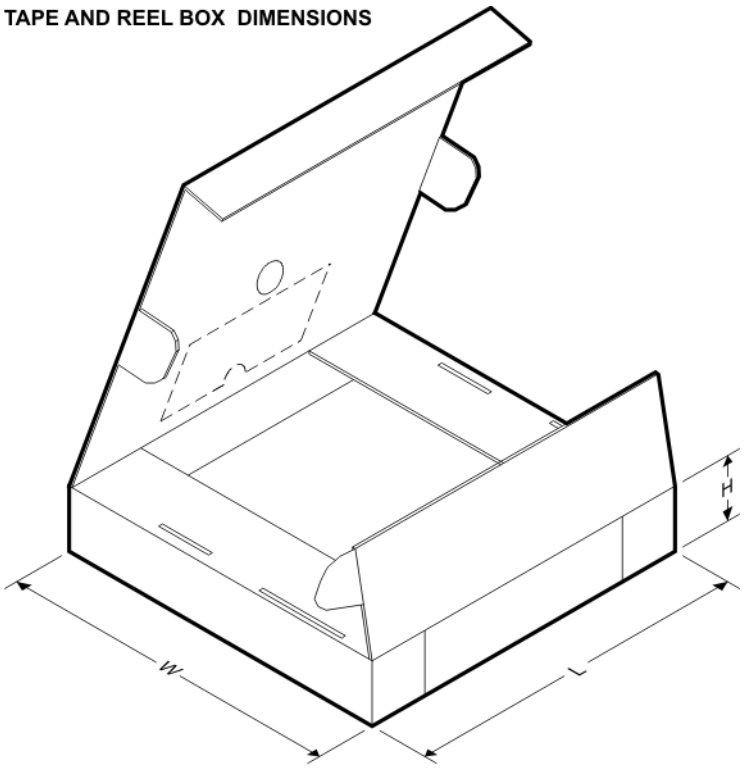
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2210IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2210IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

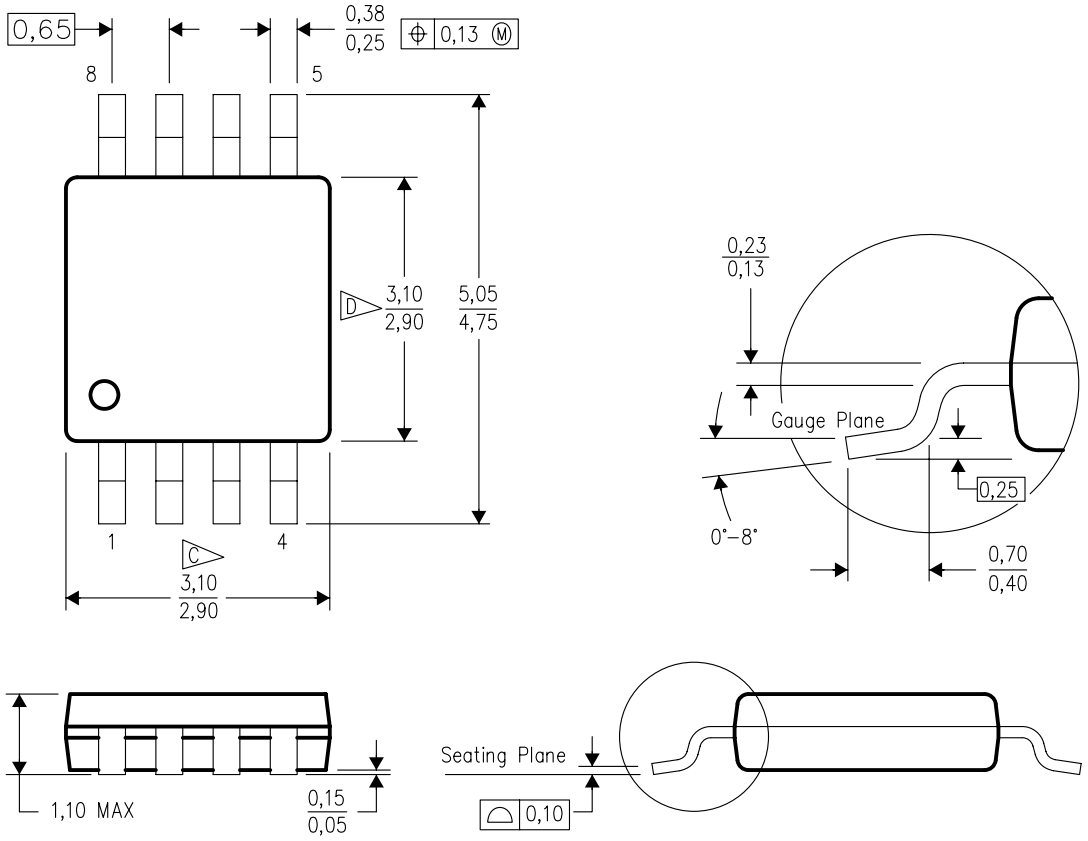
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2210IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2210IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

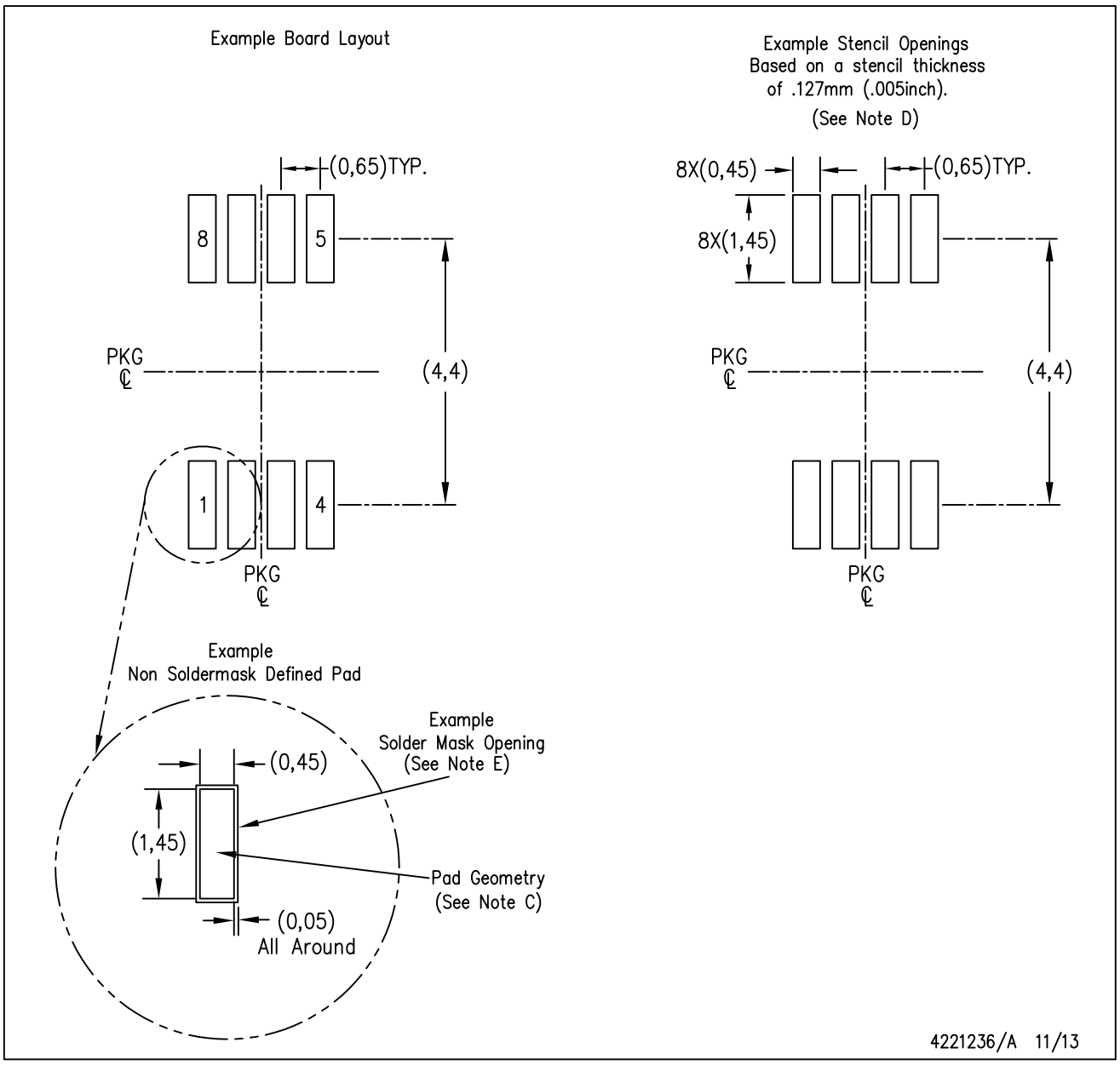
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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