INA381 26V 零漂移、电压输出、电流分流监控器（具有集成比较器）

1 特性

- 共模输入范围：–0.2V 至 26V
- 高精度放大器：
  - 失调电压，V_{CM} = 12V：500µV（最大值）
  - 失调电压，V_{CM} = 0V：150µV（最大值）
  - 失调电压漂移：1µV/°C（最大值）
  - 增益误差：1%（最大值）
  - 增益误差漂移：20ppm/°C（最大值）
- 可用放大器增益：
  - INA381A1：20V/V
  - INA381A2：50V/V
  - INA381A3：100V/V
  - INA381A4：200V/V
- 比较器技术规格：
  - 迟滞：50mV
  - 响应时间：500ns
  - 通过外部基准电压设置警报阈值
- 具有锁存模式的开漏比较器输出
- 封装：WSON-8 (2mm × 2mm)

2 应用

- 过流保护
- 电源保护
- 低侧相位电机控制
- 计算机和服务器
- 电信设备

3 说明

INA381 包括 26V 共模电流感应放大器和高速比较器，通过测量分流电阻器两侧的电压并将该电压与定义的阈值限值（通过比较器基准引脚进行设置）作比较来检测过流情况。该电流分流监控器可在独立于电源电压的 –0.2 V 至 26 V 共模电压范围内测量差分电压信号。

开漏警报输出可配置为透明模式（输出状态与输入状态保持一致）或锁存模式（复位锁存时清除警报输出）。独立比较器的警报响应时间低于 3µs，能够快速检测过流事件。由 INA381 提供的整个系统的过电流保护将低于 10µs。

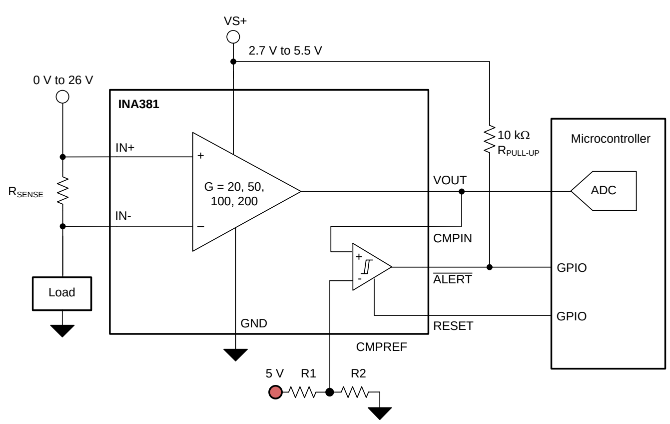
这款器件由 2.7V - 5.5V 单电源供电运行，消耗取的最大电源电流为 350µA。该器件具有扩展级工作温度范围（–40°C 至 +125°C），并且可提供 8 引脚 WSON 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA381	WSON (8)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2017) to Revision A **Page**

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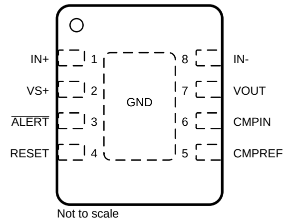
5 Pin Configuration and Functions

DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{ALERT}}$	3	Digital output	Overlimit alert, active low, open-drain output
CMPIN	6	Analog input	Signal input to the comparator
CMPREF	5	Analog input	Input reference to the comparator
IN–	8	Analog input	Connect to the load side of the shunt resistor
IN+	1	Analog input	Connect to the supply side of the shunt resistor
RESET	4	Digital input	Transparent or latch mode selection input. See the *Alert Mode* section for a detailed description on pin connections.
VOUT	7	Analog output	Current-sense amplifier output voltage
VS+	2	Supply	Power supply, 2.7 V to 5.5 V
GND	Pad	Ground	Device ground, connect the ground pad to the system ground. See the layout example in 图 54.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)[(2)]	–26	26	V
	Common-mode [(3)]	GND – 0.3	26	V
Analog input	CMPIN	GND – 0.3	(V_S) + 0.3	V
	CMPREF	GND – 0.3	(V_S) + 0.3	V
Analog output	OUT	GND – 0.3	(V_S) + 0.3	V
Digital input	RESET	GND – 0.3	(V_S) + 0.3	V
Digital output	$\overline{\text{ALERT}}$	GND – 0.3	6	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage may exceed the voltage shown without causing damage to the device if the current at that terminal is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	-0.2	12	26	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		INA381 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and CMPREF = 2 V, (unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input voltage range		–0.2		26	V
CMRR	Common-mode rejection ratio, RTI	V_{IN+} = 0 V to 26 V, T_A= –40ºC to +125ºC	84	100		dB
V_{OS}	Offset voltage, RTI (1)	V_{IN+} = 12 V, $V_{IN–}$ = 12 V		±100	±500	µV
		V_{IN+} = 0 V, $V_{IN–}$ = 0 V		±25	±150	µV
dV_{OS}/dT	Offset voltage drift, RTI (1)	T_A= –40ºC to +125ºC		0.1	1	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, T_A= –40ºC to +125ºC		±8	±40	µV/V
I_B	Input bias current	V_{SENSE} = 0 mV, I_{B+}, $I_{B–}$		80		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.05		µA
OUTPUT						
G	Gain	INA381A1		20		V/V
		INA381A2		50		V/V
		INA381A3		100		V/V
		INA381A4		200		V/V
E_G	Gain error	VOUT = 0.5 V to V_S – 0.5 V		±0.1%	±1%	
	Gain error vs temperature	T_A= –40ºC to +125ºC		1.5	20	ppm/°C
	Nonlinearity error	VOUT= 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A= –40ºC to 125ºC		V_S – 0.02	V_S – 0.05	V
	Swing to GND (2)	R_L = 10 kΩ to GND, T_A= –40ºC to 125ºC		V_{GND} + 0.0005	V_{GND} + 0.005	V
FREQUENCY RESPONSE						
BW	Bandwidth	INA381A1		350		kHz
		INA381A2		210		kHz
		INA381A3		150		kHz
		INA381A4		105		kHz
SR	Slew rate			2		V/µs
NOISE						
	Voltage noise density			40		nV/√Hz
COMPARATOR						
t_p	Propagation delay time, comparator only	CMPIN Input overdrive = 20 mV		0.4	1	µs
	Large-signal propagation delay, comparator only	CMPIN step = 0.5 V to 4.5, V_{CMPREF} = 4 V		0.4	2	µs
	Small-signal total alert propogation delay, comparator and amplifier	Input overdrive = 1 mV		2	5	µs
	Slew rate limited total alert propagation delay, comparator and amplifier	VOUT step = 0.5 V to 4.5 V_{CMPREF} = 4 V		3	10	µs
V_{OS}	Comparator offset voltage			1	5	mV
HYS	Hysteresis			50		mV
V_{IH}	High-level input voltage		1.4		6	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA		70	300	mV
	$\overline{ALERT}$ pin leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	Digital leakage input current	0 ≤ V_{IN} ≤ V_S		1		µA

(1) RTI = referred-to-input.
(2) Swing specifications are tested with an overdriven input condition.

Electrical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 10 mV, V_S = 5 V, V_{IN+} = 12 V, and CMPREF = 2 V, (unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Operating supply range	T_A = –40ºC to +125ºC	2.7		5.5	V
I_Q	Quiescent current	V_{SENSE} = 10 mV, T_A = +25ºC		250	350	μA
		T_A = –40ºC to +125ºC			450	μA
TEMPERATURE RANGE						
	Specified range		–40		125	°C

6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

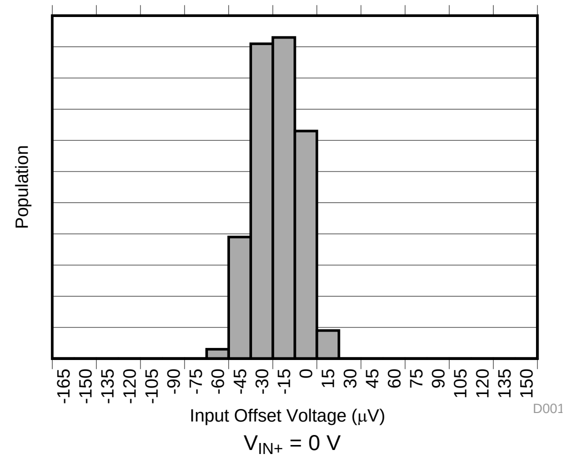


图 1. Input Offset Voltage Production Distribution (INA381A1)

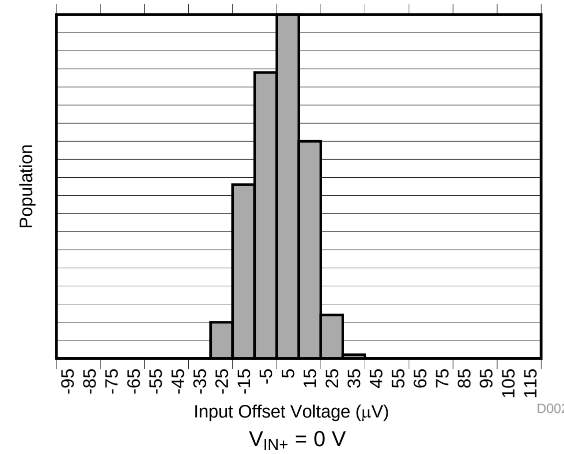


图 2. Input Offset Voltage Production Distribution (INA381A2)

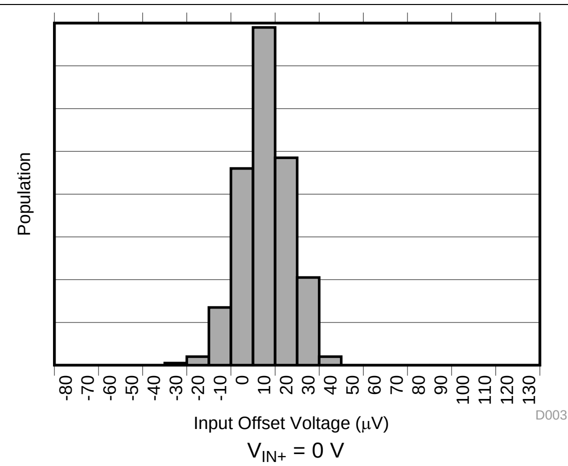


图 3. Input Offset Voltage Production Distribution (INA381A3)

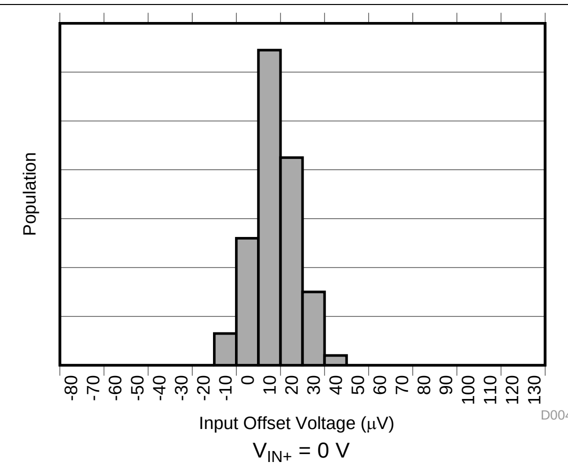


图 4. Input Offset Voltage Production Distribution (INA381A4)

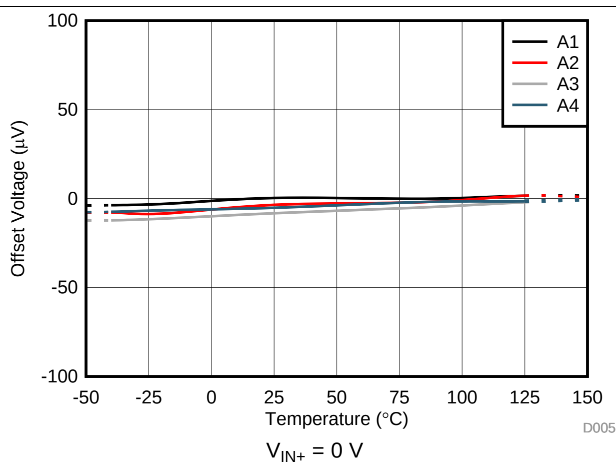


图 5. Offset Voltage vs Temperature

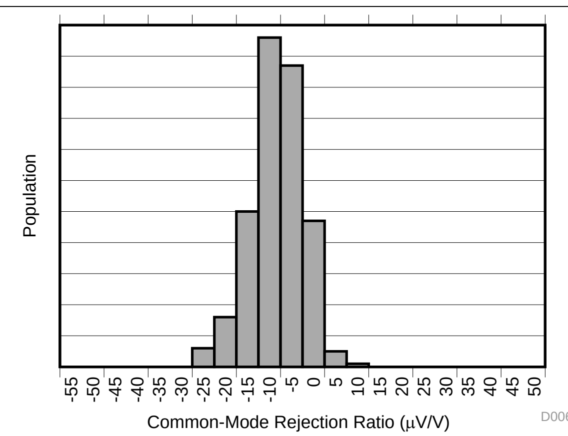


图 6. Common-Mode Rejection Production Distribution (INA381A1)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

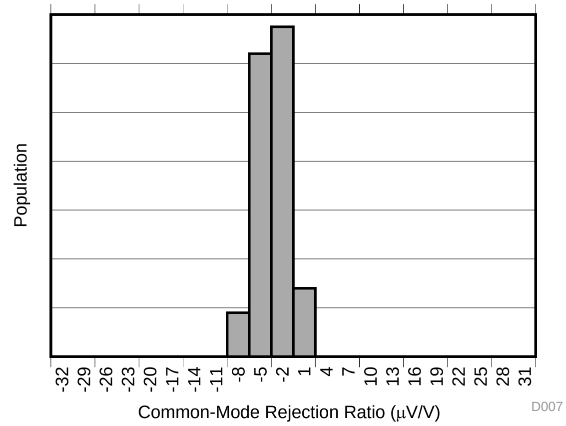


图 7. Common-Mode Rejection Production Distribution (INA381A2)

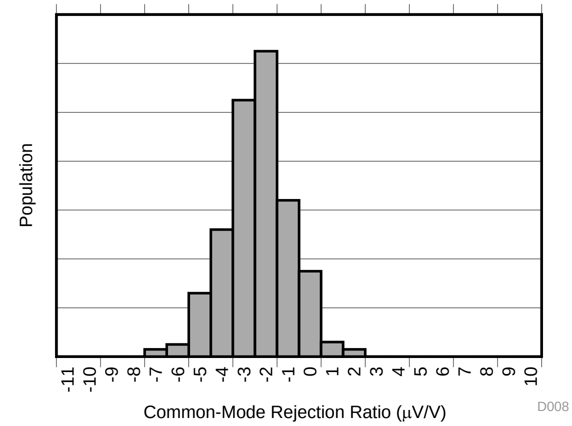


图 8. Common-Mode Rejection Production Distribution (INA381A3)

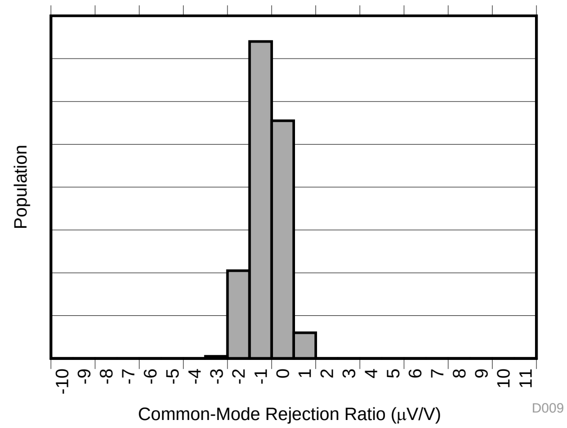


图 9. Common-Mode Rejection Production Distribution (INA381A4)

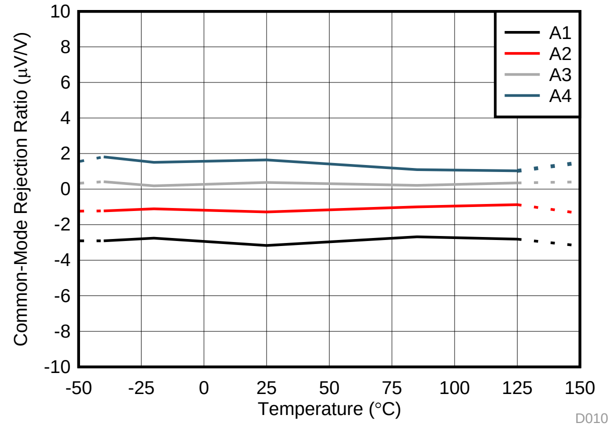


图 10. Common-Mode Rejection Ratio vs Temperature

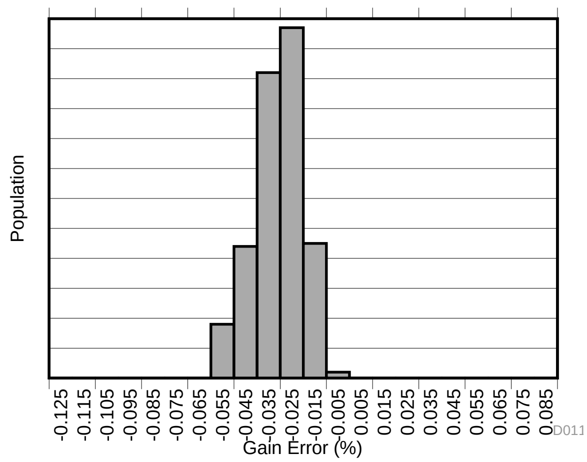


图 11. Gain Error Production Distribution (INA381A1)

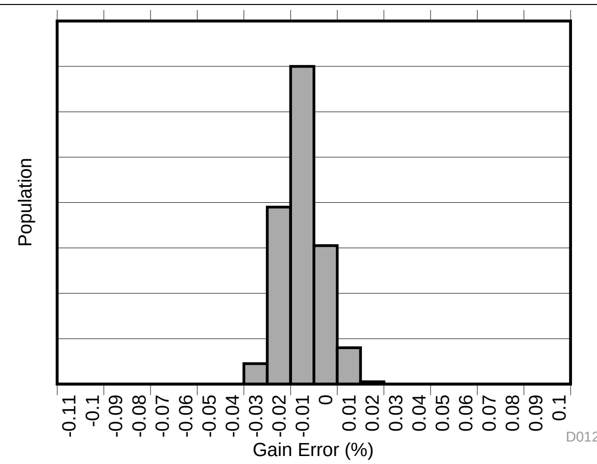


图 12. Gain Error Production Distribution (INA381A2)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

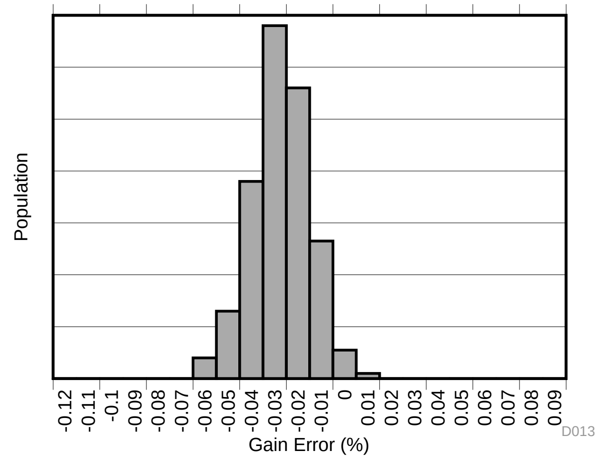


图 13. Gain Error Production Distribution (INA381A3)

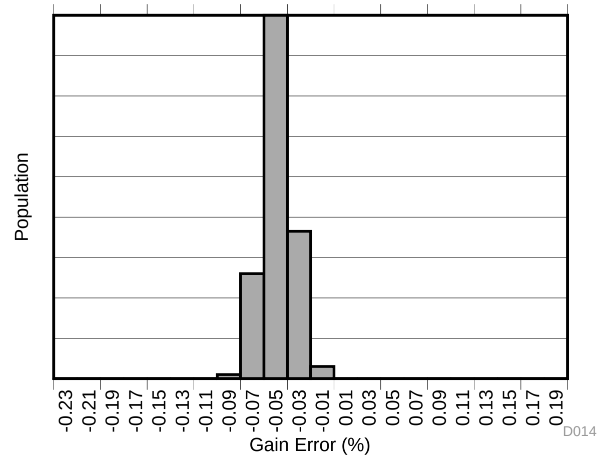


图 14. Gain Error Production Distribution (INA381A4)

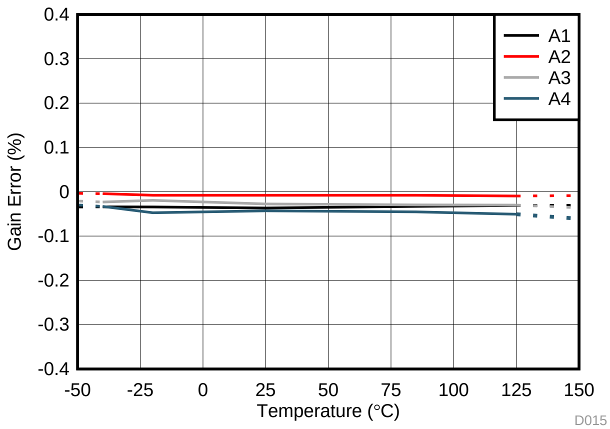


图 15. Gain Error vs Temperature

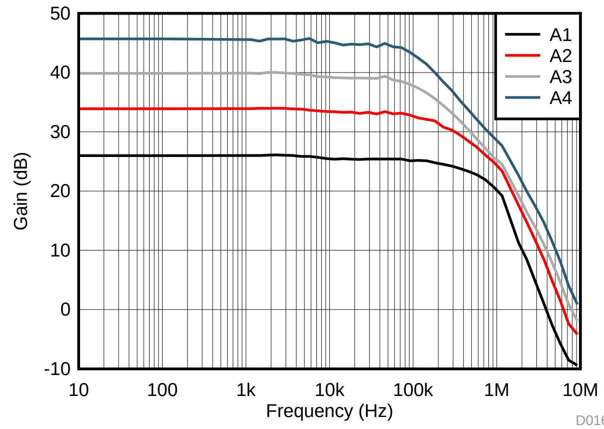


图 16. Gain vs Frequency

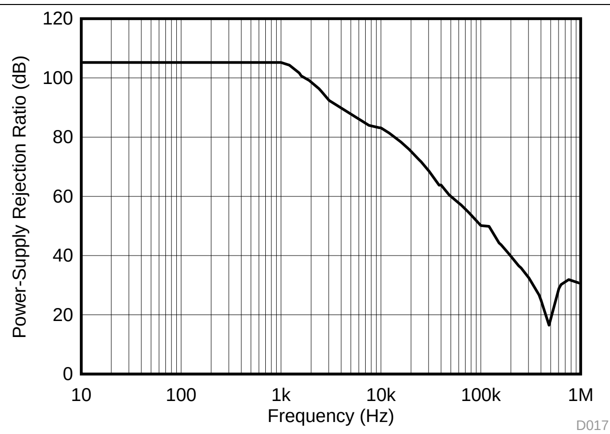


图 17. Power-Supply Rejection Ratio vs Frequency

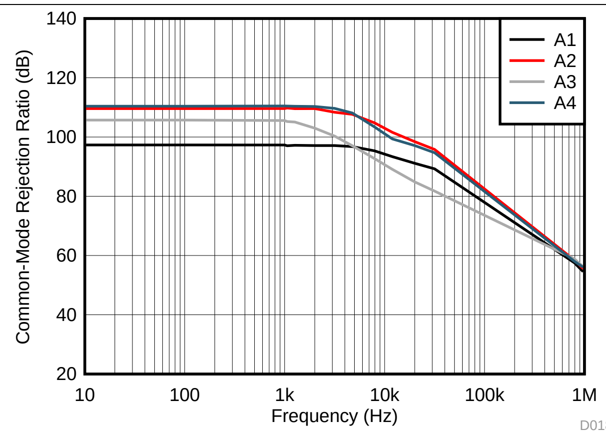


图 18. Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

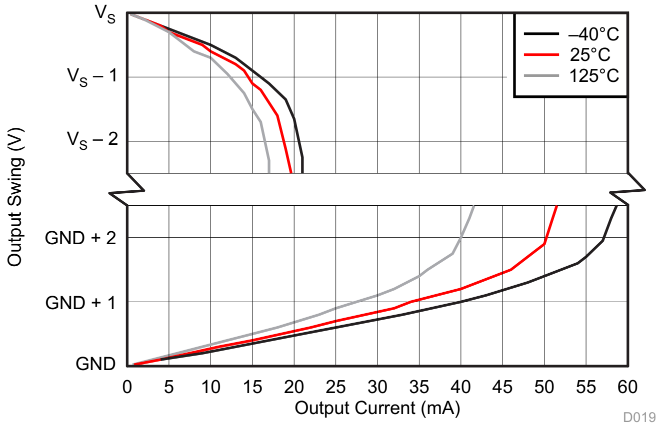
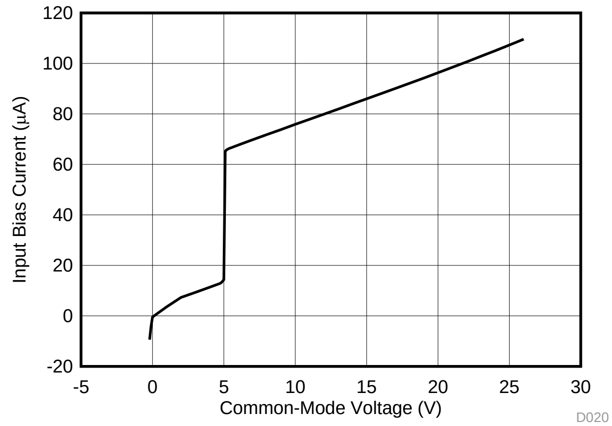
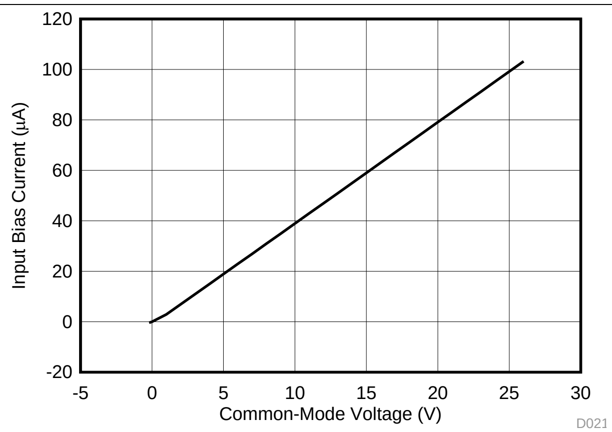


图 19. Output Voltage Swing vs Output Current



Supply voltage = 5 V

图 20. Input Bias Current vs Common-Mode Voltage



Supply voltage = 0 V

图 21. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

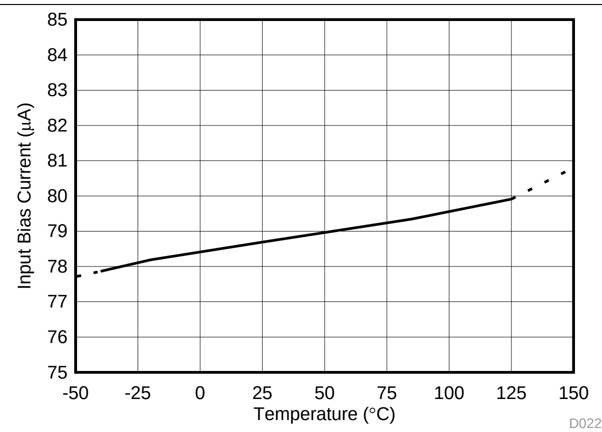


图 22. Input Bias Current vs Temperature

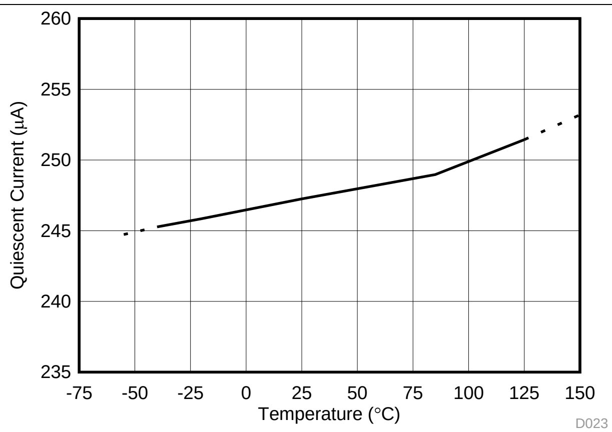


图 23. Quiescent Current vs Temperature

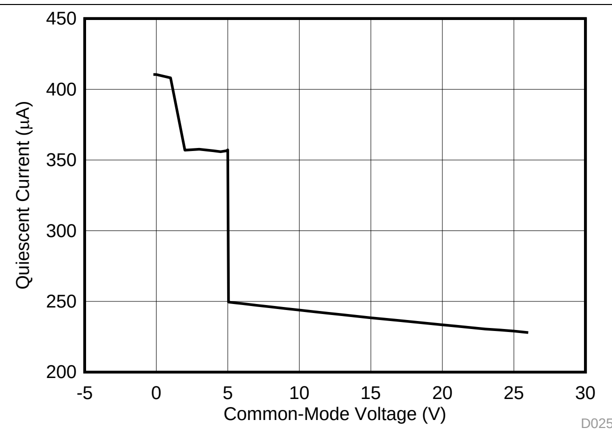


图 24. Quiescent Current vs Common-Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

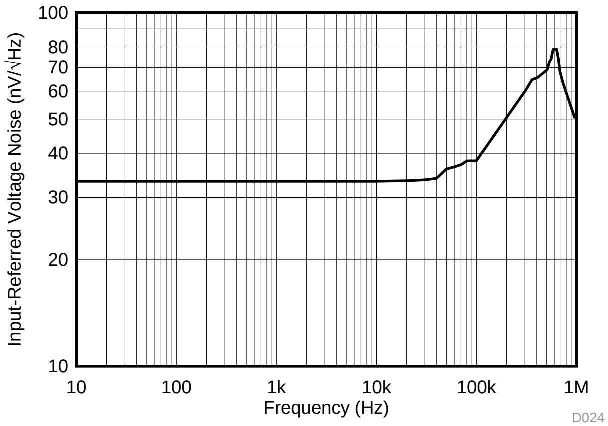


图 25. Input-Referred Voltage Noise vs Frequency (INA381A3 Devices)

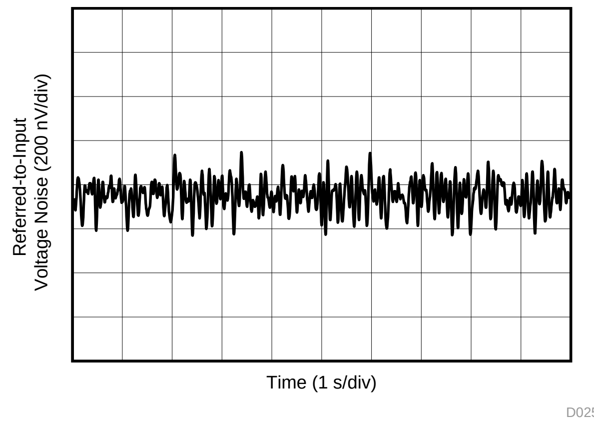
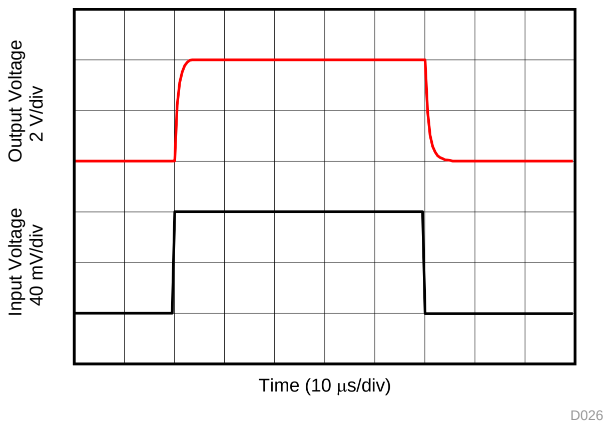


图 26. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)



80-mV$_{PP}$ input step

图 27. Step Response

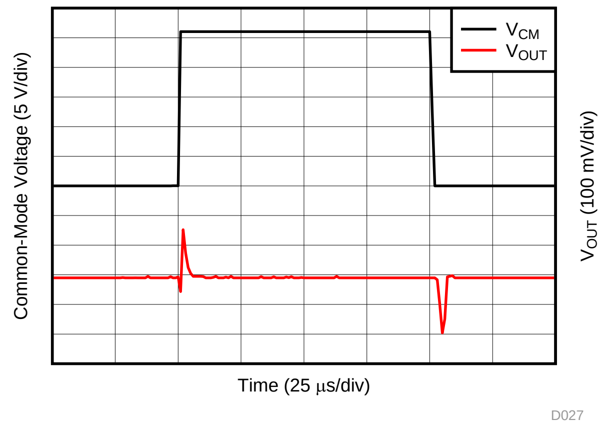


图 28. Common-Mode Voltage Transient Response

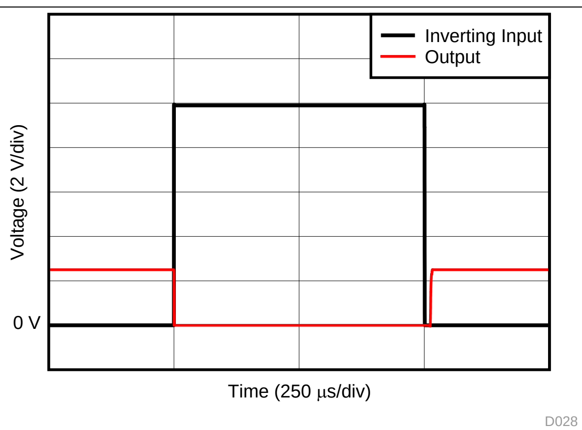


图 29. Inverting Differential Input Overload

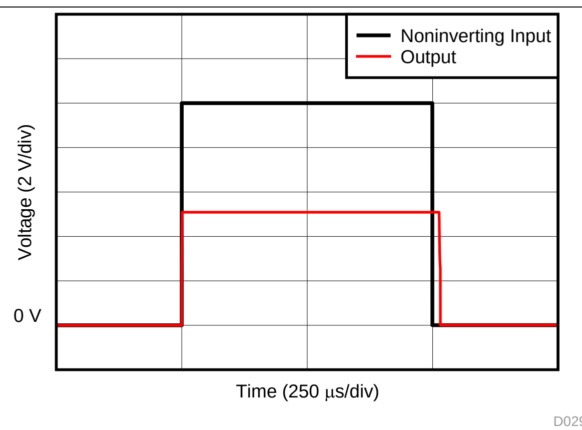


图 30. Noninverting Differential Input Overload

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

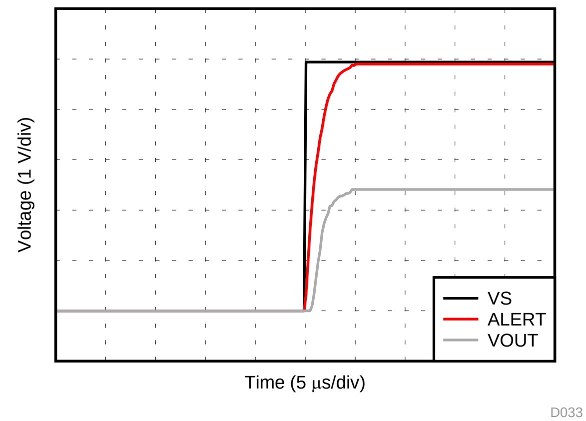


图 31. Start-Up Response

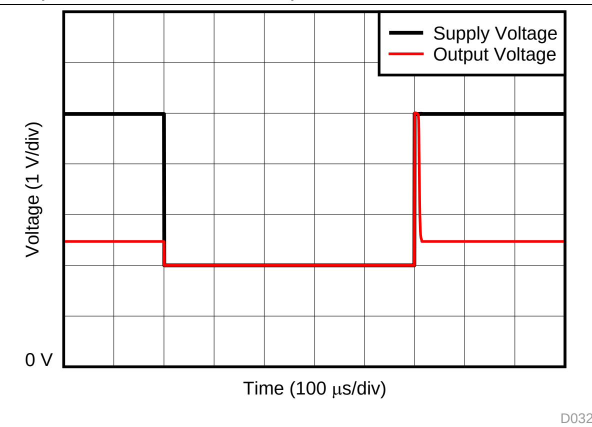


图 32. Brownout Recovery

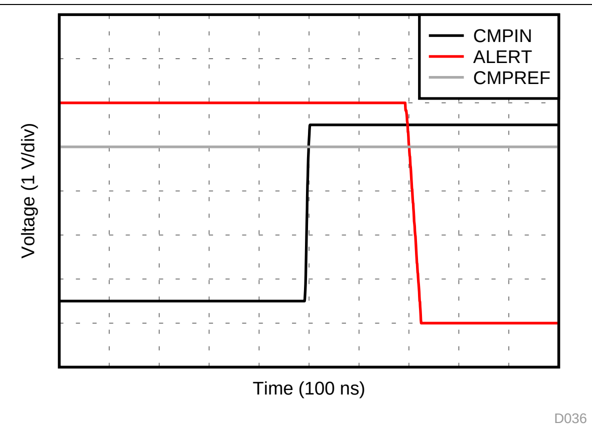


图 33. Comparator Propagation Delay

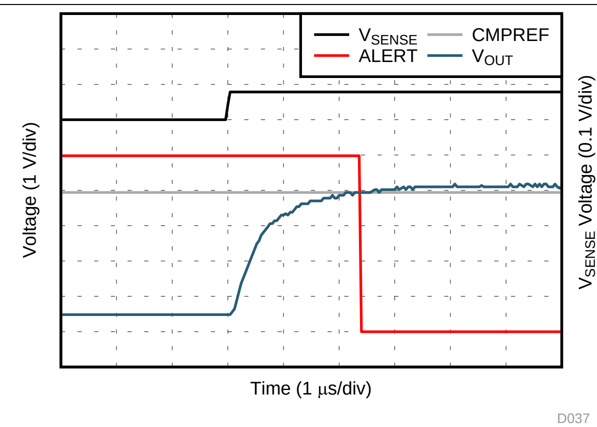


图 34. V_{SENSE} Voltage Response

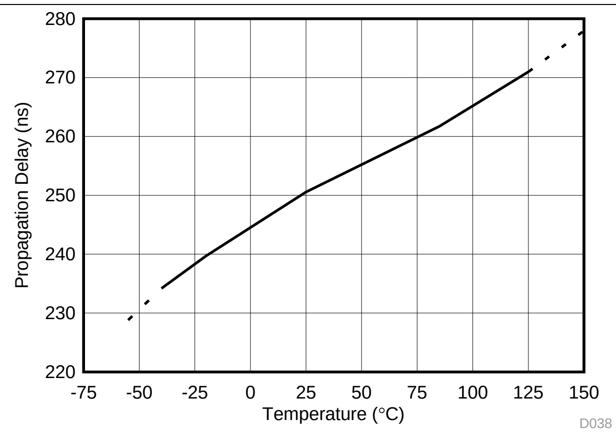


图 35. Comparator Propagation Delay vs Temperature

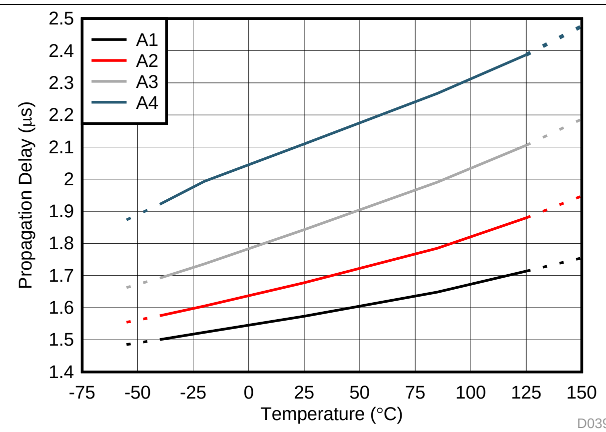


图 36. Total Propagation Delay vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and alert pullup resistor = 10 kΩ (unless otherwise noted)

图 37. Low-Level Output Voltage vs Low-Level Output Current

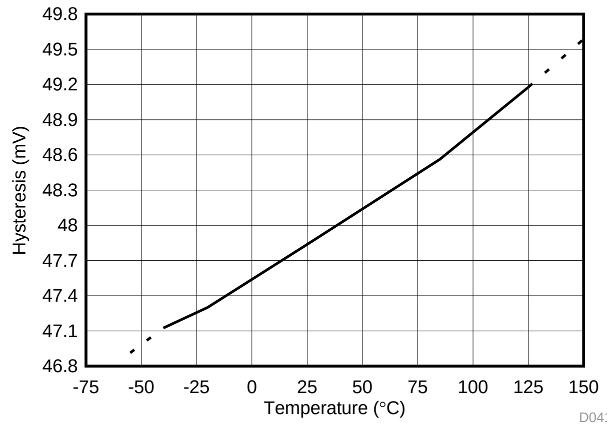


图 38. Hysteresis vs Temperature

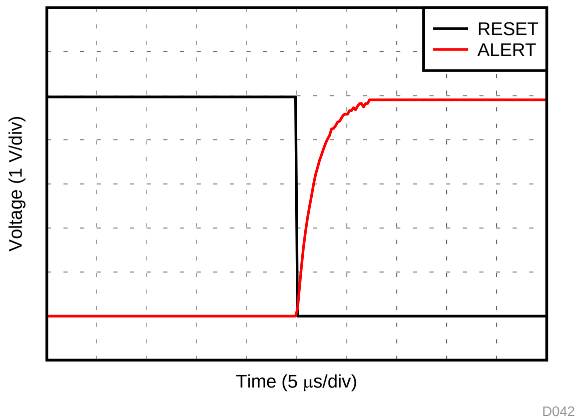


图 39. Reset and Alert Voltage Response

7 Detailed Description

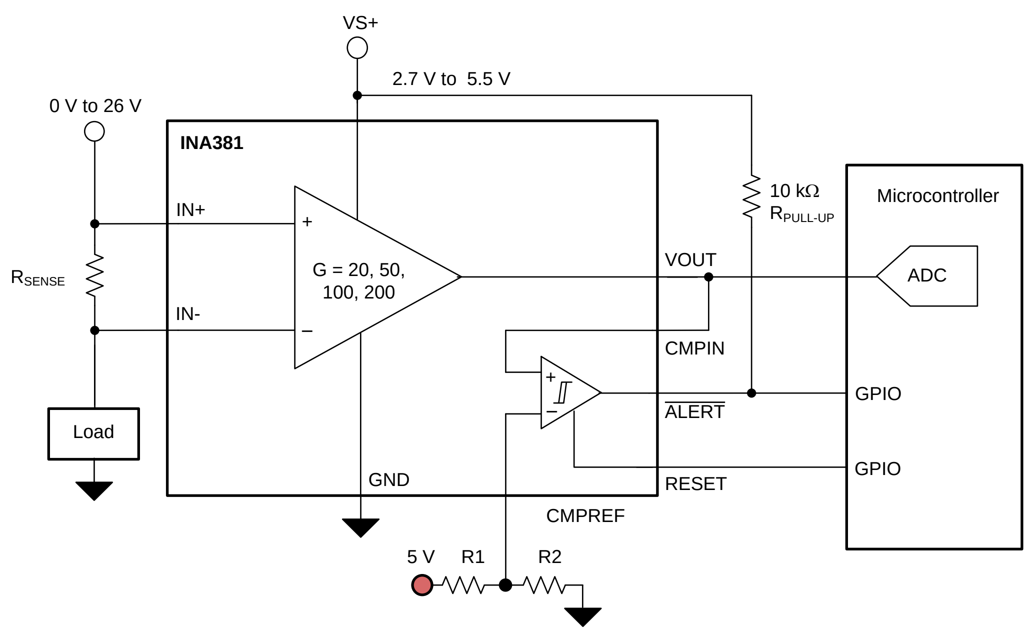
7.1 Overview

The INA381 is a zero-drift topology, current-sensing amplifier with an integrated comparator that can be used in both low-side and high-side current-sensing and protection applications. This specially-designed, current-sensing amplifier is able to accurately measure voltages developed across current-sensing resistors (also known as *current-shunt resistors*) on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the device can be powered from supply voltages as low as 2.7 V. The device can also withstand the full 26-V common-mode voltage at the input pins when the supply voltage is removed without causing damage.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 150 µV with a temperature contribution of only 1 µV/°C over the full temperature range of –40°C to +125°C. The low total offset voltage of the INA381 enables smaller current-sense resistor values to be used, and allows for a more efficient system operation without sacrificing measurement accuracy resulting from the smaller input signal.

The INA381 uses a reference input that allows for a simple method of setting the corresponding current threshold level for the device to use for out-of-range comparison. Combining the precision measurement of the current-sense amplifier and the on-board comparator enables an all-in-one overcurrent detection device. This combination creates a highly-accurate solution that is capable of fast detection of out-of-range conditions and allows the system to take corrective actions to prevent potential component or system-wide damage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wide Input Common-Mode Voltage Range

The INA381 supports input common-mode voltages from –0.2 V to 26 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S) as long as V_S stays within the operational range of 2.7 V to 5.5 V. As 图 40 shows, the ability to operate with common-mode voltages greater or less than V_S allows the INA381 to be used in high-side (and low-side) current-sensing applications.

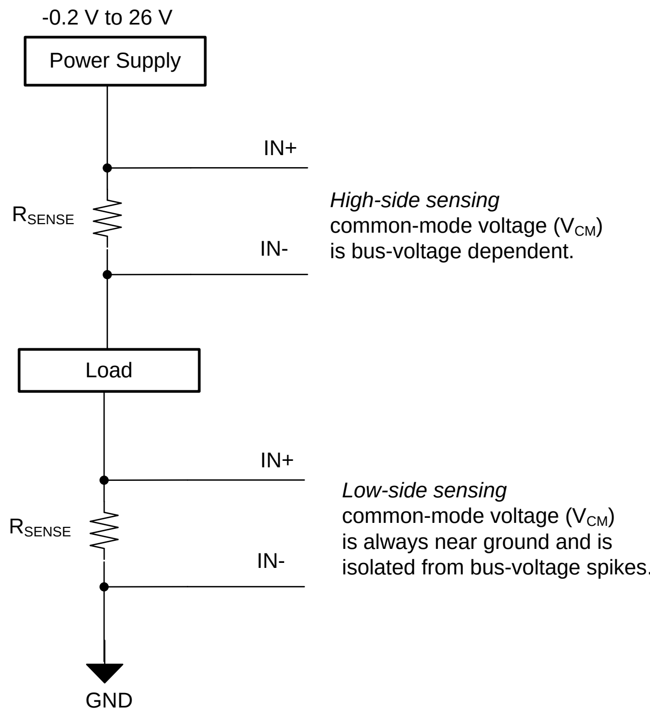


图 40. High-Side and Low-Side Current Sensing

7.3.2 Precise Low-Side Current Sensing

When used in low-side current-sensing applications, the offset voltage of the INA381 is less than 150 µV. The low offset performance of the INA381 has several benefits. First, the low offset allows the device to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves accuracy when the sense currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drops across the sense resistor accurately, thus allowing for a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current-sense circuit, and help improve the power efficiency of the end application.

The gain error of the INA381 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this gain error becomes the dominant source of error in the current-sense measurement.

7.3.3 High Bandwidth and Slew Rate

The INA381 supports small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, makes the INA381 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection. The integrated comparator within the INA381 is designed to quickly detect when the sense current is out-of-range and provides a digital output on the $\overline{\text{ALERT}}$ pin for quicker and faster responses.

Feature Description (接下页)

7.3.4 Alert Output

The device ALERT pin is an active-low, open-drain output that is designed to be pulled low when the input conditions are detected to be out-of-range. This open-drain output pin is recommended to include a 10-kΩ pullup resistor to the supply voltage. This open-drain pin can be pulled up to a voltage beyond the supply voltage, V_S, but must not exceed 5.5 V.

图 41 shows the alert output response of the internal comparator. When the output voltage of the amplifier is lower than the set reference voltage on CMPREF, the comparator output is in the default high state. When the amplifier output voltage exceeds the reference voltage set at the CMPREF pin, the comparator output becomes active and pulls low. This active low output indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred.

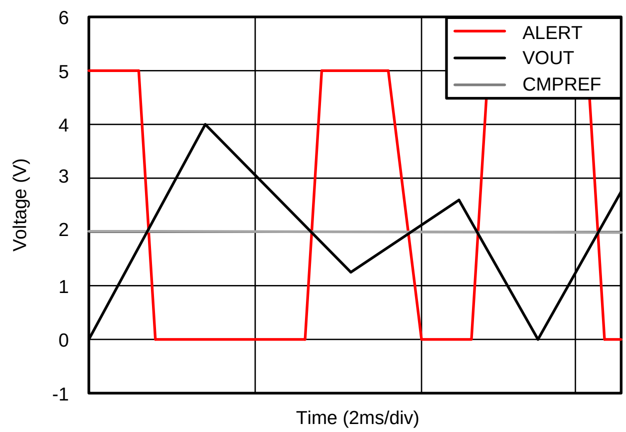


图 41. Overcurrent Alert Response

7.3.5 Alert Mode

The device has two output operating modes, transparent and latched, that are selected based on the RESET pin setting. These modes change how the ALERT pin responds following an alert when the overcurrent condition is removed.

7.3.5.1 Transparent Output Mode

The device is set to transparent mode when the RESET pin is pulled low, allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the alert output pin is pulled low. When the differential input signal drops below the alert threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is connecting the ALERT pin to a hardware interrupt input on a microcontroller. When an overcurrent condition is detected and the ALERT pin is pulled low, the controller interrupt pin detects the output state change and begins making changes to the system operation required to address the overcurrent condition. Under this configuration, the ALERT pin high-to-low transition is captured by the microcontroller so the output returns to the default high state when the overcurrent event is removed.

Feature Description (接下页)

7.3.5.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the output ALERT pin to detect an overcurrent condition, as described in the *Transparent Output Mode* section. A typical example of this application is a system that is only able to poll the ALERT pin state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, the state change of the ALERT pin can be missed when ALERT is pulled low to indicate an out-of-range event if the out-of-range condition does not appear during one of these periodic polling events. Latch mode is specifically intended to accommodate these applications.

As shown in 表 1, the device is placed into the corresponding output mode based on the signal connected to RESET. The difference between latch mode and transparent mode is how the alert output responds when an overcurrent event ends. In transparent mode (RESET = low), when the differential input signal drops below the limit threshold level after the ALERT pin asserts because of an overcurrent event, the state of the ALERT pin returns to the default high setting to indicate that the overcurrent event is complete.

表 1. Output Mode Settings

OUTPUT MODE	RESET PIN SETTING
Transparent mode	RESET = low
Latch mode	RESET = high

In latch mode (RESET = high), when an overlimit condition is detected and the ALERT pin is pulled low, the ALERT pin does not return to the default high state when the differential input signal drops below the alert threshold level. To clear the alert, the RESET pin must be pulled low for at least 100 ns. Pulling the RESET pin low returns ALERT to the default high level, if the differential input signal is below the alert threshold. If the input signal is above the threshold limit when the RESET pin is pulled low, the ALERT pin remains low. When the alert condition is detected by the system controller, the RESET pin can be set back to high to place the device back in latch mode.

图 42 shows the latch and transparent modes. In 图 42, when V_{IN} drops back below the V_{LIMIT} threshold for the first time, the RESET pin is pulled high. With the RESET pin pulled high, the device is set to latch mode so that the alert output state does not return high when the input signal drops below the V_{LIMIT} threshold. Only when the RESET pin is pulled low does the ALERT pin return to the default high level, thus indicating that the input signal is below the limit threshold. When the input signal drops below the limit threshold for the second time, the RESET pin is already pulled low. The device is set to transparent mode at this point and the ALERT pin is pulled back high when the input signal drops below the alert threshold.

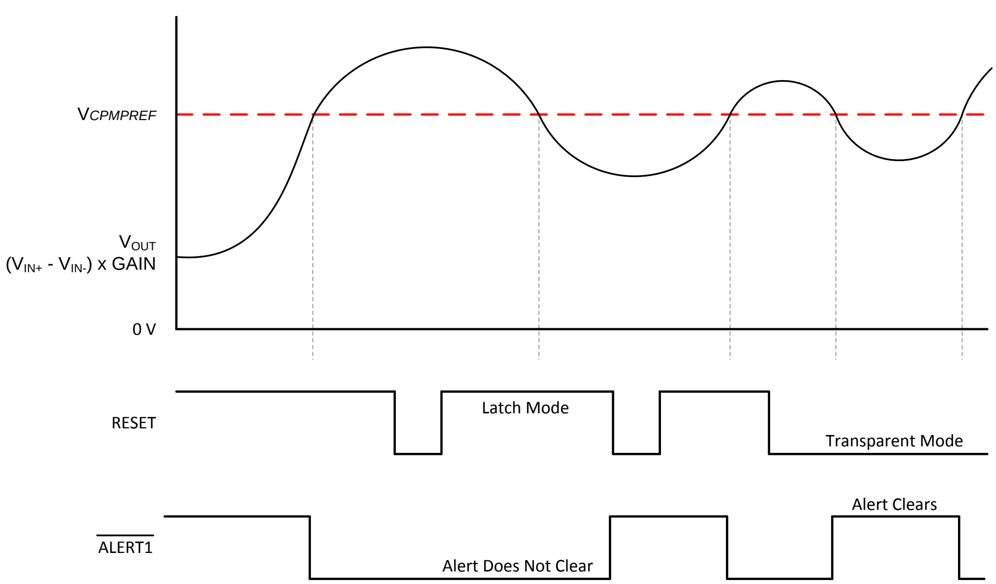


图 42. Transparent versus Latch Mode

7.3.6 Setting The Current-Limit Threshold

The VOUT voltage is the amplified voltage developed across the current-sensing resistor. The signal developed at the VOUT pin is the input voltage across the IN+ and IN– pins multiplied by the gain of the amplifier. The INA381 has four gain options, as shown in 图 43: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The VOUT pin can be externally shorted to the CMPIN pin.

The INA381 determines if an overcurrent event is present by comparing the voltage on the CMPIN pin to the corresponding signal developed at the CMPREF pin. The threshold voltage for the CMPREF pin can be set with a resistive divider or by connecting an external voltage source (such as a reference generator device). 图 44 depicts the REF3140 used as an external reference source.

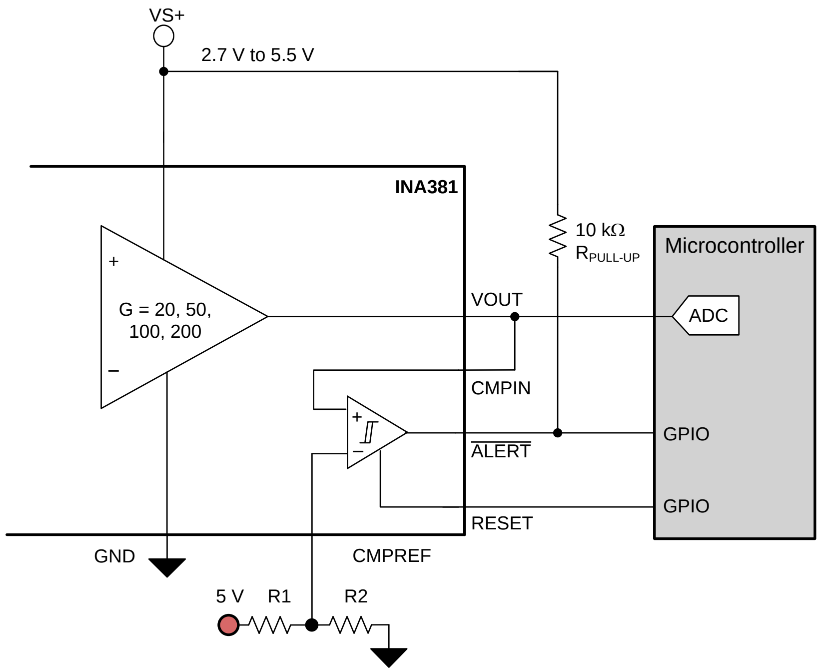


图 43. Resistor Divider Voltage

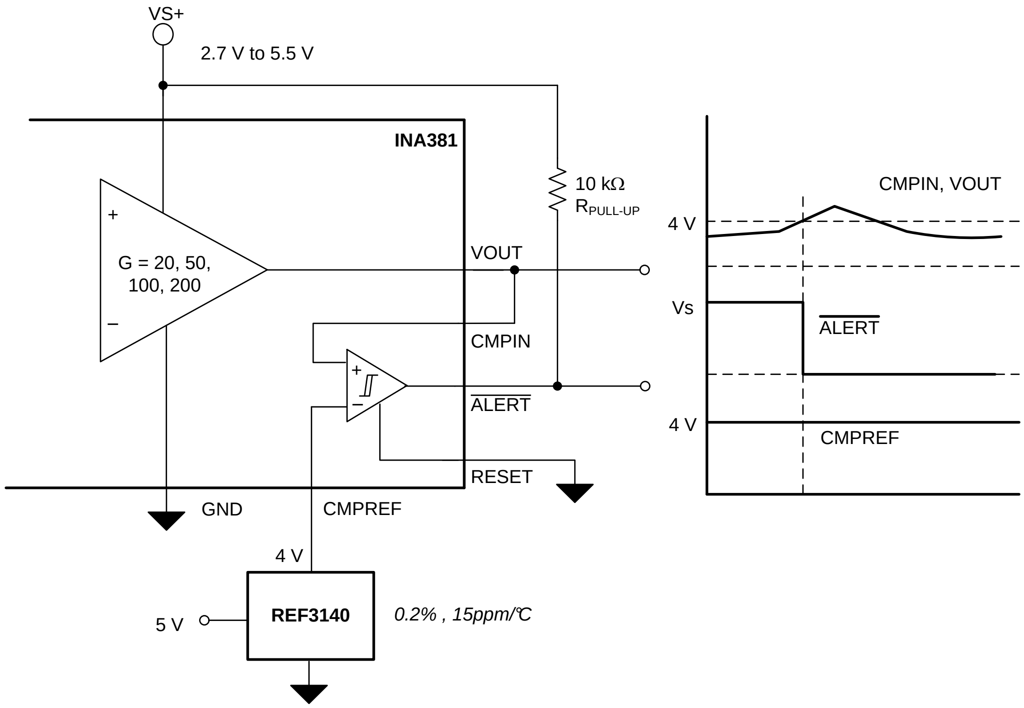


图 44. External Reference Voltage

7.3.7 Selecting a Current-Sensing Resistor

The device measures the differential voltage developed across a resistor when current flows through the component to determine if the current being monitored exceeds a defined limit. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of the device allows for measuring a wide differential input signal range across this current-sensing resistor.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger-value, current-sensing resistors inherently improves measurement accuracy.

However, a system design trade-off must be evaluated through use of larger input signals for improving the measurement accuracy. Increasing the current-sense resistor value results in increased power dissipation across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming more widely available with values reaching down as low as 1 mΩ or lower with power dissipations of up to 5 W that enable large currents to be accurately monitored with sensing resistors.

7.3.7.1 *Selecting a Current-Sensing Resistor: Example*

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires 5% accuracy for detecting a 10-A overcurrent event under 20 µs where only 250 mW is allowable for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Given the total error budget of 5%, the INA381 total error is less than 1%. The INA381 is well suited for this application because up to 1% of error is available to be attributed to the measurement error of the device under these conditions.

As shown in 表 2, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error to reduce the value of the current-sensing resistor and reduce the power dissipation further. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% and still remaining within the accuracy region.

表 2. Calculating the Current-Sensing Resistor (R_{SENSE})

PARAMETER		EQUATION	VALUE	UNIT
I_{MAX}	Maximum current		10	A
P_{D_MAX}	Maximum allowable power dissipation		250	mW
R_{SENSE_MAX}	Maximum allowable R_{SENSE}	P_{D_MAX} / I_{MAX}^2	2.5	mΩ
V_{OS}	Offset voltage, V_{CM} = 12 V		500	µV
V_{OS_ERROR}	Initial offset voltage error	$(V_{OS} / (R_{SENSE\_MAX} \times I_{MAX}) \times 100$	2%	
E_G	Gain error		1%	
$ERROR_{TOTAL}$	Total measurement error	$\sqrt{(V_{OS\_ERROR}^2 + E_G^2)}$	2.23%	
	Allowable current threshold accuracy		5%	
t_p	Total system overcurrent response time		10	µs
	Allowable overcurrent response		20	µs

7.3.8 Hysteresis

The on-board comparator in the INA381 is designed to reduce the possibility of oscillations in the alert output when the measured signal level is near the overlimit threshold level as a result of noise. When the voltage (V_{CMPIN}) exceeds the voltage developed at the CMPREF pin, the $\overline{ALERT}$ pin asserts and pulls low. The output voltage must drop below the CMPREF pin threshold voltage, as shown in 图 45, by the hysteresis level of 50 mV for the $\overline{ALERT}$ pin to de-assert and return to the nominal high state. The INA381 is designed with a hysteresis of 50 mV.

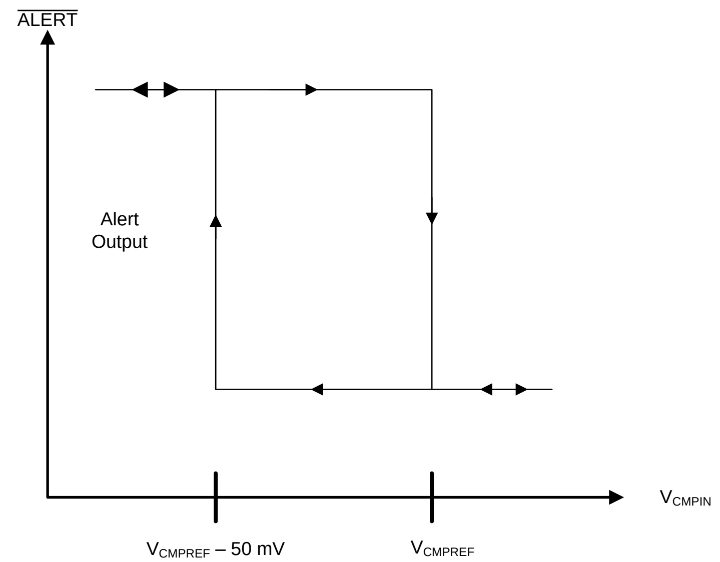


图 45. Typical Comparator Hysteresis

7.4 Device Functional Modes

7.4.1 Input Filtering

Provided that the INA381 output is connected to a high-impedance input, the best location to filter is at the device output using a simple RC network from VOUT to GND. Filtering at the output attenuates high-frequency disturbances in the common-mode voltage, differential input signal, and INA381 power-supply voltage. If filtering at the output is not possible, or if only the differential input signal needs filtering, a filter can be applied at the input pins of the device.

External filtering can help reduce the amount of noise that reaches the comparator, and thereby reduce the likelihood of a false alert from occurring. The tradeoff to adding this noise filter is that the alert response time is increased because both the input signal and noise are filtered. 图 46 shows the implementation of an input filter for the device.

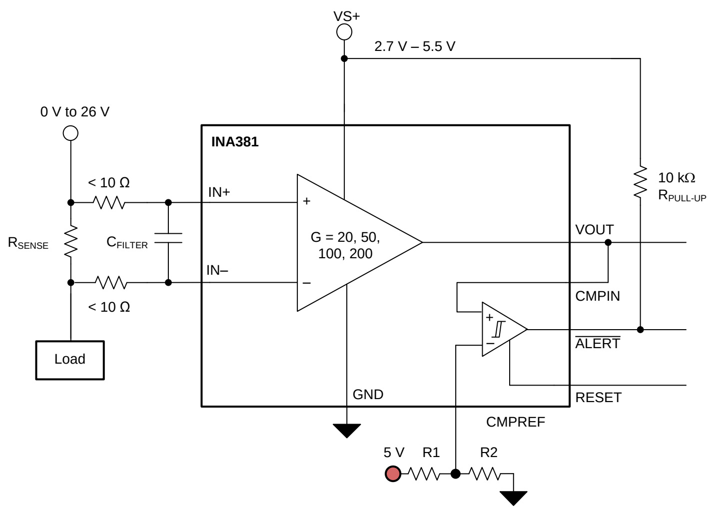


图 46. Input Filter

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in 图 46 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. 公式 2 calculates the amount of error these external filter resistors add to the measurement. 公式 1 calculates the gain error factor.

公式 1 shows that the amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance (R_F) value as well as internal input resistor R_{INT}. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Use 公式 1 to calculate the expected deviation from the shunt voltage to what is measured at the device input pins:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})}$$

where:

- R_{INT} is the internal input resistor
- R_F is the external series resistance (1)

Device Functional Modes (接下页)

With the adjustment factor from 公式 1, including the device internal input resistance shown in 表 3, this factor varies with each gain version. 表 4 lists each individual device gain error factor.

表 3. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA381A1	20	25
INA381A2	50	10
INA381A3	100	5
INA381A4	200	2.5

表 4. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA381A1	$\frac{25000}{(21 \times R_F) + 25000}$
INA381A2	$\frac{10000}{(9 \times R_F) + 10000}$
INA381A3	$\frac{1000}{R_F + 1000}$
INA381A4	$\frac{2500}{(3 \times R_F) + 2500}$

公式 2 can then calculate the gain error that can be expected from the addition of the external series resistors:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA381A2 and the corresponding gain error equation from 表 4, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 公式 2, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.

7.4.2 Adjustable Hysteresis

The device onboard comparator is designed with a hysteresis of 50 mV. The INA381 is designed for the user to change the hysteresis from a preset value of 50 mV by connecting an external resistor between VOUT and CMPIN. 图 47 shows a detailed block diagram of adding additional hysteresis.

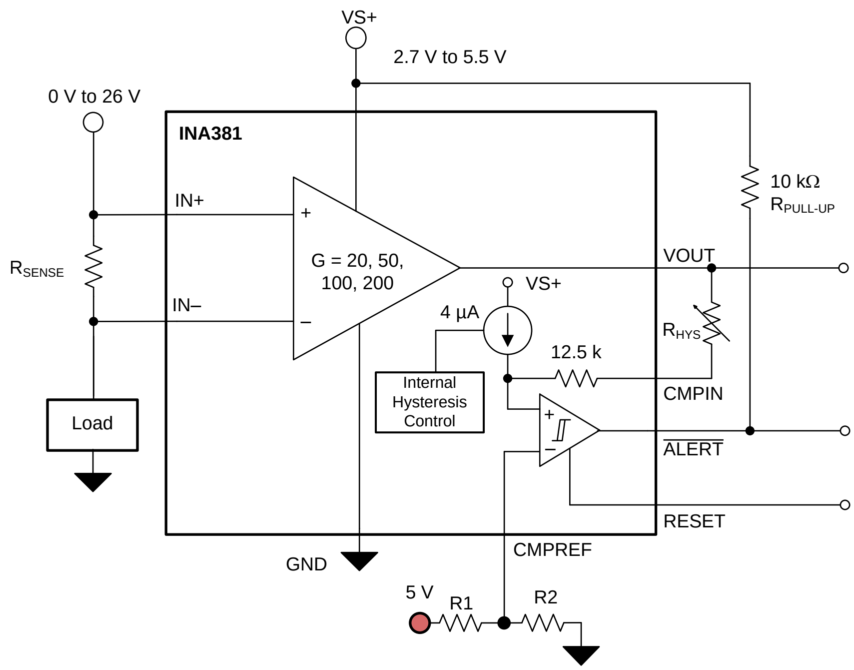


图 47. Adding Additional Hysteresis to the Comparator

Hysteresis is internally designed to preset to 50 mV in the INA381. Internal to the comparator, the INA381 has a current source of 4 µA in series with 12.5 kΩ. The internal current source and hysteresis of the comparator is set by the internal hysteresis control circuit that is enabled only after $\overline{ALERT}$ is asserted low. $\overline{ALERT}$ is asserted during an overcurrent condition when the voltage on VOUT exceeds the threshold set on the CMPREF pin. The internal 4-µA hysteresis circuits are triggered only after $\overline{ALERT}$ is asserted.

To set additional hysteresis higher than 50 mV, the R_{HYS} resistor must be connected between the VOUT and CMPIN pin. 公式 3 and 公式 4 describe the internal configuration to set the external hysteresis resistor.

$$V_{HYS} = 4\mu A \times (12500\Omega + R_{HYS}) \tag{3}$$

$$R_{HYS} = \frac{V_{HYS} - (4\mu A \times 12500\Omega)}{4\mu A} \tag{4}$$

where

- V_{HYS} is the desired hysteresis voltage
- R_{HYS} is the external resistor on the input of the CMPIN pin

表 5 lists the external resistors required at the input of the CMPIN pin to set the hysteresis.

表 5. Hysteresis Resistor Selection

HYSTERESIS VOLTAGE	EXTERNAL RESISTOR AT THE CMPIN PIN
50 mV	0 Ω
75 mV	6.25 kΩ
100 mV	12.5 kΩ
125 mV	18.75 kΩ
150 mV	25 kΩ
200 mV	37.5 kΩ
250 mV	50 kΩ
300 mV	62.5 kΩ

7.4.3 Using the INA381 With Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA381 can be used in circuits subject to transients higher than 26 V. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as shown in 图 48 as a working impedance for the Zener diode. Keep these resistors as small as possible; most often approximately 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Input Filtering* section. This circuit limits only short-term transients and, therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

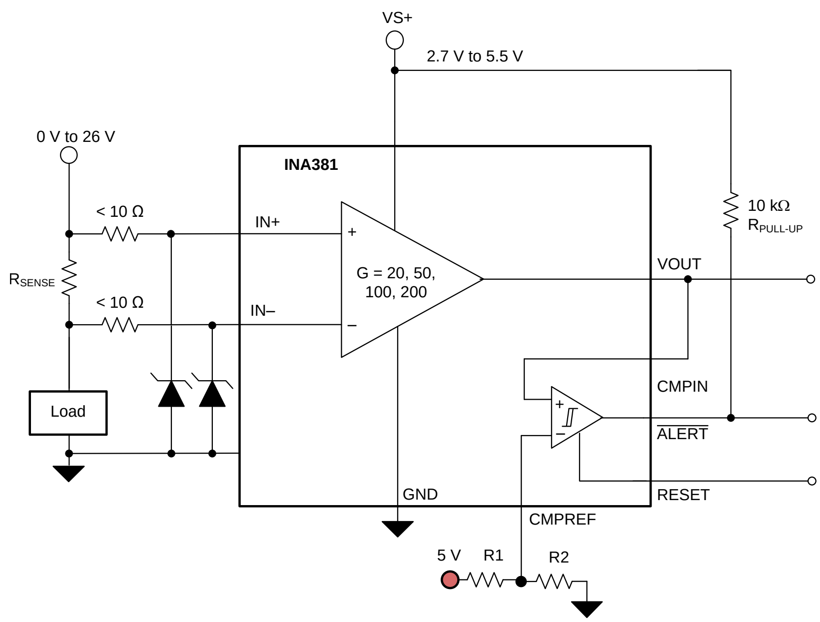


图 48. Transient Protection

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. 图 48 shows that the most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples provided in 图 48 and 图 49, the total board area required by the INA381 with all protective components is less than that of an SOIC-8 package, and only slightly greater than that of a VSSOP-8 package.

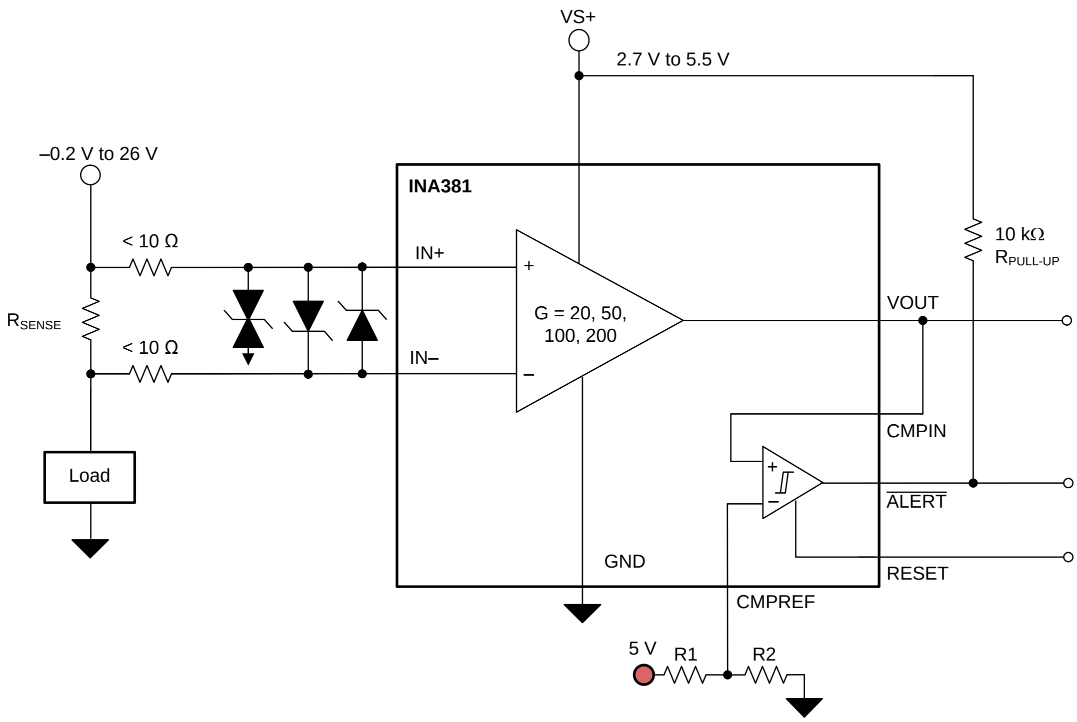


图 49. Transient Protection Using a Single Transzorb and Input Clamps

8 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA381 is designed to enable easy configuration for detecting overcurrent conditions in an application. This device is individually targeted towards unidirectional overcurrent detection of a single threshold. However, this device can also be paired with additional devices and circuitry to create more complex monitoring functional blocks.

8.2 Typical Applications

8.2.1 Typical Bidirectional Window Comparator Application

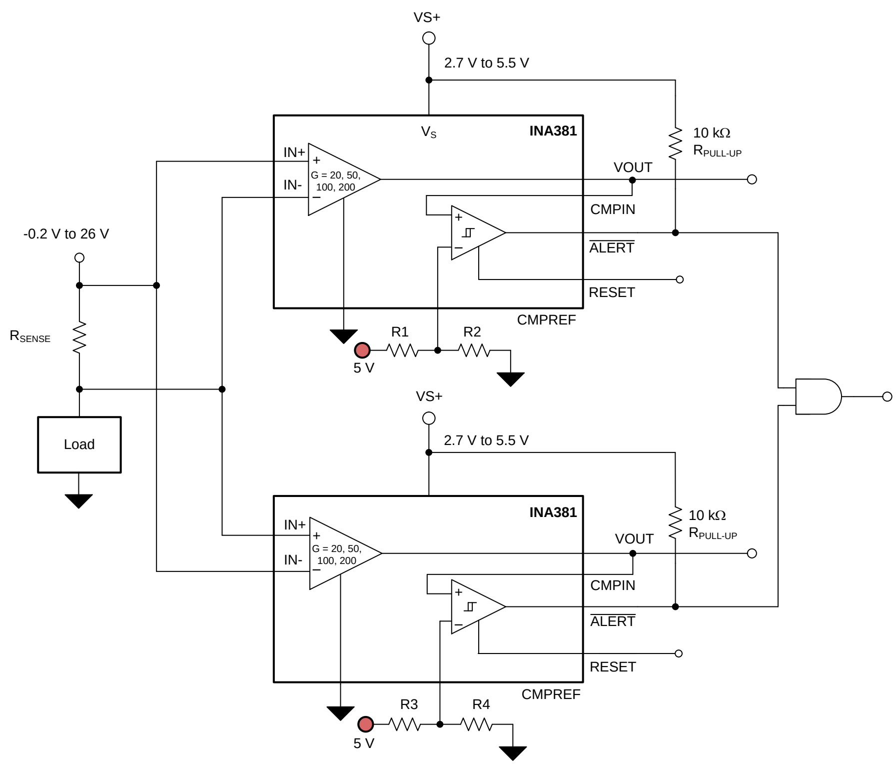


图 50. Bidirectional Application

Typical Applications (接下页)

8.2.1.1 Design Requirements

Although the INA381 is only able to measure current through a current-sensing resistor flowing in one direction, a second INA381 can be used to create a bidirectional monitor. 表 6 lists a system design example of a high-side INA381 measuring in the forward direction and one low-side INA381 measuring in the reverse direction. This example designs for maximum accuracy and also uses the alert function of both devices.

表 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_{SENSE}	12 mΩ
Power-supply voltage	5 V
Common-mode voltage	20 V
Maximum sense current	20 A
Small-signal bandwidth	> 120 kHz
Alert current threshold	19 A

8.2.1.2 Detailed Design Procedure

Although the device is only able to measure current through a current-sensing resistor flowing in one direction, a second INA381 can be used to create a bidirectional monitor. With the input pins of a second device reversed across the same current-sensing resistor, the second device is now able to detect current flowing in the other direction relative to the first device; see 图 50. The outputs of each device connect to an AND gate to detect if either of the limit threshold levels are exceeded. As shown in 表 7, the output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that either the positive overcurrent limit or the negative overcurrent limit is surpassed.

In this scenario, the maximum current expected through the shunt resistor is 20 A in either the forward or reverse direction. Because maximum accuracy is desired, the shunt resistor is maximized by taking the maximum output swing divided by the smallest gain and divided by the maximum current. The design example in 表 6 yields a shunt value of 12.3 mΩ. The closest standard 1% and 0.1% device is 12 mΩ and this value is used by both INA381 devices.

Because corrective action must be taken when the current exceeds ±19 A, the comparators require a value of 4.56 V (19 A × 0.012 Ω × 20 V/V). In this instance, a voltage divider consisting of two 4.53-kΩ resistors (R1 and R3) and two 5-kΩ resistors (R2 and R4) off the 5-V rail supply a voltage close to this value. To ensure that both device alert functions can trigger a single GPIO pin on a microcontroller, both comparator outputs feed into an AND gate. As shown in 表 7, the output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that either the positive overcurrent limit or the negative overcurrent limit is surpassed.

表 7. Bidirectional Overcurrent Output Status

OCP STATUS	OUTPUT
OCP+	0
OCP–	0
No OCP	1

8.2.1.3 Application Curve

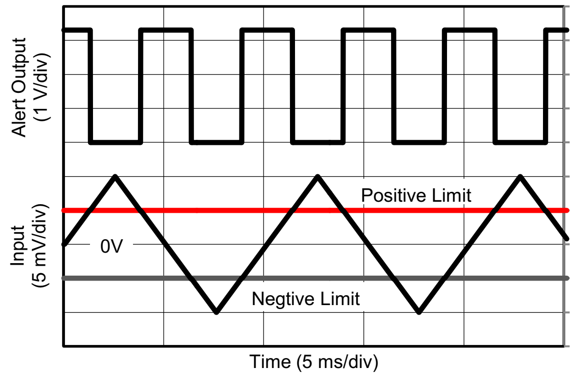


图 51. Bidirectional Application Curve

8.2.2 Typical Low-Side Sensing

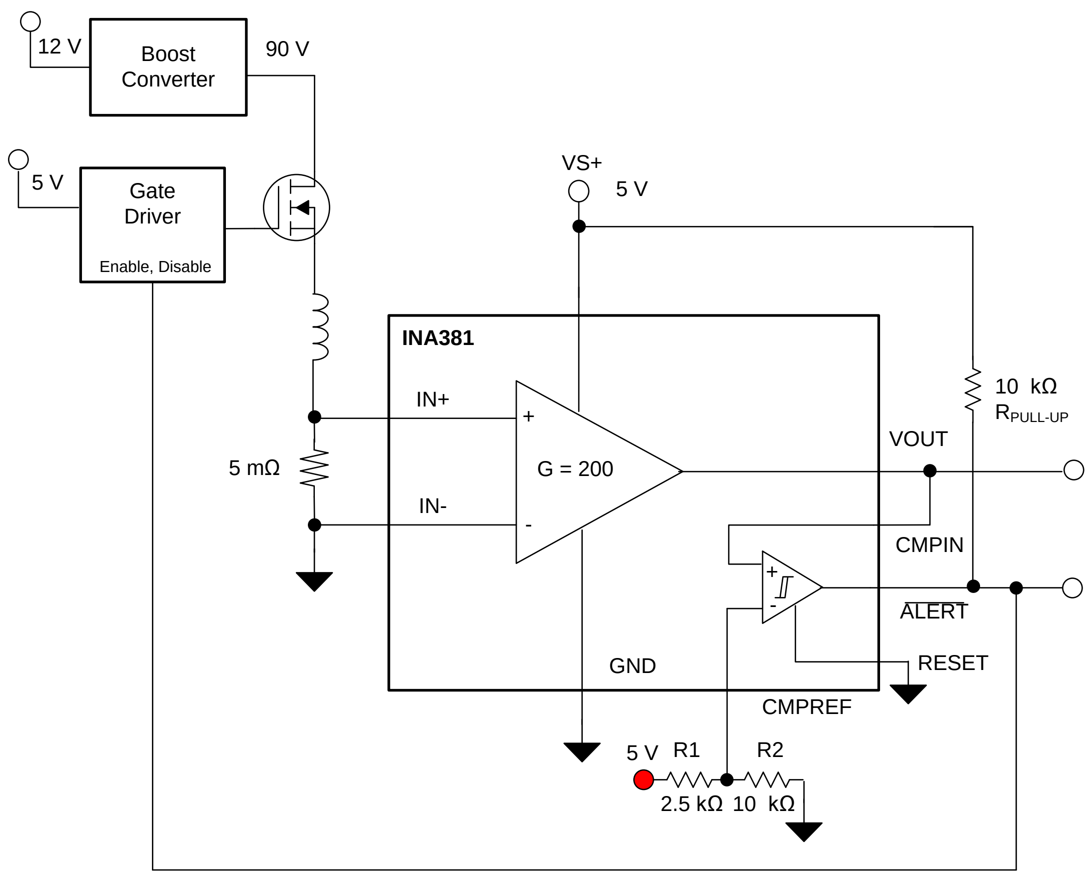


图 52. Solenoid Low-Side Current Sensing Application

8.2.2.1 Design Requirements

表 8 lists the parameters of an application design using the INA381 and $\overline{\text{ALERT}}$ functionality to create a low-side current-sense amplifier with less than a 20-µs system shutdown.

表 8. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Power-supply voltage	5 V
Low-side current sensing	V_{CM} = 0 V
Mode of operation	Unidirectional
Maximum current sense threshold	4.0 A
$\overline{\text{ALERT}}$ response time	< 20 µs
$\overline{\text{ALERT}}$ pin mode	Transparent
R_{SENSE} resistor	5 mΩ
Gain option	200 V/V

8.2.2.2 Detailed Design Procedure

The INA381 can measure current across a shunt resistor with common-mode voltage ranges from –0.3 V to 26 V. The INA381 is capable of measuring low-side current sensing allowing enough margin below ground to accurately measure current through the load. One common application for low-side current sensing is a solenoid control application. As described in 图 52, a typical high voltage solenoid application consists of a high voltage NMOS transistor, a low ohmic shunt resistor connected to the source of the NMOS transistor, and a solenoid. A solenoid is typically used for applications that can control a relay that can be triggered to an ON-OFF state. As current flows through the solenoid, the current flowing through the copper windings generate a magnetic field around the iron that can be used to open or close a relay. Typically industrial valves, electromechanical relays, and PLC control relays are often built of solenoids and the driver circuitry for solenoids are designed discretely as shown in 图 52.

A microcontroller unit is often used to control the duty cycle of the NMOS switch to control the position of the solenoid. By controlling the duty cycle of the solenoid driver the current flowing through the solenoid can be controlled, which in turn can be used to perform position control. However, for applications that need two states, an ON-OFF, a microcontroller can often be expensive and overkill for the application. If a solenoid is located remotely in specific application, the routing of the current-sense amplifier signal back to the microcontroller can create additional overhead and often increase the cost of the application. The INA381 has a built-in comparator that can be programmed to assert an $\overline{\text{ALERT}}$ when the CMPIN signal exceeds the CMPREF threshold signal. The $\overline{\text{ALERT}}$ signal can be used to feed the $\overline{\text{ALERT}}$ signal back to the gate driver circuitry of the NMOS, which can disable the NMOS switch to turn the circuit off to protect itself from damage. Effective impedance of a solenoid is an inductor in series with a resistance. If the solenoid is prone to damage, the inductor can lose its inductance and behave as a shorted resistor. If not protected, high current can flow through the solenoid and often damage the system causing permanent failure. The INA381, with an $\overline{\text{ALERT}}$ pin that can respond as fast as 10 µs, can be directly connected to the NMOS driver to shut the system beyond a current limit and, because the current limits decrease below the safe operating limit, the $\overline{\text{ALERT}}$ clears itself and enables safe operation of the solenoid. The following design example can be used as a guideline to implement the INA381 for a solenoid application.

Based on 公式 5, the design example for the CMPREF voltage is 4 V. The threshold voltage is set using simple resistor dividers R1 and R2. R1 is set with 2.5 kΩ and R2 is set with 10 kΩ. This 4-V threshold is set at the CMPREF pin. When the current exceeds 4 A, voltage on VOUT exceeds 4 V and the $\overline{\text{ALERT}}$ pin asserts a low signal indicating a fault detection. The device is configured in transparent mode by connecting the $\overline{\text{RESET}}$ pin to ground. Because of this configuration, when the current signal falls below 4 A of current, the $\overline{\text{ALERT}}$ pin is pulled high and resets the fault detection, ensuring safe operation of the solenoid. This example explains a methodology where a solenoid can be self-protected and triggered based on a set safe-operating current threshold.

$$\text{CMPREF (V)} = [\text{Alert Threshold (A)} \times \text{Shunt Resistor } (\Omega) + V_{OS}\text{ (V)}] \times \text{Gain} \quad (5)$$

In this application, 4 A and higher are considered overcurrent conditions and some corrective action must be taken to prevent the current from destroying the system. The INA381 offers corrective action through an ALERT pin that can be tailored for a specific overcurrent condition through the CMPREF pin. To set the proper CMPREF value, a gain option and an R_{SENSE} value must first be determined. This design example uses a gain of 200 V/V and an R_{SENSE} value of 5 mΩ. CMPREF is calculated according to 公式 5 in this particular case. This value is calculated to be approximately 4 V. This value can be achieved through either a voltage divider or LDO. In this particular instance, the voltage divider was chosen.

8.2.2.3 Application Curve

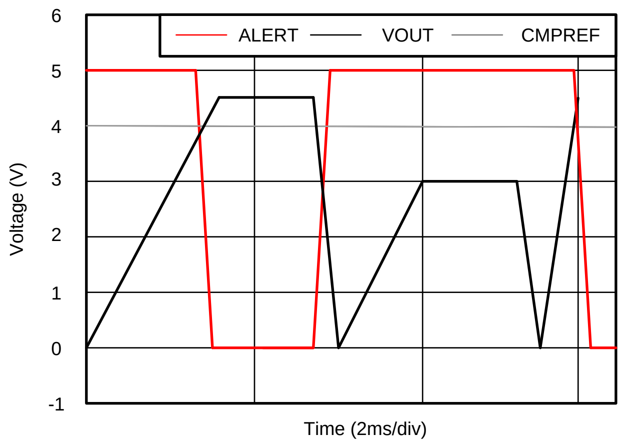


图 53. Low-Side Sensing Application Curve

9 Power Supply Recommendations

The device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power-supply pin can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 26 V. The device can withstand the full –0.2-V to 26-V range at the input pins, regardless of whether the device has power applied or not.

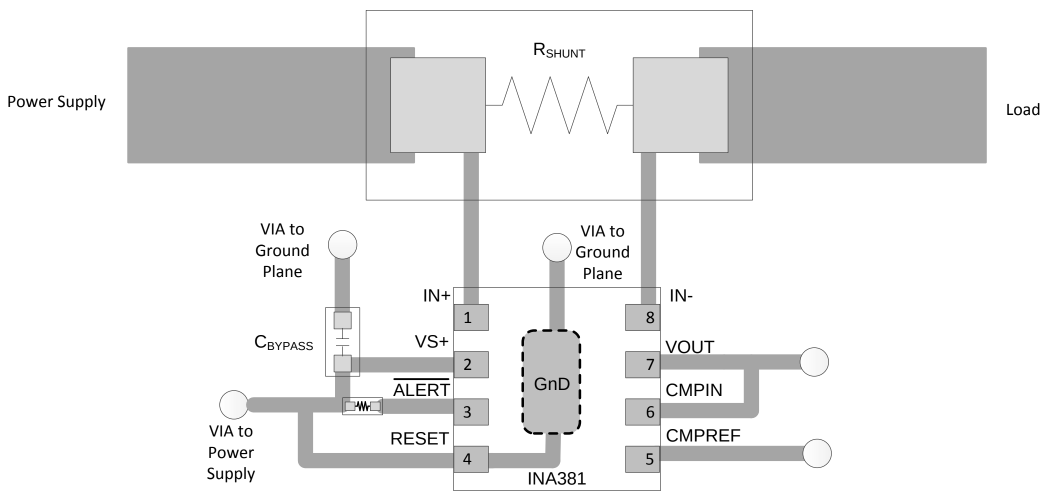
Power-supply bypass capacitors are required for stability and must be placed as closely as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Make sure the thermal pad and GND are connected to a solid ground plane of the PCB.
- The open-drain output pin is recommended to be pulled up to the supply voltage rail through a 10-kΩ pullup resistor.

10.2 Layout Example



NOTE: Connect the limit resistor directly to the GND pin.

图 54. Recommended Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：:

《REF31xx 15ppm/°C 最大值、100μA、SOT-23 系列电压基准》

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区***。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

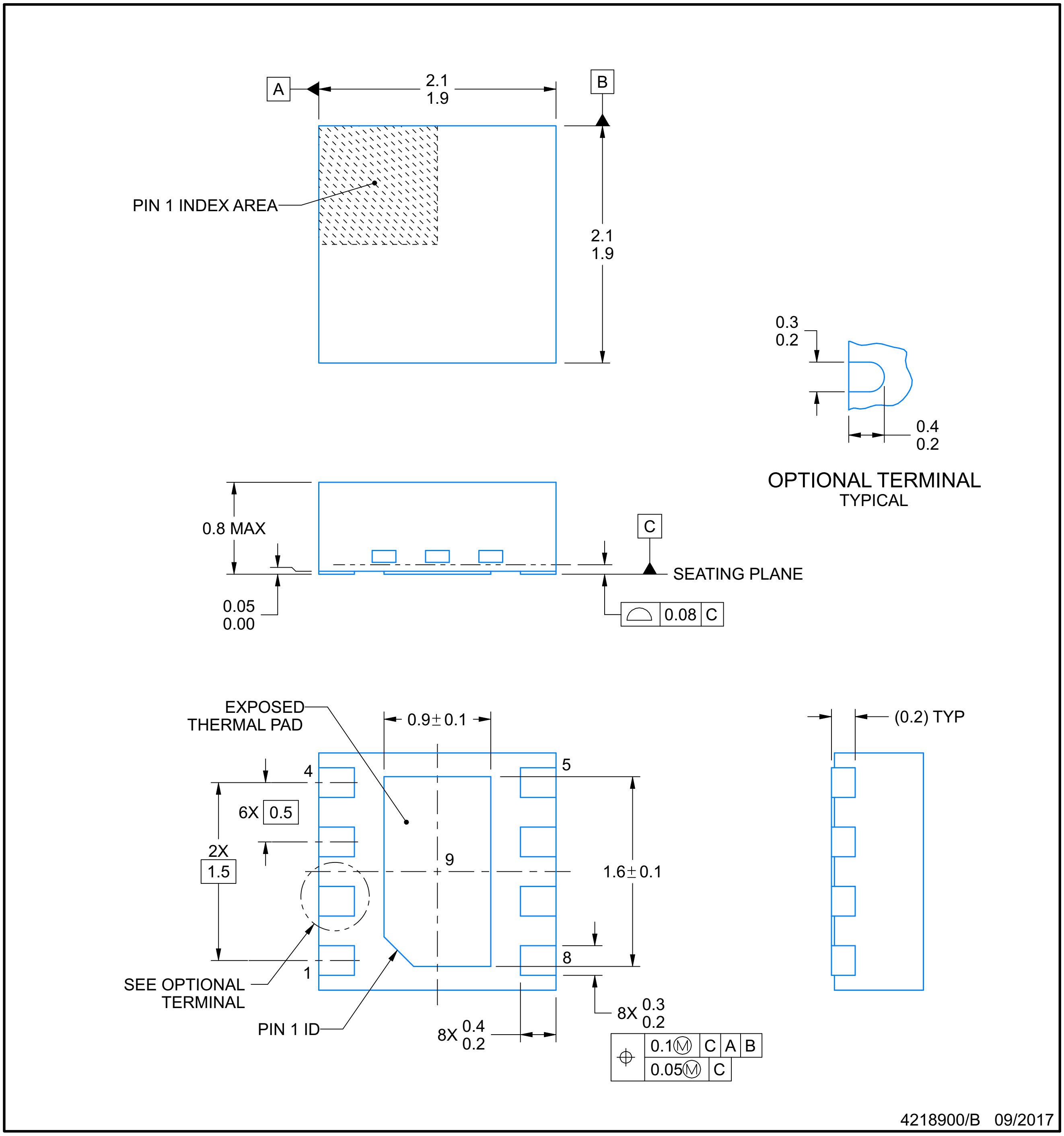
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

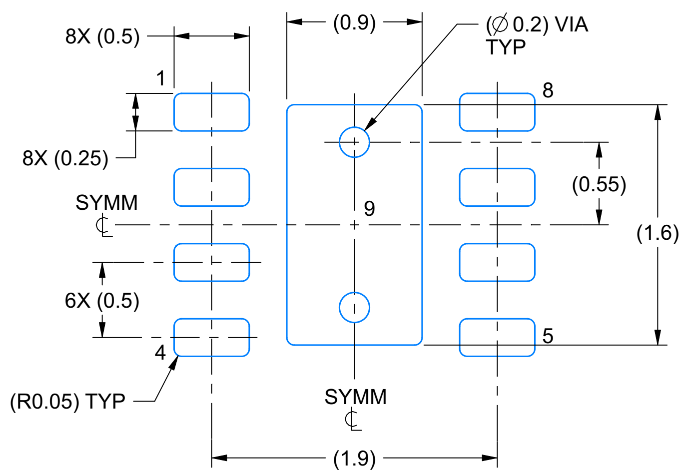
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/B 09/2017

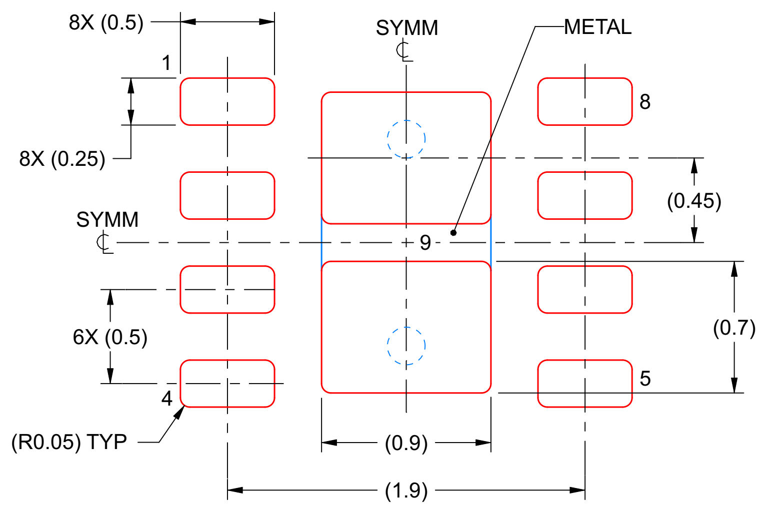
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/B 09/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA381A1IDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HWY	Samples
INA381A1IDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HWY	Samples
INA381A2IDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HXY	Samples
INA381A2IDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HXY	Samples
INA381A3IDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HZY	Samples
INA381A3IDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1HZY	Samples
INA381A4IDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I1Y	Samples
INA381A4IDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I1Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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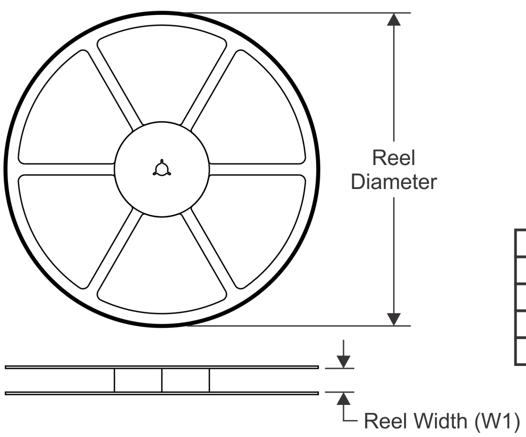
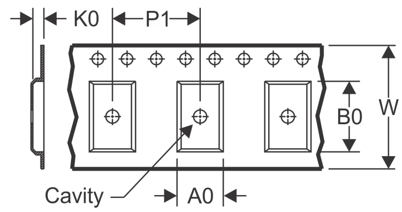
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

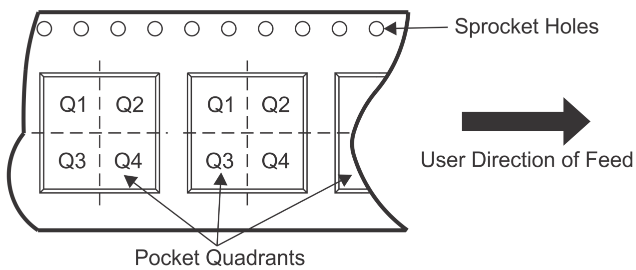


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

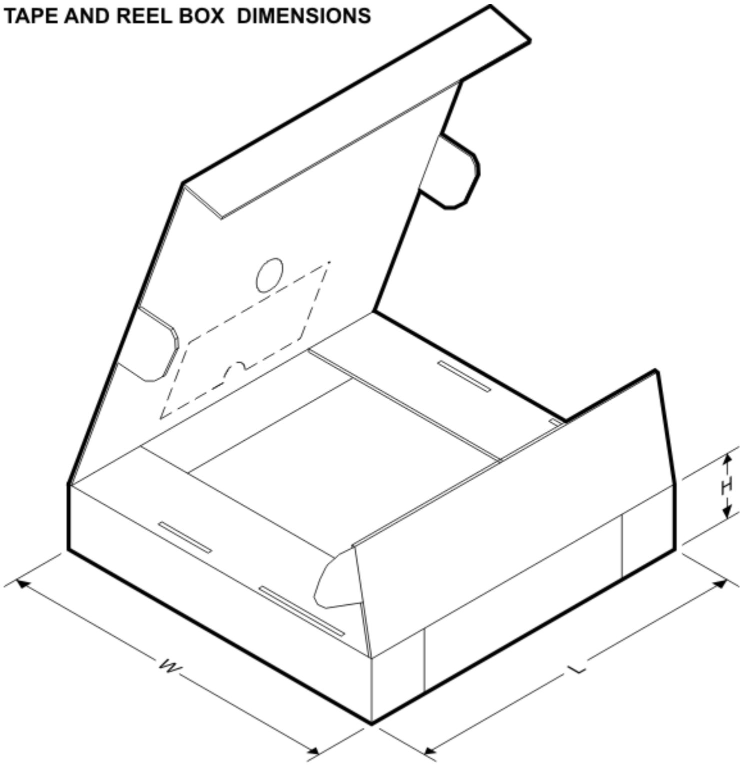
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA381A1IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A1IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A2IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A2IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A3IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A3IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A4IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA381A4IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA381A1IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A1IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
INA381A2IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A2IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
INA381A3IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A3IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
INA381A4IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA381A4IDSGT	WSON	DSG	8	250	210.0	185.0	35.0

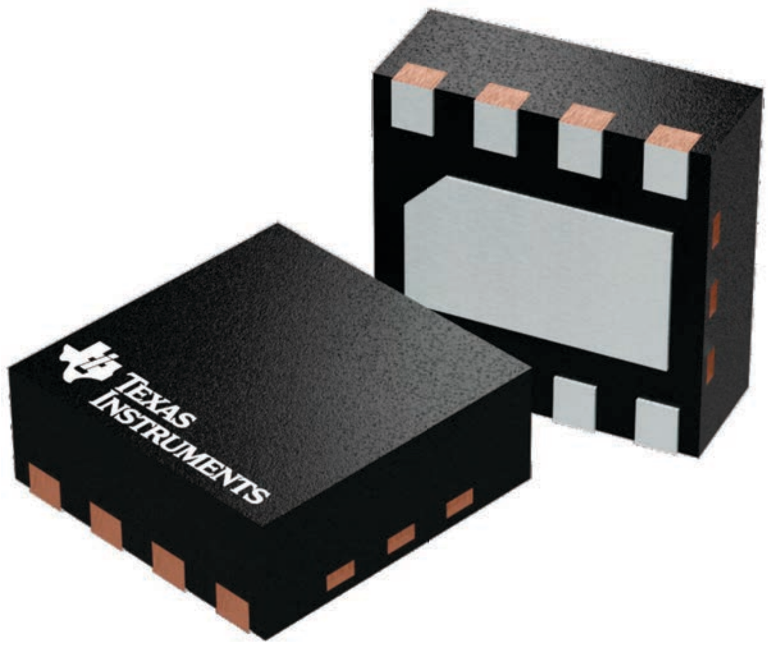
DSG 8

WSON - 0.8 mm max height

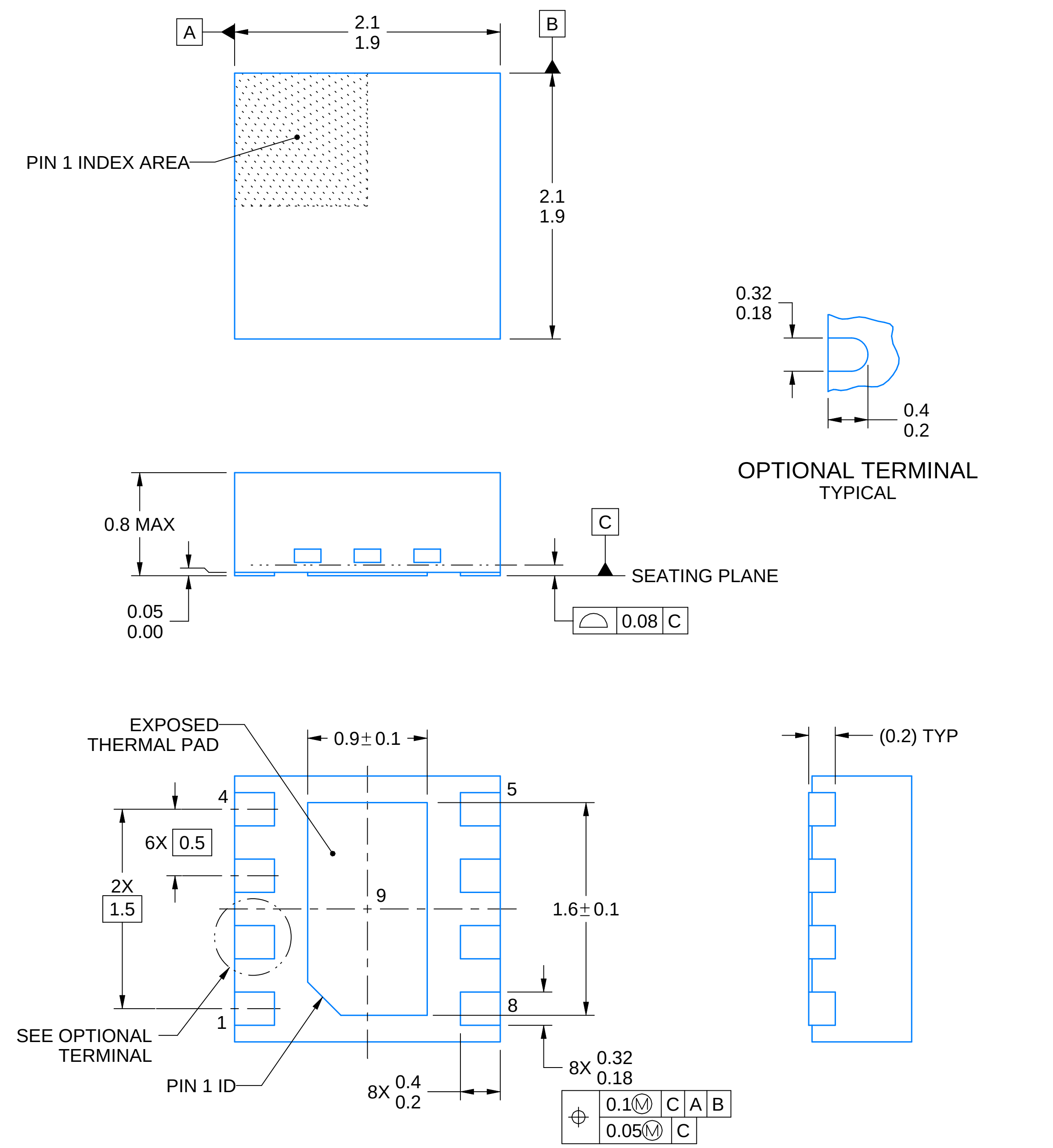
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



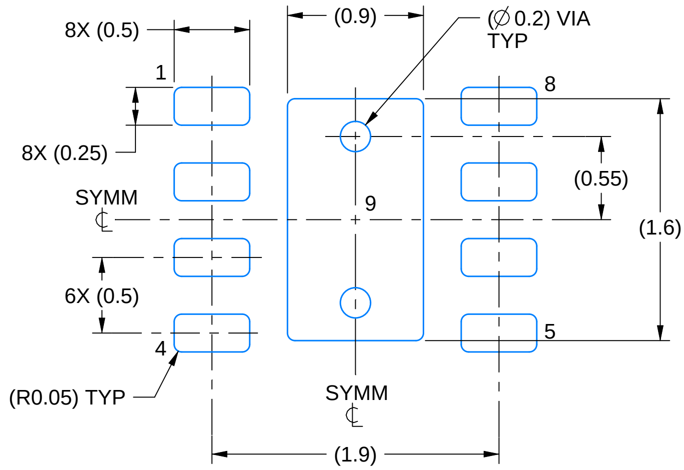
4224783/A



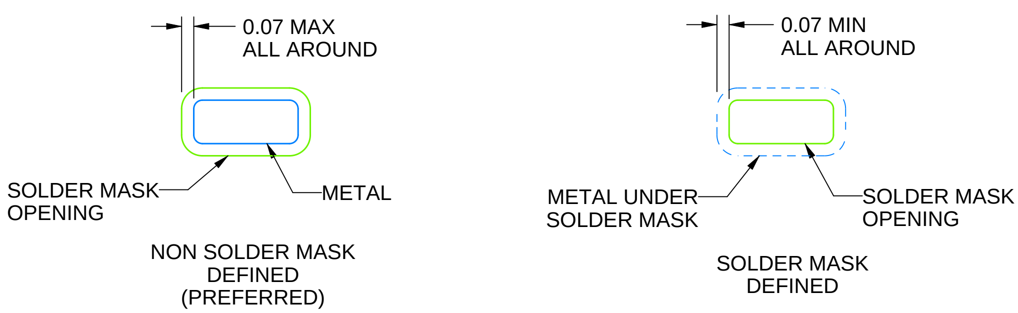
4218900/C 04/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

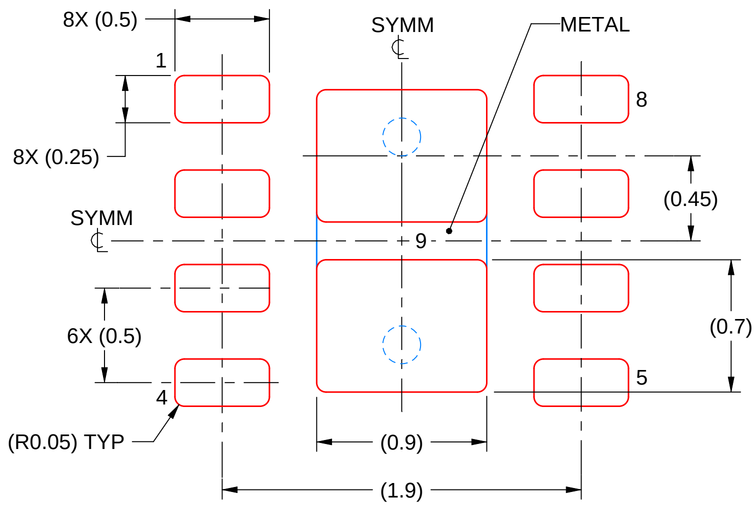


SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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