# 超低功耗，轨到轨输出，负电源轨输入，电压反馈型 (VFB) 运算放大器

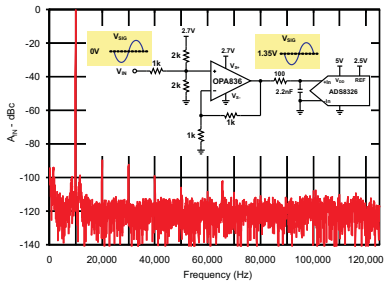
查询样片: OPA836, OPA2836

## 特性

- 低功耗：
  - 电源电压：**2.5V** 至 **5.5V**
  - 静态电流：**1mA**（典型值）
  - 断电模式：**0.5μA**（典型值）
- 带宽：**205MHz**
- 转换率：**560V/μs**
- 上升时间：**3ns (2$V_{STEP}$)**
- 稳定时间：**22ns (2$V_{STEP}$)**
- 过驱恢复时间：**60ns**
- 信噪比 **(SNR)**：在 **1kHz (1$V_{RMS}$)** 时为 **0.00013% (-117.6dBc)**
- 总谐波失真 **(THD)**：在 **1kHz (1$V_{RMS}$)** 时为 **0.00003% (-130dBc)**
- **$HD_2$/$HD_3$**：**1MHz** 时 **(2$V_{PP}$)** 为 **-85dBc/-105dBc**
- 输入电压噪声： **4.6nV/rtHz (f = 100kHz)**
- 输入偏移电压：**65μV**（最大值为 **400μV**）
- 共模抑制比 **(CMRR)**：**116dB**
- 输出驱动电流：**50mA**
- **RRO**：轨到轨输出
- 输入电压范围：**-0.2V** 至 **3.9V**（**5V** 电源）
- 工作温度范围：**-40°C** 至 **+125°C**

## 应用范围

- 低功耗信号调节
- 音频模数转换器 **(ADC)** 输入缓冲器
- 低功耗逐次逼近 **(SAR)** 和三角积分 **(ΔΣ)** 模数转换器 **(ADC)** 驱动器
- 便携式系统
- 低功耗系统
- 高密度系统




## 描述

OPA836 和 OPA2836 采用业界领先的 BiCom-3x（SiGe 互补双极型）工艺制造，是单通道和双通道超低功耗、轨到轨输出、负电源轨输入、电压反馈运算放大器，专为在 2.5V 至 5.5V 的单电源范围和 ±1.25V 至 ±2.75V 的双电源范围内的运行而设计。 每个通道的电流消耗仅为 1mA，并具有 205MHz 的单位增益带宽，这些放大器为轨到轨放大器设定了一个业界领先水平的功耗一性能比。

对于功耗十分重要的电池供电型便携式应用而言，OPA836 和 OPA2836 的低功耗及高频性能为设计人员提供了其他器件所无法获得的性能与功耗比。与流耗小于 1.5μA 的节能模式组合在一起，此器件为电池供电应用中的高频放大器提供了一款极具吸引力的解决方案。

OPA836 和 OPA2836 提供以下封装选项：

- OPA836 单通道：小外形尺寸晶体管 (SOT)23-6(DBV)，和具有集成增益电阻器的 10 引脚极薄四方扁平无引线 (WQFN)(RUN) 封装。
- OPA2836 双通道：小外形尺寸集成电路 (SOIC)-8(D)，超薄型小外形尺寸 (VSSOP) (MSOP)-10(DGS)，10 引脚极薄四方扁平无引线 (WQFN) (RUN) 和 10 引脚超薄四方扁平无引线 (UQFN) (RMC) 封装。 的第二段

OPA836 RUN 封装选项包括在一块印刷电路板上最小可能封装的集成增益设置电阻器 (≈ 2mm x 2mm)。 通过在印刷电路板 (PCB) 上添加电路迹线，可实现 +1，-1，-1.33，+2，+2.33，-3，+4，-4，+5，-5.33，+6.33，-7，+8 的增益和 -0.1429，-0.1875，-0.25，-0.33，-0.75 的反向衰减。 更多细节请参见 应用信息 部分。

该器件的特色是可在 -40°C 至 125°C 的扩展工业温度范围内运行。

**OPA836 相关产品**

| 描述 | 单通道 | 双通道 | 三通道 | 四通道 |
|---|---|---|---|---|
| 轨到轨 | — | OPA2830 | — | OPA4830 |
| 轨到轨，低功耗 | OPA835 | OPA2835 | — | — |
| 轨到轨，固定增益 | OPA832 | OPA2832 | OPA3832 | — |
| 通用，高转换率 | OPA690 | OPA2690 | OPA3690 | — |
| 低噪声，直流高精度 | OPA820 | OPA2822 | — | OPA4820 |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

版权 © 2011–2013, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGING/ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

| | | | UNITS |
|---|---|---|---|
| $V_{S-}$ to $V_{S+}$ | Supply voltage | | 5.5 |
| $V_I$ | Input voltage | | $V_{S-}$ - 0.7V to $V_{S+}$ + 0.7V |
| $V_{ID}$ | Differential input voltage | | 1 V |
| $I_I$ | Continuous input current | | 0.85 mA |
| $I_O$ | Continuous output current | | 60 mA |
| | Continuous power dissipation | | See Thermal Characteristics Specification |
| $T_J$ | Maximum junction temperature | | 150°C |
| $T_A$ | Operating free-air temperature range | | –40°C to 125°C |
| $T_{stg}$ | Storage temperature range | | –65°C to 150°C |
| | ESD ratings | HBM | 6 kV |
| | | CDM | 1 kV |
| | | MM | 200 V |

## THERMAL INFORMATION

| THERMAL METRIC(1) | | OPA836 | | OPA2836 | | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | SOT23-6 (DBV) | WQFN-10 (RUN) | SOIC-8 (D) | VSSOP (MSOP)-10 (DGS) | WQFN-10 (RUN) | UQFN-10 (RMC) | |
| | | 6 PINS | 10 PINS | 8 PINS | 10 PINS | 10 PINS | 10 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 194 | 145.8 | 150.1 | 206 | 145.8 | 143.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 129.2 | 75.1 | 83.8 | 75.3 | 75.1 | 49.0 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 39.4 | 38.9 | 68.4 | 96.2 | 38.9 | 61.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 25.6 | 13.5 | 33.0 | 12.9 | 13.5 | 3.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 38.9 | 104.5 | 67.9 | 94.6 | 104.5 | 61.9 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | n/a | n/a | n/a | |

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：ZHCA543）。


Copyright © 2011–2013, Texas Instruments Incorporated

## SPECIFICATIONS: $V_S$ = 2.7 V

Test conditions unless otherwise noted: $V_{S+}$ = +2.7 V, $V_{S-}$ = 0 V, $V_{OUT}$ = 1 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. $T_A$ = 25°C. Unless otherwise noted

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | TEST LEVEL(1) |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| Small-signal bandwidth | $V_{OUT}$ = 100 $mV_{PP}$, G = 1 | | 200 | | MHz | C |
| | $V_{OUT}$ = 100 $mV_{PP}$, G = 2 | | 100 | | | |
| | $V_{OUT}$ = 100 $mV_{PP}$, G = 5 | | 26 | | | |
| | $V_{OUT}$ = 100 $mV_{PP}$, G = 10 | | 11 | | | |
| Gain-bandwidth product | $V_{OUT}$ = 100 $mV_{PP}$, G = 10 | | 110 | | MHz | C |
| Large-signal bandwidth | $V_{OUT}$ = 1 $V_{PP}$, G = 2 | | 60 | | MHz | C |
| Bandwidth for 0.1dB flatness | $V_{OUT}$ = 1 $V_{PP}$, G=2 | | 25 | | MHz | C |
| Slew rate, Rise/Fall | $V_{OUT}$ = 1$V_{STEP}$, G = 2 | | 260/240 | | V/µs | C |
| Rise/Fall time | | | 4/4.5 | | ns | C |
| Settling time to 1%, Rise/Fall | | | 15/15 | | ns | C |
| Settling time to 0.1%, Rise/Fall | | | 30/25 | | ns | C |
| Settling time to 0.01%, Rise/Fall | | | 50/45 | | ns | C |
| Overshoot/Undershoot | | | 5/3 | | % | C |
| 2nd Order Harmonic Distortion | f = 10 kHz, $V_{IN_CM}$ = mid-supply – 0.5V | | -133 | | dBc | C |
| | f = 100 kHz, $V_{IN_CM}$ = mid-supply – 0.5V | | -120 | | | C |
| | f = 1 MHz, $V_{IN_CM}$ = mid-supply – 0.5V | | -84 | | | C |
| 3rd Order Harmonic Distortion | f = 10 kHz, $V_{IN_CM}$ = mid-supply – 0.5V | | -137 | | dBc | C |
| | f = 100 kHz, $V_{IN_CM}$ = mid-supply – 0.5V | | -130 | | | C |
| | f = 1 MHz, $V_{IN_CM}$ = mid-supply – 0.5V | | -105 | | | C |
| 2nd Order Intermodulation Distortion | f = 1 MHz, 200 kHz Tone Spacing, $V_{OUT}$ Envelope = 1$V_{PP}$, $V_{IN_CM}$ = mid-supply – 0.5V | | -90 | | dBc | C |
| 3rd Order Intermodulation Distortion | | | -90 | | dBc | C |
| Input voltage noise | f = 100 KHz | | 4.6 | | nV/√Hz | C |
| Voltage Noise 1/f corner frequency | | | 215 | | Hz | C |
| Input current noise | f = 1 MHz | | 0.75 | | pA/√Hz | C |
| Current Noise 1/f corner frequency | | | 31.7 | | kHz | C |
| Overdrive recovery time, Over/Under | Overdrive = 0.5 V | | 55/60 | | ns | C |
| Closed-loop output impedance | f = 100 kHz | | 0.02 | | Ω | C |
| Channel to channel crosstalk (OPA2836) | f = 10 kHz | | -120 | | dB | C |

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

Copyright © 2011–2013, Texas Instruments Incorporated

## SPECIFICATIONS: $V_S$ = 2.7 V

Test conditions unless otherwise noted: $V_{S+}$ = +2.7 V, $V_{S-}$ = 0 V, $V_{OUT}$ = 1 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. $T_A$ = 25°C. Unless otherwise noted

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | TEST LEVEL(1) |
|---|---|---|---|---|---|---|
| **DC PERFORMANCE** | | | | | | |
| Open-loop voltage gain ($A_{OL}$) | | 100 | 125 | | dB | A |
| Input referred offset voltage | $T_A$ = 25°C | | ±65 | ±400 | µV | A |
| | $T_A$ = 0°C to 70°C | | | ±680 | | B |
| | $T_A$ = –40°C to 85°C | | | ±760 | | |
| | $T_A$ = –40°C to 125°C | | | ±1060 | | |
| Input offset voltage drift(2) | $T_A$ = 0°C to 70°C | | ±1 | ±6.2 | µV/°C | B |
| | $T_A$ = –40°C to 85°C | | ±1 | ±6 | | |
| | $T_A$ = –40°C to 125°C | | ±1.1 | ±6.6 | | |
| Input bias current | $T_A$ = 25°C | 300 | 650 | 1000 | nA | A |
| | $T_A$ = 0°C to 70°C | 190 | | 1400 | | B |
| | $T_A$ = –40°C to 85°C | 120 | | 1500 | | |
| | $T_A$ = –40°C to 125°C | 120 | | 1800 | | |
| Input bias current drift(2) | $T_A$ = 0°C to 70°C | | ±0.33 | ±2 | nA/°C | B |
| | $T_A$ = –40°C to 85°C | | ±0.32 | ±1.9 | | |
| | $T_A$ = –40°C to 125°C | | ±0.37 | ±2.1 | | |
| Input offset current | $T_A$ = 25°C | | ±30 | ±180 | nA | A |
| | $T_A$ = 0°C to 70°C | | ±30 | ±200 | | B |
| | $T_A$ = –40°C to 85°C | | ±30 | ±215 | | |
| | $T_A$ = –40°C to 125°C | | ±30 | ±240 | | |
| Input offset current drift(2) | $T_A$ = 0°C to 70°C | | ±77 | ±460 | pA/°C | B |
| | $T_A$ = –40°C to 85°C | | ±95 | ±575 | | |
| | $T_A$ = –40°C to 125°C | | ±100 | ±600 | | |
| **INPUT** | | | | | | |
| Common-mode input range low | $T_A$ = 25°C, <3dB degradation in CMRR limit | | –0.2 | 0 | V | A |
| | $T_A$ = –40°C to 125°C, <3dB degradation in CMRR limit | | –0.2 | 0 | V | B |
| Common-mode input range high | $T_A$ = 25°C, <3dB degradation in CMRR limit | 1.5 | 1.6 | | V | A |
| | $T_A$ = –40°C to 125°C, <3dB degradation in CMRR limit | 1.5 | 1.6 | | V | B |
| Input linear operating voltage range | $T_A$ = 25°C, <6dB degradation in THD | | -0.3 to 1.75 | | V | C |
| Common-mode rejection ratio | | 91 | 114 | | dB | A |
| Input impedance common mode | | | 200\|\|1.2 | | kΩ \|\| pF | C |
| Input impedance differential mode | | | 200\|\|1 | | kΩ \|\| pF | C |
| **OUTPUT** | | | | | | |
| Linear output voltage low | $T_A$ = 25°C, G = 5 | | 0.15 | 0.2 | V | A |
| | $T_A$ = –40°C to 125°C, G = 5 | | 0.15 | 0.2 | V | B |
| Linear output voltage high | $T_A$ = 25°C, G = 5 | 2.45 | 2.5 | | V | A |
| | $T_A$ = –40°C to 125°C, G = 5 | 2.45 | 2.5 | | V | B |
| Output saturation voltage, High / Low | $T_A$ = 25°C, G = 5 | | 80/40 | | mV | C |
| Linear output current drive | $T_A$ = 25°C | ±40 | ±45 | | mA | A |
| | $T_A$ = –40°C to 125°C | ±40 | ±45 | | mA | B |

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.


Copyright © 2011–2013, Texas Instruments Incorporated

## SPECIFICATIONS: $V_S$ = 2.7 V (continued)

Test conditions unless otherwise noted: $V_{S+}$ = +2.7 V, $V_{S–}$ = 0 V, $V_{OUT}$ = 1 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. $T_A$ = 25°C. Unless otherwise noted

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | TEST LEVEL(1) |
|---|---|---|---|---|---|---|
| **GAIN SETTING RESISTORS (OPA836IRUN ONLY)** | | | | | | |
| Resistor FB1 to FB2 | DC resistance | 1584 | 1600 | 1616 | Ω | A |
| Resistor FB2 to FB3 | DC resistance | 1188 | 1200 | 1212 | Ω | A |
| Resistor FB3 to FB4 | DC resistance | 396 | 400 | 404 | Ω | A |
| Resistor Tolerance | DC resistance | | | ±1 | % | A |
| Resistor Temperature Coefficient | DC resistance | | <10 | | PPM | C |
| **POWER SUPPLY** | | | | | | |
| Specified operating voltage | | 2.5 | | 5.5 | V | B |
| Quiescent operating current per amplifer | $T_A$ = 25°C | 0.7 | 0.95 | 1.15 | mA | A |
| | $T_A$ = –40°C to 125°C | 0.6 | | 1.4 | mA | B |
| Power supply rejection (±PSRR) | | 91 | 108 | | dB | A |
| **POWER DOWN** | | | | | | |
| Enable voltage threshold | Specified "on" above $V_{S-}$ + 2.1 V | | | 2.1 | V | A |
| Disable voltage threshold | Specified "off" below $V_{S-}$ + 0.7 V | 0.7 | | | V | A |
| Powerdown pin bias current | $\overline{PD}$ = 0.5 V | | 20 | 500 | nA | A |
| Powerdown quiescent current | $\overline{PD}$ = 0. 5 V | | 0.5 | 1.5 | µA | A |
| Turn-on time delay | Time from $\overline{PD}$ = high to $V_{OUT}$ = 90% of final value | | 200 | | ns | C |
| Turn-off time delay | Time from $\overline{PD}$ = low to $V_{OUT}$ = 10% of original value | | 25 | | ns | C |

Copyright © 2011–2013, Texas Instruments Incorporated

## SPECIFICATIONS: $V_S$ = 5 V

Test conditions unless otherwise noted: $V_{S+}$ = +5 V, $V_{S-}$ = 0V, $V_{OUT}$ = 2 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. $T_A$ = 25°C. Unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | TEST LEVEL(1) |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| Small-signal bandwidth | $V_{OUT}$ = 100 $mV_{PP}$, G = 1 | | 205 | | MHz | C |
| | $V_{OUT}$ = 100 $mV_{PP}$, G = 2 | | 100 | | | |
| | $V_{OUT}$ = 100 $mV_{PP}$, G = 5 | | 28 | | | |
| | $V_{OUT}$ = 100 $mV_{PP}$, G = 10 | | 11.8 | | | |
| Gain-bandwidth product | $V_{OUT}$ = 100 $mV_{PP}$, G = 10 | | 118 | | MHz | C |
| Large-signal bandwidth | $V_{OUT}$ = 2 $V_{PP}$, G = 2 | | 87 | | MHz | C |
| Bandwidth for 0.1dB flatness | $V_{OUT}$ = 2 $V_{PP}$, G = 2 | | 29 | | MHz | C |
| Slew rate, Rise/Fall | $V_{OUT}$ = 2V Step, G = 2 | | 560/580 | | V/µs | C |
| Rise/Fall time | | | 3/3 | | ns | C |
| Settling time to 1%, Rise/Fall | | | 22/22 | | ns | C |
| Settling time to 0.1%, Rise/Fall | | | 30/30 | | ns | C |
| Settling time to 0.01%, Rise/Fall | | | 40/45 | | ns | C |
| Overshoot/Undershoot | | | 7.5/5 | | % | C |
| 2nd Order Harmonic Distortion | f = 10 kHz | | –133 | | dBc | C |
| | f = 100 kHz | | –120 | | | C |
| | f = 1 MHz | | –85 | | | C |
| 3rd Order Harmonic Distortion | f = 10 kHz | | –140 | | dBc | C |
| | f = 100 kHz | | –130 | | | C |
| | f = 1 MHz | | –105 | | | C |
| 2nd Order Intermodulation Distortion | f = 1 MHz, 200 kHz Tone Spacing, $V_{OUT}$ Envelope = 2$V_{PP}$ | | –79 | | dBc | C |
| 3rd Order Intermodulation Distortion | | | –91 | | dBc | C |
| Signal to Noise Ratio, SNR | f = 1kHz, $V_{OUT}$ = 1 $V_{RMS}$, 22kHz bandwidth | | 0.00013 | | % | C |
| | | | -117.6 | | dBc | C |
| Total Harmonic Distortion, THD | f = 1kHz, $V_{OUT}$ = 1 $V_{RMS}$ | | 0.00003 | | % | C |
| | | | -130 | | dBc | C |
| Input voltage noise | f = 100 KHz | | 4.6 | | nV/√Hz | C |
| Voltage Noise 1/f corner frequency | | | 215 | | Hz | C |
| Input current noise | f > 1 MHz | | 0.75 | | pA/√Hz | C |
| Current Noise 1/f corner frequency | | | 31.7 | | kHz | C |
| Overdrive recovery time, Over/Under | Overdrive = 0.5 V | | 55/60 | | ns | C |
| Closed-loop output impedance | f = 100 kHz | | 0.02 | | Ω | C |
| Channel to channel crosstalk (OPA2836) | f = 10 kHz | | -120 | | dB | C |

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.


Copyright © 2011–2013, Texas Instruments Incorporated

## SPECIFICATIONS: $V_S$ = 5 V

Test conditions unless otherwise noted: $V_{S+}$ = +5 V, $V_{S-}$ = 0 V, $V_{OUT}$ = 2 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. $T_A$ = 25°C. Unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | TEST LEVEL(1) |
|---|---|---|---|---|---|---|
| **DC PERFORMANCE** | | | | | | |
| Open-loop voltage gain ($A_{OL}$) | | 100 | 122 | | dB | A |
| Input referred offset voltage | $T_A$ = 25°C | | ±65 | ±400 | µV | A |
| | $T_A$ = 0°C to 70°C | | | ±685 | | B |
| | $T_A$ = –40°C to 85°C | | | ±765 | | |
| | $T_A$ = –40°C to 125°C | | | ±1080 | | |
| Input offset voltage drift(2) | $T_A$ = 0°C to 70°C | | ±1.05 | ±6.3 | µV/°C | B |
| | $T_A$ = –40°C to 85°C | | ±1 | ±6.1 | | |
| | $T_A$ = –40°C to 125°C | | ±1.1 | ±6.8 | | |
| Input bias current | $T_A$ = 25°C | 300 | 650 | 1000 | nA | A |
| | $T_A$ = 0°C to 70°C | 190 | | 1400 | | B |
| | $T_A$ = –40°C to 85°C | 120 | | 1550 | | |
| | $T_A$ = –40°C to 125°C | 120 | | 1850 | | |
| Input bias current drift(2) | $T_A$ = 0°C to 70°C | | ±0.34 | ±2 | nA/°C | B |
| | $T_A$ = –40°C to 85°C | | ±0.34 | ±2 | | |
| | $T_A$ = –40°C to 125°C | | ±0.38 | ±2.3 | | |
| Input offset current | $T_A$ = 25°C | | ±30 | ±180 | nA | A |
| | $T_A$ = 0°C to 70°C | | ±30 | ±200 | | B |
| | $T_A$ = –40°C to 85°C | | ±30 | ±215 | | |
| | $T_A$ = –40°C to 125°C | | ±30 | ±250 | | |
| Input offset current drift(2) | $T_A$ = 0°C to 70°C | | ±80 | ±480 | pA/°C | B |
| | $T_A$ = –40°C to 85°C | | ±100 | ±600 | | |
| | $T_A$ = –40°C to 125°C | | ±110 | ±660 | | |
| **INPUT** | | | | | | |
| Common-mode input range low | $T_A$ = 25°C, <3dB degradation in CMRR limit | | –0.2 | 0 | V | A |
| | $T_A$ = –40°C to 125°C, <3dB degradation in CMRR limit | | –0.2 | 0 | V | B |
| Common-mode input range high | $T_A$ = 25°C, <3dB degradation in CMRR limit | 3.8 | 3.9 | | V | A |
| | $T_A$ = –40°C to 125°C, <3dB degradation in CMRR limit | 3.8 | 3.9 | | V | B |
| Input linear operating voltage range | $T_A$ = 25°C, <6dB degradation in THD | | -0.3 to 4.05 | | V | C |
| Common-mode rejection ratio | | 94 | 116 | | dB | A |
| Input impedance common mode | | | 200\|\|1.2 | | kΩ \|\| pF | C |
| Input impedance differential mode | | | 200\|\|1 | | kΩ \|\| pF | C |
| **OUTPUT** | | | | | | |
| Linear output voltage low | $T_A$ = 25°C, G = | | 0.15 | 0.2 | V | A |
| | $T_A$ = –40°C to 125°C, G = 5 | | 0.15 | 0.2 | V | B |
| Linear output voltage high | $T_A$ = 25°C, G = 5 | 4.75 | 4.8 | | V | A |
| | $T_A$ = –40°C to 125°C, G = 5 | 4.75 | 4.8 | | V | B |
| Output saturation voltage, High / Low | $T_A$ = 25°C, G = 5 | | 100/50 | | mV | C |
| Linear output current drive | $T_A$ = 25°C | ±40 | ±50 | | mA | A |
| | $T_A$ = –40°C to 125°C | ±40 | ±50 | | mA | B |

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

Copyright © 2011–2013, Texas Instruments Incorporated

## SPECIFICATIONS: $V_S$ = 5 V (continued)

Test conditions unless otherwise noted: $V_{S+}$ = +5 V, $V_{S-}$ = 0 V, $V_{OUT}$ = 2 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply. $T_A$ = 25°C. Unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | TEST LEVEL(1) |
|---|---|---|---|---|---|---|
| **GAIN SETTING RESISTORS (OPA836IRUN ONLY)** | | | | | | |
| Resistor FB1 to FB2 | DC resistance | 1584 | 1600 | 1616 | Ω | A |
| Resistor FB2 to FB3 | DC resistance | 1188 | 1200 | 1212 | Ω | A |
| Resistor FB3 to FB4 | DC resistance | 396 | 400 | 404 | Ω | A |
| Resistor Tolerance | DC resistance | | | ±1 | % | A |
| Resistor Temperature Coefficient | DC resistance | | <10 | | PPM | C |
| **POWER SUPPLY** | | | | | | |
| Specified operating voltage | | 2.5 | | 5.5 | V | B |
| Quiescent operating current per amplifier | $T_A$ = 25°C | 0.8 | 1.0 | 1.2 | mA | A |
| | $T_A$ = –40°C to 125°C | 0.65 | | 1.5 | mA | B |
| Power supply rejection (±PSRR) | | 94 | 108 | | dB | A |
| **POWER DOWN** | | | | | | |
| Enable voltage threshold | Specified "on" above $V_{S-}$ + 2.1 V | | | 2.1 | V | A |
| Disable voltage threshold | Specified "off" below $V_{S-}$ + 0.7 V | 0.7 | | | V | A |
| Powerdown pin bias current | $\overline{PD}$ = 0.5 V | | 20 | 500 | nA | A |
| Powerdown quiescent current | $\overline{PD}$ = 0.5 V | | 0.5 | 1.5 | µA | A |
| Turn-on time delay | Time from $\overline{PD}$ = high to $V_{OUT}$ = 90% of final value | | 170 | | ns | C |
| Turn-off time delay | Time from $\overline{PD}$ = low to $V_{OUT}$ = 10% of original value | | 35 | | ns | C |

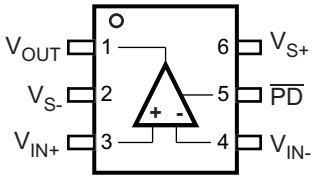

Copyright © 2011–2013, Texas Instruments Incorporated

## DEVICE INFORMATION

### PIN CONFIGURATIONS

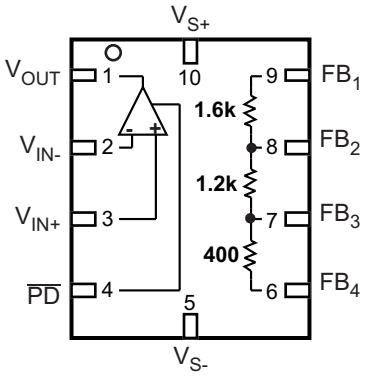
**OPA836 (TOP VIEW)**

**SOT23-6 (DBV)**



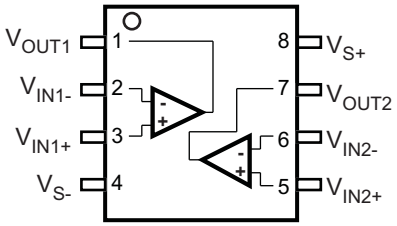

**OPA836 (TOP VIEW)**

**WQFN-10 (RUN)**



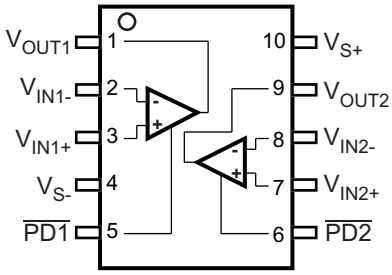

**OPA2836 (TOP VIEW)**

**SOIC-8 (D)**



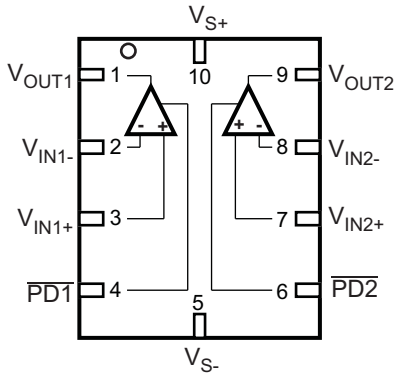

**OPA2836 (TOP VIEW)**

**VSSOP (MSOP)-10 (DGS)**




**OPA2836 (TOP VIEW)**

**WQFN-10 (RUN), UQFN-10 (RMC)**




Copyright © 2011–2013, Texas Instruments Incorporated

## PIN FUNCTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NUMBER | NAME | |
| **OPA836 DBV PACKAGE** | | |
| 1 | $V_{OUT}$ | Amplifier output |
| 2 | $V_{S-}$ | Negative power supply input |
| 3 | $V_{IN+}$ | Amplifier non-inverting input |
| 4 | $V_{IN-}$ | Amplifier inverting input |
| 5 | $\overline{PD}$ | Amplifier Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)** |
| 6 | $V_{S+}$ | Positive power supply input |
| **OPA836 RUN PACKAGE** | | |
| 1 | $V_{OUT}$ | Amplifier output |
| 2 | $V_{IN-}$ | Amplifier inverting input |
| 3 | $V_{IN+}$ | Amplifier non-inverting input |
| 4 | $\overline{PD}$ | Amplifier Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)** |
| 5 | $V_{S-}$ | Negative power supply input |
| 6 | $FB_4$ | Connection to bottom of 250 Ω internal gain setting resistors |
| 7 | $FB_3$ | Connection to junction of 750 and 250 Ω internal gain setting resistors |
| 8 | $FB_2$ | Connection to junction of 1k and 750 Ω internal gain setting resistors |
| 9 | $FB_1$ | Connection to top of 1kΩ internal gain setting resistors |
| 10 | $V_{S+}$ | Positive power supply input |
| **OPA2836 D PACKAGE** | | |
| 1 | $V_{OUT1}$ | Amplifier 1 output |
| 2 | $V_{IN1-}$ | Amplifier 1 inverting input |
| 3 | $V_{IN1+}$ | Amplifier 1 non-inverting input |
| 4 | $V_{S-}$ | Negative power supply input |
| 5 | $V_{IN2+}$ | Amplifier 2 non-inverting input |
| 6 | $V_{IN2-}$ | Amplifier 2 inverting input |
| 7 | $V_{OUT2}$ | Amplifier 2 output |
| 8 | $V_{S+}$ | Positive power supply input |
| **OPA2836 DSG PACKAGE** | | |
| 1 | $V_{OUT1}$ | Amplifier 1 output |
| 2 | $V_{IN1-}$ | Amplifier 1 inverting input |
| 3 | $V_{IN1+}$ | Amplifier 1 non-inverting input |
| 4 | $V_{S-}$ | Negative power supply input |
| 5 | $\overline{PD1}$ | Amplifier 1 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)** |
| 6 | $\overline{PD2}$ | Amplifier 2 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)** |
| 7 | $V_{IN2+}$ | Amplifier 2 non-inverting input |
| 8 | $V_{IN2-}$ | Amplifier 2 inverting input |
| 9 | $V_{OUT2}$ | Amplifier 2 output |
| 10 | $V_{S+}$ | Positive power supply input |


Copyright © 2011–2013, Texas Instruments Incorporated

## PIN FUNCTIONS (continued)

| PIN | | DESCRIPTION |
|---|---|---|
| NUMBER | NAME | |
| **OPA2836 RUN AND RMC PACKAGES** | | |
| 1 | $V_{OUT1}$ | Amplifier 1 output |
| 2 | $V_{IN1-}$ | Amplifier 1 inverting input |
| 3 | $V_{IN1+}$ | Amplifier 1 non-inverting input |
| 4 | $\overline{PD1}$ | Amplifier 1 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)** |
| 5 | $V_{S-}$ | Negative power supply input |
| 6 | $\overline{PD2}$ | Amplifier 2 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)** |
| 7 | $V_{IN2+}$ | Amplifier 2 non-inverting input |
| 8 | $V_{IN2-}$ | Amplifier 2 inverting input |
| 9 | $V_{OUT2}$ | Amplifier 2 output |
| 10 | $V_{S+}$ | Positive power supply input |

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 2.7 V

Test conditions unless otherwise noted: $V_{S+}$ = +2.7 V, $V_{S-}$ = 0 V, $V_{OUT}$ = 1 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply unless otherwise noted. $T_A$ = 25°C.

### Table of Graphs

| | | FIGURES |
|---|---|---|
| Small Signal Frequency Response | | Figure 1 |
| Large Signal Frequency Response | | Figure 2 |
| Noninverting Pulse Response | | Figure 3 |
| Inverting Pulse Response | | Figure 4 |
| Slew rate | vs Output Voltage Step | Figure 5 |
| Output Overdrive Recovery | | Figure 6 |
| Harmonic Distortion | vs Frequency | Figure 7 |
| Harmonic Distortion | vs Load Resistance | Figure 8 |
| Harmonic Distortion | vs Output Voltage | Figure 9 |
| Harmonic Distortion | vs Gain | Figure 10 |
| Output Voltage Swing | vs Load Resistance | Figure 11 |
| Output Saturation Voltage | vs Load Current | Figure 12 |
| Output Impedance | vs Frequency | Figure 13 |
| Frequency Response with Capacitive Load | | Figure 14 |
| Series Output Resistor | vs Capacitive Load | Figure 15 |
| Input Referred Noise | vs Frequency | Figure 16 |
| Open Loop Gain | vs Frequency | Figure 17 |
| Common Mode/Power Supply Rejection Ratios | vs Frequency | Figure 18 |
| Crosstalk | vs Frequency | Figure 19 |
| Power Down Response | | Figure 20 |
| Input Offset Voltage | | Figure 21 |
| Input Offset Voltage | vs Free-Air Temperature | Figure 22 |
| Input Offset Voltage Drift | | Figure 49 |
| Input Offset Current | | Figure 24 |
| Input Offset Current | vs Free-Air Temperature | Figure 25 |
| Input Offset Current Drift | | Figure 26 |

Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 2.7 V

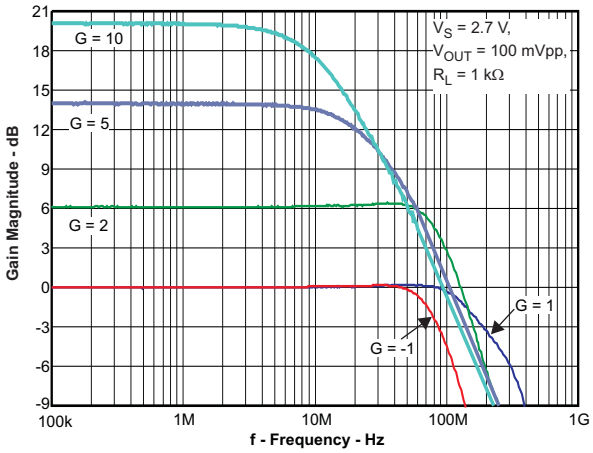



Figure 1. Small Signal Frequency Response

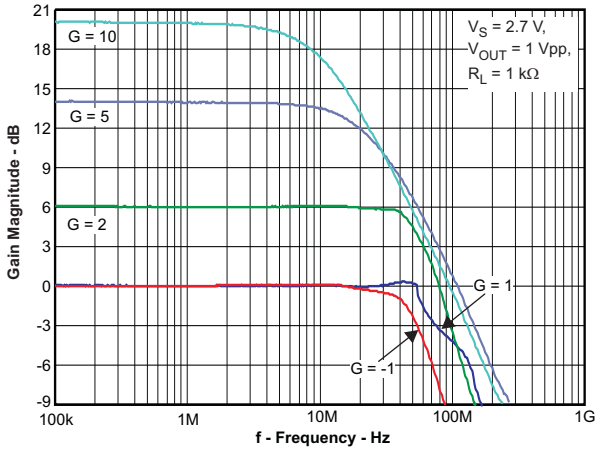



Figure 2. Large Signal Frequency Response

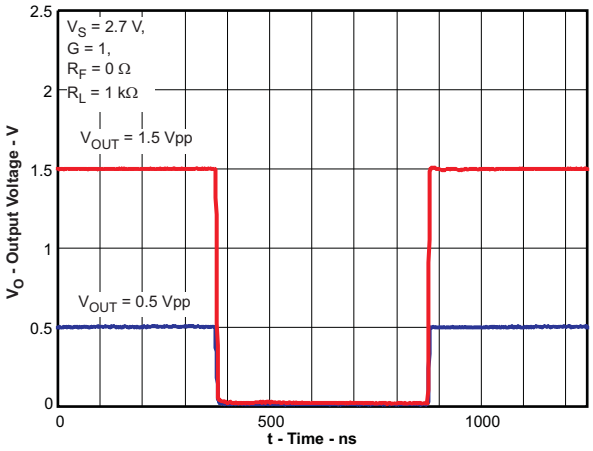



Figure 3. Noninverting Pulse Response

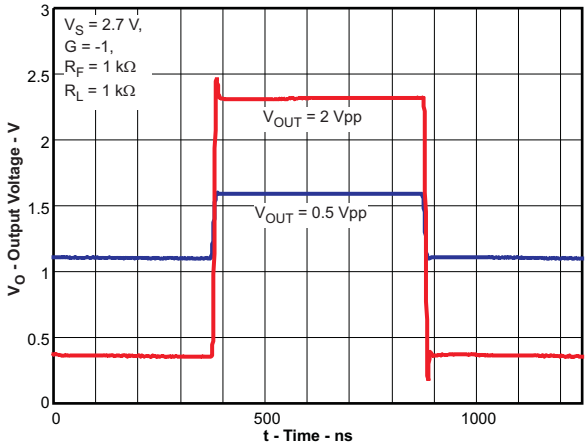



Figure 4. Inverting Pulse Response

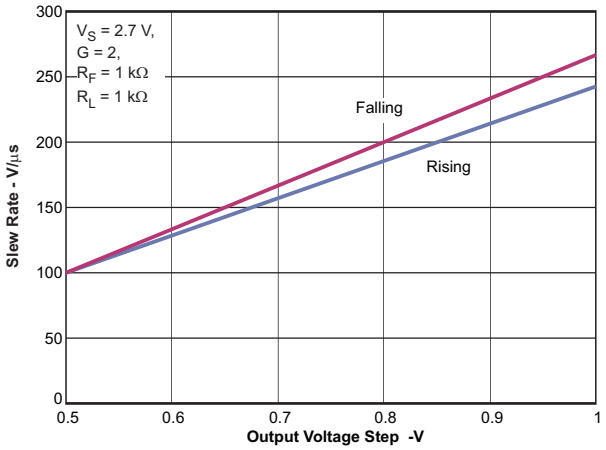



Figure 5. Slew Rate vs Output Voltage Step

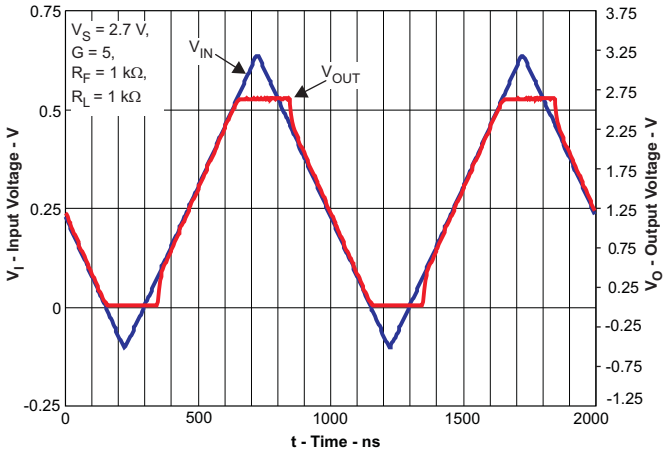



Figure 6. Output Overdrive Recovery


Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 2.7 V (continued)

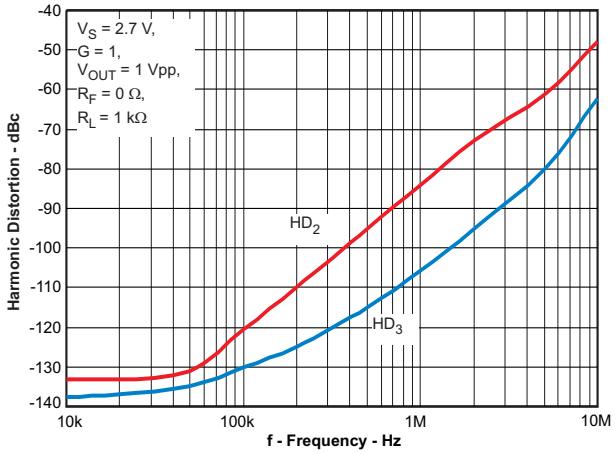



**Figure 7. Harmonic Distortion vs Frequency**

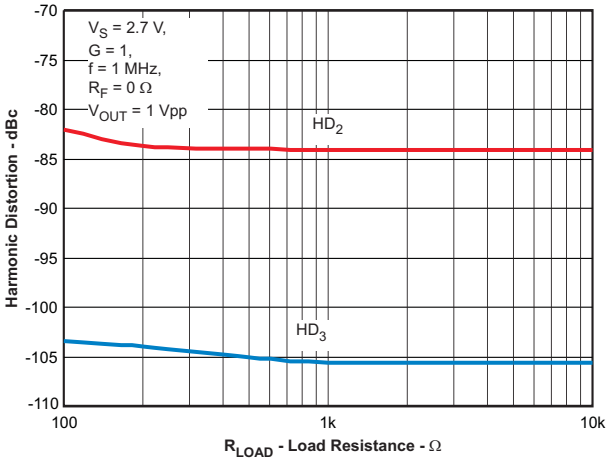



**Figure 8. Harmonic Distortion vs Load Resistance**

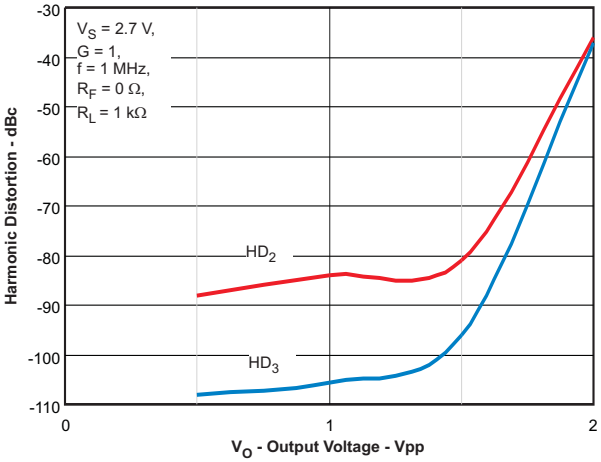



**Figure 9. Harmonic Distortion vs Output Voltage**

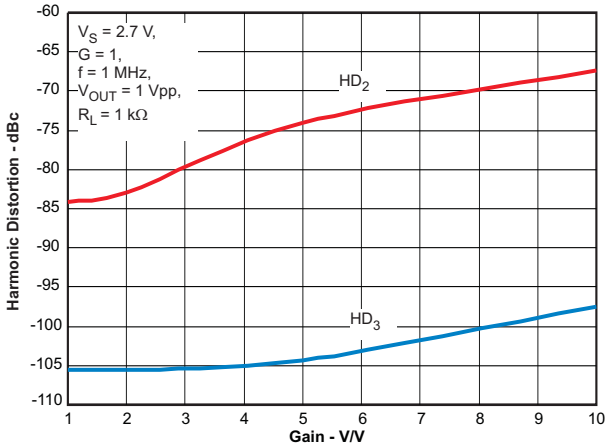



**Figure 10. Harmonic Distortion vs Gain**

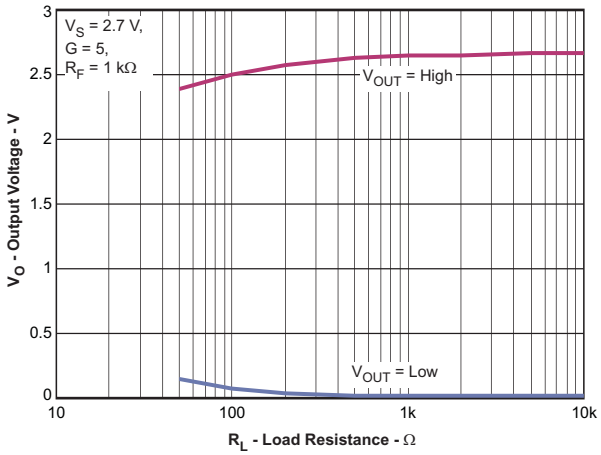



**Figure 11. Output Voltage Swing vs Load Resistance**

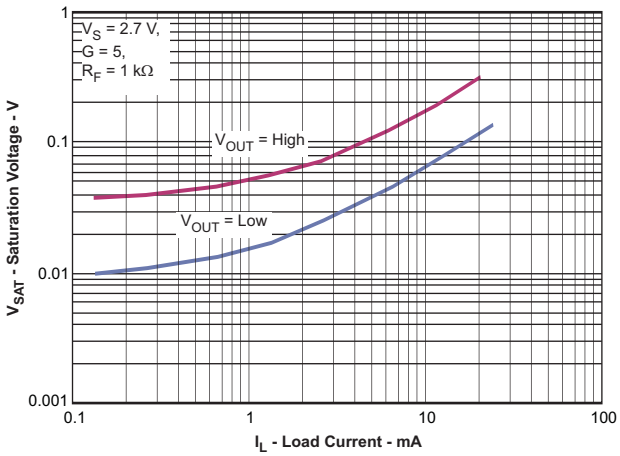



**Figure 12. Output Saturation Voltage vs Load Current**

Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 2.7 V (continued)

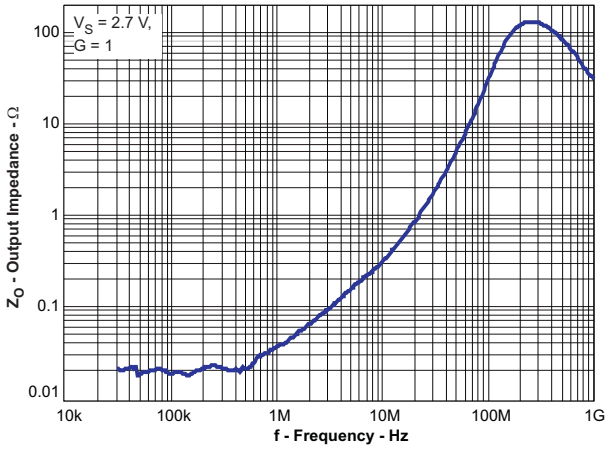



**Figure 13. Output Impedance vs Frequency**

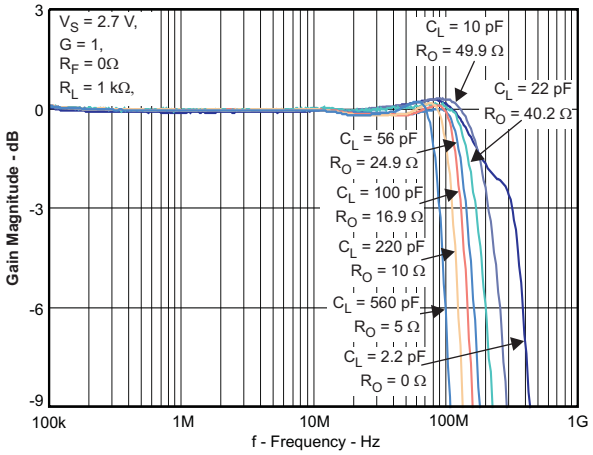



**Figure 14. Frequency Response with Capacitive Load**

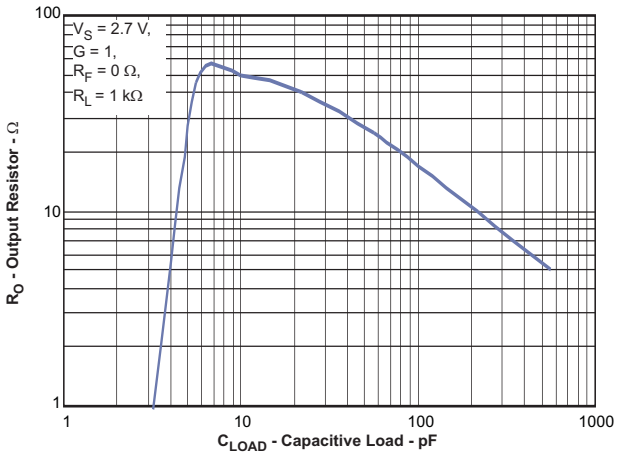



**Figure 15. Series Output Resistor vs Capacitive Load**

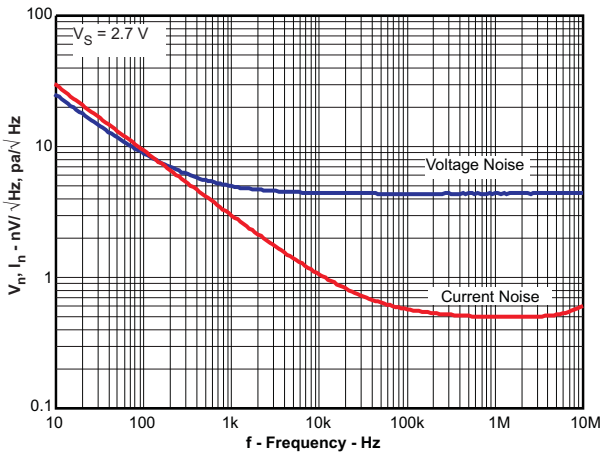



**Figure 16. Input Raftered Noise vs Frequency**

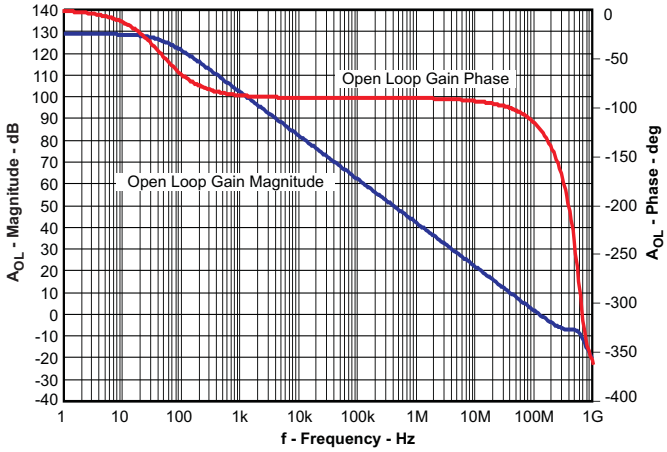



**Figure 17. Open Loop Gain vs Frequency**

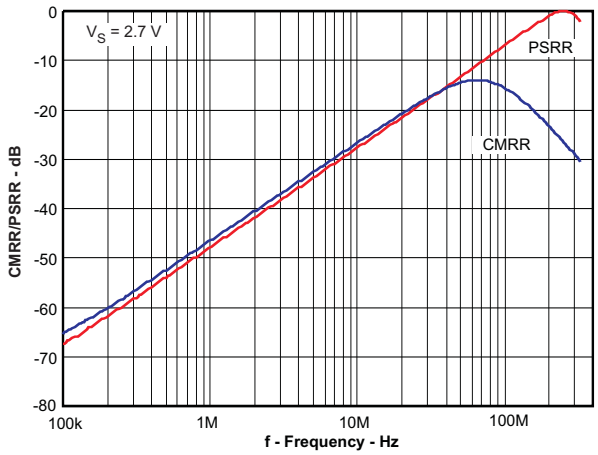



**Figure 18. Common Mode/Power Supply Rejection Ratios vs Frequency**


Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 2.7 V (continued)

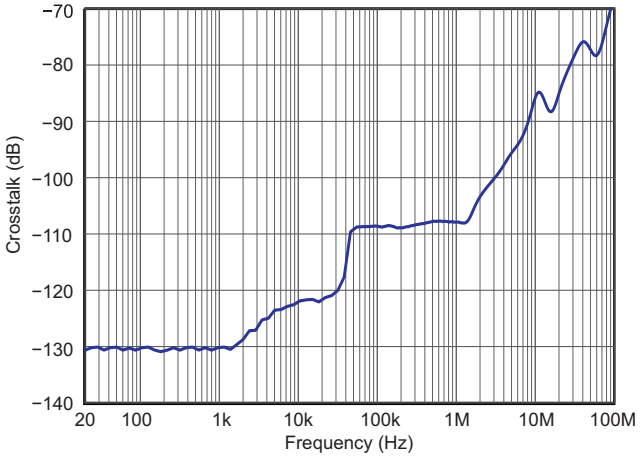



Figure 19. Crosstalk vs Frequency

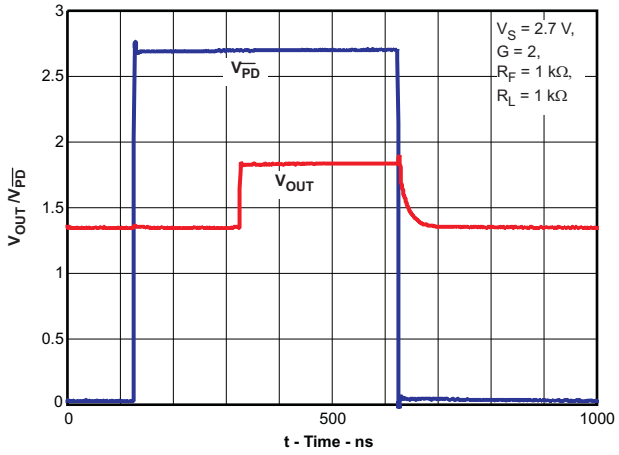



Figure 20. Power Down Response

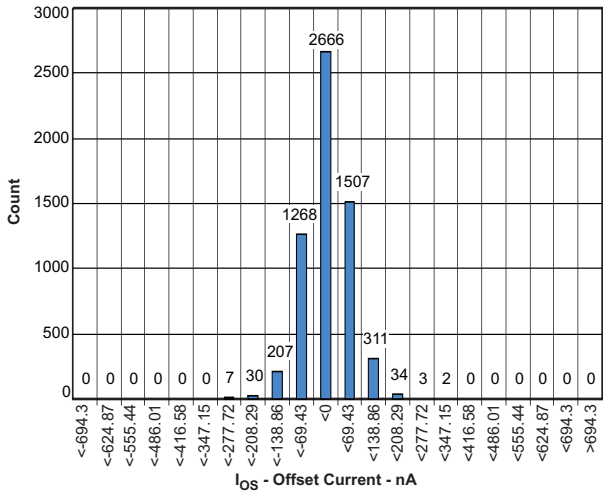



Figure 21. Input Offset Voltage

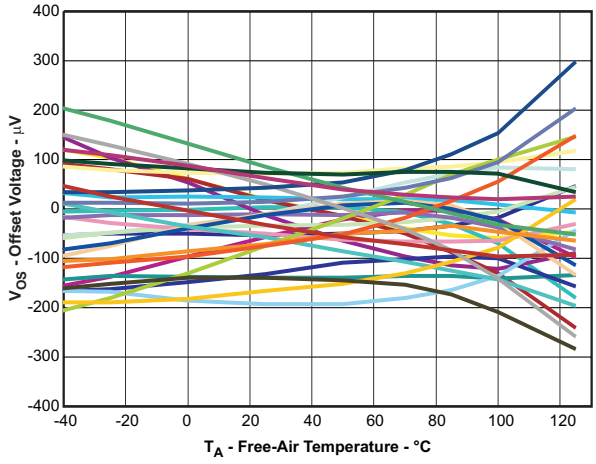



Figure 22. Input Offset Voltage vs Free-Air Temperature

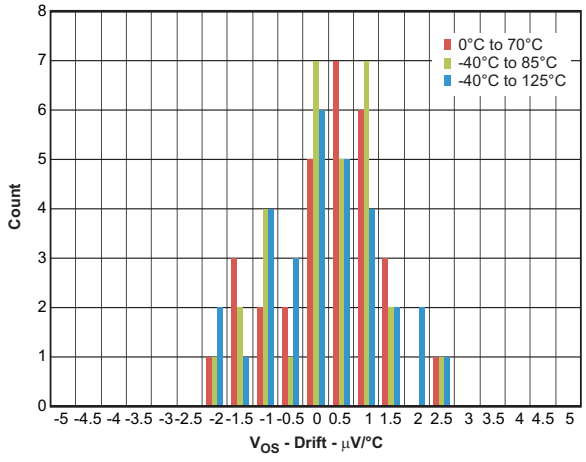



Figure 23. Input Offset Voltage Drift

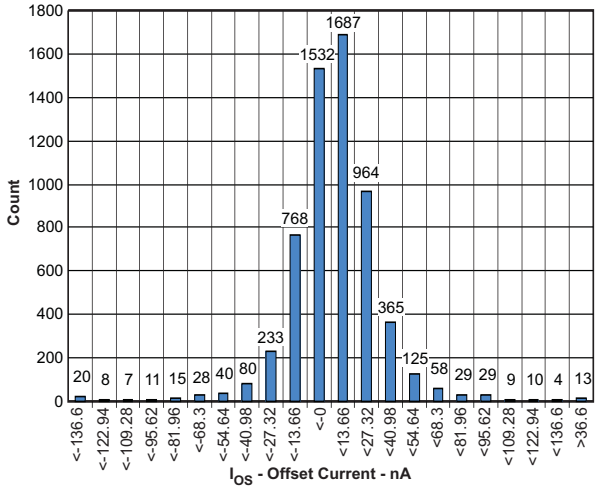



Figure 24. Input Offset Current

Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 2.7 V (continued)

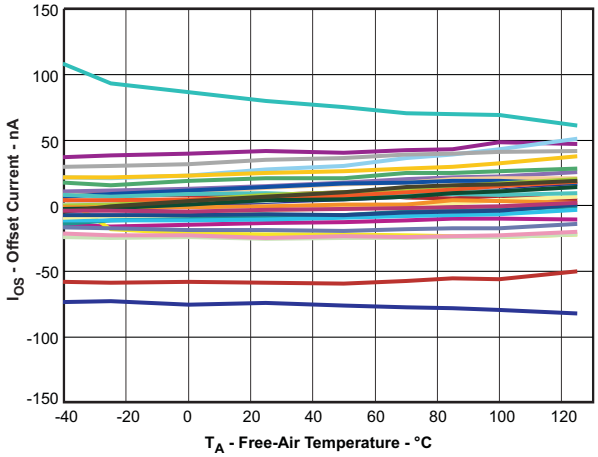



**Figure 25. Input Offset Current vs Free-Air Temperature**

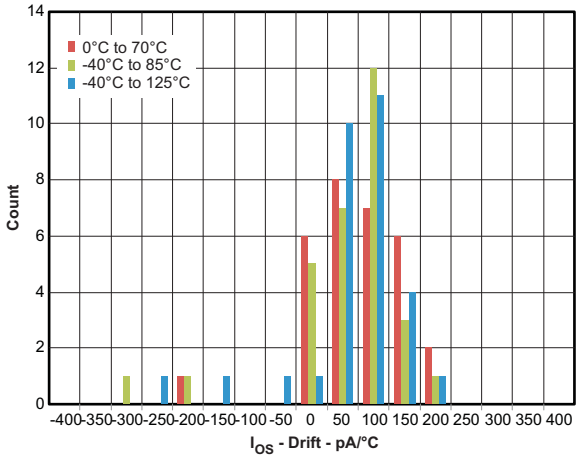



**Figure 26. Input Offset Current Drift**


Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 5 V

Test conditions unless otherwise noted: $V_{S+}$ = +5 V, $V_{S-}$ = 0 V, $V_{OUT}$ = 2 $V_{PP}$, $R_F$ = 0 Ω, $R_L$ = 1 kΩ, G = 1 V/V, Input and Output Referenced to mid-supply unless otherwise noted. $T_A$ = 25°C.

### Table of Graphs

| | | FIGURES |
|---|---|---|
| Small Signal Frequency Response | | Figure 27 |
| Large Signal Frequency Response | | Figure 28 |
| Noninverting Pulse Response | | Figure 29 |
| Inverting Pulse Response | | Figure 30 |
| Slew rate | vs Output Voltage Step | Figure 31 |
| Output Overdrive Recovery | | Figure 32 |
| Harmonic Distortion | vs Frequency | Figure 33 |
| Harmonic Distortion | vs Load Resistance | Figure 34 |
| Harmonic Distortion | vs Output Voltage | Figure 35 |
| Harmonic Distortion | vs Gain | Figure 36 |
| Output Voltage Swing | vs Load Resistance | Figure 37 |
| Output Saturation Voltage | vs Load Current | Figure 38 |
| Output Impedance | vs Frequency | Figure 39 |
| Frequency Response with Capacitive Load | | Figure 40 |
| Series Output Resistor | vs Capacitive Load | Figure 41 |
| Input Referred Noise | vs Frequency | Figure 42 |
| Open Loop Gain | vs Frequency | Figure 43 |
| Common Mode/Power Supply Rejection Ratios | vs Frequency | Figure 44 |
| Crosstalk | vs Frequency | Figure 45 |
| Power Down Response | | Figure 46 |
| Input Offset Voltage | | Figure 47 |
| Input Offset Voltage | vs Free-Air Temperature | Figure 48 |
| Input Offset Voltage Drift | | Figure 49 |
| Input Offset Current | | Figure 50 |
| Input Offset Current | vs Free-Air Temperature | Figure 51 |
| Input Offset Current Drift | | Figure 52 |

Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 5 V

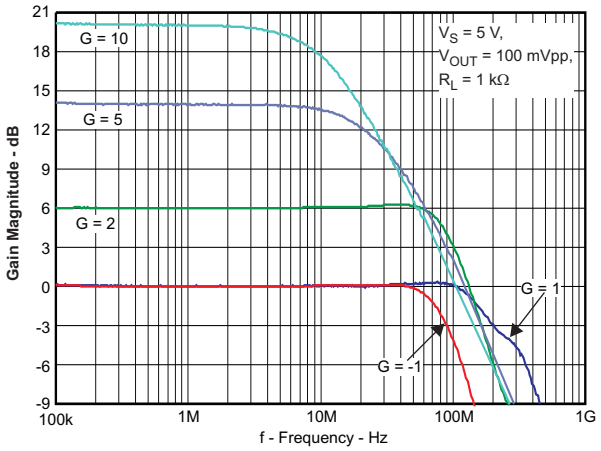



Figure 27. Small Signal Frequency Response

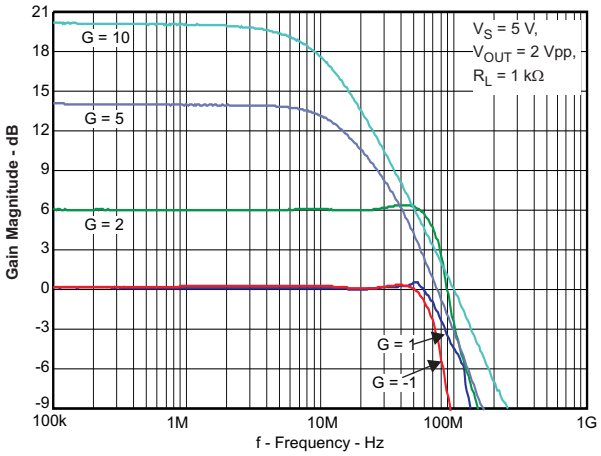



Figure 28. Large Signal Frequency Response

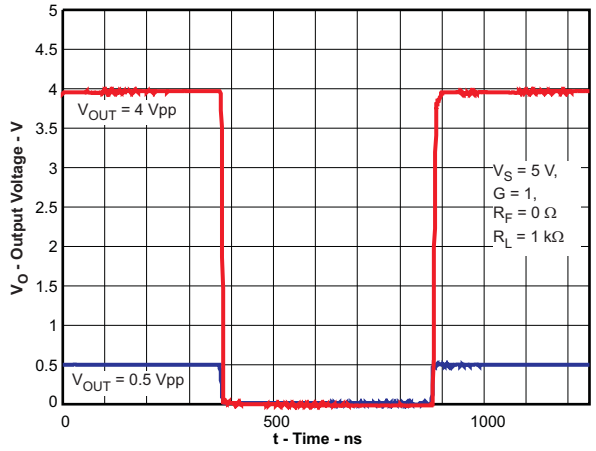



Figure 29. Noninverting Pulse Response

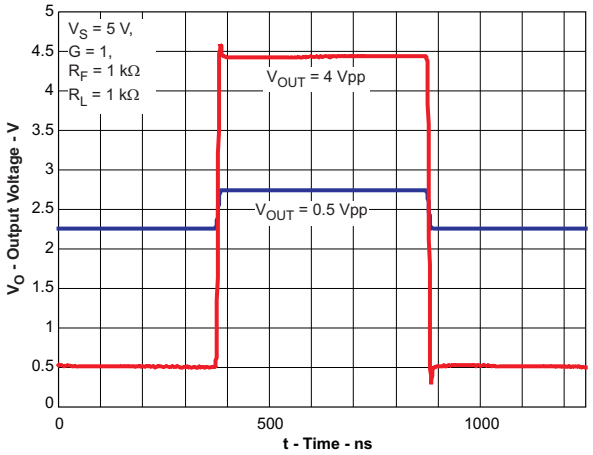



Figure 30. Inverting Pulse Response

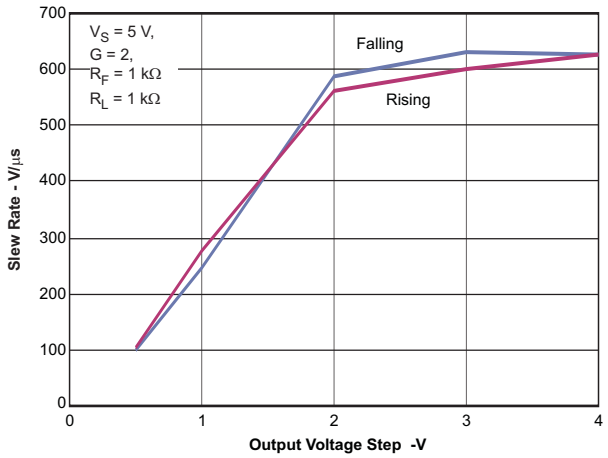



Figure 31. Slew Rate vs Output Voltage Step

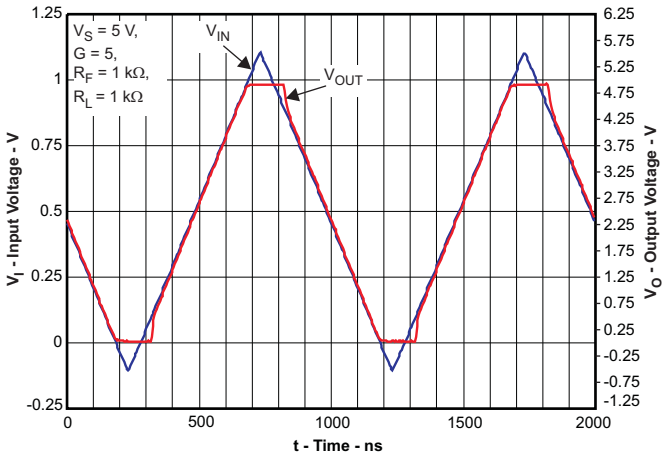



Figure 32. Output Overdrive Recovery


Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 5 V (continued)

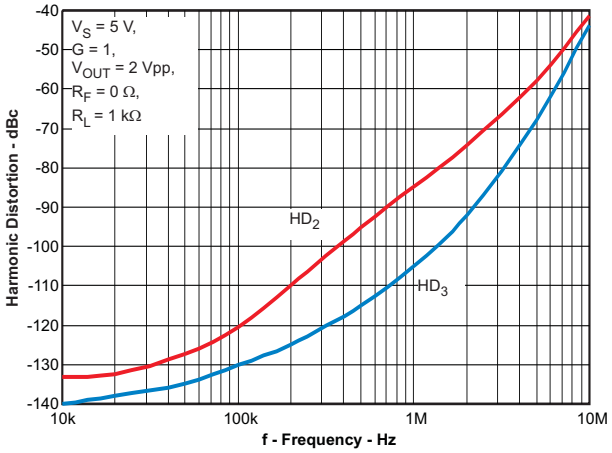



**Figure 33. Harmonic Distortion vs Frequency**

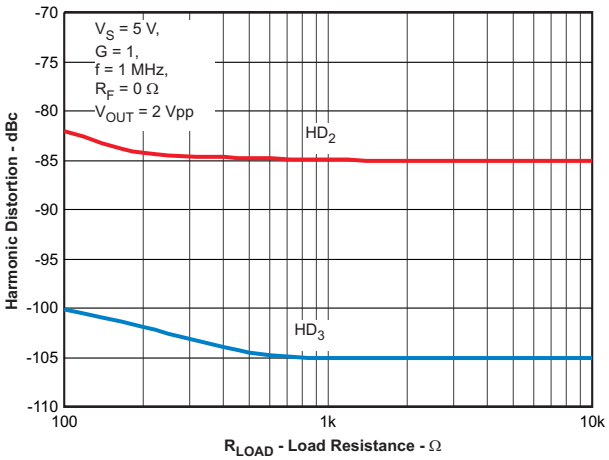



**Figure 34. Harmonic Distortion vs Load Resistance**

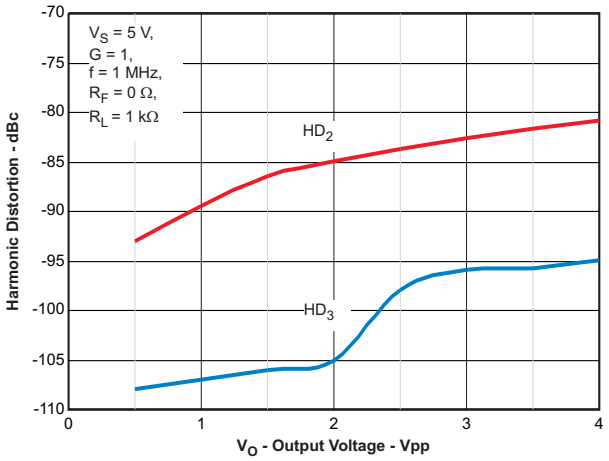



**Figure 35. Harmonic Distortion vs Output Voltage**

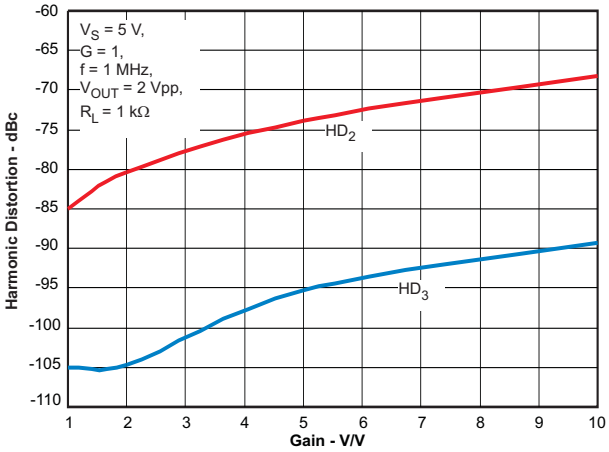



**Figure 36. Harmonic Distortion vs Gain**

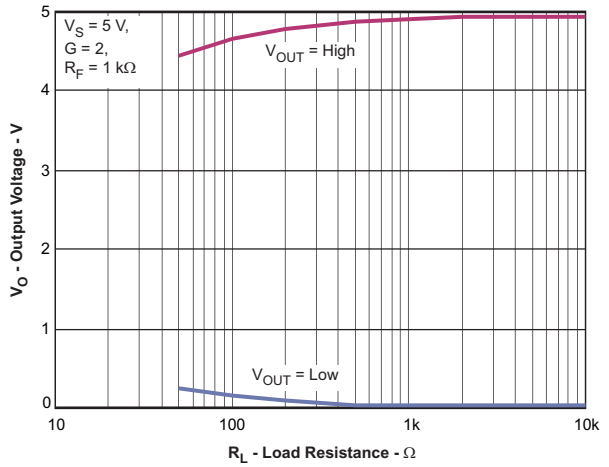



**Figure 37. Output Voltage Swing vs Load Resistance**

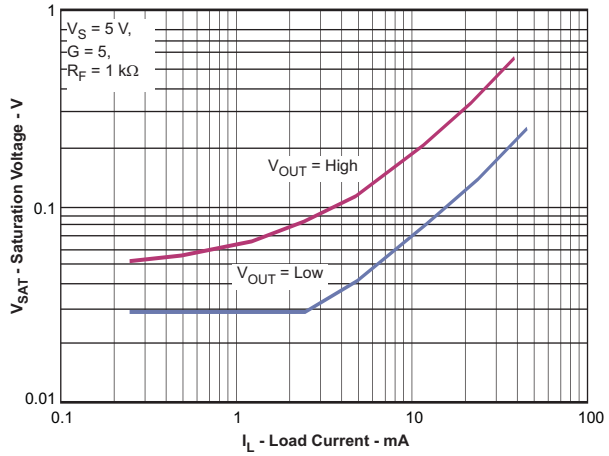



**Figure 38. Output Saturation Voltage vs Load Current**

Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 5 V (continued)

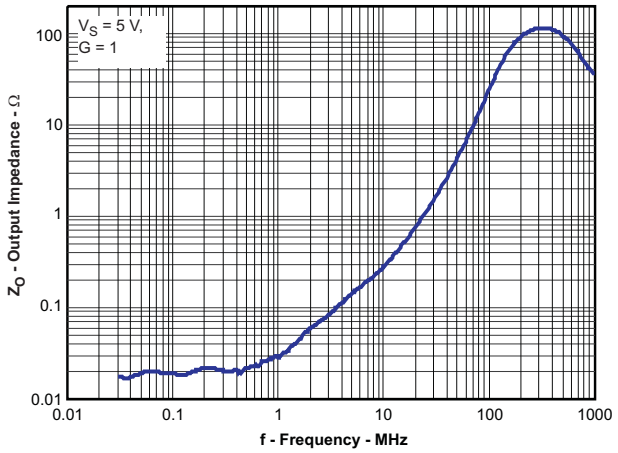



Figure 39. Output Impedance vs Frequency

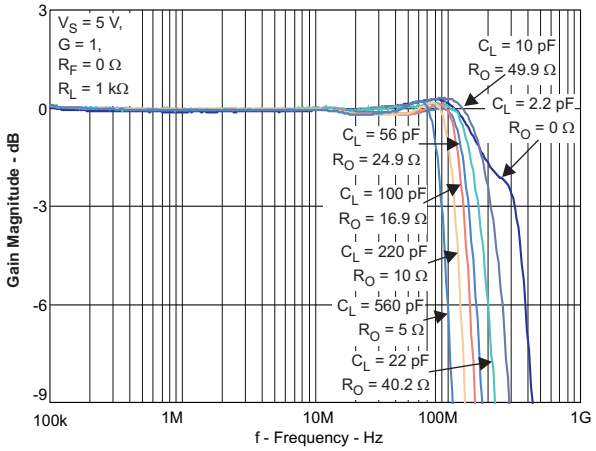



Figure 40. Frequency Response with Capacitive Load

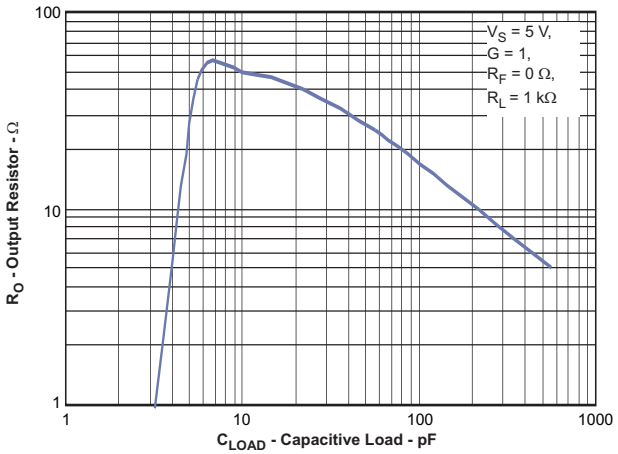



Figure 41. Series Output Resistor vs Capacitive Load

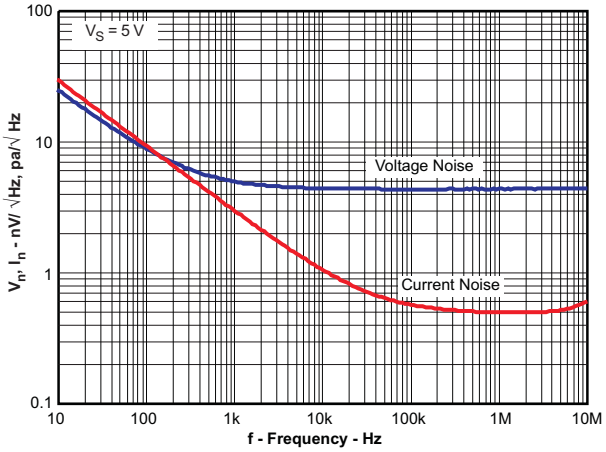



Figure 42. Input Raftered Noise vs Frequency

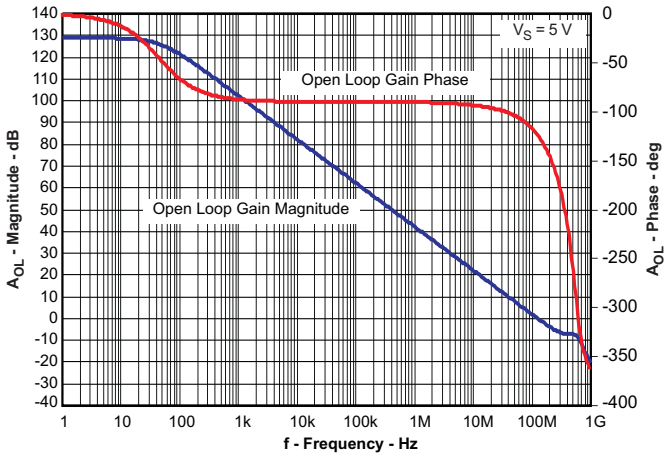



Figure 43. Open Loop Gain vs Frequency

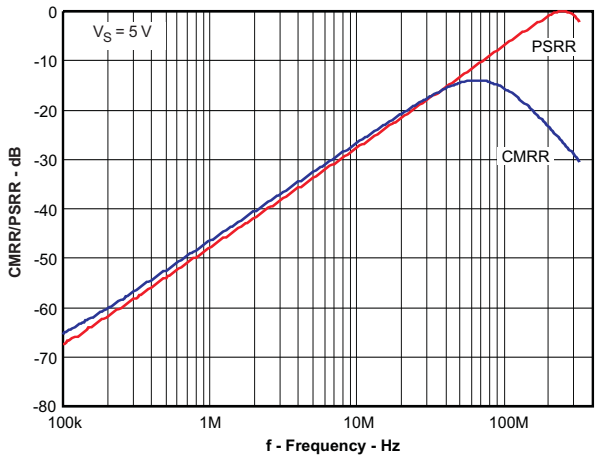



Figure 44. Common Mode/Power Supply Rejection Ratios vs Frequency


Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 5 V (continued)

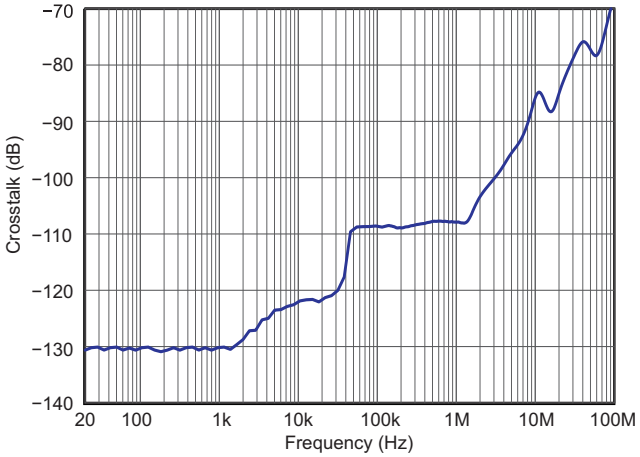



**Figure 45. Crosstalk vs Frequency**

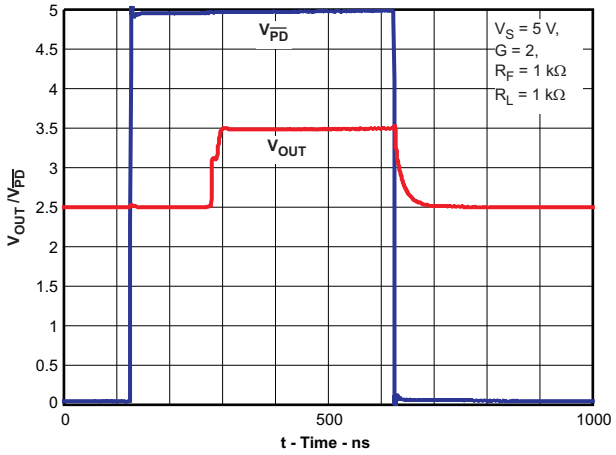



**Figure 46. Power Down Response**

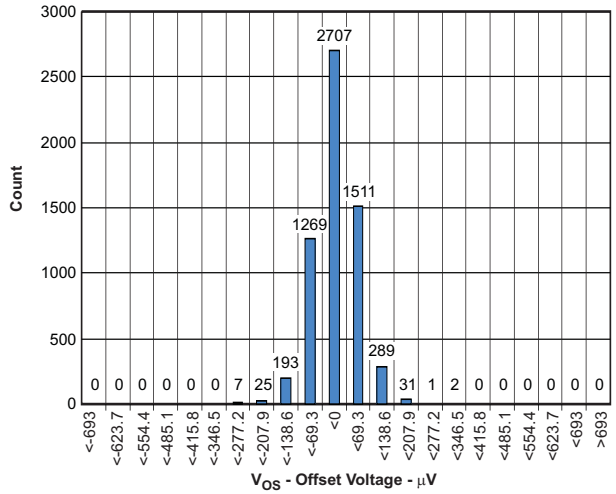



**Figure 47. Input Offset Voltage**

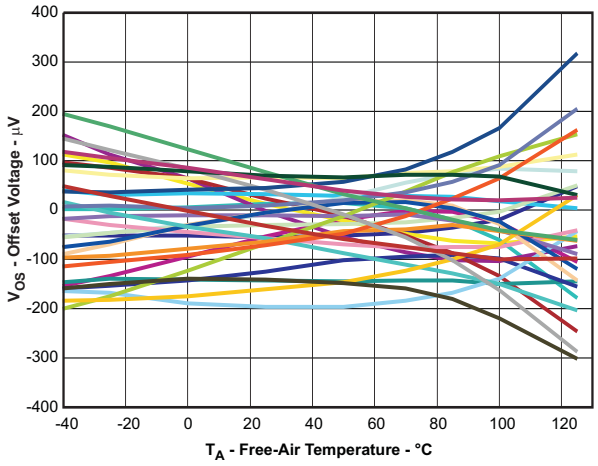



**Figure 48. Input Offset Voltage vs Free-Air Temperature**

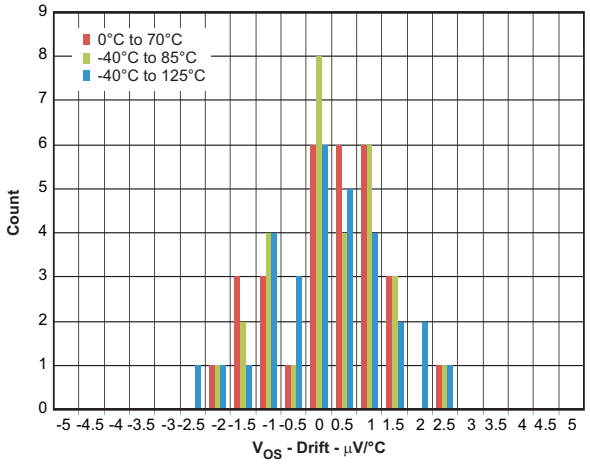



**Figure 49. Input Offset Voltage Drift**

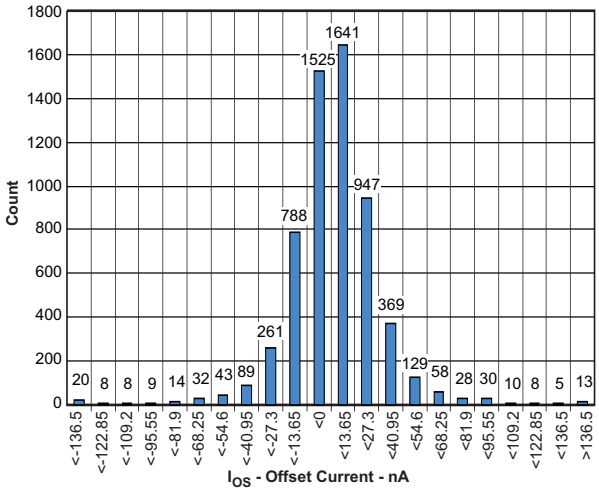



**Figure 50. Input Offset Current**

Copyright © 2011–2013, Texas Instruments Incorporated

## TYPICAL PERFORMANCE GRAPHS: $V_S$ = 5 V (continued)

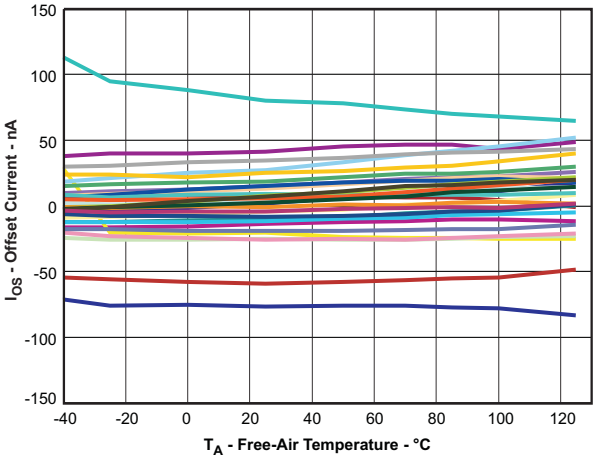



**Figure 51. Input Offset Current vs Free-Air Temperature**

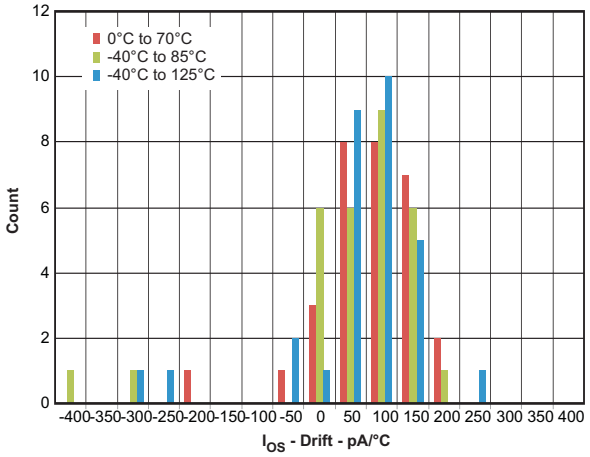



**Figure 52. Input Offset Current Drift**


Copyright © 2011–2013, Texas Instruments Incorporated

## APPLICATION INFORMATION

The following circuits show application information for the OPA836 and OPA2836. For simplicity, power supply decoupling capacitors are not shown in these diagrams.

### Non-Inverting Amplifier

The OPA836 and OPA2836 can be used as non-inverting amplifiers with signal input to the non-inverting input, $V_{IN+}$. A basic block diagram of the circuit is shown in Figure 53.

If we set $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by: $G = 1 + \frac{R_F}{R_G}$, and $V_{REF}$ provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA836 and OPA2836 are designed for the nominal value of $R_F$ to be 1kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. $R_F$ = 1kΩ should be used as a default unless other design goals require changing to other values All test circuits used to collect data for this data sheet had $R_F$ = 1kΩ for all gains other than +1. Gain of +1 is a special case where $R_F$ is shorted and $R_G$ is left open.

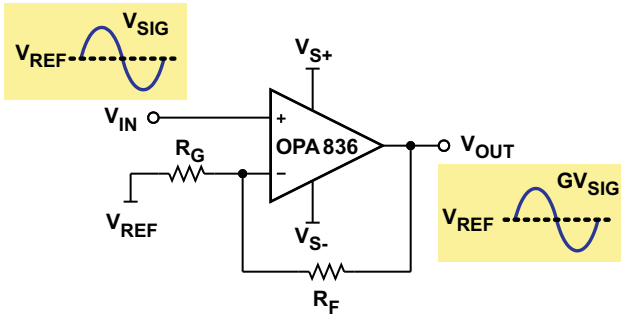



**Figure 53. Non-Inverting Amplifier**

### Inverting Amplifier

The OPA836 and OPA2836 can be used as inverting amplifiers with signal input to the inverting input, $V_{IN-}$, through the gain setting resistor $R_G$. A basic block diagram of the circuit is shown in Figure 54.

If we set $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (2)$$

The signal gain of the circuit is set by: $G = \frac{-R_F}{R_G}$ and $V_{REF}$ provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of $R_F$ should be 1kΩ for inverting gains.

Copyright © 2011–2013, Texas Instruments Incorporated

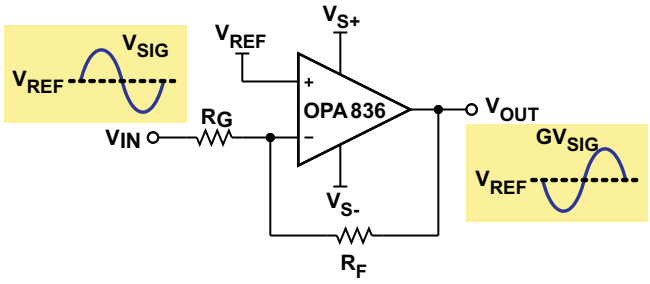



**Figure 54. Inverting Amplifier**

## Attenuators

The non-inverting circuit of Figure 53 has minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier set for gain of 1 by shorting $V_{OUT}$ to $V_{IN-}$ and removing $R_G$. Since the op amp input is high impedance, the attenuation is set by the resistor divider.

The inverting circuit of Figure 54 can be used as an attenuator by making $R_G$ larger than $R_F$. The attenuation is simply the resistor ratio. For example a 10:1 attenuator can be implemented with $R_F$ = 1 kΩ and $R_G$ = 10 kΩ.

## Single Ended to Differential Amplifier

Figure 55 shows an amplifier circuit that is used to convert single-ended signals to differential, and provides gain and level shifting. This circuit can be used for converting signals to differential in applications like line drivers for CAT 5 cabling or driving differential input SAR and ΔΣ ADCs.

By setting $V_{IN} = V_{REF} + V_{SIG}$, then

$$V_{OUT+} = G \times V_{IN} + V_{REF} \quad \text{and} \quad V_{OUT-} = -G \times V_{IN} + V_{REF} \quad \text{Where: } G = 1 + \frac{R_F}{R_G} \tag{3}$$

The differential signal gain of the circuit is 2x G, and $V_{REF}$ provides a reference around which the output signal swings. The differential output signal is in-phase with the single ended input signal.

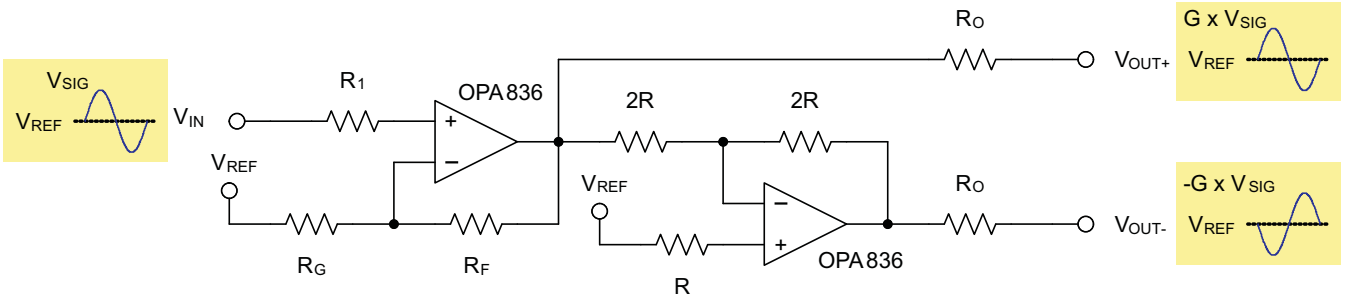



**Figure 55. Single Ended to Differential Amplifier**

Line termination on the output can be accomplished with resistors $R_O$. The impedance seen differential from the line will be 2x $R_O$. For example if 100 Ω CAT 5 cable is used with double termination, the amplifier is typically set for a differential gain of 2 V/V (6 dB) with $R_F$ = 0 Ω (short) $R_G$ = ∞Ω (open), 2R = 1 kΩ, R1 = 0 Ω, R = 499 Ω to balance the input bias currents, and $R_O$ = 49.9 Ω for output line termination. This configuration is shown in Figure 56.

For driving a differential input ADC the situation is similar, but the output resistors, $R_O$, are typically chosen along with a capacitor across the ADC input for optimum filtering and settling time performance.


Copyright © 2011–2013, Texas Instruments Incorporated

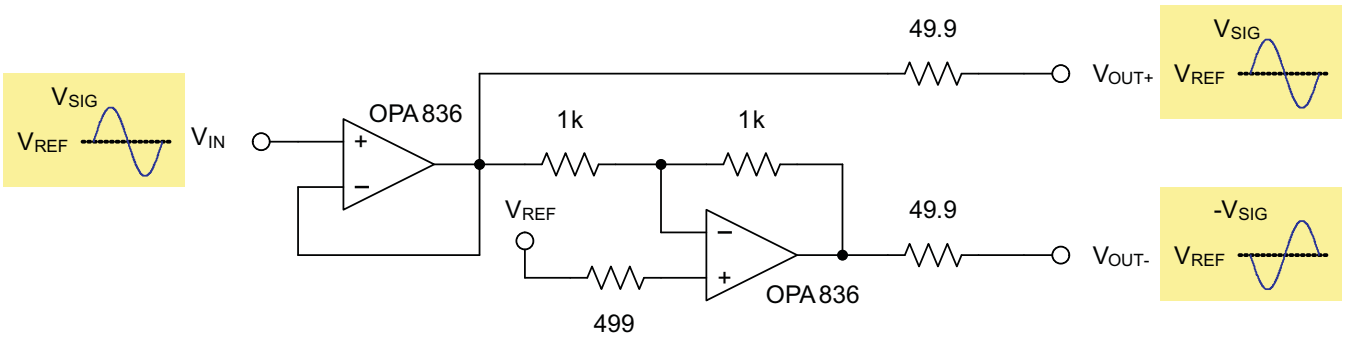



**Figure 56. CAT 5 Line Driver with Gain = 2 V/V (6 dB)**

## Differential to Signal Ended Amplifier

Figure 57 shows a differential amplifier that is used to convert differential signals to single-ended and provides gain (or attenuation) and level shifting. This circuit can be used in applications like a line receiver for converting a differential signal from a CAT 5 cable to single-ended.

If we set $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) \times \left(\frac{R_F}{R_G}\right) + V_{REF} \quad (4)$$

The signal gain of the circuit is set by: $G = \frac{R_F}{R_G}$, $V_{CM}$ is rejected, and $V_{REF}$ provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

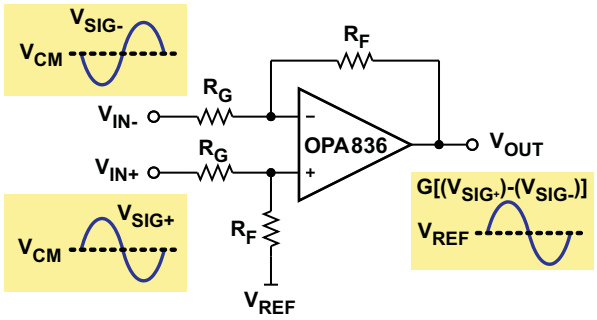



**Figure 57. Differential to Single Ended Amplifier**

Line termination can be accomplished with a resistor shunt across the input. The impedance seen differential from the line will be the resistor value in parallel with the amplifier circuit. For low gain and low line impedance the resistor value to add is approximately the impedance of the line. For example if 100 Ω CAT5 cable is used with a gain of 1 amplifier and $R_F = R_G = 1$ kΩ, adding a 100 Ω shunt across the input will give a differential impedance of 98 Ω; this should be adequate for most applications.

For best CMRR performance, resistors must be matched. A rule of thumb is CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide about 60 dB CMRR.

## Differential to Differential Amplifier

Figure 58 shows a differential amplifier that is used to amplify differential signals. This circuit has high input impedance and is often used in differential line driver applications where the signal source is a high impedance driver like a differential DAC that needs to drive a line.

If we set $V_{IN\pm} = V_{CM} + V_{SIG\pm}$ then

Copyright © 2011–2013, Texas Instruments Incorporated

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \quad (5)$$

The signal gain of the circuit is set by: $G = 1 + \frac{2R_F}{R_G}$, and $V_{CM}$ passes with unity gain. The amplifier in essence combines two non-inverting amplifiers into one differential amplifier with the $R_G$ resistor shared, which makes $R_G$ effectively ½ its value when calculating the gain. The output signals are in-phase with the input signals.

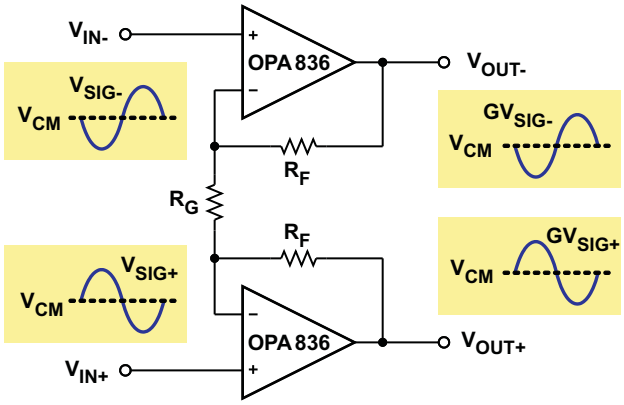



**Figure 58. Differential to Differential Amplifier**

## Instrumentation Amplifier

Figure 59 is an instrumentation amplifier that combines the high input impedance of the differential to differential amplifier circuit and the common-mode rejection of the differential to single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required like taps from a differential line or in cases where the signal source is a high impedance.

If we set $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \quad (6)$$

The signal gain of the circuit is set by:

$G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right)$, $V_{CM}$ is rejected, and $V_{REF}$ provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

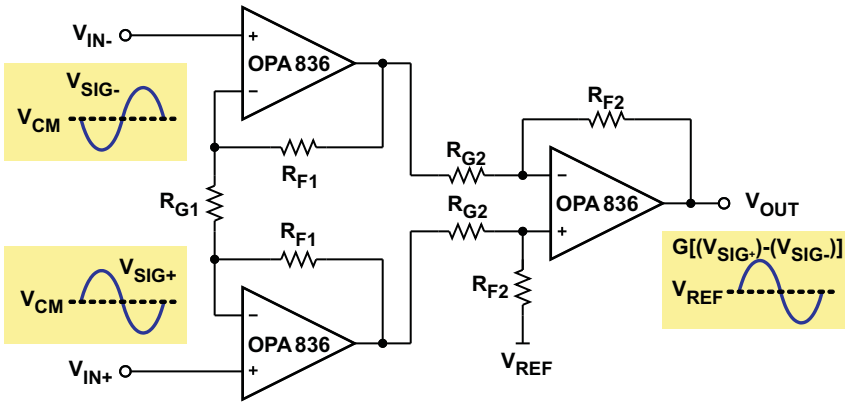



**Figure 59. Instrumentation Amplifier**


Copyright © 2011–2013, Texas Instruments Incorporated

Integrated solutions are available, but the OPA836 provides a much lower power high frequency solution. For best CMRR performance, resistors must be matched. Assuming CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide about 60 dB CMRR.

## Gain Setting with OPA836 RUN Integrated Resistors

The OPA836 RUN package option includes integrated gain setting resistors for smallest possible footprint on a printed circuit board (≈ 2mm x 2mm). By adding circuit traces on the PCB, gains of +1, -1, -1.33, +2, +2.33, -3, +4, -4, +5, -5.33, +6.33, -7, +8 and inverting attenuations of -0.1429, -0.1875, -0.25, -0.33, -0.75 can be achieved.

Figure 60 shows a simplified view of how the OPA836IRUN integrated gain setting network is implemented. Table 1 shows the required pin connections for various non-inverting and inverting gains (reference Figure 53 and Figure 54). Table 2 shows the required pin connections for various attenuations using the inverting amplifier architecture (reference Figure 54). Due to ESD protection devices being used on all pins, the absolute maximum and minimum input voltage range, $V_{S-}$ - 0.7V to $V_{S+}$ + 0.7V, applies to the gain setting resistors, and so attenuation of large input voltages will require external resistors to implement.

The gain setting resistors are laser trimmed to 1% tolerance with nominal values of 1.6 kΩ, 1.2 kΩ, and 400 Ω. They have excellent temperature coefficient and gain tracking is superior to using external gain setting resistors. The 500 Ω and 1.5 pF capacitor in parallel with the 1.6 kΩ gain setting resistor provide compensation for best stability and pulse response.

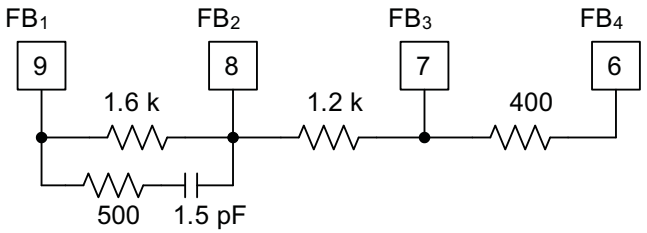



**Figure 60. OPA836IRUN Gain Setting Network**

**Table 1. Gains Setting**

| Non-inverting Gain (Figure 53) | Inverting Gain (Figure 54) | Short Pins | Short Pins | Short Pins | Short Pins |
|---|---|---|---|---|---|
| 1 V/V (0 dB) | - | 1 to 9 | | | - |
| 2 V/V (6.02 dB) | -1 V/V (0 dB) | 1 to 9 | 2 to 8 | 6 to GND | - |
| 2.33 V/V (7.36 dB) | -1.33 V/V (2.5 dB) | 1 to 9 | 2 to 8 | 7 to GND | - |
| 4 V/V (12.04 dB) | -3 V/V (9.54 dB) | 1 to 8 | 2 to 7 | 6 to GND | - |
| 5 V/V (13.98 dB) | -4 V/V (12.04 dB) | 1 to 9 | 2 to 7 or 8 | 7 to 8 | 6 to GND |
| 6.33 V/V (16.03 dB) | -5.33 V/V (14.54 dB) | 1 to 9 | 2 to 6 or 8 | 6 to 8 | 7 to GND |
| 8 V/V (18.06 dB) | -7 V/V (16.90 dB) | 1 to 9 | 2 to 7 | 6 to GND | - |

**Table 2. Attenuator Settings**

| Inverting Gain (Figure 54) | Short Pins | Short Pins | Short Pins | Short Pins |
|---|---|---|---|---|
| -0.75 V/V (-2.5 dB) | 1 to 7 | 2 to 8 | 9 to GND | - |
| -0.333 V/V (-9.54 dB) | 1 to 6 | 2 to 7 | 8 to GND | - |
| -0.25 V/V (-12.04 dB) | 1 to 6 | 2 to 7 or 8 | 7 to 8 | 9 to GND |
| -0.1875 V/V (-14.54 dB) | 1 to 7 | 2 to 6 or 8 | 6 to 8 | 9 to GND |
| -0.1429 V/V (-16.90 dB) | 1 to 6 | 2 to 7 | 9 to GND | - |

Copyright © 2011–2013, Texas Instruments Incorporated

## Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier, with high CMRR, it is important to not violate the input common-mode voltage range ($V_{ICR}$) of an op amp.

Common-mode input range low and high specifications in the table data use CMRR to set the limit. The limits are chosen to ensure CMRR will not degrade more than 3dB below its limit if the input voltage is kept within the specified range. The limits cover all process variations and most parts will be better than specified. The typical specifications are from 0.2 V below the negative rail to 1.1 V below the positive rail.

Assuming the op amp is in linear operation the voltage difference between the input pins is very small (ideally 0 V) and input common-mode voltage can be analyzed at either input pin and the other input pin is assumed to be at the same potential. The voltage at $V_{IN+}$ is easy to evaluate. In non-inverting configuration, Figure 53, the input signal, $V_{IN}$, must not violate the $V_{ICR}$. In inverting configuration, Figure 53, the reference voltage, $V_{REF}$, needs to be within the $V_{ICR}$.

The input voltage limits have fixed headroom to the power rails and track the power supply voltages. For with single 5 V supply, the linear input voltage range is –0.2 V to 3.9 V and with 2.7 V supply it is –0.2 V to 1.6V . The delta from each power supply rail is the same in either case; –0.2 V and 1.1 V.

## Output Voltage Range

The OPA836 and OPA2836 are rail-to-rail output (RRO) op amps. Rail-to-rail output typically means the output voltage can swing to within a couple hundred milli-volts of the supply rails. There are different ways to specify this; one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Both saturation and linear operation limits are affected by the current in the output, where higher currents lead to more loss in the output transistors.

Data in the ELECTRICAL SPECIFICATIONS tables list both linear and saturated output voltage specifications with 1kΩ load. and show saturated voltage swing limits versus output load resistance and and show the output saturation voltage versus load current. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power supply voltages. For example with 2 kΩ load and single 5 V supply the linear output voltage range is 0.15 V to 4.8 V and with 2.7 V supply it is 0.15 V to 2.5V. The delta from each power supply rail is the same in either case; 0.15 V and 0.2 V.

With devices like the OPA836 and OPA2836, where the input range is lower than the output range, it is typical that the input will limit the available signal swing only in non-inverting gain of 1. Signal swing in non-inverting configurations in gains > +1 and inverting configurations in any gain is generally limited by the output voltage limits of the op amp.

## Split-Supply Operation (±1.25V to ±2.75V)

To facilitate testing with common lab equipment, the OPA836 EVM SLOU314 is built to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference their inputs and outputs to ground.

Figure 61 shows a simple non-inverting configuration analogous to Figure 53 with ±2.5 V supply and $V_{REF}$ equal to ground. The input and output will swing symmetrically around ground. Due to its ease of use, split supply operation is preferred in systems where signals swing around ground, but it requires generation of two supply rails.


Copyright © 2011–2013, Texas Instruments Incorporated

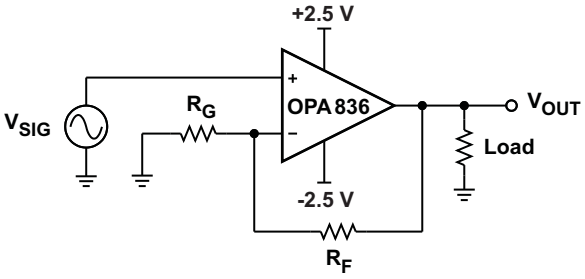



**Figure 61. Split Supply Operation**

## Single-Supply Operation (2.5 V to 5.5 V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the power supply. OPA836 and OPA2836 are designed for use with single-supply power operation and can be used with single-supply power with no change in performance from split supply as long as the input and output are biased within the linear operation of the device.

To change the circuit from split supply to single supply, level shift of all voltages by ½ the difference between the power supply rails. For example, changing from ±2.5 V split supply to 5 V single supply is shown conceptually in Figure 62.

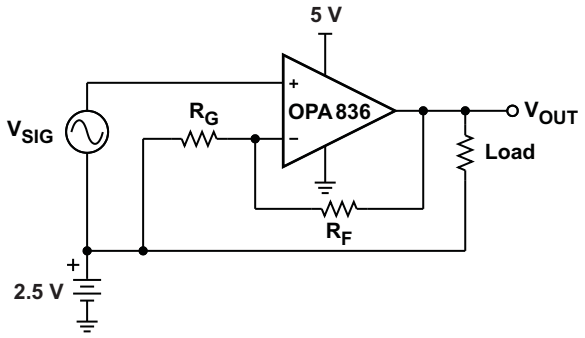



**Figure 62. Single Supply Concept**

A more practical circuit will have an amplifier or other circuit before to provide the bias voltage for the input and the output provides the bias for the next stage.

Figure 63 shows a typical non-inverting amplifier situation. With 5V single supply, a mid supply reference generator is needed to bias the negative side via $R_G$. To cancel the voltage offset that would otherwise be caused by the input bias currents, $R_1$ is chosen to be equal to $R_F$ in parallel with $R_G$. For example if gain of 2 is required and $R_F$ = 1 kΩ, select $R_G$ = 1 kΩ to set the gain and $R_1$ = 499 Ω for bias current cancellation. The value for C is dependent on the reference, but at least 0.1 µF is recommended to limit noise.

Copyright © 2011–2013, Texas Instruments Incorporated

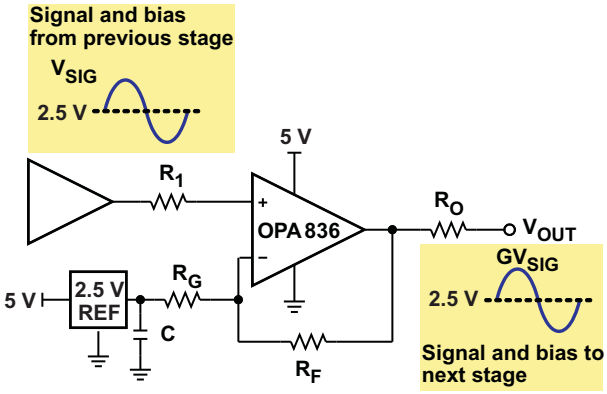



**Figure 63. Non-Inverting Single Supply with Reference**

Figure 64 shows a similar non-inverting single supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. $R_G$' and $R_G$" form a resistor divider from the 5 V supply and are used to bias the negative side with their parallel sum equal to the equivalent $R_G$ to set the gain. To cancel the voltage offset that would otherwise be caused by the input bias currents, $R_1$ in is chosen to be equal to $R_F$ in parallel with $R_G$' in parallel with $R_G$" ($R_1$= $R_F$||$R_G$'||$R_G$"). For example if gain of 2 is required and $R_F$ = 1 kΩ, selecting $R_G$' = $R_G$" = 2 kΩ gives equivalent parallel sum of 1 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). $R_1$ is then set to 499 Ω for bias current cancellation. This can be lower cost, but note the extra current draw required in the resistor divider.

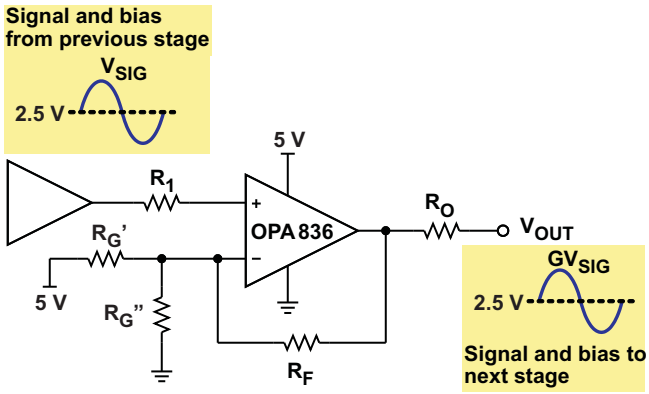



**Figure 64. Non-Inverting Single Supply with Resistors**

Figure 65 shows a typical inverting amplifier situation. With 5V single supply, a mid supply reference generator is needed to bias the positive side via $R_1$. To cancel the voltage offset that would otherwise be caused by the input bias currents, $R_1$ is chosen to be equal to $R_F$ in parallel with $R_G$. For example if gain of -2 is required and $R_F$ = 1 kΩ, select $R_G$ = 499 Ω to set the gain and $R_1$ = 332 Ω for bias current cancellation. The value for C is dependent on the reference, but at least 0.1 µF is recommended to limit noise into the op amp.


Copyright © 2011–2013, Texas Instruments Incorporated

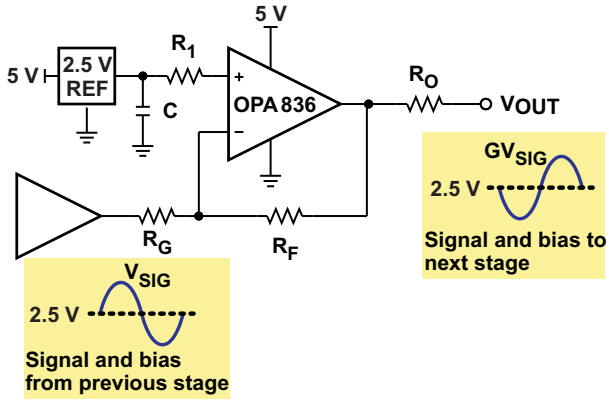



**Figure 65. Inverting Single Supply with Reference**

Figure 66 shows a similar inverting single supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. $R_1$ and $R_2$ form a resistor divider from the 5 V supply and are used to bias the positive side. To cancel the voltage offset that would otherwise be caused by the input bias currents, set the parallel sum of $R_1$ and $R_2$ equal to the parallel sum of $R_F$ and $R_G$. C should be added to limit coupling of noise into the positive input. For example if gain of –2 is required and $R_F$ = 1 kΩ, select $R_G$ = 499 Ω to set the gain. $R_1$ = $R_2$ = 665 Ω for mid supply voltage bias and for op amp input bias current cancellation. A good value for C is 0.1 µF. This can be lower cost, but note the extra current draw required in the resistor divider.

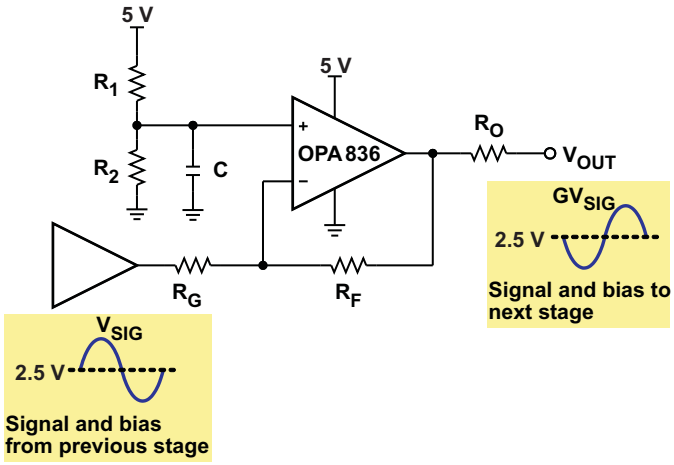



**Figure 66. Inverting Single Supply with Resistors**

## Pulse Application with Single-Supply

For pulsed applications, where the signal is at ground and pulses to some positive or negative voltage, the circuit bias voltage considerations are different than with a signal that swings symmetrical about a reference point and the circuit configuration should be adjusted accordingly. Figure 67 shows a pulsed situation where the signal is at ground (0 V) and pulses to a positive value.

Copyright © 2011–2013, Texas Instruments Incorporated

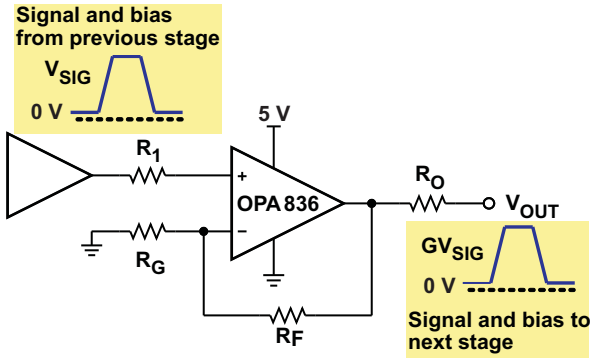



**Figure 67. Non-Inverting Single Supply with Pulse**

If the input signal pulses negative from ground, an inverting amplifier is more appropriate as shown in Figure 68. A key consideration in both non-inverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier, and since the $V_{ICR}$ of the OPA836 includes the negative supply rail, the op amp lends itself to this application.

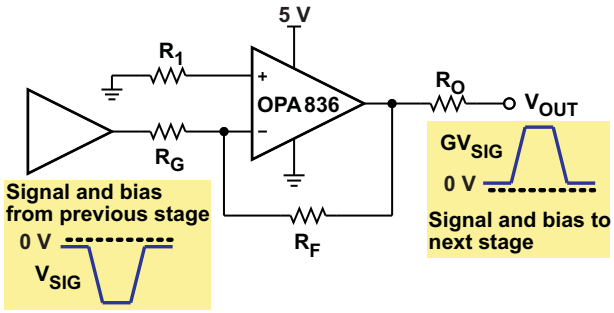



**Figure 68. Inverting Single Supply with Pulse**

## Power-Down Operation

The OPA836 and OPA2836 include a power-down mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of <1.5µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting $\overline{PD}$ pin low disables the amplifier, and places the output in a high impedance state. Note: the op amp's output in gain of +1 is high impedance similar to a 3-state high impedance gate, but in other gains the feedback network is a parallel load.

The $\overline{PD}$ pin must be actively driven high or low and should not be left floating. If the power-down mode is not used, $\overline{PD}$ should be tied to the positive supply rail.

$\overline{PD}$ logic states are TTL with reference to the negative supply rail, $V_{S-}$. When the op amp is powered from single supply and ground, driving from logic devices with similar $V_{DD}$ voltages to the op amp should not require any special consideration. When the op amp is powered from split supply, $V_{S-}$ is below ground and an open collector type of interface with pull-up resistor is more appropriate. Pull-up resistor values should be lower than 100k and the drive logic should be negated due to the inverting action of an open collector gate.


Copyright © 2011–2013, Texas Instruments Incorporated

## Low Power Applications and the Effects of Resistor Values on Bandwidth

The OPA836 and OPA2836 are designed for the nominal value of $R_F$ to be 1 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. It also loads the amplifier. For example; in gain of 2 with $R_F = R_G = 1$ kΩ, $R_G$ to ground, and $V_{OUT} = 4$ V, 2 mA of current will flow through the feedback path to ground. In gain of +1, $R_G$ is open and no current will flow to ground. In low power applications, it is desirable to reduce this current by increasing the gain setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) due to their interaction with parasitic circuit capacitance.

1. Lowers the bandwidth.
2. Lowers the phase margin
   (a) This will cause peaking in the frequency response.
   (b) And will cause over shoot and ringing in the pulse response.

Figure 69 shows the small signal frequency response on OPA836EVM for non-inverting gain of 2 with $R_F$ and $R_G$ equal to 1 kΩ, 10 kΩ, and 100kΩ. The test was done with $R_L = 1$ kΩ. Due to loading effects of $R_L$, lower values may reduce the peaking, but higher values will not have a significant effect.

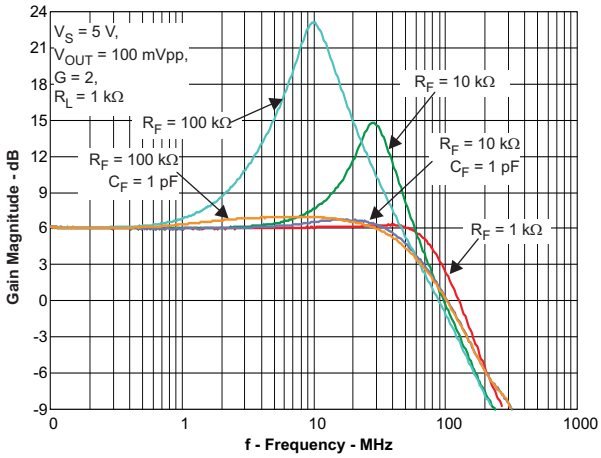



**Figure 69. Frequency Response with Various Gain Setting Resistor Values**

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response). Adding 1 pF capacitors in parallel with $R_F$ helps compensate the phase margin and restores flat frequency response. Figure 70 shows the test circuit used.

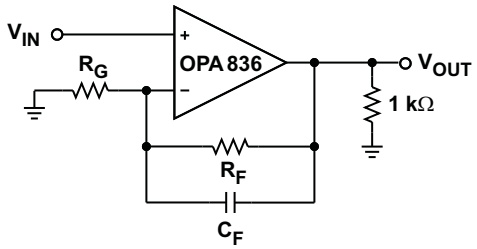



**Figure 70. G = 2 Test Circuit for Various Gain Setting Resistor Values**

Copyright © 2011–2013, Texas Instruments Incorporated

## Driving Capacitive Loads

The OPA836 and OPA2836 can drive up to a nominal capacitive load of 2.2 pF on the output with no special consideration. When driving capacitive loads greater than this, it is recommended to use a small resister ($R_O$) in series with the output as close to the device as possible. Without $R_O$, capacitance on the output will interact with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that will reduce the phase margin. This will cause peaking in the frequency response and overshoot and ringing in the pulses response. Interaction with other parasitic elements may lead to instability or oscillation. Inserting $R_O$ will isolate the phase shift from the loop gain path and restore the phase margin; however, it will also limit the bandwidth.

Figure 71 shows the test circuit and shows the recommended values of $R_O$ versus capacitive loads, $C_L$. See for frequency response with various values.

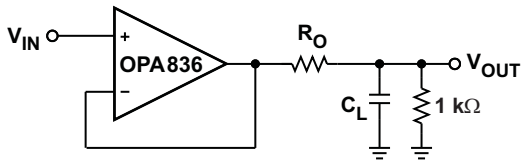



**Figure 71. $R_O$ versus $C_L$ Test Circuit**

## Active Filters

The OPA836 and OPA2836 can be used to design active filters. Figure 73 and Figure 72 show MFB and Sallen-Key circuits designed using FilterPro™ http://focus.ti.com/docs/toolsw/folders/print/filterpro.html to implement 2nd order low-pass butterworth filter circuits. Figure 74 shows the frequency response.

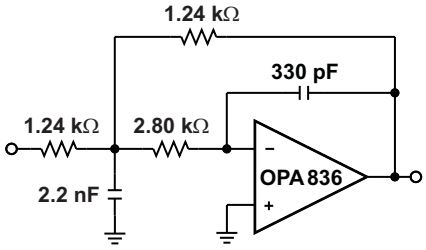



**Figure 72. MFB 100kHz 2nd Order Low-Pass Butterworth Filter Circuit**

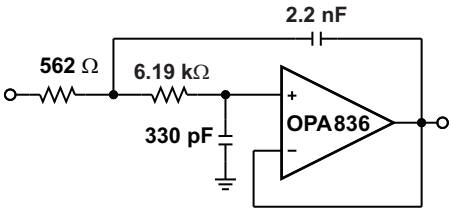



**Figure 73. Sallen-Key 100kHz 2nd Order Low-Pass Butterworth Filter Circuit**


Copyright © 2011–2013, Texas Instruments Incorporated

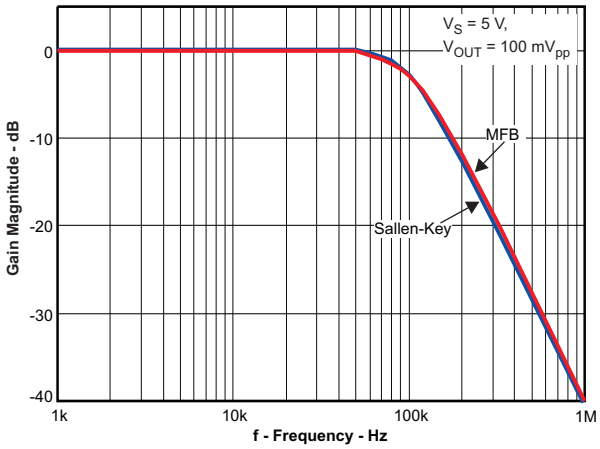



**Figure 74. MFB and Sallen-Key $2_{nd}$ Order Low-Pass Butterworth Filter Response**

MFB and Sallen-Key filter circuits offer similar performance. The main difference is the MFB is an inverting amplifier in the pass band and the Sallen-Key is non-inverting. The primary pro for each is the Sallen-Key in unity gain has no resistor gain error term, and thus no sensitivity to gain error, while the MFB has inherently better attenuation properties beyond the bandwidth of the op amp.

## Audio Frequency Performance

The OPA836 and OPA2836 provide excellent audio performance with very low quiescent power. To show performance in the audio band, a 2700 series Audio Analyzer from Audio Precision was used to test THD+N and FFT at $1V_{RMS}$ output voltage. Figure 75 is the test circuit used. Note the 100pF capacitor to ground on the input helped to decouple noise pick up in the lab and improved noise performance.

Figure 76 shows the THD+N performance with 100kΩ and 300Ω loads, with A-weighting, and with no weighting. Both loads show similar performance. With no weighting the THD+N performance is dominated by the noise whereas A-weighting provides filtering that improves the noise.

Figure 77 and Figure 78 show FFT output with a 1 kHz tone and 100kΩ and 300Ω loads. To show relative performance of the device versus the test set, one channel has the OPA836 in line between generator output and analyzer input and the other channel is in “Gen Mon” loopback mode, which internally connects the signal generator to the analyzer input. With 100 kΩ load, Figure 77, the curves are basically indistinguishable from each other except for noise, which means the OPA836 cannot be directly measured. With 300 Ω load, Figure 78, the main difference between the curves is OPA836 shows slightly higher even order harmonics, but odd order is masked by the test set performance.

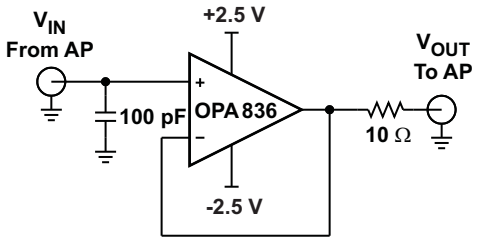



**Figure 75. OPA836 AP Analyzer Test Circuit**

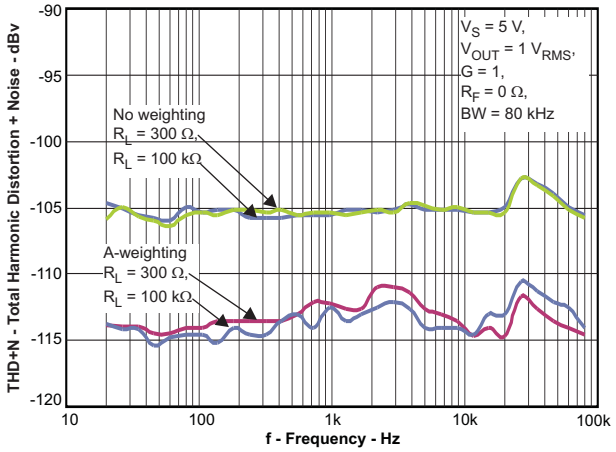



**Figure 76. OPA836 1Vrms 20 Hz to 80 kHz THD+N**

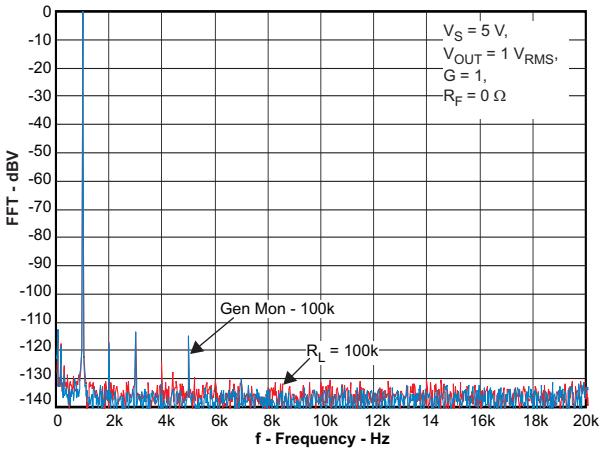



**Figure 77. OPA836 and AP Gen Mon 10kHz FFT Plot; $V_{OUT}$ = 1 $V_{RMS}$, $R_L$ = 100 kΩ**

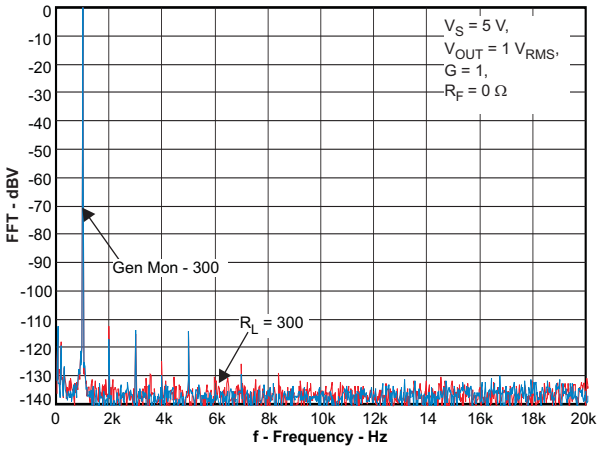



**Figure 78. OPA836 and AP Gen Mon 10 kHz FFT Plot; $V_{OUT}$ = 1 $V_{RMS}$, $R_L$ = 300Ω**

## ADC Driver Performance

The OPA836 provides excellent performance when driving high performance delta-sigma (ΔΣ) and successive approximation register (SAR) ADCs in low power audio and industrial applications.


Copyright © 2011–2013, Texas Instruments Incorporated

## OPA836 and ADS8326 Combined Performance

To show achievable performance, the OPA836 is tested as the drive amplifier for the ADS8326. The ADS8326 is a 16-bit, micro power, SAR ADC with pseudo-differential inputs and sample rates up to 250 kSPS. It offers excellent noise and distortion performance in a small 8-pin SOIC or VSSOP (MSOP) package. Low power and small size make the ADS8326 and OPA836 an ideal solution for portable and battery-operated systems, for remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

The circuit shown in Figure 79 is used to test the performance, Figure 80 is the FFT plot with 10 kHz input frequency showing the spectral performance, and the tabulated AC analysis results are in Table 3.

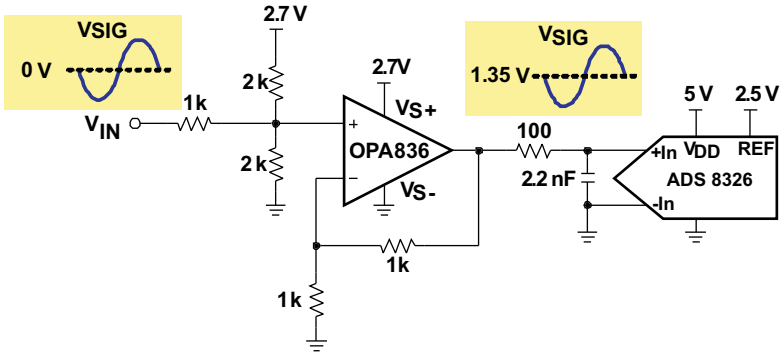



**Figure 79. OPA836 and ADS8326 Test Circuit**

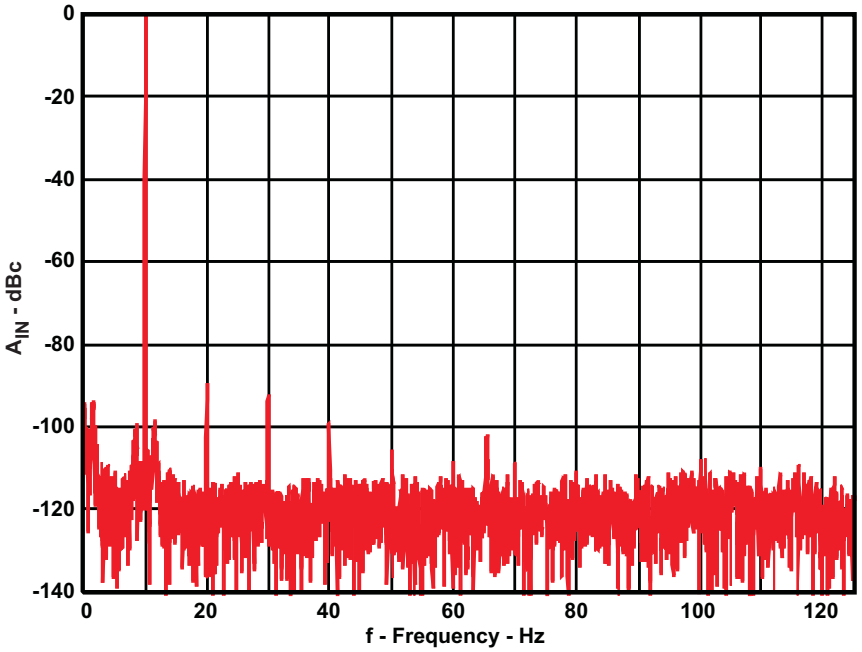



**Figure 80. ADS8326 and OPA836 10kHz FFT**

**Table 3. AC Analysis**

| Tone (Hz) | Signal (dBFS) | SNR (dBc) | THD (dBc) | SINAD (dBc) | SFDR (dBc) |
|---|---|---|---|---|---|
| 10k | –0.85 | 83.3 | –86.6 | 81.65 | 88.9 |

Copyright © 2011–2013, Texas Instruments Incorporated

## Layout Recommendations

The OPA836 EVM (SLOU314) should be used as a reference when designing the circuit board. It is recommended to follow the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into an out of the op amp.
2. The feedback path should be short and direct avoiding vias if possible especially with G = +1.
3. Ground or power planes should be removed from directly under the amplifier's negative input and output pins.
4. A series output resistor is recommended to be placed as near to the output pin as possible. See "Recommended Series Output Resistor vs. Capacitive Load" () for recommended values given expected capacitive load of design.
5. A 2.2 µF power supply decoupling capacitor should be placed within 2 inches of the device and can be shared with other op amps. For spit supply, a capacitor is required for both supplies.
6. A 0.1 µF power supply decoupling capacitor should be placed as near to the power supply pins as possible. Preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{PD}$ pin uses TTL logic levels. If not used it should tied to the positive supply to enable the amplifier. If used, it must be actively driven. A bypass capacitor is not necessary, but can be used for robustness in noisy environments.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (October 2011) to Revision E** **Page**

- Added OPA2836 RMC 封装至本文档 ..... 1
- Added RMC 封装至 描述部分 ..... 1
- Deleted Packaging/Ordering Information table, leaving only note to POA ..... 2
- Added OPA2836 RMC package to Thermal Information table ..... 2
- Added OPA2839 RMC designator to OPA2836 RUN pin out diagram ..... 9
- Added OPA2836 RMC pin definitions to Pin Functions table ..... 11

**Changes from Revision A (March 2011) to Revision B** **Page**

- Changed 将 OPA836 从产品预览改为生产数据 ..... 1


Copyright © 2011–2013, Texas Instruments Incorporated

**Changes from Revision B (May 2011) to Revision C** **Page**

- 已将“OPA836 RUN 封装...” 文本添加到描述中 ..... 1
- Removed Product Preview from all devices except OPA836IRUNT and OPA836IRUNR ..... 2
- Replaced the TBD values in the Thermal Information table ..... 2
- Changed - Channel to channel crosstalk (OPA2836) Typ value From: TBD To: -120 dB ..... 3
- Changed the Common-mode rejection ratio Min value From: 94 dB To: 91 dB ..... 4
- Added GAIN SETTING RESISTORS (OPA836IRUN ONLY) ..... 5
- Changed the Quiescent operating current ($T_A$ = 25°C) Min value From: 0.8 mA To: 0.7 mA ..... 5
- Changed the Power supply rejection (±PSRR) Min value From: 95 dB To: 91 dB ..... 5
- Changed the Powerdown pin bias current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V ..... 5
- Changed the Powerdown quiescent current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V ..... 5
- Changed - Channel to channel crosstalk (OPA2836) Typ value From: TBD To: -120 dB ..... 6
- Changed the Common-mode rejection ratio Min value From: 97 dB To: 94 dB ..... 7
- Added GAIN SETTING RESISTORS (OPA836IRUN ONLY) ..... 8
- Changed the Quiescent operating current ($T_A$ = 25°C) Min value From: 0.9 mA To: 0.8 mA ..... 8
- Changed the Power supply rejection (±PSRR) Min value From: 97 dB To: 94 dB ..... 8
- Changed the Powerdown quiescent current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V ..... 8
- Changed the Powerdown quiescent current CONDITIONS From: $\overline{PD}$ = 0.7V To: $\overline{PD}$ = 0.5V ..... 8
- Changed the OPA836 WQFN-10 (RUN) pinout image ..... 9
- Added Figure Crosstalk vs Frequency ..... 14
- Added Figure Crosstalk vs Frequency ..... 20
- Added section Single Ended to Differential Amplifier ..... 24

**Changes from Revision C (September 2011) to Revision D** **Page**

- Removed Product Preview from OPA836IRUNT and OPA836IRUNR ..... 2
- Changed Resistor Temperature Coefficient Typ value From: TBD To: <10 ..... 5
- Changed Quiescent operating current To: Quiescent operating current per amplifer ..... 5
- Changed Resistor Temperature Coefficient Typ value From: TBD To: <10 ..... 8
- Changed Quiescent operating current To: Quiescent operating current per amplifer ..... 8

Copyright © 2011–2013, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2836ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IDGS | ACTIVE | VSSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IRMCR | ACTIVE | UQFN | RMC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IRMCT | ACTIVE | UQFN | RMC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IRUNR | ACTIVE | QFN | RUN | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA2836IRUNT | ACTIVE | QFN | RUN | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2836 | Samples |
| OPA836IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | QTL | Samples |
| OPA836IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | QTL | Samples |
| OPA836IRUNR | ACTIVE | QFN | RUN | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 836 | Samples |
| OPA836IRUNT | ACTIVE | QFN | RUN | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 836 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

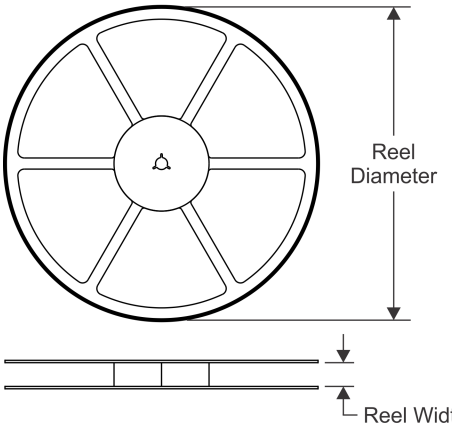
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

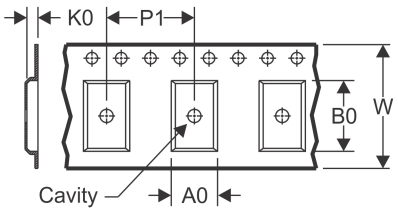
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

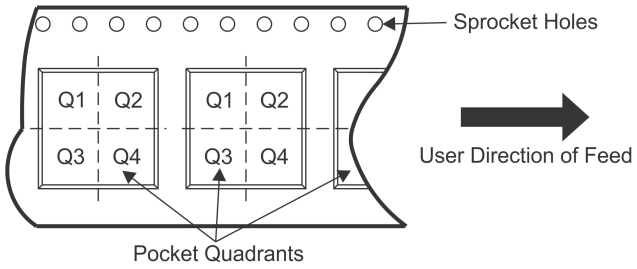



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

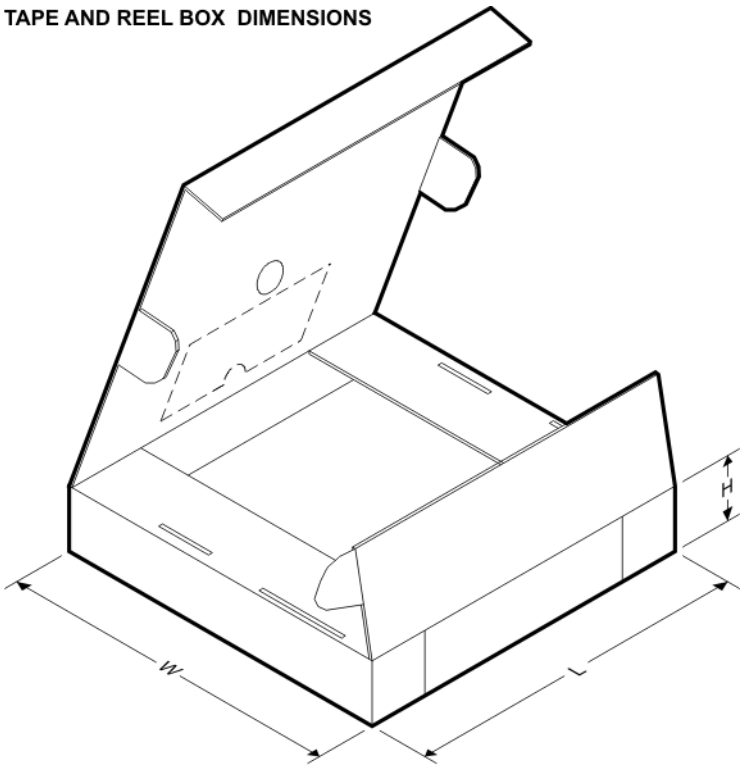
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2836IDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2836IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2836IRMCR | UQFN | RMC | 10 | 3000 | 180.0 | 9.5 | 2.3 | 2.3 | 1.1 | 2.0 | 8.0 | Q2 |
| OPA2836IRMCT | UQFN | RMC | 10 | 250 | 180.0 | 9.5 | 2.3 | 2.3 | 1.1 | 2.0 | 8.0 | Q2 |
| OPA2836IRUNR | QFN | RUN | 10 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| OPA2836IRUNT | QFN | RUN | 10 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| OPA836IDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA836IDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA836IRUNR | QFN | RUN | 10 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| OPA836IRUNT | QFN | RUN | 10 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

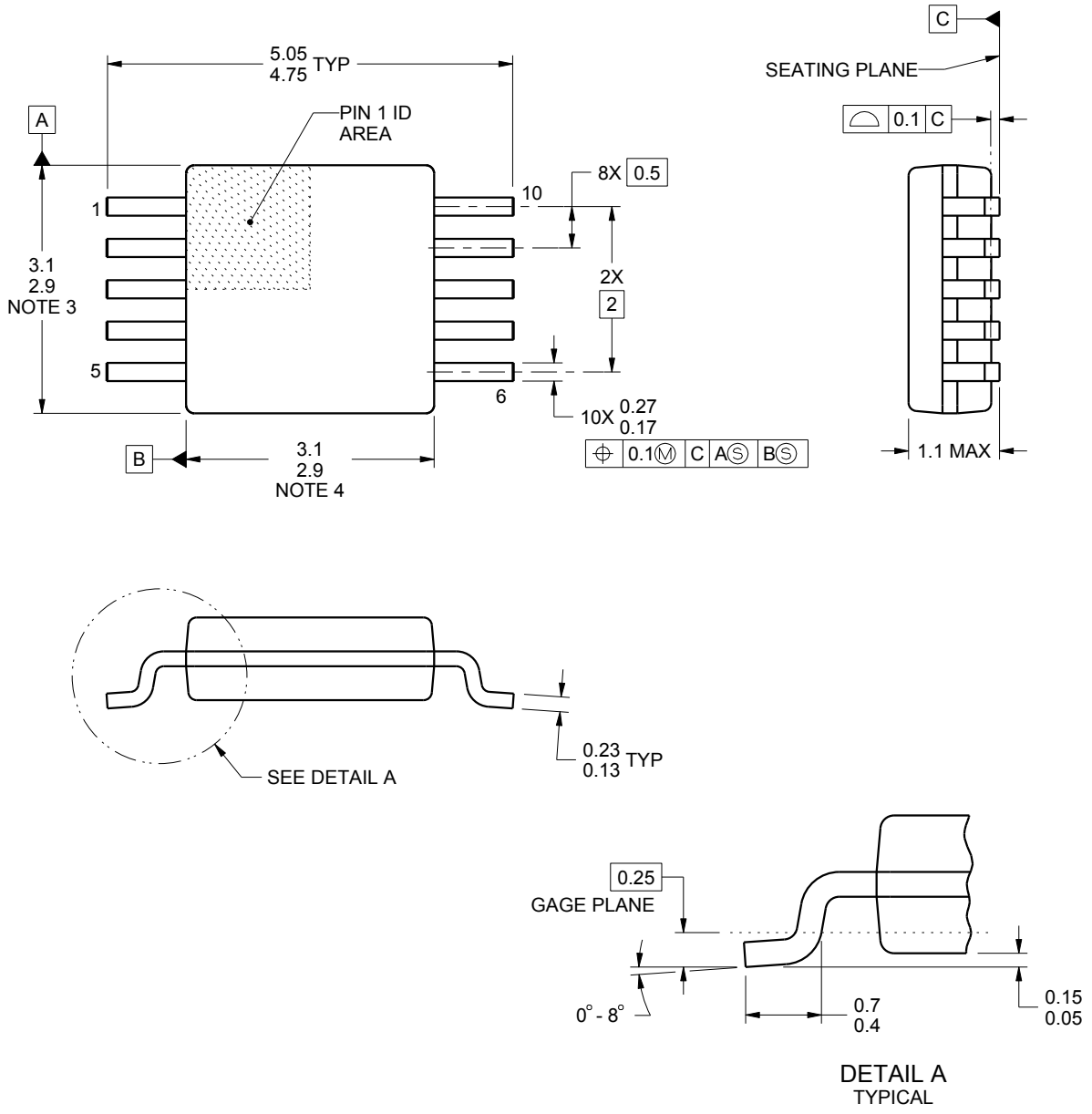
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2836IDGSR | VSSOP | DGS | 10 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2836IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| OPA2836IRMCR | UQFN | RMC | 10 | 3000 | 205.0 | 200.0 | 30.0 |
| OPA2836IRMCT | UQFN | RMC | 10 | 250 | 205.0 | 200.0 | 30.0 |
| OPA2836IRUNR | QFN | RUN | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA2836IRUNT | QFN | RUN | 10 | 250 | 210.0 | 185.0 | 35.0 |
| OPA836IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| OPA836IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| OPA836IRUNR | QFN | RUN | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA836IRUNT | QFN | RUN | 10 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DGS0010A

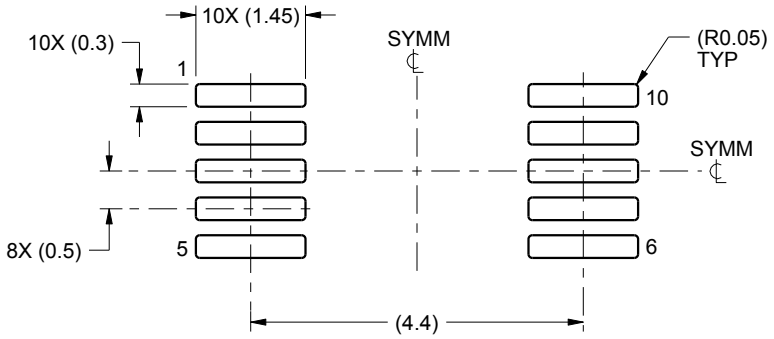
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

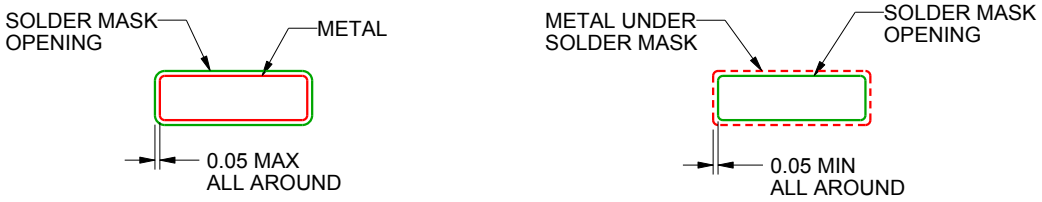



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

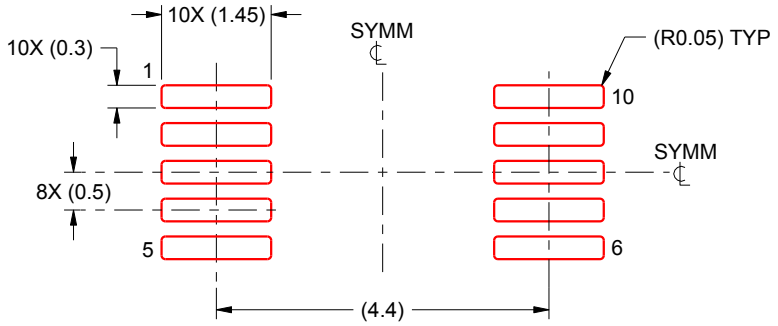



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



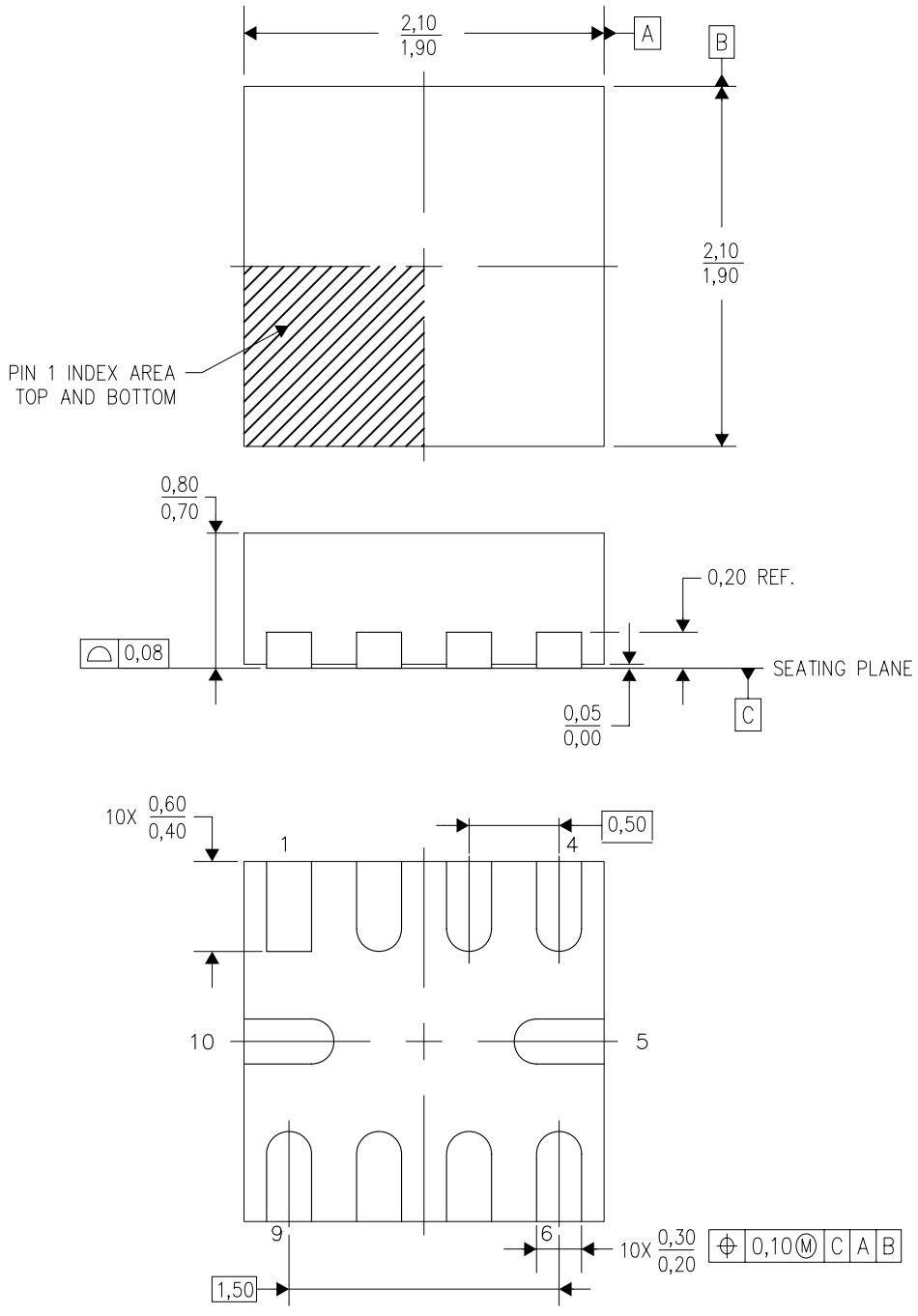

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

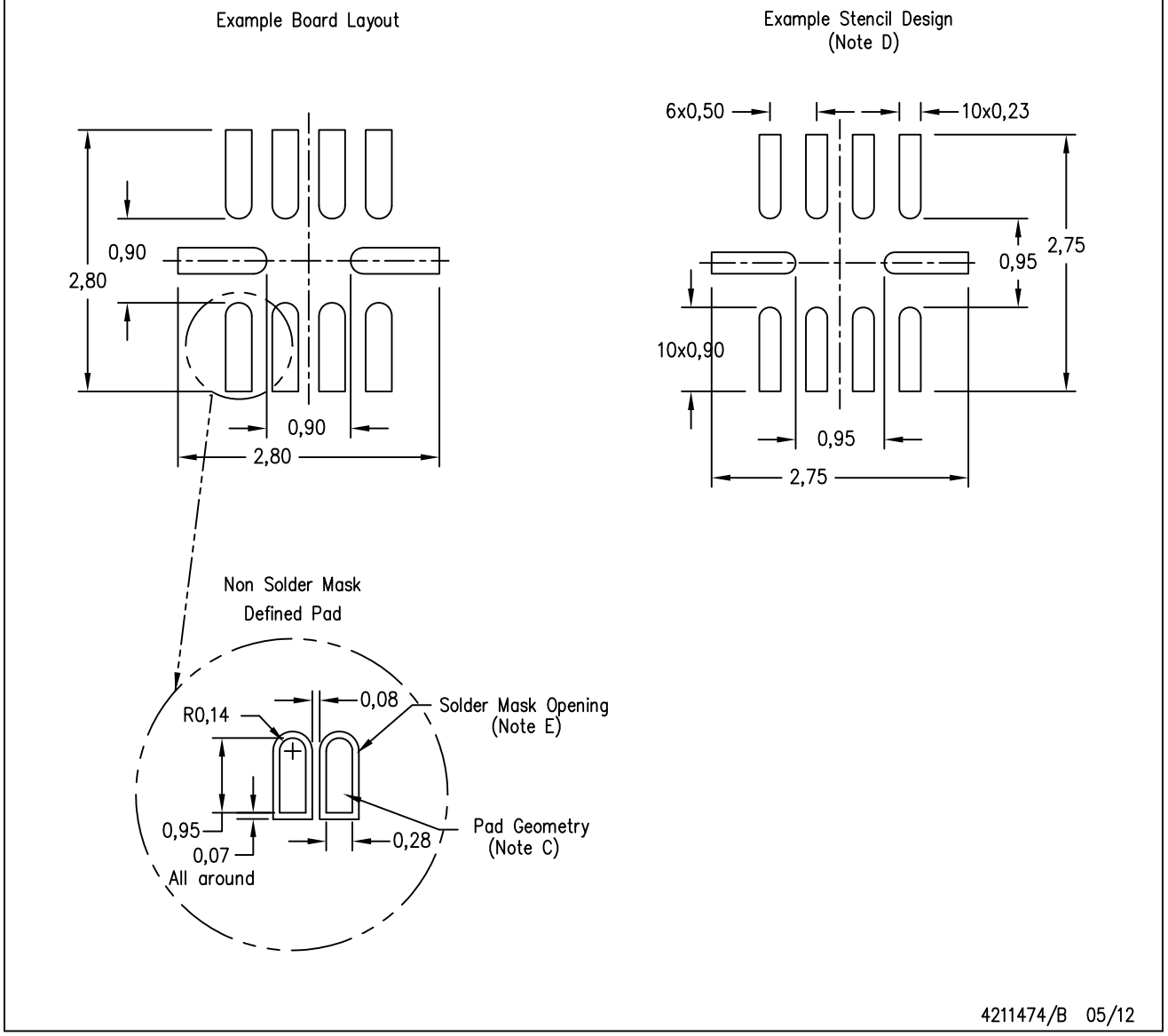
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RUN (S–PWQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



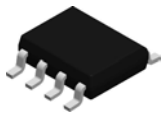

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.

# RUN (S–PWQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




4211474/B 05/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

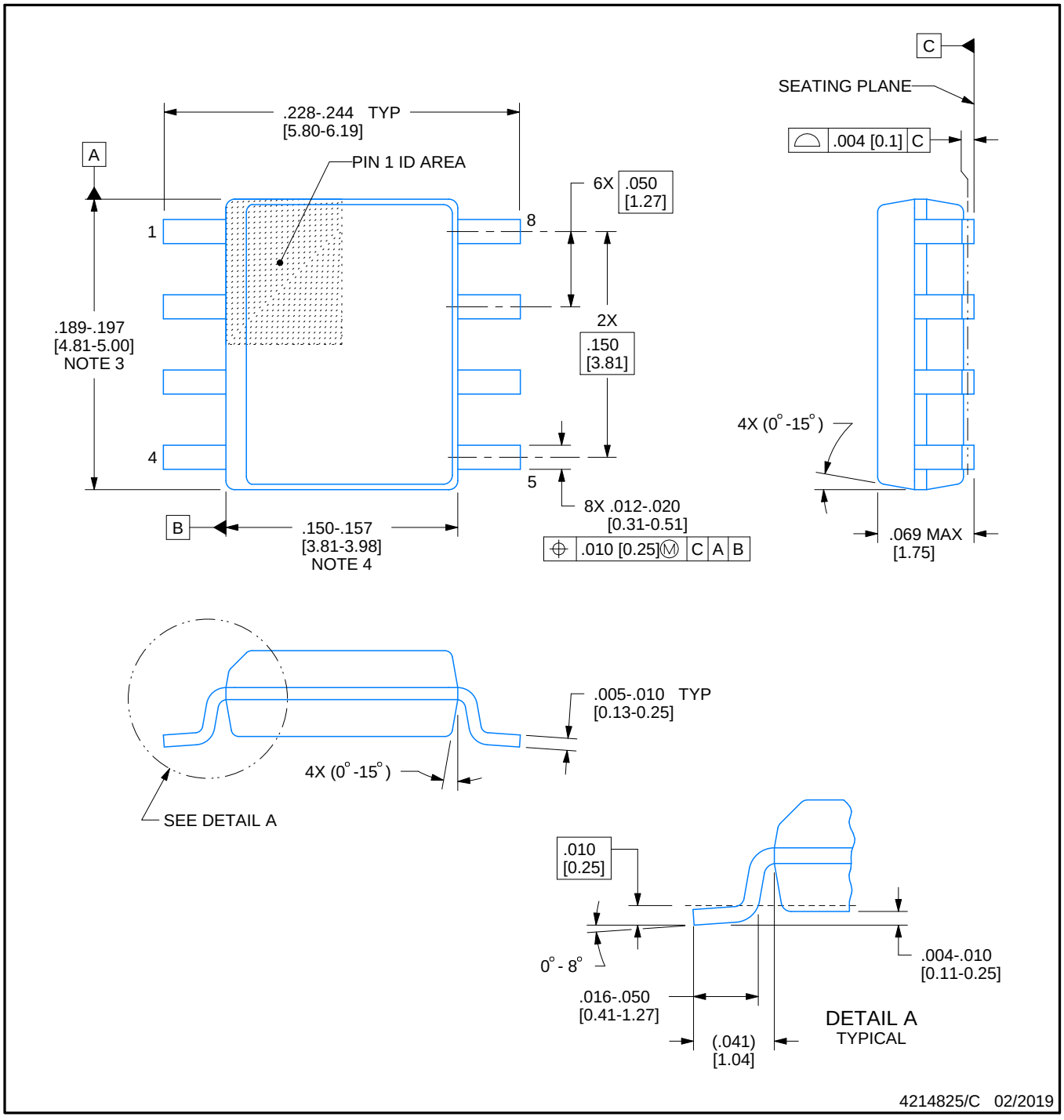


# PACKAGE OUTLINE

## D0008A

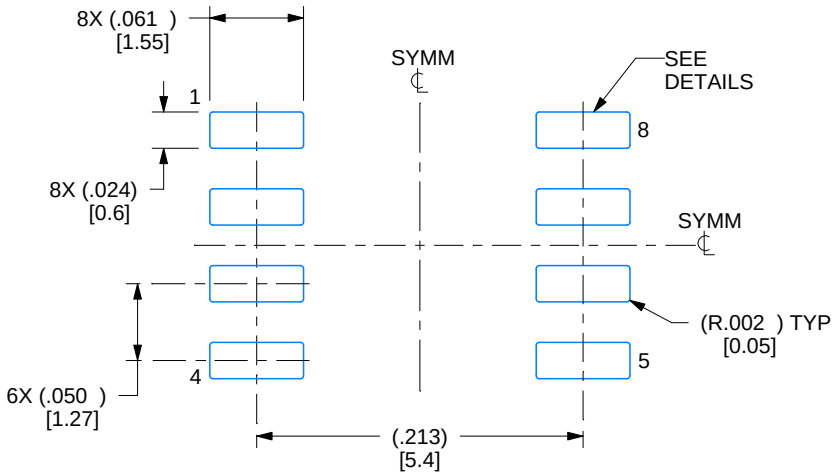
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

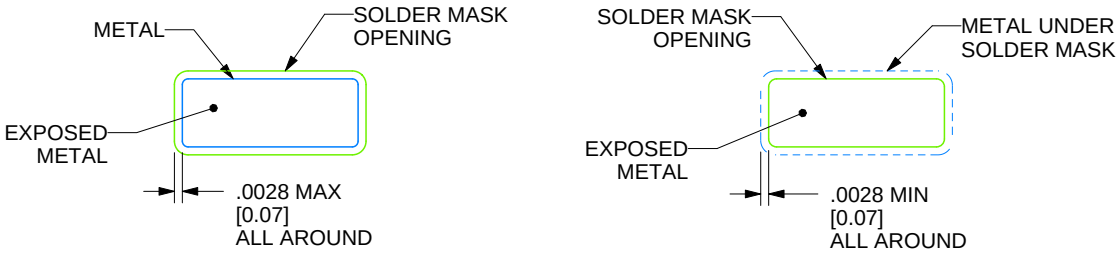



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

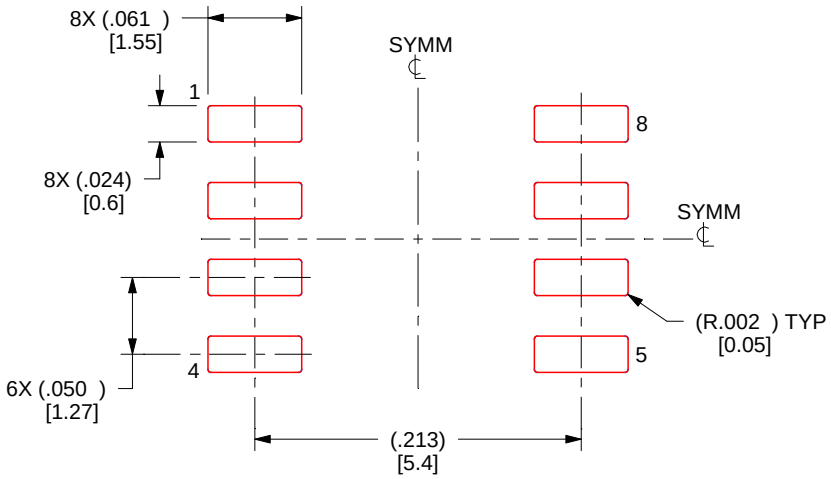
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

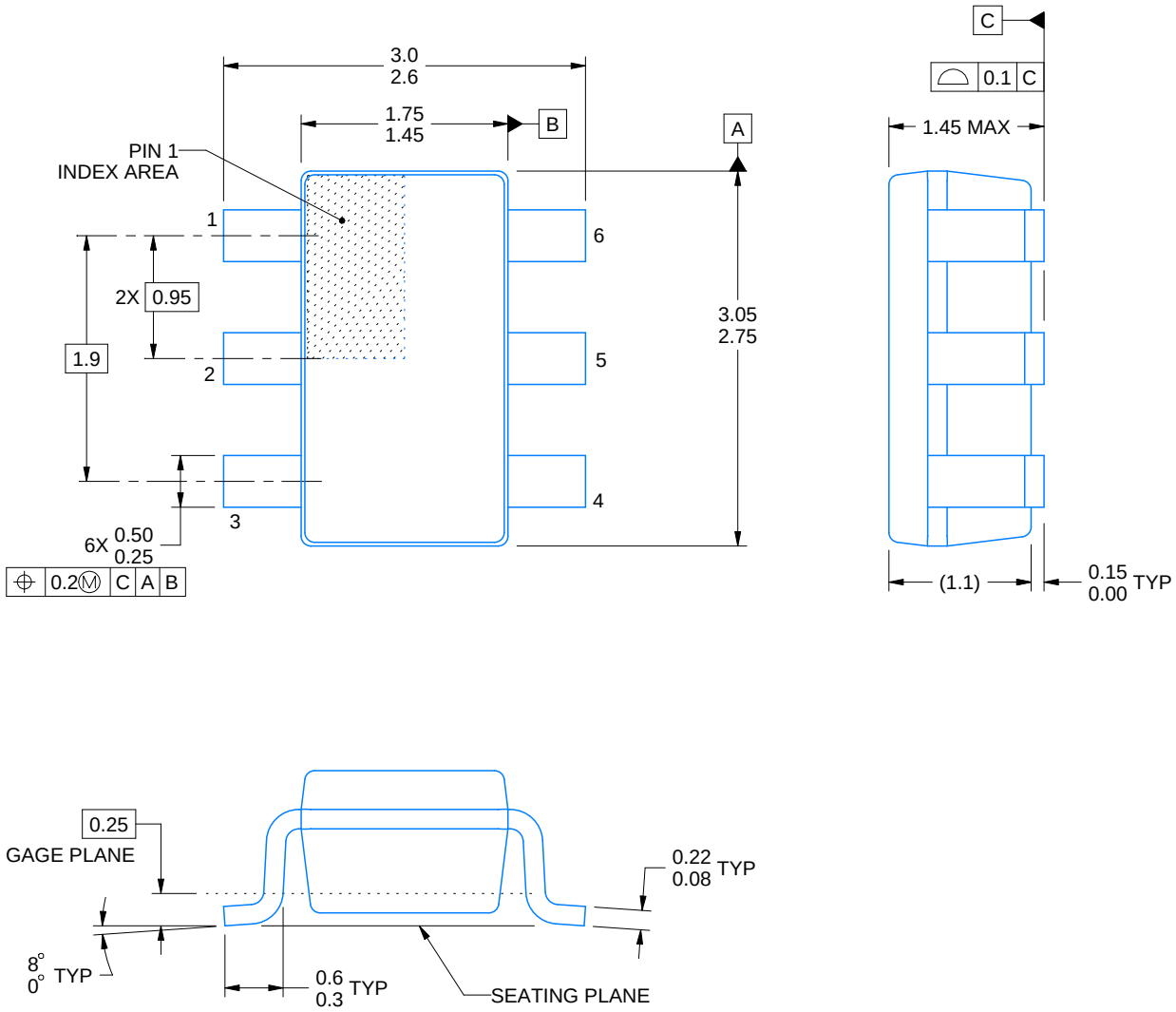
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

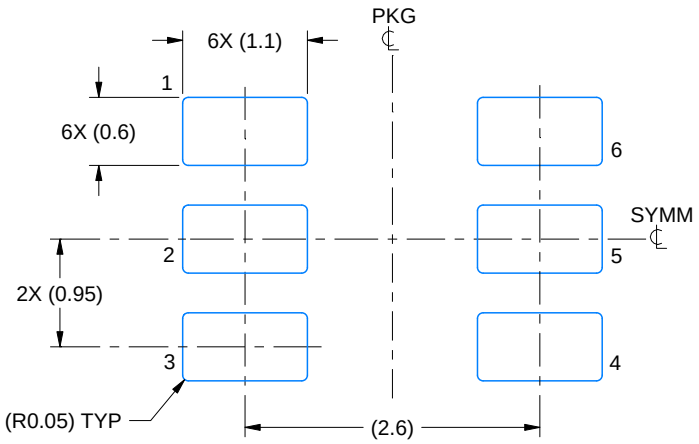
SMALL OUTLINE TRANSISTOR



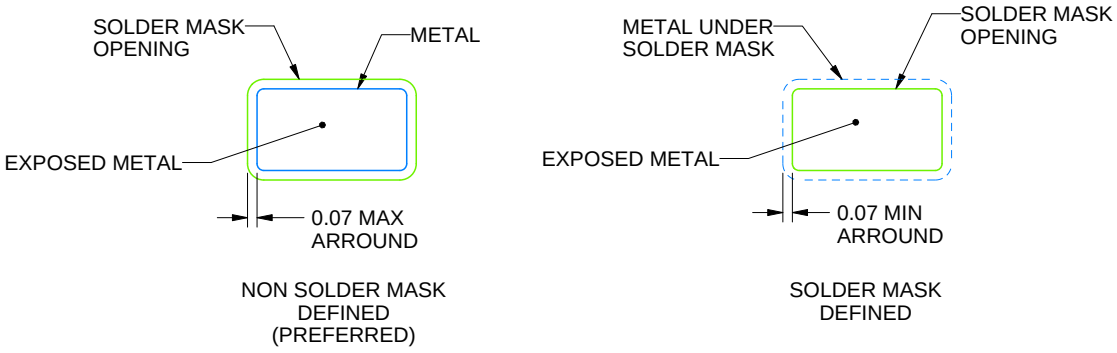

4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

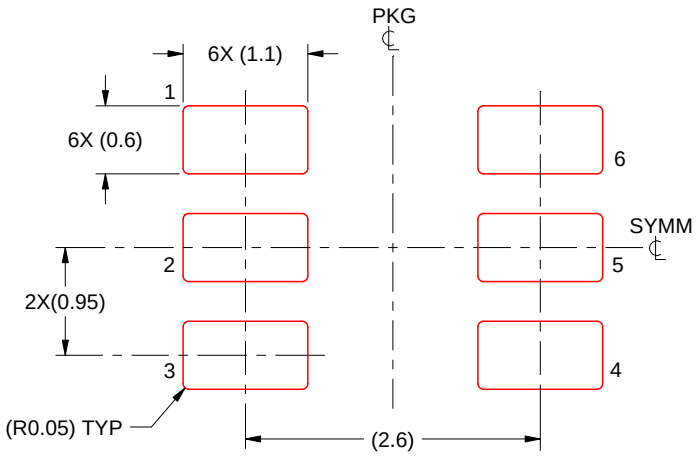



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



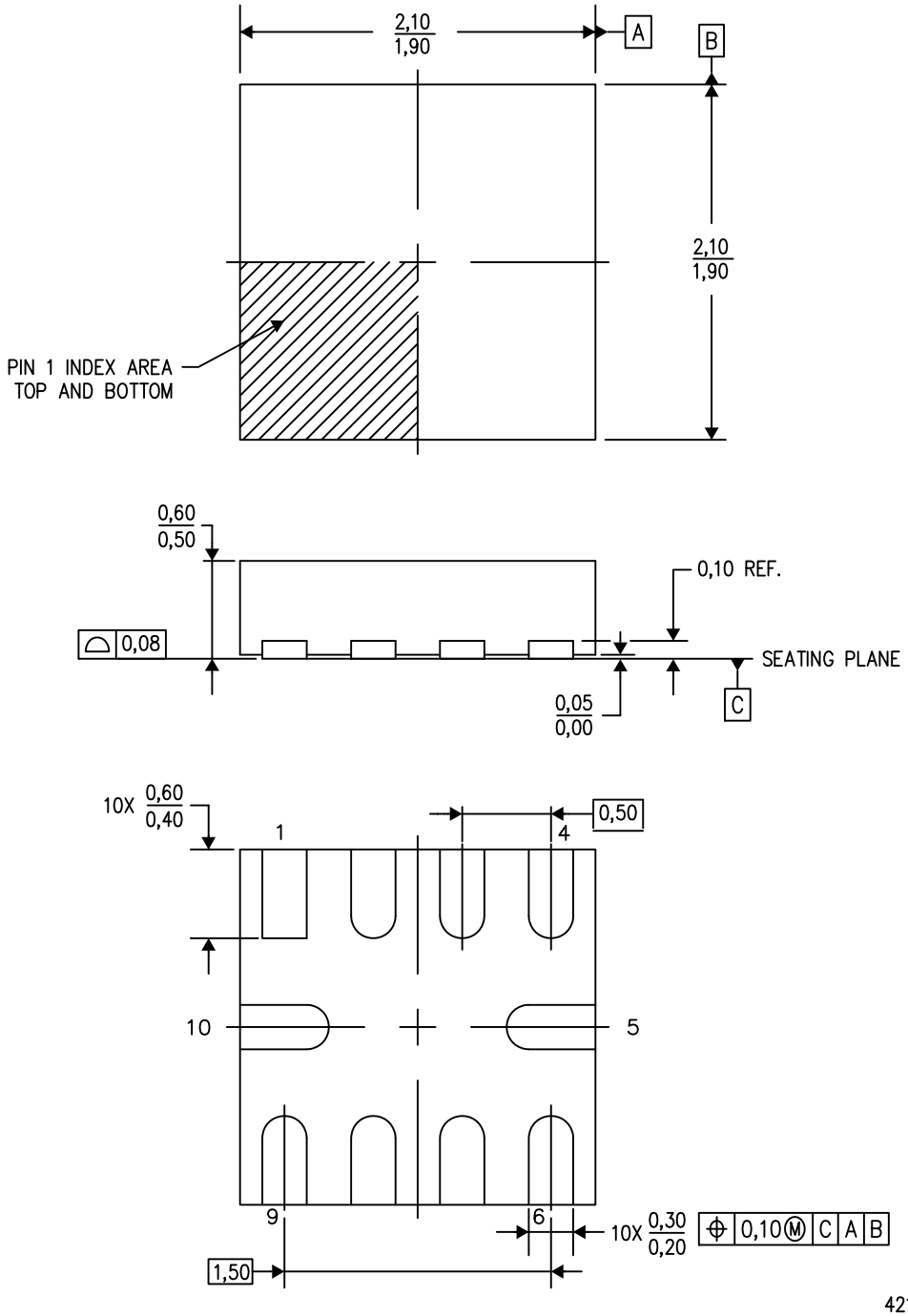

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

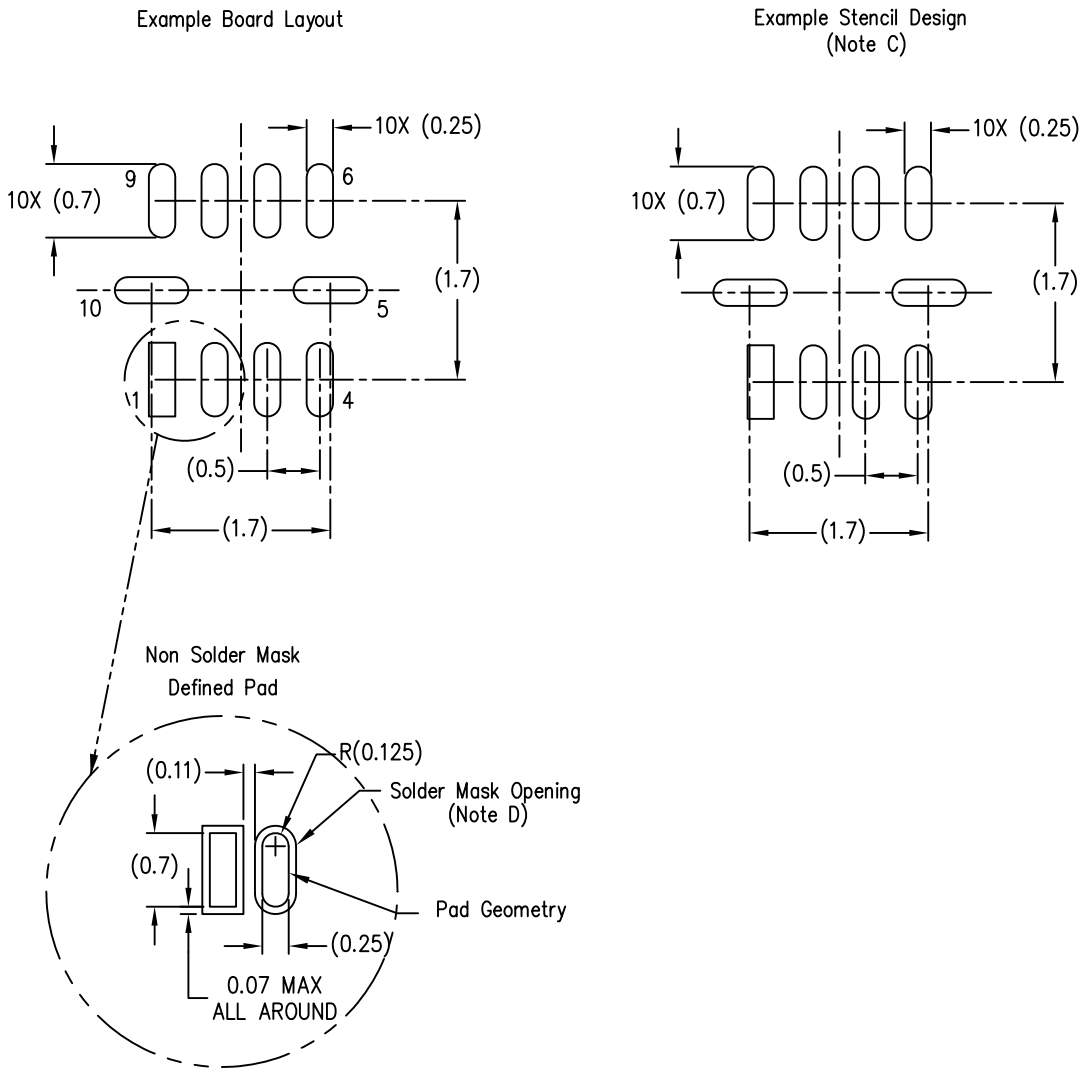
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RMC (S–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.

RMC (S–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




4221693/A 10/2014

NOTES:
A. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# 重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司