具有 4-V/V 增益的三通道 ED 滤波器视频放大器

查询样品: THS7320

特性

- 超低的总静态电流：**3.5 mA**（在 **3 V** 电压下）
- 停用电源电流：**0.15 µA**
- 三阶 **Butterworth** 低通滤波器：
  - **–1 dB**（在 **17 MHz** 频率下）
  - **–3 dB**（在 **20 MHz** 频率下）
  - 衰减：**21 dB**（在 **43 MHz** 频率下）
  - 支持 **Y'P'$_B$P'$_R$ 480p/576p** 或 **R'G'B'** 视频
  - 支持过采样系统生成 **CVBS**、**S** 视频或 **Y'P'$_B$P'$_R$ 480i/576i**
- 具有 **150-mV** 输出漂移的 **DC** 耦合输入
- 内置增益：**4 V/V (12 dB)**
- 单电源操作：**+2.6 V** 至 **+5 V**
- 轨至轨输出支持 **AC** 或 **DC** 耦合
- 低差分增益/相位：**0.1%/0.1°**
- 输出引脚支持 **±8-kV IEC ESD** 保护
- 超小型的 **WCSP 9** 焊球封装：
  - 纤巧的 **PCB** 面积：**0.96 mm x 0.96 mm**（典型值）
  - 超低的高度：**0.5 mm**（最大值）
  - 间距：**0.3 mm**

应用

- 个人媒体播放器
- 数码相机
- 蜂窝电话视频输出缓冲

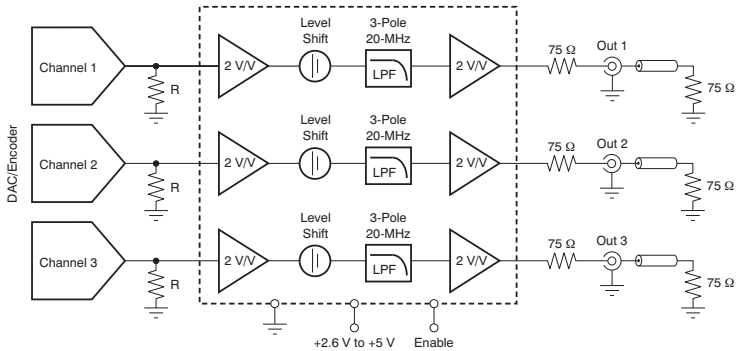
说明

THS7320 采用革命性的互补型锗化硅 (SiGe) BiCom-3X 工艺制造，是一款超低功耗、单电源、2.6 V 至 5 V、三通道集成型视频缓冲器，具有 4 V/V 的增益。该器件非常适合于将尺寸与功耗作为重要参数的电池供电型应用。总静态电流仅为 3.5 mA（在 3 V 电压下），而视频部分在停用时的静态电流最低可减小至 0.15 µA。

THS7320 的视频部分包括三个具有三阶 Butterworth 特性的增强型分辨率 (ED) 滤波器通道。 .这些滤波器可用作数模转换器 (DAC) 重构滤波器或模数转换器 (ADC) 抗混叠滤波器。 另外，THS7320 还非常适合于过采样系统，此类系统可产生标准分辨率 (SD) 信号，包括 CVBS、S 视频、480i/576iY'P'$_B$P'$_R$、Y'U'V' 和 R'G'B'。

THS7320 专为 DC 耦合输入而设计。 为了减轻任意的 DAC/编码器终端干扰，采用了超高 (2.4 MΩ) 的输入阻抗。 内部电平移位在输出端增加了 150 mV 补偿，以消除饱和或限幅问题。 轨至轨输出支持 DC 或 AC 耦合。

THS7320 采用一种超小型的 9 焊球晶圆芯片规模封装 (WCSP)，这种封装仅需占用超小的 0.92-mm^2（典型值）印刷电路板 (PCB) 面积。



简化的应用电路

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
THS7320IYHCR	DSBGA (9-Ball WCSP)	QJK	Tape and Reel, 3000	Pb-Free, Green
THS7320IYHCT	DSBGA (9-Ball WCSP)	QJK	Tape and Reel, 250	Pb-Free, Green

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Eco-Status information. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree.
Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage, V_{S+} to GND		–0.4 to +5.5	V
Video input voltage, video enable pin		–0.4 to V_{S+} + 0.4	V
Output current, I_O		±75	mA
Continuous power dissipation		See Thermal Information table	
Maximum junction temperature, any condition(2), T_J		+150	°C
Maximum junction temperature, continuous operation, long-term reliability(3), T_J		+125	°C
Storage temperature range, T_{stg}		+300	°C
ESD ratings: all pins	Human body model (HBM)	6000	V
	Charge device model (CDM)	1000	V
	Machine model (MM)	200	V
ESD ratings: video output pins	IEC 61000-4-2 contact discharge	20	kV

(1) Stresses these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	2.6	3	5	V
Ambient temperature, T_A	–40		+85	°C

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ELECTRICAL CHARACTERISTICS: V_{S+} = 3 V, Video Section

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input and output, unless otherwise noted.

PARAMETER	CONDITIONS	THS7320IYHC			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
AC PERFORMANCE						
Passband bandwidth	–0.1 dB, relative to 1 MHz		11		MHz	C
	±1 dB, relative to 1 MHz	14	17		MHz	A
–3-dB bandwidth	Relative to 1 MHz	17	20		MHz	B
Normalized stop band gain	f = 43 MHz, relative to 1 MHz		–21	–12	dB	A
	f = 54 MHz, relative to 1 MHz		–27		dB	C
Group delay	f = 100 kHz		19		ns	C
Group delay variation	f = 11 MHz with respect to 1 MHz		4		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC and PAL		0.1		%	C
Differential phase	NTSC and PAL		0.1		°	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–80		dB	C
Signal-to-noise ratio	100 kHz to 13.5 MHz, non-weighted		65		dB	C
	100 kHz to 13.5 MHz, unified weighting		75		dB	C
	100 kHz to 6 MHz, non-weighted		69		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Rise/fall time	V_{OUT} = 2-V step		20		ns	C
Slew rate	V_{OUT} = 2-V step		80		V/µs	C
Output impedance	f = 12 MHz		1.4		Ω	C
	f = 12 MHz, return loss		41		dB	C
	Disabled		20 || 11		kΩ || pF	C
Crosstalk	Output referred at connectors, f = 10 MHz		–51		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V	75	150	320	mV	A
Input voltage range	At dc input, limited by output		–0.03 to 0.65		V	C
Input bias current		–1000	–130	–40	nA	A
Input resistance			2.4 || 2		MΩ || pF	C
Voltage gain		3.92	4	4.08	V/V	A
Gain matching	Channel-to-channel	–1	±0.2	+1	%	A
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to GND	2.62	2.8		V	A
Low output voltage swing	R_L = 150 Ω to GND		0.01		V	C
Output current	Short-circuit		65		mA	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation only. (C) Typical value only for information.

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ELECTRICAL CHARACTERISTICS: V_{S+} = 3 V, Video Section (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input and output, unless otherwise noted.

PARAMETER	CONDITIONS	THS7320IYHC			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
POWER SUPPLY (V_{S+})						
Operating Voltage	V_{S+}	2.5	3	5.5	V	B
V_{S+} total quiescent current	Video enable pin = 1.8 V, no load, V_{IN} = 0 V	2.7	3.5	4.7	mA	A
	Video enable pin = 0 V, no load, V_{IN} = 0 V		0.15	1	µA	A
V_{S+} power-supply rejection ratio (PSRR)	At dc	44	50		dB	A
VIDEO ENABLE LOGIC CHARACTERISTICS						
V_{IH}	Enabled	1.17			V	A
V_{IL}	Disabled			0.4	V	A
I_{IH}	Enable pin = 1.8 V, current flows into the pin		1.8	3	µA	A
I_{IH}	Enable pin = 3 V, current flows into the pin		3	5	µA	A
I_{IL}	Enable pin = 0 V, current flows into the pin		–0.01	–0.5	µA	A
Input resistance			1		MΩ	C
Disable time			130		ns	C
Enable time			120		ns	C

THERMAL INFORMATION

THERMAL METRIC(1)		THS7320IYHC	UNITS
		YHC	
		9 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	159.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	2.2	
θ_{JB}	Junction-to-board thermal resistance	2.4	
ψ_{JT}	Junction-to-top characterization parameter	8.9	
ψ_{JB}	Junction-to-board characterization parameter	88.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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VIDEO PARAMETER MEASUREMENT INFORMATION

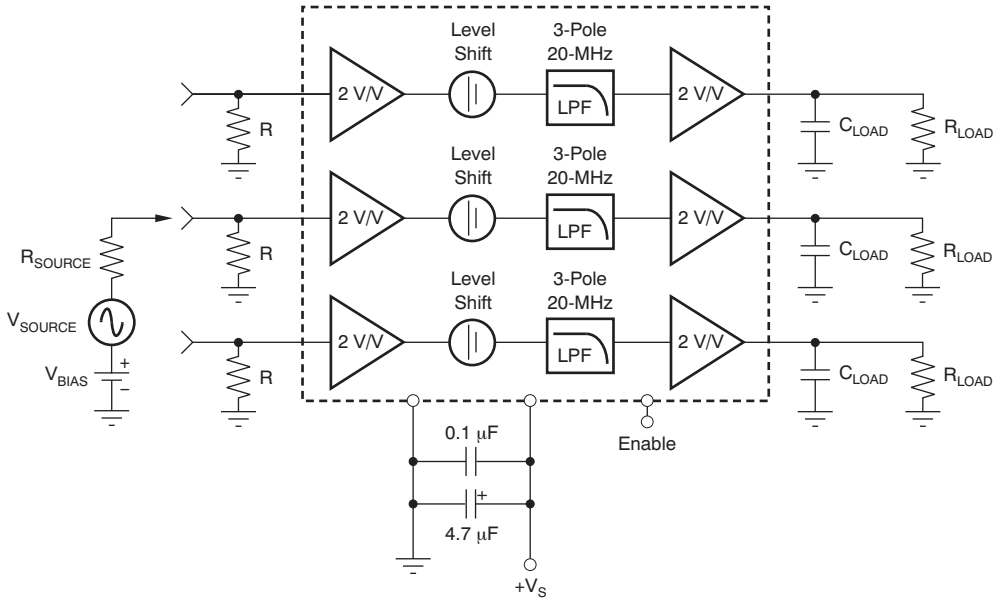
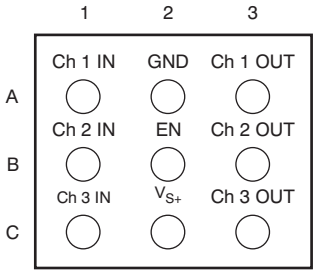


Figure 1. Test Circuit

PIN CONFIGURATION

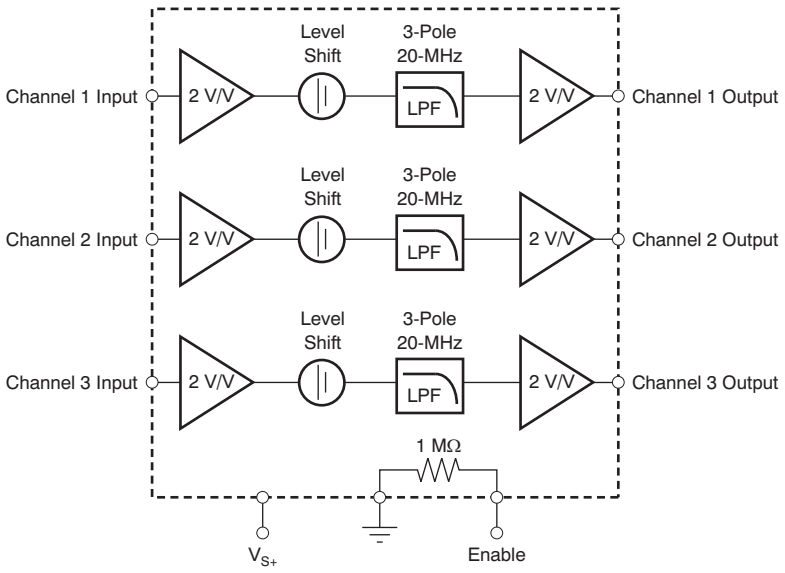
YHC PACKAGE
WCSP 9-BALL
(TOP VIEW)



PIN ASSIGNMENTS

NAME	NO.	I/O	DESCRIPTION
Channel 1 input	A1	I	Video input, channel 1
GND	A2	I	Ground for all circuitry
Channel 1 output	A3	O	Video output, channel 1
Channel 2 input	B1	I	Video input, channel 2
EN	B2	I	Video enable pin. Logic high enables the video channels; logic low disables the video channels.
Channel 2 output	B3	O	Video output, channel 2
Channel 3 input	C1	I	Video input, channel 3
V_{S+}	C2	I	Power-supply pin; connect to +2.6 V up to +5 V.
Channel 3 output	C3	O	Video output, channel 3

FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

Table 1. Table of Graphs: V_{S+} = 2.6 V

TITLE	FIGURE
Signal Gain vs Frequency	Figure 2, Figure 3
Phase vs Frequency	Figure 4
Group Delay vs Frequency	Figure 5
Differential Gain	Figure 6
Differential Phase	Figure 7
Small-Signal Frequency Response vs Capacitive Load	Figure 8
Small-Signal Frequency Response vs Resistive Load	Figure 9
Crosstalk vs Frequency	Figure 10
Second-Order Harmonic Distortion vs Frequency	Figure 11
Third-Order Harmonic Distortion vs Frequency	Figure 12
Large-Signal Pulse Response vs Time	Figure 13
Small-Signal Pulse Response vs Time	Figure 14
Slew Rate vs Output Voltage	Figure 15
Enable/Disable Response vs Time	Figure 16

Table 2. Table of Graphs: V_{S+} = 3 V

TITLE	FIGURE
Signal Gain vs Frequency	Figure 17, Figure 18
Small-Signal Frequency vs Temperature	Figure 19, Figure 21
Small-Signal Frequency vs Temperature (Enlarged)	Figure 20, Figure 22
Phase vs Frequency	Figure 23
Group Delay vs Frequency	Figure 24
Differential Gain	Figure 25
Differential Phase	Figure 26
Small-Signal Frequency Response vs Capacitive Load	Figure 27
Small-Signal Frequency Response vs Resistive Load	Figure 28
Crosstalk vs Frequency	Figure 29
Second-Order Harmonic Distortion vs Frequency	Figure 30
Third-Order Harmonic Distortion vs Frequency	Figure 31
Large-Signal Pulse Response vs Time	Figure 32
Small-Signal Pulse Response vs Time	Figure 33
Slew Rate vs Output Voltage	Figure 34
Enable/Disable Response vs Time	Figure 35

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Table 3. Table of Graphs: V_{S+} = 5 V

TITLE	FIGURE
Signal Gain vs Frequency	Figure 36, Figure 37
Phase vs Frequency	Figure 38
Group Delay vs Frequency	Figure 39
Differential Gain	Figure 40
Differential Phase	Figure 41
Small-Signal Frequency Response vs Capacitive Load	Figure 42
Small-Signal Frequency Response vs Resistive Load	Figure 43
Crosstalk vs Frequency	Figure 44
Second-Order Harmonic Distortion vs Frequency	Figure 45
Third-Order Harmonic Distortion vs Frequency	Figure 46
Large-Signal Pulse Response vs Time	Figure 47
Small-Signal Pulse Response vs Time	Figure 48
Slew Rate vs Output Voltage	Figure 49
Enable/Disable Response vs Time	Figure 50

Table 4. Table of Graphs: General

TITLE	FIGURE
Output Impedance vs Frequency	Figure 51
S22 Output Return Loss vs Frequency	Figure 52
Disabled Output Impedance vs Frequency	Figure 53
Power-Supply Rejection Ratio vs Frequency	Figure 54

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TYPICAL CHARACTERISTICS: V_{S+} = 2.6 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

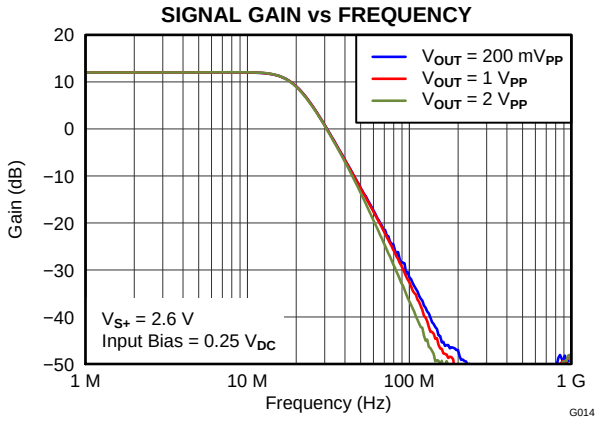


Figure 2.

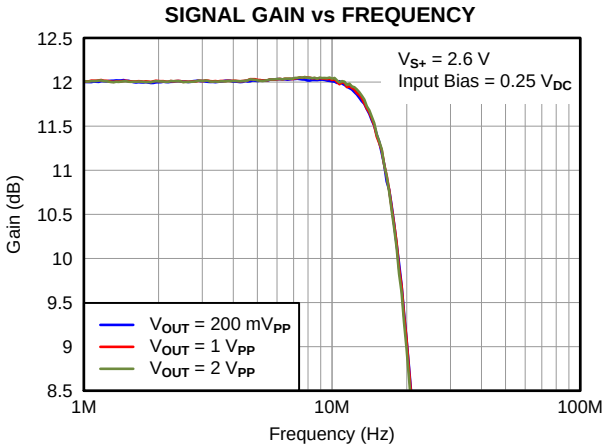


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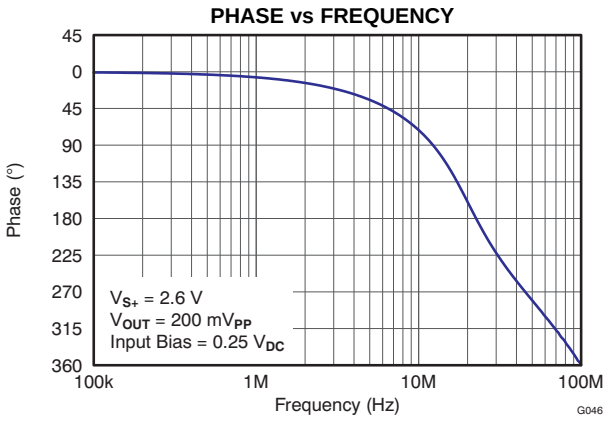


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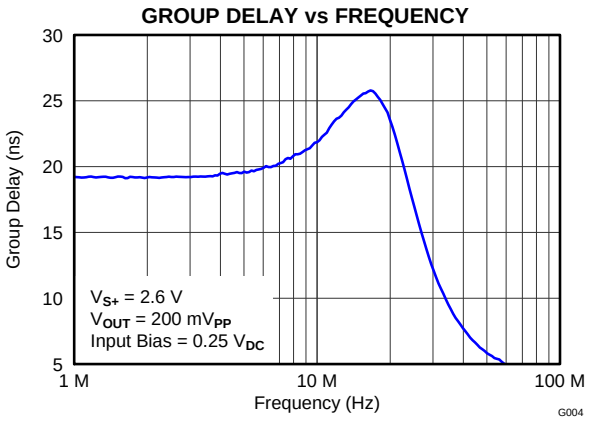


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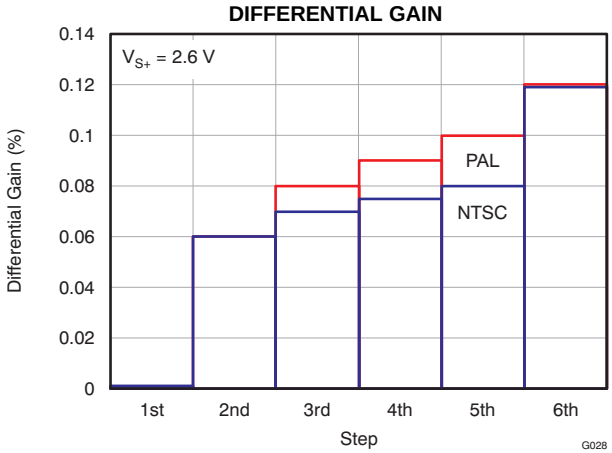


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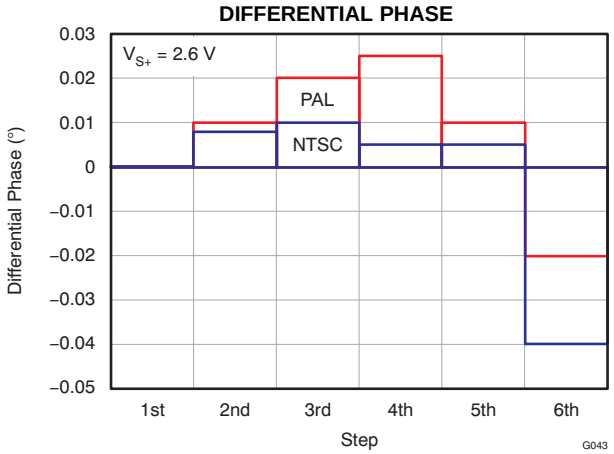


Figure 7.

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TYPICAL CHARACTERISTICS: V_{S+} = 2.6 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOAD

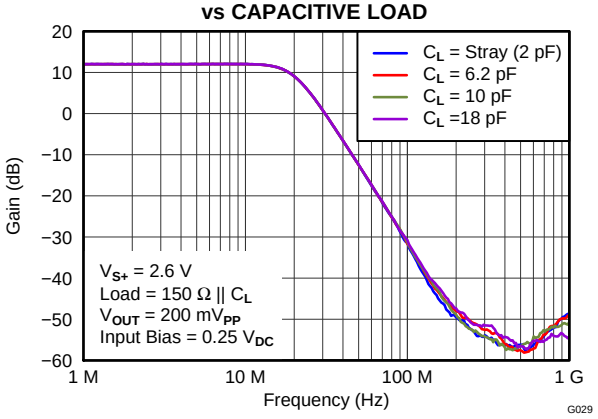


Figure 8.

SMALL-SIGNAL FREQUENCY RESPONSE vs RESISTIVE LOAD

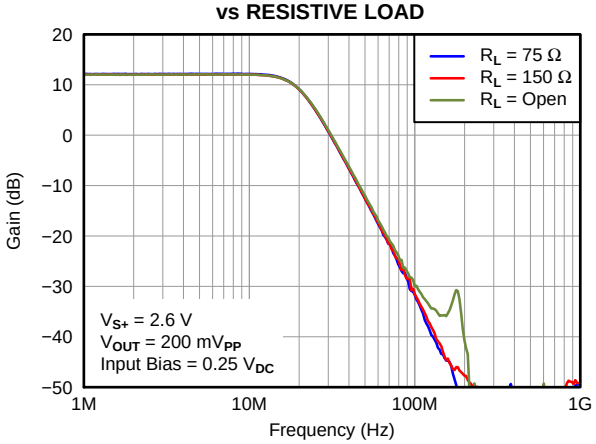


Figure 9.

CROSSTALK vs FREQUENCY (1)

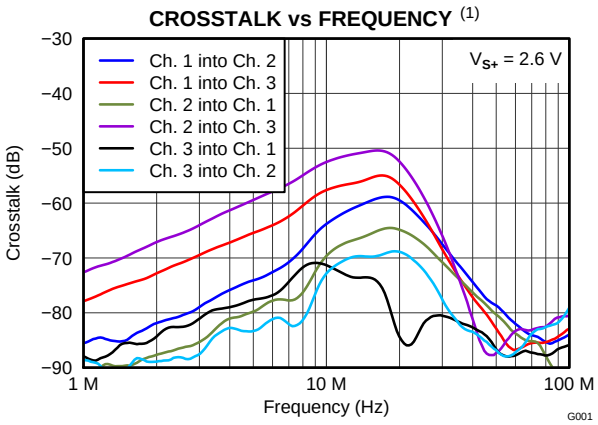


Figure 10.

SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

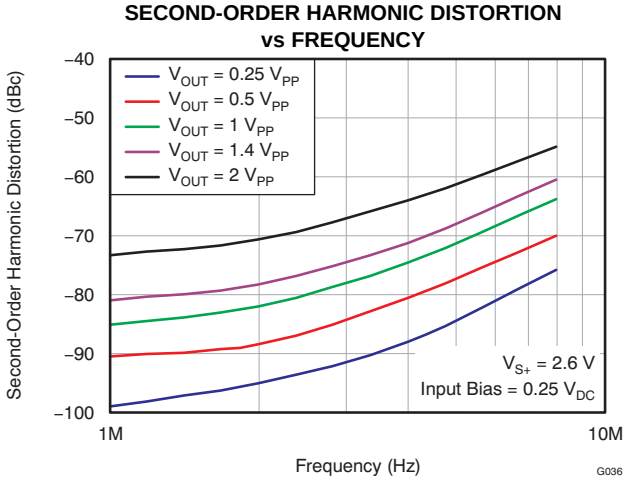


Figure 11.

THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

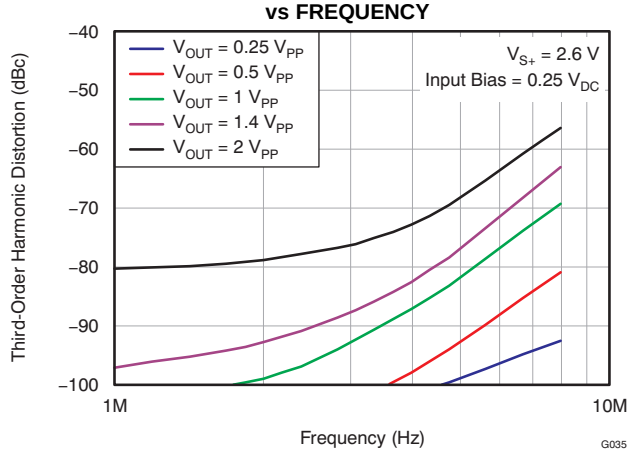


Figure 12.

LARGE-SIGNAL PULSE RESPONSE vs TIME

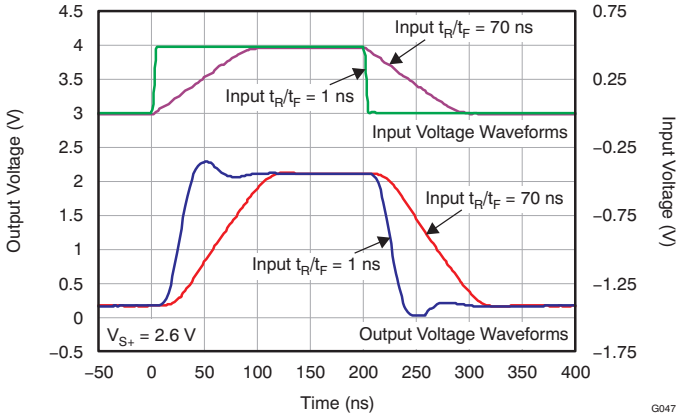


Figure 13.

(1) Measured at output connector relative to source output connector.

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TYPICAL CHARACTERISTICS: V_{S+} = 2.6 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

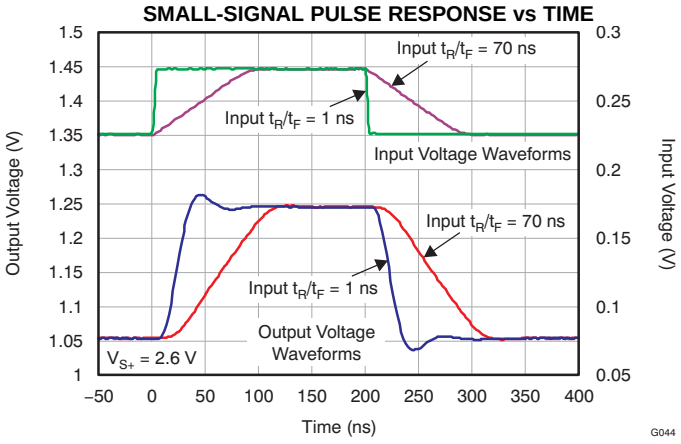


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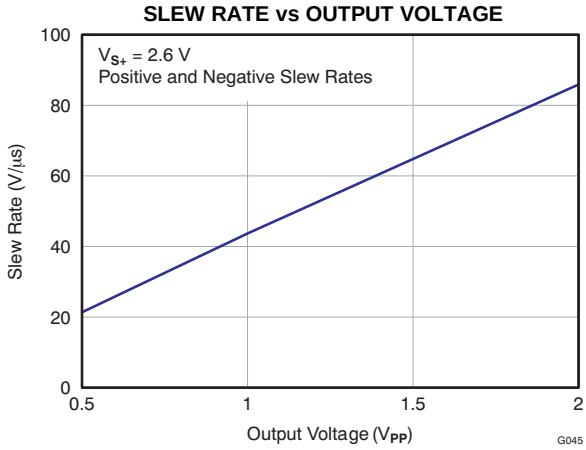


Figure 15.

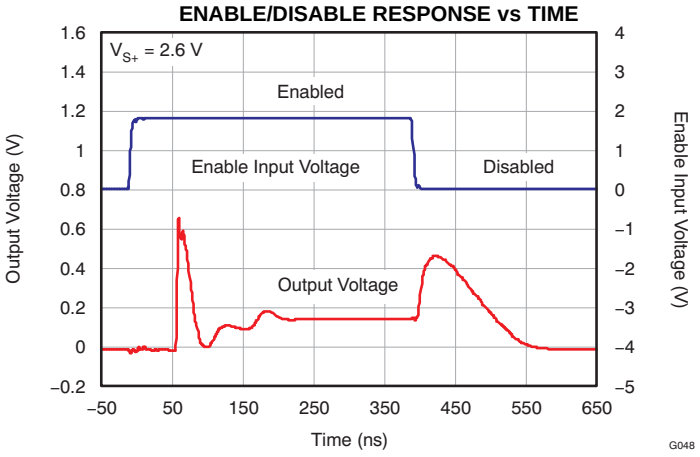


Figure 16.

TYPICAL CHARACTERISTICS: V_{S+} = 3 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

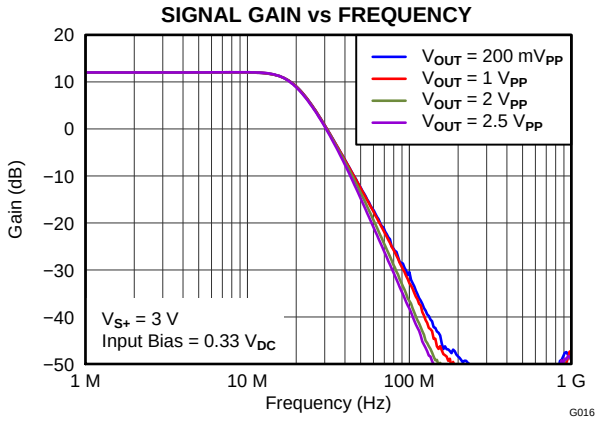


Figure 17.

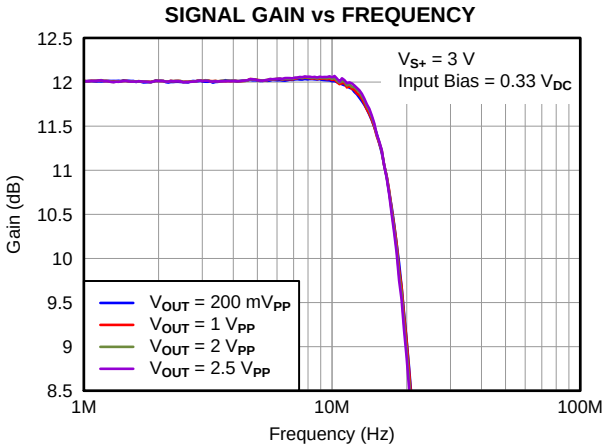


Figure 18.

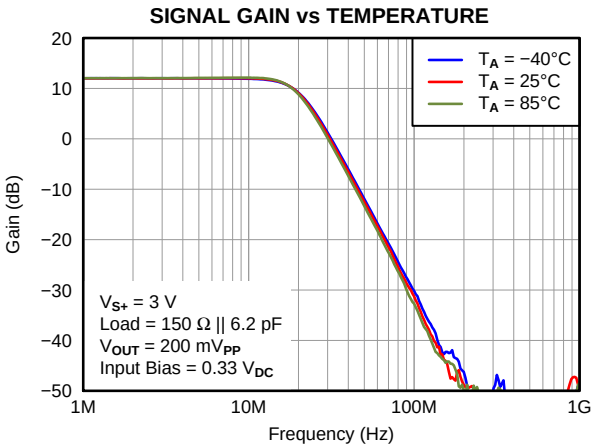


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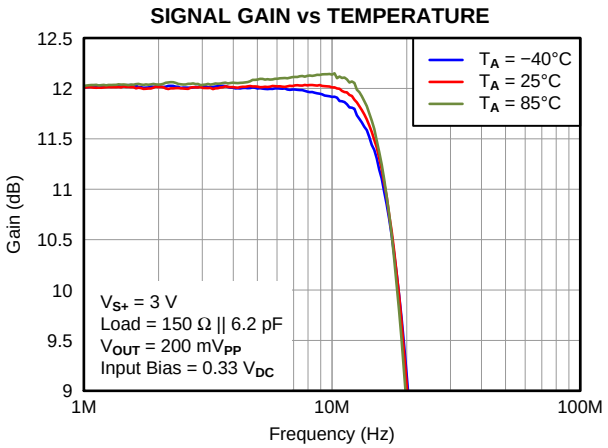


Figure 20.

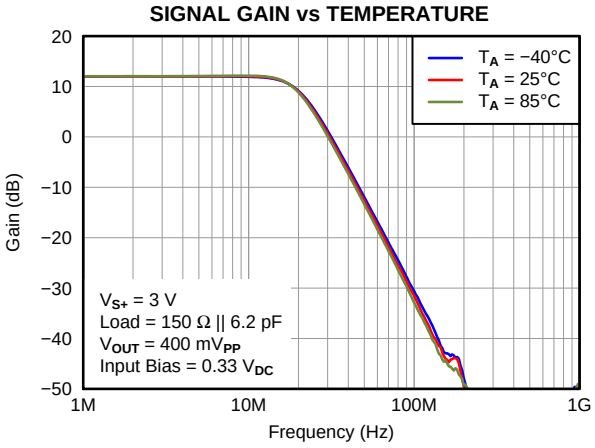


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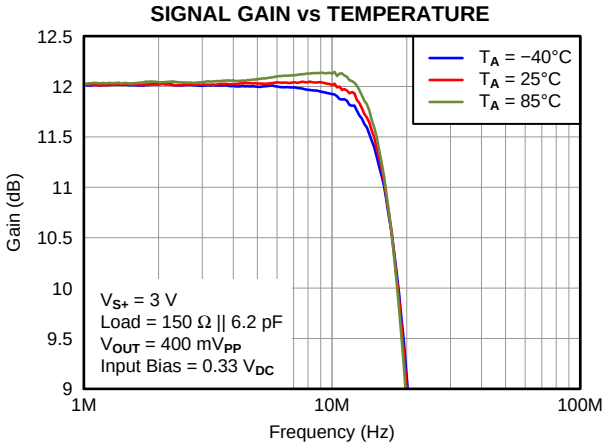


Figure 22.

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TYPICAL CHARACTERISTICS: V_{S+} = 3 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

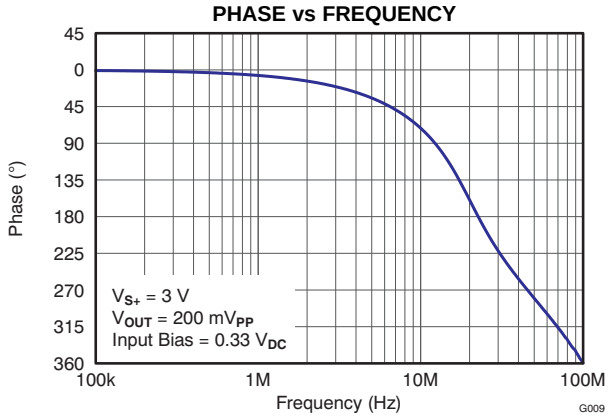


Figure 23.

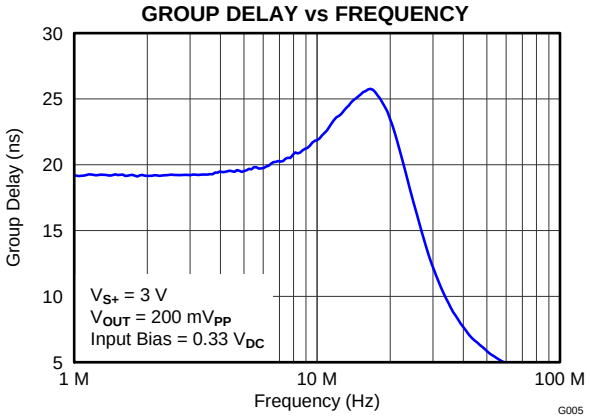


Figure 24.

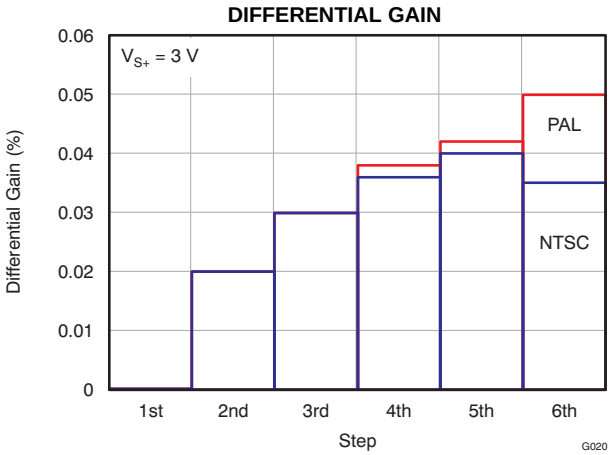


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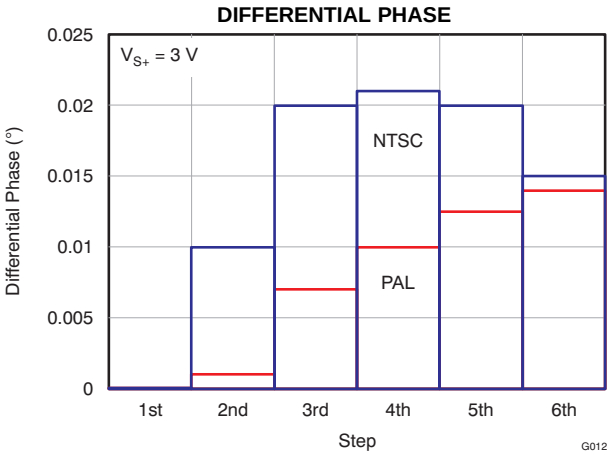


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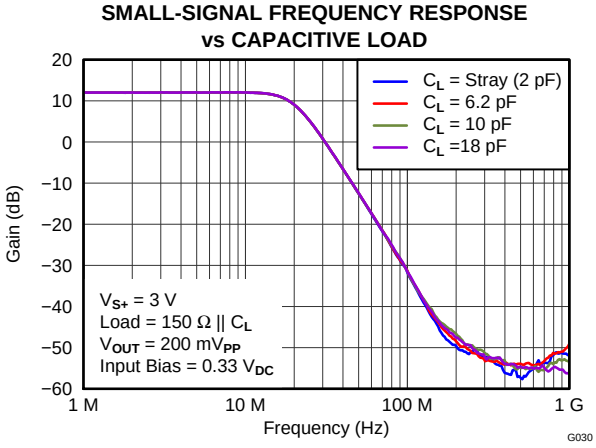


Figure 27.

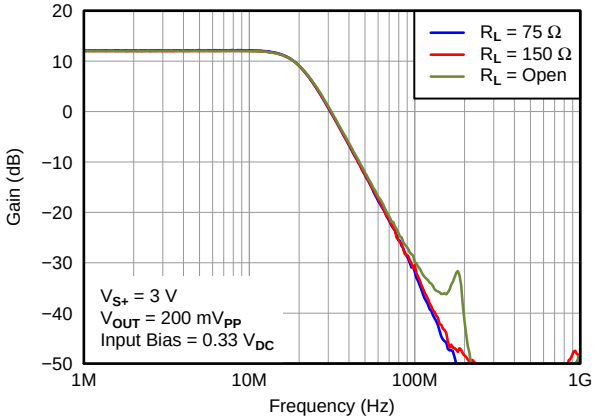


Figure 28.

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TYPICAL CHARACTERISTICS: V_{S+} = 3 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

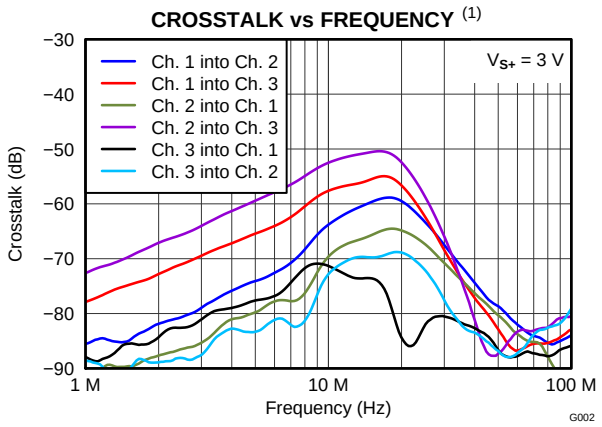


Figure 29.

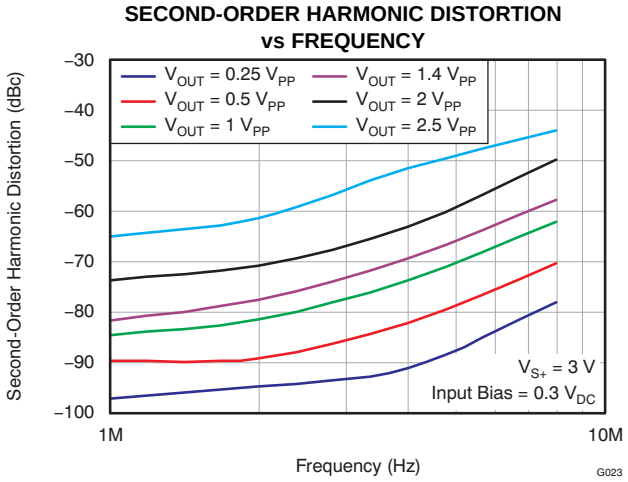


Figure 30.

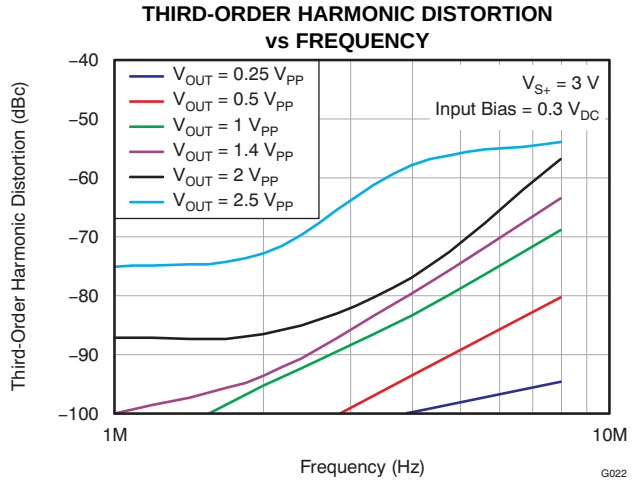


Figure 31.

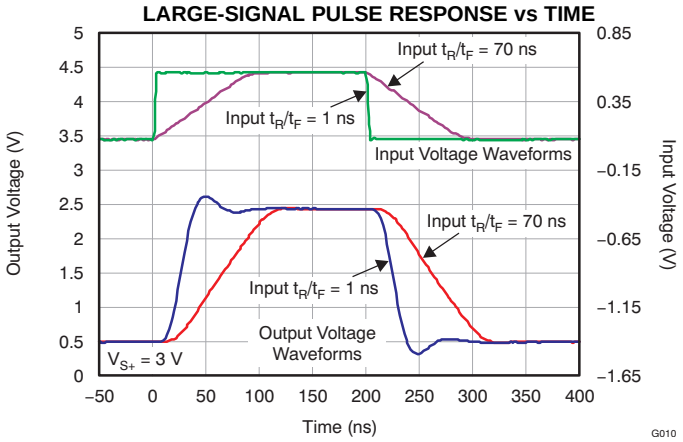


Figure 32.

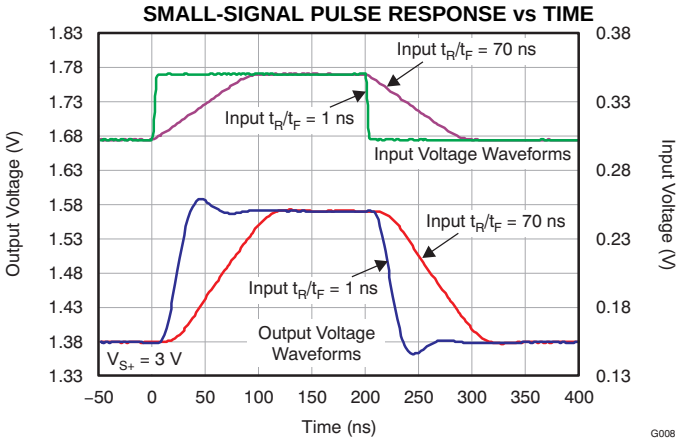


Figure 33.

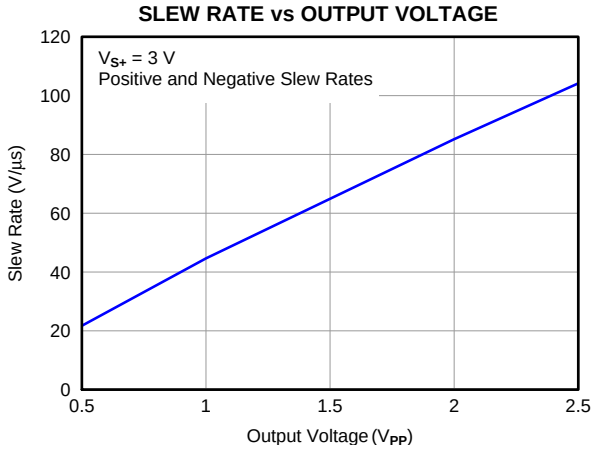


Figure 34.

(1) Measured at output connector relative to source output connector.

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TYPICAL CHARACTERISTICS: V_{S+} = 3 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

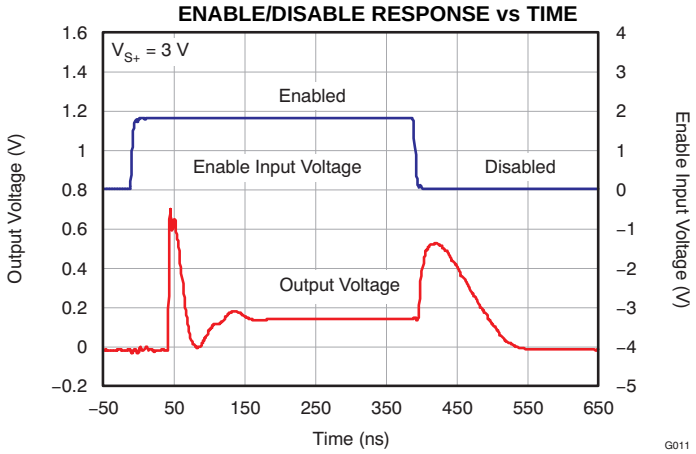


Figure 35.

TYPICAL CHARACTERISTICS: V_{S+} = 5 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

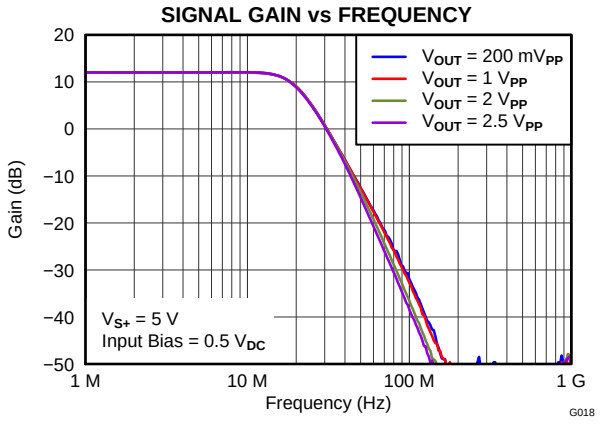


Figure 36.

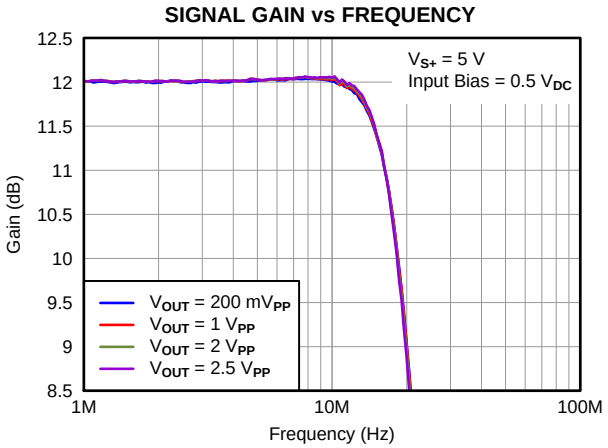


Figure 37.

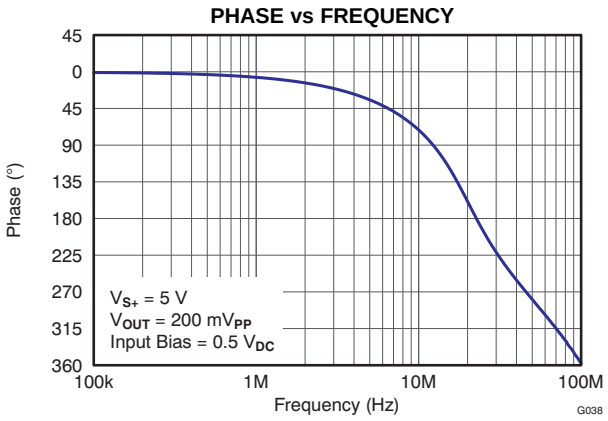


Figure 38.

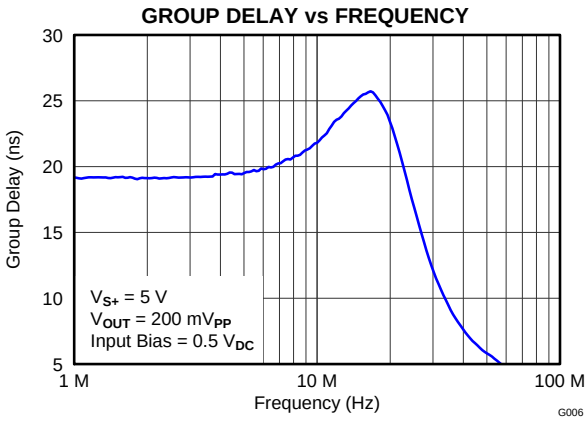


Figure 39.

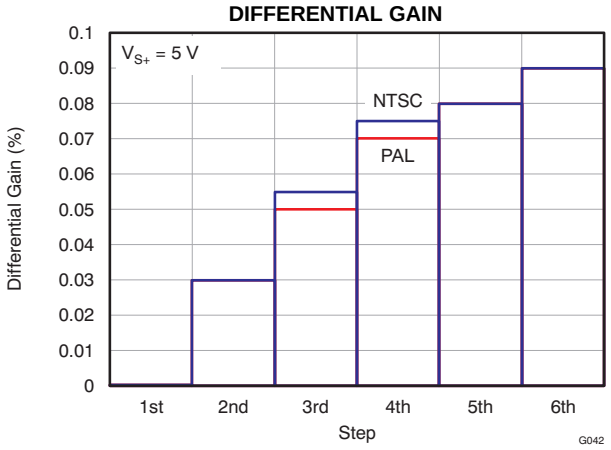


Figure 40.

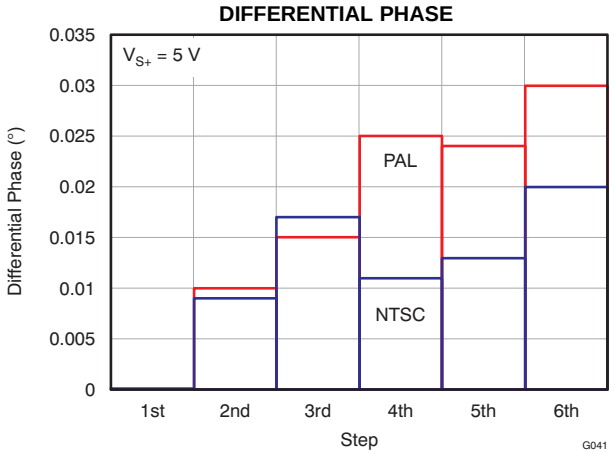


Figure 41.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOAD

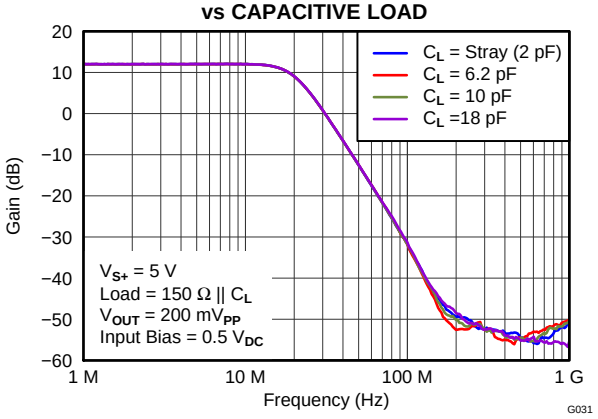


Figure 42.

SMALL-SIGNAL FREQUENCY RESPONSE vs RESISTIVE LOAD

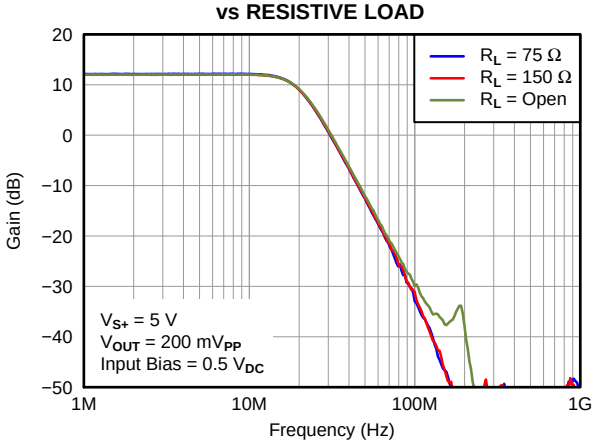


Figure 43.

CROSSTALK vs FREQUENCY (1)

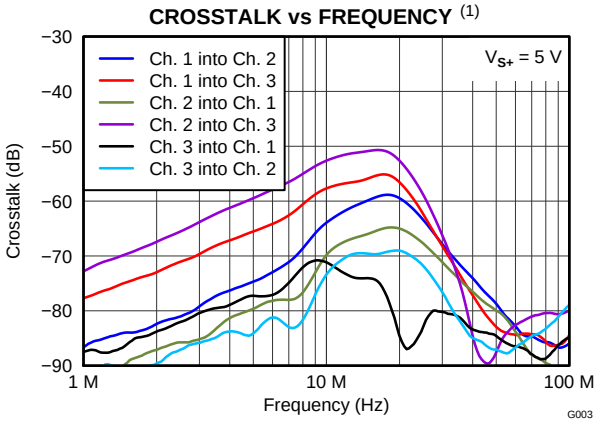


Figure 44.

SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

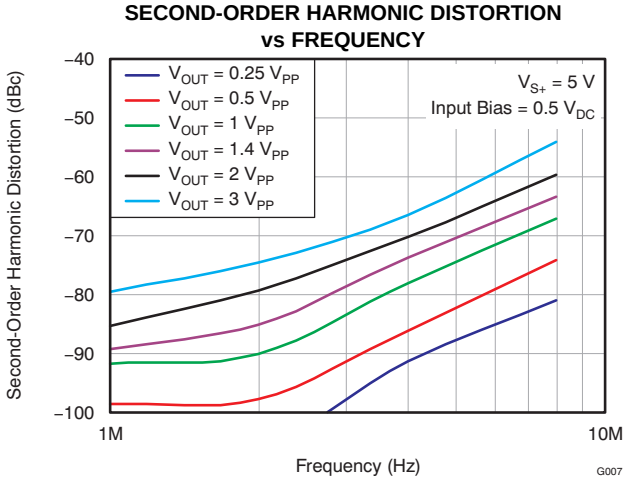


Figure 45.

THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

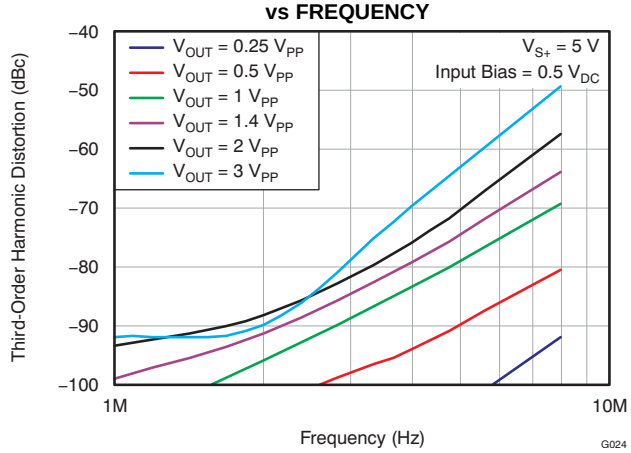


Figure 46.

LARGE-SIGNAL PULSE RESPONSE vs TIME

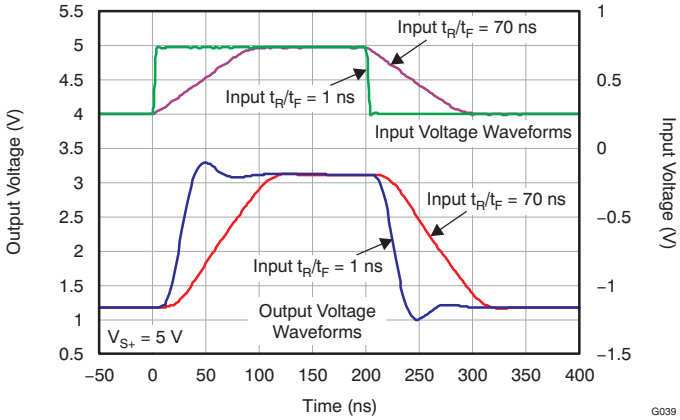


Figure 47.

(1) Measured at output connector relative to source output connector.

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TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SMALL-SIGNAL PULSE RESPONSE vs TIME

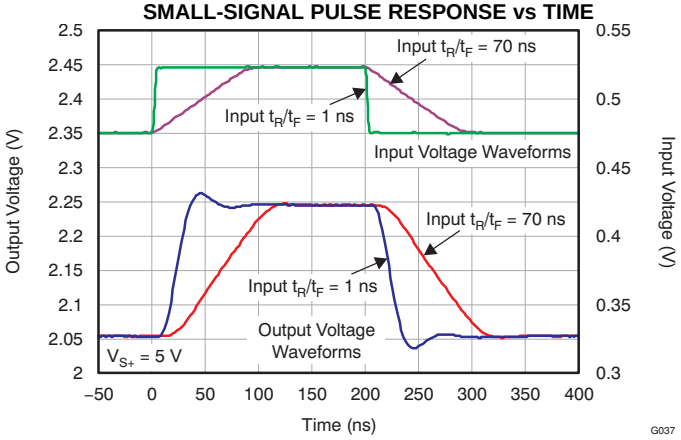


Figure 48.

SLEW RATE vs OUTPUT VOLTAGE

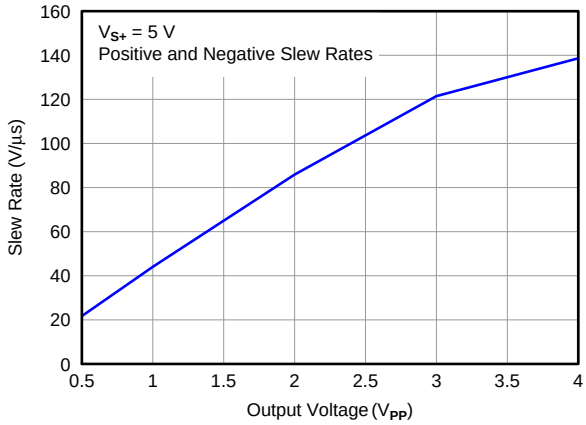


Figure 49.

ENABLE/DISABLE RESPONSE vs TIME

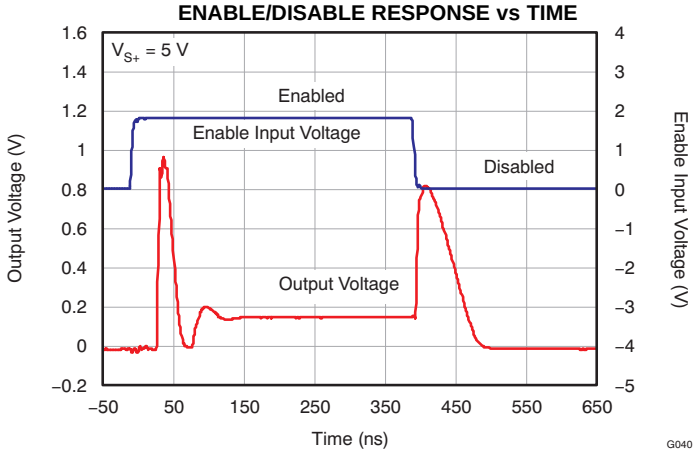


Figure 50.

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TYPICAL CHARACTERISTICS: General

At TA = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

OUTPUT IMPEDANCE vs FREQUENCY

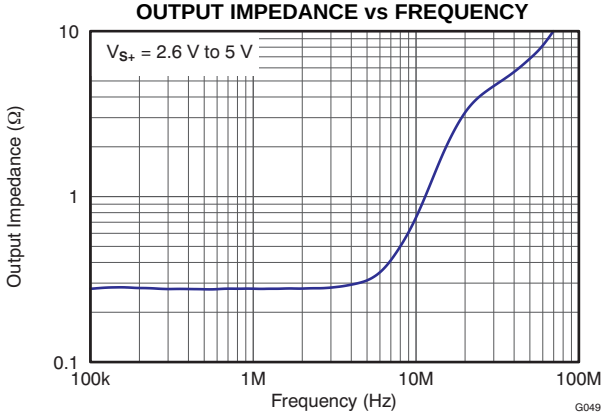


Figure 51.

S22 OUTPUT RETURN LOSS vs FREQUENCY

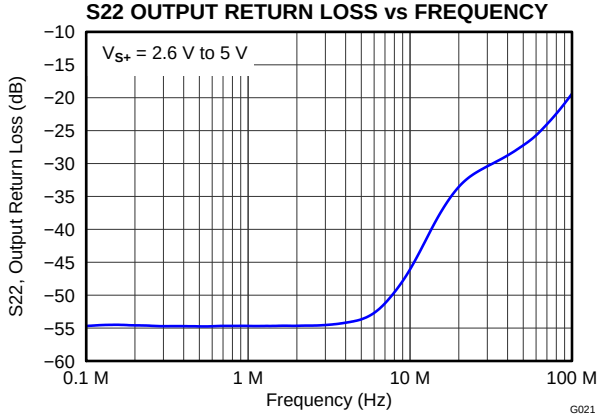


Figure 52.

DISABLED OUTPUT IMPEDANCE vs FREQUENCY

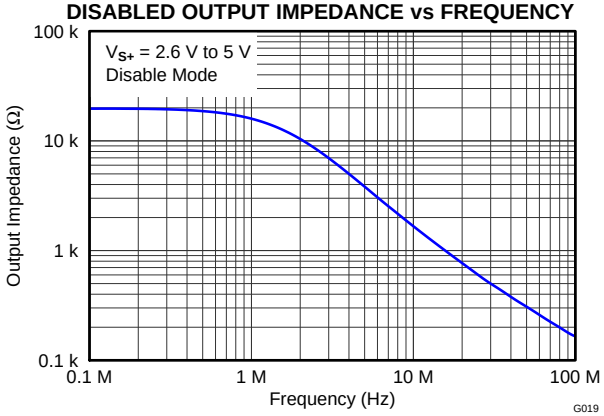


Figure 53.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

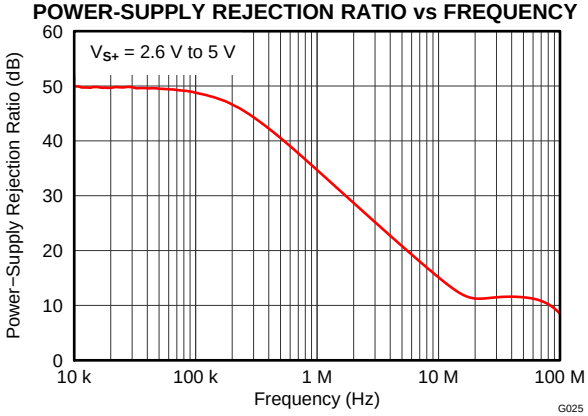


Figure 54.

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APPLICATION INFORMATION

The THS7320 includes a triple-channel video output amplifier and filter that supports three enhanced-definition (ED) video and/or RGB video output buffers. The THS7320 also supports standard definition (SD) video for oversampled systems with a DAC sampling frequency of 54 MHz or greater. Although the THS7320 can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters. Built on the revolutionary, complementary silicon germanium (SiGe) BiCom3X process, the THS7320 incorporates many attributes not typically found in integrated video parts while consuming very low power. The THS7320 video portion includes these features:

- Single-supply 2.6-V to 5-V operation with low total quiescent current of 3.4 mA at 3.3 V
- Enable mode for shutting down the THS7320 video amplifiers to save system power in power-sensitive applications
- DC input configuration with internal 150-mV dc level shifting to prevent sync crushing and saturation effects
- Third-order, 20-MHz (–3-dB) low-pass filter for DAC reconstruction or ADC image rejection; ideal for:
  - NTSC/PAL 480p/576p Y'P'$_B$P'$_R$ or G'B'R' (R'G'B') signals
  - NTSC/PAL/SECAM composite video (CVBS), S-Video Y'/C', 480i/576i Y'P'$_B$P'$_R$, and G'B'R' (R'G'B') signals for oversampled systems
- Internally-fixed gain of 4-V/V (+12-dB) amplifiers that allow for dc-coupling or traditional ac-coupling

OPERATING VOLTAGE

The THS7320 is designed to operate from 2.6 V to 5 V over the –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high-quality, low-temperature coefficient capacitors. The design of the THS7320 allows operation down to 2.5 V, but it is recommended to use at least a 2.7-V supply to ensure that no issues arise with headroom or clipping with 100% color-saturated CVBS signals. If only 75% color saturated CVBS is supported, then the output voltage requirements are reduced to 2 V_{PP} on the output, allowing a 2.6-V supply to be used without issues.

A 0.1-µF capacitor should be placed as close as possible to each power-supply pin to avoid potential ringing or oscillation. Additionally, a large capacitor (such as 4.7 µF to 100 µF) should be placed on the power-supply line to minimize interference with 50-Hz/60-Hz line frequencies.

VIDEO INPUT VOLTAGE

The THS7320 input range allows for an input signal range from –0.06 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 4 V/V (+12 dB) and the internal output level shift of 150 mV (typical), the output is generally the limiting factor for the allowable linear input range. For example, with a 3-V supply, the linear input range is from 0.15 V to 0.75 V. However, because of the gain and level shift, the linear output range limits the allowable linear input range from approximately –0.03 V to 0.65 V.

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VIDEO INPUT OVERVOLTAGE PROTECTION

The THS7320 is built using a very high-speed, complementary, bipolar CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal electrostatic discharge (ESD) protection diodes to the power supplies, as shown in Figure 55.

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

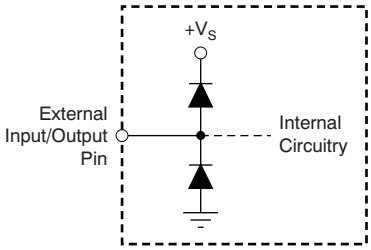


Figure 55. Internal ESD Protection For Video Section

TYPICAL VIDEO CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit using the THS7320 as a video buffer is shown in Figure 56. It shows a DAC or encoder dc-coupled to the input channels of the THS7320 and the output of the THS7320 dc-coupled to the video line. These signals can be NTSC, PAL, or SECAM signals including composite video baseband signal (CVBS), S-Video Y'C', component Y'P'$_B$P'$_R$ video, broadcast G'B'R' video, or computer R'G'B' video signals.

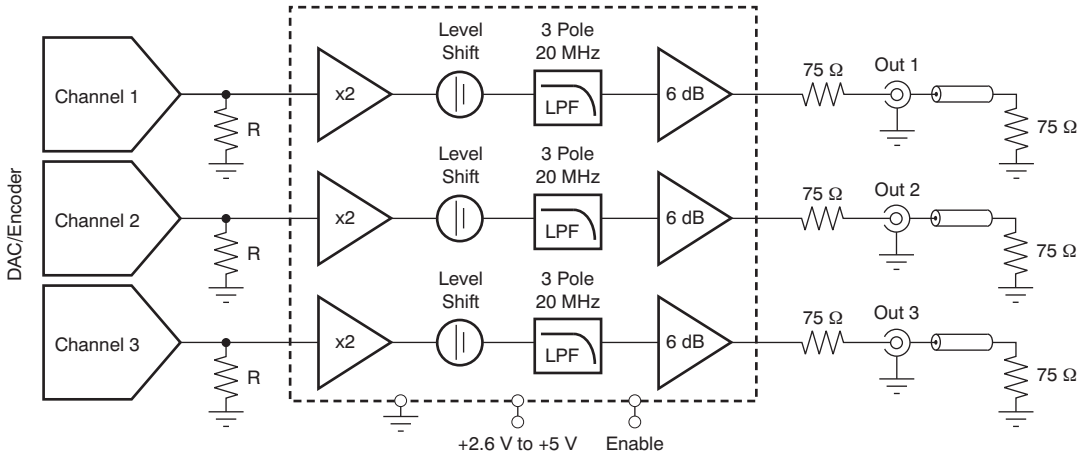


Figure 56. Typical THS7320 Video Section with DC-Coupled Encoder/DAC and DC-Coupled Line Driving

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (*Y*) term. This usage accounts for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, *gamma*, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

This rationale is also used for the chroma (*C'*) term. Chroma is derived from the nonlinear R'G'B' terms and, thus, it is nonlinear. Chrominance (*C*) is derived from linear RGB, giving the difference between chroma (C') and chrominance (C). The color difference signals (P'$_B$/P'$_R$/U'/V') are also referenced in this manner to denote the nonlinear (gamma corrected) signals.

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R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The Society of Motion Picture and Television Engineers (SMPTE) component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This practice is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Because the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

INPUT OPERATION

The THS7320 allows for dc-coupled inputs. Most DACs or video encoders can be dc-connected to the THS7320 with essentially any DAC termination resistance desired for the system. One of the potential drawbacks to dc-coupling is when 0 V is applied to the input from the DAC. Although the input of the THS7320 allows for a 0-V input signal without issue, the output swing of a traditional amplifier cannot yield a 0-V signal that results in possible clipping of the signal. This limitation is true for any single-supply amplifier because of the characteristics of the output transistors. Neither CMOS nor bipolar transistors can achieve 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the video signal receiver uses an automatic gain control (AGC) loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This correction may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits may use the chroma burst amplitude for amplitude control. For this situation, reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals that may not be desirable.

To eliminate saturation or clipping problems, the THS7320 has a 150-mV output level shift feature. This feature takes the input voltage and adds an internal +37.5-mV shift to the input signal. Because of the 12-dB (4-V/V) gain, the resulting output with a 0-V applied input signal is approximately 150 mV. The THS7320 rail-to-rail output stage can create this output level while connected to a typical video load. This configuration ensures the sync signal clipping or saturation does not occur. This shift is constant, regardless of the input signal. The equation for this level shift is $V_{OUT} = (V_{IN} \times 4\ V/V) + 0.15\ V$. For example, if a 0.5-V input is applied, the output is (0.5 V × 4 V/V) + 0.15 V = 2.15 V.

Because the internal gain is fixed at +12 dB (4 V/V), it dictates the allowable linear input voltage range. For example, if the power supply is set to 3 V, the maximum output is approximately 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ([2.8 V – 0.15 V]/4) = 0.66 V. This range is valid for up to the maximum recommended 5-V power supply that allows approximately a ([4.8 V – 0.15 V]/4) = 1.16-V input range while avoiding clipping on the output.

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The input impedance of the THS7320 is dictated by the internal high-impedance gain of 2 V/V initial amplifier, as shown in Figure 57. This buffer has a very high 2.4-MΩ || 2-pF input impedance that is effectively transparent to the source with no interactions. Unlike other products where the filter elements are tied directly to the input pin without buffering, there are no filter performance changes or interaction with the DAC termination resistance. Note that the internal voltage shift does not appear at the input pin; it only shows at the output pin.

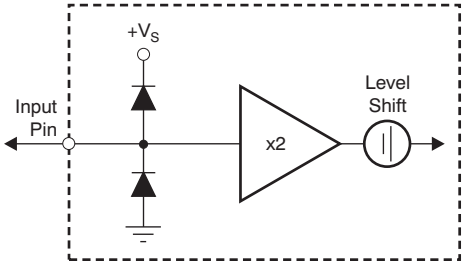


Figure 57. Equivalent Video Section DC Input Mode Circuit

While ac-coupling with dc-biasing using external resistor dividers can be done, it is generally not recommended because of the large resistor values required. These large resistor values coupled with the input bias current of the THS7320 input can cause a significant voltage shift to appear on the input. If ac-coupling is necessary for a system, several elements must be taken into account for a proper design: the high-pass corner frequency (typically desired to be approximately 2.5 Hz); the size of the input capacitor value; the parallel input resistance of the voltage divider; and the input bias current. Contact Texas Instruments for design support if ac-coupling is necessary in the design.

DC-COUPLED OUTPUT

The THS7320 video section incorporates a rail-to-rail output stage that can drive the line directly without the need for large ac-coupling capacitors. This design offers the best line tilt and field tilt (droop) performance because no ac-coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt as a result of the input ac-coupling continues to be seen on the output, regardless of the output coupling. The 70-mA output current drive capability of the THS7320 is designed to drive the video line while keeping the output dynamic range as wide as possible.

One concern of dc-coupling, however, arises if the line is terminated to ground. If an ac-bias input configuration is used or if a dc reference from the DAC is applied, such as S-Video C'/component P'_B/or component P'_R signals, the output of the THS7320 then has a dc bias on the output, such as 1 V. This configuration allows a dc current path to flow, such as 1 V/150 Ω = 6.67 mA. The result of this configuration is a slightly decreased high output voltage swing and an increase in power dissipation of the THS7320. While the THS7320 was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer. Using a 5-V supply, this configuration can result in an additional power dissipation of (5 V – 1 V) × 6.67 mA = 26.7 mW per channel. With a 3.3-V supply, this dissipation reduces to 15.3 mW per channel. The overall low quiescent current of the THS7320 design minimizes potential thermal issues even when used at high ambient temperatures, but power and thermal analysis should always be examined in any system to ensure that no issues arise. Be sure to use RMS power and not instantaneous power when evaluating the thermal performance.

Note that the THS7320 can drive the line with dc-coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output (typically 75 Ω). This requirement helps isolate capacitive loading effects from the THS7320 output. Failure to properly isolate capacitive loads may result in ringing or oscillation. The stray capacitance appearing directly at the THS7320 output pins should be kept below 18 pF. One method to ensure this condition is valid is to verify that the 75-Ω source resistor is placed next to each THS7320 output pin.

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There are many reasons dc-coupling is desirable, including reduced costs, PCB area reduction, and no line tilt or field tilt. A common question is whether or not there are any drawbacks to using dc-coupling. There are a few potential issues that must be examined, such as the dc current bias as discussed above. Another potential risk is whether this configuration meets industry standards. EIA-770 stipulates that the *back porch* shall be 0 V ± 1 V as measured at the receiver. With a double-terminated load system, this requirement implies a 0-V ± 2-V level at the video amplifier output. The THS7320 can easily meet this requirement without issue. However, in Japan, the EIAJ CP-1203 specification stipulates a 0-V ± 0.1-V level with no signal. This requirement can be met with the THS7320 in disable mode, but while active it cannot meet this specification without output ac-coupling.

AC-COUPLED OUTPUT

A very common method of coupling the video signal to the line is with a large capacitor. This capacitor is typically between 220 µF and 1000 µF, although 470 µF is very typical. The value of this capacitor must be large enough to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document. AC-coupling is performed for several reasons, but the most common is to ensure full interoperability with the receiving video system. This approach ensures that regardless of the reference dc voltage used on the transmitting side, the receiving side re-establishes the dc reference voltage to its own requirements.

In the same way as the dc output mode of operation discussed previously, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. This 75-Ω series resistor should be placed next to the THS7320 output to minimize capacitive loading effects.

Because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitor. These large value capacitors are generally aluminum electrolytic. It is well-known that these capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-µF to 0.01-µF capacitors help pass these high-frequency signals (greater than 1 MHz) with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in an S-Video system is not required to perform at as low (or as high) a frequency as the luma channels. Thus, the capacitor values of the chroma line(s) can be smaller, such as 0.1 µF.

Figure 58 shows a typical configuration where the input is dc-coupled and the output is also ac-coupled. AC-coupled inputs are generally required when current-sink DACs are used or the input is connected to an unknown source, such as when the THS7320 is used as an input device.

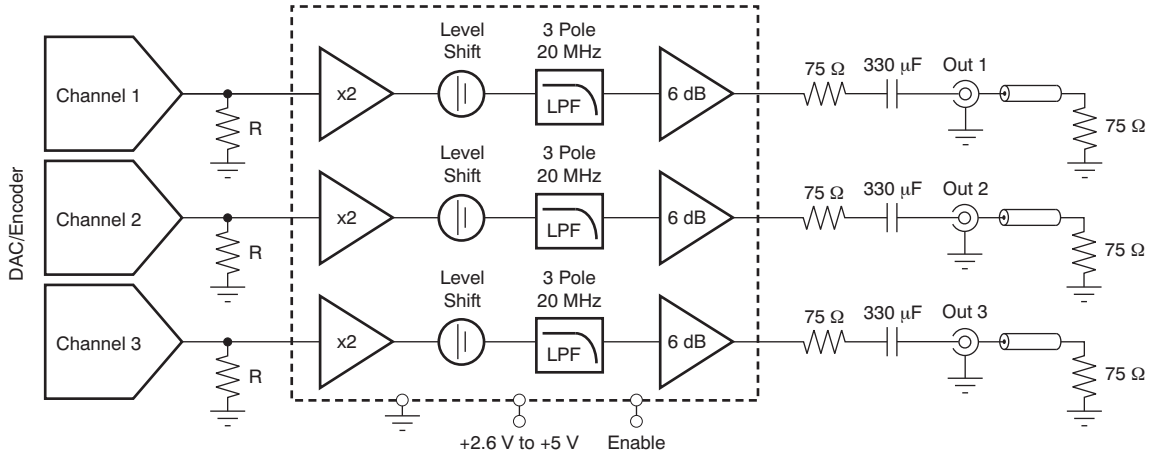


Figure 58. Typical DC Input System Driving AC-Coupled Video Lines

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LOW-PASS FILTER

Each channel of the THS7320 video section incorporates a third-order, low-pass filter. These video reconstruction filters minimize DAC images from being passed on to the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems as a result of aliasing of the ADC in the receiver. Another benefit of the filter is to smooth out aberrations in the signal that DACs typically have associated with the digital stepping of the signal. This benefit helps with picture quality and ensures that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The concern with the Butterworth characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or Chebyshev, is not recommended for video applications because of the very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. Considering this group delay with the fact that video can go from a white pixel to a black pixel over and over again, it is easy to see that ringing can occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is an acceptable compromise for both attenuation and group delay.

The THS7320 filters have a nominal corner (–3-dB) frequency at 20 MHz and a –1-dB passband typically at 17 MHz. This 20-MHz filter is ideal for enhanced definition (ED) NTSC or PAL 480p/576p Y'P'$_B$P'$_R$ or G'B'R'/R'G'B' signals. For oversampled systems, the THS7320 works well for passing standard definition (SD) NTSC, PAL, or SECAM composite video (CVBS), S-Video signals (Y'C'), 480i/576i Y'P'$_B$P'$_R$, Y'U'V', broadcast G'B'R' signals, and R'G'B' video signals. The 20-MHz, –3-dB corner frequency was designed to achieve 27-dB of attenuation at 54 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as a result of aliasing effects of an ADC found in a receiver. Another specification ensured for the THS7320 is attenuation at 43 MHz. This frequency is derived from the fact that the ED Y' signal has an 11-MHz bandwidth. Following standard sampling theory, this means that the second Nyquist zone image starts at 54 MHz – 11 MHz = 43 MHz.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 54 MHz for traditional ED DACs); they continue around the sampling frequency harmonics of 2 × f_S, 3 × f_S, 4 × f_S, and so on (that is, 108 MHz, 162 MHz, 216 MHz, etc.). Because of these multiple images, an ADC can fold down into the baseband signal, meaning that the low-pass filter must also eliminate these higher-order images. The THS7320 filters are designed to attenuate all of these higher frequencies without *bounce* effect that some filters can allow.

The filter frequencies were chosen to account for process variations in the THS7320. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering is sufficient to meet the system demands. Thus, the recommendations for the filter frequencies was not arbitrarily selected and is a good compromise that should meet the demands of most systems.

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BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system (such as the THS7320) over a passive system are PCB area and filter variations. The ultra-small MicrostarCSP 9-ball package is much smaller over a passive RLC network, especially a three-pole passive network for three channels. Additionally, consider that inductors have at best ±10% tolerances (normally, ±15% to ±20% is common) and capacitors typically have ±10% tolerances. A Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q-factor (or peaking), and channel-to-channel delay have wide variations. These variances can lead to potential performance and quality issues in mass-production environments. The THS7320 solves most of these problems with the corner frequency being essentially the only variable.

Another concern about passive filters is the use of inductors. Inductors are magnetic components, and are therefore susceptible to electromagnetic coupling/interference (EMC/EMI). Some common coupling can occur because of other video channels nearby using inductors for filtering, or it can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation and can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature change. To minimize temperature effects, the THS7320 uses low-temperature coefficient resistors and high-quality, low-temperature coefficient capacitors found in the BiCom3X process. These filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This approach maintains a low channel-to-channel time delay that is required for proper video signal performance.

Another benefit of the THS7320 over a passive RLC filter are the input and output impedances. With a passive filter, the input impedance presented to the DAC varies significantly, from 35 Ω to over 1.5 kΩ, and may cause voltage variations over frequency. The THS7320 input impedance is 2.4 MΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impact the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7320.

On the output side of the filter, a passive filter again has a large impedance variation over frequency. The EIA770 specifications require the return loss to be at least 25 dB over the video frequency range of use. For a video system, this requirement implies that the source impedance (which includes the source, series resistor, and the filter) must be better than 75 Ω, +9 Ω/–8 Ω. The THS7320 is an operational amplifier that approximates an ideal voltage source, which is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss meeting EIA specifications, this output impedance must maintain a 75-Ω impedance. A wide impedance variation of a passive filter cannot ensure this level of performance. On the other hand, the THS7320 has approximately 1.4 Ω of output impedance, or a return loss of 41 dB, at 11 MHz. Thus, the system is matched significantly better with a THS7320 compared to a passive filter.

One final benefit of the THS7320 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load: the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This requirement forces the DAC to drive at least 1.25 V_P (100% saturation CVBS)/37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when three channels are being driven.

Using the THS7320 with a high input impedance can reduce DAC power dissipation significantly. This outcome is possible because the resistance that the DAC drives can be substantially increased. It is common to set this resistance in a DAC by a current-setting resistor on the DAC itself. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving significant amounts of power. For example, a 3.3-V, three-channel DAC dissipates 330 mW alone for the steering current capability (three channels × 33.3 mA × 3.3 V) if it must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 41 mW (three channels × 4.16 mA × 3.3 V), or over eight times lower power. For overall system power, this scenario must also account for the THS7320 power. The THS7320 only consumes 3.4-mA total quiescent current. The quiescent power added is then 3.3 V × 3.4 mA = 11.2 mW. The total system power is then 41 mW + 11 mW = 52 mW, or a factor of six times lower power compared to the DAC driving the line directly. Saving power by adding the THS7320 in a system is easy to see and accomplish, not to mention that it incorporates the added benefit of a three-pole filter on each channel.

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EVALUATION MODULE

To evaluate the THS7320, an evaluation module (EVM) is available. The EVM allows dc-coupled input and output configurations. Inputs and outputs include BNC connectors commonly found in video systems along with 75-Ω effective input termination resistors, 75-Ω series source termination resistors, and 75-Ω characteristic impedance traces. This EVM is designed to be used with a single supply from 2.6 V up to 5 V.

The EVM input configuration sets all channels for dc input coupling. The input signal must be within 0 V to approximately 0.75 V for proper operation. Failure to be within this range saturates and/or clips the output signal. Refer to the *Application Information* section for further information.

The THS7320 incorporates an easy method to configure the enable mode. JP1 controls the enable feature. Connecting JP1 to GND applies 0 V to the enable pin and the THS7320 is placed into shutdown mode consuming nominally 0.15 µA of quiescent current. Moving JP1 to $+V_S$ causes the THS7320 to be in normal operation mode where the quiescent current should be nominally 3.4 mA for the entire EVM. This quiescent current is with no load or no signal applied on the input. Adding a load or input signal causes the quiescent current to vary accordingly.

An example procedure to confirm proper device operation with standard lab equipment is described in the following sections.

REQUIRED EQUIPMENT

- One dc power supply: +3.0 V, 50-mA output (minimum) is recommended
- One dc current meter: resolution to 1 mA, capable of maximum current the dc power supply can supply
- Function or arbitrary waveform generator
- Oscilloscope: 50-MHz bandwidth (minimum) is recommended
- Banana-to-banana patch cords
- BNC test cables

BASIC SETUP

1. Set the dc power supply to +3.0 V. Set the current limit on the dc power supply to 50 mA.
2. Connect the positive (+) terminal of the power supply to the positive (+) terminal of the current meter.
3. Connect the negative (–) terminal of the current meter to the V_{S+} terminal of the EVM (J7).
4. Connect the common ground terminal of the power supply to the ground (GND) terminal on the EVM (J8).
5. Connect the output of the waveform generator to the channel 1 input on the EVM (J1)
6. Connect the probe ground to the GND of the EVM.

TESTING THE EVM

The EVM can be tested by following these steps:

1. Enable the 3.0-V_{DC} power supply.
2. Verify that the current meter is reading nominally 3.5 mA (2.7 mA to 4.7 mA, minimum and maximum).
3. Set the function generator such that a 1-MHz, 0.5-V_{PP} sine wave (with an 0.40-V_{DC} offset) appears on the THS7320 input pin. The function generator ac and dc levels may have to be adjusted to ensure the proper voltage appears on the THS7320 input pins because most function generators have a 50-Ω source impedance and the THS7320 incorporates a double 37.4-Ω resistor termination divider scheme for a total 75-Ω termination.
4. Probe the device side of R12, which is connected to the THS7320 channel 1 output pin.
5. Verify that the oscilloscope displays the THS7320 channel 1 output voltage amplitude as 2.0 V_{PP} ±0.1 V with a nominal 1.75-V_{DC} offset.
6. Repeat steps 3 through 5 for channels 2 and 3.
7. When confirmed, turn off the function generator and power supply.
8. Note that if video equipment is used with the THS7320EVM, the proper input and output 75-Ω terminations already exist on the EVM along with the proper input voltage divider. This functionality makes the EVM very easy to test video signals with no modifications to the EVM.

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Figure 59 shows the EVM schematic. Figure 60 through Figure 63 illustrate the layers of the EVM PCB, incorporating standard high-speed layout practices. Table 5 lists the bill of materials as the board comes supplied from Texas Instruments.

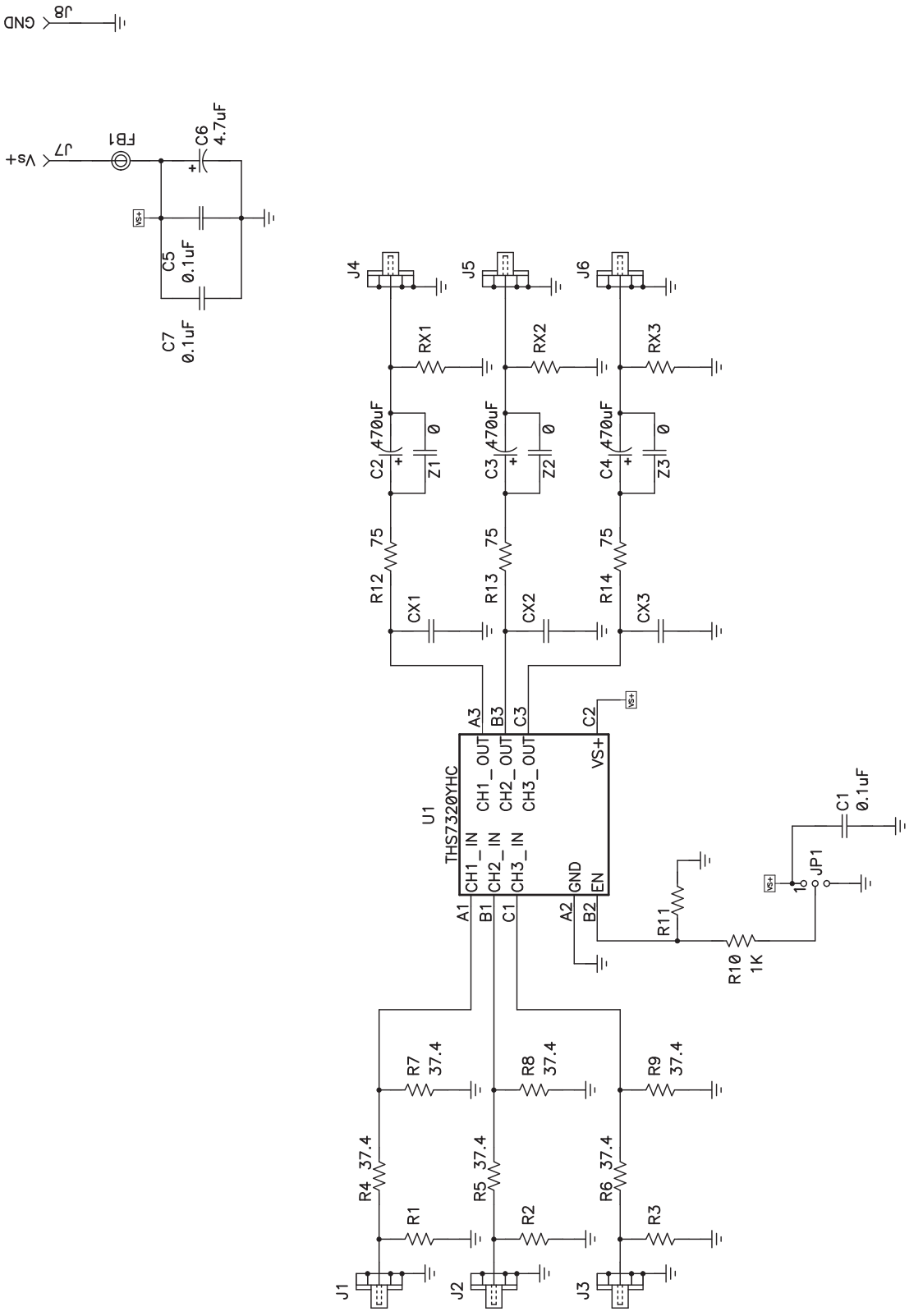


Figure 59. THS7320 EVM Schematic

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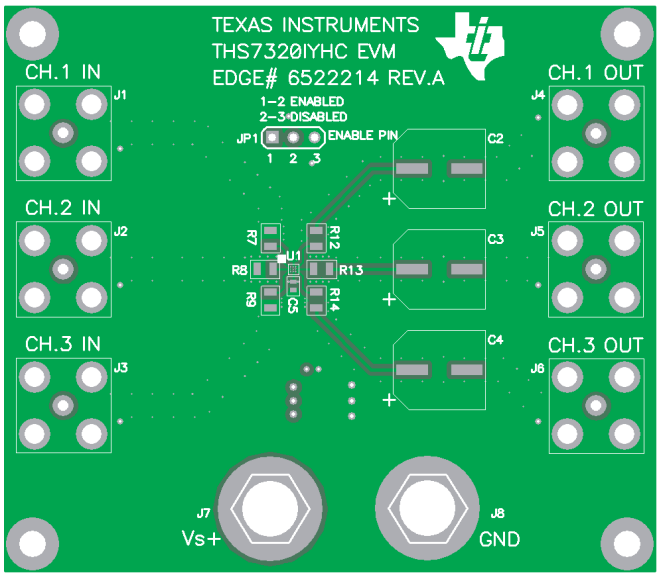


Figure 60. THS7320 EVM PCB Top Layer

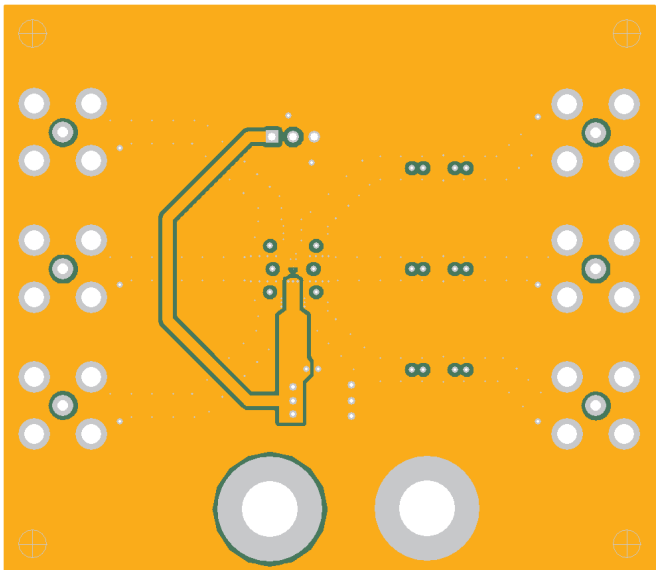


Figure 61. THS7320 EVM PCB Layer 2

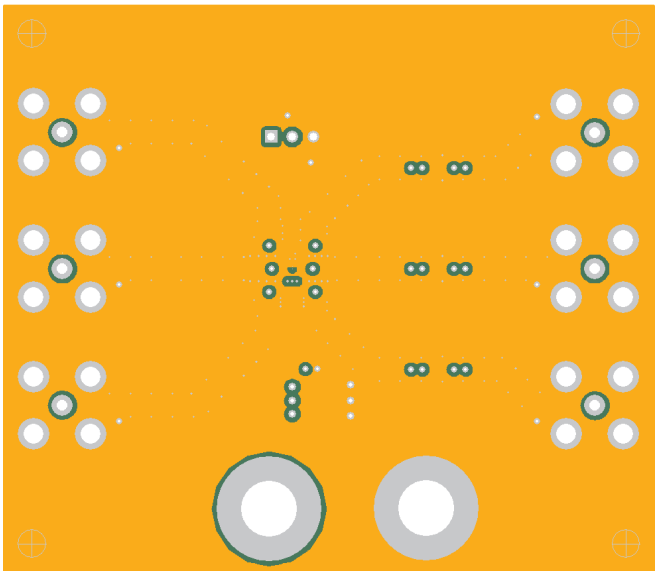


Figure 62. THS7320 EVM PCB Layer 3

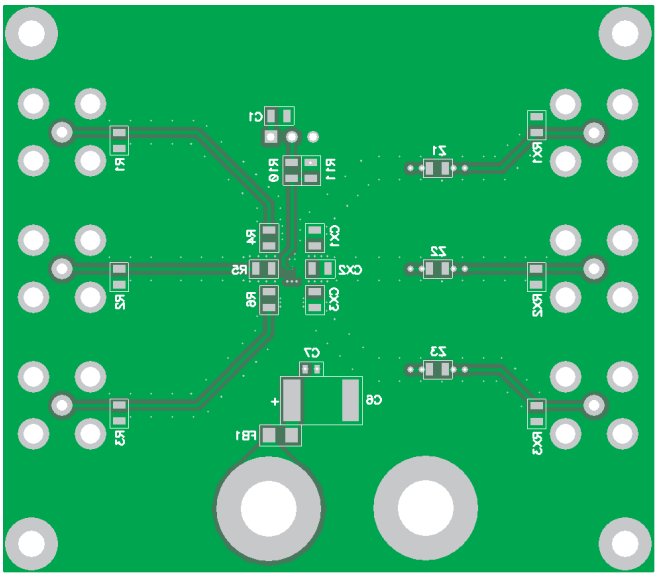


Figure 63. THS7320 EVM PCB Bottom Layer

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THS7320IYHC EVM Bill of Materials

Table 5. THS7320 EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1	1	Bead, ferrite, 2.5 A, 330 Ω	0805	(TDK) MPZ2012S331A	(Digi-Key) 445-1569-1-ND
2	C6	1	Capacitor, 4.7 µF, tantalum, 35V, 10%, low ESR	C	(AVX) TPSC475K035R0600	(Digi-Key) 478-1772-1-ND
3	CX1-CX3	3	Open	0805	—	—
4	C5	1	Capacitor, 0.1 µF, ceramic, 16V, X7R	0402	(TDK) C1005X7R1C104K	(Digi-Key) 445-4952-1-ND
5	C7	1	Capacitor, 0.1 µF, ceramic, 16V, X7R	0603	(AVX) 0603YC104KAT2A	(Digi-Key) 478-1239-1-ND
6	C1	1	Capacitor, 0.1 µF, ceramic, 50V, X7R	0805	(AVX) 08055C104KAT2A	(Digi-Key) 478-1395-1-ND
7	C2-C4	3	Capacitor, aluminum, 470 µF, 10V, 20%	F	(Panasonic) EEE-FP1A471AP	(Digi-Key) PCE4526CT-ND
8	R1-R3, R11, RX1-RX3	7	Open	0805	—	—
9	Z1-Z3	3	Resistor, 0 Ω, 1/8W	0805	(ROHM) MCR10EZPJ000	(Digi-Key) RHM0.0ARCT-ND
10	R4-R9	6	Resistor, 37.4 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF37R4	(Digi-Key) RHM37.4CCT-ND
11	R12-R14	3	Resistor, 75 Ω, 1/8W, 1%	0805	(ROHM) MCR10EZHF75.0	(Digi-Key) RHM75.0CCT-ND
12	R10	1	Resistor, 1 kΩ, 1/8W, 1%	0805	(ROHM) MCR10EZHF1001	(Digi-Key) RHM1.00KCCT-ND
13	J7, J8	2	Jack, banana receptance, 0.25" dia. hole	—	(SPC) 15459	(Newark) 79K5034
14	J1-J6	6	Connector, BNC, jack, 75 Ω	—	(Amphenol) 31-5329-72RFX	(Newark) 93F7554
15	JP1	1	Header, 0.1" CTRS, 0.025" sq. pins	3 POS.	(Sullins) PBC36SAAN	(Digi-Key) S1011E-36-ND
16	JP1	1	Shunts	—	(Sullins) SSC02SYAN	(Digi-Key) S9002-ND
17	U1	1	IC, THS7320	YHC	(TI) THS7320IYHC	—
18	—	4	Standoff, 4-40 HEX, 0.625" length	—	(Keystone) 1808	(Digi-Key) 1808K-ND
19	—	4	Screw, Phillips, 4-40, 0.250"	—	PMSSS 440 0025 PH	(Digi-Key) H703-ND
20	—	1	Board, printed circuit	—	EDGE # 6522214 REV.A	—

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2012) to Revision B **Page**

- Added the *Required Equipment*, *Basic Setup*, and *Testing the EVM* sections 27

Changes from Original (July 2011) to Revision A **Page**

- Added THS7320IYHCT row to Package/Ordering Information table 2

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.6 V to 5.5 V and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
THS7320IYHCR	ACTIVE	DSBGA	YHC	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QJK	Samples
THS7320IYHCT	ACTIVE	DSBGA	YHC	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QJK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

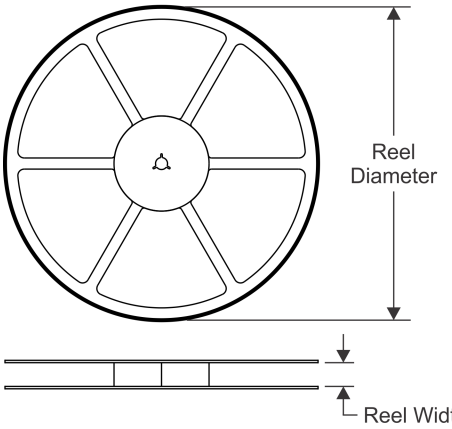
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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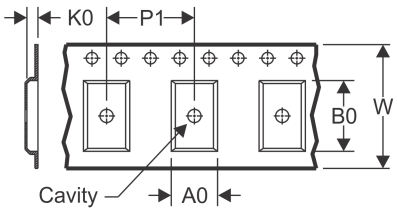
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

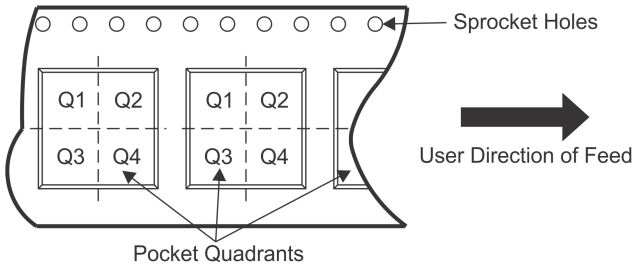


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

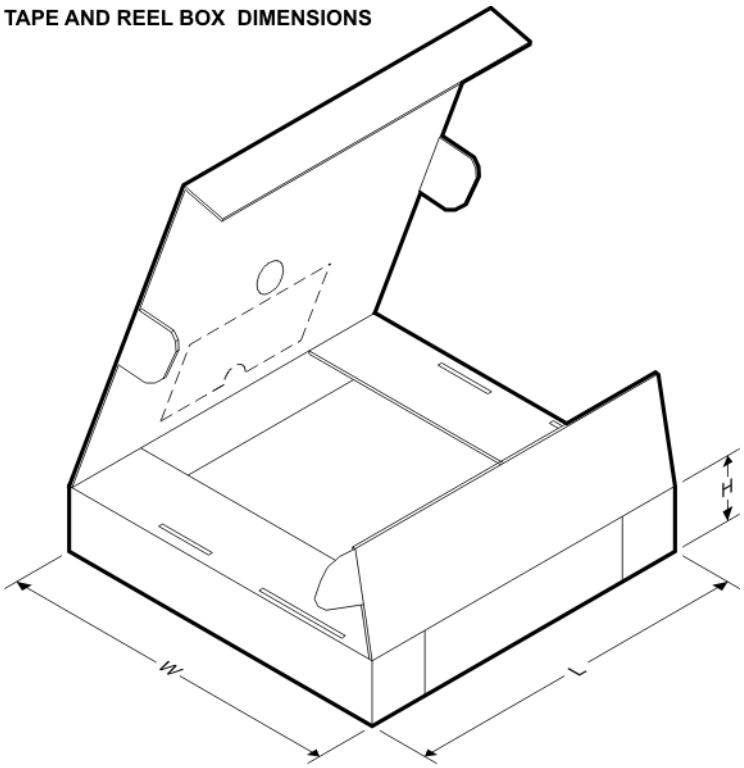
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7320IYHCT	DSBGA	YHC	9	250	180.0	8.4	1.06	1.06	0.56	4.0	8.0	Q1

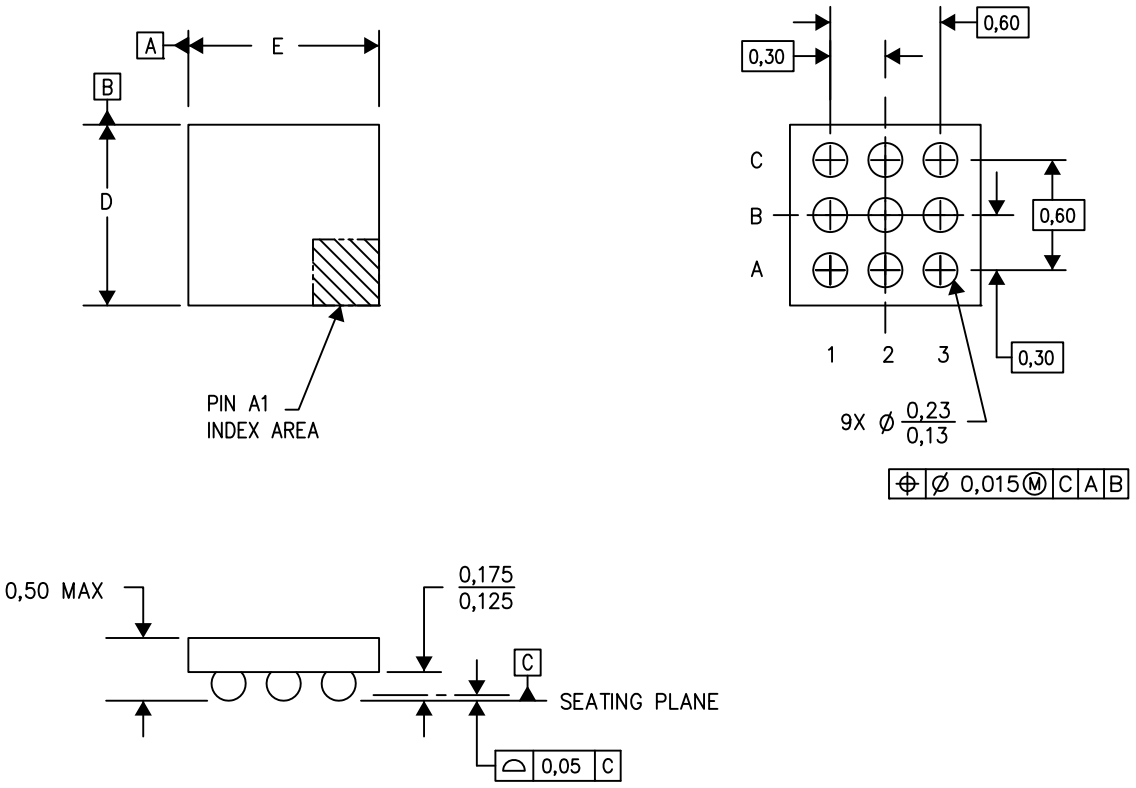
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7320IYHCT	DSBGA	YHC	9	250	182.0	182.0	20.0

YHC (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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