THS6226A 门控 H 类，双端口 VDSL2 线路驱动器

1 特性

- 数字式可调节静态电流：9.4mA 至 24.8mA
- 偏置电流步长：1.0mA
- 独立的升压和主线路驱动器禁用
- 低功率线路端接模式
- 完全电容器再充电：200µs
- 低输出电压噪声密度：6.5nV/√Hz 输入引入电压噪声
- 低多音频功率比 (MTPR) 失真：70dB 加上 +19.8dBm G.993.2 — 传输模式 8b
- -83dBc HD3（1MHz，60Ω 差分）
- 高输出电流：（可向 60Ω 负载输送 383mA 的电流）
- 宽输出摆幅：40V_{PP}（+12V，100Ω 差分负载和一个 1:1.4 变压器）
- 高带宽：97MHz
- 端口至端口隔离度：1MHz 时大于 90dB
- 电源抑制比 (PSRR)：在 1MHz 频率下提供了 70dB 的良好隔离

2 应用范围

- 非常适合于所有的 VDSL2 传输模式
- 与 ADSL，ADSL2+ 和 ADSL2++ 系统向后兼容

3 说明

THS6226A 是一款双端口，H 类，电流反馈架构，差分线路驱动器放大器系统，此系统非常适合于 xDSL 系统。 该器件旨在应用于超高位速率数字用户线路 2 (VDSL2) 线路驱动器系统，此类系统可启用本地 DTM 信号，同时用良好线性支持高于 20.5dBm 的线路功率（在高达 8.5MHz 的频率条件下），从而支持 G.993.2 VDSL2 8b 传输模式。 另外，此器件还拥有足以支持 14.5dBm 线路功率（在高达 30MHz 的频率下）的中心局传输的高速度。

此器件的独特架构可实现极小的静态电流，同时仍然实现超高线性度。 在全偏置条件和 1MHz 频率下，差分失真为 -91dBc，并在 5MHz 频率下减少为仅有 -75dBc。 对于并不需要放大器全部性能的线路长度，放大器的多种固定偏置设定值可提升节能效果。 为了在所有的系统配置中实现更大的灵活性及节能幅度，以 0.1mA 的偏置电流步长对静态电流进行数字化调节，调节范围从 7.67mA 至 23mA。 对于那些希望在不传输时节省更多电能的系统，此器件可在其线路端接模式中使用，以保持阻抗匹配。

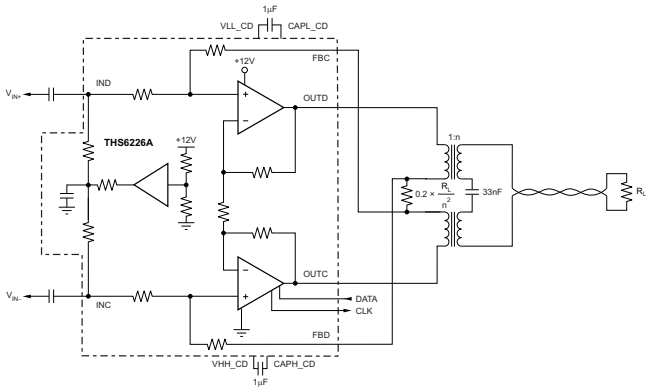
12V 电源上的宽输出摆幅与出色的电流驱动能力相结合，可实现宽动态余量，从而将失真保持在尽可能低的水平。 此器件采用超薄四方扁平无引线 (VQFN)-32 PowerPAD™ 封装。

器件信息(1)

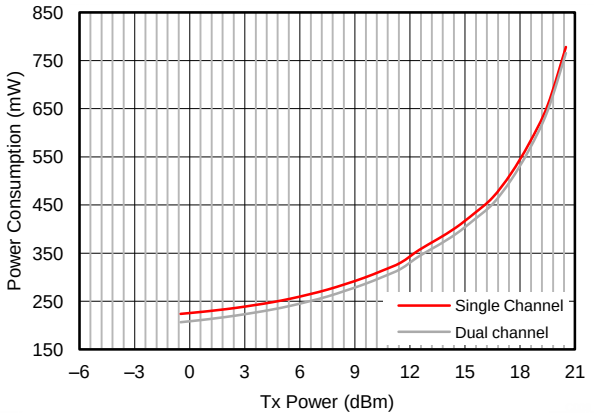
产品型号	封装	封装尺寸（标称值）
THS6226A	VQFN (32)	5.00mm x 5.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

利用 THS6226A 的一个端口的典型 VDSL2 线路驱动器电路



功耗与 Tx 间的关系



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

目录

1 特性 1
2 应用范围 1
3 说明 1
4 修订历史记录 2
5 **Pin Configuration and Functions** 3
6 **Specifications** 5
6.1 Absolute Maximum Ratings 5
6.2 Handling Ratings 5
6.3 Recommended Operating Conditions 6
6.4 Thermal Information 6
6.5 Electrical Characteristics: V_S = +12 V 6
6.6 Timing Characteristics 8
6.7 Typical Characteristics 9
7 **Detailed Description** 14
7.1 Overview 14
7.2 Functional Block Diagram 14
7.3 Feature Description 15
7.4 Device Functional Modes 15
7.5 Programming 16
8 **Applications and Implementation** 19
8.1 Application Information 19
8.2 Typical Application 19
8.3 Initialization Set Up 21
9 **Power Supply Recommendations** 21
10 **Layout** 22
10.1 Layout Guidelines 22
10.2 Layout Example 23
11 器件和文档支持 24
11.1 文档支持 24
11.2 Trademarks 24
11.3 Electrostatic Discharge Caution 24
11.4 Glossary 24
12 机械封装和可订购信息 24

4 修订历史记录

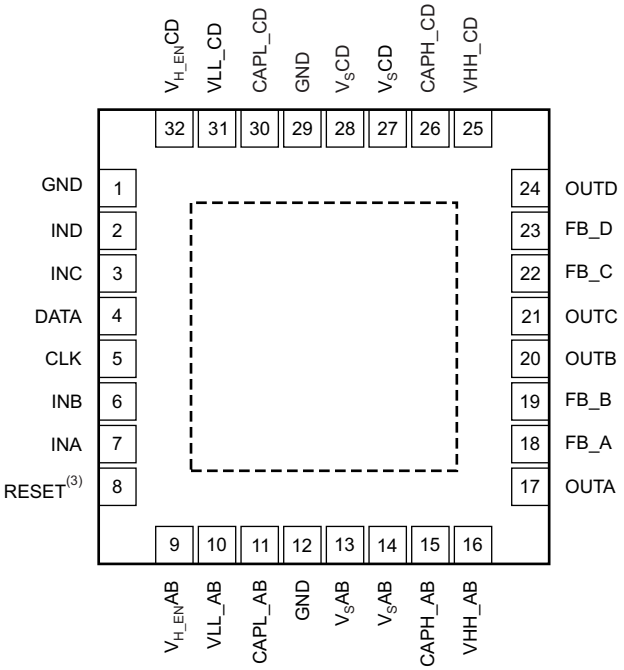
Changes from Original (April 2014) to Revision A **Page**

- Changed HBM parameter in Handling Ratings table 5

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5 Pin Configuration and Functions

RHB Package(1)(2)
VQFN-32
(Top View)



(1) The PowerPAD is electrically isolated from all other pins and can be connected to any potential voltage range from V_{S-} to V_{S+}. Typically, the PowerPAD is connected to the GND plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

(2) The device defaults to the disabled mode at power-up.

(3) Default is GND (internal pull-down resistor).

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Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 12, 29	GND	—	Analog ground
2	IND	I	Input D of amplifier CD
3	INC	I	Input C of amplifier CD
4	DATA	I	Serial interface data pin
5	CLK	I	Serial interface CLK pin
6	INB	I	Input B of amplifier AB
7	INA	I	Input A of amplifier AB
8	RESET	I	Reset the internal register to 00h (startup conditions, state machine may require resetting)
9	V_{H_EN}AB	I	Class H mode control pin for amplifier AB
10	VLL_AB	—	Amplifier AB low pump supply
11	CAPL_AB	—	Amplifier AB negative voltage pump capacitor pin
13, 14	V_SAB	—	Amplifier AB supply voltage
15	CAPH_AB	—	Amplifier AB positive voltage pump capacitor pin
16	VHH_AB	—	Amplifier AB high pump supply
17	OUTA	O	Output A of amplifier AB
18	FB_A	I	Feedback for active output impedance of amplifier AB
19	FB_B	I	Feedback for active output impedance of amplifier AB
20	OUTB	O	Output B of amplifier AB
21	OUTC	O	Output C of amplifier CD
22	FB_C	I	Feedback for active output impedance of amplifier CD
23	FB_D	I	Feedback for active output impedance of amplifier CD
24	OUTD	O	Output D of amplifier CD
25	VHH_CD	—	Amplifier CD high pump supply
26	CAPH_CD	—	Amplifier CD positive voltage pump capacitor pin
27, 28	V_SCD	—	Amplifier CD supply voltage
30	CAPL_CD	—	Amplifier CD negative voltage pump capacitor pin
31	VLL_CD	—	Amplifier CD low pump supply
32	V_{H_EN}CD	I	Class H mode control pin for amplifier CD
PowerPAD		—	The PowerPAD must be connected to any internal PCB ground plane using multiple vias for good thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, GND to V_{S+}	Class AB only		16.5	V
	Class H only		12.8	V
Input voltage, V_I			15	V
Output current, I_O	Static dc(2)		±100	mA
Continuous power dissipation		See Thermal Information table		
Temperature	Maximum junction, any condition, T_J(3)		150	°C
	Maximum junction, continuous operation, long-term reliability, T_J(4)		130	°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The device incorporates a PowerPAD on the underside of the chip, which functions as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which could permanently damage the device. See the technical brief *PowerPAD™ Thermally Enhanced Package* (SLMA002) for more information about using the PowerPAD thermally-enhanced package. Under high-frequency ac operation (> 10 kHz), the short-term output current capability is much greater than the continuous dc output current rating. This short-term output current rating is roughly 8.5 times the dc capability, or approximately ±850 mA.
(3) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(4) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Supply and ground pins with respect to PowerPad: GND (pins 1, 12, 29), V_SAB (pins 13, 14), V_SCD (pins 27, 28)	–1.5	1.5	kV
			All other pins	–2	2	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		–500	500	V

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Power-supply voltage range	Class H	10		12.6	V
	Class AB	10		15	V
Operating junction temperature		–40		130	°C

6.4 Thermal Information

THERMAL METRIC(1)		THS6226A RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.0	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	6.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_S = +12 V

At T_A = 25°C, R_{MATCH} = 10.2 Ω, transformer turn ratio 1:1.4, R_L = 100-Ω differential at transformer output, full bias mode, and active impedance circuit configuration, unless otherwise noted. Each port is tested independently.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
	Small-signal bandwidth, –3 dB	V_O = 2 V_{PP}, differential at OUTCD and OUTAB, gain = 19 V/V		97		MHz	C
	0.1-dB bandwidth flatness	V_O = 2 V_{PP}		30		MHz	C
	Large-signal bandwidth	V_O = 7.5 V_{PP}		80		MHz	C
SR	Slew rate (10% to 90% level)	V_O = 15-V step, differential		1750		V/µs	C
	Rise-and-fall time	V_O = 2 V_{PP}		3.6		ns	C
HD2	Second-harmonic distortion	Full bias, f = 1 MHz, V_O = 2 V_{PP}, R_L = 60-Ω differential		–87		dBc	C
		Full bias, f = 5 MHz, V_O = 2 V_{PP}, R_L = 60-Ω differential		–73		dBc	C
HD3	Third-harmonic distortion	Full bias, f = 1 MHz, V_O = 2 V_{PP}, R_L = 60-Ω differential		–83		dBc	C
		Full bias, f = 5 MHz, V_O = 2 V_{PP}, R_L = 60-Ω differential		–71		dBc	C
	Differential input voltage noise	f = 1 MHz, input-referred		6.5		nV/√Hz	C
DC PERFORMANCE							
	Differential gain	Closed-loop configuration		19		V/V	C
	Differential gain error(2)	T_A = 25°C			±8%		A
V_{IO}	Input offset voltage	T_A = 25°C		±1	±10	mV	A
		T_A = –40°C to 85°C			±11	mV	B
	Input offset voltage drift				15	µV/°C	B
	Input offset voltage matching	Channels 1 to 2 and 3 to 4 only, T_A = 25°C		±1	±10	mV	A
INPUT CHARACTERISTICS							
	Noninverting input resistance			2 || 2		kΩ || pF	C
	Input bias voltage	T_A = 25°C	5.8	6	6.2	V	A

(1) Test levels: **(A)** 100% tested at 25°C. Overtemperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Negative feedback loop only.

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Electrical Characteristics: V_S = +12 V (continued)

At T_A = 25°C, R_{MATCH} = 10.2 Ω, transformer turn ratio 1:1.4, R_L = 100-Ω differential at transformer output, full bias mode, and active impedance circuit configuration, unless otherwise noted. Each port is tested independently.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
OUTPUT CHARACTERISTICS								
	Class H output	Voltage swing	R_L = 60-Ω differential, class H operation(3)(4), each output, T_A = 25°C	16	17.5		V	A
				–4	–5.5		V	A
			T_A = –40°C to 85°C(3)(4)	15.7			V	B
				–3.7			V	B
		Current (sourcing, sinking)	R_L = 60-Ω differential, class H operation, T_A = 25°C	±333	±383		mA	A
			T_A = –40°C to 85°C	±323			mA	B
	Class AB output	Voltage swing	R_L = 60-Ω differential, normal operation(3), each output, T_A = 25°C	9.9	10.1		V	A
				2.1	1.9		V	A
			T_A = –40°C to 85°C(3)	9.8			V	B
				2.2			V	B
		Current (sourcing, sinking)	R_L = 60-Ω differential, normal operation, T_A = 25°C	±130	±137		mA	A
			T_A = –40°C to 85°C	±126			mA	B
	Short-circuit output current				1		A	C
z_o	Output impedance		f = 1 MHz, differential		25		Ω	C
	Crosstalk		f = 1 MHz, V_{OUT} = 2 V_{PP}, port 1 to port 2		–90		dB	C
POWER SUPPLY								
	Maximum operating voltage		Class AB, T_A = 25°C	10	12	15	V	A
			T_A = –40°C to 85°C	10		15	V	B
			Class H	10	12	12.6	V	B
			T_A = –40°C to 85°C	10		12.6	V	B
I_Q	Quiescent current (I_{S+})		Per port, bias 15, class H enable (power supplies connected together), T_A = 25°C	23.4	24.6	25.8	mA	A
			T_A = –40°C to 85°C	22.9		26.1	mA	B
			Per port, bias 15, class H disable (power supplies connected together), T_A = 25°C	22.8	24.0	25.2	mA	A
			T_A = –40°C to 85°C	22.3		25.7	mA	B
			Bias current step		1		mA	C
			Per port, bias 0, class H disable (power supplies connected together), T_A = 25°C	8.5	9.7	10.9	mA	A
			T_A = –40°C to 85°C	8.0		11.4	mA	B
			Per port, line termination mode (B9 = B8 = B7 = B6 = 0) (power supplies connected together)		7.0		mA	C
			Both ports, main amplifiers and class H disable (B9 = B8 = B7 = B6 = 0)		1.9	2.4	mA	A
			T_A = –40°C to 85°C			2.5	mA	B
PSRR	Power-supply rejection ratio		Differential, from 12 V, GND, T_A = 25°C	60	70		dB	A
			T_A = –40°C to 85°C	58			dB	B

(3) Measured at the amplifier outputs (pins 17, 20, 21, and 24).
(4) Capacitor fully charged, no droop.

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Electrical Characteristics: V_S = +12 V (continued)

At T_A = 25°C, R_{MATCH} = 10.2 Ω, transformer turn ratio 1:1.4, R_L = 100-Ω differential at transformer output, full bias mode, and active impedance circuit configuration, unless otherwise noted. Each port is tested independently.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
LOGIC							
Logic pin	Logic threshold	Logic 1, with respect to GND(5)	1.9			V	C
		Logic 0, with respect to GND(5)			0.8	V	C
	Input Bias current	Logic X = 0.5 V (logic 0), T_A = 25°C		10	25	µA	A
		T_A = –40°C to 85°C			30	µA	B
		Logic X = 3.3 V (logic 1), T_A = 25°C		66	125	µA	A
		T_A = –40°C to 85°C			130	µA	B
	Input impedance			50 || 1		kΩ || pF	C
$t_{d(on)}$	Turn-on time delay	Time for I_S to reach 50% of final value		1		µs	C
$t_{d(off)}$	Turn-off time delay	Time for I_S to reach 50% of final value		1		µs	C

(5) The GND pin usable range is from $V_{S–}$ to (V_{S+} – 5 V).

6.6 Timing Characteristics

PARAMETER		MIN	MAX	UNITS
t_{CL}	Clock period	200		ns

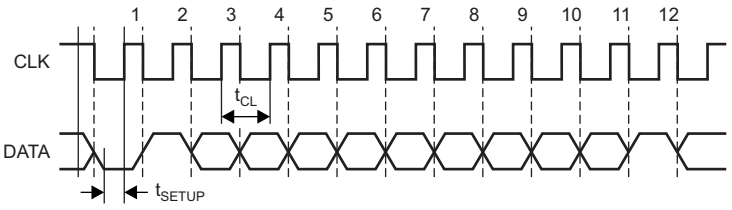
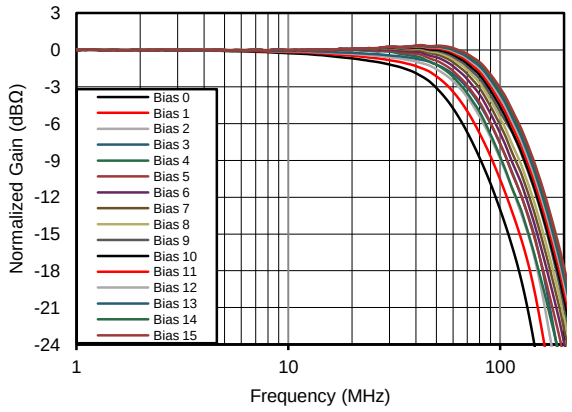


Figure 1. Serial Interface Timing

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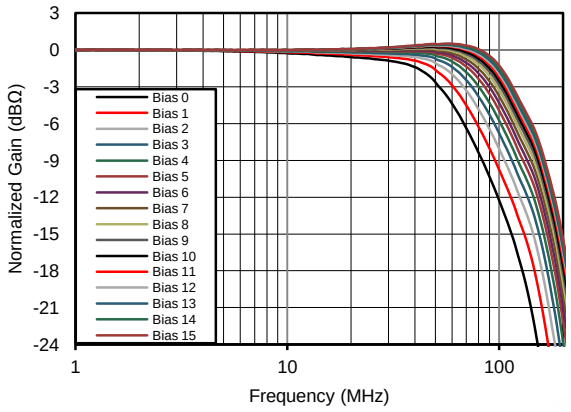
6.7 Typical Characteristics

At T_A = 25°C, 1:1.4 transformer, and 10.2-Ω matching resistance, unless otherwise noted



V_O = 2 V_{PP}

Figure 2. Normalized Small-Signal Frequency Response



V_O = 7.5 V_{PP}

Figure 3. Normalized Large-Signal Frequency Response

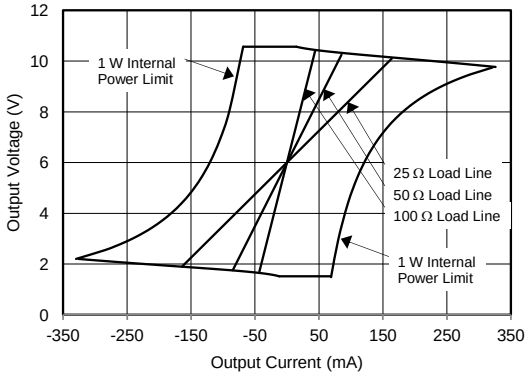
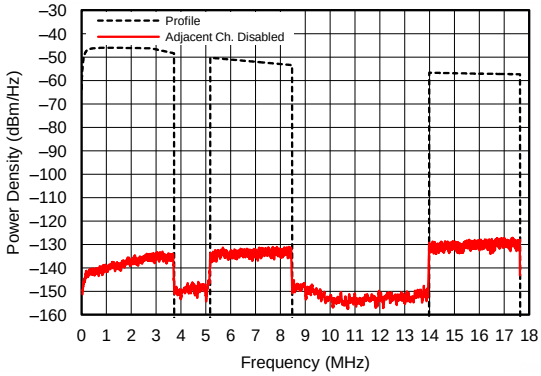


Figure 4. Output Voltage vs Output Current



14.5-dBm Tx Power in One Channel Bias 11
MTPR Measured on Adjacent channel

Figure 5. Profile 17a Crosstalk

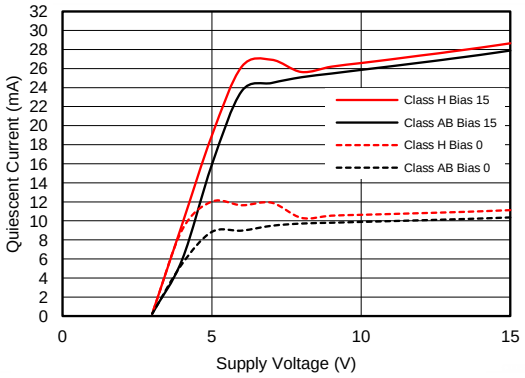


Figure 6. Quiescent Current vs Supply Voltage

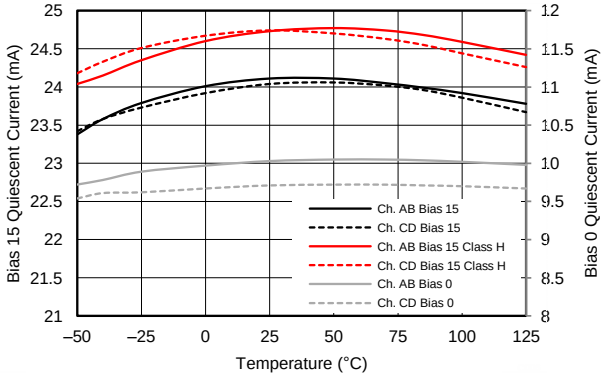
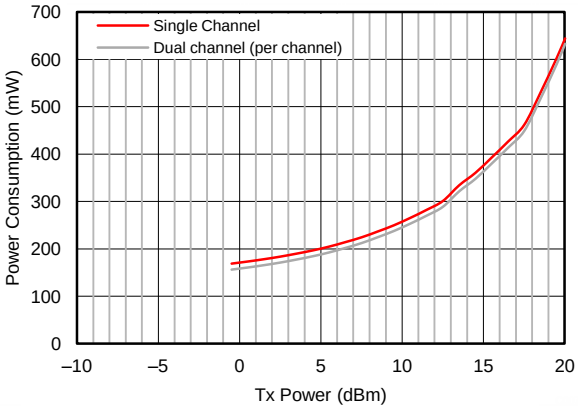


Figure 7. Quiescent Current vs Temperature

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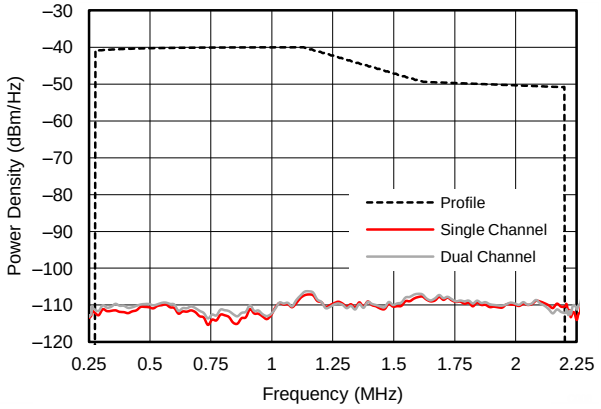
Typical Characteristics (continued)

At T_A = 25°C, 1:1.4 transformer, and 10.2-Ω matching resistance, unless otherwise noted



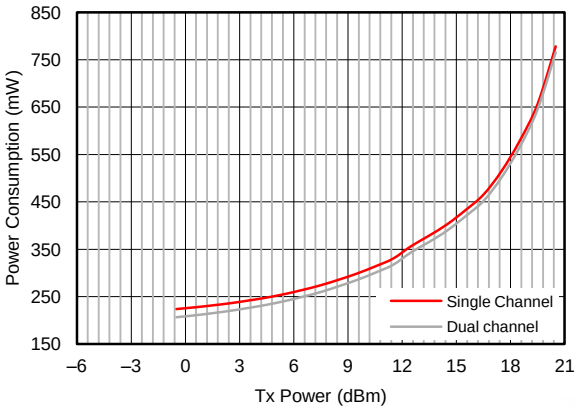
1:1.4 Transformer into 100 Ω Bias 2
ADSL

Figure 8. ADSL Power Consumption vs Tx Power



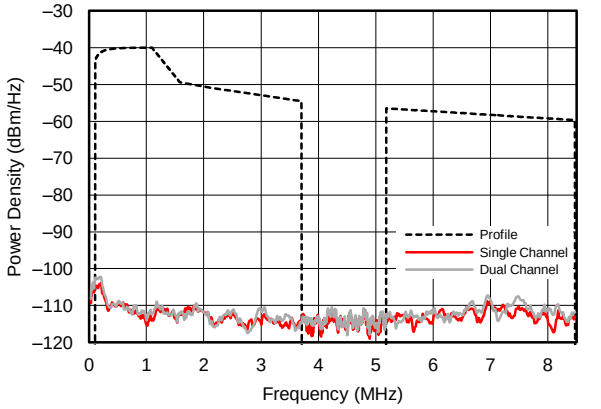
19.8-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 2

Figure 9. ADSL MTPR



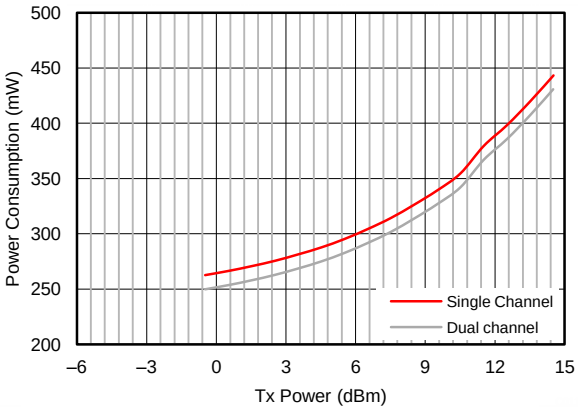
1:1.4 Transformer into 100 Ω VDSL Profile 8
Bias 7

Figure 10. Profile 8 Power Consumption vs Tx Power



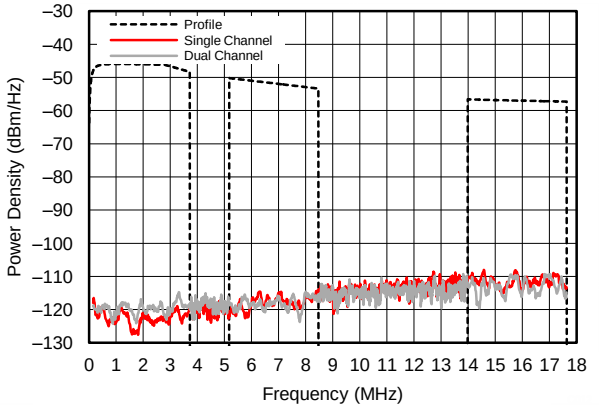
20.5-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 7

Figure 11. Profile 8 MTPR



1:1.4 Transformer into 100 Ω VDSL Profile 17
Bias 11

Figure 12. Profile 17 Power Consumption vs Tx Power



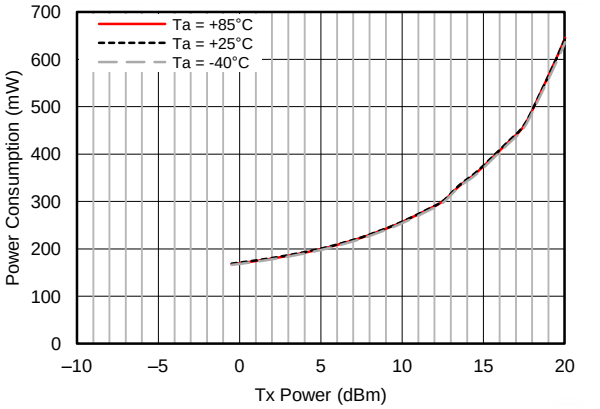
14.5-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 11

Figure 13. Profile 17 MTPR

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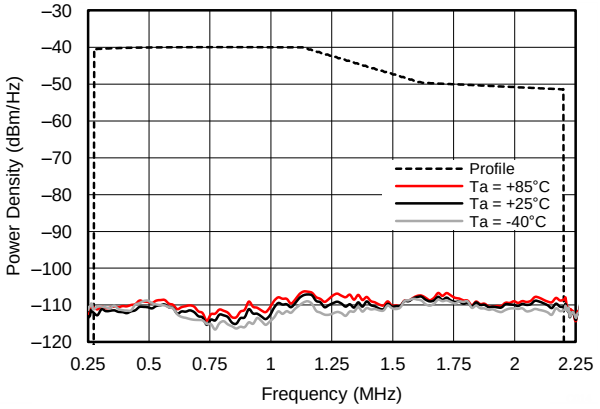
Typical Characteristics (continued)

At T_A = 25°C, 1:1.4 transformer, and 10.2-Ω matching resistance, unless otherwise noted



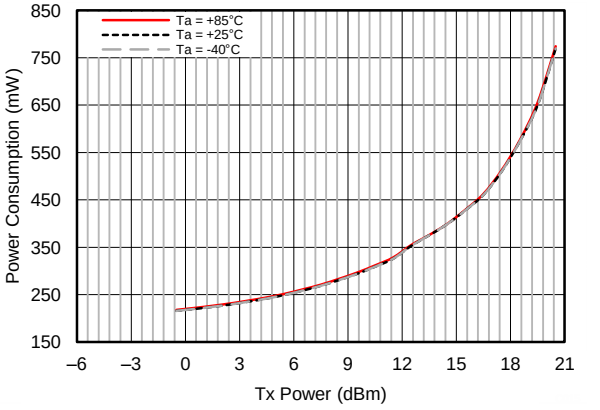
1:1.4 Transformer into 100 Ω Bias 2
ADSL

Figure 14. Single-Channel ADSL Power Consumption vs Temperature



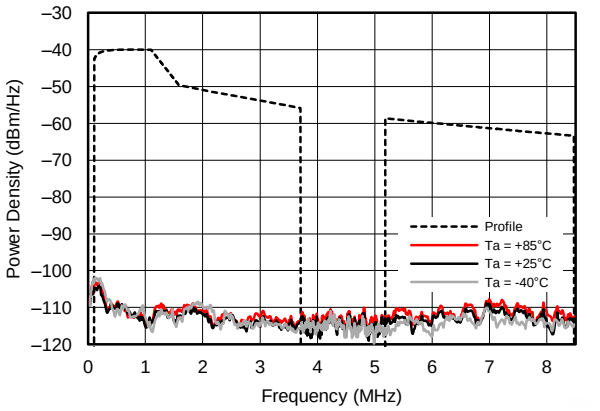
19.8-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 2

Figure 15. Single-Channel ADSL MTPR vs Temperature



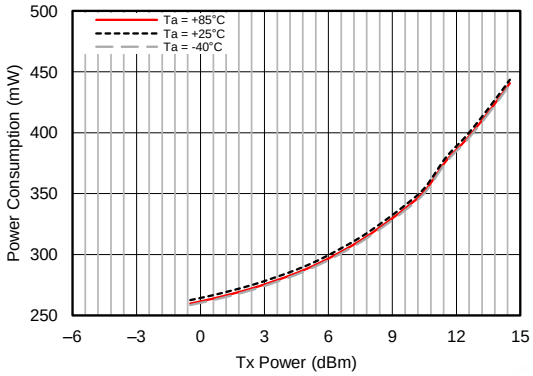
1:1.4 Transformer into 100 Ω VDSL Profile 8
Bias 7

Figure 16. Single-Channel Profile 8 Power Consumption vs Temperature



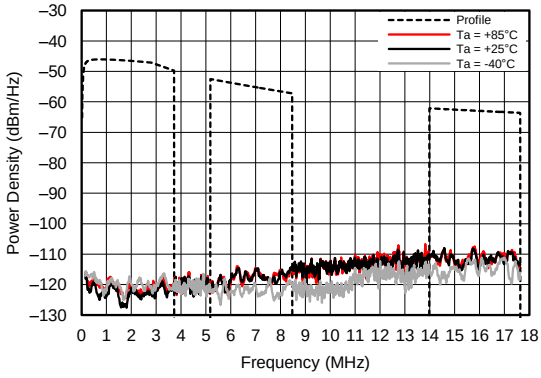
20.5-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 7

Figure 17. Single-Channel Profile 8 MTPR vs Temperature



1:1.4 Transformer into 100 Ω VDSL Profile 17
Bias 11

Figure 18. Single-Channel Profile 17 Power Consumption vs Temperature



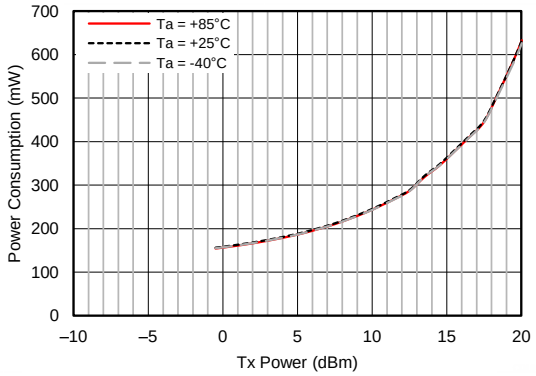
14.5-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 11

Figure 19. Single-Channel Profile 17 MTPR vs Temperature

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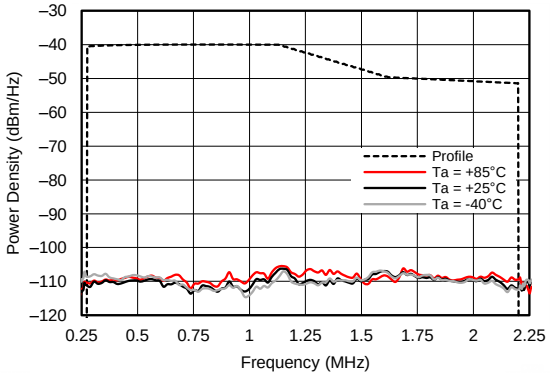
Typical Characteristics (continued)

At T_A = 25°C, 1:1.4 transformer, and 10.2-Ω matching resistance, unless otherwise noted



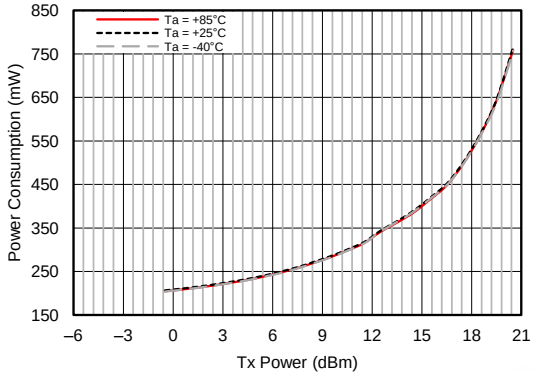
1:1.4 Transformer into 100 Ω — Bias 2
ADSL — Per Channel

Figure 20. Dual-Channel ADSL Power Consumption vs Tx Power



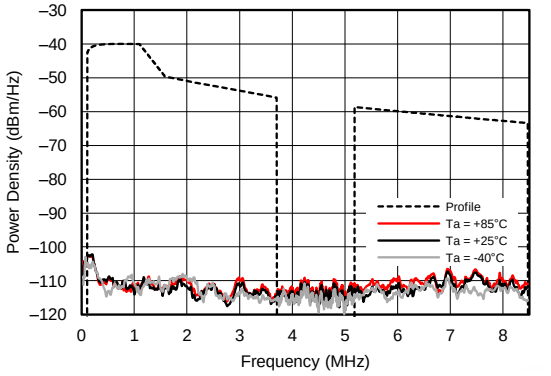
19.8-dBm Tx Power — 1:1.4 Transformer into 100 Ω
Bias 2

Figure 21. Dual-Channel ADSL MTPR vs Temperature



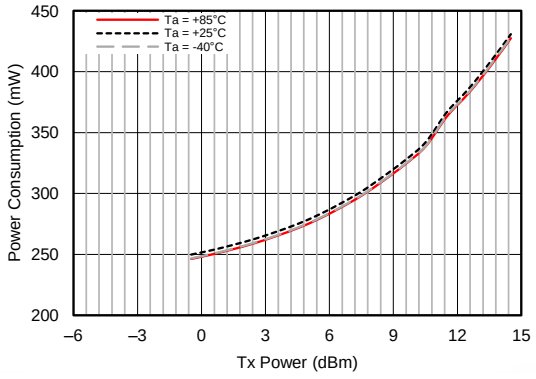
1:1.4 Transformer into 100 Ω — Bias 7
VDSL Profile 8 — Per Channel

Figure 22. Dual-Channel Profile 8 Power Consumption vs Temperature



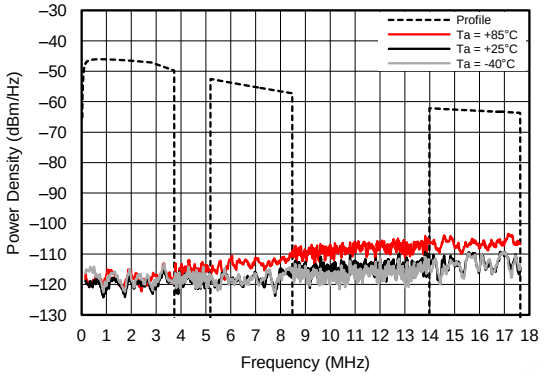
20.5-dBm Tx Power — 1:1.4 Transformer into 100 Ω
Bias 7

Figure 23. Dual-Channel Profile 8 MTPR vs Temperature



1:1.4 Transformer into 100 Ω — Bias 11
VDSL Profile 17 — Per Channel

Figure 24. Dual-Channel Profile 17 Power Consumption vs Temperature



14.5-dBm Tx Power — 1:1.4 Transformer into 100 Ω
Bias 11

Figure 25. Dual-Channel Profile 17 MTPR vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, 1:1.4 transformer, and 10.2-Ω matching resistance, unless otherwise noted

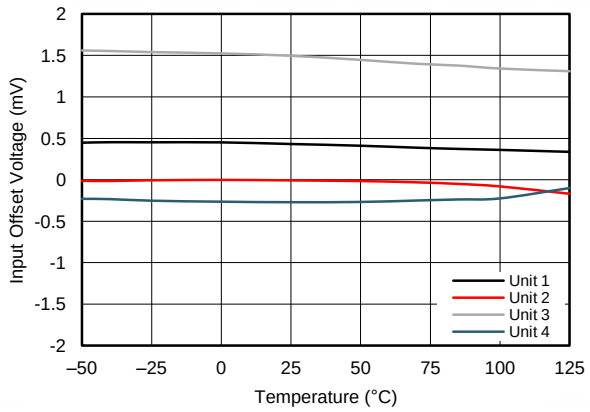


Figure 26. Input Offset Voltage vs Temperature

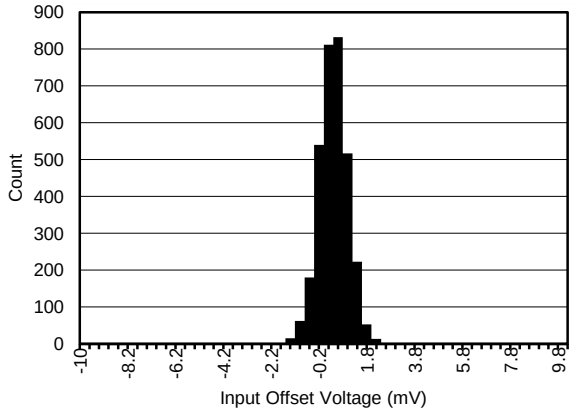
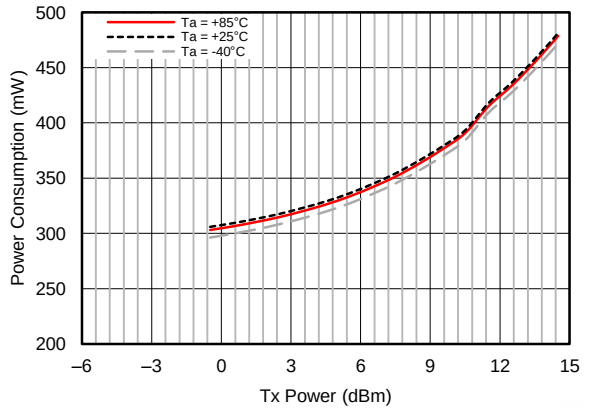
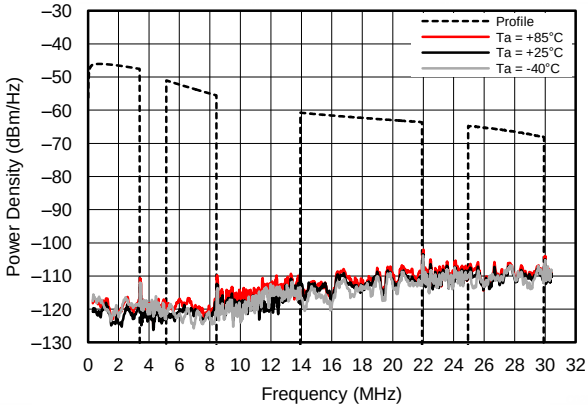


Figure 27. Input Offset Voltage Histogram



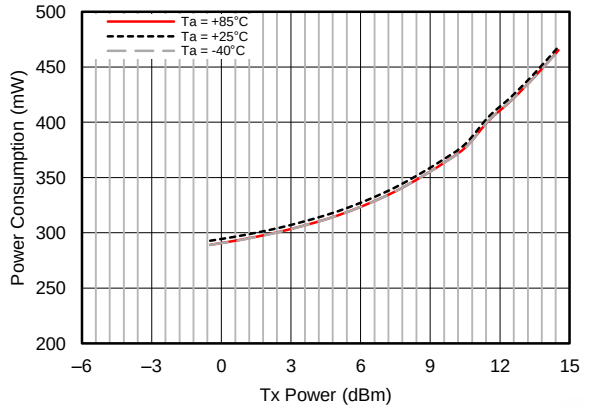
1:1.4 Transformer into 100 Ω Bias 15
VDSL Profile 30

Figure 28. Single-Channel Profile 30 Power Consumption vs Temperature



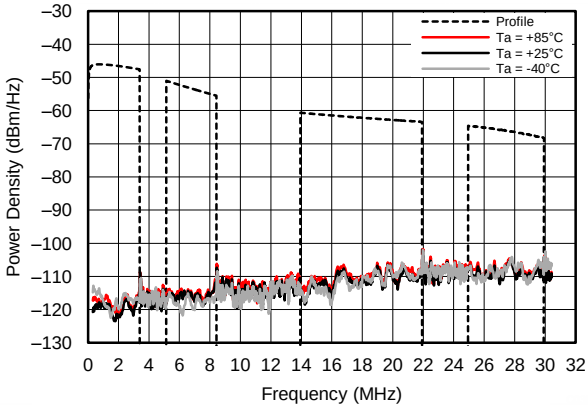
14.5-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 15

Figure 29. Single-Channel Profile 30 MTPR vs Temperature



Per Channel

Figure 30. Dual-Channel Profile 30 Power Consumption vs Temperature



14.5-dBm Tx Power 1:1.4 Transformer into 100 Ω
Bias 15

Figure 31. Dual-Channel Profile 30 MTPR vs Temperature

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7 Detailed Description

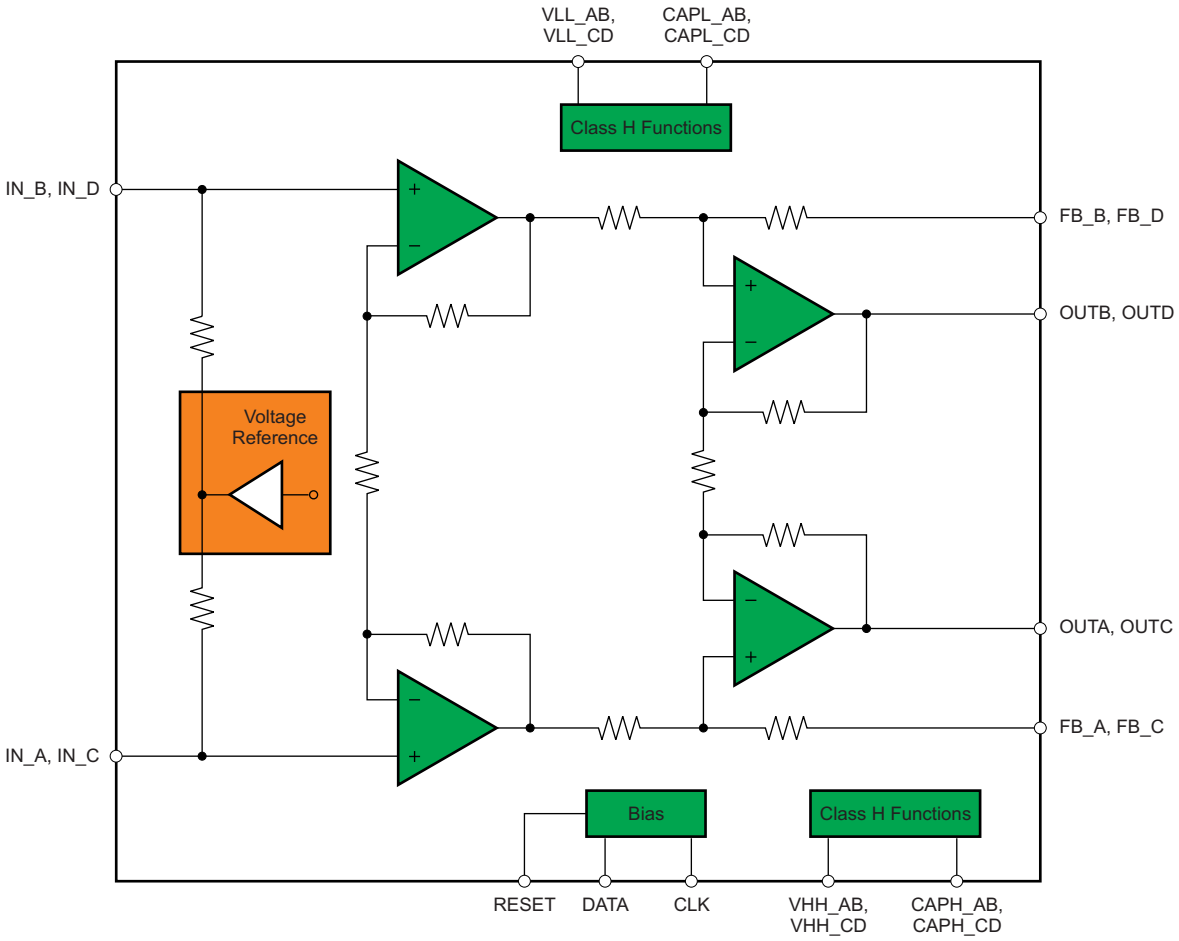
7.1 Overview

The THS6226A class H line driver provides exceptional ac performance in conjunction with wide output voltage swing. The class H operation allows voltage swings to exceed the power supply for short intervals limited only by the charge in the capacitor. In class AB mode, the device is capable of driving a 100-Ω load from +1.8 V to +10.2 V. In class H mode, under the same conditions, the output voltage range becomes an impressive –5.5 V to +17.5 V, or 46 V_{PP} differentially with the capacitor fully charged.

The *Functional Block Diagram* section shows a fully-differential, noninverting amplifier configuration with active impedance. In this configuration, the 10.2-Ω matching resistor appears through the transformer as 100 Ω, minimizing reflection on the line. This active impedance scheme also minimizes transmission losses, as compared to passive termination. Device gain is fixed and is equal to 19 V/V from the input to the output of the amplifier ($IN_{AB/CD}$ to $OUT_{AB/CD}$), not including the transformer-turn ratio or the termination loss.

To simplify the implementation as well as to provide design flexibility, the device contains an integrated mid-supply buffer that provides the correct biasing to the amplifier core without requiring any external components. Also present is a two-pin serial interface that provides exceptional design flexibility and allows minimal power consumption for each xDSL profile.

7.2 Functional Block Diagram



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7.3 Feature Description

The device incorporates several hardware and functionality features: a high output current line driver, a charge pump, a voltage reference, a logic circuit, an active impedance, and a RESET pin. The device has two ports. Each port consists of a high output current line driver, a charge pump, and a reference voltage. Common circuits are the RESET feature and the logic circuit.

7.3.1 High Output Current Line Driver

The main purpose for the device is to provide a high output current into a heavy load. For the THS6226A, with its xDSL application targeted, the load is typically 100 Ω and currents as high as 400 mA are supported with excellent linearity. The core of the line driver is a class AB amplifier providing both good efficiency and high current drive capability. The high output line driver is the core of the device and any external circuit interface is located on both the device inputs and output.

7.3.2 Charge Pump

The class H functionality of the device is brought on by the integration of a charge pump. The charge pump is a power-supply function to the line driver. The role of the charge pump is to vary the power supply from (12 V / GND) to (20 V / –8 V) and allow the line driver to support high peak to average ratio (PAR) signals while minimizing power consumption and maintaining excellent linearity. The charge pump is controlled externally by the V_{H_EN} pin. A logic high on the V_{H_EN} pin results in the power supply of the class AB line driver going to (20 V / –8 V), while a logic low on the V_{H_EN} pin results in normal operation under the (12 V / GND) supplies.

7.3.3 Voltage Reference

An internal voltage reference provides the device common-mode input and output voltage.

7.3.4 Logic

The DATA and CLK pins allow access to the internal logic circuit implemented in the device. This logic circuit allows each channel to either be programmed individually for quiescent current, turn the charge pump on or off, disable the main amplifier, or select the line termination mode. For more information on programming, refer to the *Programming* section.

7.3.5 Active Impedance

The line driver incorporates the positive feedback path to provide the termination to the load. For the device, the synthesis factor implemented is 5.

7.3.6 RESET Pin

The RESET pin provides a quick and easy way to disable the two ports immediately if a fault condition on the line occurs.

7.4 Device Functional Modes

There are several functional modes for the device. These functional modes can be accessed with the CLK and DATA pins. Each main line driver quiescent current can be set to 16 different bias modes: bias 0 through bias 15. Additionally, the line driver and class H feature can be controlled to have the following configuration:

- Class AB mode is the main line driver by itself. The output voltage is limited by the (12 V / GND) power-supply rails. The quiescent current is then set by four bits.
- Class H mode is the main line driver used in conjunction with the class H feature. The output voltage is limited by the (20 V / –8 V) internally-generated power-supply rails. The quiescent current of the main line driver is set by four bits, as in class AB mode.
- Line termination mode is the powered-down mode for the line driver. This mode maintains line termination but has reduced linearity performance.
- Disabled mode.

For more information on these mode, refer to the *Programming* section.

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7.5 Programming

7.5.1 Programming the Device

Programming the device is accomplished through a serial interface (pins 4 and 5) and proceeds in the following sequence:

- Two start bits are required (B0 = 0 followed by B1 = 1).
- B2 through B9 are used to program the device. (Table 1 lists the bit descriptions.)
- B10 (described in Table 2) is the parity bit that controls whether the word is loaded or not.
- B11 is the stop bit and must be set to B11 = 1.

Figure 32 shows the required sequence.

Table 1. DATA Sequence

PARAMETER	DESCRIPTION
B0, B1	Start bits
B2, B3	Channel select
B4, B5	Power-down features
B6-B9	Quiescent current setting
B10	Parity bit
B11	Stop bit

Table 2. Parity Bit

B10	ODD PARITY BIT
0	For an odd number of high bits in B2 to B9, set B10 to 0
1	For an even number of high bits in B2 to B9, set B10 to 1

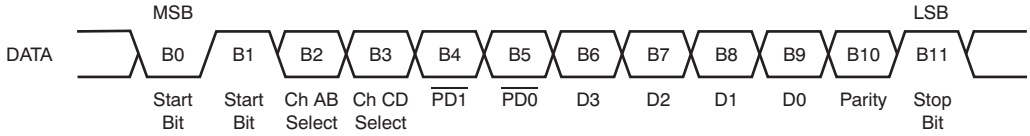


Figure 32. DATA Description

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7.5.2 Quiescent Current

The device quiescent current is dissipated in two main device modules: the class AB and the charge pump. Bits B4 ($\overline{PD1}$) and B5 ($\overline{PD0}$) select one of the possible four modes of operation:

1. Class AB mode (charge pump disabled),
2. Class H mode (charge pump enabled),
3. Disable mode, or
4. Line termination mode (maintains line matching, core amplifier at very low bias mode and charge pump disabled for lowest power consumption possible).

Table 3 lists the details on each bit functionality and the approximate quiescent current. The various power modes are shown in Table 3. For all modes, when B6 through B9 are not defined, set B9 = B8 = B7 = B6 = 0 to achieve the lowest power dissipation possible.

Table 3. Power Modes

B4 (PD1)	B5 (PD0)	POWER-DOWN MODE	APPROXIMATE I_Q (mA per Port)
0	0	Power-down (B9 = B8 = B7 = B6 = 0)	0.85
0	1	Line termination mode (B9 = B8 = B7 = B6 = 0)	4.4
1	0	Class AB driver I_Q set by B6 to B9, class H disabled	—
1	1	Class AB driver I_Q set by B6 to B9, class H enabled	—

The class AB quiescent current is set by bits B6 to B9, using B4 and B5 for the power-down function and B2 and B3 for channel selection. The approximate quiescent current for the amplifier core is shown in Table 4.

Table 4. Class AB Quiescent Current

BIAS	B6 (D3)	B7 (D2)	B8 (D1)	B9 (D0)	QUIESCENT CURRENT SETTING	APPROXIMATE I_Q (mA per Port)
0	0	0	0	0		9.4
1	0	0	0	1		10.4
2	0	0	1	0	ADSL2+ mode	11.5
3	0	0	1	1		12.5
4	0	1	0	0		13.6
5	0	1	0	1		14.6
6	0	1	1	0		15.7
7	0	1	1	1	Profile 8b mode	16.7
8	1	0	0	0		17.8
9	1	0	0	1		18.8
10	1	0	1	0		19.8
11	1	0	1	1	Profile 17a mode	20.8
12	1	1	0	0		21.8
13	1	1	0	1		22.8
14	1	1	1	0		23.8
15	1	1	1	1		24.8

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Channel selection is shown in Table 5. Each channel can be programmed independently, or together if both B2 and B3 are set to 1.

Table 5. Channel Selection

B2 (Channel AB)	B3 (Channel CD)	CHANNEL SELECT
0	0	Bits B4 to B9 are ignored
0	1	Channel B programmed with B4 to B9
1	0	Channel A programmed with B4 to B9
1	1	Channels A and B programmed with B4 to B9

At startup, the internal register is set as shown in Figure 33.

Figure 33. Internal Register

7	6	5	4	3	2	1	0
Ch. AB Select (B2)	Ch. CD Select (B3)	$\overline{PD1}$(B4)	$\overline{PD0}$(B5)	D3 (B6)	D2 (B7)	D1 (B8)	D0 (B9)
W	W	W	W	W	W	W	W

LEGEND: W = Write

In this condition, the total quiescent power dissipation is 10.2 mW per port on a +12-V supply.

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8 Applications and Implementation

8.1 Application Information

The device is a dual-port, very-high-bit-rate digital subscriber line (VDSL), class H line driver. Typically, the signal is generated by a high-speed digital-to-analog converter (DAC). The device drives a twisted pair.

The digital subscriber line (DSL) system is ac-coupled as it transmits information above the audio band. On the input of the line driver, this ac-coupling translates into the series capacitors to isolate the dc voltage coming from the DAC output common-mode voltage. On the output, a transformer is used to help isolate the 48V present between tip and ring of the telephone line.

The transformer can be set to any useful ratio. In practice, the transformer-turn ratio is set between 1:1 and 1:1.4 for the device. As mentioned in the *Feature Description* section, the active impedance synthesis factor is 5. This synthesis factor means that the termination resistor is 1/5th of the load impedance reflected to the transformer secondary. Thus, the correct termination can be selected based on the transformer-turn ratio.

Note that the resulting load detected by the amplifier may affect the amplifier linearity or output voltage swing capabilities.

8.2 Typical Application

The typical application circuit for this application is shown in Figure 34.

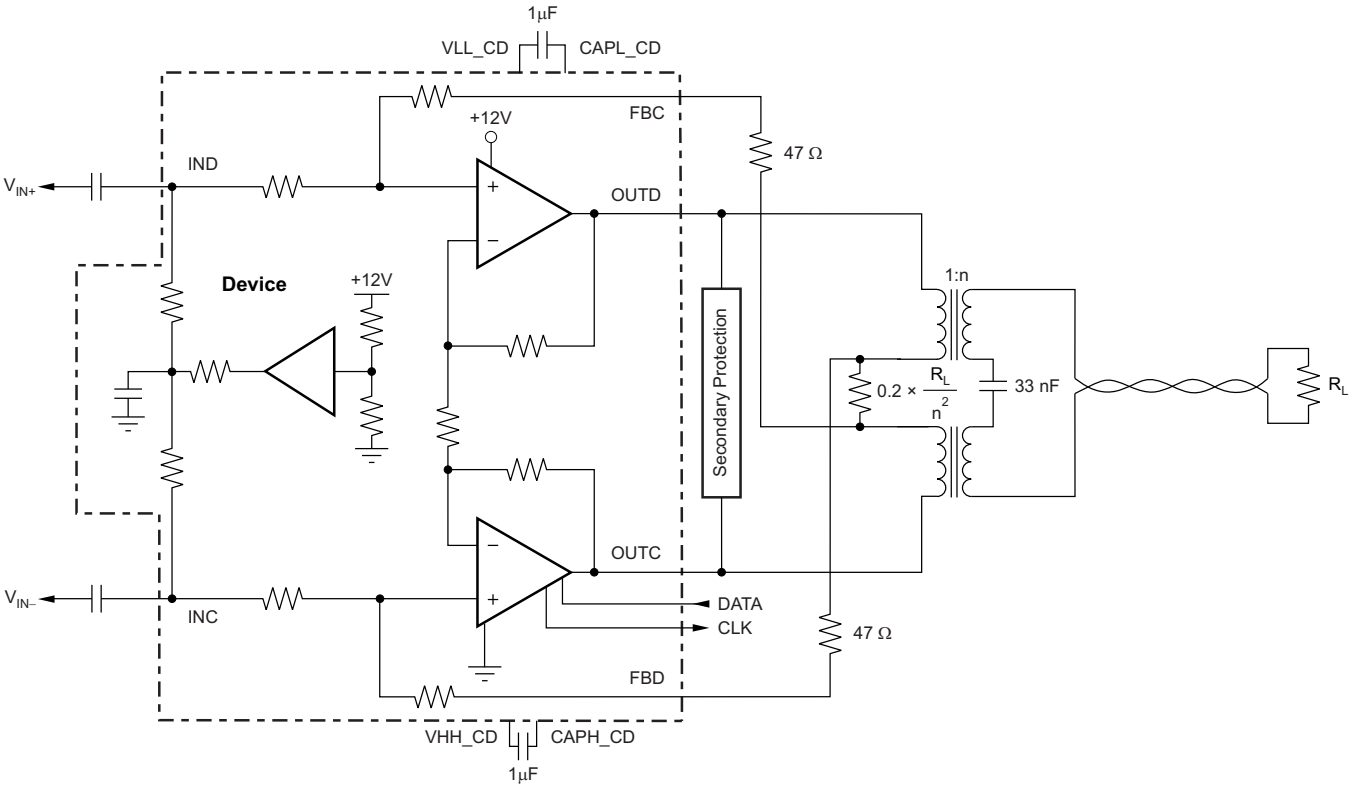


Figure 34. Typical VDSL Line Driver Circuit Configuration

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Typical Application (continued)

8.2.1 Design Requirements

Table 6. Design Requirements

DESIGN REQUIREMENT	CONDITION
AC-coupling capacitors	0.1 µF
Synthesis factor	5
Output transformer ratio	1:1.4
Surge protection circuit	Not shown

8.2.2 Detailed Design Procedure

The input capacitor forms a high-pass filter with the device input impedance. This pole must be set at a frequency low enough to not interfere with the desired signal.

The output transformer can be changed to any transformer-turn ratio. Note that the load is expected to be a transmission line with 100-Ω characteristic impedance. Referred to the transformer secondary, the load detected by the amplifier is $1 / n^2$ with 1:n being the transformer-turn ratio.

Practical limitations force the transformer-turn ratio to be between 1.4:1 and 1:2. At the lighter load detected by the amplifier (1.4:1), the voltage swing is limited by the class H and the maximum achievable swing of the amplifier. At the heaviest load (1:2), the voltage swing is limited by the current drive capability of the amplifier. To satisfy the synthesis impedance factor and the loading, the series resistance (R_S) can be set to $R_S = R_L / 5 = 100\ \Omega / (5 \times n^2)$.

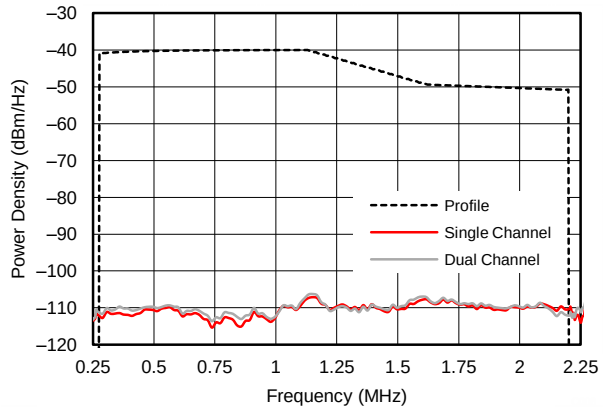
For the charge pump, consider the thermal characteristic of the capacitor (X7R, X5R, or Y5V can be used for the charge pump).

For the power-supply bypass, consider using only X7R or X5R because of the better stability of these materials over temperature.

For surge protection, consider adding 47-Ω resistors in series on the positive feedback path. The secondary protection is also normally added after the series resistance on the secondary transformer.

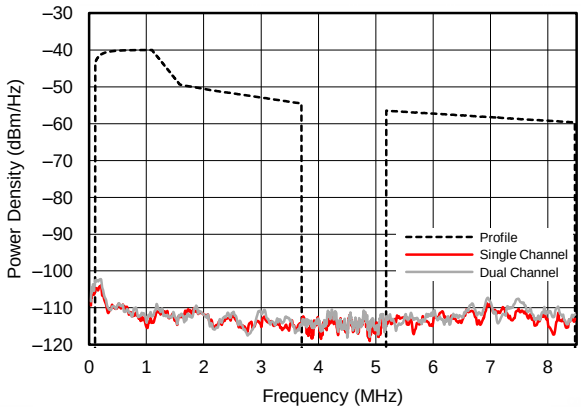
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8.2.3 Application Curves



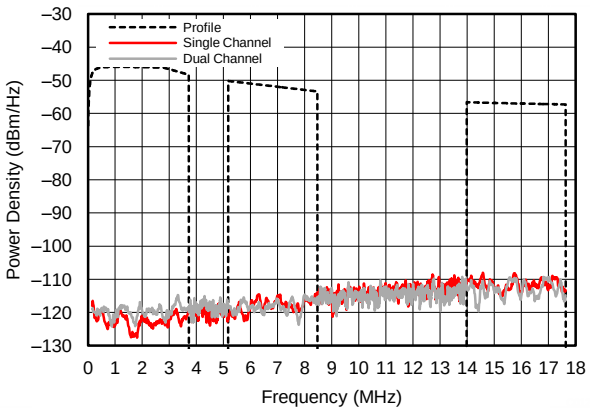
19.8-dBm Tx Power
1:1.4 Transformer into 100 Ω
Bias 2

Figure 35. ADSL MTPR



20.5-dBm Tx Power
1:1.4 Transformer into 100 Ω
Bias 7

Figure 36. VDSL 8b MTPR



14.5-dBm Tx Power
1:1.4 Transformer into 100 Ω
Bias 11

Figure 37. VDSL 17a MTPR

8.3 Initialization Set Up

After the initial power-up and prior to sending any words to program the device, TI recommends sending a string of twelve 1s (111111111111) to ensure that the state machine is initialized.

9 Power Supply Recommendations

As a result of large recharge current flowing in and out of the four charge pump capacitors during charge pump discharge and recharge events, TI recommends placing bypass capacitors that are at least equal in value to the charge pump capacitor close to each supply voltage pin. A minimum of 2-µF bypass capacitors for each channel are required to minimize any transient appearing on the power supply because both positive and negative charge pump 1-µF bypass capacitors are recharged on the +12-V supply.

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10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6226A requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a. **Minimize parasitic capacitance** to any ac ground for all signal I/O pins. Excessive parasitic capacitance on the inverting input pin can cause instability. In the line driver application, the parasitic capacitance forms a pole with the load detected by the amplifier and may reduce the effective bandwidth of the application circuit, thus leading to degraded performance. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

b. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors. An additional low ESR supply decoupling capacitor (≥ 2 µF, X7R or X5R) to ground is necessary to provide a transient current during the charge pump capacitors recharge.

c. **Careful selection and placement of external components preserves the high-frequency performance of the device.** Use very low reactance type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and printed circuit board traces as short as possible. Never use wire-wound type resistors in a high-frequency application.

d. **Connections to other wideband devices** on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.

e. **Do not socket a high-speed part such as the THS6226A.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the device onto the board.

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10.2 Layout Example

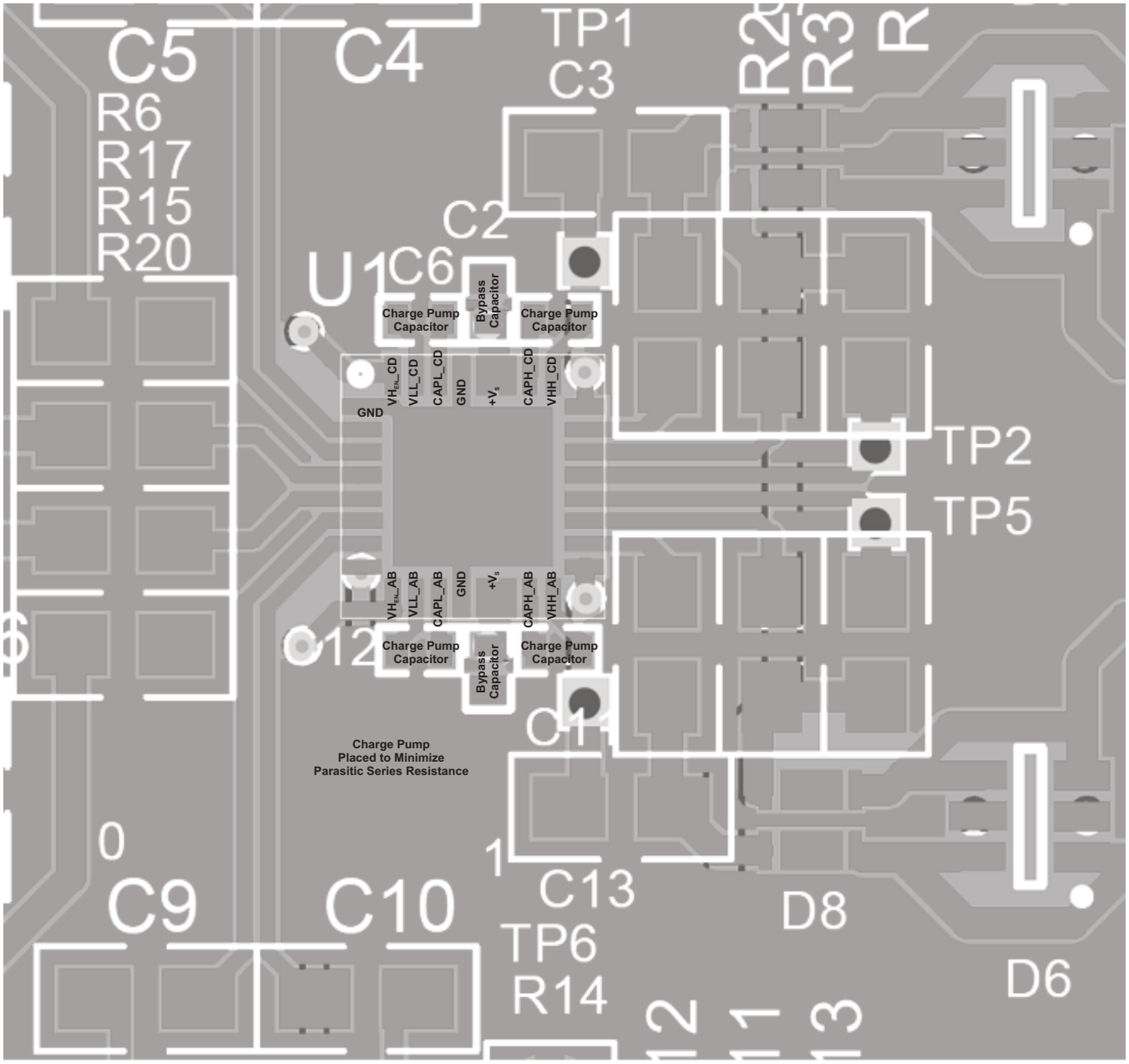


Figure 38. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《*PowerPAD™ 耐热增强型封装*》(，SLMA002

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6226AIRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	HS6226A IRHB	Samples
THS6226AIRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	HS6226A IRHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

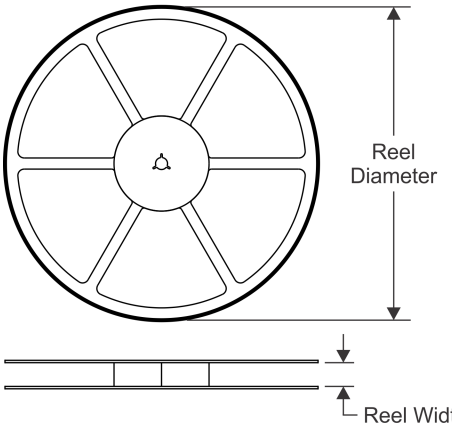
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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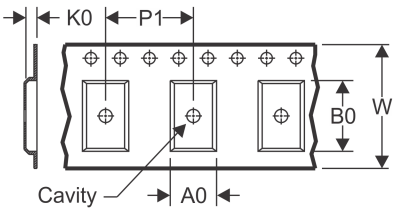
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

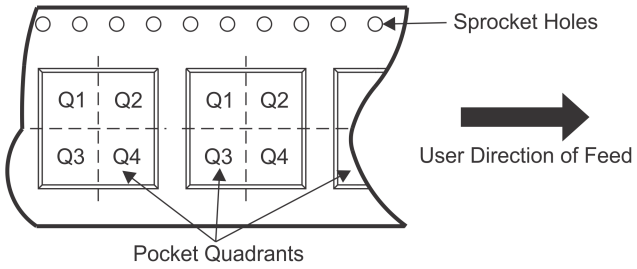


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

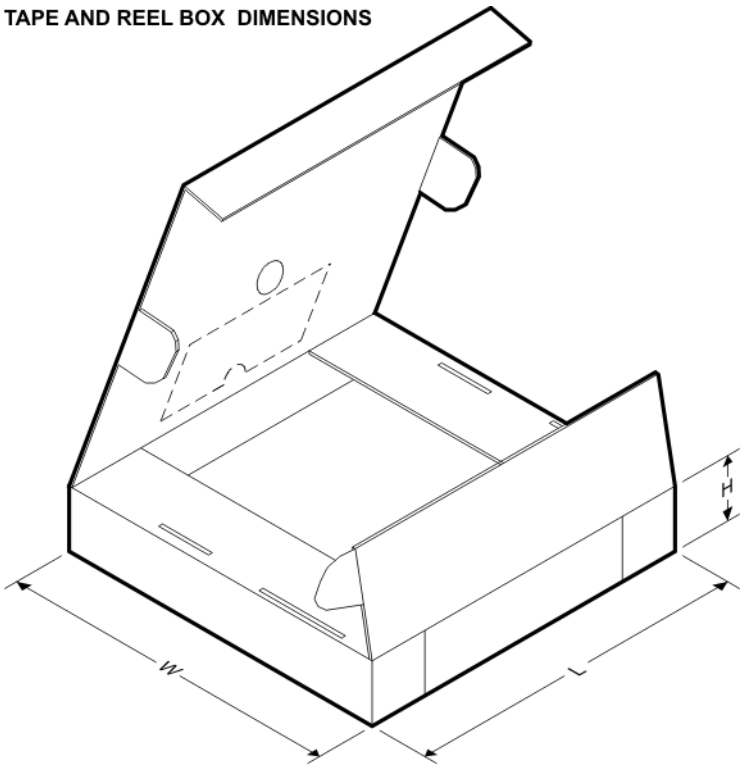
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6226AIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
THS6226AIRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6226AIRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
THS6226AIRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

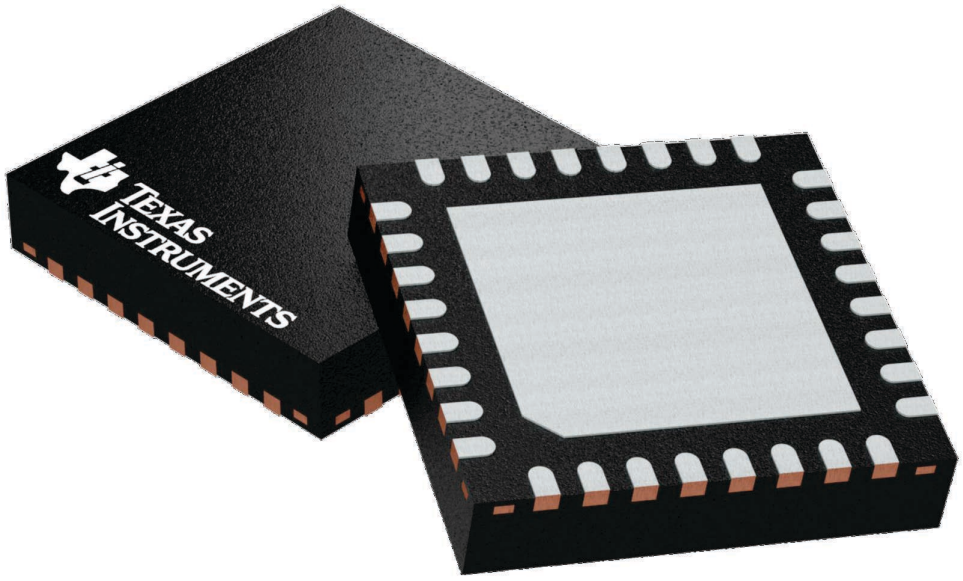
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

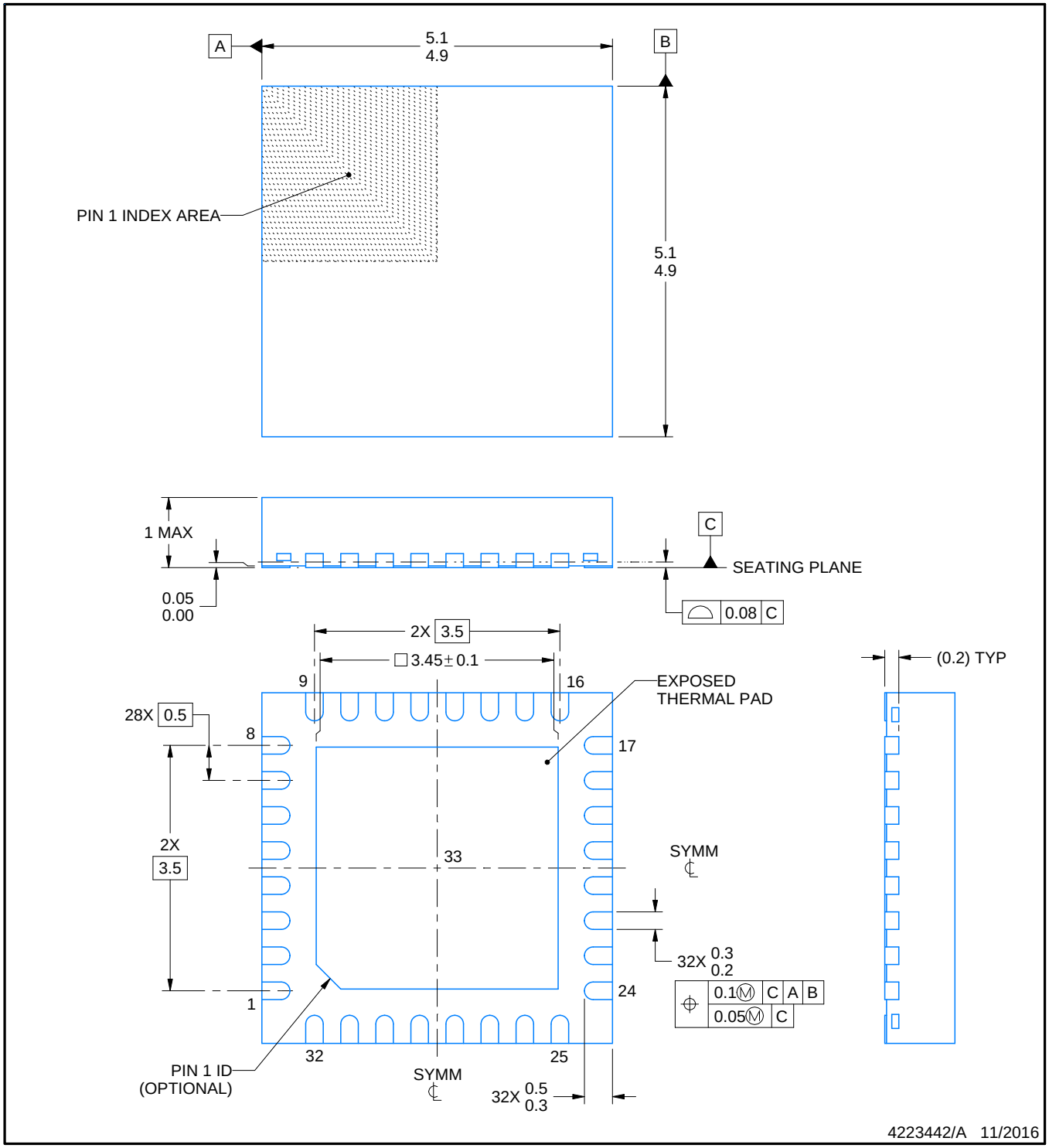
4224745/A

RHB0032E

PACKAGE OUTLINE

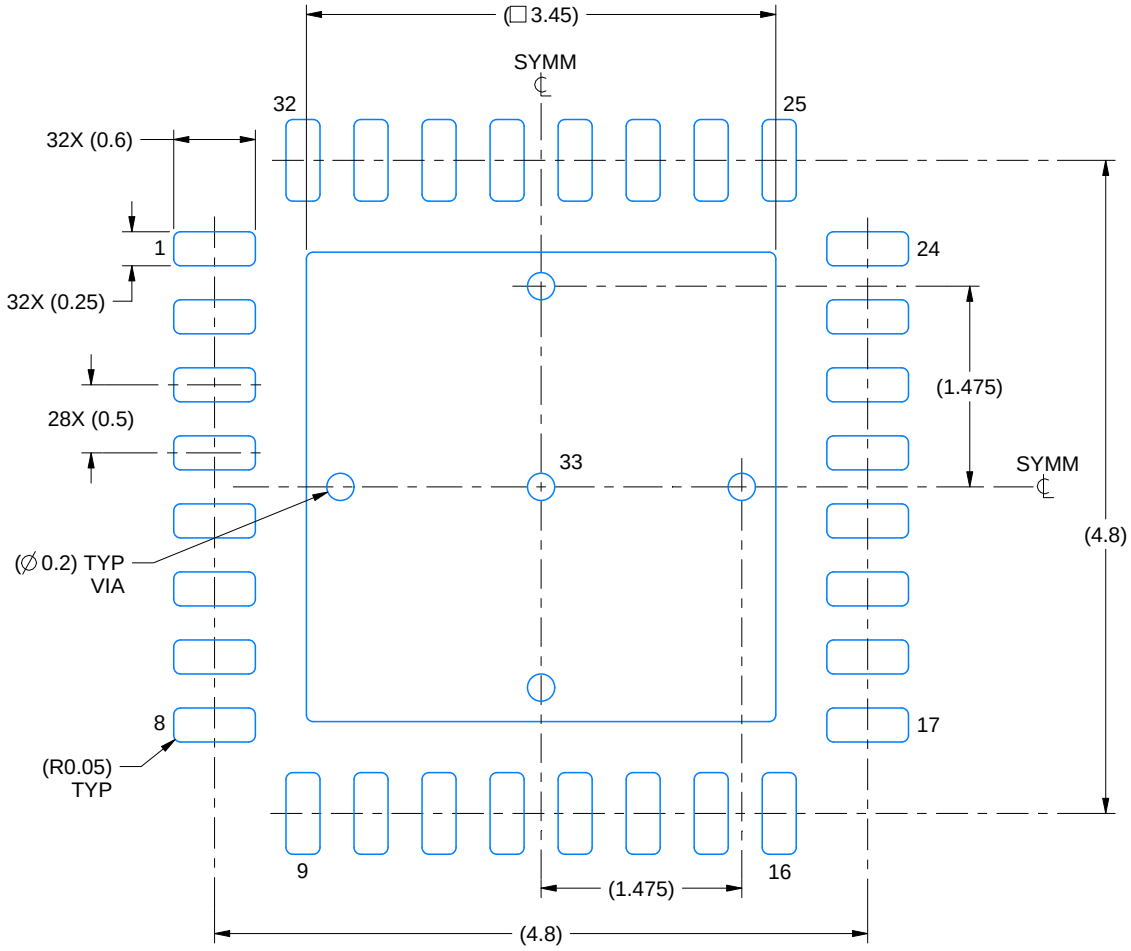
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

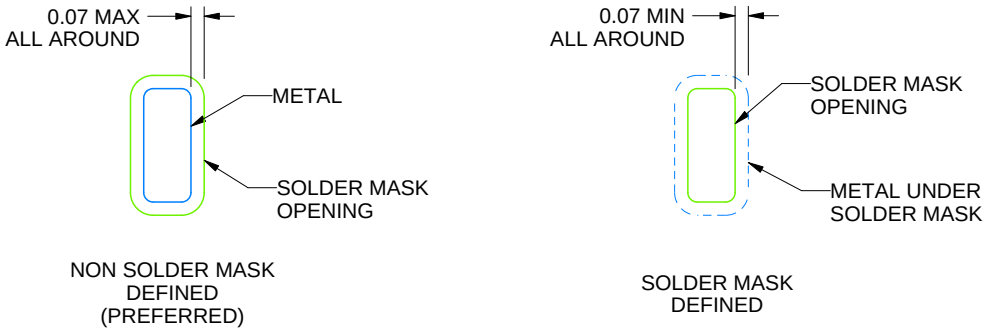


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

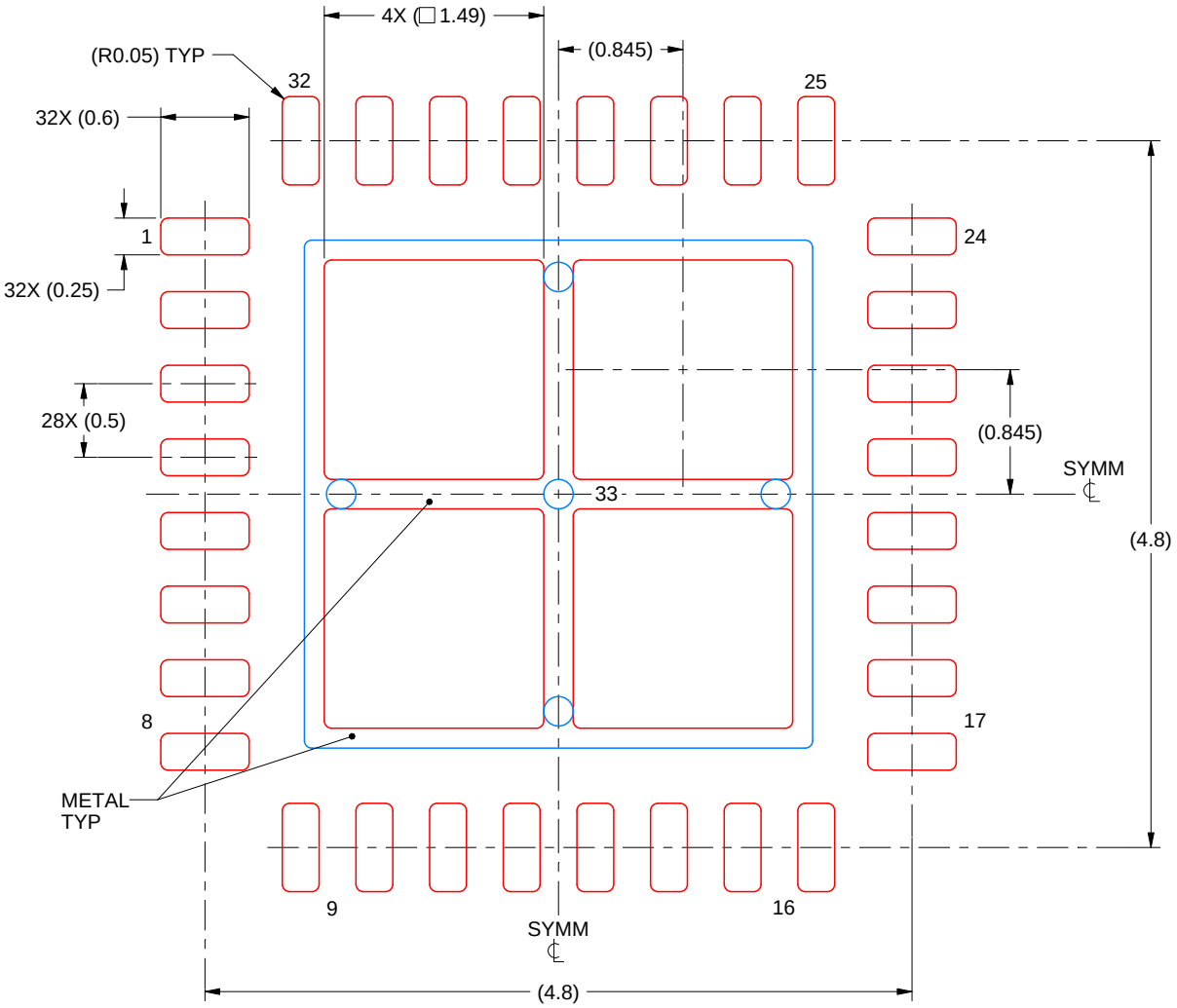


SOLDER MASK DETAILS

4223442/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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