OPAx626 高速、高精度、低失真 16 位和 18 位模数转换器 (ADC) 驱动器

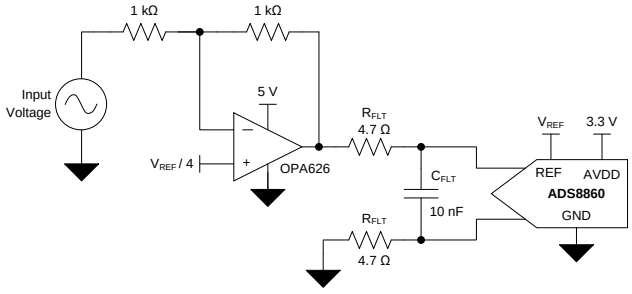
1 特性

- 出色的动态性能：
  - 低失真：100kHz 时，HD2 为 –122dBc；HD3 为 –140dBc
  - 增益带宽 (G = 100)：120MHz
  - 转换率：115V/µs
  - 4V 输出时的 16 位稳定时间： 280ns
  - 低电压噪声：10kHz 时为 2.5nV/√Hz
  - 低输出阻抗：1MHz 时为 1Ω
- 出色的直流精度：
  - 偏移电压：±100µV（最大值）
  - 偏移电压漂移：±3µV/ºC（最大值）
  - 低静态电流：2mA（典型值）
- 输入共模范围包括负电源轨
- 轨到轨输出
- 宽额定温度范围：-40℃ 至 +125℃

2 应用

- 精密逐次逼近寄存器 (SAR) ADC 驱动器
- 精密电压基准缓冲器
- 可编程逻辑控制器
- 测试和测量设备
- 科学仪表
- 高吞吐量数据采集系统
- 高密度、多路复用数据采集系统

SAR ADC 驱动器



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3 说明

OPAx626 系列运算放大器是 16 位和 18 位 SAR ADC 驱动器，具备高精度、低总谐波失真 (THD) 及低噪声等特性。该系列高精度运放在额定工作条件下的 16 位稳定时间为 280ns，可提供真正的 16 位有效位数 (ENOB)。该系列器件具备高直流精度（偏移电压仅为 100µV）、120MHz 的宽增益带宽积以及 2.5nV/√Hz 的低宽带噪声，并且经优化可驱动高吞吐量、高分辨率的 SAR ADC， 例如 ADS88xx 系列 SAR ADC。

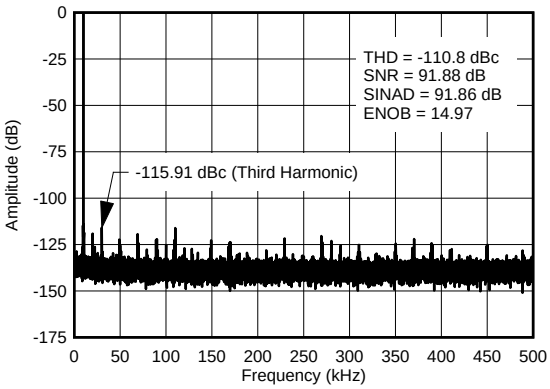
OPAx626 系列采用 5 引脚小外形尺寸晶体管 (SOT) 封装和
8 引脚超薄小外形尺寸 (VSSOP) 封装，额定工作温度范围为 –40°C 至 +125℃。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA626	小外形尺寸晶体管 (SOT) (5)	2.90mm x 1.60mm
OPA2626	超薄小外形尺寸封装 (VSSOP) (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

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（f_{IN} = 10kHz，1MSPS FFT）



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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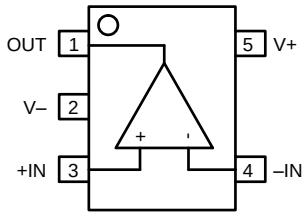
4 修订历史记录

日期	修订版本	注释
7 月2 月	*	最初发布版本。

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5 Pin Configuration and Functions

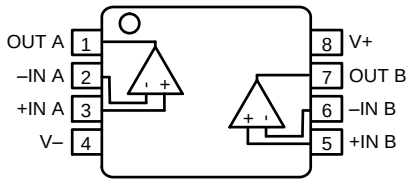
OPA626 DBV Package
5-Pin SOT
Top View



Pin Functions: OPA626

PIN		I/O	DESCRIPTION
NAME	NO		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output terminal
V+	5	—	Positive supply voltage
V–	2	—	Negative supply voltage

OPA2626 DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2626

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input for channel A
–IN A	2	I	Inverting input for channel A
+IN B	5	I	Noninverting input for channel B
–IN B	6	I	Inverting input for channel B
OUT A	1	O	Output terminal for channel A
OUT B	7	O	Output terminal for channel B
V+	8	—	Positive supply voltage
V–	4	—	Negative supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S	(V+) – (V–)		6	V
Input voltage(2)	+IN	(V–) – 0.3	(V+) + 0.3	V
	–IN	(V–) – 0.3	(V+) + 0.3	
Output voltage	OUT	(V–)	(V+)	V
Sink current	+IN		10	mA
	–IN		10	
	OUT		150	
Source current	+IN		10	mA
	–IN		10	
	OUT		150	
Temperature	Operating junction	–40	150	°C
	Operating free-air temperature, T_A	–55	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For input voltages beyond the power-supply rails, voltage or current must be limited.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply input voltage, (V+) – (V–)		2.7		5.5	V
V_I	Input voltage	+IN	(V–)		(V+) – 1.15	V
		–IN	(V–)		(V+) – 1.15	
V_O	Output voltage		(V–)		(V+)	V
I_O	Output current		–120		120	mA
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		OPA626 DBV (SOT) 5 PINS	OPA2626 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.9	171.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.6	68.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.7	91.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.1	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.2	90.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics: High-Supply

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			80		MHz
φ_m	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			120		MHz
SR	Slew rate	V_O = 1-V step, G = 1			45		V/µs
		V_O = 4-V step, G = 2			115		
t_{settle}	Settling time	V_O = 4-V step, G = 2	Settling time to 0.1% (10-bit accuracy)		80		ns
			to 0.005% (14-bit accuracy)		110		
			to 0.00153% (16-bit accuracy)		280		
	Overshoot	V_O = 4-V step, G = 2			2.5%		
	Undershoot	V_O = 4-V step, G = 2			3%		
HD2	Second-order harmonic Distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		144		dBc
			f = 100 kHz		122		
			f = 1 MHz		80		
HD3	Third-order harmonic Distortion	V_O = 2 V_{PP}, G = 2	f = 10 kHz		155		dBc
			f = 100 kHz		140		
			f = 1 MHz		80		
	Second-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			90		dBc
	Third-order intermodulation distortion	V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			100		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz, peak-to-peak			0.8		μV_{PP}
		f = 0.1 Hz to 10 Hz, rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 1 kHz			3.2		$nV/\sqrt{Hz}$
		f = 10 kHz			2.5		
I_n	Input current noise density	f = 1 kHz			6.6		$pA/\sqrt{Hz}$
		f = 10 kHz			3.5		
t_{OR}	Overload recovery time	G = 5			50		ns
Z_o	Open-loop output impedance	f = 1 MHz			1		Ω
	Crosstalk	DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to 125°C				±300	

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Electrical Characteristics: High-Supply (continued)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			0.5	±3	µV/°C
		OPA2626 only, T_A = –40°C to 125°C			0.6	±4	
PSRR	Power-supply rejection ratio	2.7 V ≤ (V+) ≤ 5 V		100			dB
			T_A = –40°C to 125°C	90	120		
I_B	Input bias current				2	4	µA
		T_A = –40°C to 125°C				5.7	
		OPA2626 only, T_A = –40°C to 125°C				6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to 125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to 125°C				150	
		OPA2626 only, T_A = –40°C to 125°C				350	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to 125°C			0.6		nA/°C
OPEN LOOP GAIN							
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to 125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	106	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	110	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to 125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to 125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 1.2		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.5		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to 125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to 125°C			40	
I_{sc}	Short-circuit current				130		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA,			2	2.2	mA
			T_A = –40°C to 125°C			3.1	

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6.6 Electrical Characteristics: Low-Supply

at T_A = 25°C, V+ = 2.7 V, V– = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Unity gain frequency	V_O = 10 mV_{PP}			76		MHz
φ_m	Phase margin				50		Degrees
GBW	Gain-bandwidth product	G = 100, V_O = 10 mV_{PP}			110		MHz
SR	Slew rate	V_O = 1-V step, G = 2			45		V/µs
t_{settle}	Settling time	V_O = 1-V step, G = 2	to 0.1%		80		ns
			to 0.01%		170		
			to 0.000763% (17-bit accuracy)		250		
	Overshoot	V_O = 1-V step, G = 2			6%		
	Undershoot	V_O = 1-V step, G = 2			5%		
HD2	Second order harmonic Distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		136		dBc
			f = 100 kHz		118		
			f = 1 MHz		80		
HD3	Third order harmonic Distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}	f = 10 kHz		143		dBc
			OPA2625 only, f = 10 kHz		143		
			f = 100 kHz		130		
			OPA2625 only, f = 100 kHz		125		
			f = 1 MHz		85		
			OPA2625 only, f = 1 MHz		74		
	Second order inter-modulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1 V, V_O = 2 V_{PP}, f = 1 MHz, 200-kHz tone spacing			95		dBc
	Third order inter-modulation distortion	(V+) = 3.3 V, (V–) = 0 V, V_{COM} = 1.1V, V_O = 1 V_{PP}, f = 1 MHz, 200-kHz tone spacing			104		dBc
V_N	Input noise voltage	f = 0.1 Hz to 10 Hz peak to peak			0.8		μV_{PP}
		f = 0.1 Hz to 10 Hz rms			120		nV_{RMS}
V_n	Input voltage noise density	f = 10 kHz			2.5		nV/√Hz
I_n	Input current noise density	f = 10 kHz			3.5		pA/√Hz
t_{OR}	Overload recovery time	G = 5			35		ns
Z_o	Open-loop output impedance	f = 1 MHz			1.3		Ω
	Crosstalk	DC			150		dB
		f = 1 MHz			127		
DC PERFORMANCE							
V_{OS}	Input offset voltage				15	±100	µV
		T_A = –40°C to 125°C				±300	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C			0.5	±3.1	µV/°C
		OPA2626 only, T_A = –40°C to 125°C			0.6	±4	
I_B	Input bias current				2	4	µA
		T_A = –40°C to 125°C				5.7	
		OPA2626 only, T_A = –40°C to 125°				6.5	
dI_B/dT	Input bias current drift	T_A = –40°C to 125°C			15		nA/°C
I_{OS}	Input offset current				20	120	nA
		T_A = –40°C to 125°C				150	
		OPA2626 only, T_A = –40°C to 125°				200	
dI_{OS}/dT	Input offset current drift	T_A = –40°C to 125°C			80		pA/°C
OPEN-LOOP GAIN							

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Electrical Characteristics: Low-Supply (continued)

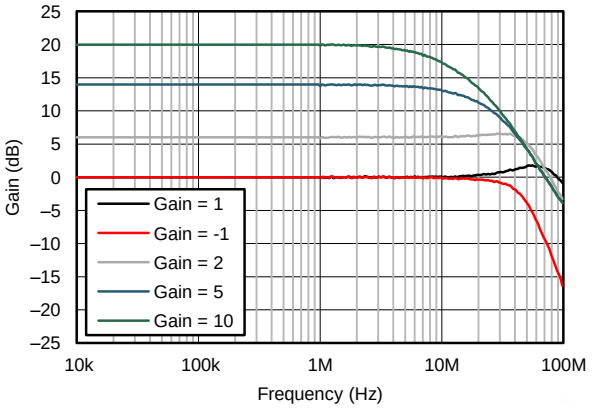
at T_A = 25°C, V+ = 2.7 V, V– = 0 V, V_{COM} = V_O = 1.35 V, gain (G) = 1, R_F = 1 kΩ, C_F = 2.7 pF, C_{LOAD} = 20 pF, and R_{LOAD} = 1 kΩ connected to 1.35 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω		110			dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		114			
		T_A = –40°C to 125°C	(V–) + 0.2 V < V_O < (V+) – 0.2 V, R_{LOAD} = 600 Ω	100	128		
			(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ	104	132		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to 125°C		(V–)		(V+) – 1.15	V
CMRR	Common-mode rejection ratio	(V–) < V_{COM} < (V+) – 1.15 V		100	117		dB
			T_A = –40°C to 125°C	90	115		
INPUT IMPEDANCE							
Z_{ID}	Differential input impedance				27 || 0.8		KΩ || pF
Z_{IC}	Common-mode input impedance				47 || 1.2		MΩ || pF
OUTPUT							
	Output voltage swing to the rail	R_{LOAD} = 600 Ω			60	80	mV
			T_A = –40°C to 125°C			100	
		R_{LOAD} = 10 kΩ			20	35	
			T_A = –40°C to 125°C			40	
I_{SC}	Short-circuit current				80		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			2	2.1	mA
			T_A = –40°C to 125°C			2.8	

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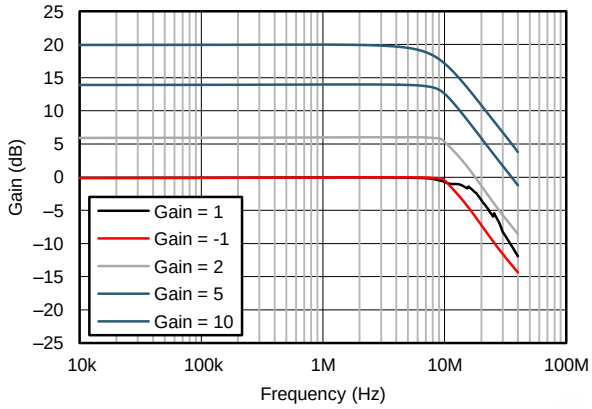
6.7 Typical Characteristics

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



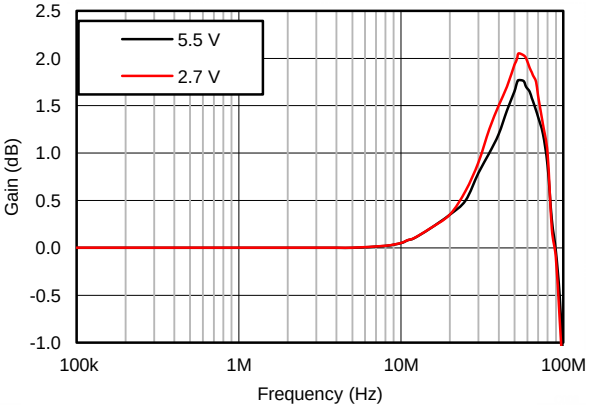
V_O = 10 mV_{PP}

图 1. Small-Signal Frequency Response for Various Gains



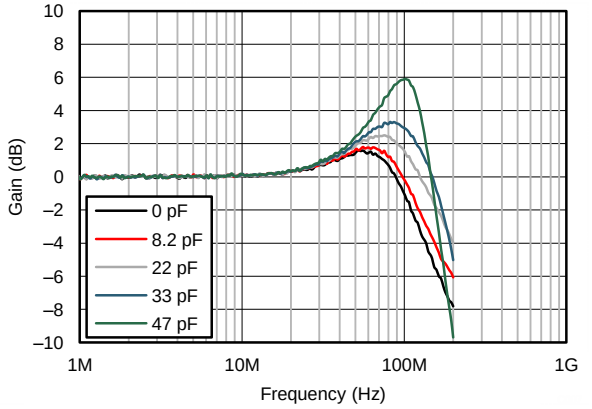
V_O = 2 V_{PP}

图 2. Large-Signal Frequency Response for Various Gains



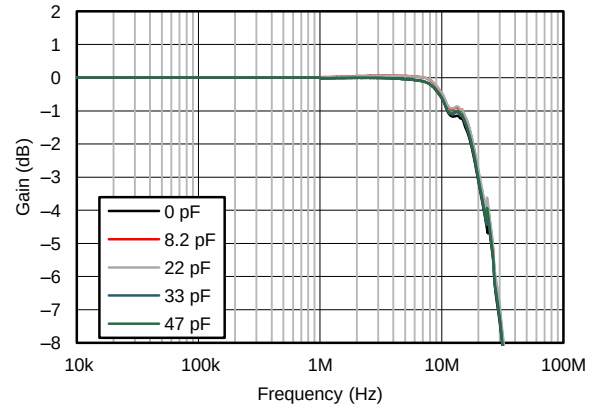
V_O = 10 mV_{PP}, G = 1

图 3. Small-Signal Frequency Response for Various Power Supply Voltages



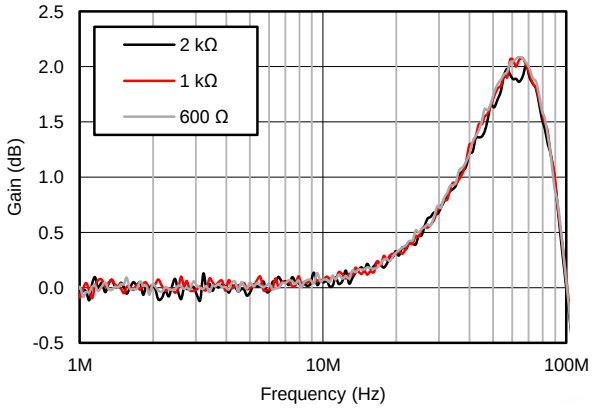
V_O = 10 mV_{PP} , G = 1

图 4. Small-Signal Frequency Response for Various Capacitive Loads



V_O = 2 V_{PP}, G = 1

图 5. Large-Signal Frequency Response for Various Capacitive Loads



V_O = 10 mV_{PP} , G = 1

图 6. Small-Signal Frequency Response for Various Resistive Loads

Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

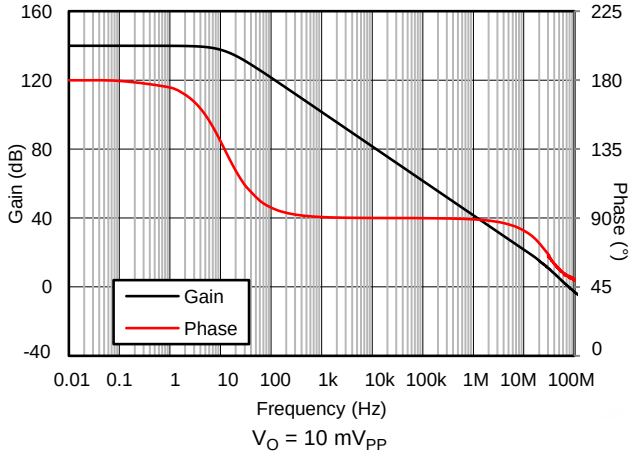


图 7. Open-Loop Gain and Phase vs Frequency

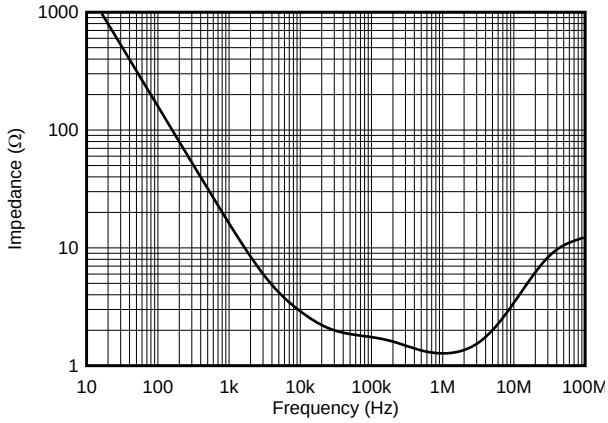


图 8. Open-Loop Output Impedance vs Frequency

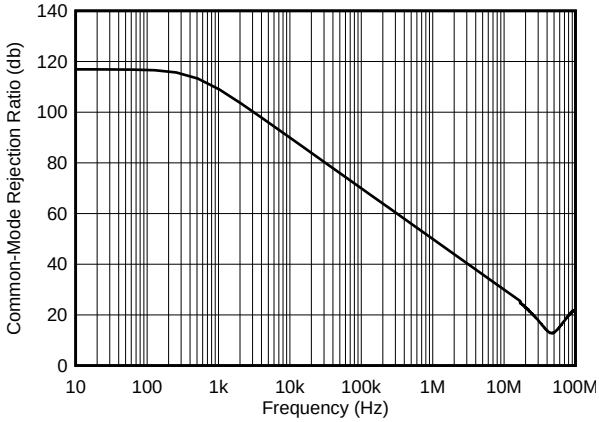


图 9. Common-Mode Rejection Ratio vs Frequency

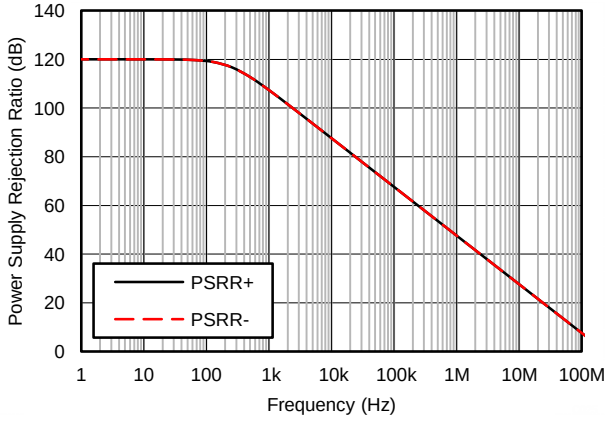


图 10. Power-Supply Rejection Ratio vs Frequency

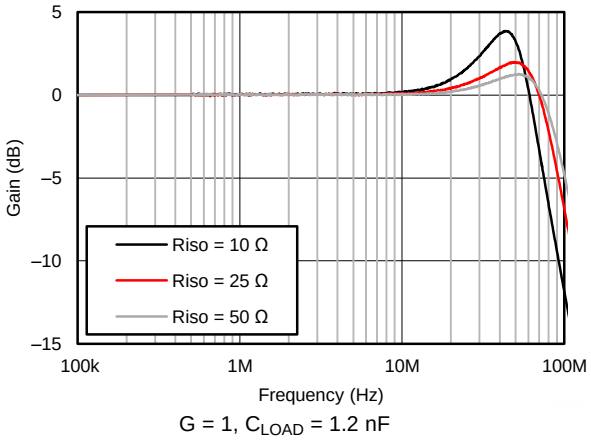


图 11. Series Resistance for Capacitive Load Stability

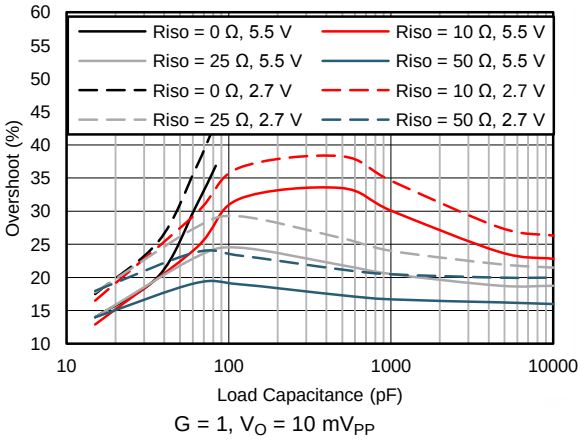
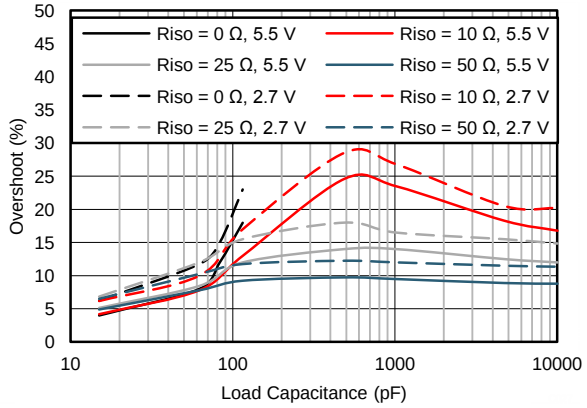


图 12. Overshoot vs Capacitive Load, G = 1

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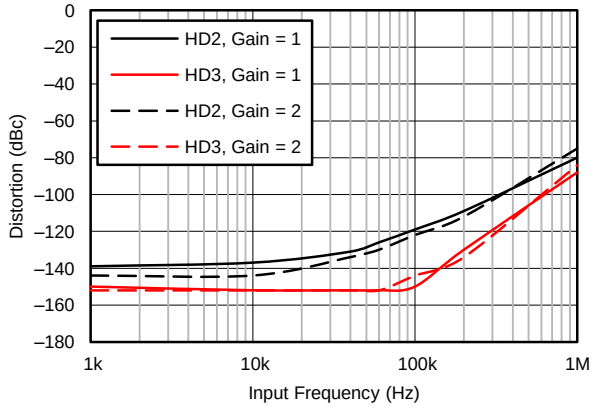
Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



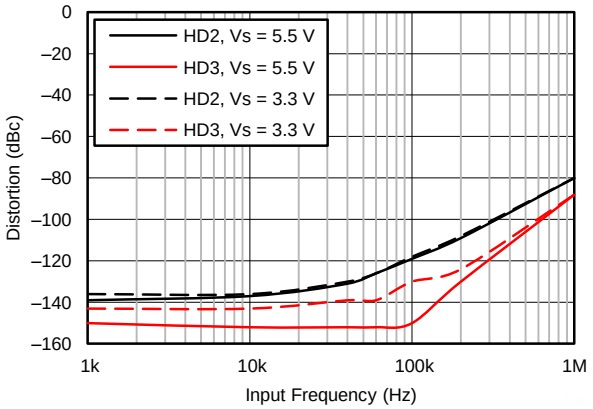
G = –1, V_O = 10 mV_{PP}

图 13. Overshoot vs Capacitive Load, G = –1



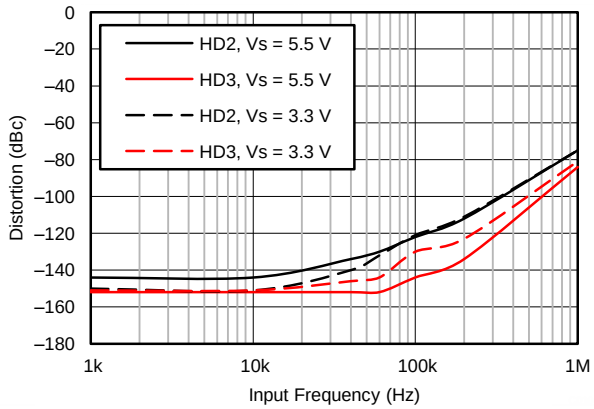
V_S = 5.5 V, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

图 14. Distortion vs Frequency for Various Gains



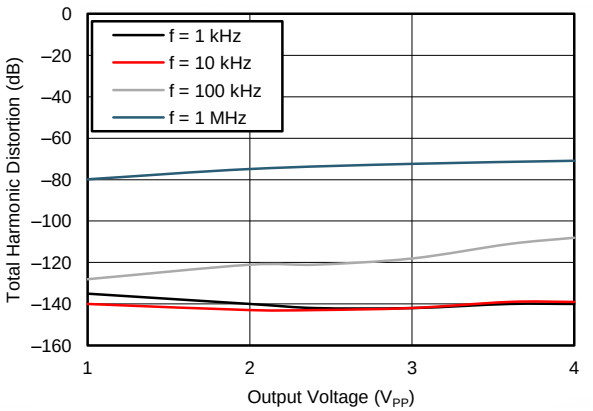
G = 1, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

图 15. Distortion vs Frequency for Various Power Supplies



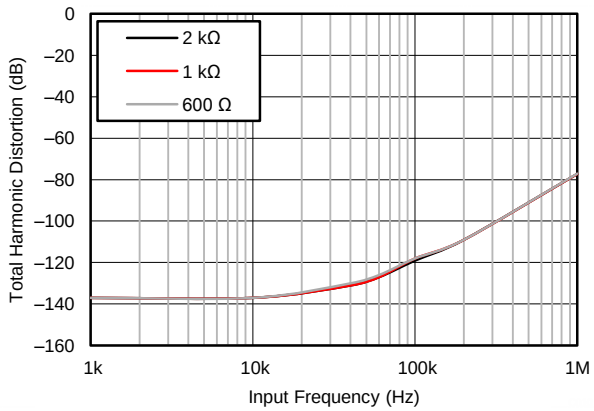
G = 2, V_O = 2 V_{PP}, R_{LOAD} = 600 Ω

图 16. Distortion vs Frequency for Various Power Supplies



G = 1, R_{LOAD} = 600 Ω

图 17. Total Harmonic Distortion vs Output Voltage for Various Frequencies



G = 1, V_O = 2 V_{PP} , R_{LOAD} = 600 Ω

图 18. Total Harmonic Distortion vs Frequency for Various Loads

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Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

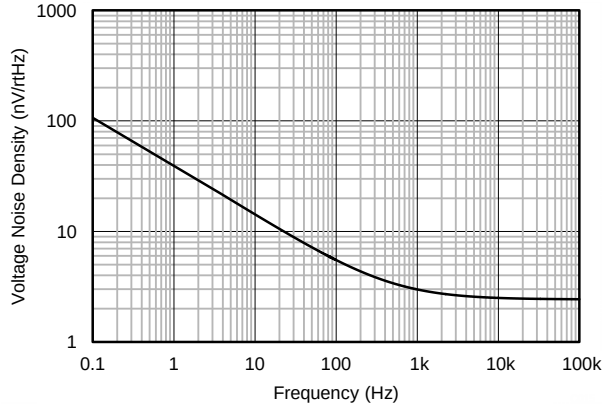


图 19. Voltage Noise Density vs Frequency

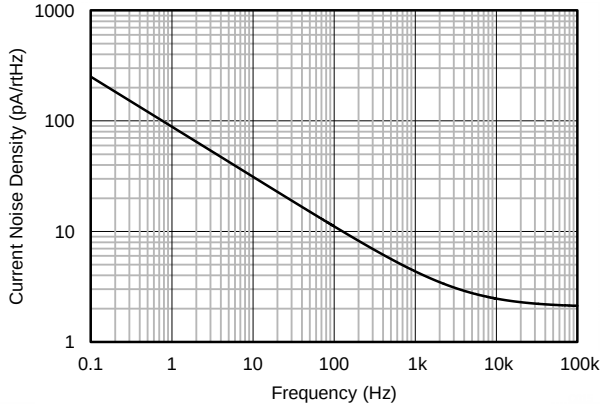


图 20. Current Noise Density vs Frequency

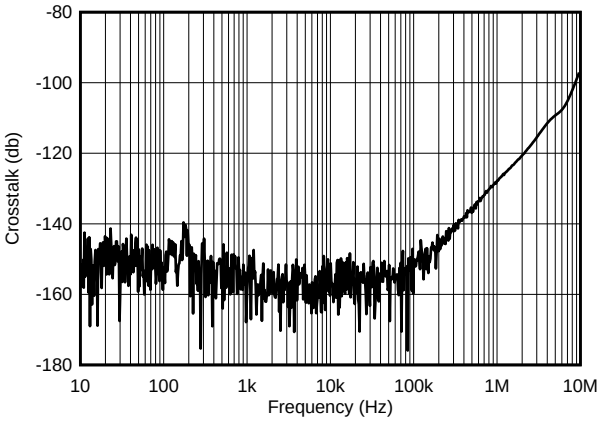


图 21. Crosstalk vs Frequency

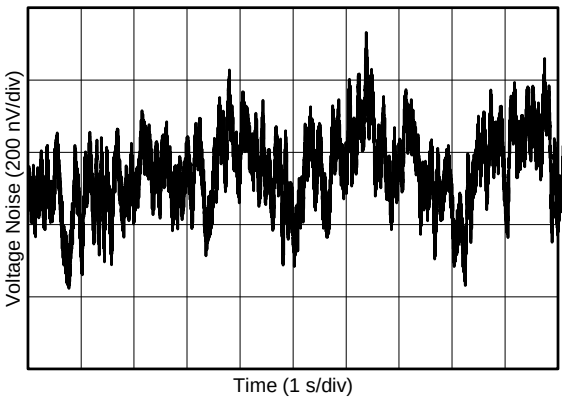


图 22. 0.1-Hz to 10-Hz Voltage Noise

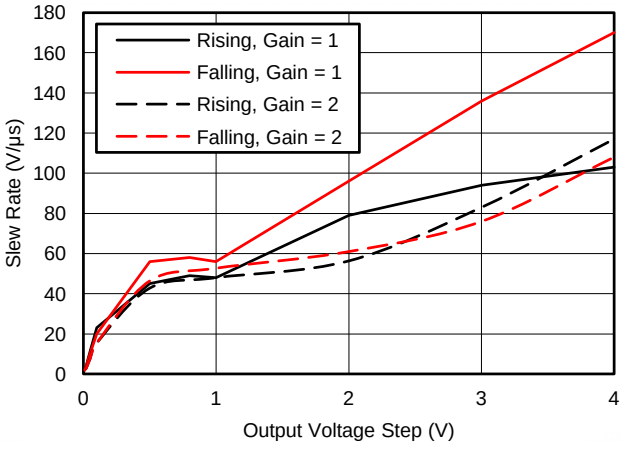


图 23. Slew Rate vs Output Step Size

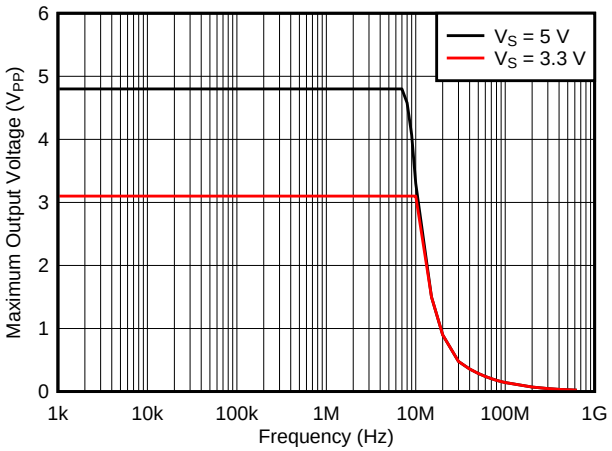
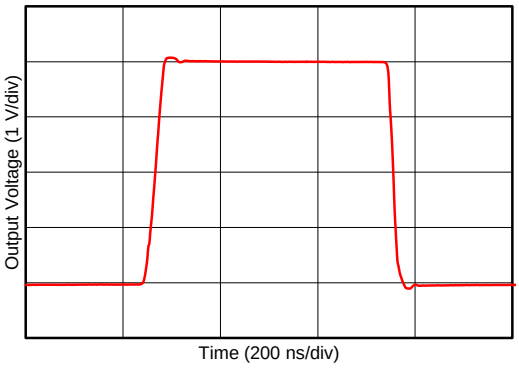


图 24. Maximum Output Voltage vs Frequency

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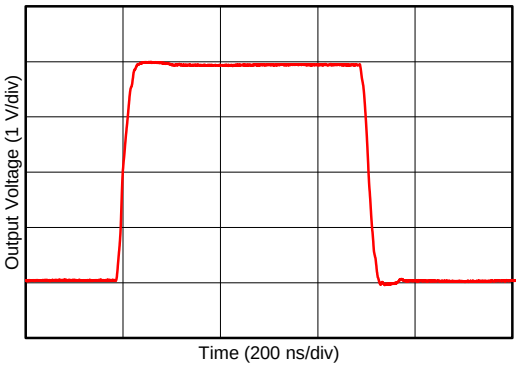
Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



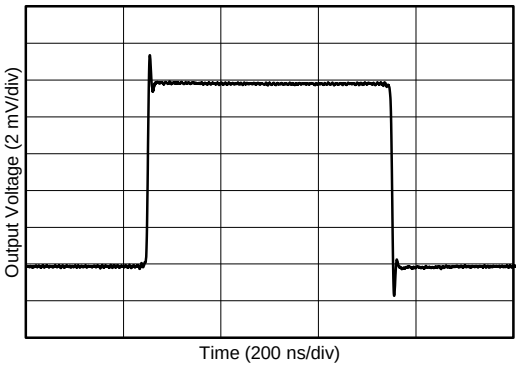
G = 1, V_O = 4-V step

图 25. Large-Signal Pulse Response



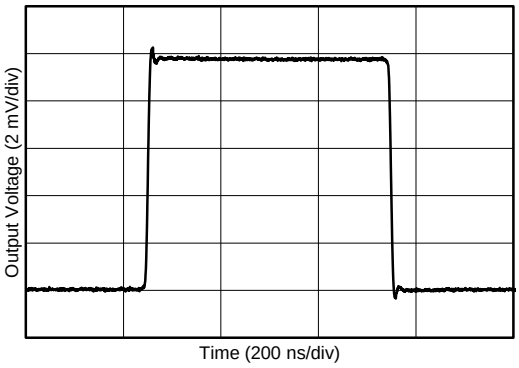
G = –1, V_O = 4-V step

图 26. Large-Signal Pulse Response



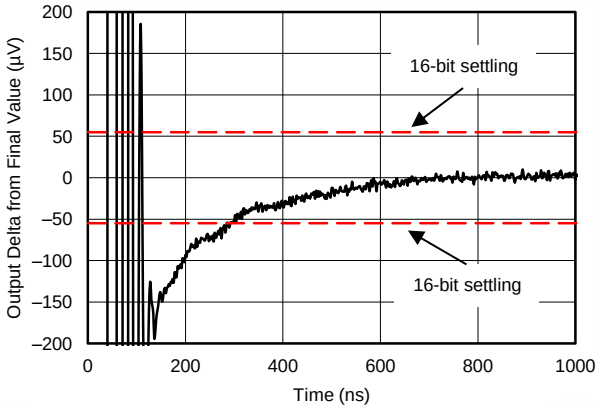
G = 1, V_O = 10-mV step

图 27. Small-Signal Pulse Response



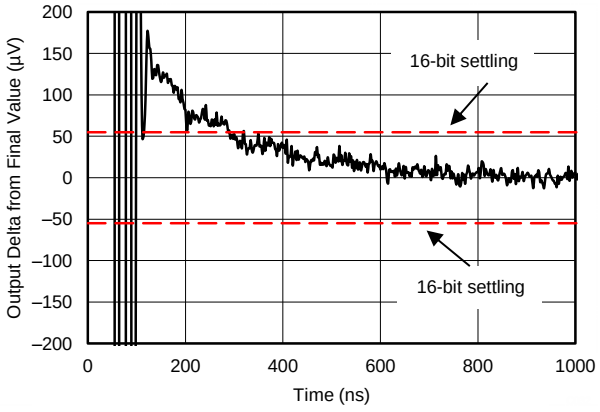
G = –1, V_O = 10-mV step

图 28. Small-Signal Pulse Response



V_O = 3.6-V step at t = 0 s

图 29. 16-Bit Negative Settling Time

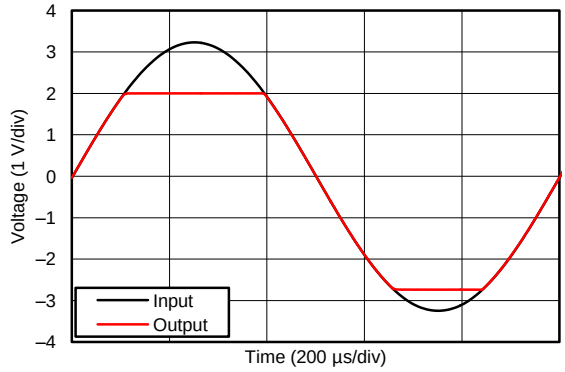


V_O = 3.6-V step at t = 0 s

图 30. 16-Bit Positive Settling Time

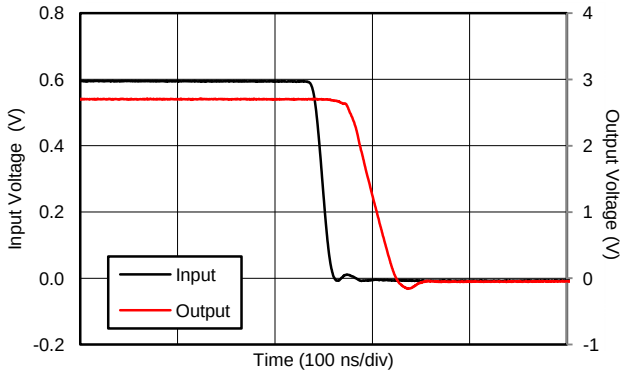
Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



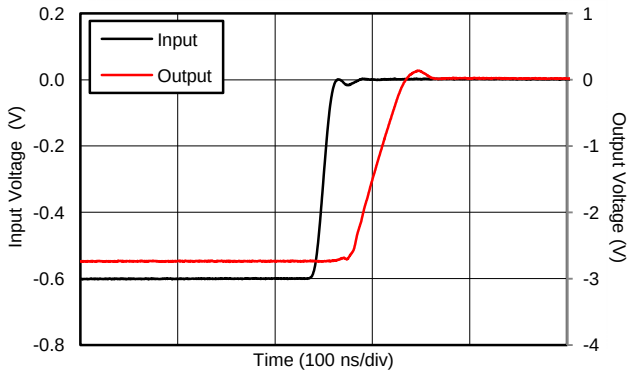
V_S = ±2.75 V, G = 1

图 31. No Phase Reversal



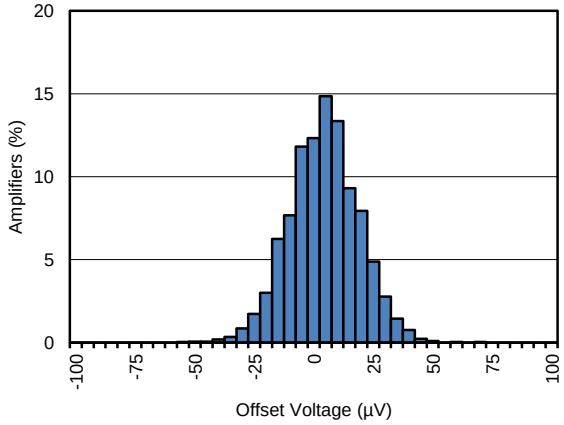
V_S = ±2.75 V, G = 5

图 32. Positive Overload Recovery



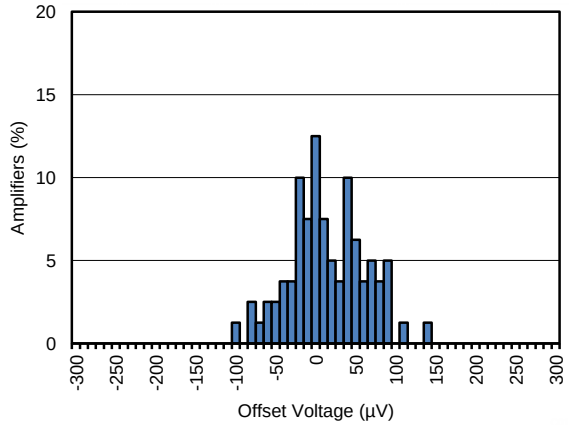
V_S = ±2.75 V, G = 5

图 33. Negative Overload Recovery



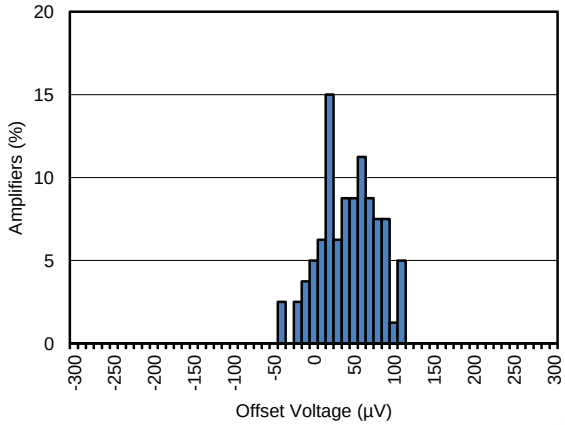
Distribution taken from 3139 amplifiers, T_A = 25°C

图 34. Input Offset Voltage Distribution



Distribution taken from 80 amplifiers, T_A = 125°C

图 35. Input Offset Voltage Distribution



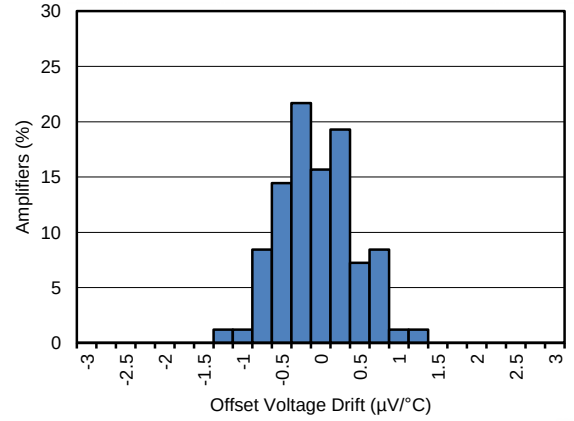
Distribution taken from 80 amplifiers, T_A = –40°C

图 36. Input Offset Voltage Distribution

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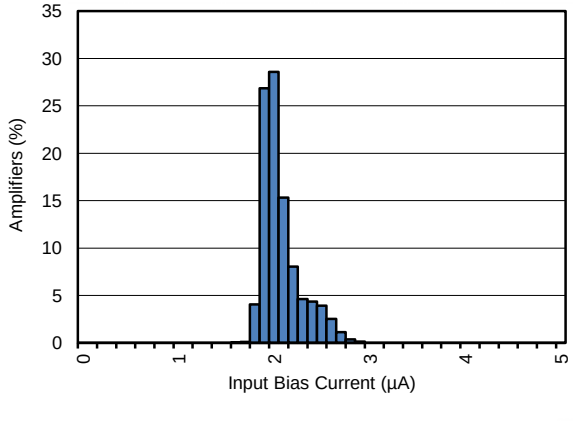
Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



Distribution taken from 75 amplifiers, T_A = –40°C to +125°C

图 37. Input Offset Voltage Drift Distribution



Distribution taken from 3139 amplifiers

图 38. Input Bias Current Distribution

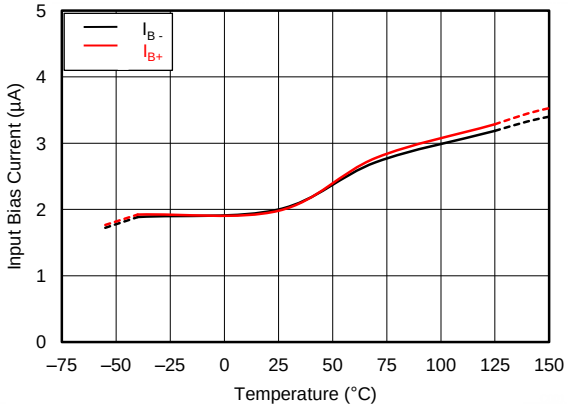
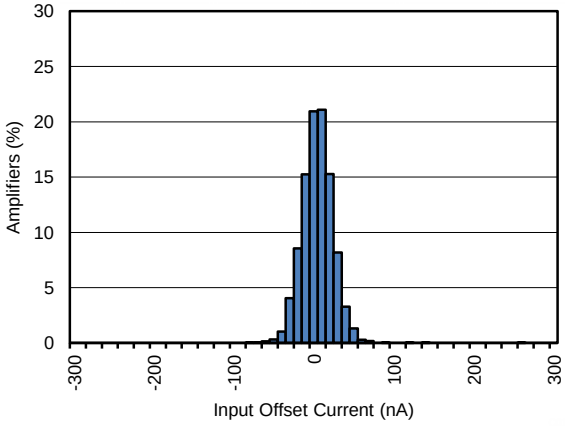


图 39. Input Bias Current vs Temperature



Distribution taken from 3139 amplifiers

图 40. Input Offset Current Distribution

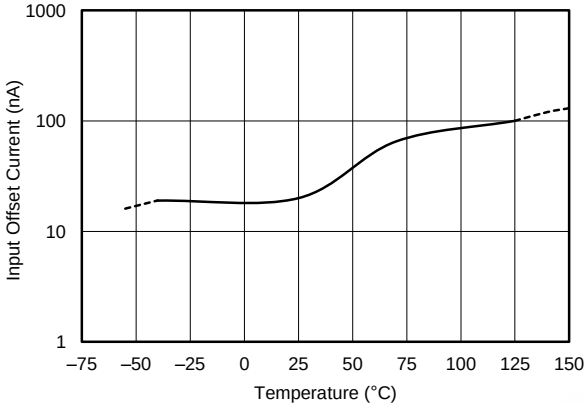


图 41. Input Offset Current vs Temperature

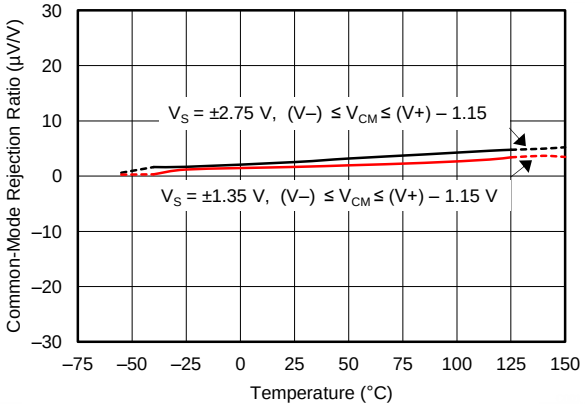
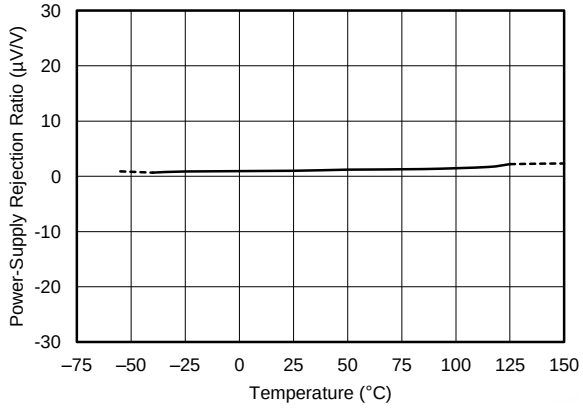


图 42. Common-Mode Rejection Ratio vs Temperature

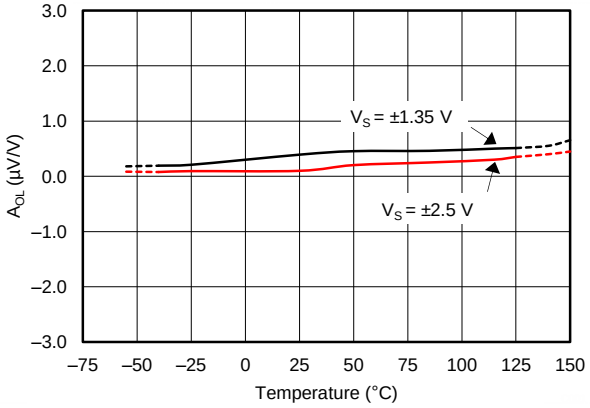
Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)



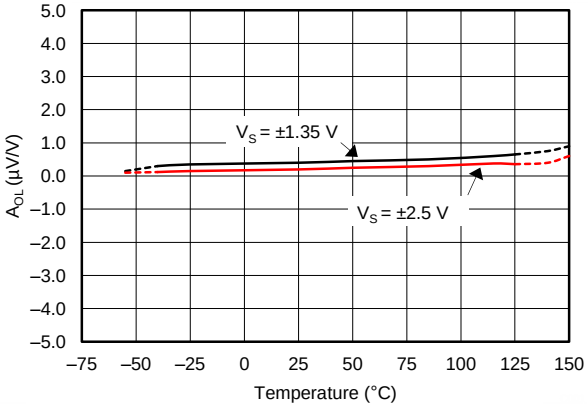
2.7 V ≤ V_S ≤ 5.5 V

图 43. Power-Supply Rejection Ratio vs Temperature



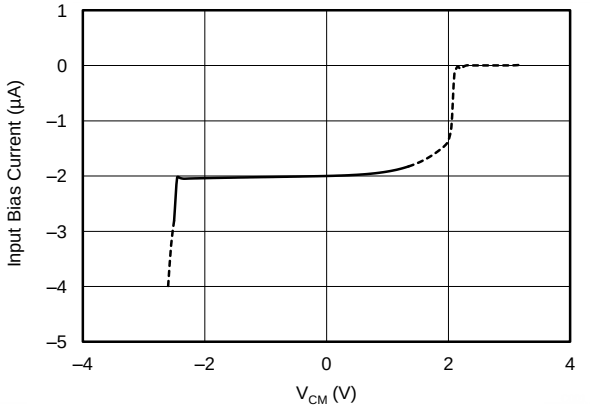
R_{LOAD} = 10 kΩ

图 44. Open-Loop Gain vs Temperature with 10-kΩ Load



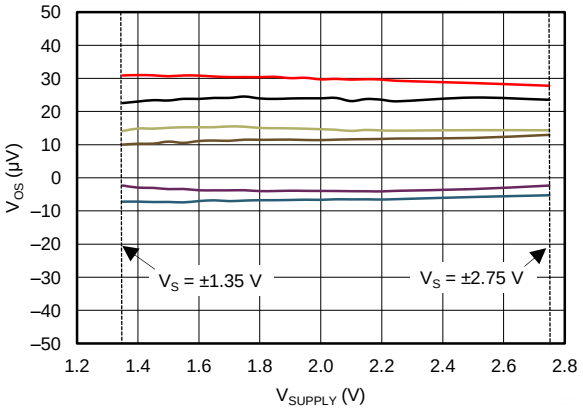
R_{LOAD} = 600 Ω

图 45. Open-Loop Gain vs Temperature with 600-Ω Load



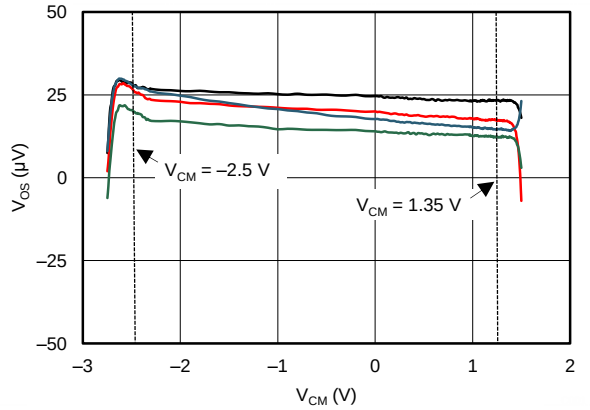
V_S = ±2.5 V

图 46. Input Bias Current vs Input Common-Mode Voltage



6 typical units shown, V_S = ±1.35 V to ±2.75 V

图 47. Input Offset Voltage vs Power-Supply Voltage



6 typical units shown, V_S = ±2.5 V

图 48. Input Offset Voltage vs Common-Mode Voltage

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Typical Characteristics (接下页)

at T_A = 25°C, V+ = 5 V, V– = 0 V, V_{COM} = V_O = 2.5 V, gain (G) = 2, R_F = 1 kΩ, C_F= 2.7 pF, C_{LOAD}= 20 pF, and R_{LOAD} = 2 kΩ connected to 2.5 V (unless otherwise noted)

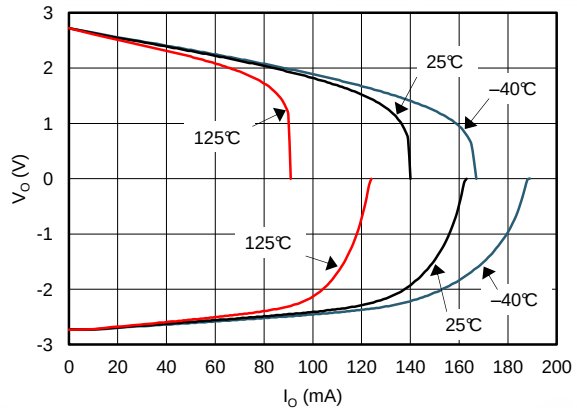


图 49. Output Voltage vs Output Current

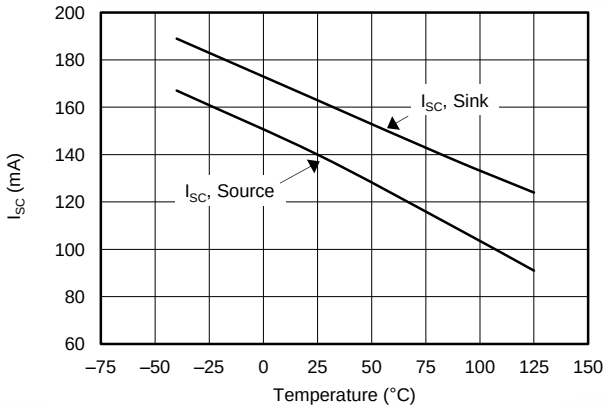


图 50. Short-Circuit Current vs Temperature

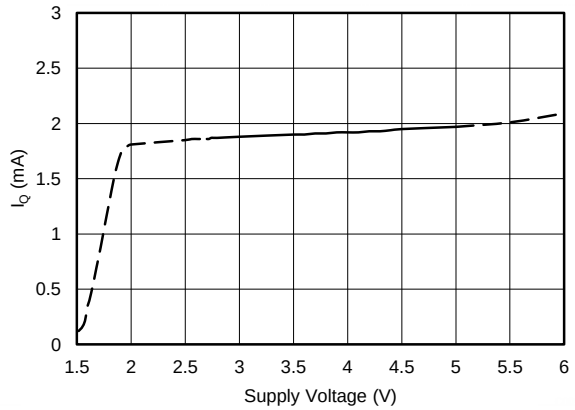


图 51. Quiescent Current vs Power-Supply Voltage

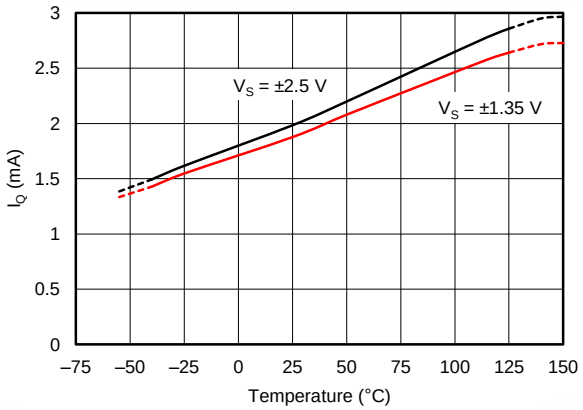
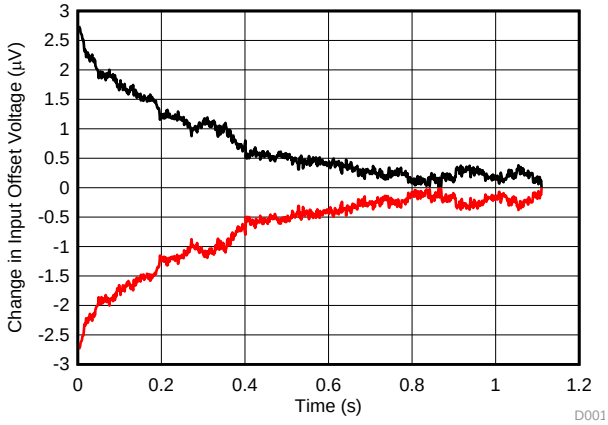


图 52. Quiescent Current vs Temperature



OPA626 powered on at t = 0 s, PCB dimensions: 4 in^2, 2 layer, FR4

图 53. Warm-Up Time

7 Parameter Measurement Information

7.1 DC Parameter Measurements

The circuit shown in 图 54 measures the dc input offset related parameters of the OPAx626 family. Input offset voltage, power supply rejection ratio, common-mode rejection ratio and open loop gain can be measured with this circuit. The basic test procedure requires setting the inputs (the power-supply voltage, V_S, and the common-mode voltage, V_{CM}), to the desired values. V_O is set to the desired value by adjusting the loop-drive voltage while measuring V_O. After all inputs are configured, measure the input offset at the V_X measurement point. Calculate the input offset voltage by dividing the measured result by 101. Changing the voltages on the various inputs changes the input offset voltage. The input parameters can be measured according to the relationships illustrated in 公式 1 through 公式 5.

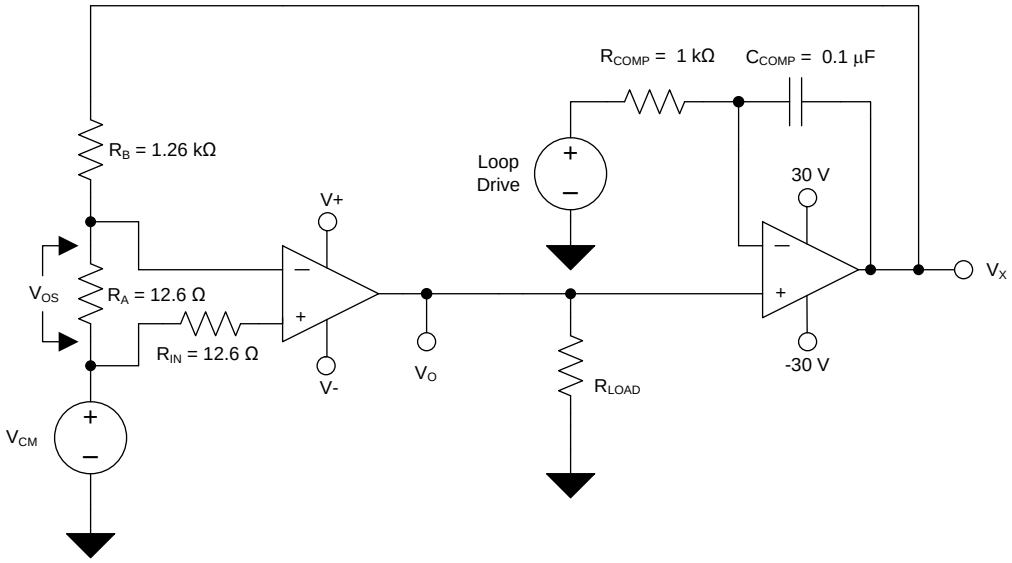


图 54. DC-Parameters Measurement Circuit

$$V_{OS} = \frac{V_X}{101} \quad (1)$$

$$V_{OSDrift} = \frac{\Delta V_{OS}}{\Delta Temperature} \quad (2)$$

$$PSRR = \frac{\Delta V_{OS}}{\Delta V_{SUPPLY}} \quad (3)$$

$$CMRR = \frac{\Delta V_{OS}}{\Delta V_{CM}} \quad (4)$$

$$AOL = \frac{\Delta V_O}{\Delta V_{OS}} \quad (5)$$

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7.2 Transient Parameter Measurements

The circuit shown in 图 55 measures the transient response of the OPAx626 family. Configure V+, V–, R_{ISO}, R_{LOAD}, and C_{LOAD} as desired. Monitor the input and output voltages on an oscilloscope or other signal analyzer. Use this circuit to measure large-signal and small-signal transient response, slew rate, overshoot, and capacitive-load stability.

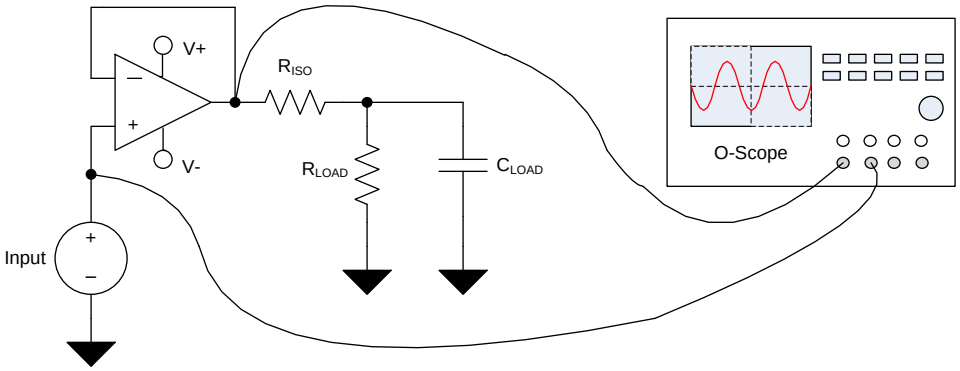


图 55. Pulse-Response Measurement Circuit

7.3 AC Parameter Measurements

The circuit shown in 图 56 measures the ac parameters of the OPAx626 family. Configure V+, V–, and C_{LOAD} as desired. The THS4271 family is used to buffer the input and output of the OPAx626 family to prevent loading by the gain phase analyzer. Monitor the input and output voltages on a gain phase analyzer. Use this circuit to measure the gain bandwidth product, and open-loop gain versus frequency versus capacitive load.

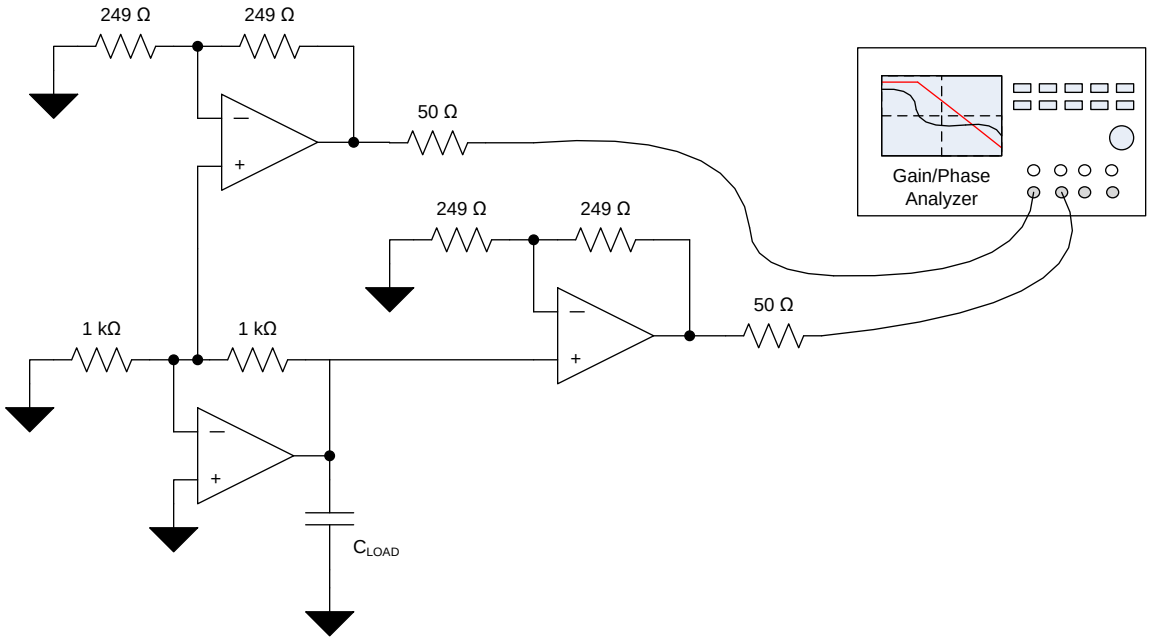


图 56. AC-Parameters Measurement Circuit

7.4 Noise Parameter Measurements

The circuit shown in 图 57 measures the voltage noise of the OPAx626 family. Configure V+, V–, and C_{LOAD} as desired.

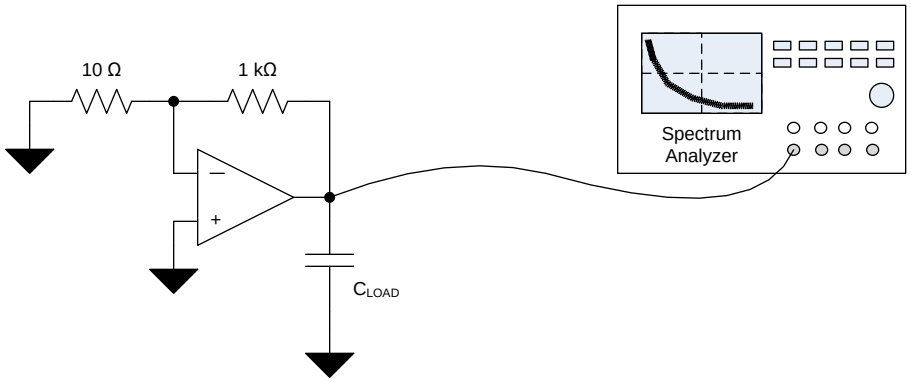


图 57. Voltage Noise Measurement Circuit

The circuit shown in 图 58 measures the current noise of the OPAx626 family. Configure V+, V– and C_{LOAD} as desired.

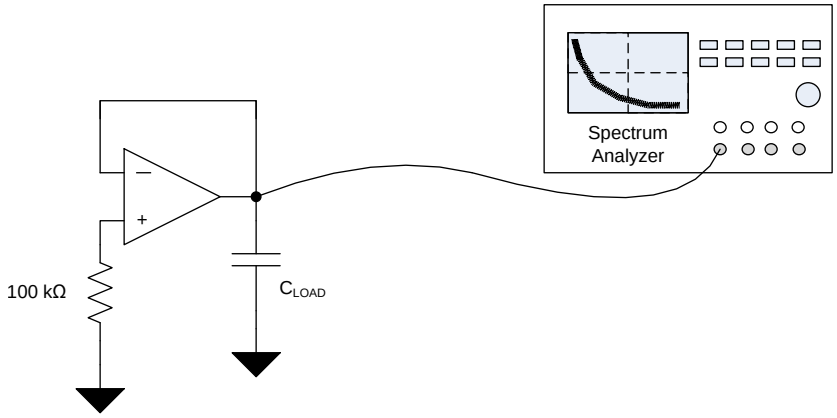


图 58. Current Noise Measurement Circuit

The circuit shown in 图 59 measures the 0.1-Hz to 10-Hz voltage noise of the OPAx626 family . Configure V+, V–, and C_{LOAD} as desired.

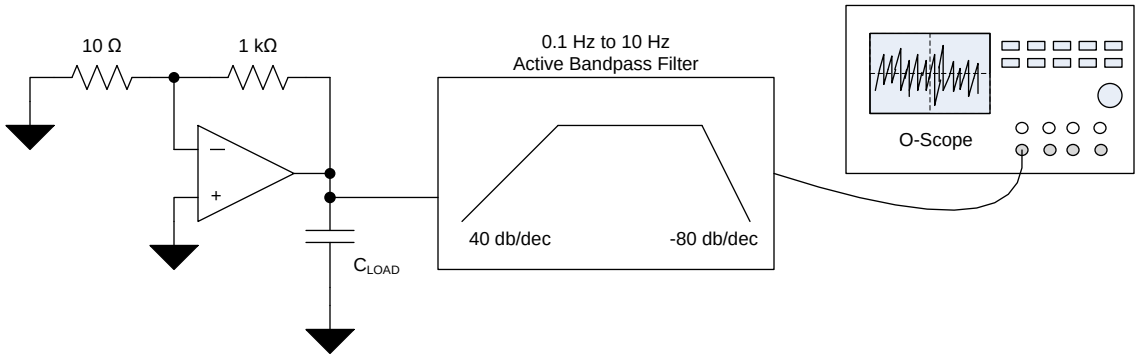


图 59. 0.1-Hz to 10-Hz Voltage-Noise Measurement Circuit

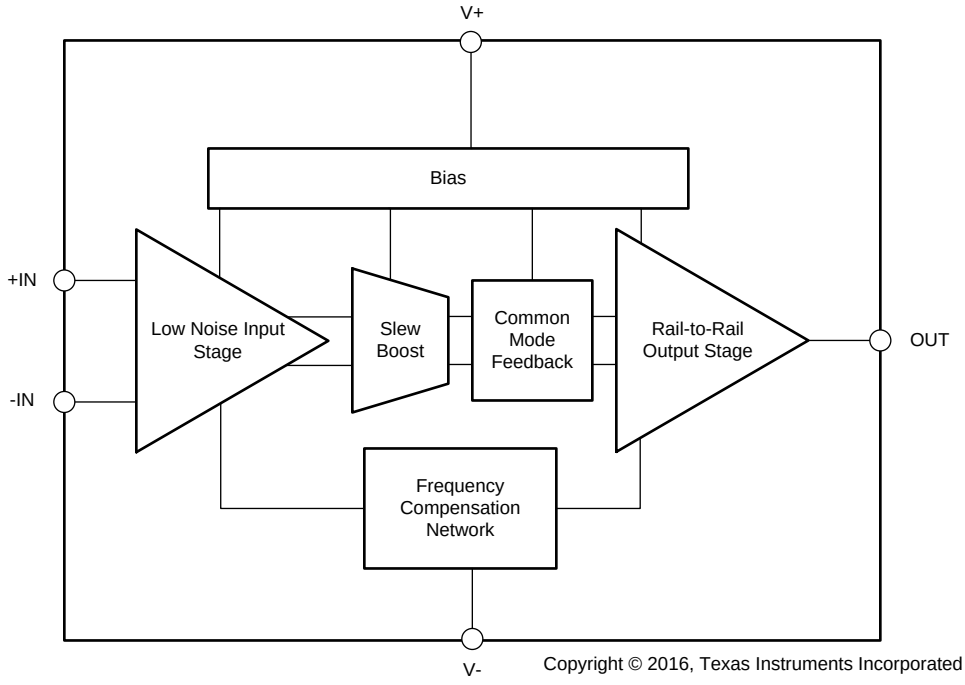
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8 Detailed Description

8.1 Overview

The OPAx626 family **consists of** fast-settling, high slew rate, high-bandwidth, voltage-feedback operational amplifiers. Low offset and low offset drift combine with the superior dynamic performance and low output impedance, resulting in an amplifier suited for driving 16-bit SAR ADCs, and buffering precision voltage references in industrial applications. The OPAx626 family **consists of** low-noise input, slew boost, and rail-to-rail output stages.

8.2 Functional Block Diagram



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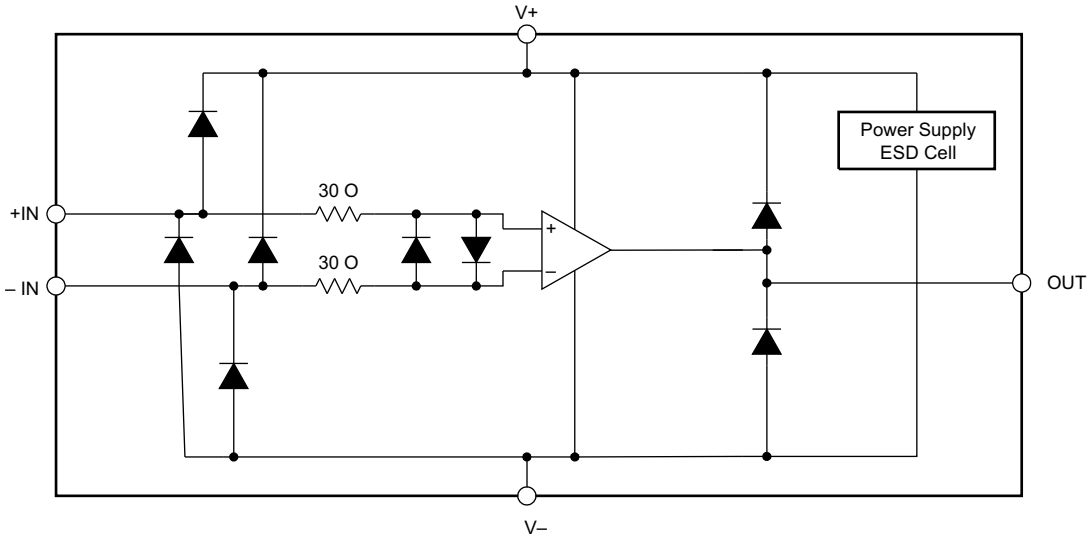
8.3 Feature Description

8.3.1 SAR ADC Driver

The OPAx626 family is designed to drive precision (16-bit and 18-bit) SAR ADCs at sample rates up to 1 MSPS. The combination of low output impedance, low THD, low noise, and fast settling time make the OPAx626 family the ideal choice for driving both the SAR ADC inputs, as well as the reference input to the ADC. Internal slew boost circuitry increases the slew rate as a function of the input signal magnitude, resulting in settling from a 4-V step input to 16-bit levels within 280 ns. Low output impedance (1 Ω at 1 MHz) ensures capacitive load stability with minimal overshoot.

8.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly. A good understanding of this basic ESD circuitry and how the ESD circuitry relates to an electrical overstress event is helpful. (See 图 60 for an illustration of the ESD circuits contained in the OPAx626 family). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



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图 60. Simplified ESD Circuit

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8.4 Device Functional Modes

The OPAx626 family has a single functional mode and is operational when the power supply voltage, V_S, is between 2.7 V (±1.35 V) and 5.5 V (±2.75 V).

8.4.1 High-Drive Mode

The OPAx626 family has 120-MHz gain bandwidth, 2.5-nV/√Hz input-referred noise, and consumes 2 mA of quiescent current. Additionally, the OPAx626 family has an offset voltage of 100 µV (maximum) and offset voltage drift of 1 µV/°C (typical). This combination of high precision, high speed, and low noise makes this device suitable for use as an input driver for high-precision, high-throughput SAR ADCs such as the ADS88xx family of SAR ADCs, as shown in 图 61.

9 Application and Implementation

注

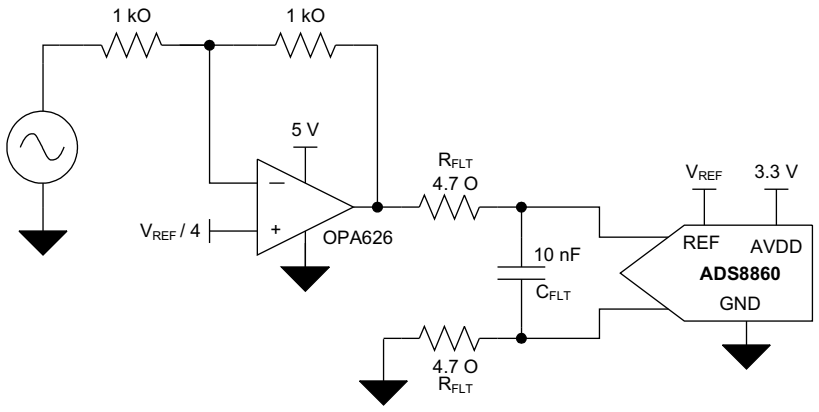
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx626 family consists of precision, high-speed, voltage-feedback operational amplifiers. Fast settling to 16-bit levels, low THD, and low noise make the OPAx626 family suitable for driving SAR ADC inputs and buffering precision voltage references. With a wide power-supply voltage range from 2.7 V to 5.5 V, and operating from –40°C to +125°C, the OPAx626 family is suitable for a variety of high-speed, industrial applications. The following sections show application information for the OPAx626 family. For simplicity, power-supply decoupling capacitors are not shown in these diagrams.

9.2 Typical Applications

9.2.1 Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver



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图 61. Single-Supply, 16-Bit, 1-MSPS SAR ADC Driver

9.2.1.1 Design Requirements

An SAR ADC, such as the ADS8860 device, uses sampling capacitors on the data converter input. During the signal acquisition phase, these sampling capacitors are connected to the ADC analog input terminals, AINP and AINN, through a set of switches. After the acquisition period has elapsed, the internal sampling capacitors are disconnected from the input terminals and connected to the ADC input through a second set of switches, during this period the ADC is performing the analog-to-digital conversion. 图 62 illustrates this architecture.

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Typical Applications (接下页)

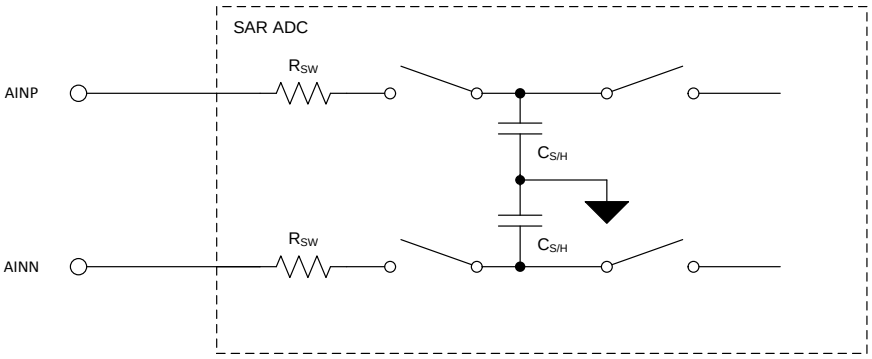


图 62. Simplified SAR ADC Input

The SAR ADC inputs and sampling capacitors must be driven by the OPA626 device to 16-bit levels within the acquisition time of the ADC. For the example illustrated in 图 61, the OPA626 device is used to drive the ADS8860 device at a sample rate of 1 MSPS.

9.2.1.2 Detailed Design Procedure

The circuit illustrated in 图 61 consists of the SAR ADC driver, a low-pass filter and the SAR ADC. The SAR ADC driver circuit consists of an OPA626 device configured in an inverting gain of 1. The filter consists of R_{FLT} and C_{FLT}, connected between the OPA626 output and the ADS8860 input. Selecting the proper values for each of these passive components is critical to obtain the best performance from the ADC. Capacitor C_{FLT} serves as a charge reservoir, providing the necessary charge to the ADC sampling capacitors. The dynamic load presented by the ADC creates a glitch on the filter capacitor, C_{FLT}. To minimize the magnitude of this glitch, choose a value for C_{FLT} large enough to maintain a glitch amplitude of less than 100 mV. Maintaining such a low glitch amplitude at the amplifier output makes sure that the amplifier remains in the linear operating region, and results in a minimum settling time. Using 公式 6, a 10-nF capacitor is selected for C_{FLT}.

$$C_{FLT} \geq 15 \times C_{SH} \tag{6}$$

Connecting a 10-nF capacitor directly to the OPA626 output degrades the OPA626 phase margin and results in stability and settling-time problems. To properly drive the 10-nF capacitor, use a series resistor (R_{FLT}) to isolate the capacitor, C_{FLT}, from the OPA626 device. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, consider the impact upon the THD due to the voltage divider effect from R_{FLT} reacting with the switch resistance (R_{SW}) of the ADC input circuit, as well as the impact of the output impedance upon amplifier stability. In this example, 4.7-Ω resistors are selected. In this design example, 图 13 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, and in this example is equivalent to 2 × R_{FLT}.

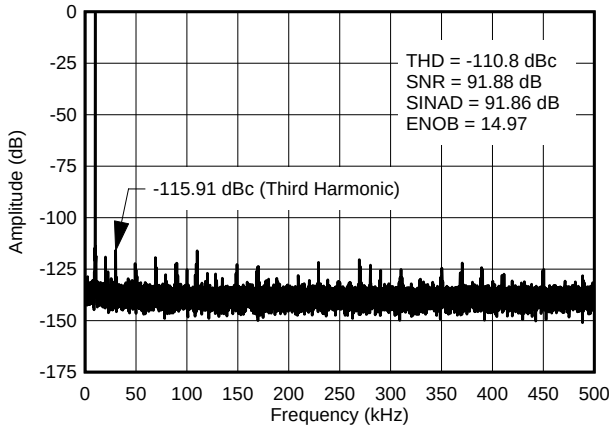
TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design, TIDU014, "Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design".

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9.2.1.3 Application Curves

图 63 illustrates the performance of the circuit shown in 图 61.



4096-point FFT at 1 MSPS, f_{IN} = 10 kHz , V_{IN} = 1.5 V_{RMS}

图 63. ADC Output FFT for 图 61

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9.2.2 Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

In order to operate a high-resolution, 16-bit ADC at its maximum throughput, the full-scale voltage step must settle to better than 16-bit accuracy at the ADC inputs within the minimum specified acquisition time (t_{ACQ}). This settling imposes very stringent requirements on the driver amplifier in terms of large-signal bandwidth, slew rate, and settling time. 图 64 illustrates a typical multiplexed ADC driver application using the OPA626 device.

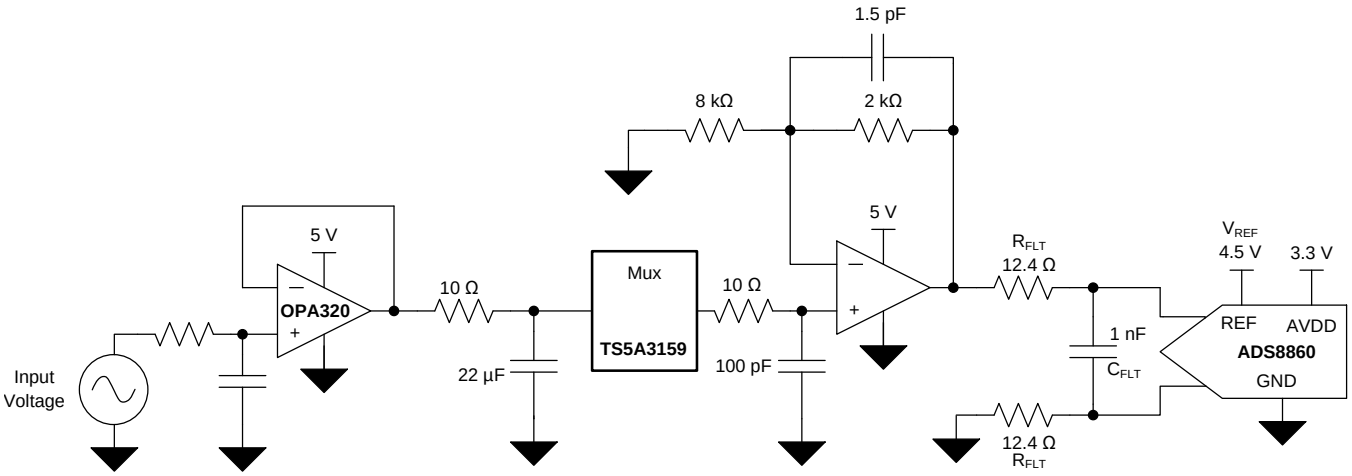


图 64. Single-Supply, 16-Bit, 1-MSPS, Multiplexed, SAR ADC Driver

9.2.2.1 Design Requirements

To optimize this circuit for performance, this design does not allow any large signal input transients at the driver circuit inputs for a small quiet-time period (t_{QT}) towards the end of the previous conversion. The input step voltage can appear anytime from the beginning of conversion (CONVST rising edge) until the elapse of a half cycle time ($0.5 \times t_{CYC}$). This timing constraint on the input step allows a minimum settling time of ($t_{QT} + t_{ACQ}$) for the ADC input to settle within the required accuracy, in the worst-case scenario. This provides more time for the output of the amplifer to slew and settle within the required accuracy before the next conversion starts. 图 65 illustrates this timing sequence.

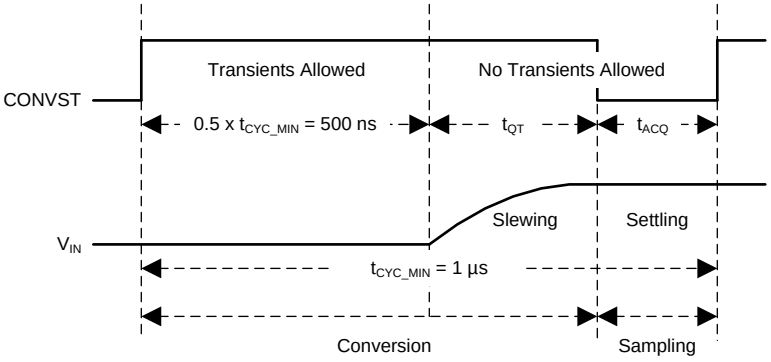


图 65. Timing Diagram for Input Signals

9.2.2.2 Detailed Design Procedure

An ADC input driver circuit consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and the low output impedance provides a buffer between the signal source and the ADC input. The RC filter helps attenuate the sampling charge-injection from the switched-capacitor input stage of the ADC and acts as an anti-aliasing filter to band-limit the wideband noise contributed by the front-end circuit. The design of the ADC input driver involves optimizing the bandwidth of the circuit, driven by the following requirements:

- The $R_{FLT}C_{FLT}$ filter bandwidth must be low to band-limit the noise fed into the input of the ADC thereby increasing the signal-to-noise ratio (SNR) of the system.
- The overall system bandwidth must be large enough to accommodate optimal settling of the input signal at the ADC input before the conversion starts.

C_{FLT} is chosen based upon 公式 7 . C_{FLT} is chosen to be 1 nF.

$$C_{FLT} \geq 15 \times C_{SH} \tag{7}$$

Connecting a 1-nF capacitor directly to the output of the OPA626 device would degrade the OPA626 phase margin and result in stability and settling time problems. To properly drive the 1-nF capacitor, a series resistor, R_{FLT}, is used to isolate the capacitor, C_{FLT}, from the OPA626 device. R_{FLT} must be sized based upon several constraints. To determination a suitable value for R_{FLT}, the system designer must consider the impact upon the THD due to the voltage divider effect from R_{FLT} reacting with the switch resistance, R_{SW}, of the ADC input circuit as well as the impact of the output impedance upon amplifier stability. In this example 12.4-Ω resistors are selected. In this design example, 图 12 can be used to estimate a suitable value for R_{ISO}. R_{ISO} represents the total resistance in series with C_{FLT}, which in this example is equivalent to 2 × R_{FLT}.

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design, TIDU012, "Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design".

9.2.2.3 Application Curves

图 66 illustrates the performance of the circuit shown in 图 64.

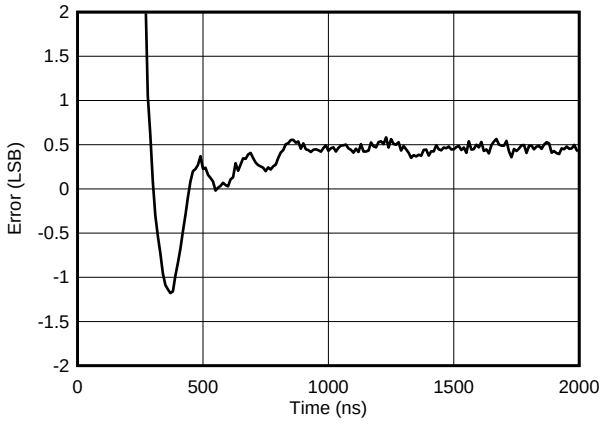


图 66. Positive Transient Response for 图 64

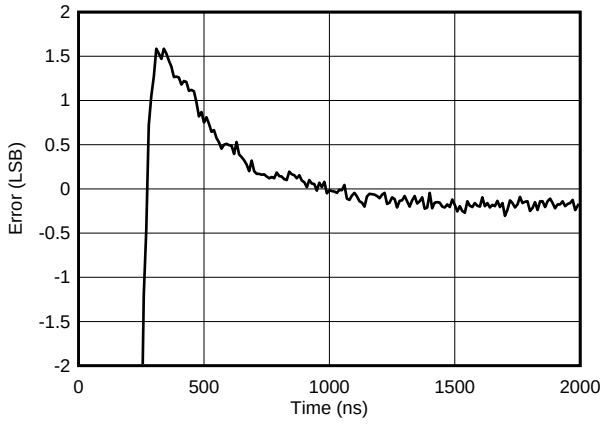


图 67. Negative Transient Response for 图 64

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10 Power Supply Recommendations

The OPAx626 family is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section. Place bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

CAUTION

Supply voltages larger than 6 V can cause permanent damage to the device. See to the section.

11 Layout

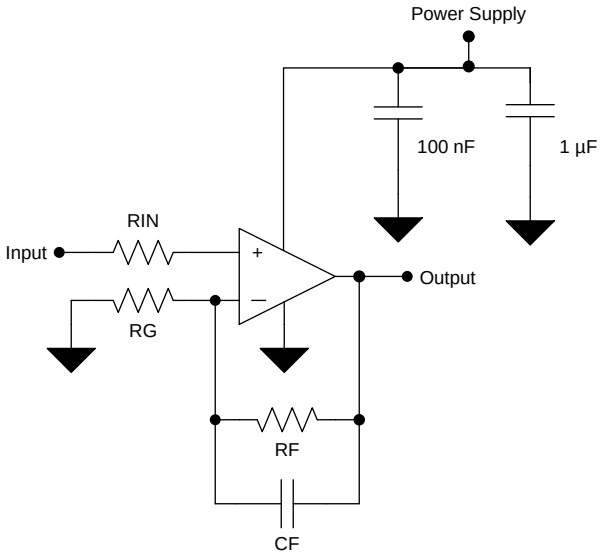
11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Use bypass capacitors to reduce the noise coupled from the power supply. Connect low ESR, ceramic, bypass capacitors between the power supply pins (V+ and V–) and the ground plane. Place the bypass capacitors as close to the device as possible with the 100-nF capacitor closest to the device, as indicated in 图 68. For single-supply applications, bypass capacitors on the V– pin are not required.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. (For more details, refer to *Circuit Board Layout Techniques*.)
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Minimize parasitic coupling between +IN and OUT for best ac performance.
- Place the external components as close to the device as possible. As shown in 图 68, keeping RF, CF, and RG close to the inverting input will minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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11.2 Layout Example



(Schematic Representation)

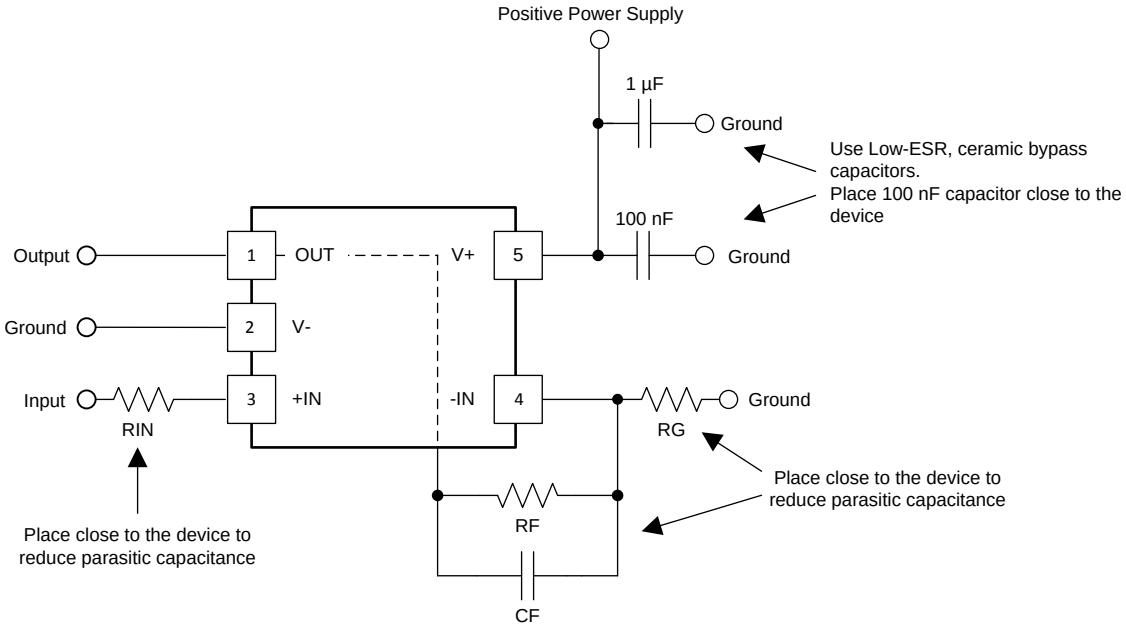


图 68. PCB Layout Example

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12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

12.1.1.2 TI 高精度设计

欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

12.2 文档支持

12.2.1 相关文档

《16 位、1MSPS 多路复用数据采集参考设计指南》

针对最低失真和噪声进行功耗优化的 16 位 1MSPS 数据采集块参考设计

《电路板布局布线技巧》

12.3 相关链接

表 1 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
OPA626	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2626	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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TINA is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2626IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6	Samples
OPA2626IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	16R6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

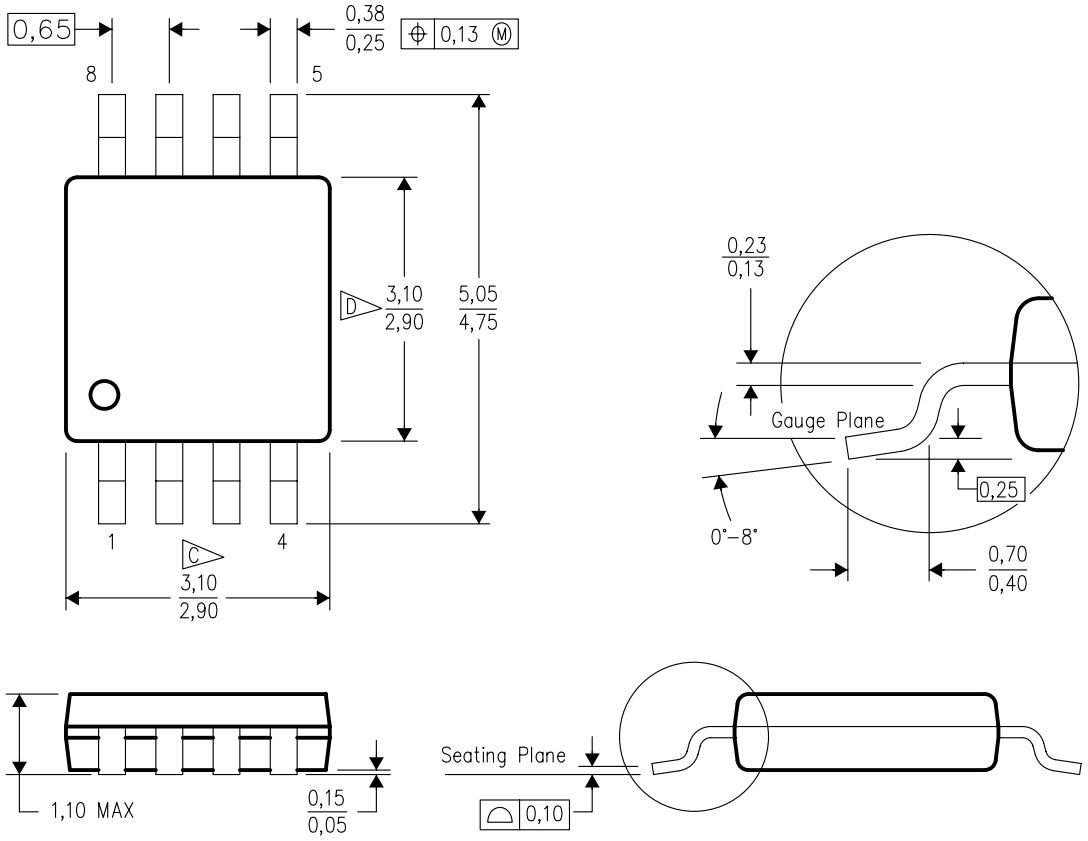
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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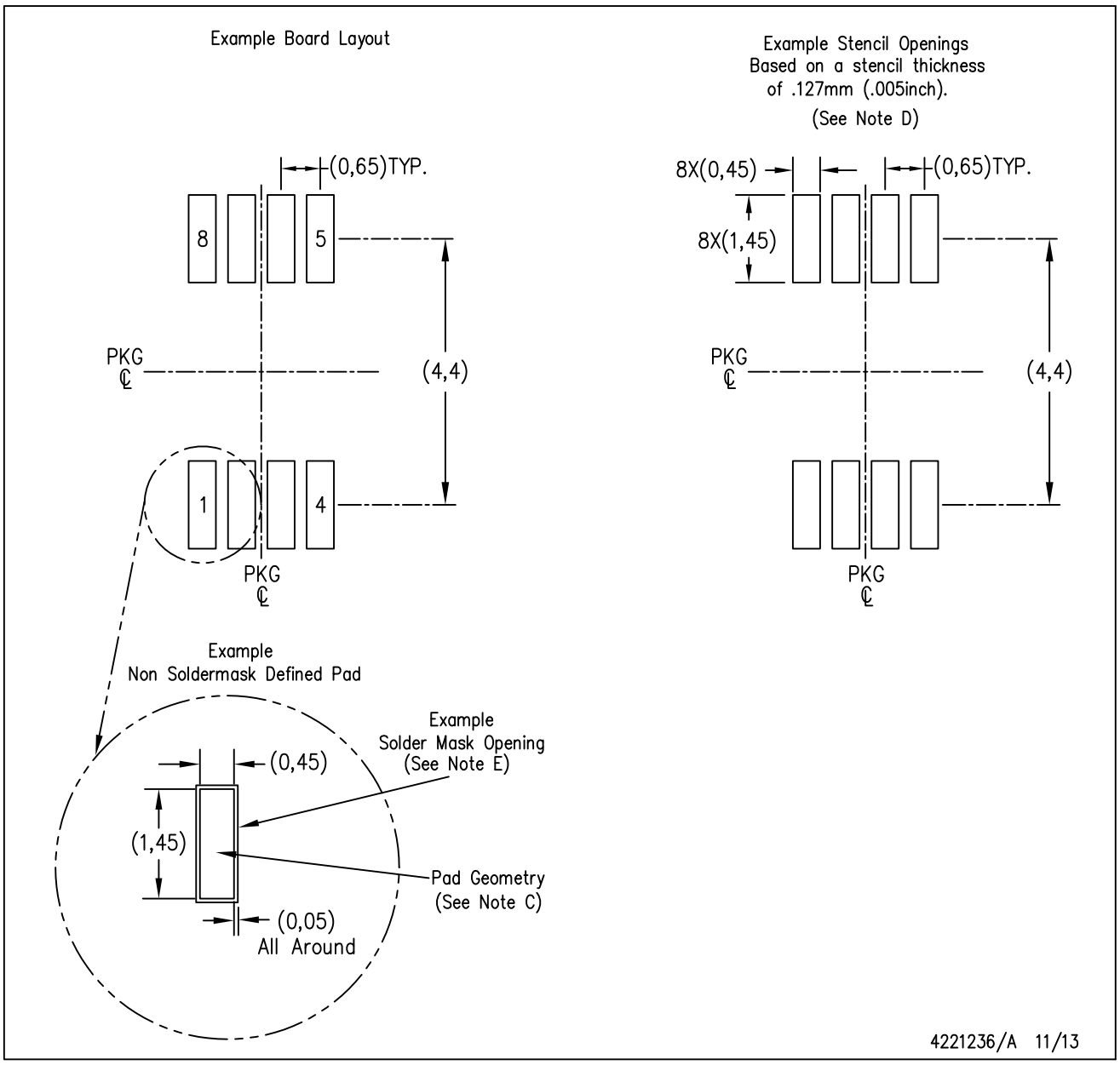
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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