INA821 35μV 失调电压、7-nV/√Hz 噪声、低功耗精密仪表放大器

1 特性

- 低失调电压：10μV（典型值）、35μV（最大值）
- 增益漂移：5ppm/°C (G = 1)、35ppm/°C (G > 1)（最大值）
- 噪声：7nV/√Hz
- 带宽：4.7MHz (G = 1)、290kHz (G = 100)
- 与 1nF 容式负载一起工作时保持稳定
- 输入保护电压高达 ±40V
- 共模抑制：112dB，G = 10（最小值）
- 电源抑制：114dB，G = 1（最小值）
- 电源电流：650μA（最大值）
- 电源范围：
  - 单电源：4.5 V 至 36 V
  - 双电源：±2.25V 至 ±18V
- 额定温度范围：
  –40°C 至 +125°C
- 封装：8 引脚 SOIC

2 应用

- 工业过程控制
- 断路器
- 电池检测仪
- 心电图 (ECG) 放大器
- 电力自动化
- 医疗仪表
- 便携式仪表

3 说明

INA821 是一款高精度仪表放大器，可实现低功耗并且可在较宽的单电源或双电源电压范围内运行。可通过单个外部电阻器在 1 到 10,000 范围内设置任意增益。由于采用超 β 输入晶体管（这些晶体管可提供较低的输入失调电压、失调电压漂移、输入偏置电流以及输入电压和电流噪声），该器件可提供出色的精度。附加电路可以为输入提供高达 ±40V 的过压保护。

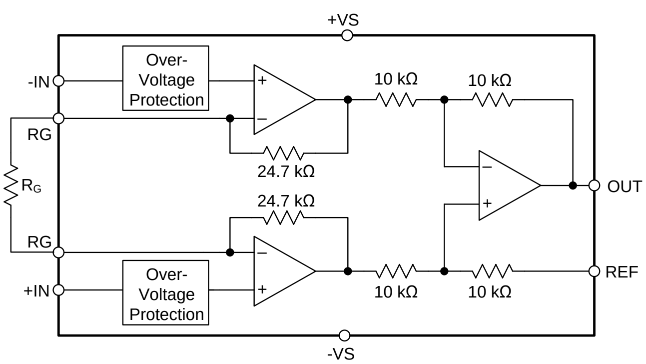
INA821 经过优化，可提供较高的共模抑制比。当 G = 1 时，整个输入共模范围内共模抑制比超过 92dB。该器件可在 4.5V 单电源和高达 ±18V 的双电源供电情况下实现低电压运行。INA821 可提供 8 引脚 SOIC 封装，额定温度范围为 –40°C 至 +125°C。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
INA821	SOIC (8)	4.90mm × 3.91mm

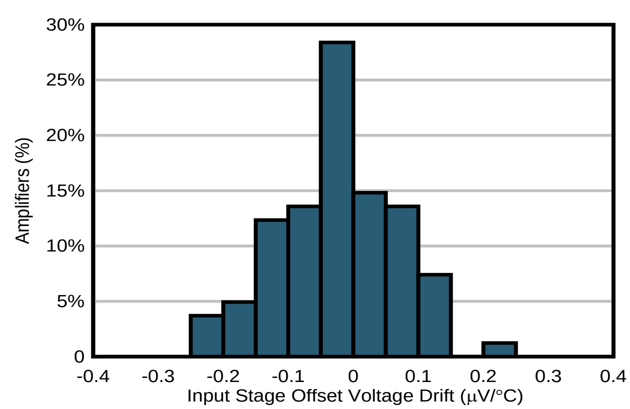
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

INA821 简化内部原理图



$$G = 1 + \frac{49.4\ k\Omega}{R_G} \qquad V_O = G\left(V_{+IN} - V_{-IN}\right) + V_{REF}$$

输入阶段失调电压漂移的典型分布



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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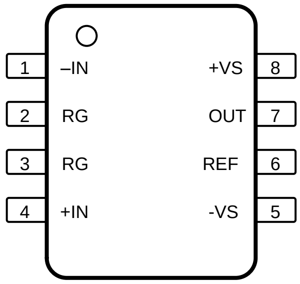
5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA821	35-µV Offset, 0.4 µV/°C V_{OS} drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier	G = 1 + 49.4kOhms / RG	2, 3
INA819	35-µV Offset, 0.4 µV/°C V_{OS} drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50kOhms / RG	2, 3
INA828	50-µV Offset, 0.5 µV/°C V_{OS} drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50kOhms / RG	1, 8
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA	G = 1 + 100kOhms / RG	1, 8
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V	digital programmable	N/A
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion	G = 0.2 V/V	N/A
PGA112	Precision programmable gain op amp with SPI	digital programmable	N/A

6 Pin Configuration and Functions

**D Package
8-Pin SOIC
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	1	I	Negative (inverting) input
+IN	4	I	Positive (noninverting) input
OUT	7	O	Output
RG	2, 3	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
REF	6	I	Reference input. This pin must be driven by a low impedance source.
–VS	5	—	Negative supply
+VS	8	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–20	20	V
Signal input pins	Voltage	–40	40	V
	REF pin	–20	20	
Signal output pins		$(-V_S) - 0.5$	$(+V_S) + 0.5$	V
Output short-circuit(2)			Continuous	
Operating Temperature, T_A		–50	150	°C
Junction Temperature, T_J			175	
Storage Temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S	Single-supply	4.5	36	V
	Dual-supply	±2.25	±18	
Specified temperature	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA821 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input stage offset voltage(1) (2)	G = 100, RTI		10	35	µV
		T_A = –40°C to 125°C(3)			75	µV
		vs temperature, T_A = –40°C to 125°C			0.4	µV/°C
V_{OSO}	Output stage offset voltage(1) (2)	G = 1		50	350	µV
		T_A = –40°C to 125°C(3)			850	µV
		vs temperature, T_A = –40°C to 125°C			5	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI	110	120		dB
		G = 10, RTI	114	130		
		G = 100, RTI	130	135		
		G = 1000, RTI	136	140		
z_{id}	Differential impedance			100 || 1		GΩ || pF
z_{ic}	Common-mode impedance			100 || 7		GΩ || pF
	RFI filter, –3-dB frequency			45		MHz
V_{CM}	Operating input range(4)		(V–) + 2		(V+) – 2	V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C			See 图 51 to 图 54	
	Input overvoltage range	T_A = –40°C to 125°C(3)			±40	V
CMRR	Common-mode rejection ratio	At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1	92	105		dB
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 10	112	125		
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 100	132	145		
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1000	140	150		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		0.15	0.5	nA
		T_A = –40°C to 125°C			2	
I_{OS}	Input offset current	V_{CM} = V_S / 2		0.15	0.5	nA
		T_A = –40°C to 125°C			2	
NOISE VOLTAGE						
e_{NI}	Input stage voltage noise(5)	f = 1 kHz, G = 100, R_S = 0 Ω		7		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		0.14		$µV_{PP}$
e_{NO}	Output stage voltage noise(5)	f = 1 kHz, R_S = 0 Ω		65		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		2.5		$µV_{PP}$
I_n	Noise current	f = 1 kHz		130		fA/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100		4.7		pA_{PP}
GAIN						
G	Gain equation				1 + (49.4 kΩ / R_G)	V/V
	Range of gain		1		1000	V/V
GE	Gain error	G = 1, V_O = ±10 V		±0.005%	±0.025%	
		G = 10, V_O = ±10 V		±0.025%	±0.15%	
		G = 100, V_O = ±10 V		±0.025%	±0.15%	
		G = 1000, V_O = ±10 V		±0.05%		
	Gain vs temperature(6)	G = 1, T_A = –40°C to 125°C			±5	ppm/°C
		G > 1, T_A = –40°C to 125°C			±35	

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}{}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Specified by characterization.
(4) Input voltage range of the INA821 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves 图 51 through 图 54 for more information.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}{}^2 + (e_{NO} / G)^2]}$
(6) The values specified for G > 1 do not include the effects of the external gain-setting resistor, "R_G".

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain nonlinearity	G = 1 to 10, V_O = –10 V to 10 V, R_L = 10 kΩ		1	10	ppm
		G = 100, V_O = –10 V to 10 V, R_L = 10 kΩ			15	
		G = 1000, V_O = –10 V to 10 V, R_L = 10 kΩ		10		
		G = 1 to 100, V_O = –10 V to 10 V, R_L = 2 kΩ		30		
OUTPUT						
	Voltage swing		(V–) + 0.15		(V+) – 0.15	V
	Load capacitance stability			1000		pF
Z_O	Closed-loop output impedance	f = 10 kHz		1.3		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±20		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		4.7		MHz
		G = 10		970		kHz
		G = 100		290		
		G = 1000		30		
SR	Slew rate	G = 1, V_O = ±10 V		2.0		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 10 V		6		µs
		0.01%, G = 1000, V_{STEP} = 10 V		40		
		0.001%, G = 1 to 100, V_{STEP} = 10 V		10		
		0.001%, G = 1000, V_{STEP} = 10 V		50		
REFERENCE INPUT						
R_{IN}	Input impedance			10		kΩ
	Voltage range		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
V_S	Power-supply voltage	Single-supply	4.5		36	V
		Dual-supply	±2.25		±18	
I_Q	Quiescent current	V_{IN} = 0 V		600	650	µA
		vs temperature, T_A = –40°C to 125°C			870	

7.6 Typical Characteristics - Table of Graphs

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

表 1. Table of Graphs

DESCRIPTION	FIGURE
Typical Distribution of Input Stage Offset Voltage	图 1
Typical Distribution of Input Stage Offset Voltage Drift	图 2
Typical Distribution of Output Stage Offset Voltage	图 3
Typical Distribution of Output Stage Offset Voltage Drift	图 4
Input Stage Offset Voltage vs Temperature	图 5
Output Stage Offset Voltage vs Temperature	图 6
Typical Distribution of Input Bias Current T_A = 25°C	图 7
Typical Distribution of Input Bias Current T_A = 90°C	图 8
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Input Bias Current vs Temperature	图 10
Input Offset Current vs Temperature	图 11
Typical CMRR Distribution G=1	图 12
Typical CMRR Distribution G=10	图 13
. CMRR vs Temperature G=1	图 14
CMRR vs Temperature G=10	图 15
Input Current vs Input Overvoltage	图 16
CMRR vs Frequency (RTI)	图 17
CMRR vs Frequency (RTI, 1-kΩ source imbalance)	图 18
Positive PSRR vs Frequency (RTI)	图 19
Negative PSRR vs Frequency (RTI)	图 20
Gain vs Frequency	图 21
Voltage Noise Spectral Density vs Frequency (RTI)	图 22
Current Noise Spectral Density vs Frequency (RTI)	图 23
0.1-Hz to 10-Hz RTI Voltage Noise G = 1	图 24
0.1-Hz to 10-Hz RTI Voltage Noise G = 1000	图 25
0.1-Hz to 10-Hz RTI Current Noise	图 26
Typical Distribution of Gain Error G=1	图 27
Typical Distribution of Gain Error G=10	图 28
Input Bias Current vs Common-Mode Voltage	图 29
Gain Error vs Temperature G = 1	图 30
Gain Error vs Temperature G = 10	图 31
.Supply Current vs Temperature	图 32
Gain Nonlinearity G = 1	图 33
Gain Nonlinearity G = 10	图 34
Offset Voltage vs Negative Common-Mode Voltage	图 35
Offset Voltage vs Positive Common-Mode Voltage	图 36
Positive Output Voltage Swing vs Output Current	图 37
Negative Output Voltage Swing vs Output Current	图 38
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Large-Signal Frequency Response	图 40
THD+N vs Frequency	图 41
Overshoot vs Capacitive Loads	图 42
Small-Signal Response G = 1	图 43
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Small-Signal Response G = 100	图 45

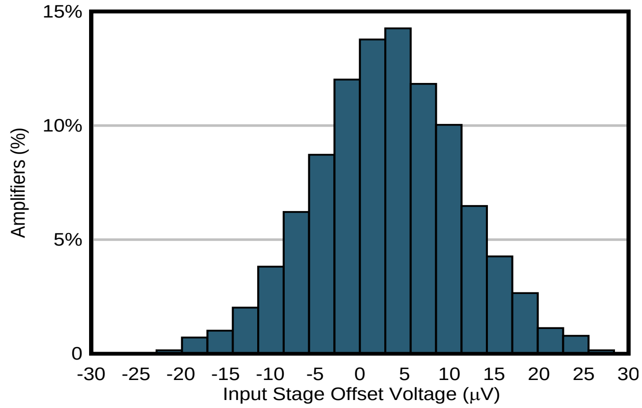
Typical Characteristics - Table of Graphs (接下页)

表 1. Table of Graphs (接下页)

DESCRIPTION	FIGURE
Small-Signal Response G = 1000	图 46
Large Signal Step Response	图 47
Closed-Loop Output Impedance	图 48
Differential-Mode EMI Rejection Ratio	图 49
Common-Mode EMI Rejection Ratio	图 50
Input Common-Mode Voltage vs Output Voltage G = 1, V_S = 5 V	图 51
Input Common-Mode Voltage vs Output Voltage G = 100, V_S = 5 V	图 52
Input Common-Mode Voltage vs Output Voltage V_S =±5 V	图 53
Input Common-Mode Voltage vs Output Voltage V_S =±15 V	图 54

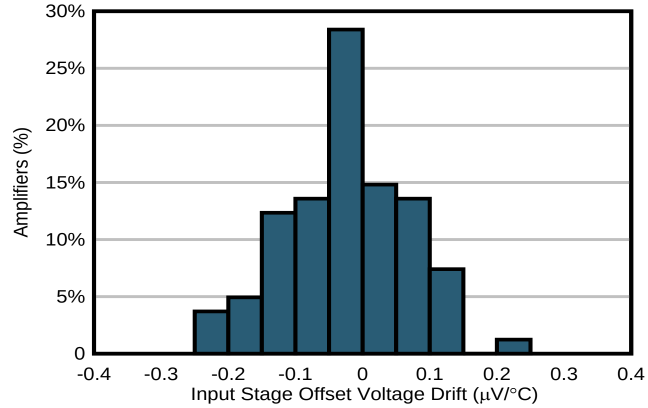
7.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



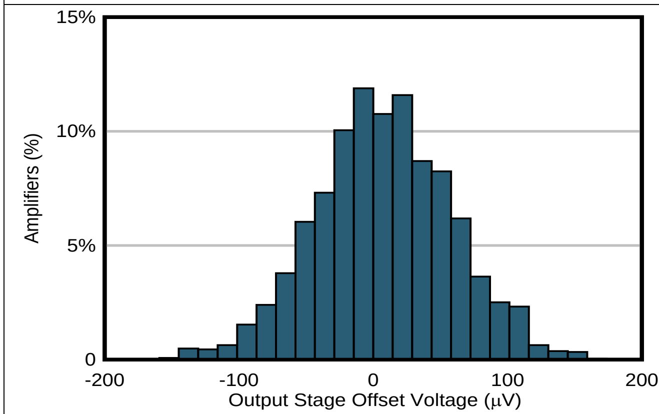
N = 2667 Mean = 3.1 µV Std. Dev. = 8.1 µV

图 1. Typical Distribution of Input Stage Offset Voltage



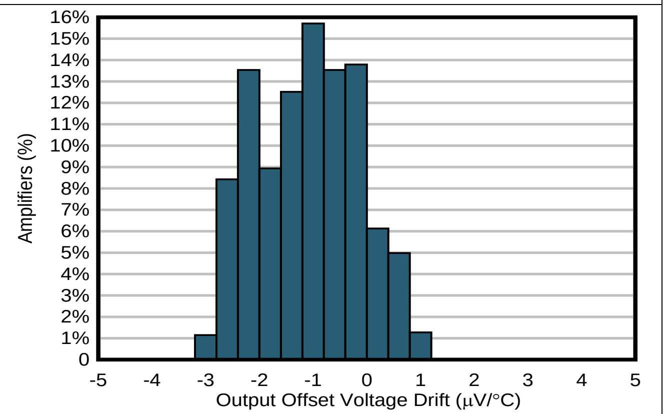
N = 81 Mean = -0.03 µV/°C Std. Dev. = 0.09 µV/°C

图 2. Typical Distribution of Input Stage Offset Voltage Drift



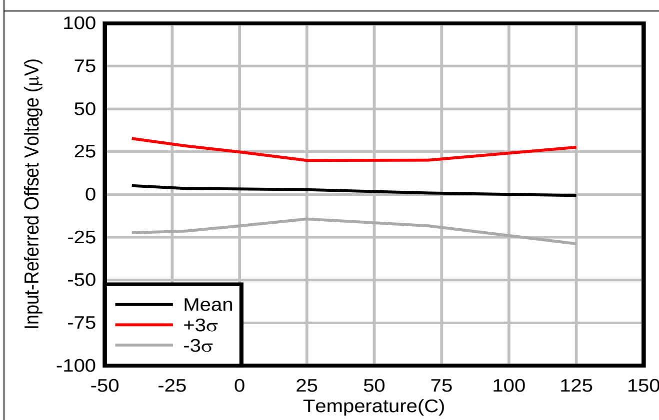
N = 2667 Mean = 7.7 µV Std. Dev. = 50.7 µV

图 3. Typical Distribution of Output Stage Offset Voltage



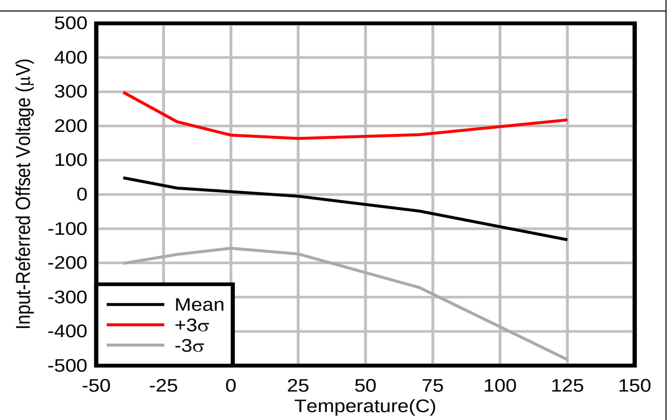
N = 81 Mean = –1.09 µV/°C Std. Dev. = 0.94 µV/°C

图 4. Typical Distribution of Output Stage Offset Voltage Drift



81 units

图 5. Input Stage Offset Voltage vs Temperature



81 units

图 6. Output Stage Offset Voltage vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

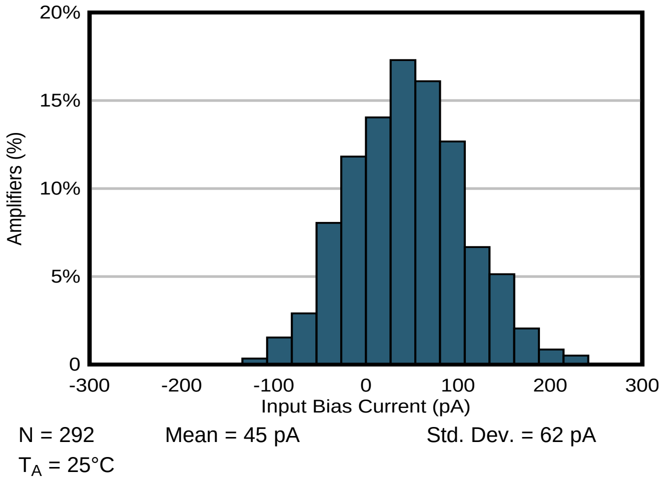


图 7. Typical Distribution of Input Bias Current T_A = 25°C

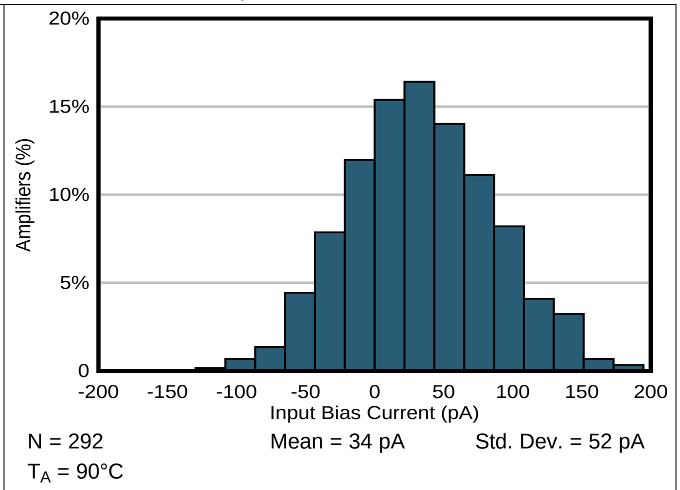


图 8. Typical Distribution of Input Bias Current T_A = 90°C

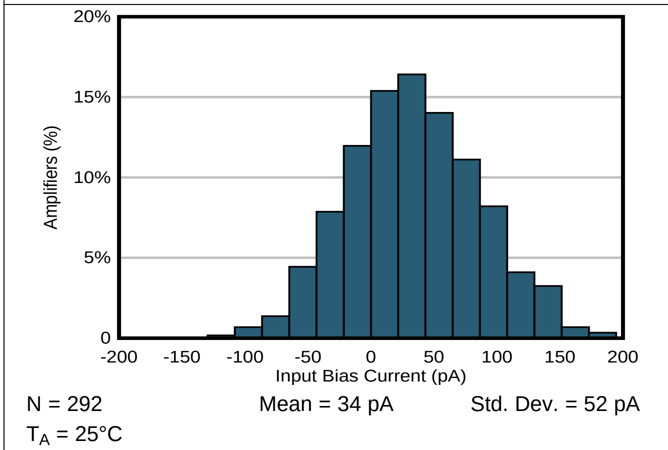


图 9. Typical Distribution of Input Offset Current

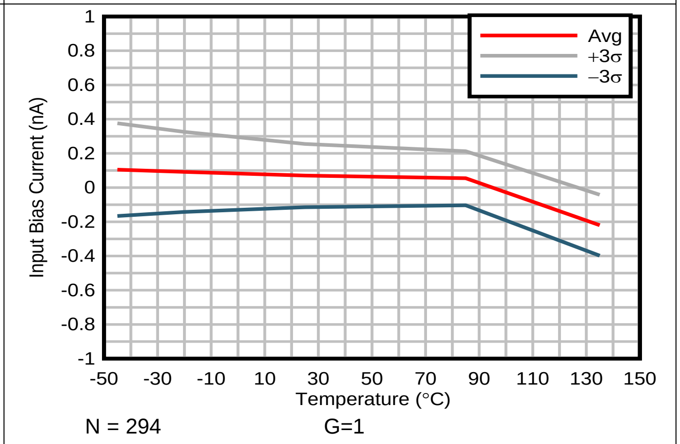


图 10. Input Bias Current vs Temperature

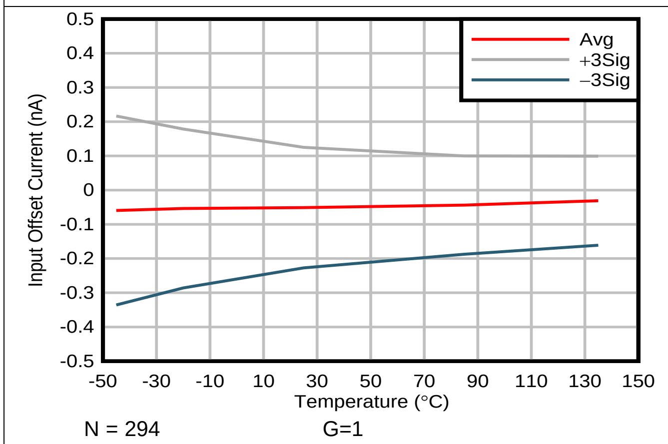


图 11. Input Offset Current vs Temperature

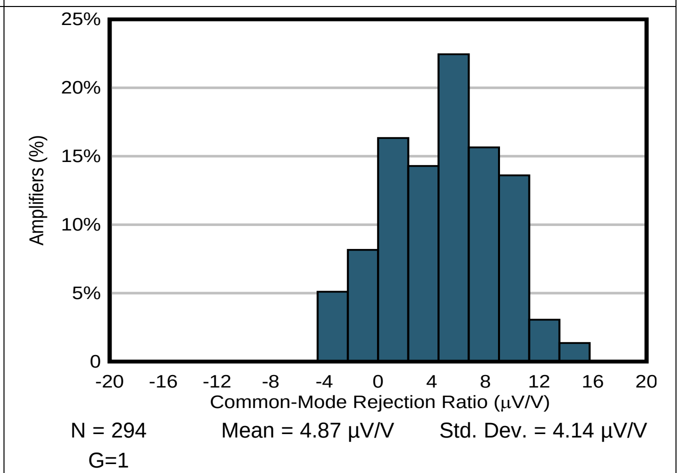
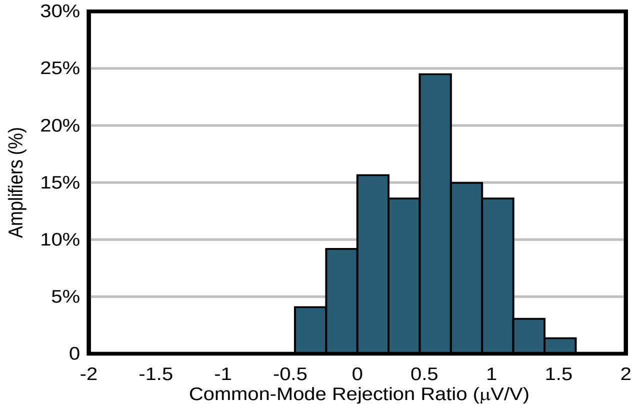


图 12. Typical CMRR Distribution G=1

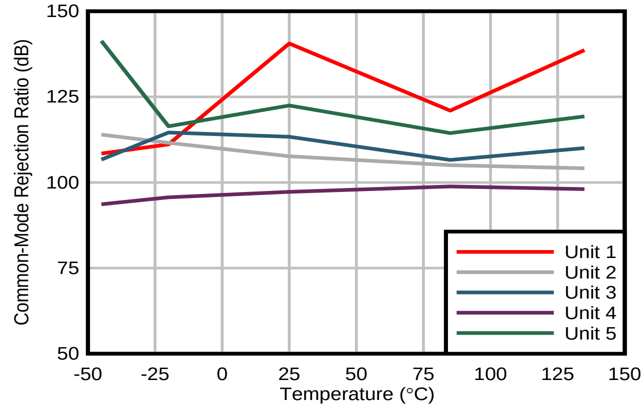
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



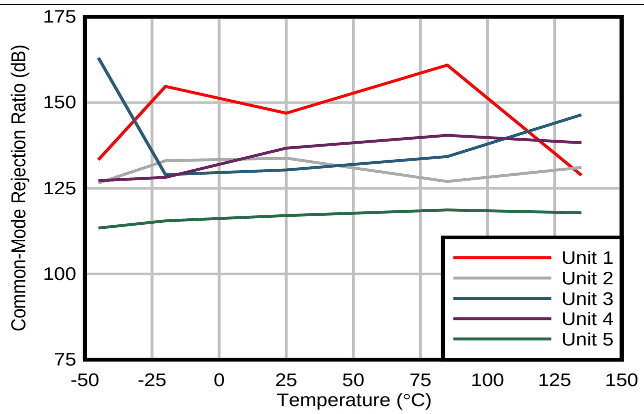
N = 294 Mean = 0.51 µV/V Std. Dev. = 0.42 µV/V
G=10

图 13. Typical CMRR Distribution G=10



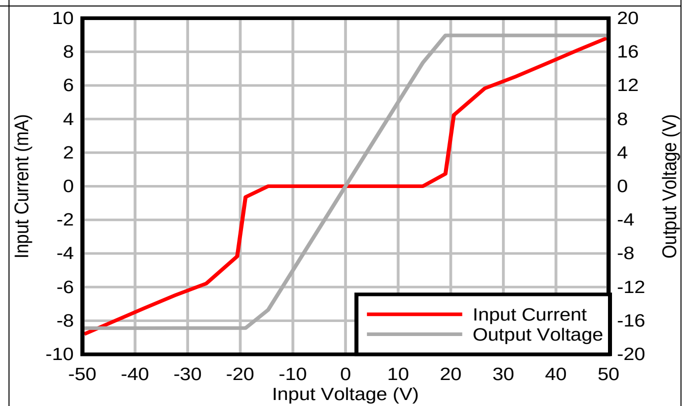
N = 5 G = 1

图 14. CMRR vs Temperature G = 1



N = 5 G = 10

图 15. CMRR vs Temperature G = 10



V_S = ±18 V

图 16. Input Current vs Input Overvoltage

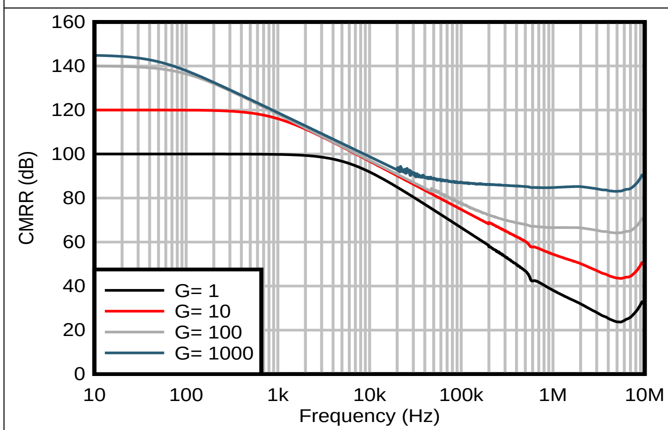


图 17. CMRR vs Frequency (RTI)

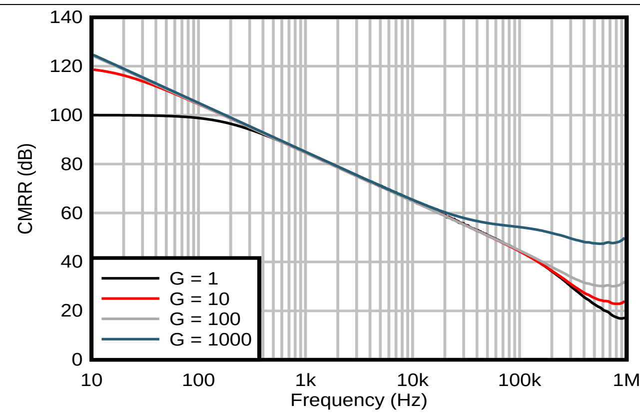


图 18. CMRR vs Frequency (RTI, 1-kΩ source imbalance)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

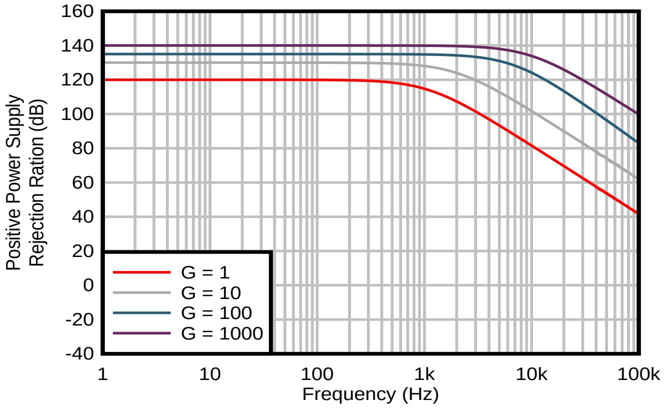


图 19. Positive PSRR vs Frequency (RTI)

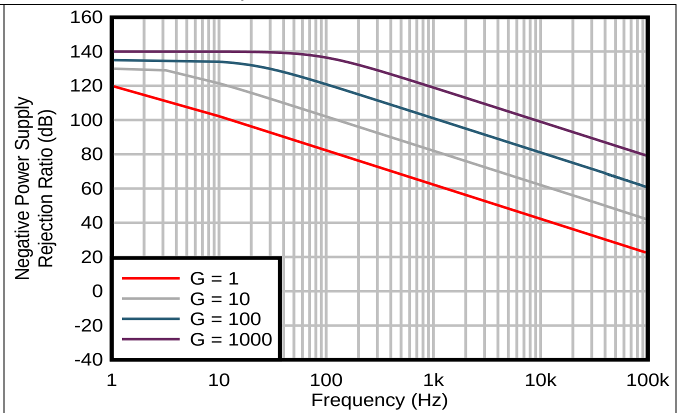


图 20. Negative PSRR vs Frequency (RTI)

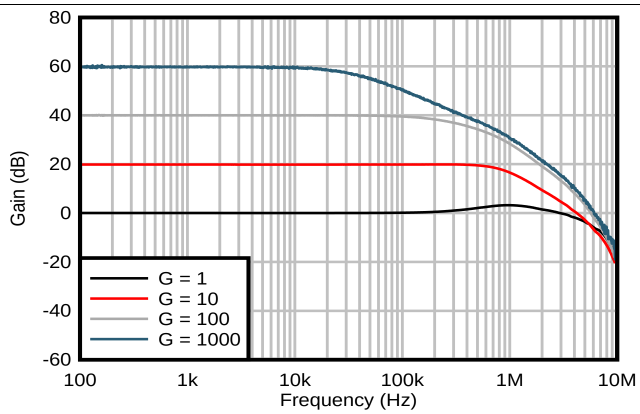


图 21. Gain vs Frequency

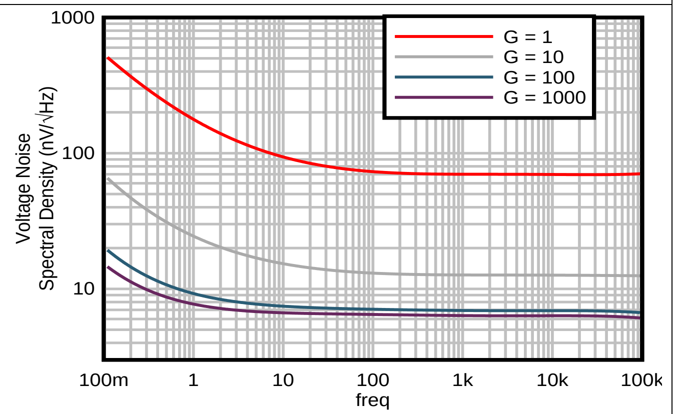


图 22. Voltage Noise Spectral Density vs Frequency (RTI)

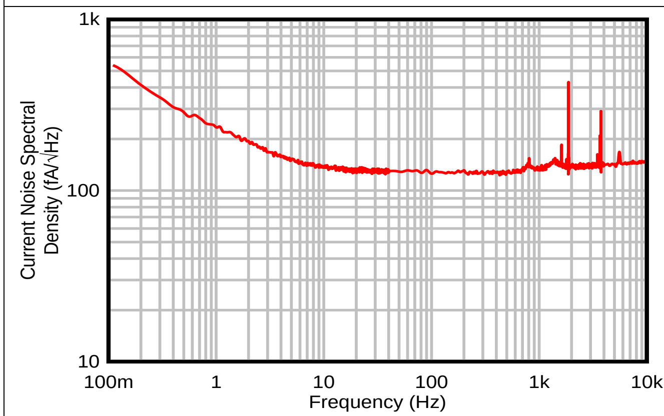
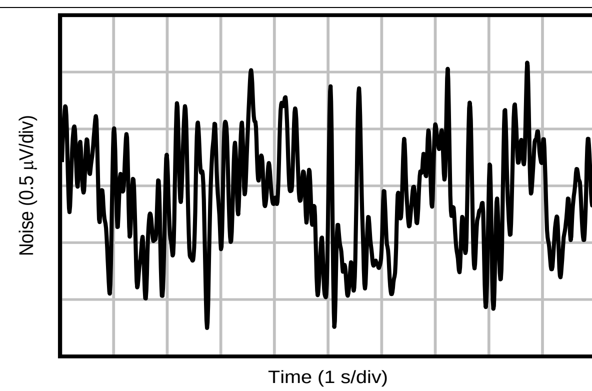


图 23. Current Noise Spectral Density vs Frequency (RTI)



G = 1

图 24. 0.1-Hz to 10-Hz RTI Voltage Noise G = 1

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

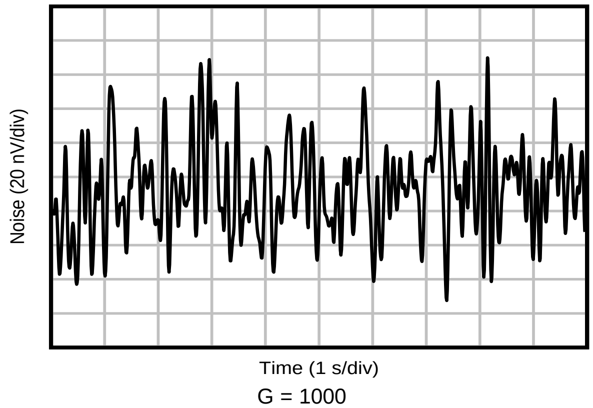


图 25. 0.1-Hz to 10-Hz RTI Voltage Noise G = 1000

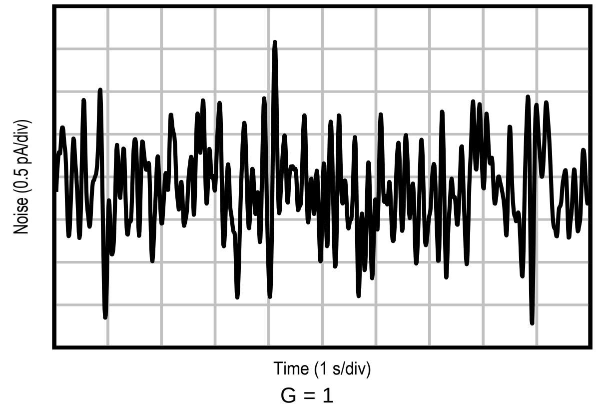


图 26. 0.1-Hz to 10-Hz RTI Current Noise

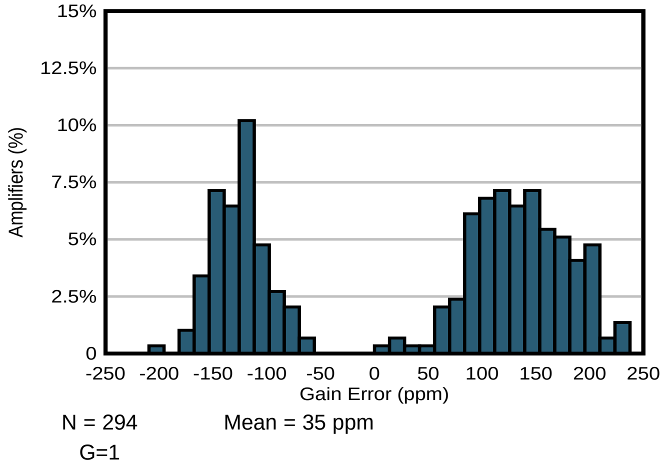


图 27. Typical Distribution of Gain Error G=1

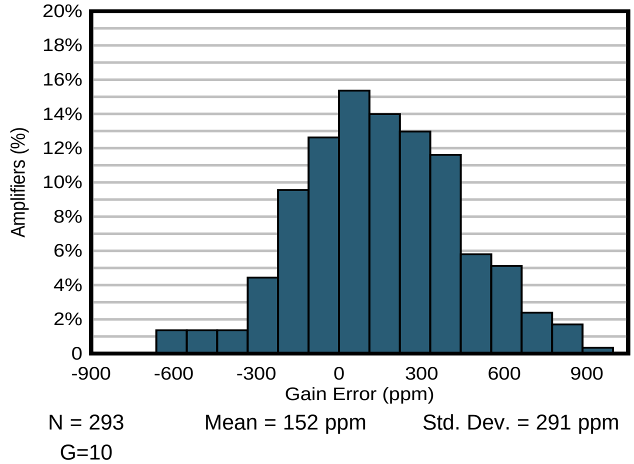


图 28. Typical Distribution of Gain Error G=10

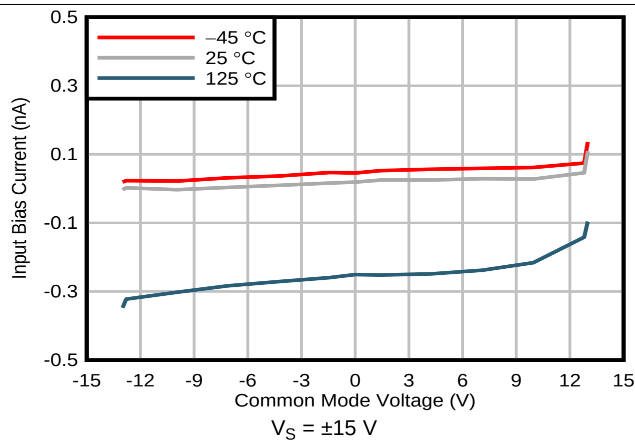


图 29. Input Bias Current vs Common-Mode Voltage

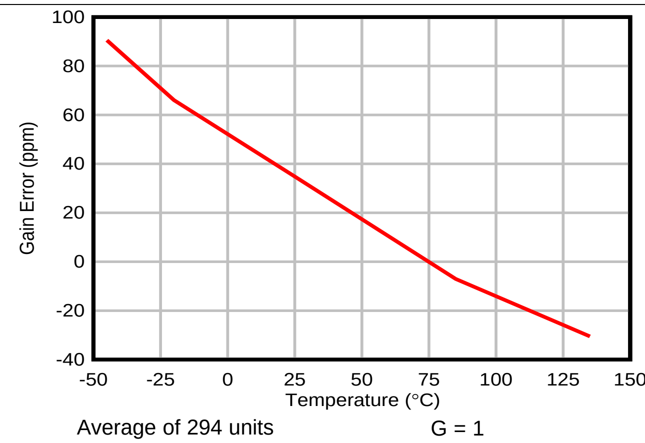
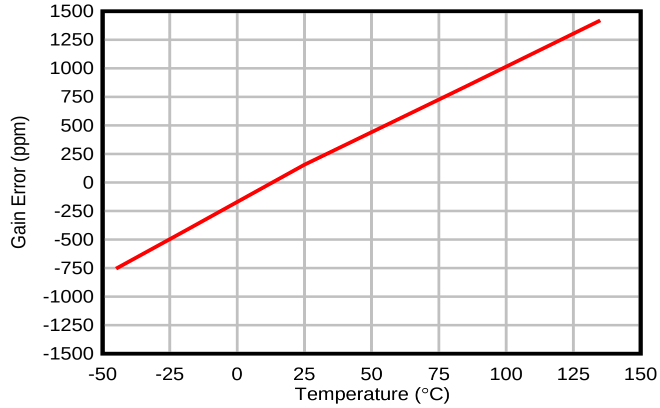


图 30. Gain Error vs Temperature G = 1

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



Average of 294 units

G = 10

图 31. Gain Error vs Temperature G = 10

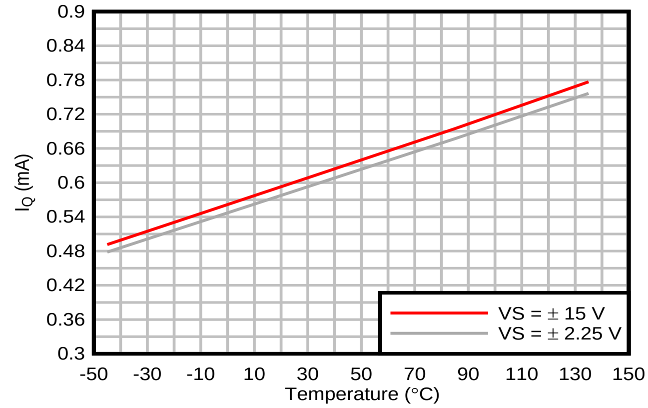
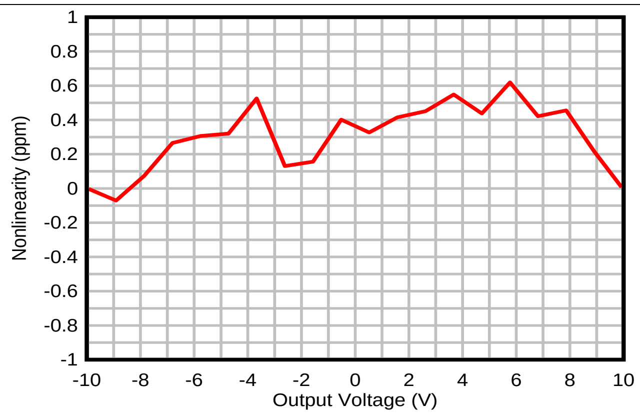
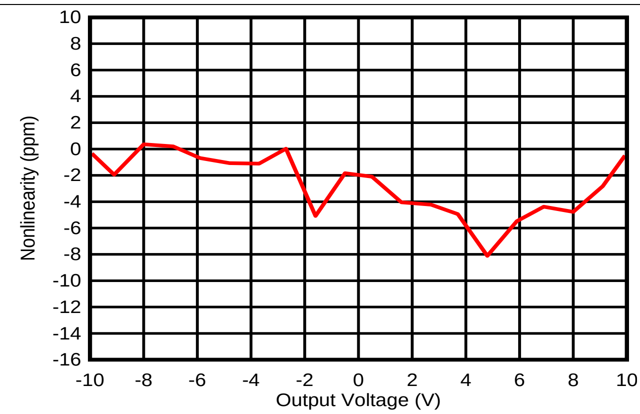


图 32. Supply Current vs Temperature



G = 1

图 33. Gain Nonlinearity G = 1



G = 10

图 34. Gain Nonlinearity

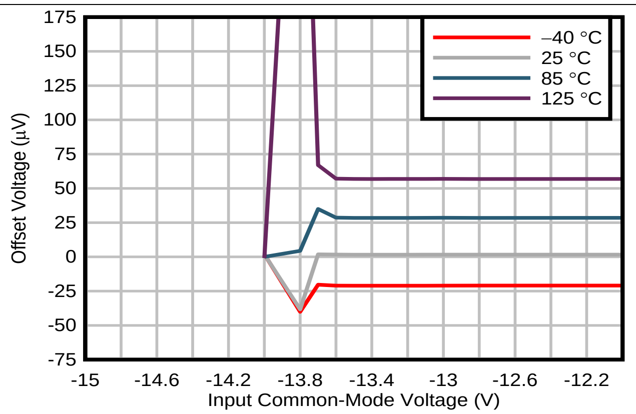


图 35. Offset Voltage vs Negative Common-Mode Voltage

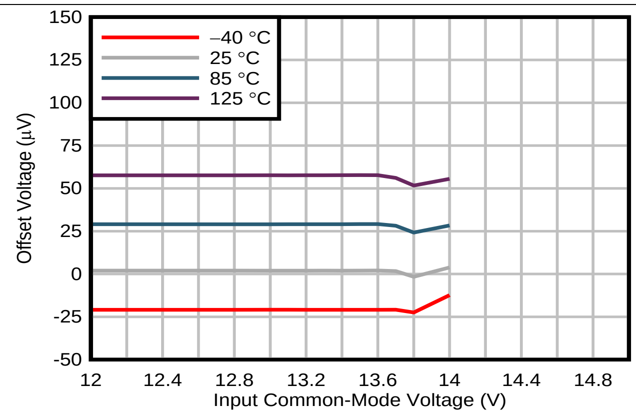


图 36. Offset Voltage vs Positive Common-Mode Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

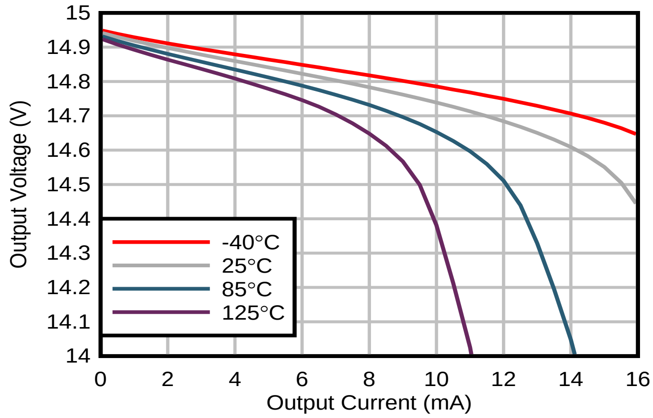


图 37. Positive Output Voltage Swing vs Output Current

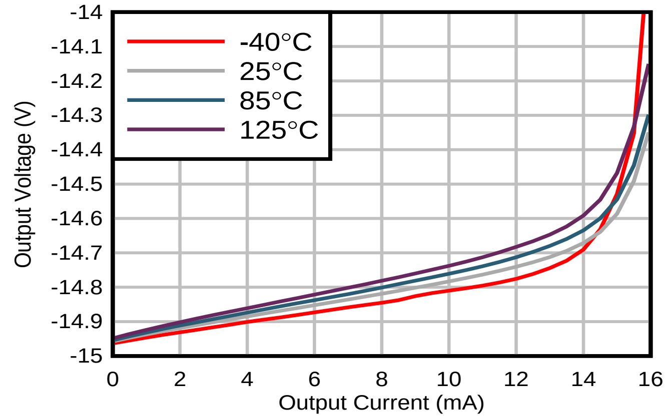


图 38. Negative Output Voltage Swing vs Output Current

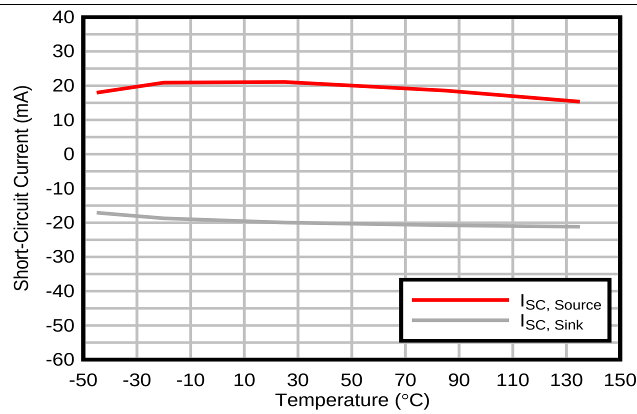


图 39. Short Circuit Current vs Temperature

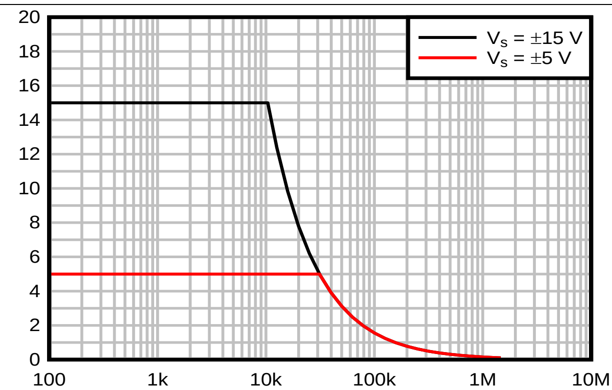
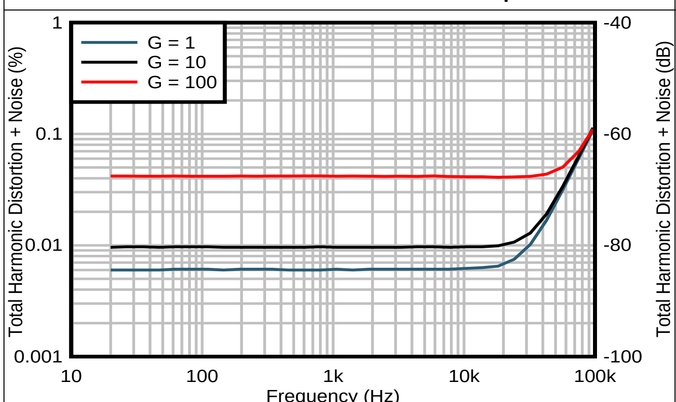


图 40. Large-Signal Frequency Response



500-kHz measurement bandwidth

1-V_{RMS} output voltage 100-kΩ load

图 41. THD+N vs Frequency

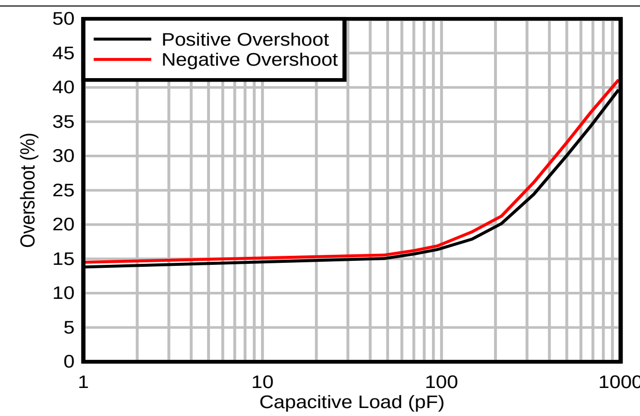
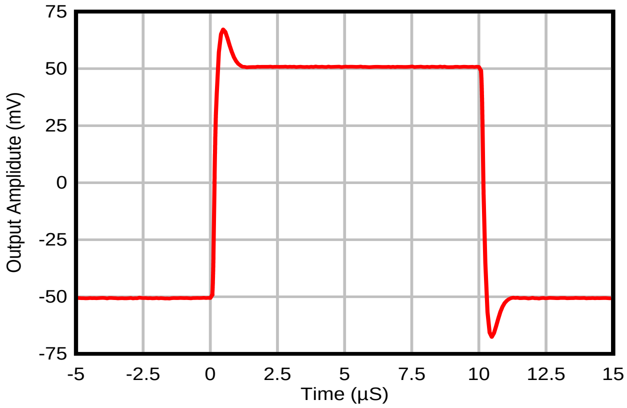


图 42. Overshoot vs Capacitive Loads

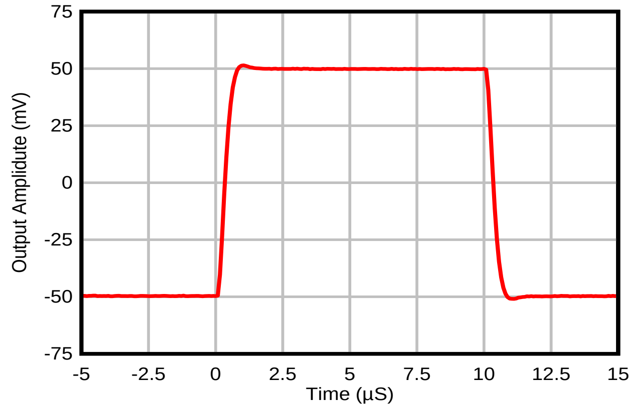
Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



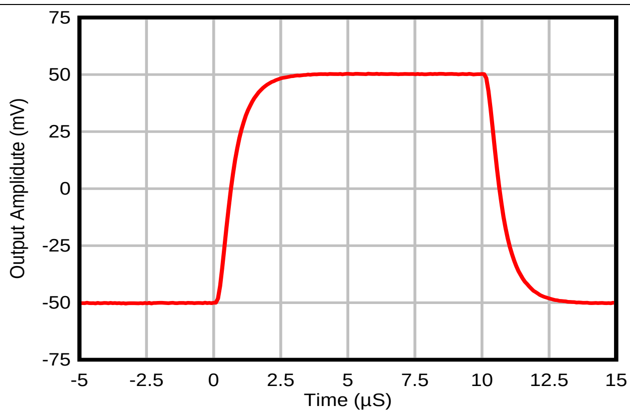
G = 1 R_L = 10 kΩ C_L = 100 pF

图 43. Small-Signal Response



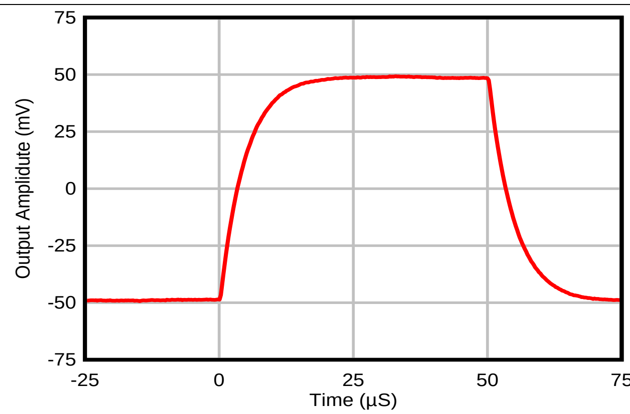
G = 10 R_L = 10 kΩ C_L = 100 pF

图 44. Small-Signal Response



G = 100 R_L = 10 kΩ C_L = 100 pF

图 45. Small-Signal Response



G = 1000 R_L = 10 kΩ C_L = 100 pF

图 46. Small-Signal Response

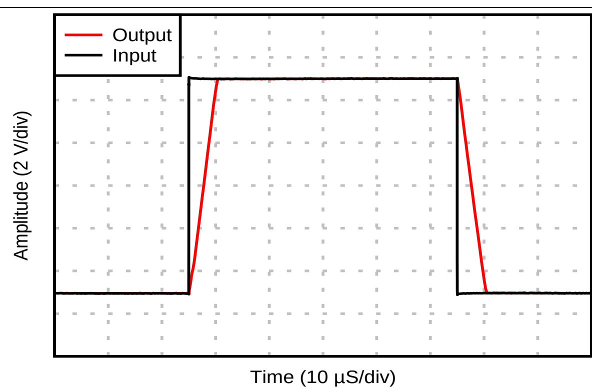


图 47. Large Signal Step Response

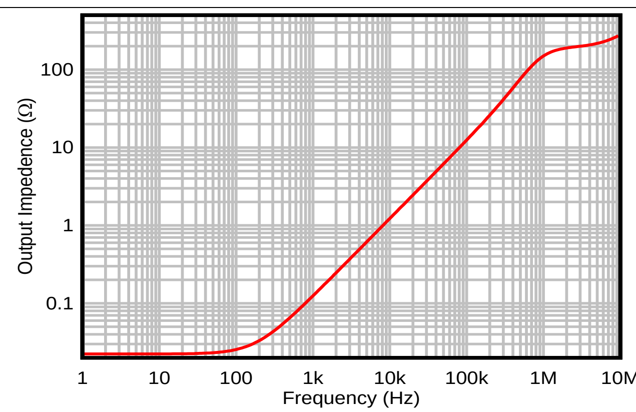


图 48. Closed-Loop Output Impedance

Typical Characteristics (接下页)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

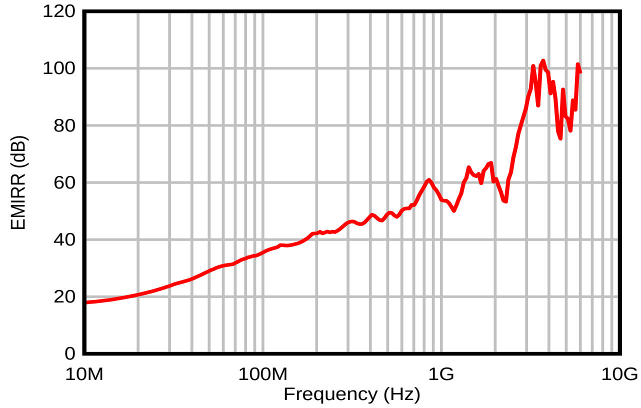


图 49. Differential-Mode EMI Rejection Ratio

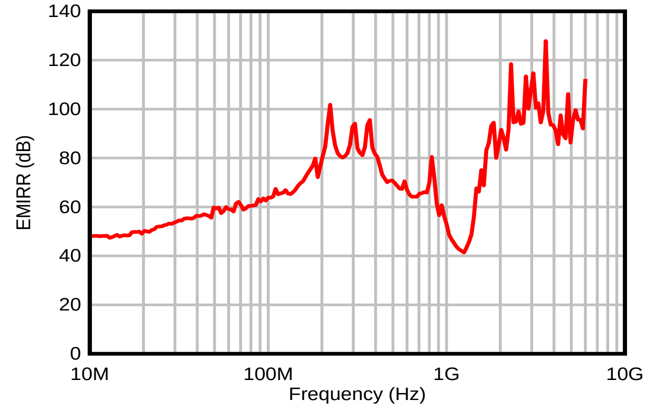
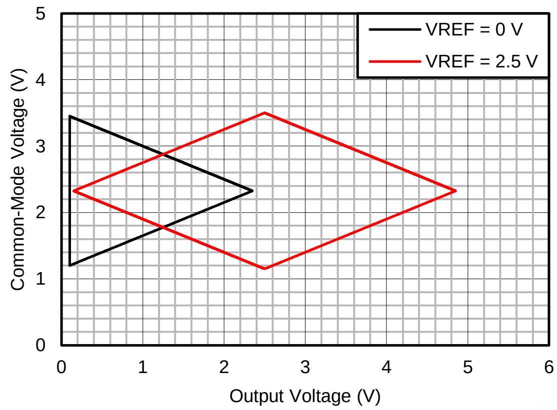
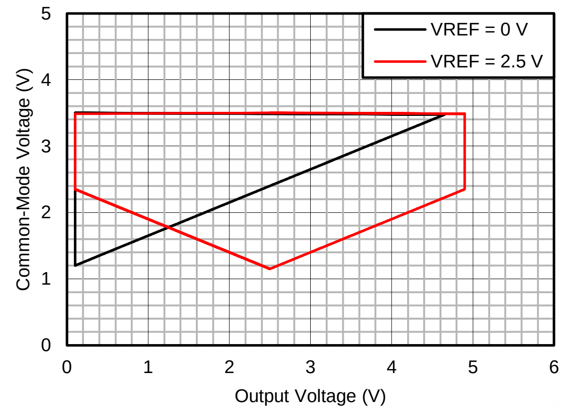


图 50. Common-Mode EMI Rejection Ratio



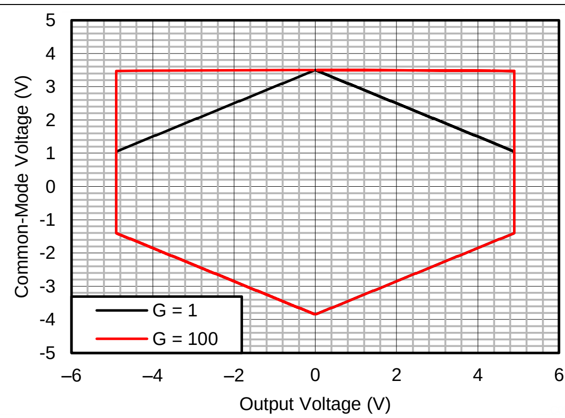
V_S = 5 V G = 1

图 51. Input Common-Mode Voltage vs Output Voltage



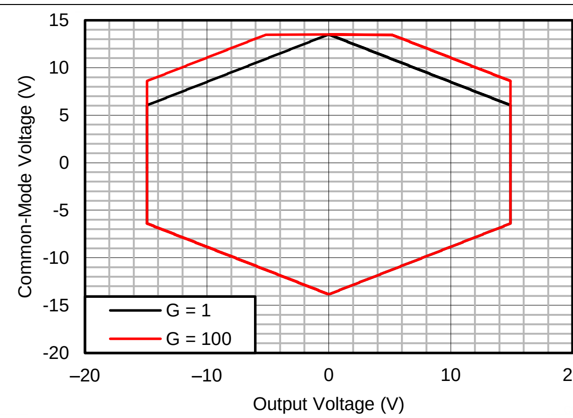
V_S = 5 V G = 100

图 52. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

图 53. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

图 54. Input Common-Mode Voltage vs Output Voltage

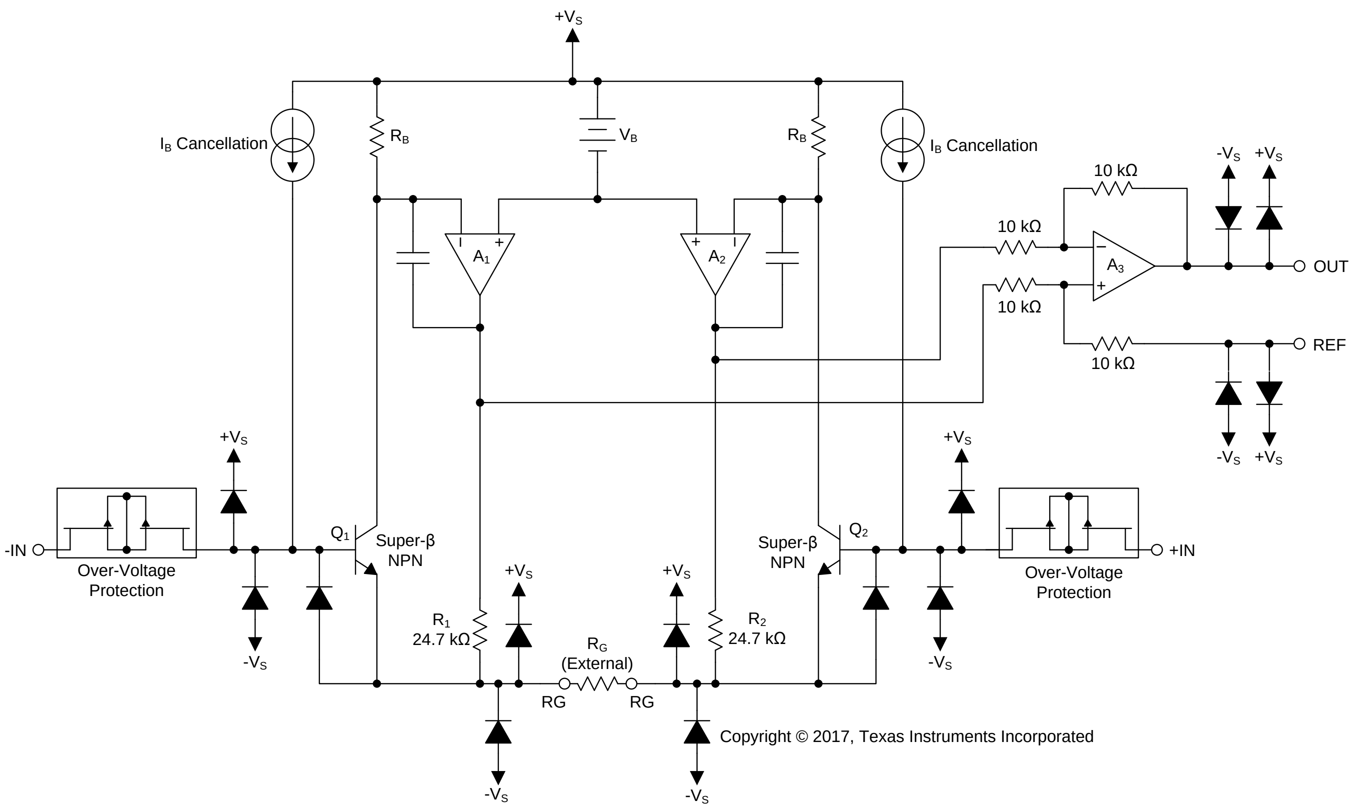
8 Detailed Description

8.1 Overview

The INA821 is a monolithic precision instrumentation amplifier incorporating a current-feedback input stage and a 4-resistor difference amplifier output stage. The differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier (A_3) removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produces output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Setting the Gain

图 55 shows that the gain of the INA821 is set by a single external resistor (R_G) connected between the RG pins (pins 1 and 8).

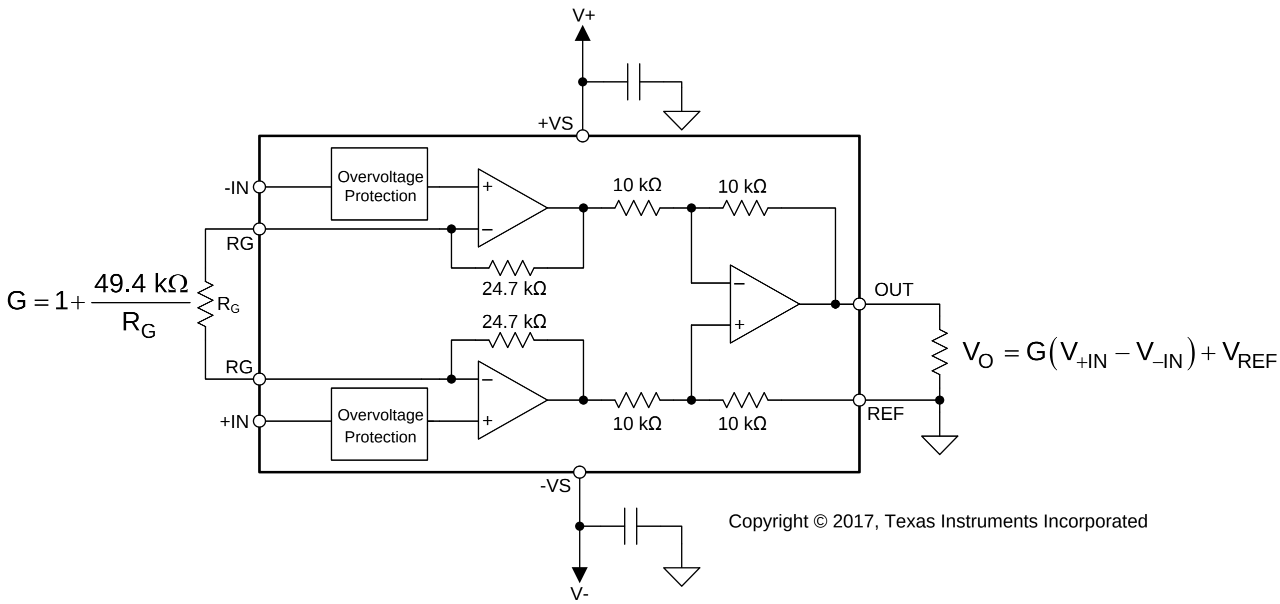


图 55. Simplified Diagram of the INA821 With Gain and Output Equations

The value of R_G is selected according to:

$$G = 1 + \frac{49.4\ k\Omega}{R_G} \tag{1}$$

表 2 lists several commonly used gains and resistor values. The 49.4-kΩ term in 公式 1 is a result of the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA821. As shown in 图 55 and explained in more details in section Layout, it is highly recommended to connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.

表 2. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	49.4 k	49.9 k
5	12.35 k	12.4 k
10	5.489 k	5.49 k
20	2.600 k	2.61 k
50	1.008 k	1 k
100	499	499
200	248	249
500	99	100
1000	49.4	49.9

8.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor (R_G) affects gain. The contribution of R_G to gain accuracy and drift is determined from 公式 1.

The best gain drift of 5 ppm/℃ (maximum) is achieved when the INA821 uses G = 1 without R_G connected. In this case, gain drift is limited by the slight mismatch of the temperature coefficient of the integrated 10-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 24.7-kΩ resistors in the feedback of A_1 and A_2 relative to the drift of the external gain resistor (R_G.) The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over alternate options.

Low resistor values required for high gain make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on the R_G pins maintains optimal CMRR over frequency; see 图 17.

8.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA821 to reject EMI. The offset resulting from an input EMI signal is calculated using 公式 2:

$$\Delta V_{OS} = \left(\frac{V_{RF\_PEAK}^{2}}{100\ mV_P} \right) \cdot 10^{-\left(\frac{EMIRR\ (dB)}{20} \right)}$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal. (2)

图 56 and 图 57 show the INA821 EMIRR graph for differential and common-mode EMI rejection across this frequency range. 表 3 shows the EMIRR values for the INA821 at frequencies encountered in real-world applications. Applications listed in 表 3 are centered on or operated near the particular frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing.

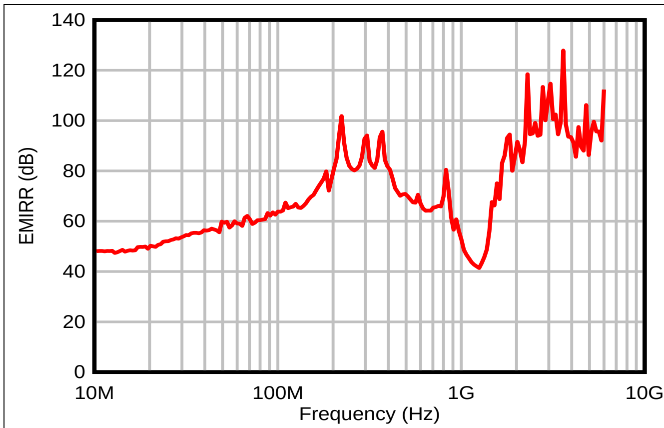


图 56. Common-Mode EMIRR Testing

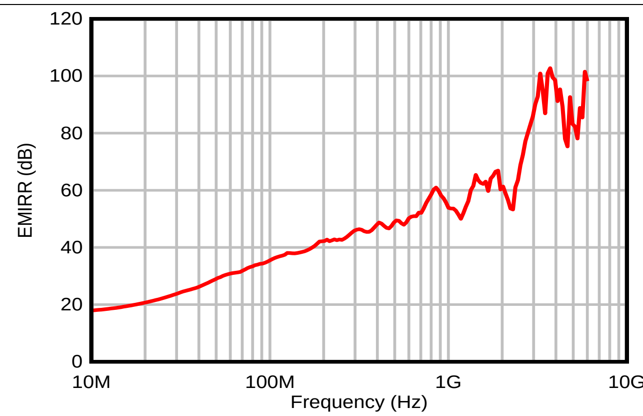


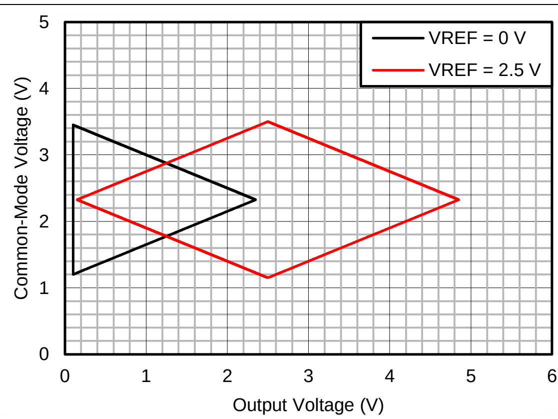
图 57. Differential Mode EMIRR Testing

表 3. INA821 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	60 dB	88 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58 dB	60 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	66 dB	89 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	73 dB	98 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	99 dB	111 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	83 dB	91 dB

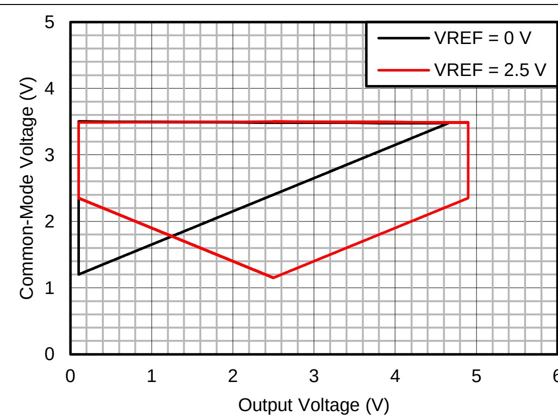
8.3.3 Input Common-Mode Range

The linear input voltage range of the INA821 input circuitry extends within 2 V of power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in 图 58, 图 53 and 图 54. The common-mode range for other operating conditions is best calculated using the *INA common-mode range calculating tool*. The INA821 device operates over a wide range of power supplies and V_{REF} configurations, which provides a comprehensive guide to common-mode range limits for all possible conditions.



V_S = 5 V G = 1

图 58. Input Common-Mode Voltage vs Output Voltage



V_S = 5 V G = 100

图 59. Input Common-Mode Voltage vs Output Voltage

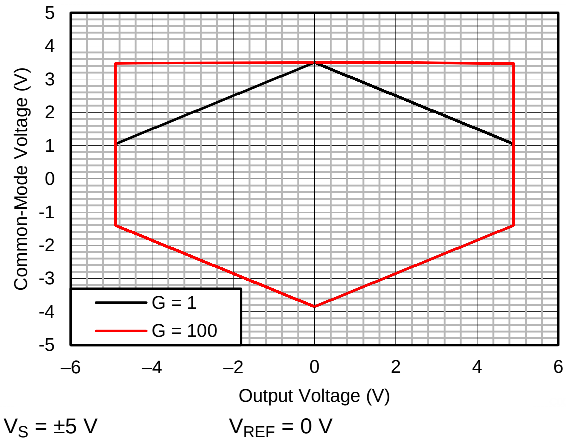


图 60. Input Common-Mode Voltage vs Output Voltage

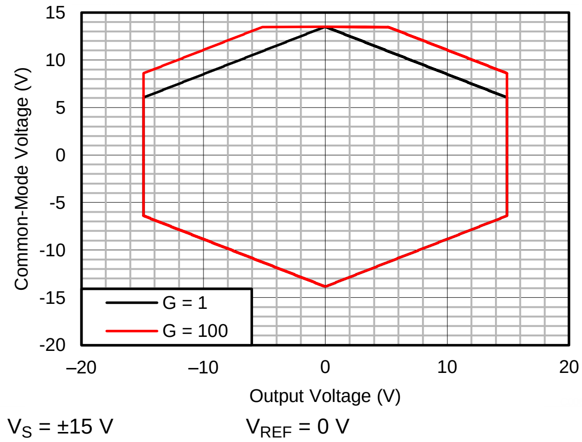


图 61. Input Common-Mode Voltage vs Output Voltage

8.3.4 Input Protection

The inputs of the INA821 device are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and 40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

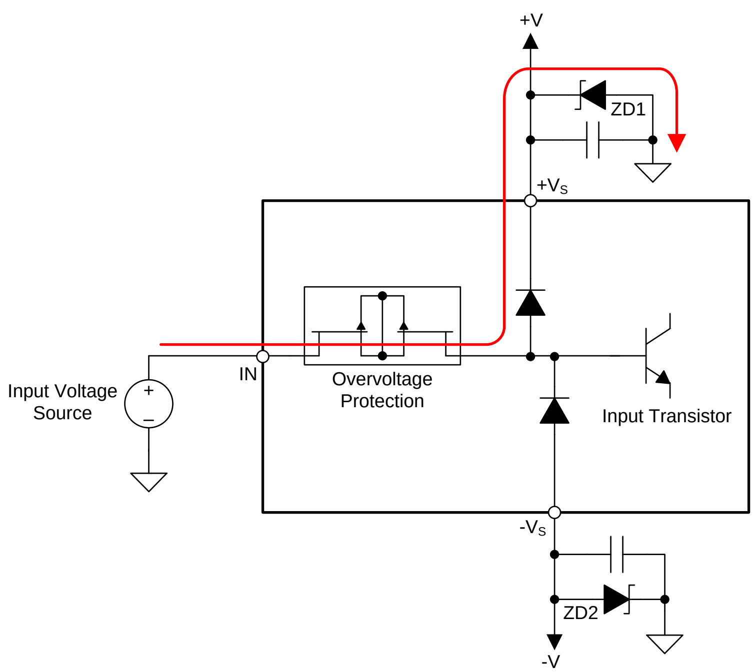


图 62. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see 图 62. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in 图 62) must be placed on the power supplies to provide a current pathway to ground. 图 63 shows the input current for input voltages from –40 V to 40 V when the INA821 is powered by ±15-V supplies.

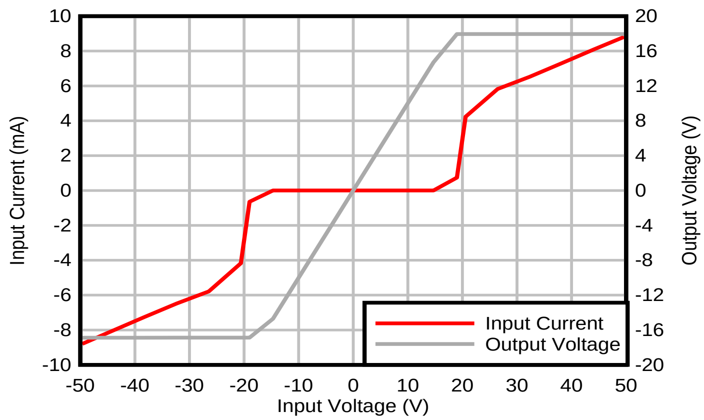


图 63. Input Current vs Input Overvoltage

8.3.5 Operating Voltage

The INA821 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.3.6 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimizing these errors is important by choosing high-precision components such as the INA821 that have improved specifications in critical areas that impact the precision of the overall system. 图 64 shows an example application.

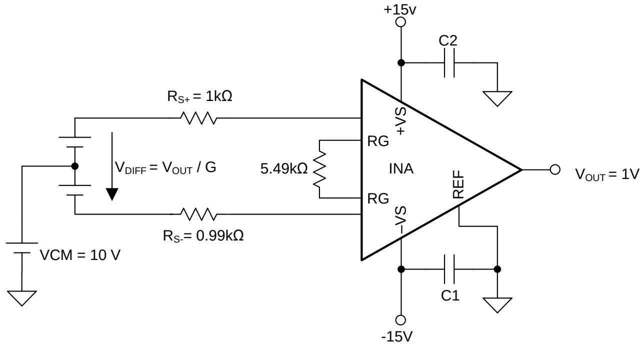


图 64. Example Application with G = 10 V/V and 1 V Output Voltage

Resistor-adjustable devices (such as the INA821) show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1, (for instance, G = 10 V/V or G = 100 V/V) the gain error becomes a significant error source because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA821 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). 表 5 summarizes the major error sources in common INA applications and compares the three cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor) and G = 100 (499-Ω external resistor). All calculations are assuming an output voltage of V_{OUT} = 1 V. Thus, the input signal V_{DIFF} which is given by $V_{DIFF}= V_{OUT}/G$ will exhibit smaller and smaller amplitudes with increasing gain G, e.g. V_{DIFF} = 1 mV at G = 1000 in this example. All calculations refer the error to the input for easy comparison and system evaluation. As can be seen in 表 5, errors generated by the input stage (such as input offset voltage) are more dominant at higher gain while the effects of output stage are suppressed because they are divided by the gain when referring them back to the input. Note that the gain error and gain drift error are much more significant for gains greater than 1 because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. In most applications, static errors (absolute accuracy errors) can readily be removed during calibration in production, while the drift errors will be the key factors limiting overall system performance.

表 4. System Specifications for Error Calculation

Quantity	Value
Vout (V)	1
VCM (V)	10
VS(V)	1
Rs+ (Ω)	1000
Rs- (Ω)	999
Rg tolerance (%)	0.01
Rg drift (ppm/°C)	10
Temp range upper limit (°C)	105

表 5. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA821			
		SPECIFICATION	G = 1 ERROR (ppm)	G = 100 ERROR (ppm)	G = 1000 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C					
Input offset voltage (µV)	V_{OSI} / V_{DIFF}	35	35	350	3500
Output offset voltage (µV)	$V_{OSO} / (G \times V_{DIFF})$	350	350	350	350
Input offset current (nA)	$I_{OS} \times$ maximum $(R_{S+}, R_{S-}) / V_{DIFF}$	0.5	1	5	50
CMRR (dB) (min)	$V_{CM} / (10^{CMRR/20} \times V_{DIFF})$	92 (G = 1), 112 (G = 10), 132 (G = 100)	251	251	251
PSRR (dB) (min)	$(V_{CC} - V_S) / (10^{PSRR/20} \times V_{DIFF})$	110 (G = 1), 114 (G = 10), 130 (G = 100)	3	20	32
Gain error from INA (%) (max)	$GE(\%) \times 10^4$	0.02 (G = 1), 0.15 (G = 10, 100)	200	1500	1500
Gain error from external resistor RG (%) (max)	$GE(\%) \times 10^4$	0.01	100	100	100
Total absolute accuracy error (ppm) at 25°C, worst case	sum of all errors		940	2576	5738
Total absolute accuracy error (ppm) at 25°C, average	rms sum of all errors		487	1603	3834
DRIFT TO 105°C					
Gain drift from INA (ppm/°C) (max)	$GTC \times (T_A - 25)$	5 (G = 1), 35 (G = 10, 100)	400	2800	2800
Gain drift from external resistor RG (ppm/°C) (max)	$GTC \times (T_A - 25)$	10	800	800	800
Input offset voltage drift (µV/°C) (max)	$(V_{OSI\_TC} / V_{DIFF}) \times (T_A - 25)$	0.4	32	320	3200
Output offset voltage drift (µV/°C)	$[V_{OSO\_TC} / (G \times V_{DIFF})] \times (T_A - 25)$	5	400	400	400
Offset current drift (pA/°C)	$I_{OS\_TC} \times$ maximum $(R_{S+}, R_{S-}) \times (T_A - 25) / V_{DIFF}$	20	2	16	160
Total drift error to 105°C (ppm), worst case	sum of all errors		1634	4336	7360
Total drift error to 105°C (ppm), typical	rms sum of all errors		980	2957	4348
RESOLUTION					
Gain nonlinearity (ppm of FS)		10 (G = 1, 10), 15 (G = 100)	10	10	15
Voltage noise (@1 kHz) (µVpp)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left(\frac{e_{NO}}{G}\right)^2} \times \frac{6}{V_{DIFF}}$	$e_{NI} = 7$, $e_{NO} = 65$	1335	886	3566
Current noise (@1kHz) (pA/√Hz)	$I_N \times$ maximum $(R_{S+}, R_{S-}) \times$ sqrt $(BW) / V_{DIFF}$	0.13	0.4	2	11
Total resolution error (ppm), worst case	sum of all errors		1345	896	3581
Total resolution error (ppm), typical	rms sum of all errors		1335	886	3566
TOTAL ERROR					
Total error (ppm), worst case	sum of all errors		3919	7808	16724
Total error (ppm), typical	rms sum of all errors		1726	3478	6806

8.4 Device Functional Modes

The INA821 has a single functional mode and is operational when the power supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA821 is 36 V (±18 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reference Pin

The output voltage of the INA821 is developed with respect to the voltage on the reference pin (REF.) Often in dual-supply operation, the reference pin (pin 6) connects to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA821 drives a single-supply ADC.

The voltage source applied to the reference pin must have a low output impedance. As shown in 图 65, any resistance at the reference pin (R_{REF} in 图 65) is in series with one of the internal 10-kΩ resistors.

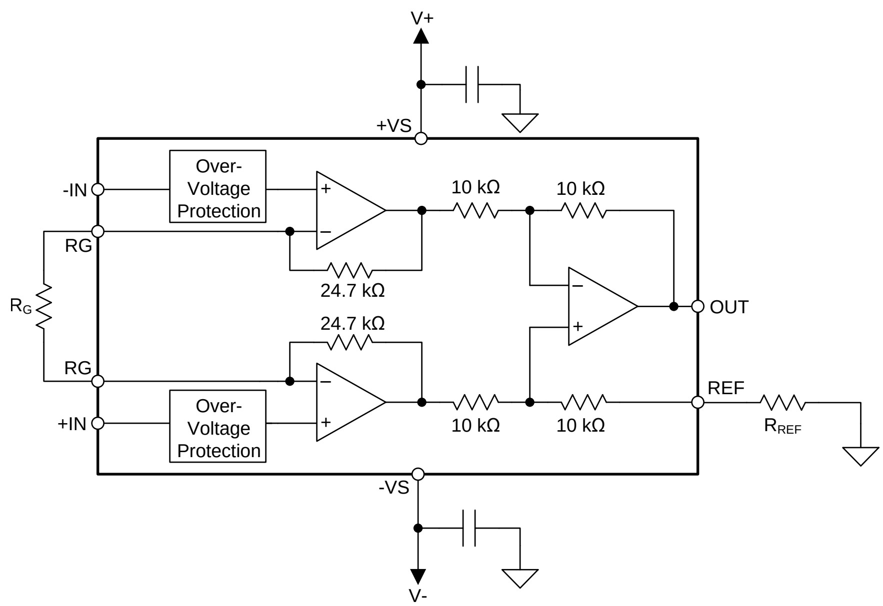


图 65. Parasitic Resistance Shown at the Reference Pin

The parasitic resistance at the reference pin (R_{REF}) creates an imbalance in the four resistors of the internal difference amplifier, resulting in degraded common-mode rejection ratio (CMRR). 图 66 shows the degradation in CMRR of the INA821 for increasing resistance at the reference pin. For the best performance, keep the source impedance to the REF pin (R_{REF}) below 5 Ω.

Application Information (接下页)

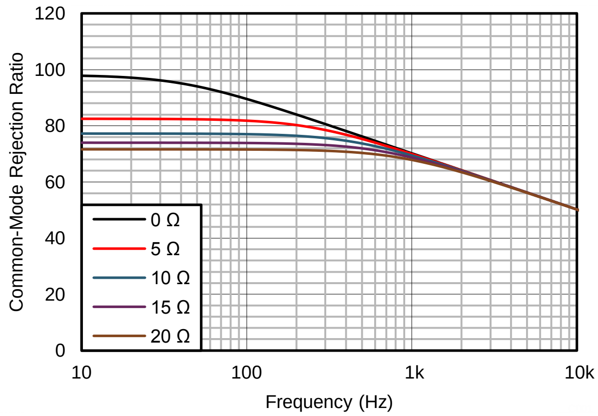


图 66. The Effect of Increasing Resistance at the Reference Pin

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp as shown in 图 67 to avoid CMRR degradation.

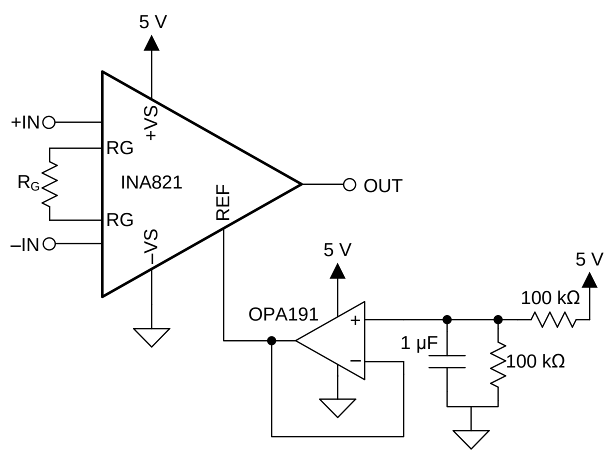


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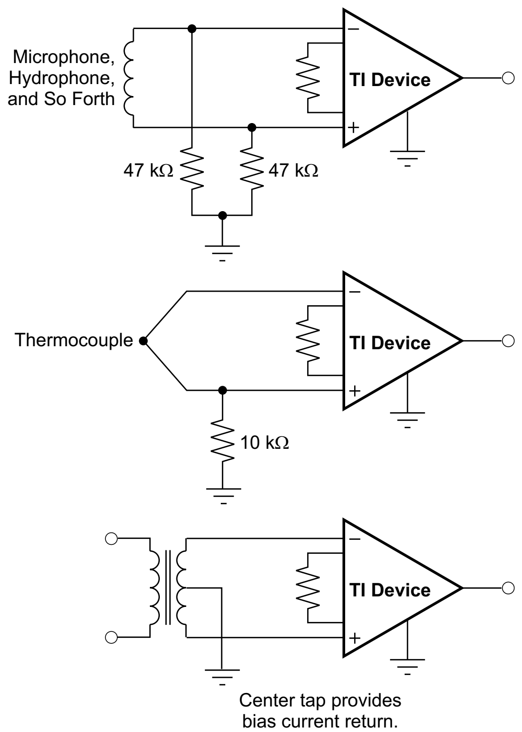
图 67. Using an Op Amp to Buffer Reference Voltages

9.1.2 Input Bias Current Return Path

The input impedance of the INA821 is extremely high (approximately 100 GΩ.) However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 图 68 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA821 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in 图 68). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

Application Information (接下页)



(1) Center tap provides bias current return.

图 68. Providing an Input Common-Mode Current Path

9.2 Typical Application

图 69 shows a three-pin programmable-logic controller (PLC) design for the INA821. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Typically, PLCs have these input and output ranges.

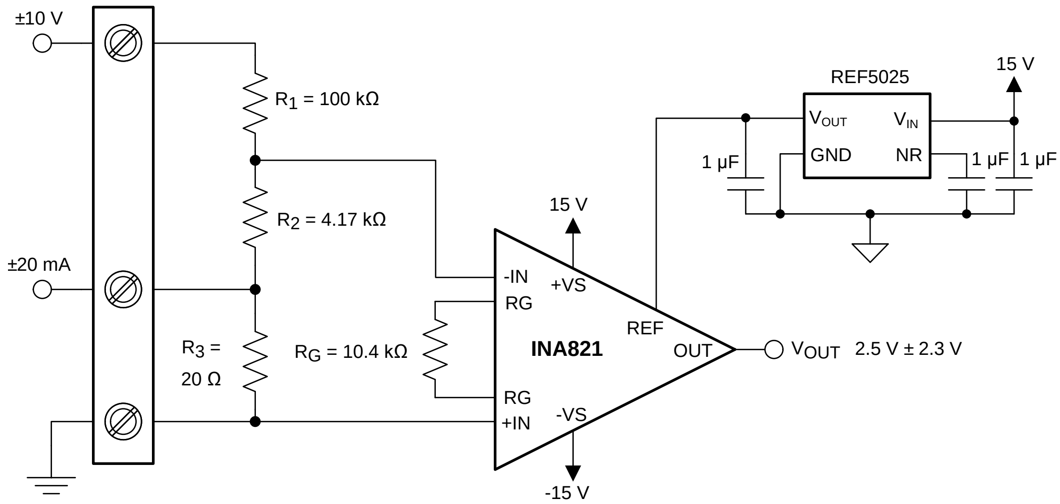


图 69. PLC Input (±10 V, 4 mA to 20 mA)

9.2.1 Design Requirements

For this application, the design requirements are:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20 mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

9.2.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 图 69: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, 公式 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF}$$

where

- G represents the gain of the instrumentation amplifier
- V_D represents the differential voltage at the INA821 inputs
- V_{REF} is the voltage at the INA821 REF pin
- I_{IN} is the input current (3)

公式 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF}$$

where

- V_{IN} is the input voltage (4)

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. The R_1 value is 100 kΩ because increasing the R_1 value increases noise. The value of R_3 must be small compared to R_1 and R_2. The value of R_3 is 20 Ω because that resistance value is smaller than R_1 and yields an input voltage of ±400 mV when operating in current mode (±20 mA).

Typical Application (接下页)

Use 公式 5 to calculate R_2 if V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ \text{k}\Omega \quad (5)$$

The value from 公式 5 is not a standard 0.1% value, so 4.17 kΩ is selected. R_1 and R_2 use 0.1% tolerance resistors to minimize error.

Use 公式 6 to calculate the gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ \text{V} - 2.5\ \text{V}}{400\ \text{mV}} = 5.75\ \frac{\text{V}}{\text{V}} \quad (6)$$

公式 7 calculates the gain-setting resistor value using the INA821 gain equation (公式 1.)

$$R_G = \frac{49.4\ \text{k}\Omega}{G - 1} = \frac{49.4\ \text{k}\Omega}{5.75 - 1} = 10.4\ \text{k}\Omega \quad (7)$$

Use a standard 0.1% resistor value of 10.5 kΩ for this design.

9.2.3 Application Curves

图 70 and 图 71 show typical characteristic curves for the circuit in 图 69.

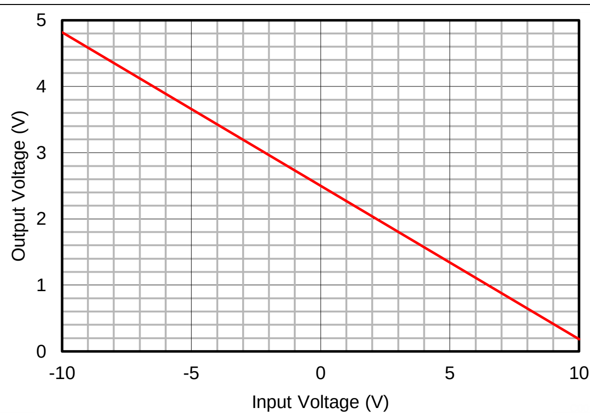


图 70. PLC Output Voltage vs Input Voltage

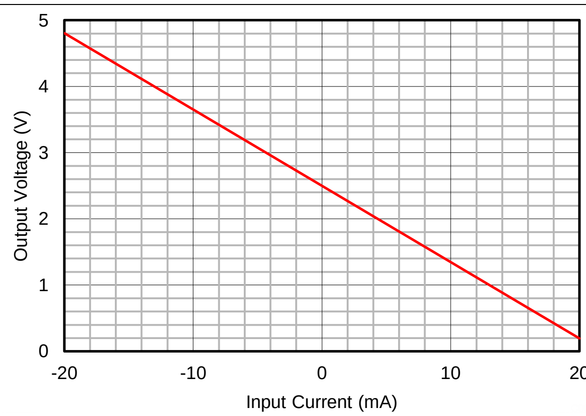


图 71. PLC Output Voltage vs Input Current

9.3 Other Application Examples

9.3.1 Resistance Temperature Detector Interface

图 72 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 to 5 V. The linearization technique employed is described in *Analog linearization of resistance temperature detectors*. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.

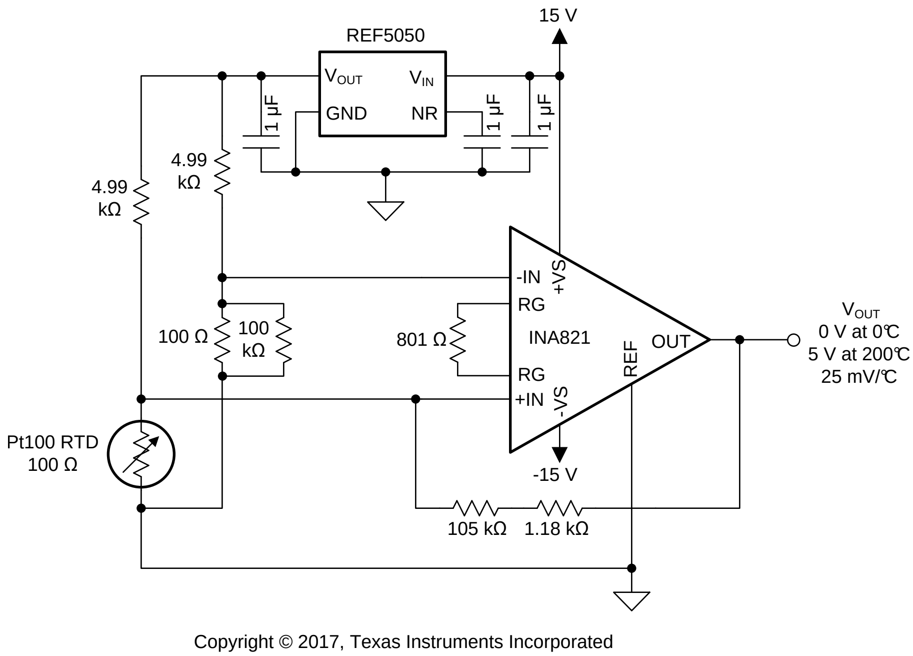


图 72. A 3-Wire Interface for RTDs With Analog Linearization

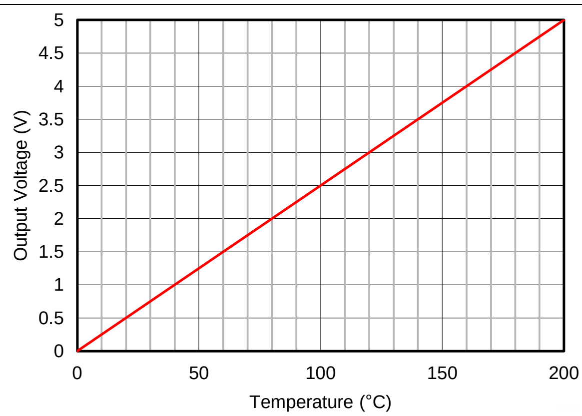


图 73. Transfer Function of 3-Wire RTD Interface

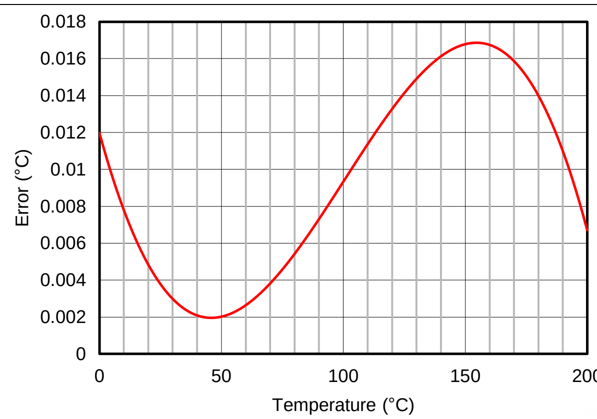


图 74. Temperature Error Over Full Temperature Range

10 Power Supply Recommendations

The nominal performance of the INA821 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device operates using power supplies from ±2.25 V (4.5 V) to ±18 V (36 V) and non midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in *Typical Characteristics*.

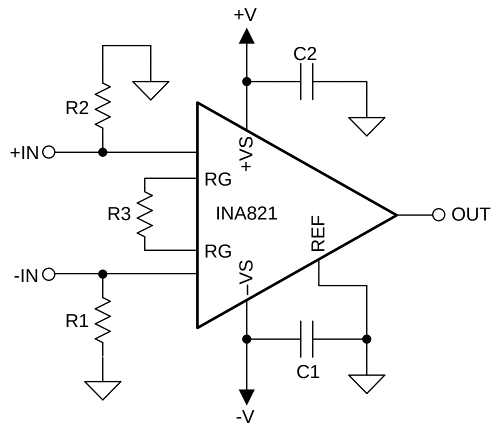
11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 75, keep R_G close to the pins to minimize parasitic capacitance.
- Keep the traces as short as possible.

11.2 Layout Example



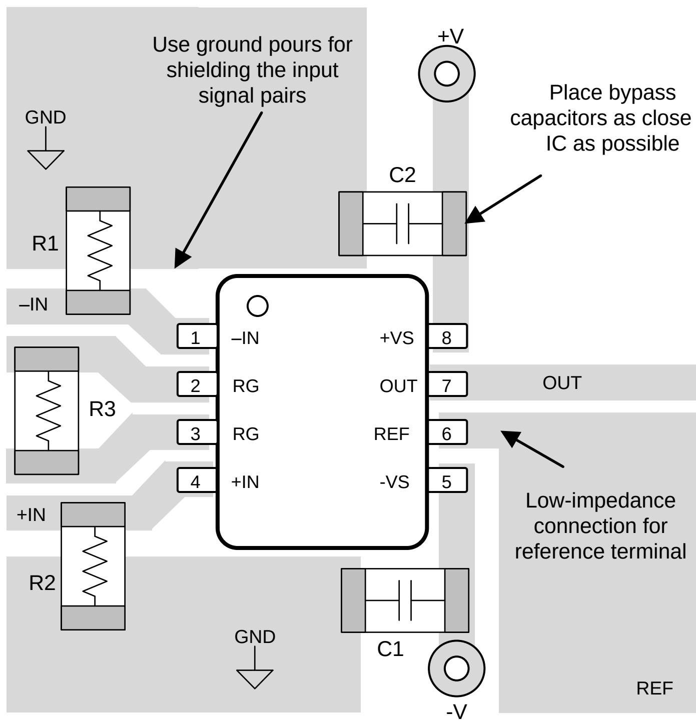


图 75. Example Schematic and Associated PCB Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《REF50xx 低噪声、极低温漂、高精度电压基准》*
- *OPA191 低功耗精密 36V e-trim CMOS 放大器*
- TINA-TI 软件文件夹
- INA 共模范围计算器

12.2 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA821ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821	Samples
INA821IDGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
INA821IDGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
INA821IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA821	Samples
XINA821IDGKT	ACTIVE	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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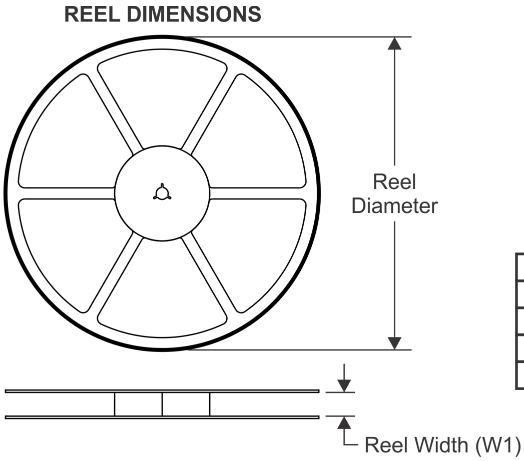
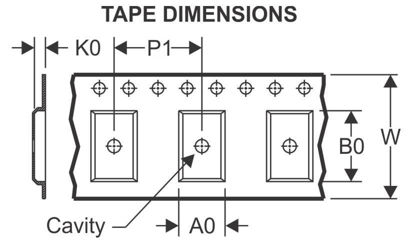
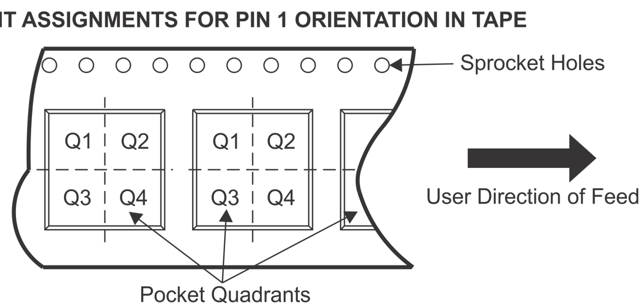
TAPE AND REEL INFORMATION





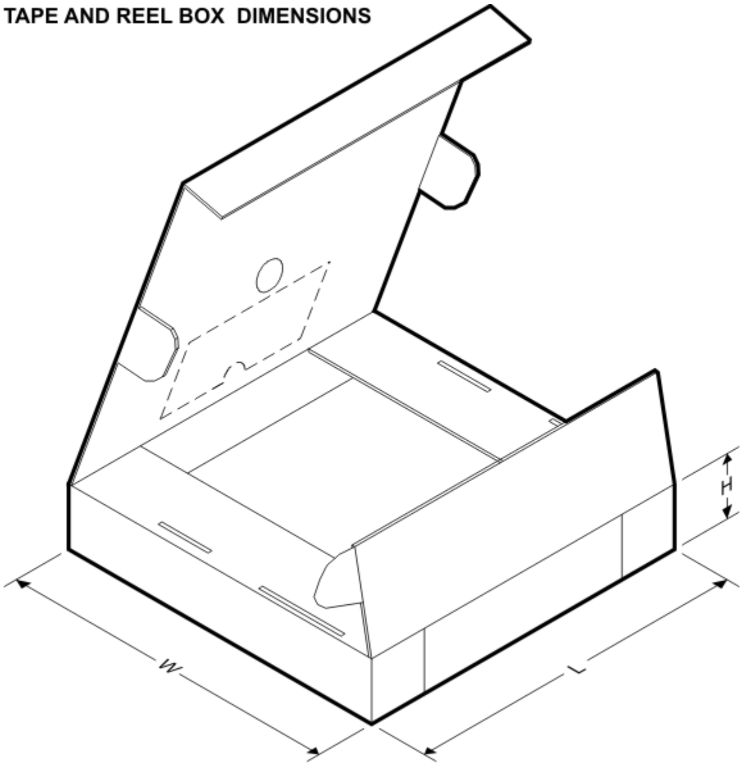
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

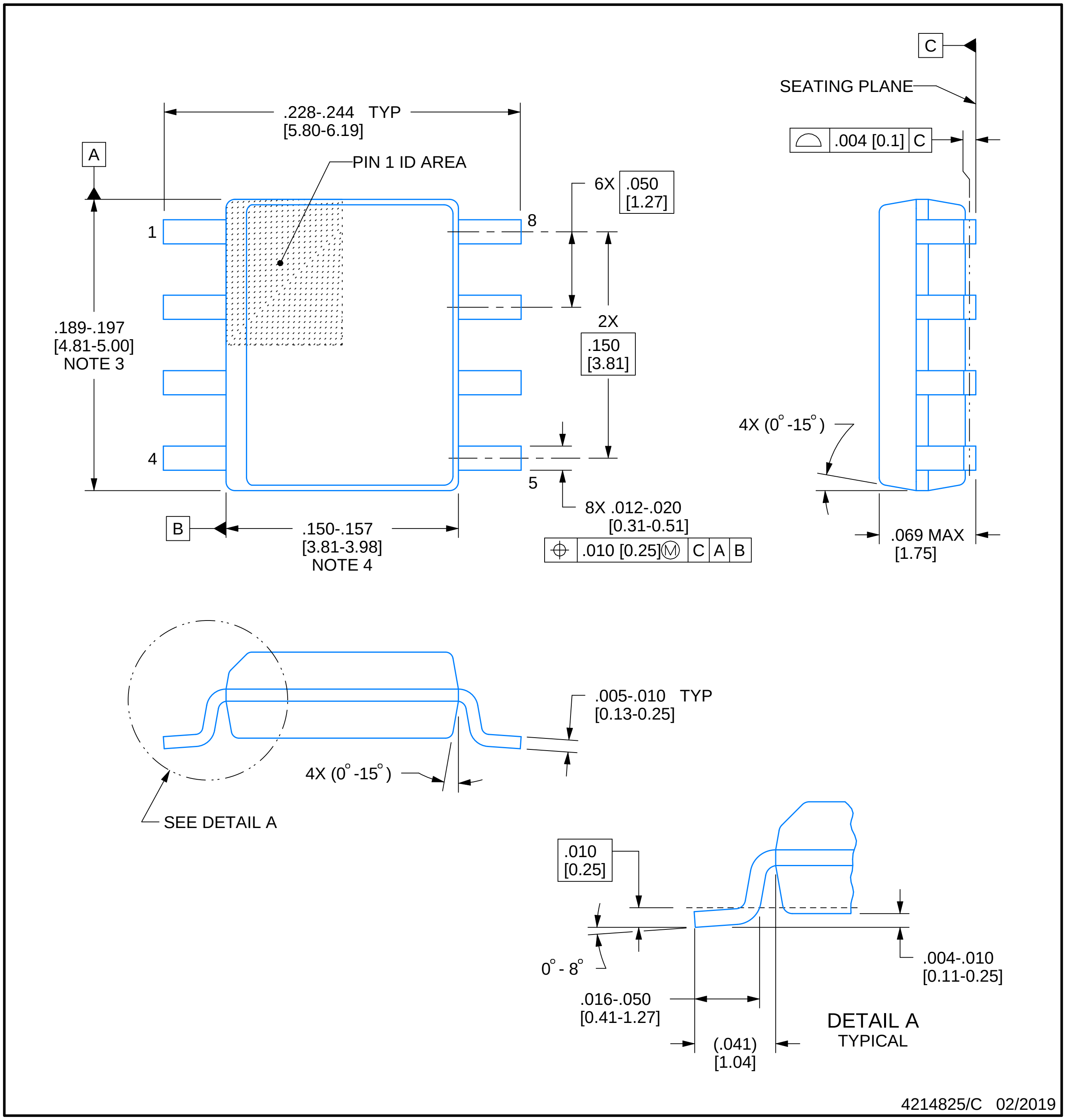
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA821IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



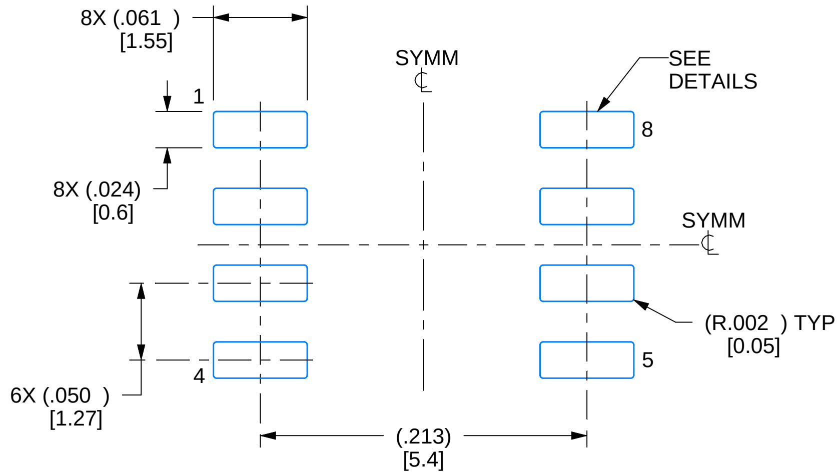
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA821IDR	SOIC	D	8	2500	367.0	367.0	35.0

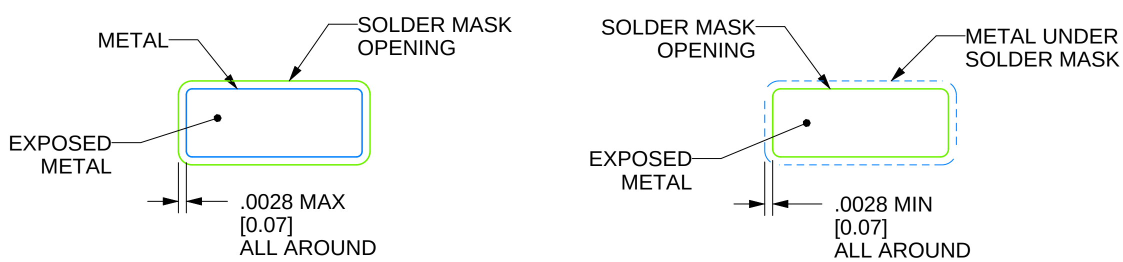


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

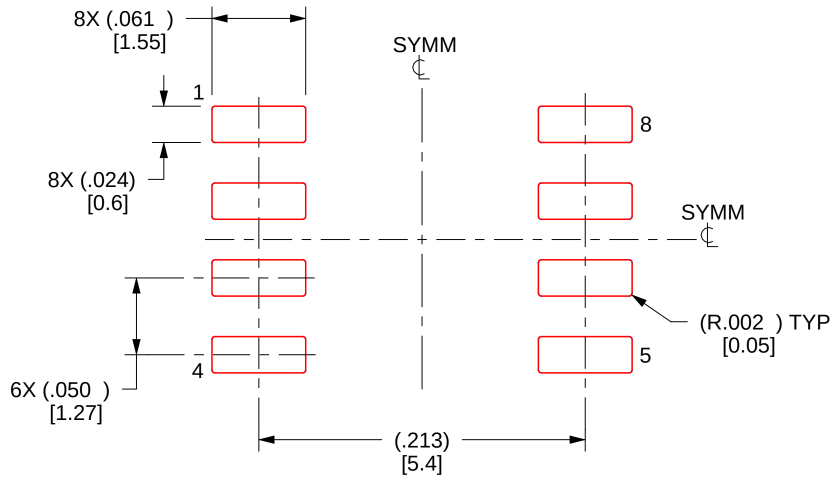
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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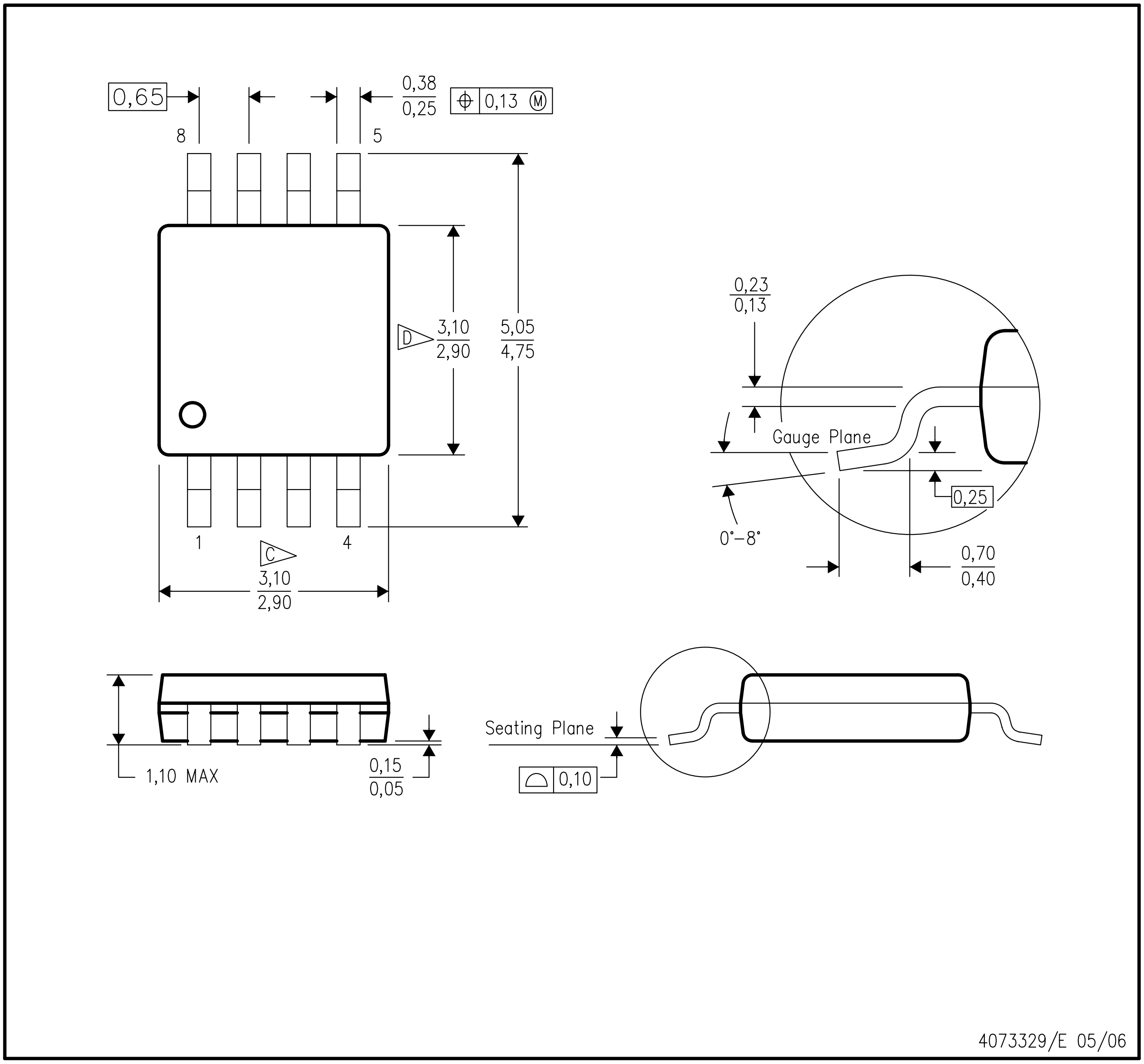
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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