



高共模电压差动放大器

特性

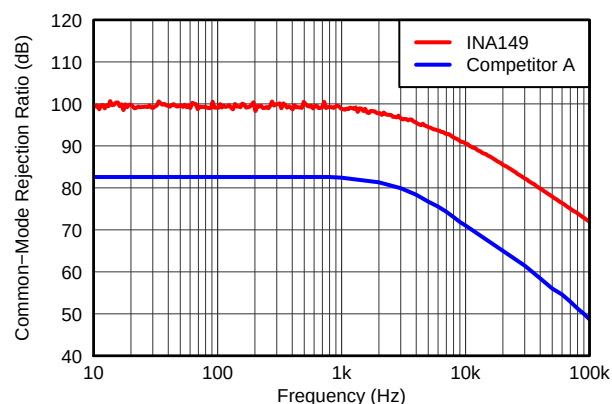
- 共模电压范围: **$\pm 275\text{ V}$**
- 最小共模抑制比 (CMRR): 在 -55°C 至 $+125^{\circ}\text{C}$ 间为 **84 dB**
- **DC** 规范
 - 最大偏移电压: **$3500\text{ }\mu\text{V}$**
 - 最大增益误差: **0.047%**
 - 最大增益非线性: **0.001% FSR** 在 25°C
- **AC** 性能
 - 带宽: **500 kHz**
 - 典型转换率: **$5\text{ V}/\mu\text{s}$**
- 宽电源电压范围: **$\pm 2.0\text{ V}$ 至 $\pm 18\text{ V}$**
 - 最大静态电流: **$1100\text{ }\mu\text{A}$**
 - **$\pm 15\text{-V}$** 电源上的输出摆幅: **$\pm 13.5\text{ V}$**
- 输入保护
 - 共模电压: **$\pm 500\text{ V}$**
 - 差分电压: **$\pm 500\text{ V}$**

应用

- 高压电流感应
- 电池电压监视
- 电源电流监视
- 电机控制
- 隔离电路的替代产品

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装/测试场所
- 一个制造场所
- 军用温度范围 ($-55^{\circ}\text{C}/125^{\circ}\text{C}$) 内可用⁽¹⁾
- 拓展的产品使用寿命
- 拓展的产品变更通知
- 产品可追溯性



(1) 可提供额外温度范围-请与厂家联系

说明

INA149 是一款高精度单位增益差动放大器, 此放大器具有很高的输入共模电压范围。它是一款包含有高精度运算放大器和集成薄膜电阻器网路的单一单片器件。INA149 能够精确测量高达 $\pm 275\text{ V}$ 的共模信号出现时的小额差分电压。INA149 输入受到瞬时共模或者高达 500 V 的差分过载保护。

在很多无需电流隔离的应用中, INA149 可以取代隔离放大器。此功能可以省去昂贵的隔离的输入端电源并去除相关纹波、噪音和静态电流。INA149 出色的 0.0005% 非线性和 500-kHz 带宽特性使之优于传统隔离放大器。

INA149 与 INA117-和 INA148-类型高共模电压放大器引脚兼容并且提供优于上述两设备的性能。INA149 采用小外形尺寸集成电路 (SOIC)-8 封装。此器件额定军用温度范围介于 -55°C 至 $+125^{\circ}\text{C}$ 。



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English Data Sheet: **SBOS608**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	ORDERABLE PART NUMBER	PACKAGE MARKING	VID NUMBER
-55°C to 125°C	SOIC-8 - D	INA149AMDREP	INA149AM	V62/12614-01XE

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		INA149	UNIT
Supply voltage	(V+) – (V–)	40	V
Input voltage range	Continuous	300	V
Common-mode and differential, 10 s		500	V
Maximum Voltage on REF _A and REF _B		(V–) – 0.3 to (V+) + 0.3	V
Input current on any input pin ⁽²⁾		10	mA
Output short-circuit current duration		Indefinite	
Operating temperature range		–55 to +125	°C
Storage temperature range		–65 to +150	°C
Junction temperature		+150	°C
ESD rating	Human body model (HBM)	1500	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	100	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) REF_A and REF_B are diode clamped to the power-supply rails. Signals applied to these pins that can swing more than 0.3 V beyond the supply rails should be limited to 10 mA or less.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		INA149	UNITS
		D (SOIC)	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	110	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	57	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	54	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	11	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	53	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS: V+ = +15 V and V– = –15 V

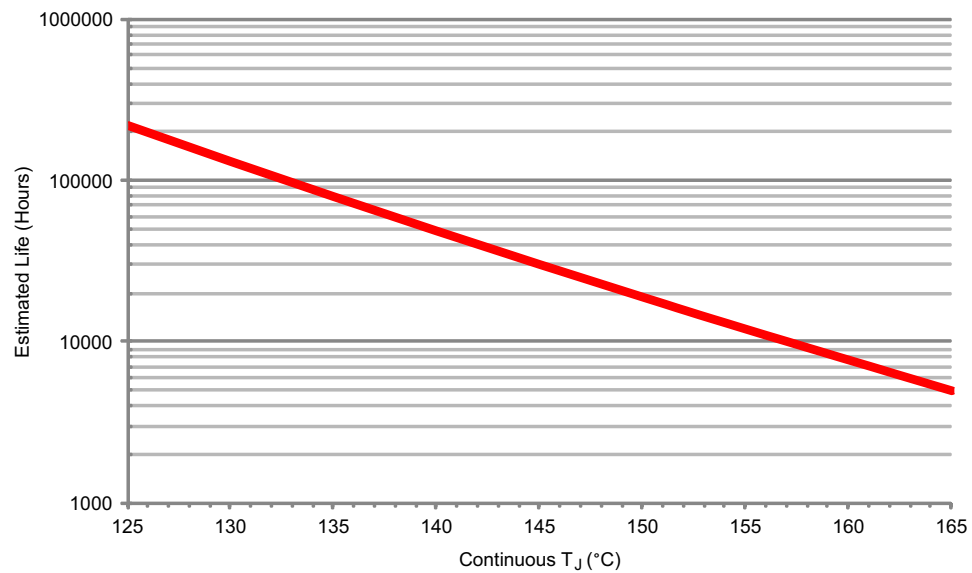
At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_{CM} = \text{REF}_A = \text{REF}_B = \text{GND}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	INA149			UNIT
		MIN	TYP	MAX	
GAIN					
Initial	V _{OUT} = ±10.0 V,	1			V/V
Gain error	V _{OUT} = ±10.0 V, T _A = −55°C to +125°C	±0.005	±0.047	%FSR	
Gain	vs temperature, T _A = −55°C to +125°C	±1.5	ppm/°C		
Nonlinearity		±0.0005	±0.001	%FSR	
OFFSET VOLTAGE					
Initial offset	T _A = −55°C to +125°C	350	3500	μV	
	vs temperature, T _A = −55°C to +125°C	2.5	μV/°C		
	vs supply (PSRR), V _S = ±2 V to ±18 V, T _A = −55°C to +125°C	90	120	dB	
INPUT					
Impedance	Differential	800			kΩ
	Common-mode	200			kΩ
Voltage range	Differential	−13.5	13.5	V	
	Common-mode	−275	275	V	
Common-mode rejection (CMRR)	At dc, V _{CM} = ±275 V, T _A = −55°C to +125°C	84	98	dB	
	At ac, 500 Hz, V _{CM} = 500 V _{PP}	90			dB
	At ac, 1 kHz, V _{CM} = 500 V _{PP}	90			dB
OUTPUT					
Voltage range	T _A = −55°C to +125°C	−13.5	13.5	V	
Short-circuit current		±25			mA
Capacitive load drive	No sustained oscillations	10			nF
OUTPUT NOISE VOLTAGE					
0.01 Hz to 10 Hz		20			μV _{PP}
10 kHz		550			nV/√Hz
DYNAMIC RESPONSE					
Small-signal bandwidth		500			kHz
Slew rate	V _{OUT} = ±10-V step, T _A = −55°C to +125°C	1.7	5	V/μs	
Full-power bandwidth	V _{OUT} = 20 V _{PP}	32			kHz
Settling time	0.01%, V _{OUT} = 10-V step	7			μs
POWER SUPPLY					
Voltage range		±2	±18	V	
Quiescent current	V _S = ±18 V, V _{OUT} = 0 V	810	950	μA	
	vs temperature, T _A = −55°C to +125°C	0.95	1.1	mA	
TEMPERATURE RANGE					
Specified		−55	+125	°C	
Operating		−55	+125	°C	
Storage		−65	+150	°C	

ELECTRICAL CHARACTERISTICS: $V_+ = 5\text{ V}$ and $V_- = 0\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to 2.5 V , and $V_{CM} = \text{REF}_A = \text{REF}_B = 2.5\text{ V}$, unless otherwise noted.

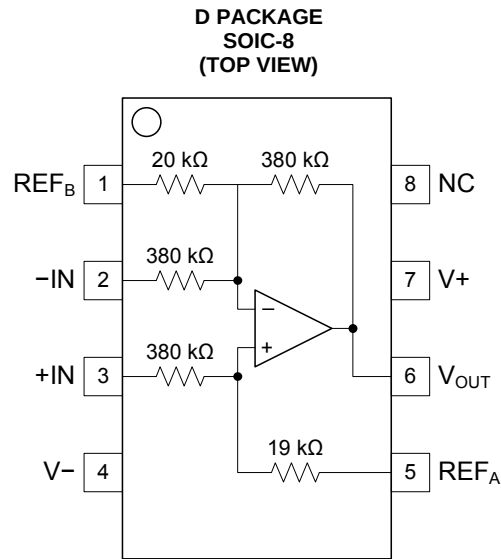
PARAMETER	TEST CONDITIONS	INA149			UNIT
		MIN	TYP	MAX	
GAIN					
Initial	V _{OUT} = 1.5 V to 3.5 V	1			V/V
Gain error	V _{OUT} = 1.5 V to 3.5 V	±0.005			%FSR
Gain	vs temperature, T _A = −55°C to +125°C	±1.5			ppm/°C
Nonlinearity		±0.0005			%FSR
OFFSET VOLTAGE					
Initial offset		350			μV
	vs temperature, T _A = −55°C to +125°C	3			μV/°C
	vs supply (PSRR), V _S = 4 V to 5 V	120			dB
INPUT					
Impedance	Differential	800			kΩ
	Common-mode	200			kΩ
	Common-mode	−20	25		V
Common-mode rejection	At dc, V _{CM} = −20 V to 25 V	100			dB
	vs temperature, T _A = −55°C to +125°C, at dc	100			dB
	At ac, 500 Hz, V _{CM} = 49 V _{PP}	100			dB
	At ac, 1 kHz, V _{CM} = 49 V _{PP}	90			dB
OUTPUT					
Voltage range		1.7	3.4		V
Short-circuit current		±15			mA
Capacitive load drive	No sustained oscillations	10			nF
OUTPUT NOISE VOLTAGE					
0.01 Hz to 10 Hz		20			μV _{PP}
10 kHz		550			nV/√Hz
DYNAMIC RESPONSE					
Small-signal bandwidth		500			kHz
Slew rate	V _{OUT} = 2 V _{PP} step	5			V/μs
Full-power bandwidth	V _{OUT} = 2 V _{PP}	32			kHz
Settling time	0.01%, V _{OUT} = 2 V _{PP} step	7			μs
POWER SUPPLY					
Voltage range		5			V
Quiescent current	V _S = 5 V	810			μA
	vs temperature, T _A = −55°C to +125°C	1			mA



- A. See datasheet for absolute maximum and minimum recommended operating conditions.
- B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. INA149 Wirebond Life Derating Chart

PIN CONFIGURATION



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
-IN	2	Inverting input
+IN	3	Noninverting input
NC	8	No internal connection
REF _A	5	Reference input
REF _B	1	Reference input
V-	4	Negative power supply
V+	7	Positive power supply ⁽¹⁾
V _{OUT}	6	Output

(1) In this document, (V+) – (V-) is referred to as V_S.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

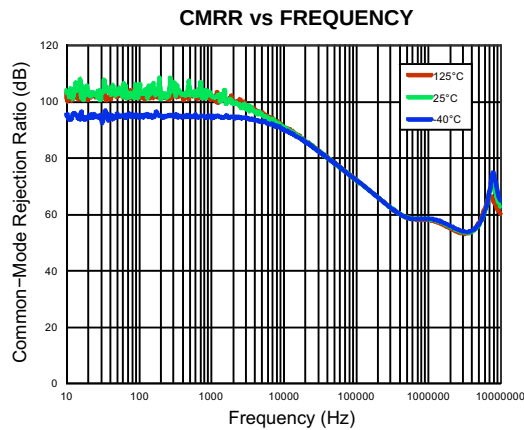


Figure 2.

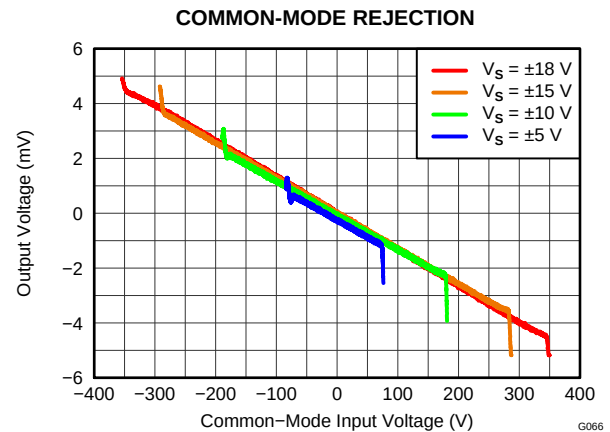


Figure 3.

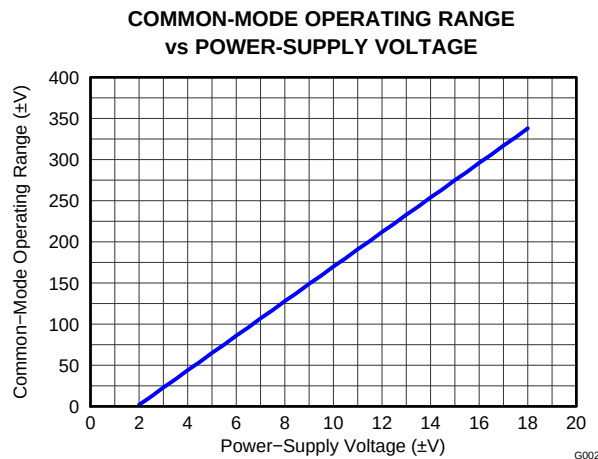


Figure 4.

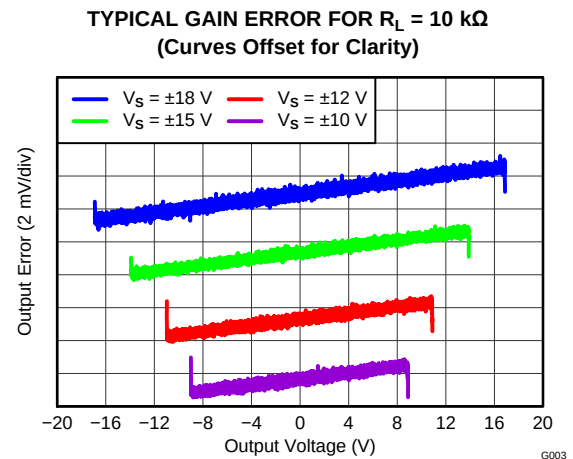


Figure 5.

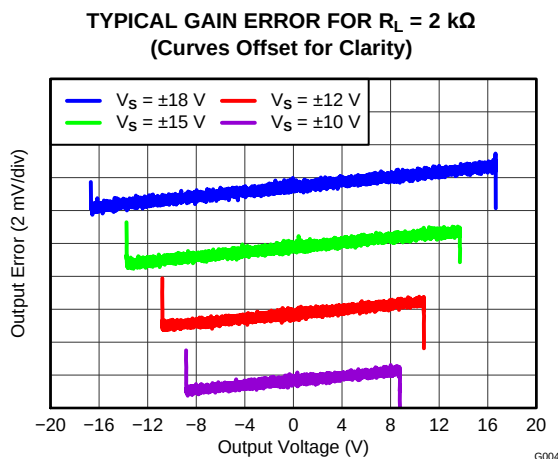


Figure 6.

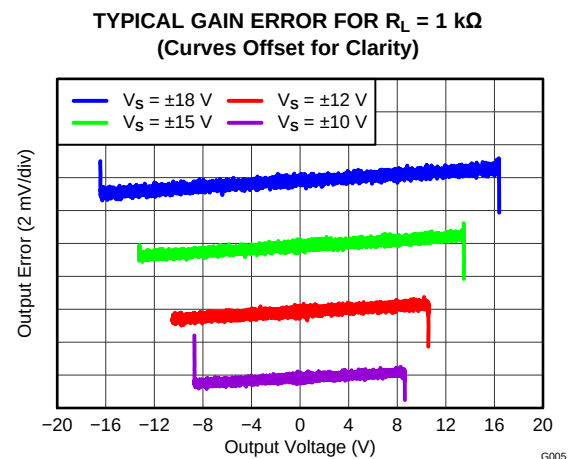


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

TYPICAL GAIN ERROR FOR LOW SUPPLY VOLTAGES (Curves Offset for Clarity)

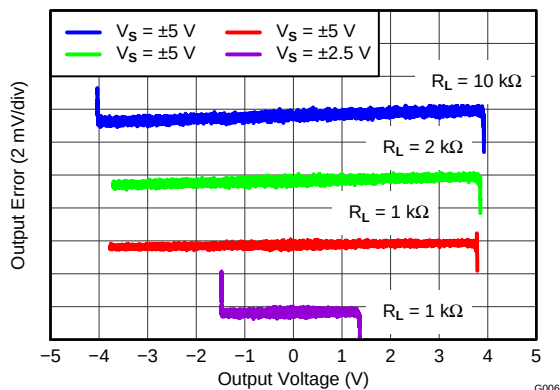


Figure 8.

GAIN NONLINEARITY

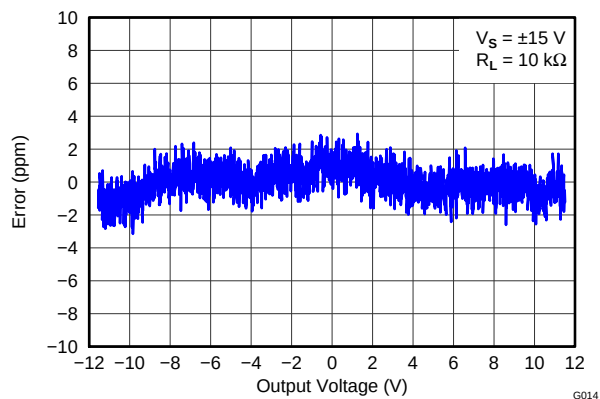


Figure 9.

GAIN NONLINEarity

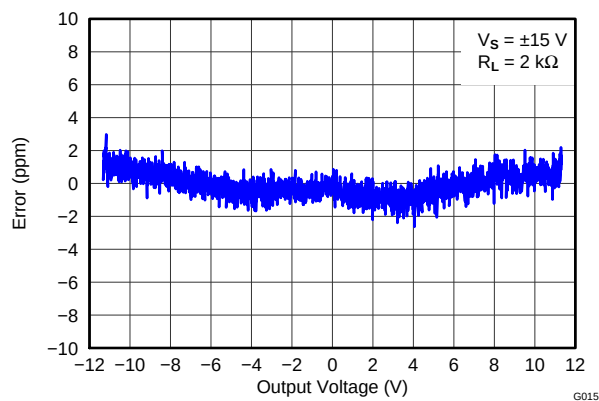


Figure 10.

GAIN NONLINEarity

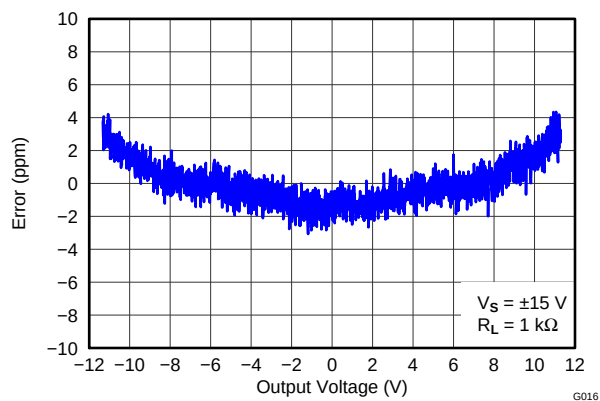


Figure 11.

GAIN NONLINEarity

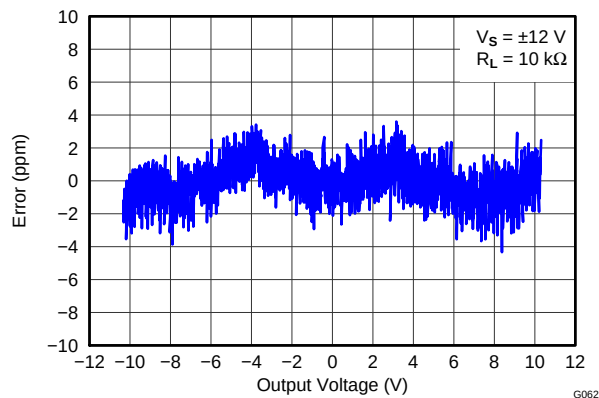


Figure 12.

OUTPUT VOLTAGE vs LOAD CURRENT

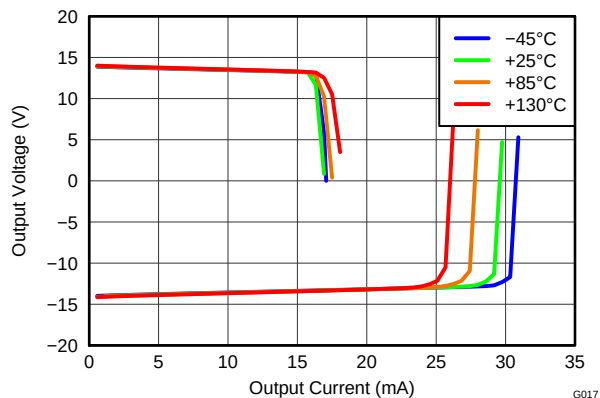


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

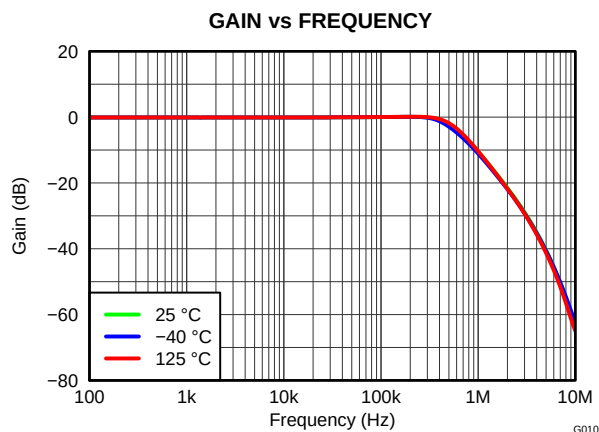


Figure 14.

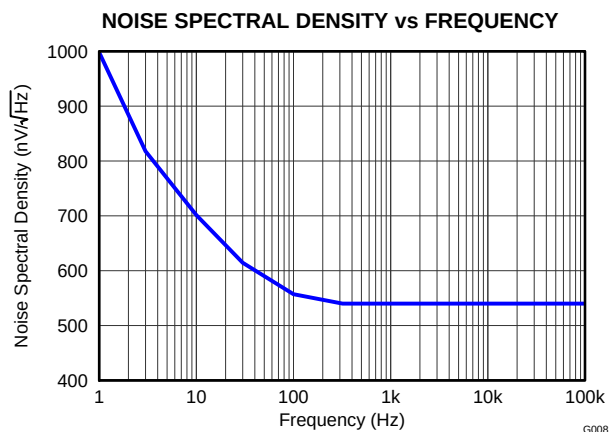


Figure 15.

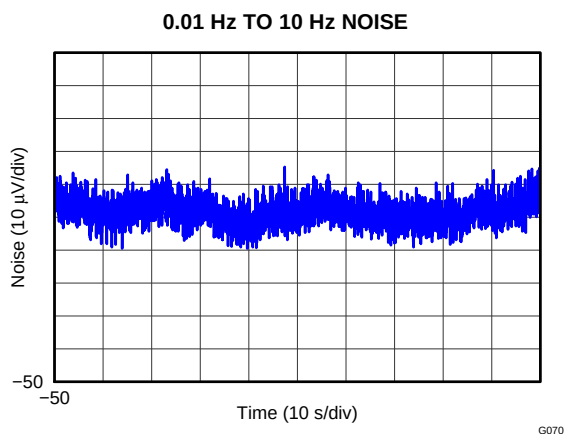


Figure 16.

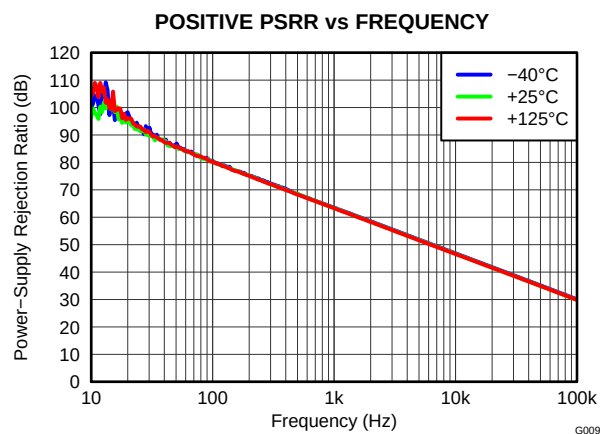


Figure 17.

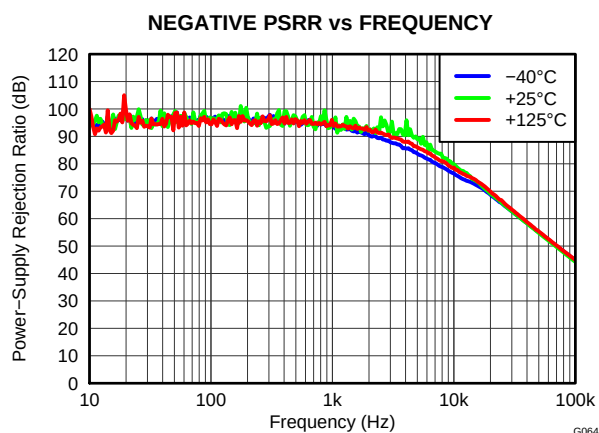


Figure 18.

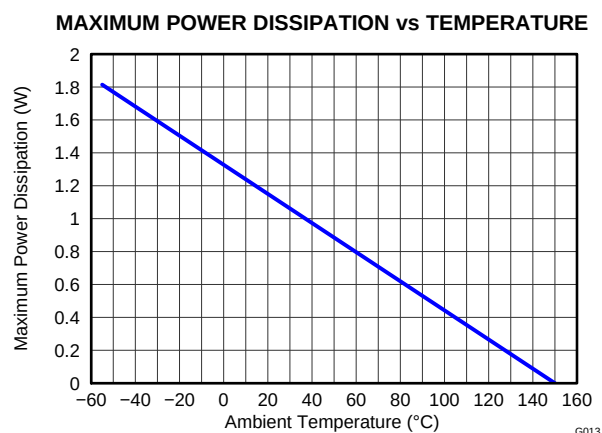


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

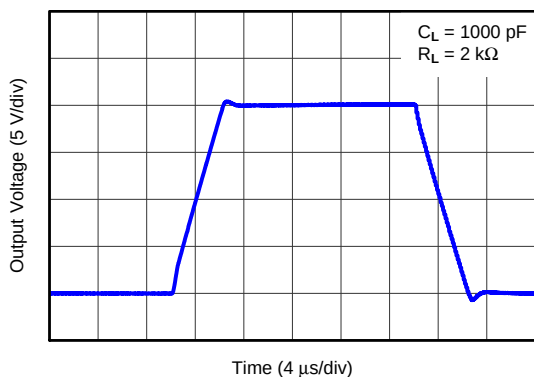


Figure 20.

G011

SMALL-SIGNAL STEP RESPONSE

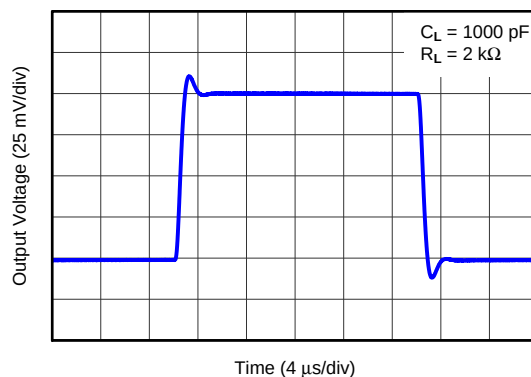


Figure 21.

G012

SMALL-SIGNAL RESPONSE vs CAPACITIVE LOAD

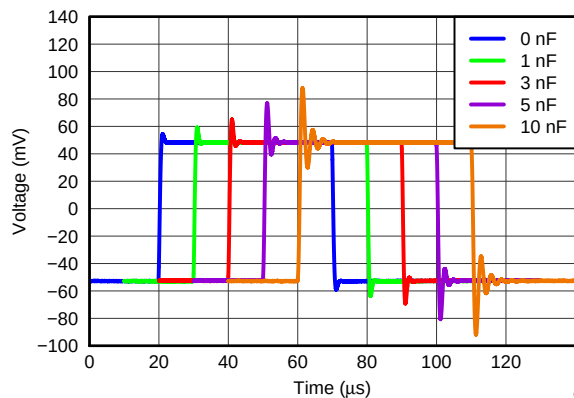


Figure 22.

G065

SETTLING TIME

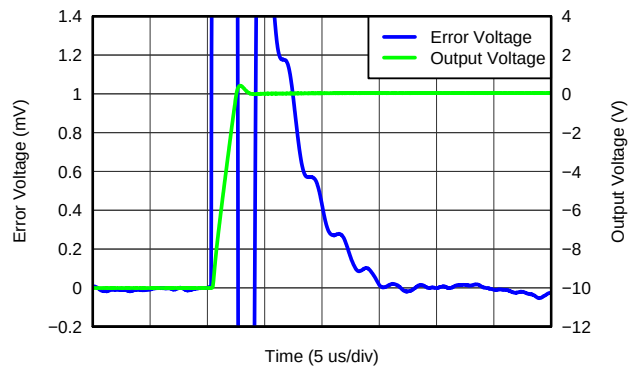


Figure 23.

G018

SETTLING TIME

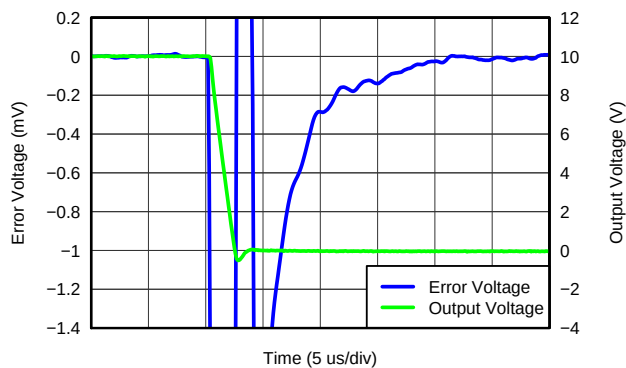


Figure 24.

G063

CMRR HISTOGRAM

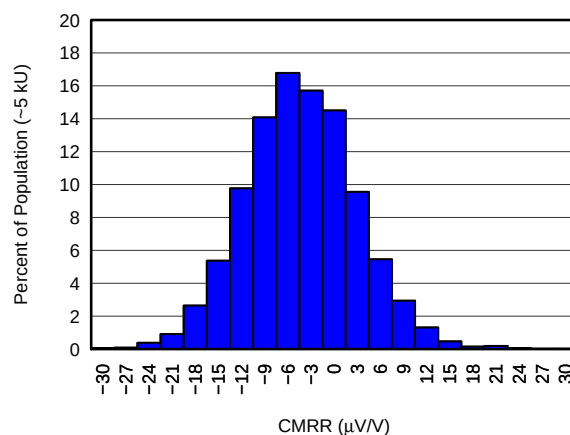


Figure 25.

G019

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

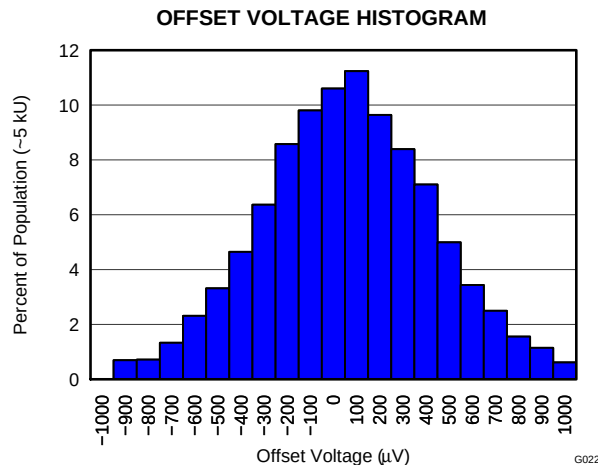


Figure 26.

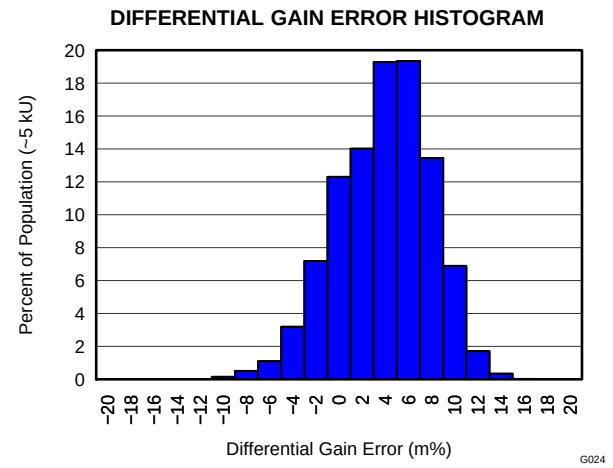


Figure 27.

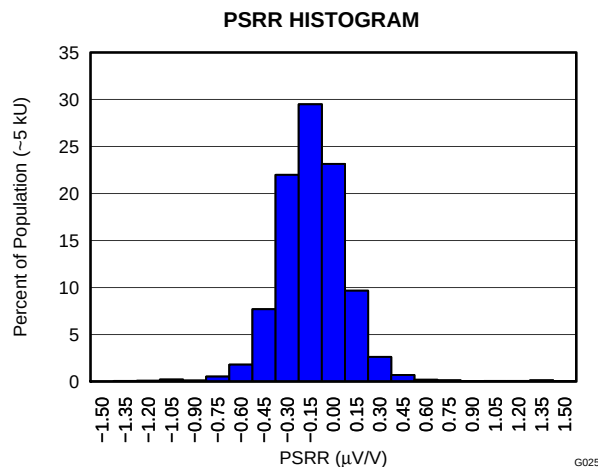


Figure 28.

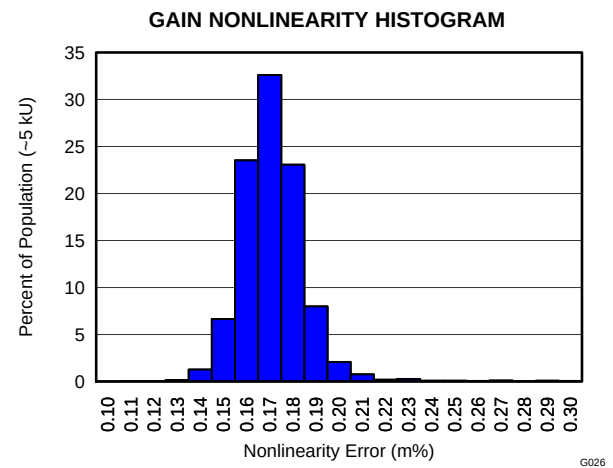


Figure 29.

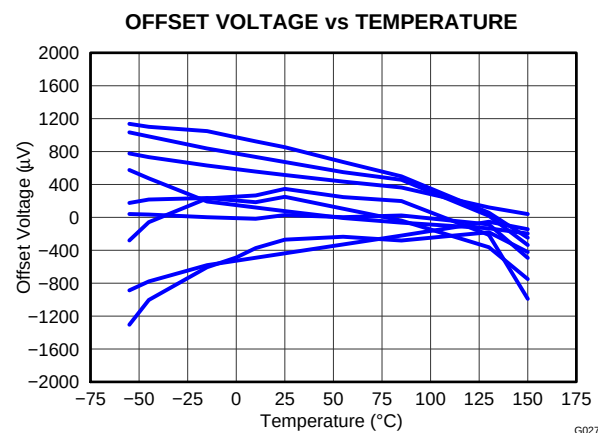


Figure 30.

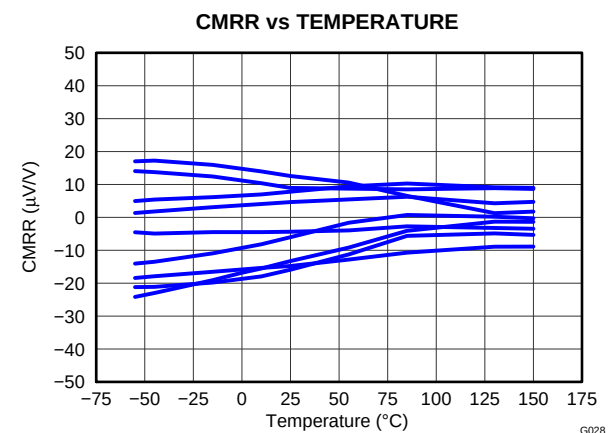


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

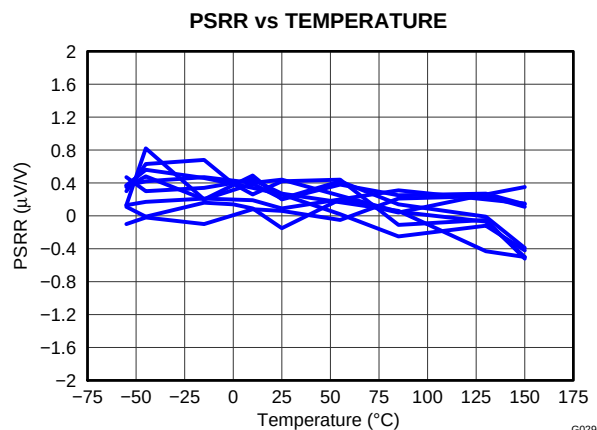


Figure 32.

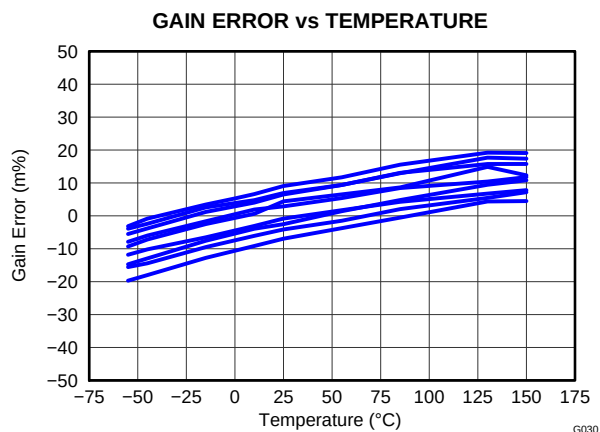


Figure 33.

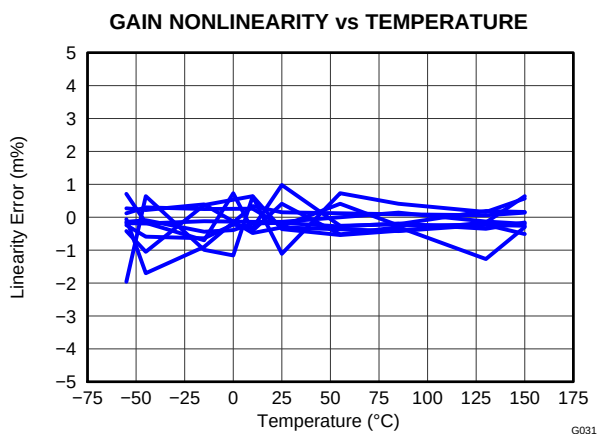


Figure 34.

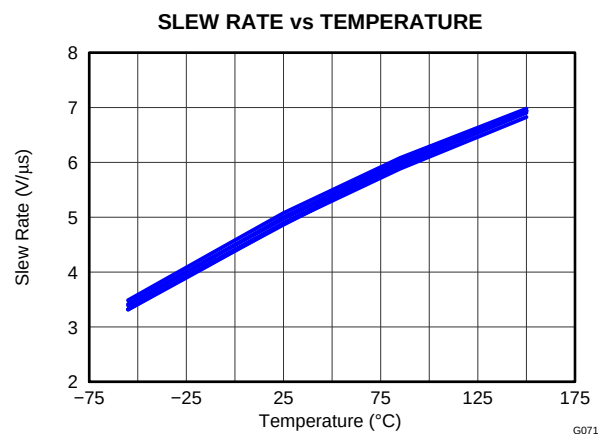


Figure 35.

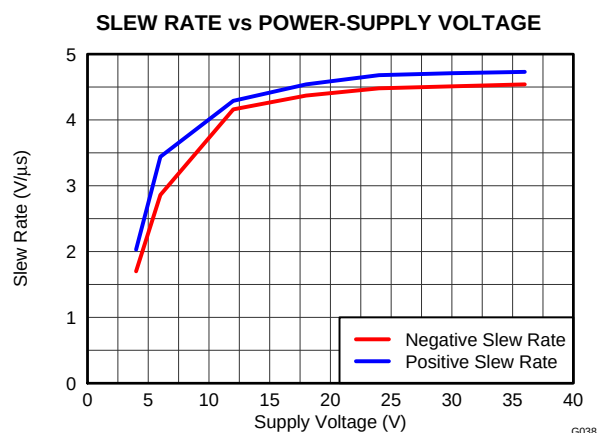


Figure 36.

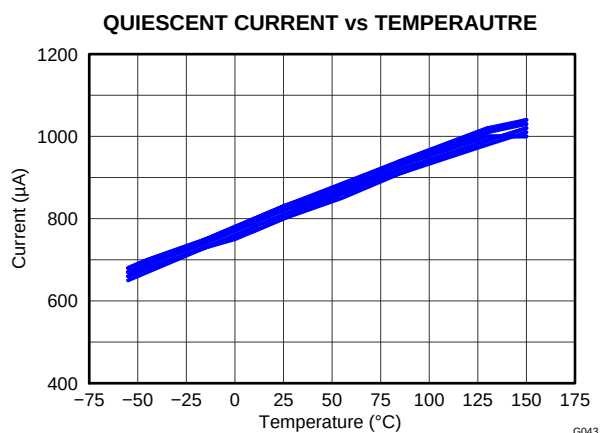


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$ connected to ground, and $V_S = \pm 15\text{ V}$, unless otherwise noted.

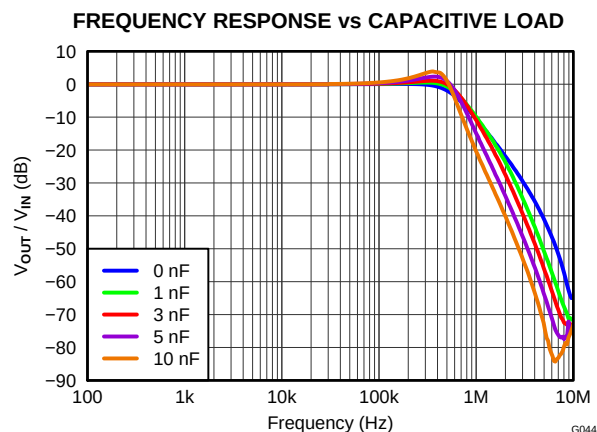


Figure 38.

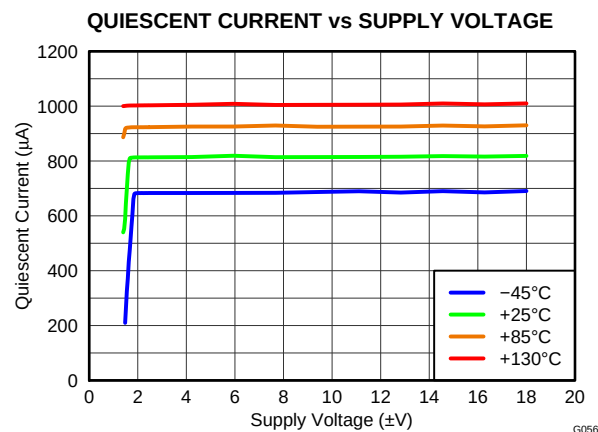


Figure 39.

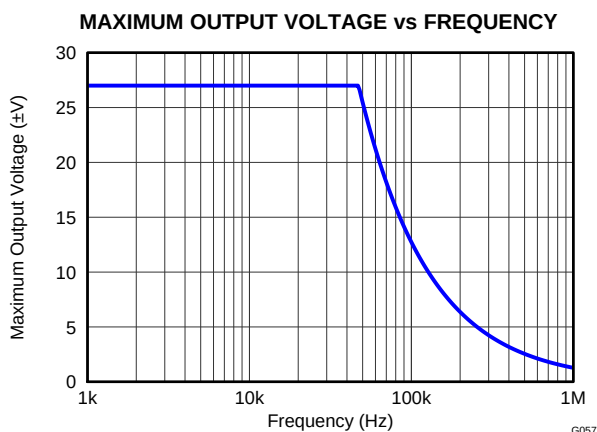


Figure 40.

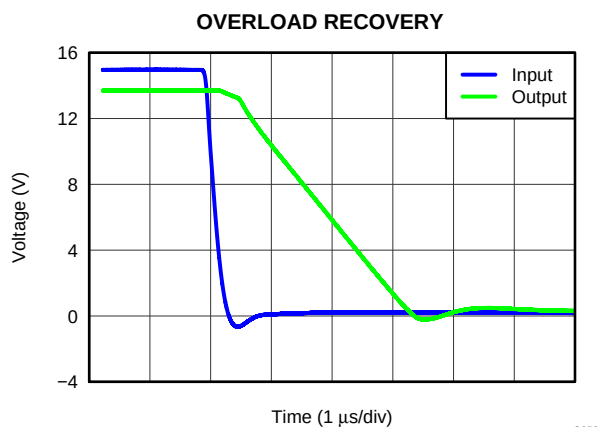


Figure 41.

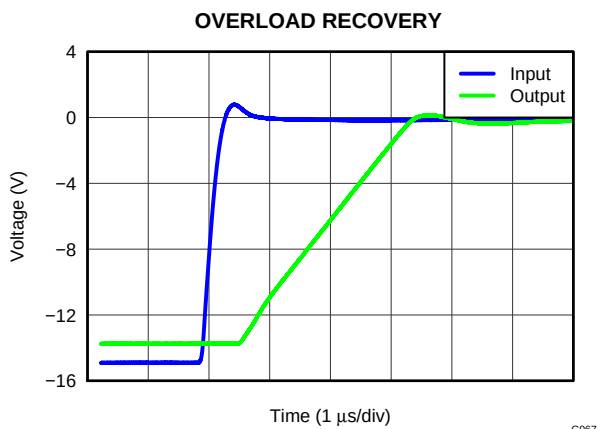


Figure 42.

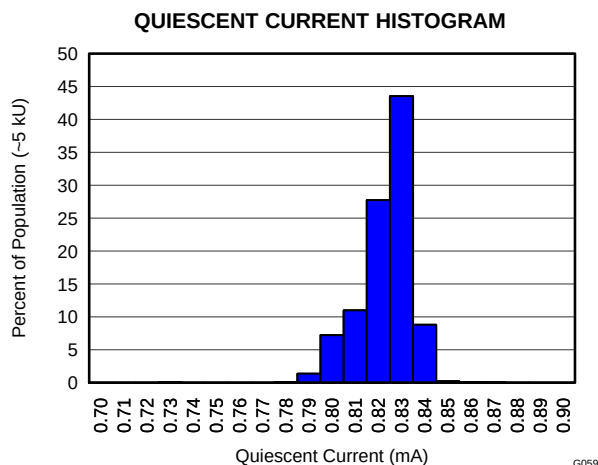


Figure 43.

APPLICATION INFORMATION

BASIC INFORMATION

Figure 44 shows the basic connections required for dual-supply operation. Applications with noisy or high-impedance power-supply lines may require decoupling capacitors placed close to the device pins. The output voltage is equal to the differential input voltage between pins 2 and 3. The common-mode input voltage is rejected. Figure 45 shows the basic connections required for single-supply operation.

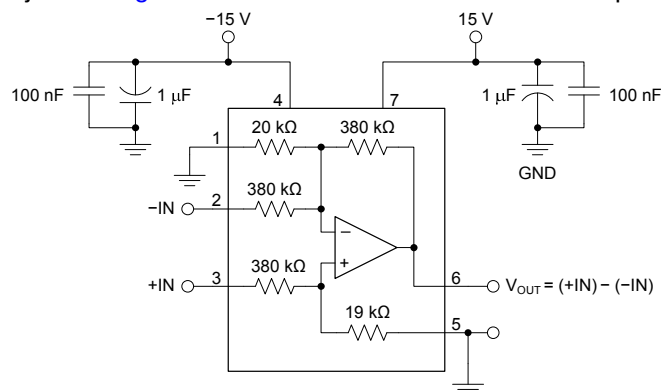


Figure 44. Basic Power and Signal Connections for Dual-Supply Operation

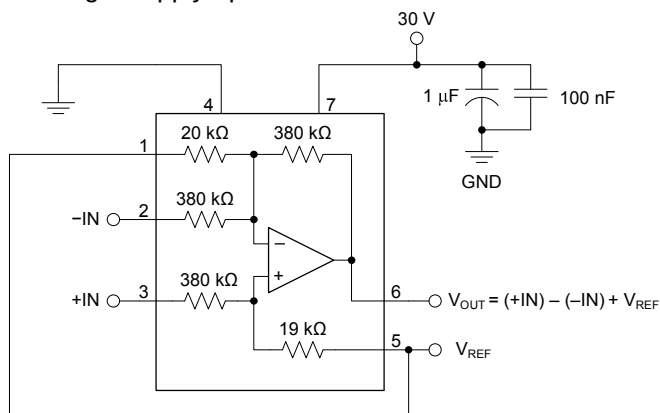


Figure 45. Basic Power and Signal Connections for Single-Supply Operation

TRANSFER FUNCTION

Most applications use the INA149 as a simple unity-gain difference amplifier. The transfer function is given in Equation 1:

$$V_{OUT} = (+IN) - (-IN) \quad (1)$$

Some applications, however, apply voltages to the reference terminals (REF_A and REF_B). The complete transfer function is given in Equation 2:

$$V_{OUT} = (+IN) - (-IN) + 20 \times REF_A - 19 \times REF_B \quad (2)$$

COMMON-MODE RANGE

The high common-mode range of the INA149 is achieved by dividing down the input signal with a high precision resistor divider. This resistor divider brings both the positive input and the negative input within the input range of the internal operational amplifier. This input range depends on the supply voltage of the INA149.

Both Figure 3 and Figure 4 can be used to determine the maximum common-mode range for a specific supply voltage. The maximum common-mode range can also be calculated by ensuring that both the positive and the negative input of the internal amplifier are within 1.5 V of the supply voltage.

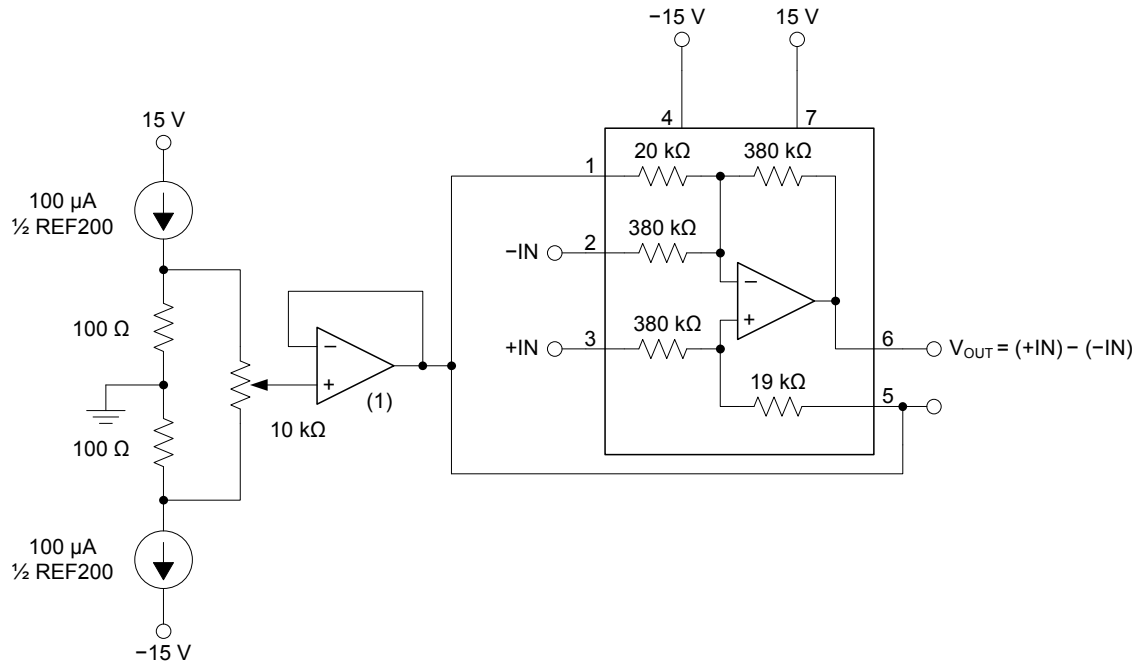
In case the voltage at the inputs of the internal amplifier exceeds the supply voltage, the internal ESD diodes start conducting current. This current must be limited to 10 mA to make sure not to exceed the absolute maximum ratings for the device.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA149 depends on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedance driving the two inputs. A 75-Ω resistance in series with pins 2 or 3 decreases the common-mode rejection ratio (CMRR) from 100 dB (typical) to 74 dB.

Resistance in series with the reference pins also degrades CMR. A 4-Ω resistance in series with pins 1 or 5 decreases CMRR from 100 dB to 74 dB.

Most applications do not require trimming. Figure 46 shows an optional circuit that may be used for trimming offset voltage and common-mode rejection.



(1) The [OPA171](#) (a 36-V, low-power, RRO, general-purpose operational amplifier) can be used for this application.

Figure 46. Offset Voltage Trim Circuit

MEASURING CURRENT

The INA149 can be used to measure a current by sensing the voltage drop across a series resistor, R_S . Figure 47 shows the INA149 used to measure the supply currents of a device under test.

The sense resistor imbalances the input resistor matching of the INA149, thus degrading its CMR. Also, the input impedance of the INA149 loads R_S , causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor (R_C), equal to the value of R_S , as shown in Figure 47. If R_S is less than 5 Ω , degradation in the CMR is negligible and R_C can be omitted. If R_S is larger than approximately 1 k Ω , trimming R_C may be required to achieve greater than 84-dB CMR. This error is caused by the INA149 input impedance mismatch.

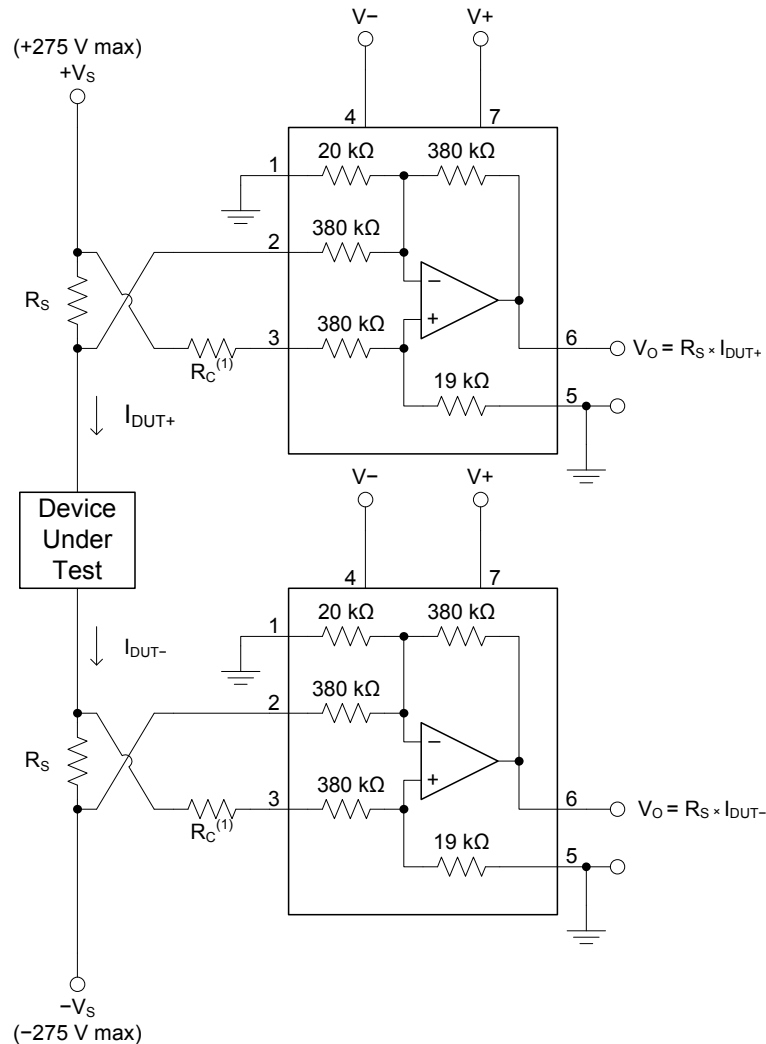


Figure 47. Measuring Supply Currents of a Device Under Test

If R_S is more than approximately 50 Ω , the gain error is greater than the 0.02% specification of the INA149. This gain error can be corrected by slightly increasing the value of R_S . The corrected value (R_S') can be calculated by

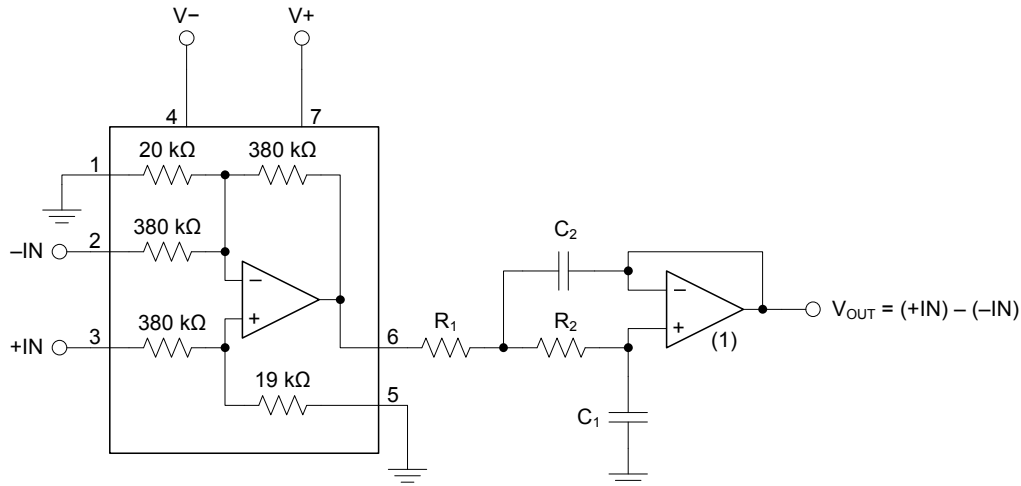
$$R_S' = R_S \times 380 \text{ k}\Omega / (380 \text{ k}\Omega - R_S) \quad (3)$$

NOISE PERFORMANCE

The wideband noise performance of the INA149 is dominated by the internal resistor network. The thermal or *Johnson noise* of these resistors measures approximately 550 nV/√Hz. The internal op amp contributes virtually no excess noise at frequencies above 100 Hz.

Many applications may be satisfied with less than the full 500-kHz bandwidth of the INA149. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in [Figure 48](#) limits bandwidth and reduces noise. Because the INA149 has a 1/f noise corner frequency of approximately 100 Hz, a cutoff frequency below 100 Hz does not further reduce noise.

Component values for different filter frequencies are shown in [Table 1](#).



(1) For most applications, the [OPA171](#) can be used as an operational amplifier. For directly driving successive-approximation register (SAR) data converters, the [OPA140](#) is a good choice.

Figure 48. Output Filter for Noise Reduction

Table 1. Components Values for Different Filter Bandwidths

BUTTERWORTH LOW-PASS (f _{-3 dB})	OUTPUT NOISE (mV _{PP})	R ₁	R ₂	C ₁	C ₂
200 kHz	1.8	No filter			
100 kHz	1.1	11 kΩ	11.3 kΩ	100 pF	200 pF
10 kHz	0.35	11 kΩ	11.3 kΩ	1 nF	2 nF
1 kHz	0.11	11 kΩ	11.3 kΩ	10 nF	20 nF
100 Hz	0.05	11 kΩ	11.3 kΩ	0.1 μF	0.2 μF

BATTERY CELL VOLTAGE MONITOR

The INA149 can be used to measure the voltages of single cells in a stacked battery pack. Figure 49 shows an examples for such an application.

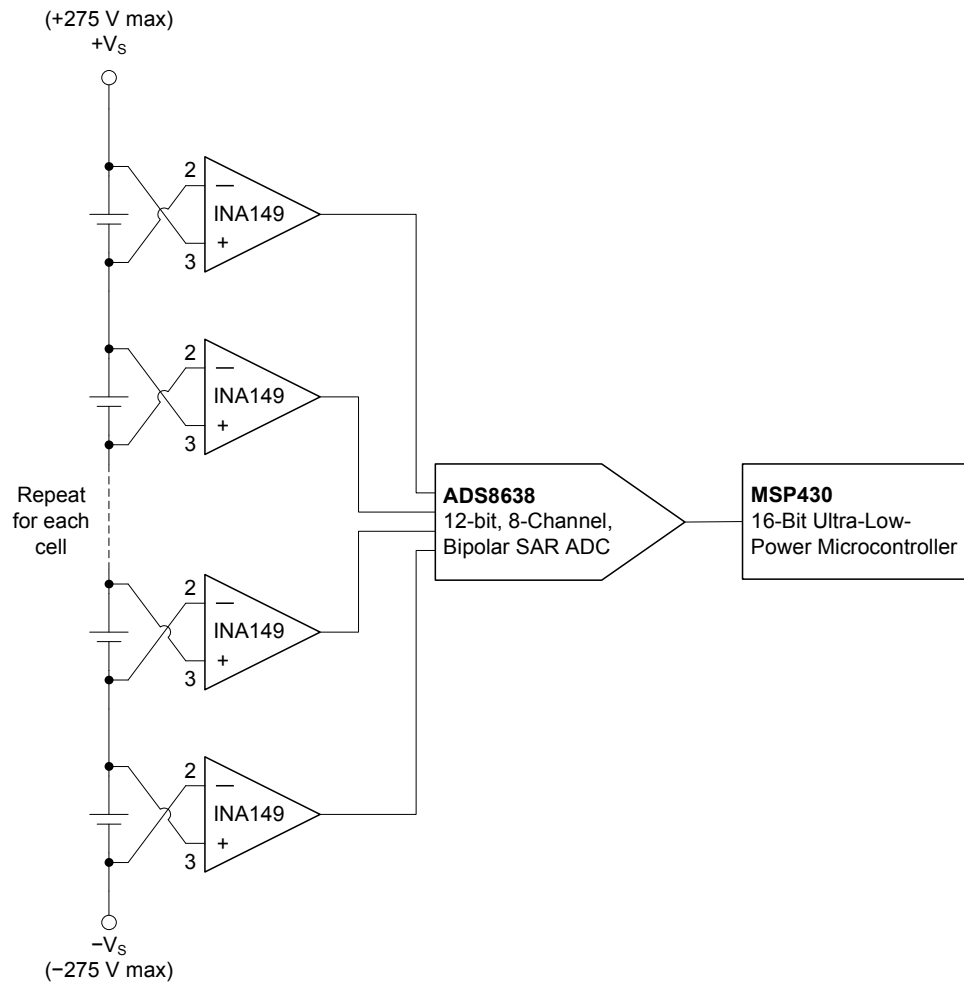


Figure 49. Battery Cell Voltage Monitor

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
INA149AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	INA 149AM	Samples
V62/12614-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	INA 149AM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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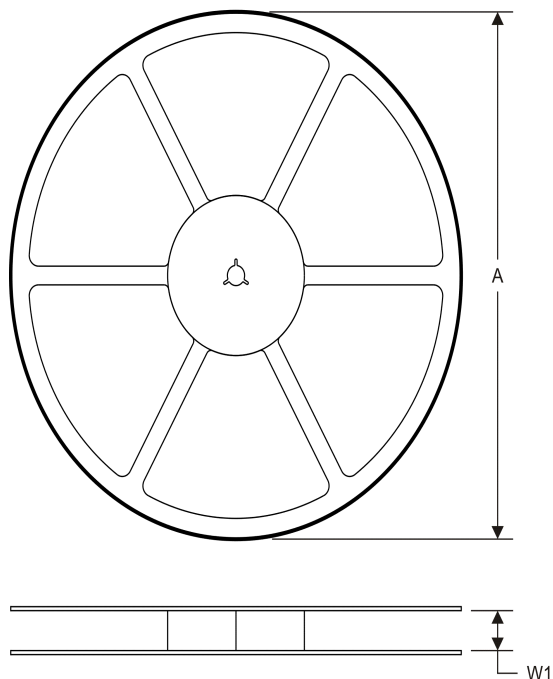
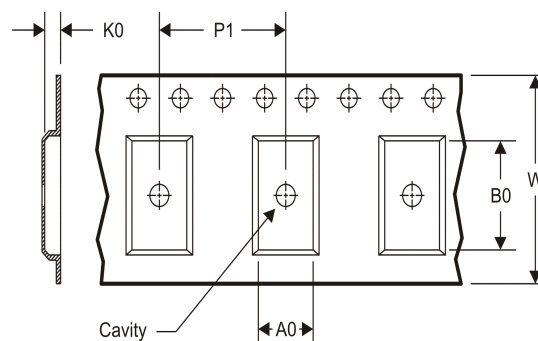
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA149-EP :

-
- Catalog: [INA149](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


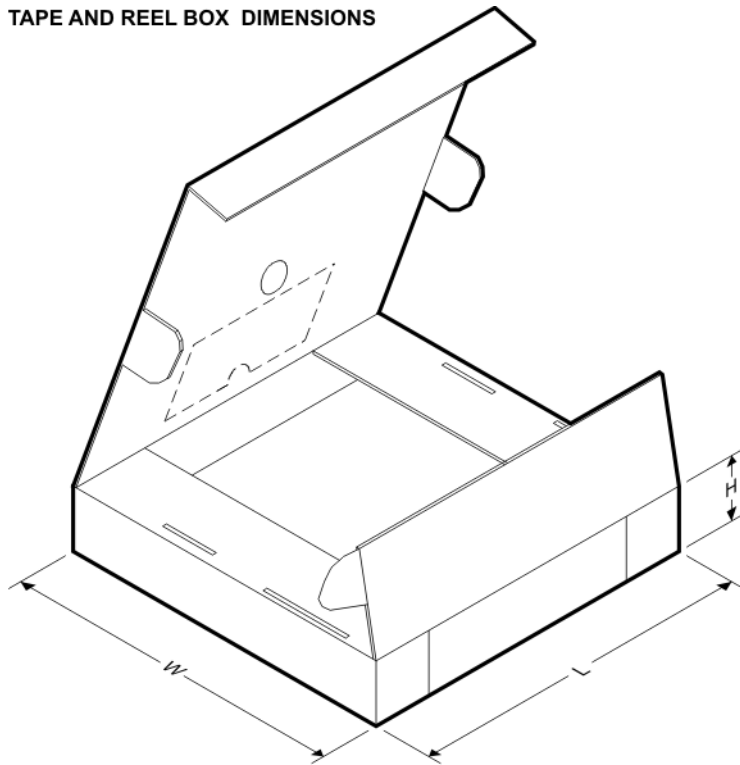
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

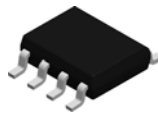
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA149AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA149AMDREP	SOIC	D	8	2500	367.0	367.0	35.0

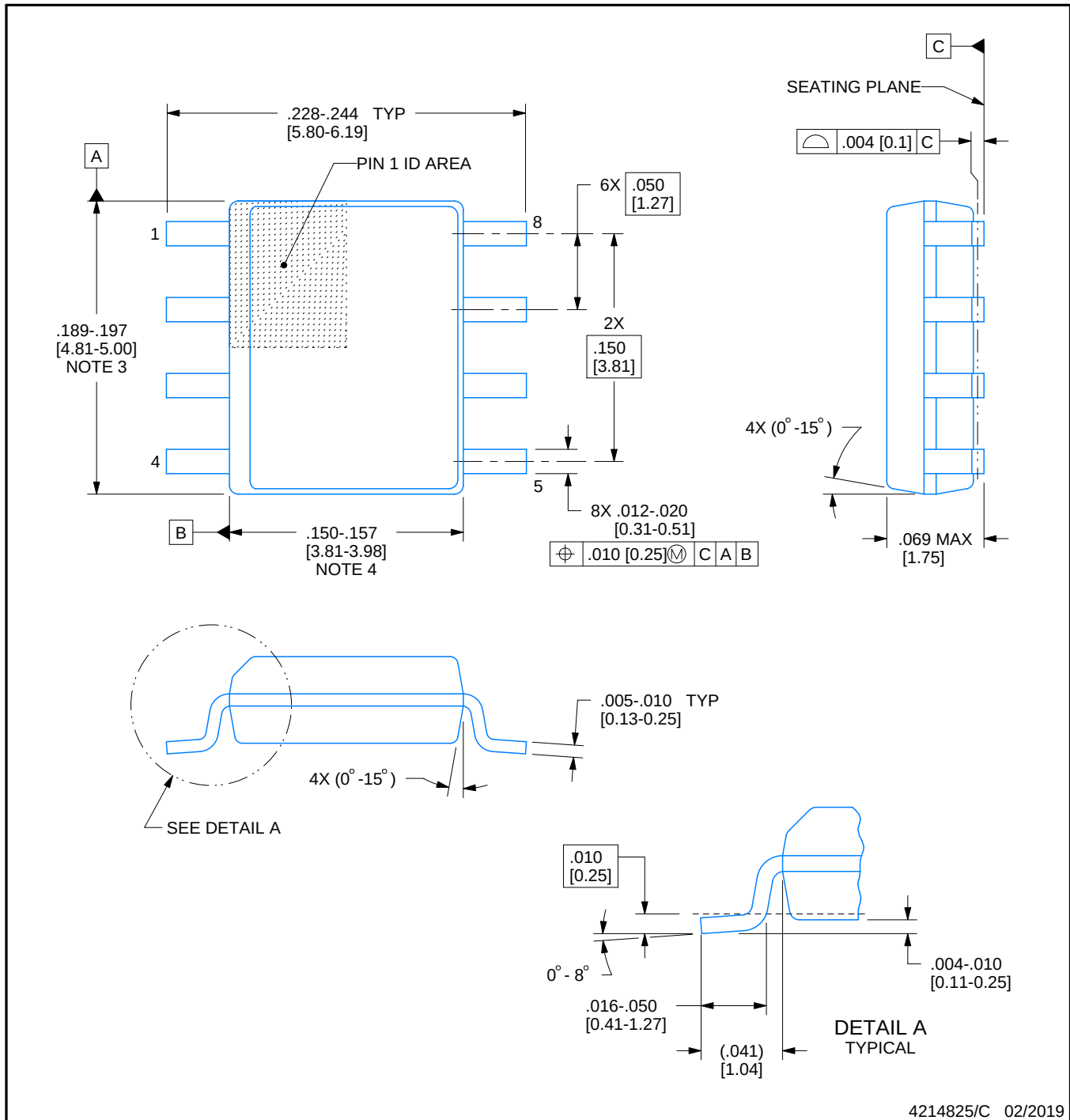


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

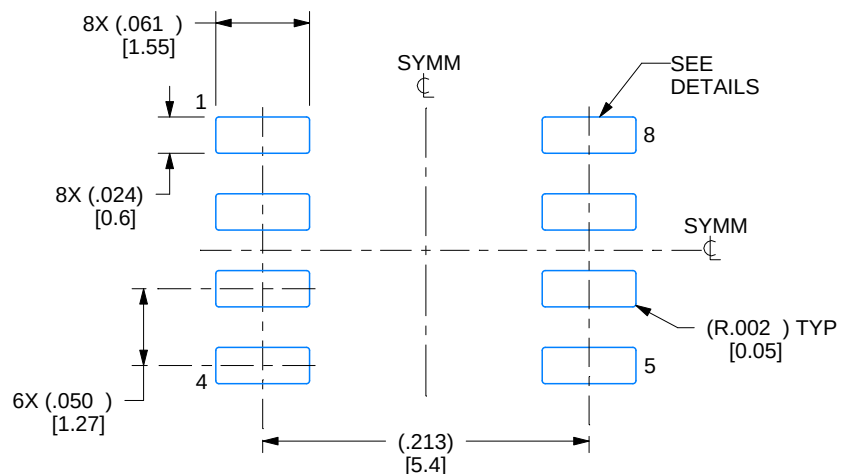
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

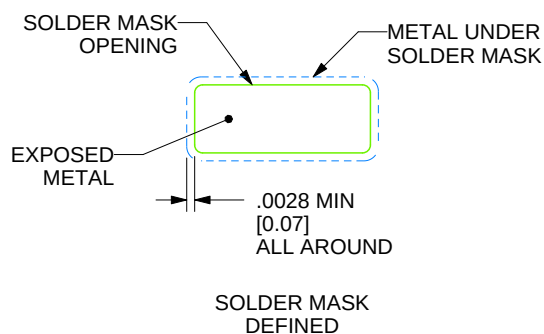
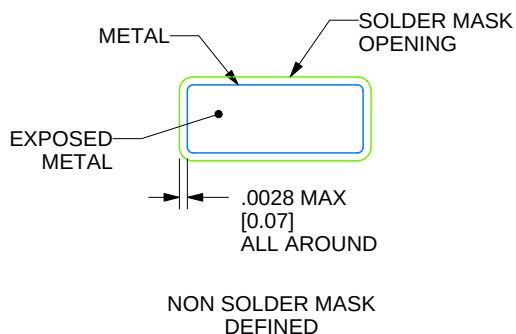
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

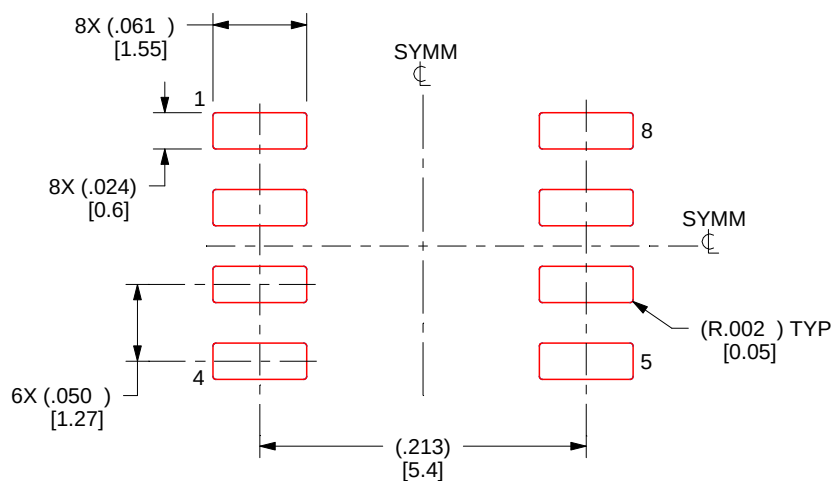
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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