

INA1650-Q1 SoundPlus™ 高共模抑制线路接收器

1 特性

- 符合汽车应用 要求
- 符合 AEC-Q100 标准，其中包括以下内容：
 - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
 - 器件 HBM ESD 分类等级：2
 - 器件 CDM ESD 分类等级：C5
- 高共模抑制：91dB（典型值）
- 高输入阻抗：1MΩ（差分）
- 超低噪声：-104.7dBu，未加权
- 超低总谐波失真 + 噪声：-120dB THD+N（22dBu，22kHz 带宽）
- 短路保护
- 集成电磁干扰 (EMI) 滤波器
- 宽电源电压范围：±2.25V 至 ±18V
- 采用小型 14 引脚 TSSOP 封装

2 应用

- 车厢麦克风前置放大器
- 信息娱乐系统
- 音频输入电路
- 线路驱动器
- 外部音频功率放大器

3 说明

INA1650-Q1 SoundPlus™ 音频线路接收器可实现 91dB 的极高共模抑制比 (CMRR)，同时对于 22dBu 信号电平，可在 1kHz 下保持 -120dB 的超低 THD+N。与其他线路接收器产品不同，INA1650-Q1 CMRR 确定了温度特性并且经生产测试，可在各种应用中提供始终如一的性能。

INA1650-Q1 支持 ±2.25V 到 ±18V 的宽电源电压范围（电源电流为 10.5mA）。除两个线路接收器通道之外，INA1650-Q1 还包含一个缓冲中位电压基准输出，允许将其配置为用于双电源或单电源应用。中间电源输出可用作信号链中其他模拟电路的偏置电压。

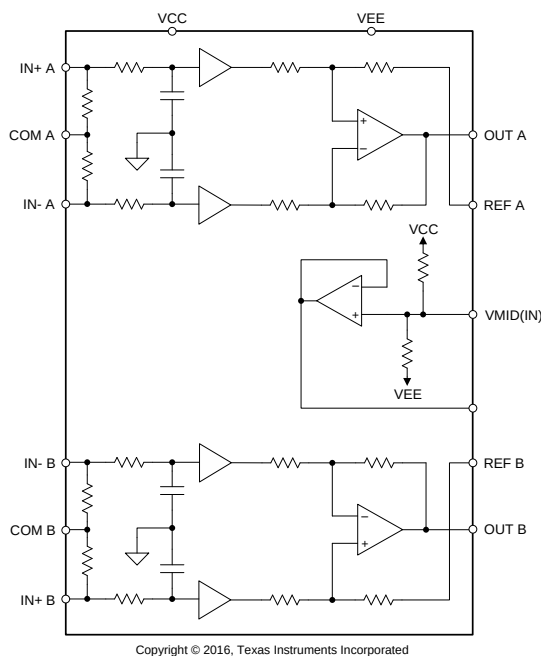
INA1650-Q1 特点 独特的内部布局，即使在过驱或过载条件下也可在通道间实现最低串扰和零交互。此器件的额定温度介于 -40°C 至 +125°C 之间。

器件信息⁽¹⁾

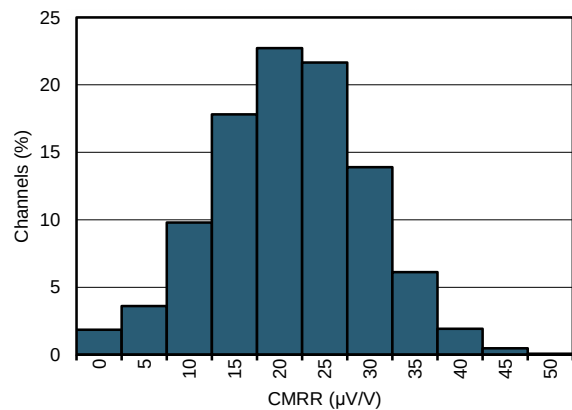
器件型号	封装	封装尺寸（标称值）
INA1650-Q1	薄型小外形尺寸封装 (TSSOP) (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

INA1650-Q1 简化内部原理图



CMRR 直方图（5746 通道）



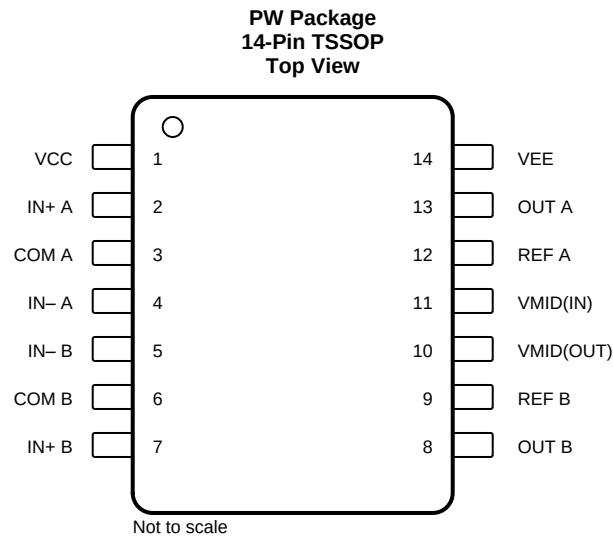
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4 修订历史记录

日期	修订版本	说明
2017 年 8 月	*	初始发行版

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM A	3	I	Input common, channel A
COM B	6	I	Input common, channel B
IN+ A	2	I	Noninverting input, channel A
IN– A	4	I	Inverting input, channel A
IN+ B	7	I	Noninverting input, channel B
IN– B	5	I	Inverting input, channel B
OUT A	13	O	Output, channel A
OUT B	8	O	Output, channel B
REF A	12	I	Reference input, channel A. This pin must be driven from a low impedance.
REF B	9	I	Reference input, channel B. This pin must be driven from a low impedance.
VCC	1	—	Positive (highest) power supply
VEE	14	—	Negative (lowest) power supply
VMID(IN)	11	I	Input node of internal supply divider. Connect a capacitor to this pin to reduce noise from the supply divider circuit.
VMID(OUT)	10	O	Buffered output of internal supply divider.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V+) - (V-)$		40	V
	Input voltage (Signal inputs, enable, ground)	$(V-) - 0.5$	$(V+) + 0.5$	
	Input differential voltage		$(V+) - (V-)$	
Current	Input current (all pins except power-supply pins)		± 10	mA
	Output short-circuit ⁽²⁾		Continuous	
Temperature	Operating, T_A	-55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to $V_S / 2$ (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	± 4000	V
	Charged-device model (CDM), per AEC Q100-011	± 1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage ($V+ - V-$)	4.5 (± 2.25)		36 (± 18)	V
Specified temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA1650-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics:

at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	$V_O = 3\text{ V}_{\text{RMS}}$, $f = 1\text{ kHz}$, 90-kHz measurement bandwidth, $V_S = \pm 18\text{ V}$	0.00039%			
			−108.1		dB	
		$V_{\text{IN}} = 22\text{ dBu}$ (9.7516 V_{RMS}) , $F_{\text{IN}} = 1\text{ kHz}$, $V_S = \pm 18\text{ V}$, 90-kHz measurement bandwidth	0.000174%			
			−115.2		dB	
IMD	Intermodulation distortion	SMPTE and DIN two-tone, 4:1 (60 Hz and 7 kHz) $V_O = 3\text{ V}_{\text{RMS}}$, 90-kHz measurement bandwidth	0.0005%			
			−106.1		dB	
		CCIF twin-tone (19 kHz and 20 kHz), $V_O = 3\text{ V}_{\text{RMS}}$, 90-kHz measurement bandwidth	0.00066%			
			−103.6		dB	
AC PERFORMANCE						
BW	Small-signal bandwidth		2.7			MHz
SR	Slew rate		10			V/ μs
	Full-power bandwidth ⁽¹⁾	$V_O = 1\text{ V}_P$	1.59			MHz
PM	Phase margin	$C_L = 20\text{ pF}$	71°			
		$C_L = 200\text{ pF}$	54°			
t_s	Settling time	To 0.01%, $V_S = \pm 18\text{ V}$, 10-V step	2.2			μs
	Overload recovery time		330			ns
	Channel separation	$f = 1\text{ kHz}$, REF and COM pins connected to ground	140			dB
		$f = 1\text{ kHz}$, REF and COM pins connected to VMID(OUT)	130			dB
	EMI/RFI filter corner frequency		80			MHz
NOISE						
e_n	Output voltage noise density ⁽²⁾	$f = 20\text{ Hz}$ to 20 kHz , no weighting	4.5			μV_{RMS}
			−104.7		dBu	
		$f = 100\text{ Hz}$	47			$\text{nV}/\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$	31		
OFFSET VOLTAGE						
V_{OS}	Output offset voltage		± 1	± 3		mV
		$T_A = -40^\circ\text{C}$ to 125°C ⁽²⁾		± 4		
dV_{OS}/dT	Output offset voltage drift ⁽²⁾	$T_A = -40^\circ\text{C}$ to 125°C	2	7		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio		2			$\mu\text{V}/\text{V}$
GAIN						
	Gain		1			V/V
	Gain error		0.04%	0.05%		
		$T_A = -40^\circ\text{C}$ to 125°C ⁽²⁾	0.05%	0.06%		
	Gain nonlinearity	$V_S = \pm 18\text{ V}$, $-10\text{ V} < V_O < 10\text{ V}$ ⁽²⁾	1		5	ppm
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V−) + 0.25	(V+) − 2		V
CMRR	Common-mode rejection ratio	(V−) + 0.25 V ≤ V_{CM} ≤ (V+) − 2 V, REF and COM pins connected to ground, $V_S = \pm 18\text{ V}$	85	91		dB
		$T_A = -40^\circ\text{C}$ to 125°C ⁽²⁾	82	89		
		(V−) + 0.25 V ≤ V_{CM} ≤ (V+) − 2 V, REF and COM pins connected to VMID(OUT), $V_S = \pm 18\text{ V}$	82	86		
		$T_A = -40^\circ\text{C}$ to 125°C ⁽²⁾	76	84		
CMRR	Common-mode rejection ratio	(V−) + 0.25 V ≤ V_{CM} ≤ (V+) − 2 V, REF and COM pins connected to ground, $V_S = \pm 18\text{ V}$, R_S mismatch = 20 Ω	84			dB

(1) Full-power bandwidth = $SR / (2\pi \times V_P)$, where SR = slew rate.

(2) Specified by design and characterization.

INA1650-Q1

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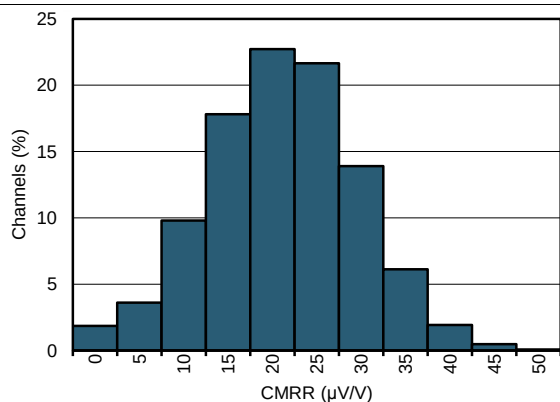
www.ti.com.cn
Electrical Characteristics: (continued)

 at $T_A = 25^\circ\text{C}$, $V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
Differential				850	1000	1150	kΩ
Common-mode				212.5	250	287.5	kΩ
Input resistance mismatch					0.01%	0.25%	
SUPPLY DIVIDER CIRCUIT							
Nominal output voltage				$\frac{[(V+) + (V-)]}{2}$			V
Output voltage offset		VMID(IN) = ((V+) + (V-) / 2		2	4		mV
Input impedance		VMID(IN) pin, f = 1 kHz		250			kΩ
Output resistance		VMID(OUT) pin		0.35			Ω
Output voltage noise		20 Hz to 20 kHz, C _{MID} = 1 μF		1.56			μV _{RMS}
Output capacitive load limit		Phase Margin > 45°, R _{ISO} = 0 Ω		150			pF
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	R _L = 2 kΩ	350			mV
			R _L = 600 Ω	1100			
	Negative rail	R _L = 2 kΩ	430				
		R _L = 600 Ω	1300				
Z _{OUT}	Output impedance	f ≤ 100 kHz, I _{OUT} = 0 A			< 1		Ω
I _{SC}	Short-circuit current	V _S = ±18 V			±75		mA
C _{LOAD}	Capacitive load drive				See Figure 19		pF
POWER SUPPLY							
I _Q	Quiescent current	I _{OUT} = 0 A		8	10.5	12	mA
			T _A = −40°C to 125°C ⁽²⁾			14	

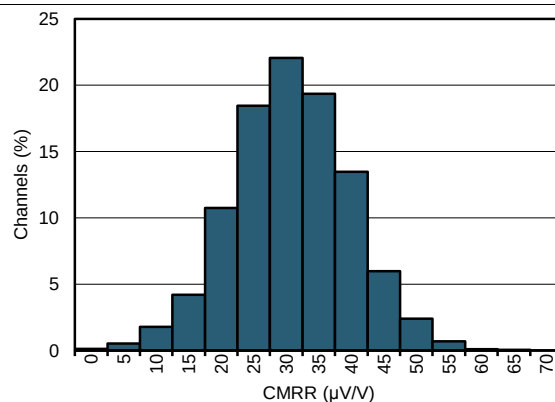
6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)



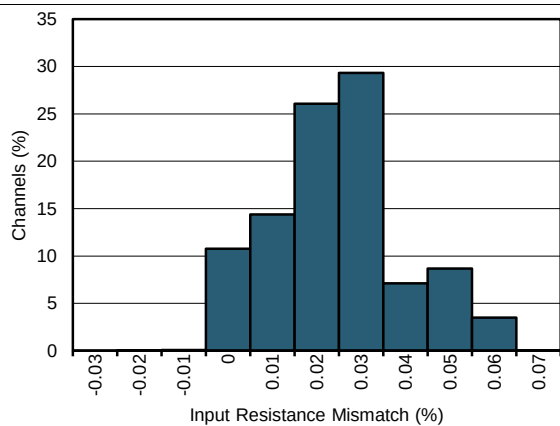
5746 Channels
 V_{REF} Pins Connected to Ground

图 1. Common-Mode Rejection Ratio Distribution



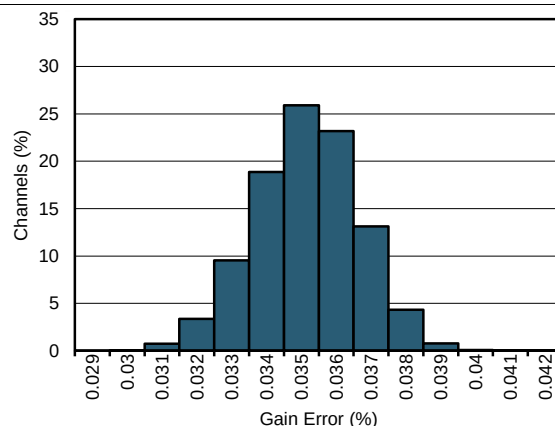
5746 Channels
 V_{REF} Pins Connected to $V_{MID(OUT)}$

图 2. Common-Mode Rejection Ratio Distribution



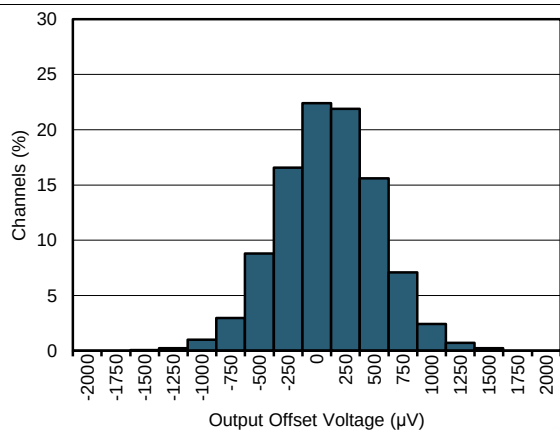
5746 Channels

图 3. Distribution of Mismatch in 500-k Ω Input Resistors



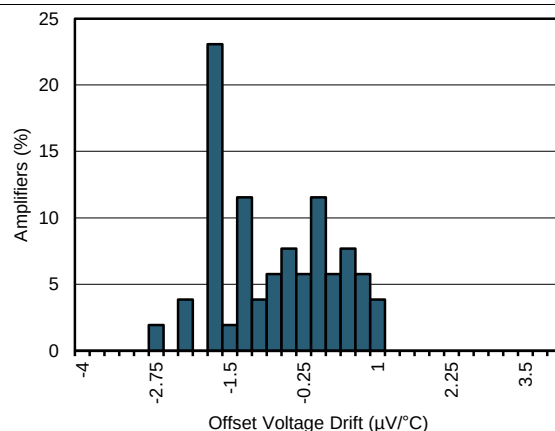
5746 Channels

图 4. Gain Error Distribution



5746 Channels

图 5. Offset Voltage Distribution



52 Channels

图 6. Offset Voltage Drift Distribution

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

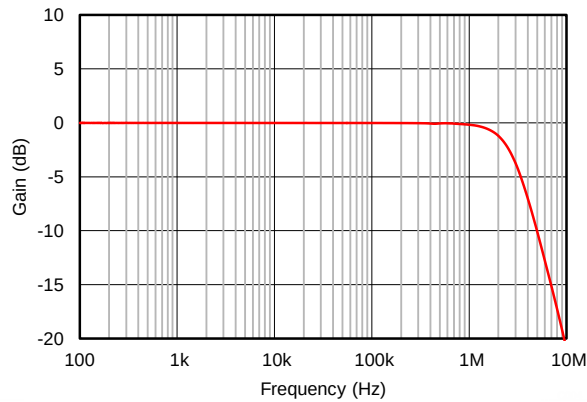


图 7. Frequency Response

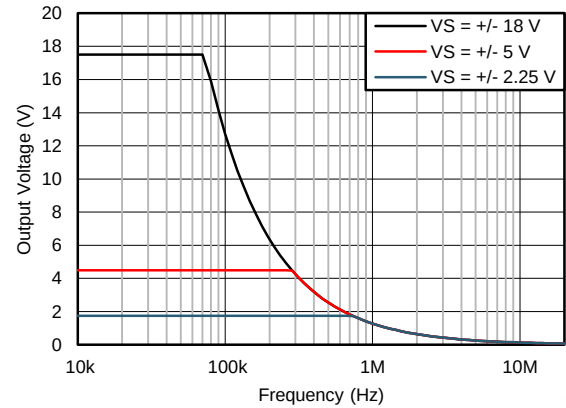


图 8. Maximum Output Voltage vs Frequency

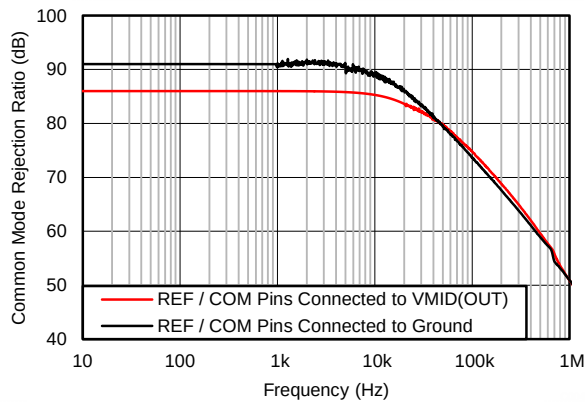


图 9. Common-Mode Rejection Ratio vs Frequency

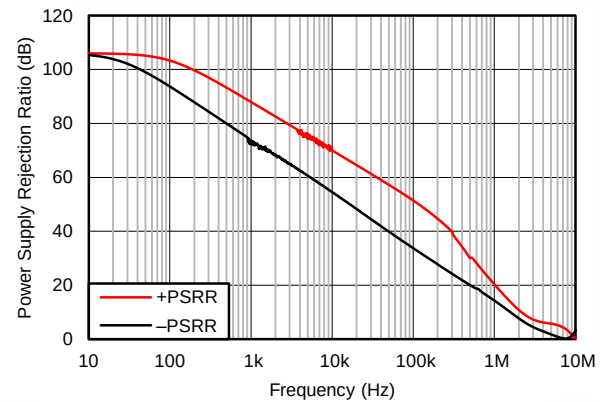


图 10. Power Supply Rejection Ratio vs Frequency

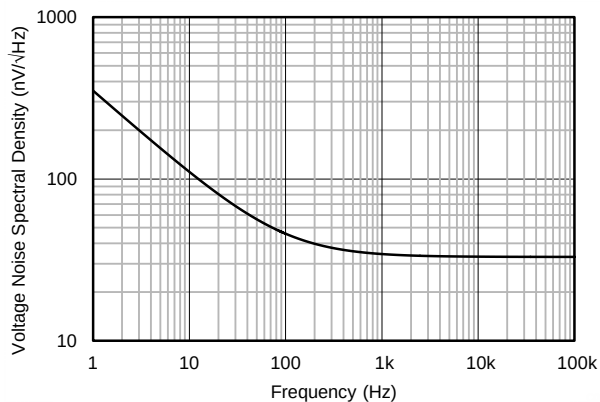


图 11. Voltage Noise Spectral Density

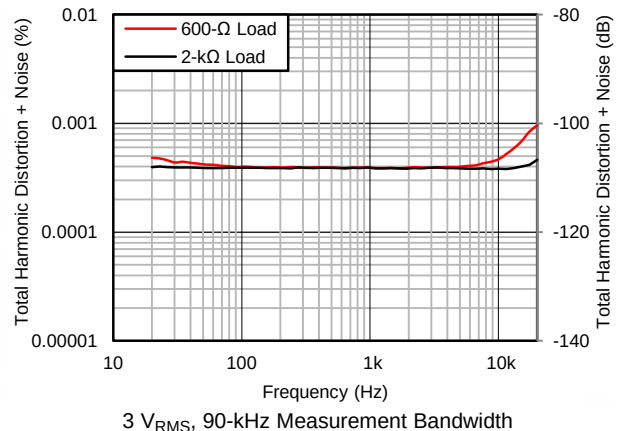


图 12. THD+N vs Frequency

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

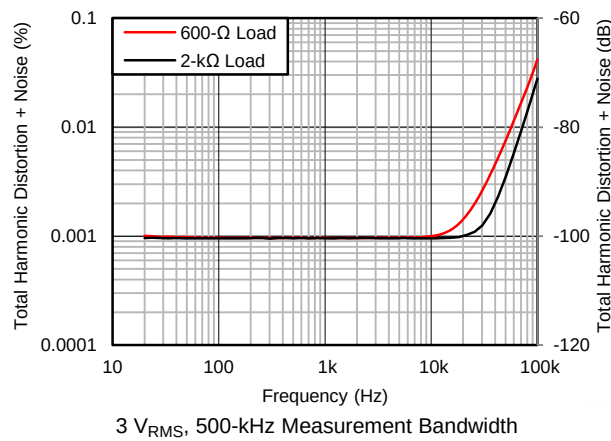


图 13. THD+N vs Frequency

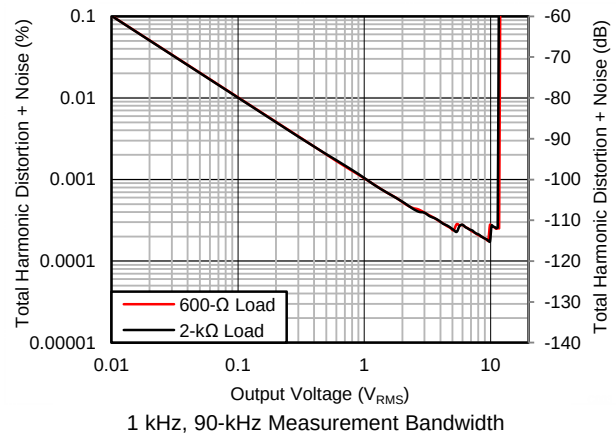


图 14. THD+N vs Output Amplitude

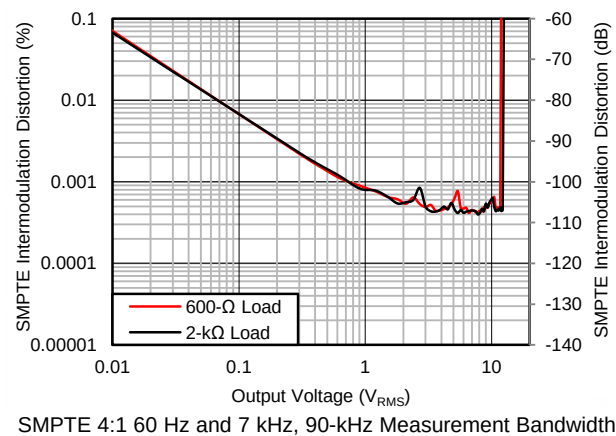


图 15. SMPTE Intermodulation Distortion vs Output Amplitude

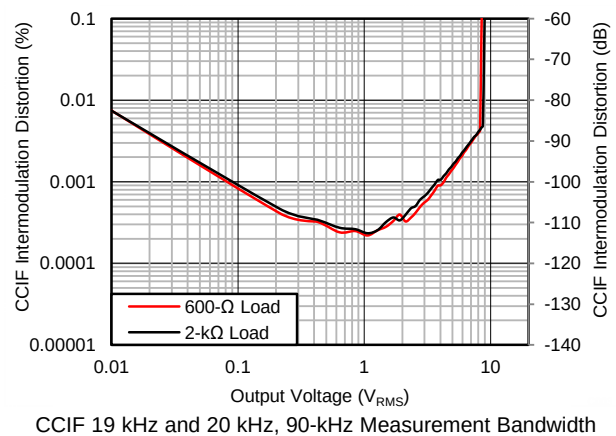


图 16. CCIF Intermodulation Distortion vs Output Amplitude

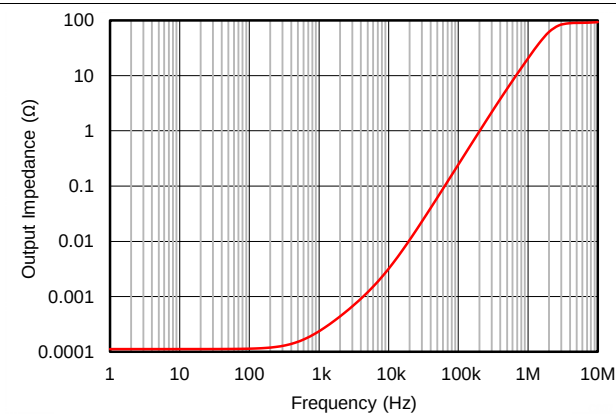


图 17. Signal Path Output Impedance vs Frequency

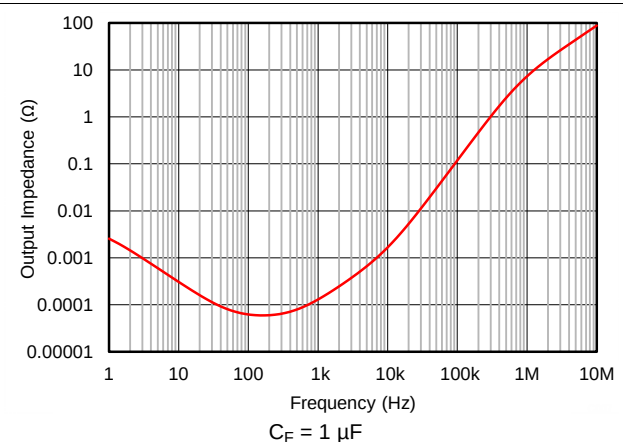


图 18. Supply Divider Output Impedance vs Frequency

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

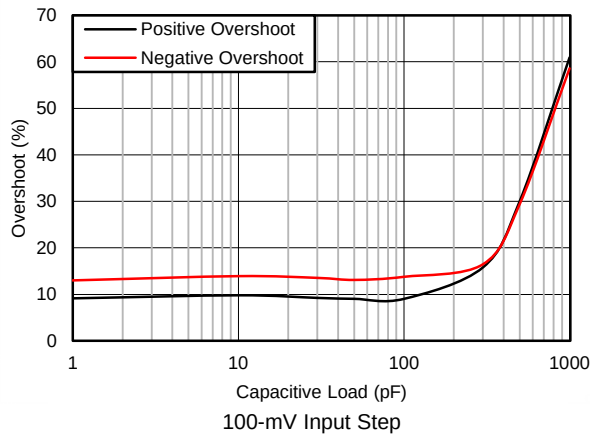


图 19. Overshoot vs Capacitive Load

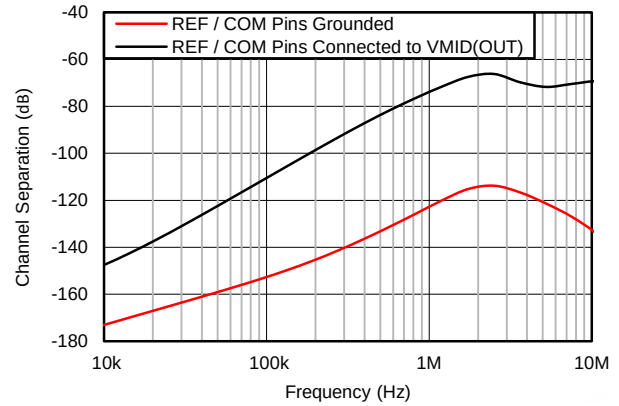
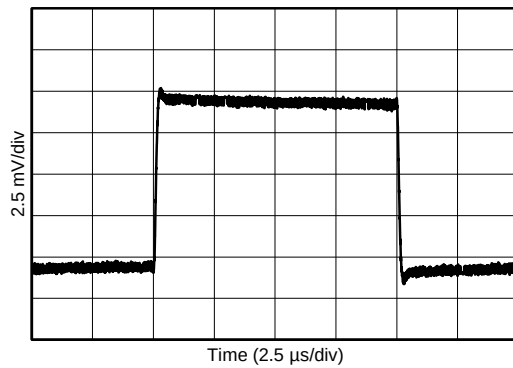
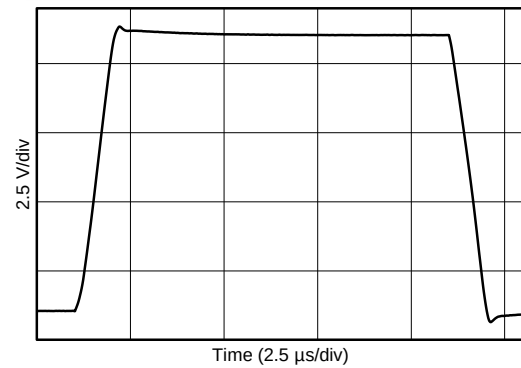


图 20. Channel Separation vs Frequency



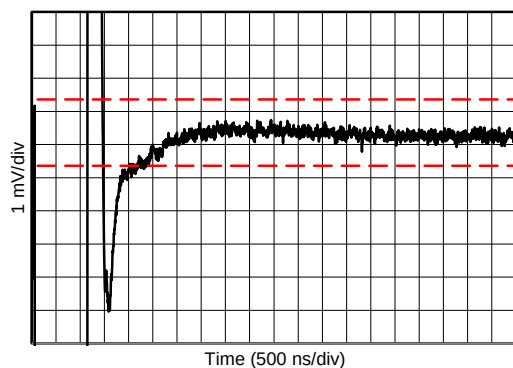
10-mV Input Step

图 21. Small-Signal Step Response



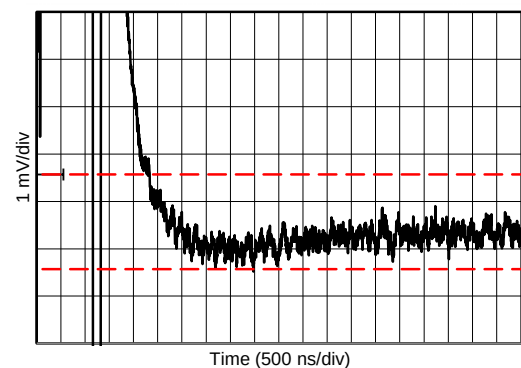
10-V Input Step

图 22. Large-Signal Step Response



10-V Input Step, 0.01% Settling = $\pm 1\text{ mV}$

图 23. Rising-Edge Settling Time



10-V Input Step, 0.01% Settling = $\pm 1\text{ mV}$

图 24. Falling-Edge Settling Time

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

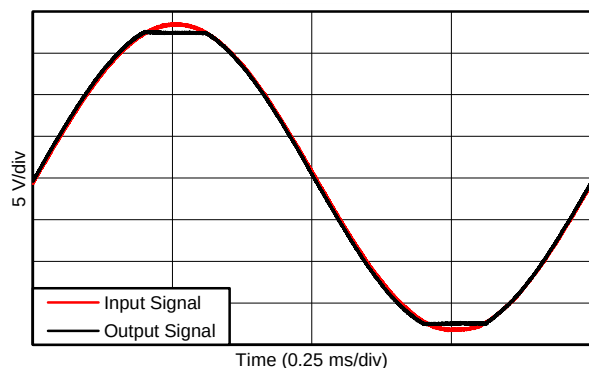


图 25. No Phase Reversal

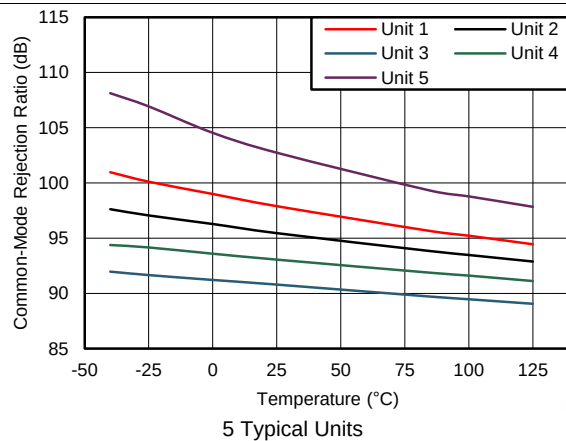


图 26. CMRR vs Temperature

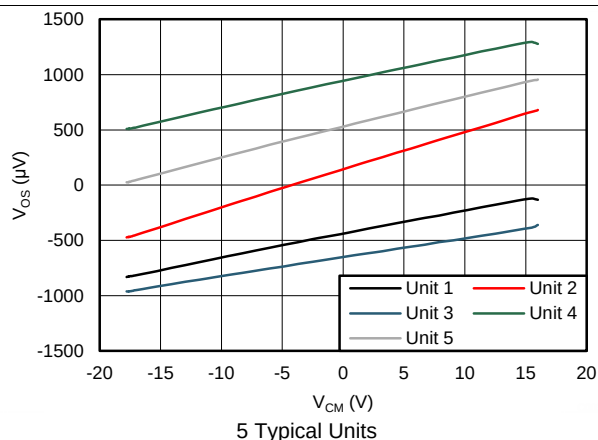


图 27. Output Offset Voltage vs Common-Mode Voltage

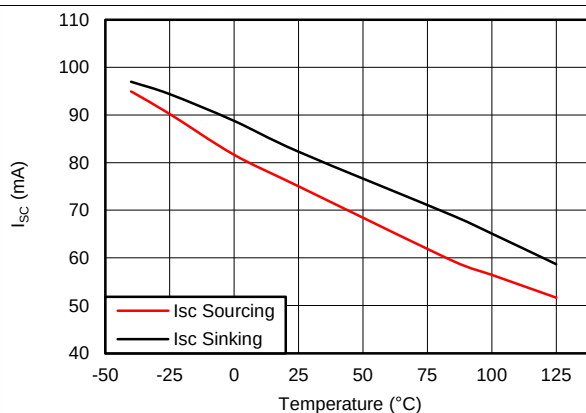


图 28. Short-Circuit Current vs Temperature

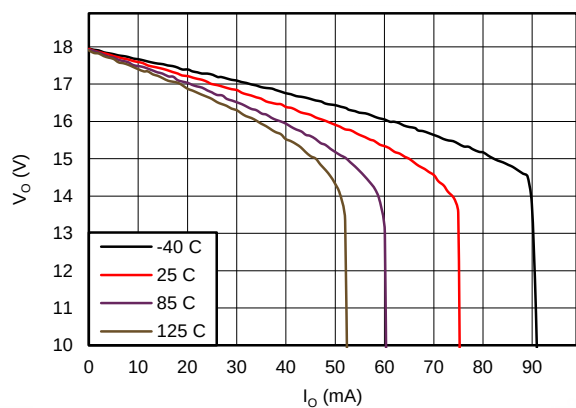


图 29. Positive Output Voltage vs Output Current

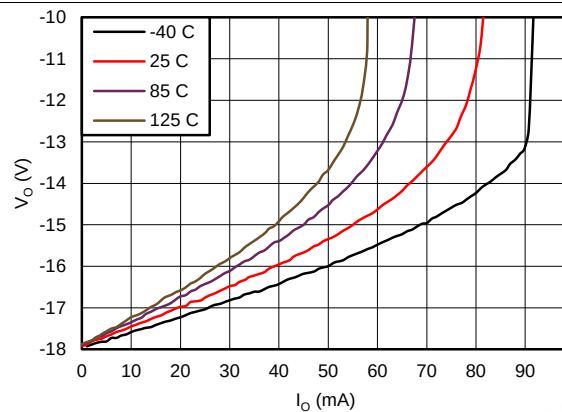


图 30. Negative Output Voltage vs Output Current

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

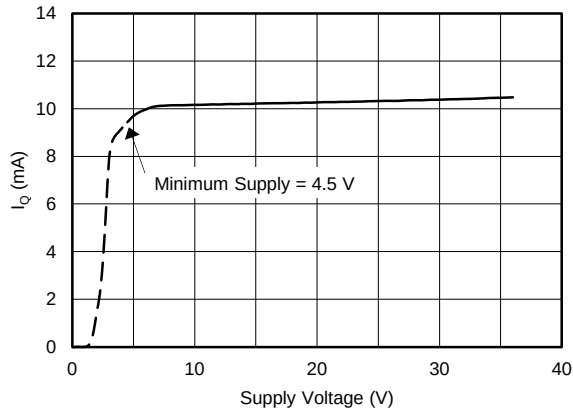


图 31. Power Supply Current vs Power Supply Voltage

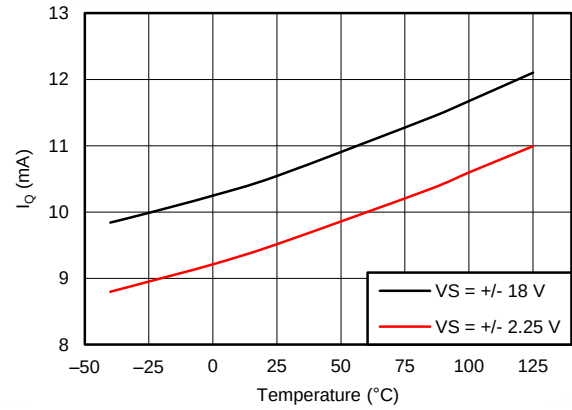


图 32. Power Supply Current vs Temperature

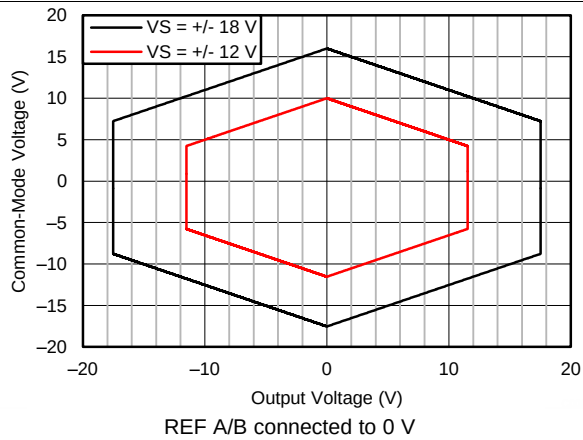


图 33. Input Common-Mode Voltage vs Output Voltage

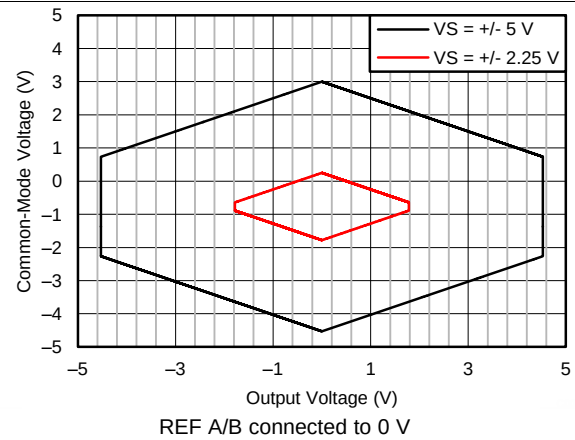


图 34. Input Common-Mode Voltage vs Output Voltage

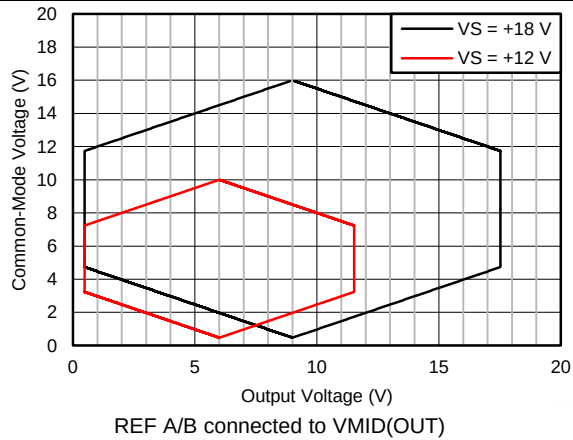


图 35. Input Common-Mode Voltage vs Output Voltage

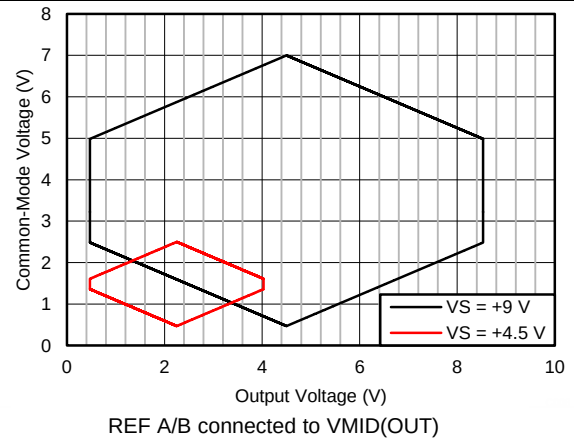


图 36. Input Common-Mode Voltage vs Output Voltage

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 2\text{ k}\Omega$ (unless otherwise noted)

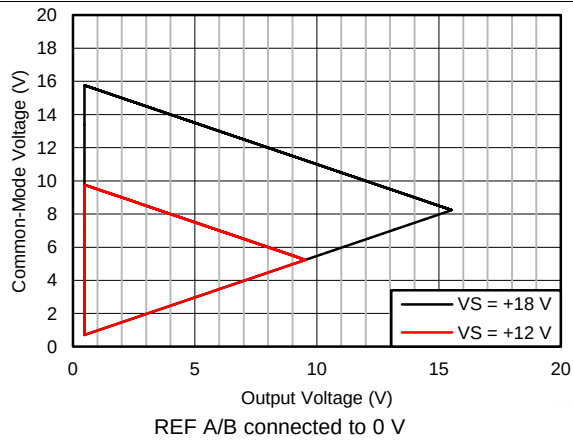


图 37. Input Common-Mode Voltage vs Output Voltage

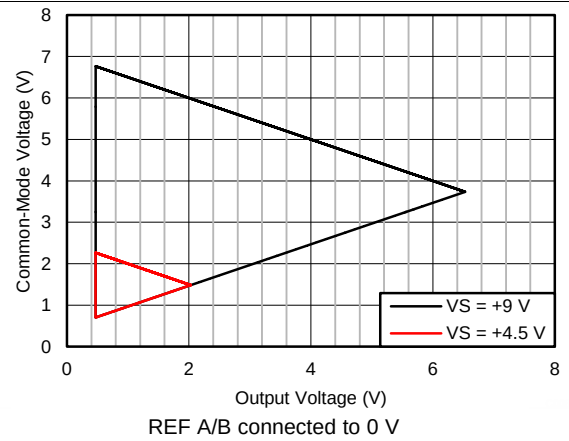


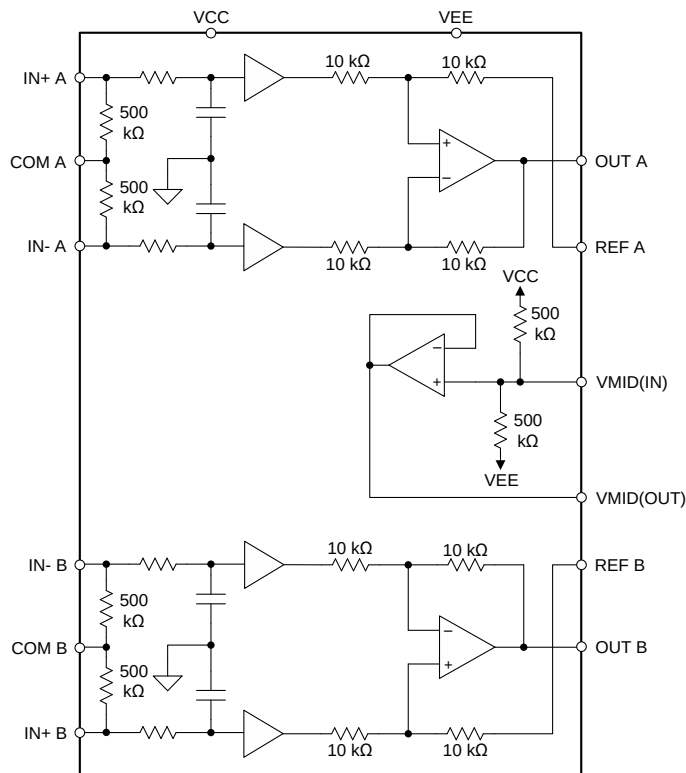
图 38. Input Common-Mode Voltage vs Output Voltage

7 Detailed Description

7.1 Overview

The INA1650-Q1 combines high-performance audio operational amplifier cores with high-precision resistor networks to provide exceptional audio performance and rejection of noise, which may be externally coupled into the audio signal path. The two channels of the INA1650-Q1 use an instrumentation amplifier topology with a fixed unity gain to provide high input impedance and a high common-mode rejection ratio (CMRR). Unlike other line receiver products that use a simple four-resistor difference amplifier topology, the INA1650-Q1 topology provides excellent CMRR even with mismatched source impedances.

7.2 Functional Block Diagram



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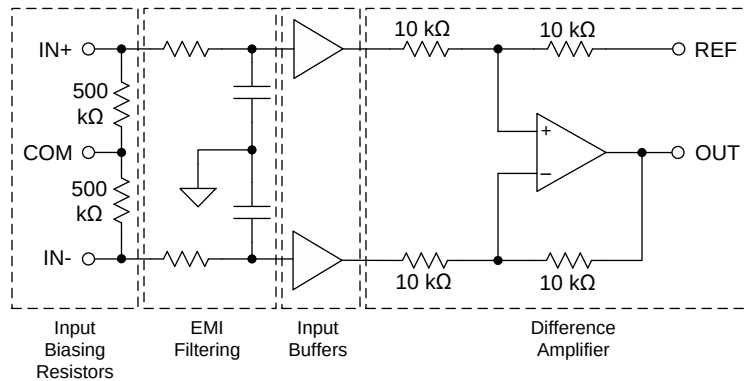
7.3 Feature Description

7.3.1 Audio Signal Path

There are two audio signal pathways present in the INA1650-Q1. [图 39](#) highlights the basic elements present in each audio signal pathway. The primary elements are: input biasing resistors, electromagnetic interference (EMI) filtering, input buffers, and a difference amplifier. The primary role of an audio line receiver is to convert a differential input signal into a single-ended output signal while rejecting noise that is common to both inputs (common-mode noise). The difference amplifier (which consists of an op amp and four matched 10-kΩ resistors) accomplishes this task. The basic transfer function of the circuit is shown in [公式 1](#):

$$V_{OUT} = (V_{IN+} - V_{IN-}) + V_{REF} \quad (1)$$

Feature Description (接下页)



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图 39. INA1650-Q1 Audio Signal Path (Single Channel Shown)

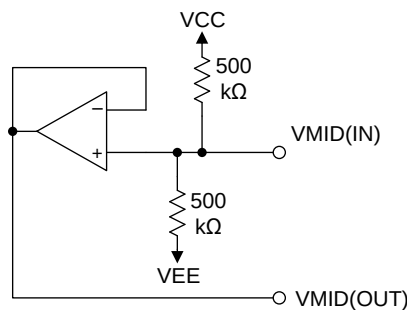
The input buffers prevent external resistances (such as those from the PCB, connectors, or cables) from ruining the precise matching of the internal 10-kΩ resistors that would degrade the high common-mode rejection of the difference amplifier. As is typical of many amplifiers, a small bias current flows into or out of the buffer amplifier inputs. This current must flow to a common potential for the buffer to function properly. The input biasing resistors provide an internal pathway for this current to the COM pin. The COM pin can connect to ground in a dual-supply system or the output of the internal supply divider (VMID(OUT)) in single-supply applications. Finally, EMI filtering is added to the input buffers to prevent high-frequency interference signals from propagating through the audio signal pathway.

7.3.2 Supply Divider

The INA1650-Q1 integrates a supply-divider circuit which may bias the input common-mode voltage and output reference voltage to the halfway point between the applied power supply voltages. The nominal output voltage of the supply divider circuit is shown in 公式 2:

$$V_{\text{MID(OUT)}} = \frac{V_{\text{CC}} + V_{\text{EE}}}{2} \quad (2)$$

图 40 illustrates the internal topology of the supply-divider circuit. The supply divider consists of two 500-kΩ resistors connected between the VCC and VEE pins of the INA1650-Q1. The noninverting input of a buffer amplifier is connected to the midpoint of the voltage divider that is formed by the 500-kΩ resistors. The buffer amplifier provides a low-impedance output that is required to bias the REF pins without degrading the CMRR. For dual-supply applications where the supply divider circuit may not be used, no connection is required for the VMID(IN) or VMID(OUT) pins.



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图 40. Internal Supply Divider Circuit

Feature Description (接下页)

7.3.3 EMI Rejection

The INA1650-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources (such as wireless communications) and densely-populated boards with a mix of analog signal-chain and digital components. The INA1650-Q1 is specifically designed to minimize susceptibility to EMI by incorporating an internal low-pass filter. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing. Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA1650-Q1 to reject EMI. 图 41 and 图 42 show the INA1650-Q1 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. 表 1 shows the EMIRR values for the INA1650-Q1 at frequencies commonly encountered in real-world applications. Applications listed in 表 1 can be centered on or operated near the particular frequency shown.

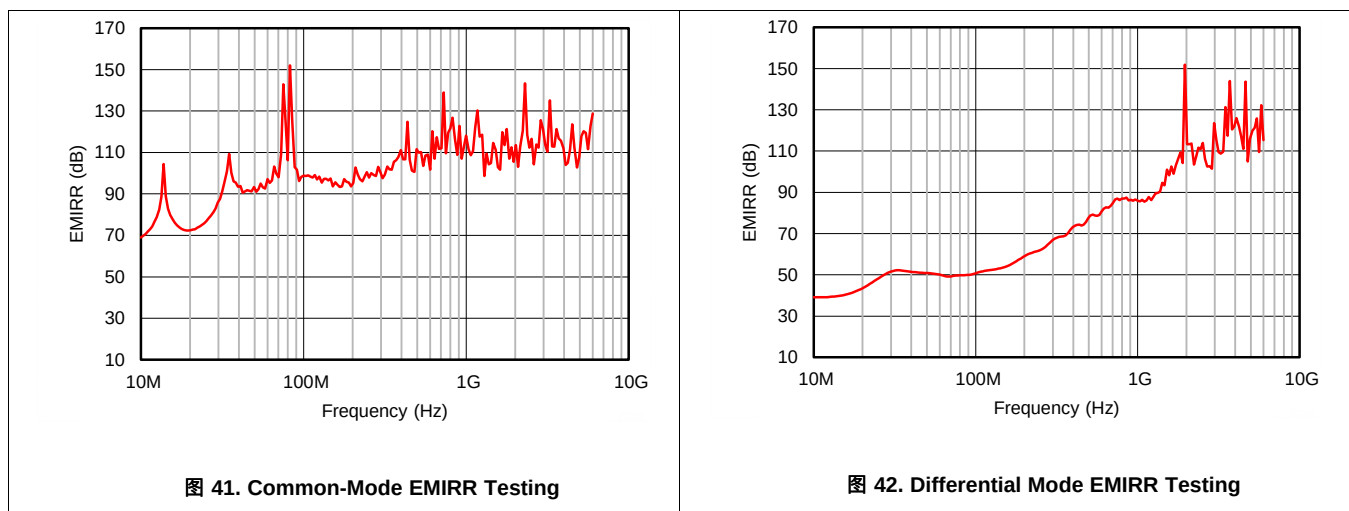


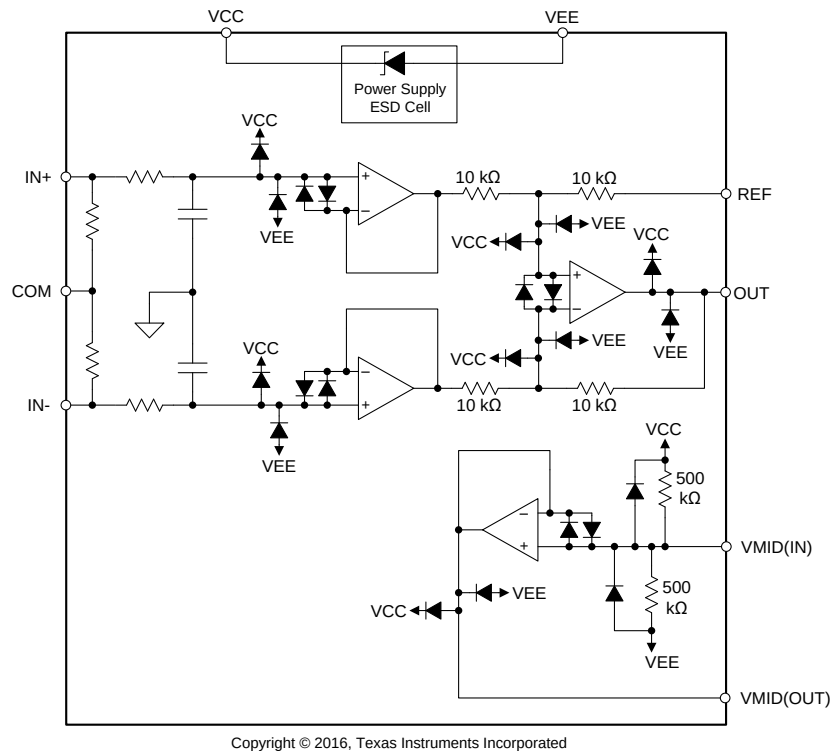
表 1. INA1650-Q1 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	73 dB	111 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	86 dB	123 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	106 dB	121 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	112 dB	119 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	117 dB	121 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	116 dB	108 dB

7.3.4 Electrical Overstress

Designers typically ask questions about the capability of an amplifier to withstand electrical overstress. These questions typically focus on the device inputs, but can involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal ESD protection is built into these circuits to protect them from accidental ESD events both before and during

product assembly. A good understanding of basic ESD circuitry and the relevance of circuitry to an electrical overstress event is helpful. 图 43 illustrates the ESD circuits contained in the INA1650-Q1. The ESD protection circuitry involves several current-steering diodes that are connected from the input and output pins and routed back to the internal power-supply lines. This protection circuitry is intended to remain inactive during normal circuit operation. The input pins of the INA1650-Q1 are protected with internal diodes that are connected to the power-supply rails. These diodes clamp the applied signal to prevent the input circuitry from damage. If the input signal voltage exceeds the power supplies by more than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. A series input resistor can typically limit the current. Some signal sources are inherently current-limited and do not require limiting resistors.



**图 43. INA1650-Q1 Internal ESD Protection Circuitry
(Single Channel and Supply-Divider Shown for Simplicity)**

7.3.5 Thermal Shutdown

If the junction temperature of the INA1650-Q1 exceeds approximately 170°C, a thermal shutdown circuit disables the amplifier to protect the device from damage. The amplifier is automatically re-enabled after the junction temperature falls below the shutdown threshold temperature. If the condition that caused excessive power dissipation is not removed, the amplifier oscillates between a shutdown and enabled state until the output fault is corrected.

7.4 Device Functional Modes

7.4.1 Single-Supply Operation

The INA1650-Q1 can be used on single power supplies ranging from 4.5 V to 36 V. Use the COM and REF pins to level shift the internal voltages into a linear operating condition. Ideally, connecting the REF and COM pins to a midsupply potential (such as the VMID(OUT) pin) avoids saturating the output of the internal amplifiers.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

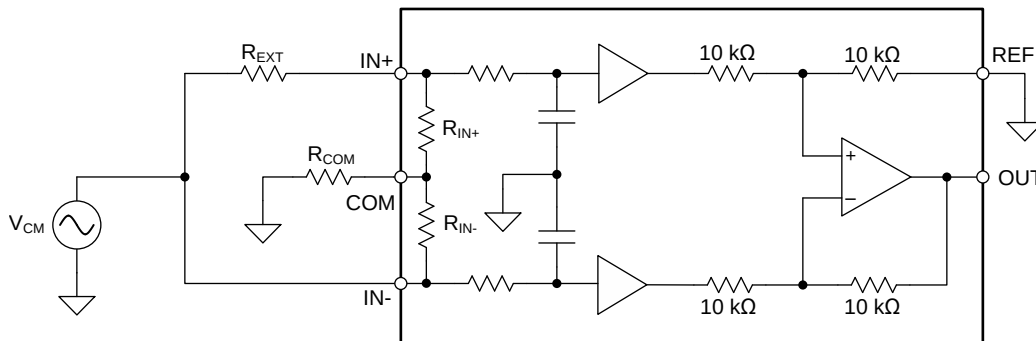
8.1 Application Information

8.1.1 Input Common-Mode Range

The linear input voltage range of the INA1650-Q1 input circuitry extends from 350 mV inside the negative supply voltage to 2 V below the positive supply, and maintains 85-dB (minimum) common-mode rejection throughout this range. The INA1650-Q1 operates over a wide range of power supplies and V_{REF} configurations; providing a comprehensive guide to common-mode range limits for all possible conditions is impractical. The common-mode range for most operating conditions is best calculated using the [INA common-mode range calculating tool](#).

8.1.2 Common-Mode Input Impedance

The high CMRR of many line receivers can degrade by impedance mismatches in the system. 图 44 shows a common-mode noise source (V_{CM}) connected to both inputs of a single channel of the INA1650-Q1. An external parasitic resistance (R_{EXT}) represents the mismatch in impedances between the common-mode noise source and the inputs of the INA1650-Q1. This mismatched impedance may be due to PCB layout, connectors, cabling, passive component tolerances, or the circuit topology. The presence of R_{EXT} in series with the $IN+$ input degrades the overall CMRR of the system because the voltage at $IN+$ is no longer equal to the voltage at $IN-$. Therefore, a portion of the common-mode noise converts to a differential signal and passes to the output.



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图 44. A Single Channel of the INA1650-Q1 Shown With Source Impedance Mismatch (R_{EXT}) and Optional Resistor (R_{COM})

While the INA1650-Q1 is significantly more resistant to these effects than typical line receivers, connecting a resistor (R_{COM}) from the COM pin to the system ground further improves CMRR performance. 图 45 shows the CMRR of the INA1650-Q1 (typical CMRR of 92 dB) for increasing source impedance mismatches. If the COM pin is connected directly to ground (R_{COM} equal to 0 Ω), a 20- Ω source impedance mismatch degrades the CMRR from 92 dB to 83.7 dB. However, if R_{COM} has a value of 1 M Ω , the CMRR only degrades to 89.6 dB, which is an improvement of approximately 6 dB.

Application Information (接下页)

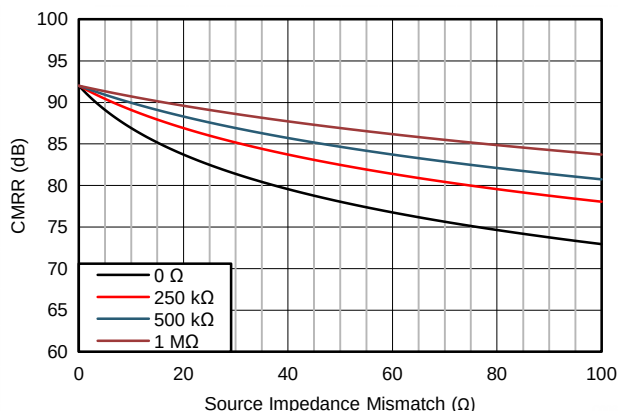


图 45. CMRR vs Source Impedance Mismatch for Different R_{COM} Values

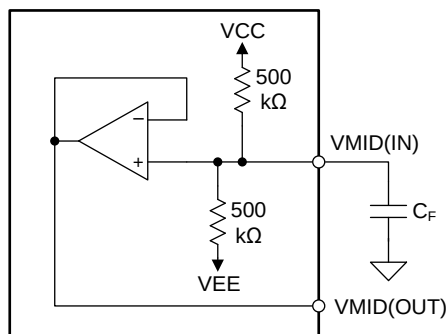
R_{COM} does not need to be a high-precision resistor with a very tight tolerance. Low-cost 5% or 1% resistors can be used with no degradation in overall performance. The addition of R_{COM} does not increase the noise of the audio signal path.

In single-supply systems where AC coupling is used at the inputs of the INA1650-Q1, adding R_{COM} lengthens the start-up time of the circuit. The input AC-coupling capacitors are charged to the midsupply voltage through the R_{COM} resistor, which may take a substantial amount of time if R_{COM} has a large value (such as 1 MΩ). Do not use R_{COM} in these systems if start-up time is a concern. In dual-supply systems with input AC-coupling capacitors, the capacitor voltage does not need to be charged to a midsupply point, because the capacitor voltage settles to ground by default. Therefore, R_{COM} does not increase start-up time in dual-supply systems.

8.1.3 Start-Up Time in Single-Supply Applications

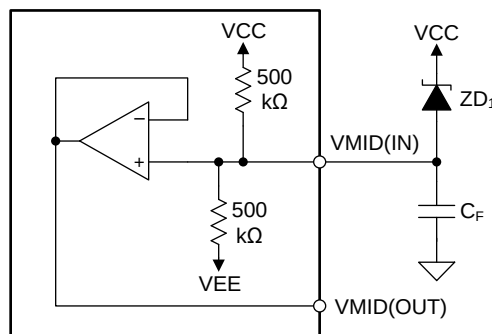
The internal supply divider of the INA1650-Q1 is constructed using two 500-kΩ resistors connected in series between the VCC and VEE pins. These resistors are matched on-chip to provide a reference voltage that is exactly one half of the power supply voltage. Noise from the power supplies and thermal noise from the resistors degrades the overall audio performance of the INA1650-Q1 if allowed to enter the signal path. Therefore, TI recommends a filter capacitor (C_F) is connected to the VMID(IN) pin, as shown in 图 46. The C_F capacitor forms a low-pass filter with the internal 500-kΩ resistors. Noise above the corner frequency of this filter is passed to ground and is removed from the audio signal path. The corner frequency of the filter is shown in 公式 3:

$$F_{-3dB} = \frac{1}{2 \cdot \pi \cdot 250 \text{ k}\Omega \cdot C_F} \quad (3)$$



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图 46. Connect a Capacitor (C_F) to the VMID(IN) Pin to Reduce Noise from the Voltage Divider



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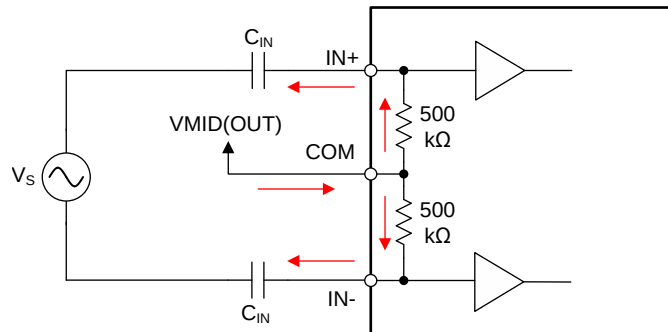
图 47. A Zener Diode (ZD1) Connected to the Positive Supply Can Decrease Start-Up Time

Application Information (接下页)

When power is applied to the INA1650-Q1, the filter capacitor (C_F) charges through the internal 500-k Ω resistors. If the C_F capacitor has a large value, the time required for $V_{MID(OUT)}$ to reach the final midsupply voltage may be extensive. Adding a zener diode from the VMID(IN) pin to the positive power supply (as shown in 图 47) reduces this time. The zener voltage must be slightly greater than one half of the power supply voltage.

Using large AC-coupling capacitors increases the start-up time of the line receiver circuit in single-supply applications. When power is applied, the AC-coupling capacitors begin to charge to the midsupply voltage applied to the COM pin through a current flowing through the input resistors as shown in 图 48. The INA1650-Q1 functions properly when the input common-mode voltage (and the capacitor voltage) is within the specified range. The time required for the input common-mode voltage to reach 98% of the final value is shown in 公式 4:

$$T_{98\%} = 4 \cdot R \cdot C_{IN} = 4 \cdot 500 \text{ k}\Omega \cdot C_{IN} \quad (4)$$



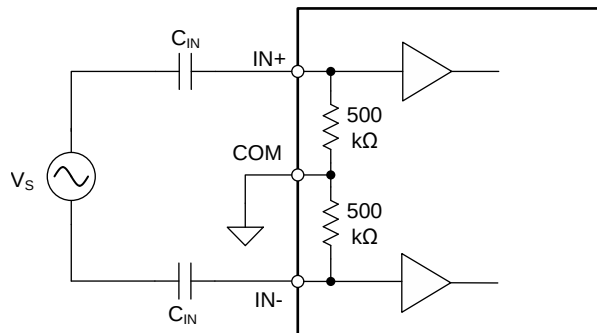
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图 48. AC-Coupling Capacitors Charge to the Mid-Supply Voltage Through the Input Resistors

8.1.4 Input AC Coupling

The signal path in most audio systems is typically AC-coupled to avoid the propagation of DC voltages, which can potentially damage loudspeakers or saturate power amplifiers. The capacitor values must be selected to pass the desired bandwidth of audio signals. The high-pass corner frequency is calculated with 公式 5:

$$F_C = \frac{1}{2 \cdot \pi \cdot (2 \cdot R_{IN}) \cdot \frac{C_{IN}}{2}} = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} \quad (5)$$



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图 49. AC-Coupling Capacitors Form a High-Pass Filter With INA1650-Q1 Input Resistors

Application Information (接下页)

Although the input resistors of the INA1650-Q1 are matched typically within 0.01%, large capacitors are usually mismatched. The mismatch in the values of the AC-coupling capacitors causes the corner frequencies at the two signal inputs (IN+ and IN–) to be different, which can degrade CMRR at low frequency. For this reason, TI recommends placing the high-pass corner frequency well below the audio bandwidth and to use a resistor in series with the COM pin (R_{COM}), as shown in 图 44 if possible. See the [Common-Mode Input Impedance](#) section for more information on placing a resistor in series with the COM pin. 图 50 shows the effect of a 5% mismatch in the values of the input AC-coupling capacitors with and without an R_{COM} resistor. Comparing CMRR at 100 Hz: 1- μ F AC-coupling capacitors with a 5% mismatch degrade the CMRR to 75 dB, while 10- μ F capacitors and a 1-M Ω R_{COM} resistor shows 92 dB of CMRR.

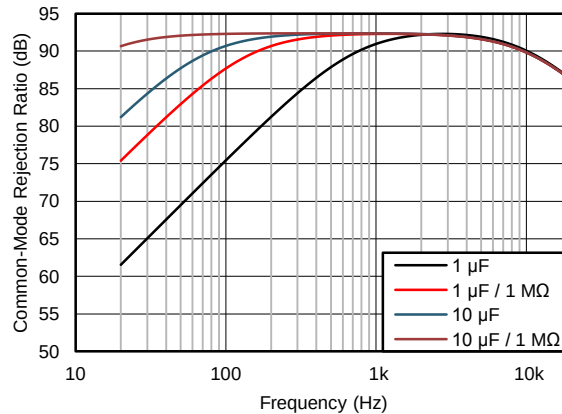
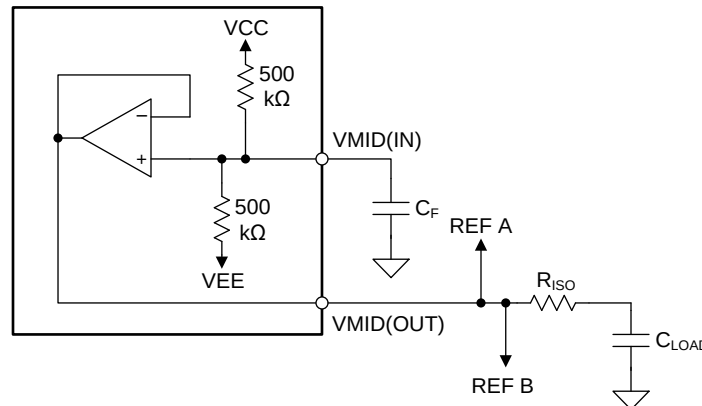


图 50. CMRR Degradation Due to a 5% Mismatch in AC-Coupling Capacitors

8.1.5 Supply Divider Capacitive Loading

The VMID(OUT) pin of the INA1650-Q1 is stable with capacitive loads up to 150 pF. An isolation resistor (R_{ISO} in 图 51), must be used if capacitive loads larger than 150 pF are connected to the VMID(OUT) pin. 图 51 shows the recommended configuration of an isolation resistor in series with the capacitive load. The REF pins of the INA1650-Q1 must connect directly to the VMID(OUT) pin before the isolation resistor. Any resistance placed between the VMID(OUT) pin and the reference pins degrades the CMRR of the device. 图 52 shows the recommended value for the isolation resistor for increasing capacitive loads.



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图 51. Place an Isolation Resistor Between the VMID(OUT) Pin and Large Capacitive Loads

Application Information (接下页)

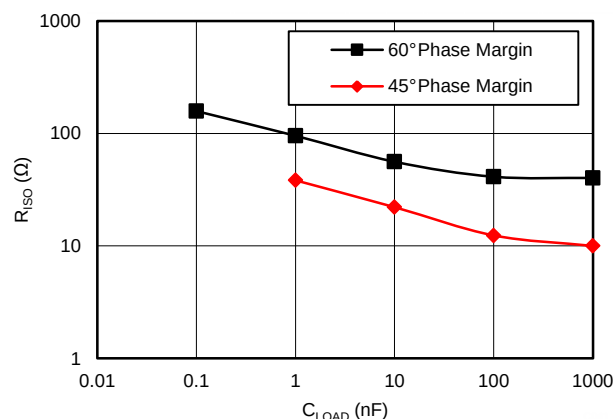
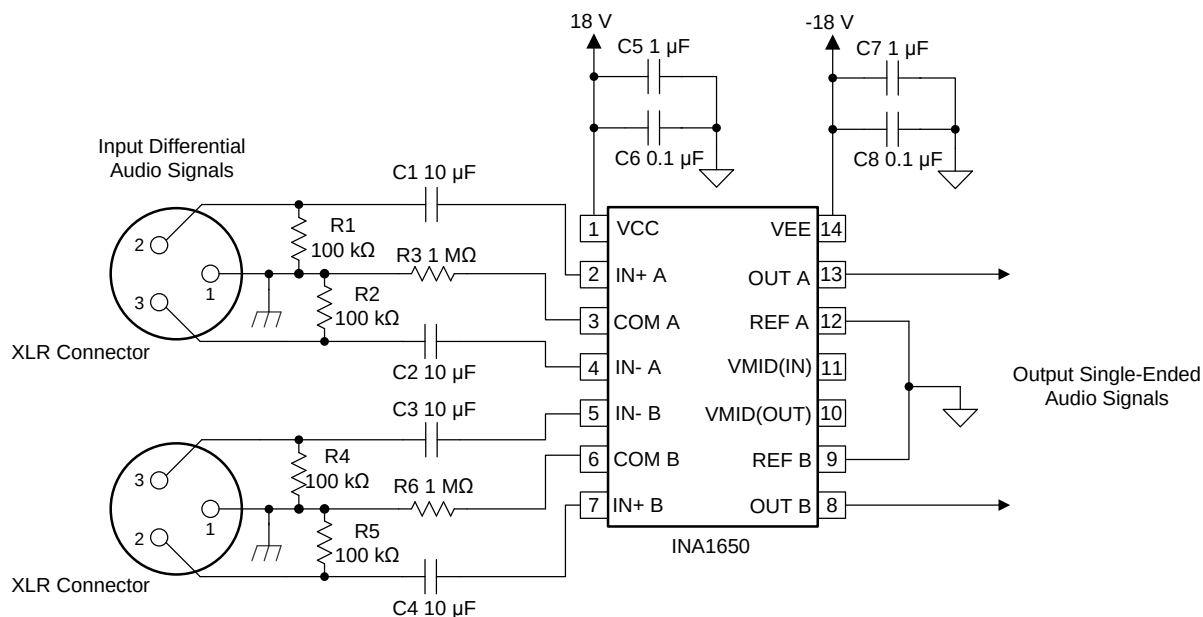


图 52. Recommended Isolation Resistor Value vs Capacitive Load

8.2 Typical Application

The INA1650-Q1 is designed to require a minimum number of external components to achieve data sheet-level performance in audio line-receiver applications. 图 53 shows the INA1650-Q1 device used as a differential audio line receiver in split-supply systems that are common in many audio applications. The line receiver recovers a differential audio signal which may have been affected by significant common-mode noise.



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图 53. INA1650-Q1 Device Used as a Line Receiver for Differential Audio Signals in a Split-Supply System

Typical Application (接下页)

8.2.1 Design Requirements

- Power Supply Voltage: ± 18 V
- Frequency Response: < 0.1 dB deviation from 20 Hz to 20 kHz
- Common-Mode Rejection Ratio: > 80 dB at 1 kHz
- THD+N: < -100 dB (4-dBu input signal, 1-kHz fundamental, 90-kHz measurement bandwidth)

8.2.2 Detailed Design Procedure

The passive components shown in 图 53 are selected using the information given in the [Application Information](#) and [Layout Guidelines](#) sections. All 10- μ F input AC-coupling capacitors (C1, C2, C3, and C4) maximize the CMRR performance at low frequency, as shown in 图 50. The high-pass corner frequency for input signals meets the design requirement for frequency response, as 公式 6 shows:

$$F_C = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} = \frac{1}{2 \cdot \pi \cdot (500 \text{ k}\Omega) \cdot (10 \text{ }\mu\text{F})} = 0.032 \text{ Hz} \quad (6)$$

1-M Ω R_{COM} resistors (R3 and R4) further improve CMRR performance at low frequency. Resistors R1, R2, R4, and R5 provide a discharge pathway for the AC-coupling capacitors in the event that audio equipment with a DC offset voltage is connected to the inputs of the circuit. These resistors are optional and may degrade the CMRR performance with mismatches in source impedance. Finally, capacitors C5, C6, C7, and C8 provide a low-impedance pathway for power supply noise to pass to ground rather than interfering with the audio signal. No connection is necessary on the VMID(IN) and VMID(OUT) pins because the supply-divider circuit is not used in this particular application.

8.2.3 Application Curves

图 54 through 图 59 illustrate the measured performance of the line receiver circuit. 图 54 shows the measured frequency response. The gain of the circuit is 0 dB as expected with 0.1-dB magnitude variation at 10 Hz. The measured CMRR of the circuit (图 55) at 1 kHz equals 94 dB without any source impedance mismatch. Adding a 10- Ω source impedance mismatch degrades the CMRR at 1 kHz to 92 dB. The high-frequency degradation of CMRR shown in 图 55 for the 10- Ω source impedance mismatch cases is due to the capacitance of the cables used for the measurement. The total harmonic distortion plus noise (THD+N) is plotted over frequency in 图 56. For a 4-dBu (1.23 V_{RMS}) input signal level, the THD+N remains flat at -101.6 dB (0.0008%) over the measured frequency range. Increasing the signal level to 22 dBu further decreases the THD+N to -115.2 dB (0.00017%) at 1 kHz, but the THD+N rises above 7 kHz. Measuring the THD+N vs Output Amplitude (图 57) at 1 kHz shows a constant downward slope until the noise floor of the audio analyzer is reached at 5 V_{RMS} . The constant downward slope indicates that noise from the device dominates THD+N at this frequency instead of distortion harmonics. 图 58 and 图 59 confirm this conclusion. For a 4-dBu signal level, the second harmonic is barely visible above the noise floor at -140 dBu. Increasing the signal level to 22 dBu produces distortion harmonics above the noise floor. The largest harmonic in this case is the second at -111.2 dBu, or -133.2 dB relative to the fundamental.

Typical Application (接下页)

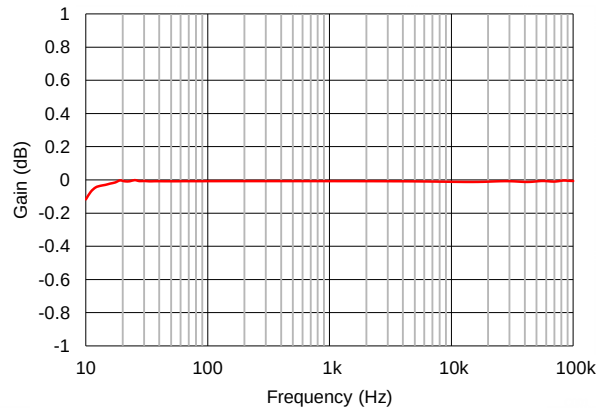


图 54. Frequency Response

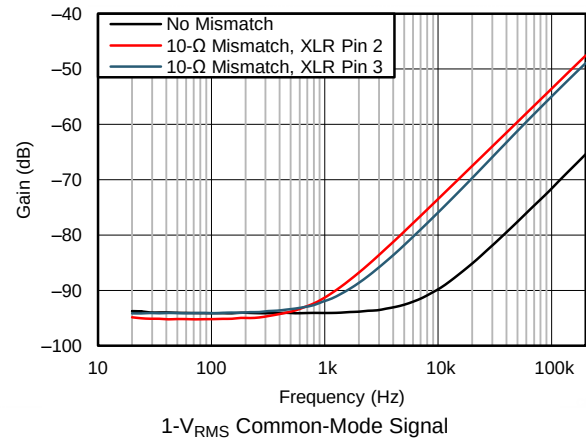


图 55. Common-Mode Rejection Ratio vs Frequency

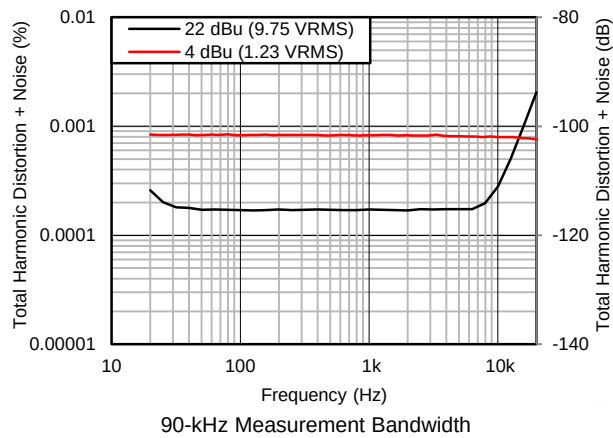


图 56. THD+N vs Frequency

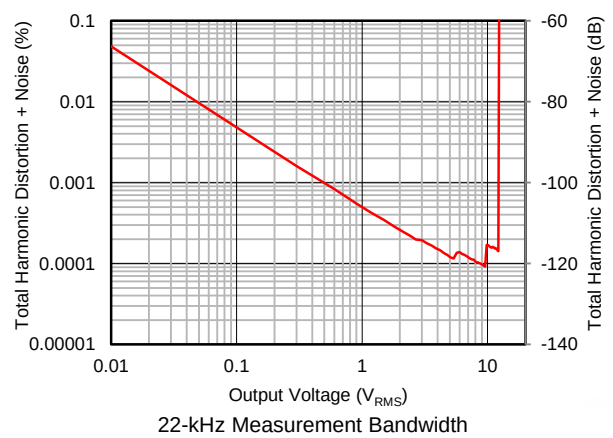


图 57. THD+N vs Amplitude

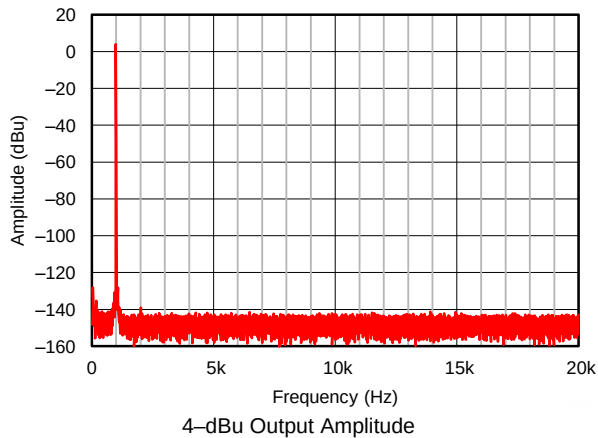


图 58. Output Spectrum

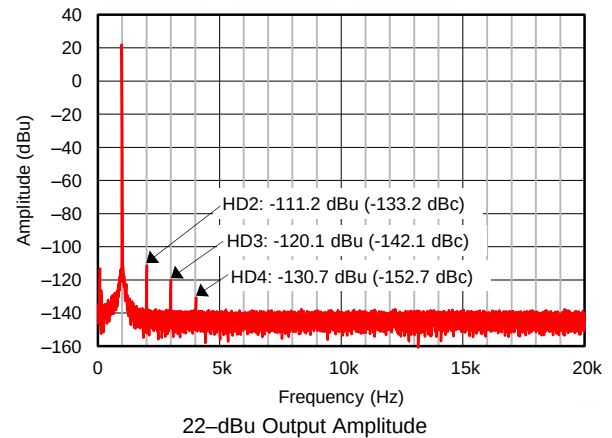


图 59. Output Spectrum

8.3 Other Applications

The low noise and distortion of the INA1650-Q1 make the device well suited for a variety of applications in professional and consumer audio products. However, these same performance metrics make the INA1650-Q1 useful for industrial, test and measurement, and data-acquisition applications. The examples shown here are possible applications where the INA1650-Q1 provides exceptional performance.

8.3.1 Two-Channel Microphone Input for Automotive Infotainment Systems

The high CMRR, low-noise, and ease-of-use in single supply applications make the INA1650-Q1 well suited for applications in automotive infotainment systems. Figure 61 illustrates a high-CMRR input circuit for in-cabin microphones used for hands-free phone systems. The microphones are connected with matched bias resistors, R_{BIAS} , to preserve the high-CMRR performance of the INA1650-Q1. The exact value of the microphone bias voltage, V_{BIAS} , and the R_{BIAS} resistors depends on the particular microphones used. It is common in hands-free systems to bandwidth-limit the audio signal to the range of frequencies for speech. As shown in Figure 61, all filtering components are placed at the output of the INA1650-Q1 rather than the input to preserve high CMRR. The values shown in Figure 61 will limit the signal bandwidth to approximately 100 Hz to 10 kHz.

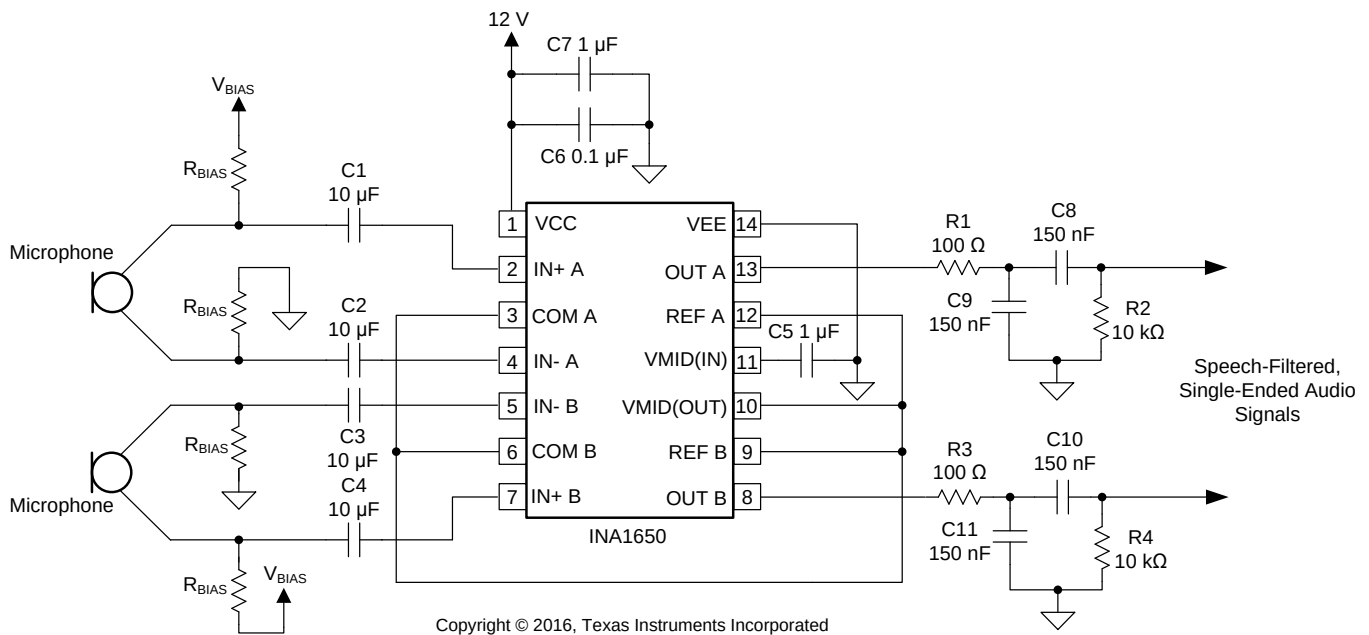
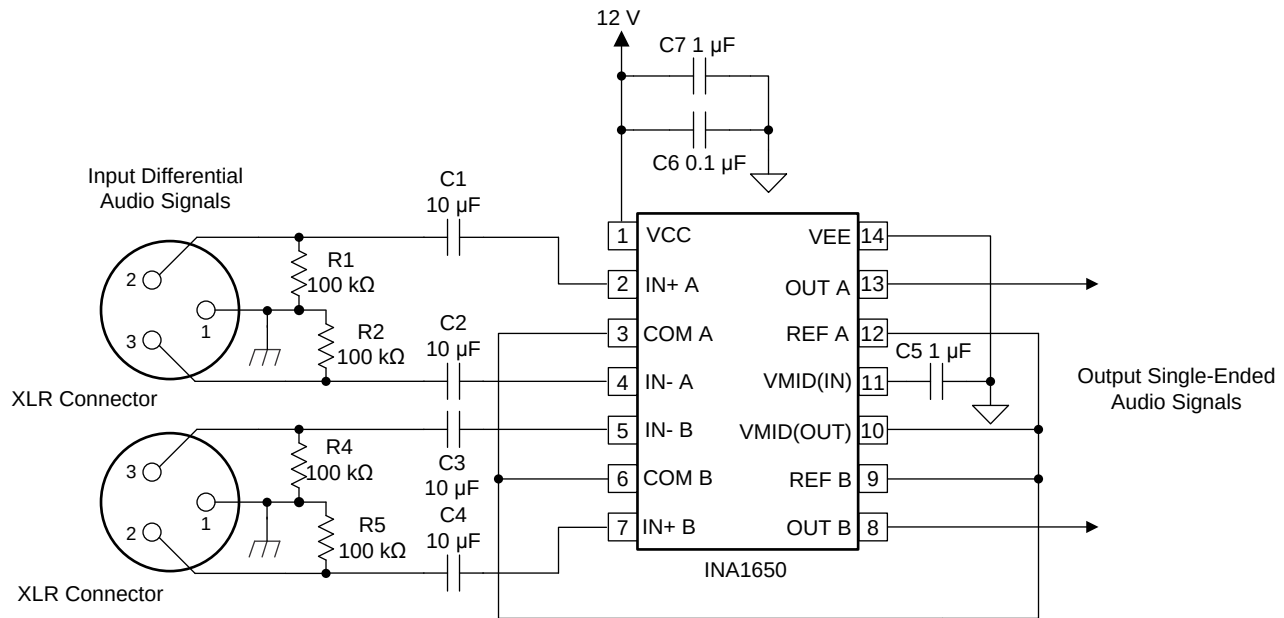


图 60. Two-channel Microphone Input For Automotive Infotainment Systems

8.3.2 Differential Line Receiver for Single-Supply Applications

The INA1650-Q1 can simply operate in single-supply applications by connecting the COM and REF pins to the output of the internal supply divider (VMID(OUT) pin). Adding a 1-μF capacitor to the VMID(IN) pin to filters noise from the power supply and the internal voltage divider.

Other Applications (接下页)



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图 61. Differential Line Receiver for Single-Supply Applications

8.3.3 Floating Single-Ended Input Line Receiver for Ground Loop Noise Reduction

Ground loops commonly form in audio systems where the equipment is interconnected with coaxial cables, which introduces significant common-mode noise. If the sheath of the coaxial cable is connected to the equipment chassis and safety ground, a ground loop forms, which includes the main electrical wiring and the audio signal path. The INA1650-Q1 can break these ground loops by floating the sheath of the coaxial cable through resistors (R3 and R4 in 图 62) so ground noise appears at the inputs of the INA1650-Q1 as a common-mode signal. Capacitors C8 and C9 provide a high-frequency pathway to ground for radio frequency interference (RFI). A transient voltage suppressor (TVS) connected between the coaxial sheath and the chassis ground is shown in 图 62. This TVS protects the inputs of the INA1650-Q1 in the event of an electrostatic discharge to the signal input.

Other Applications (接下页)

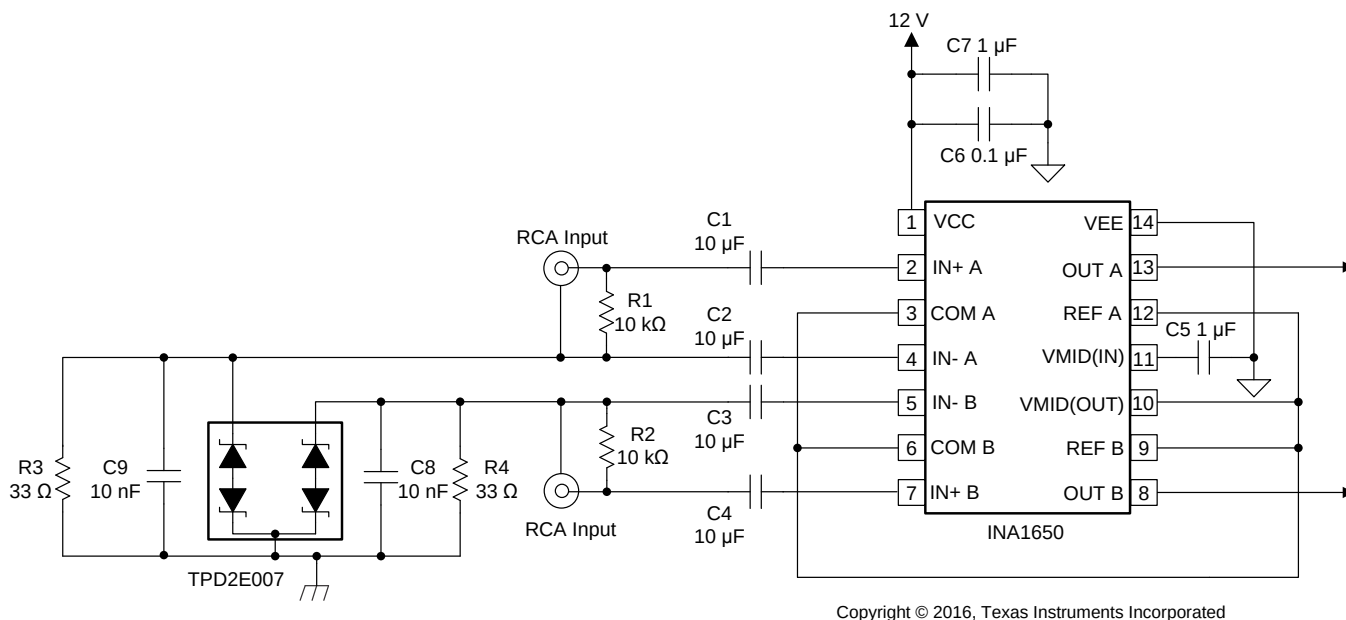


图 62. Ground Loop Isolation in Single-Ended Systems

8.3.4 Floating Single-Ended Input Line Receiver With Differential Outputs

The application in 图 62 can be further extended to include differential outputs, which are necessary for audio ADCs and many Class-D amplifier devices. 图 63 shows the addition of an OPA1688 audio operational amplifier to the outputs of the INA1650-Q1 that convert the single-ended outputs to differential outputs.

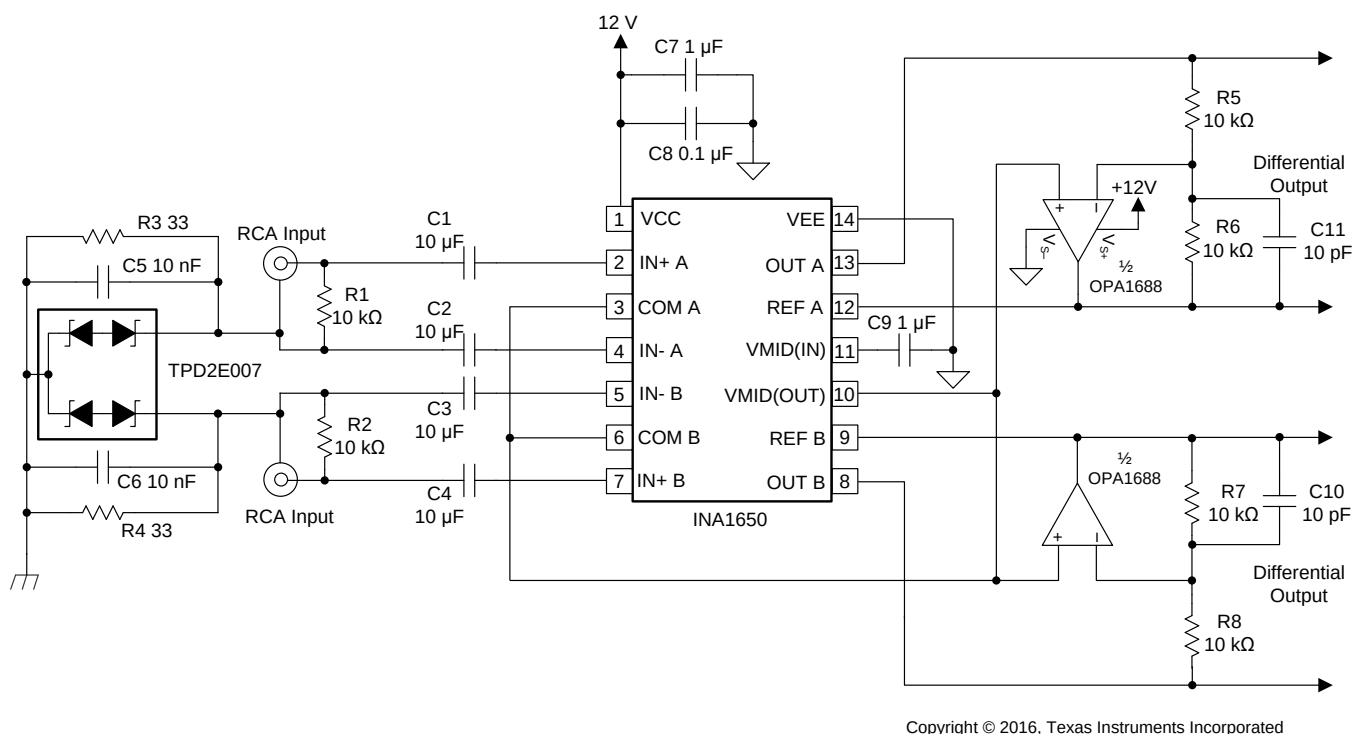


图 63. Single-Ended Line-Receiver Circuit With Differential Outputs

Other Applications (接下页)

8.3.5 TRS Audio Interface in Single-Supply Applications

The INA1650-Q1 can be used for auxiliary audio inputs which may use a tip-ring-sleeve (TRS) connector where both audio channels share a common ground connection. 图 64 shows the INA1650-Q1 configured as a line receiver for a TRS interface to remove common-mode noise on the sleeve connection.

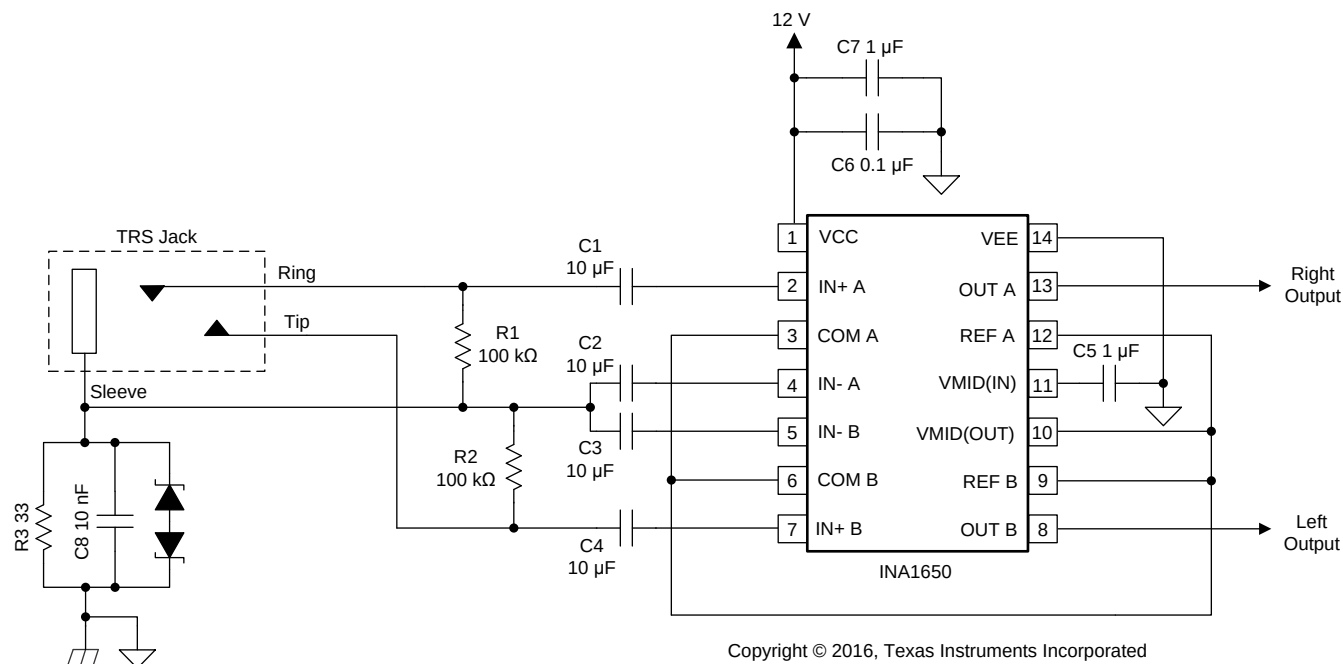
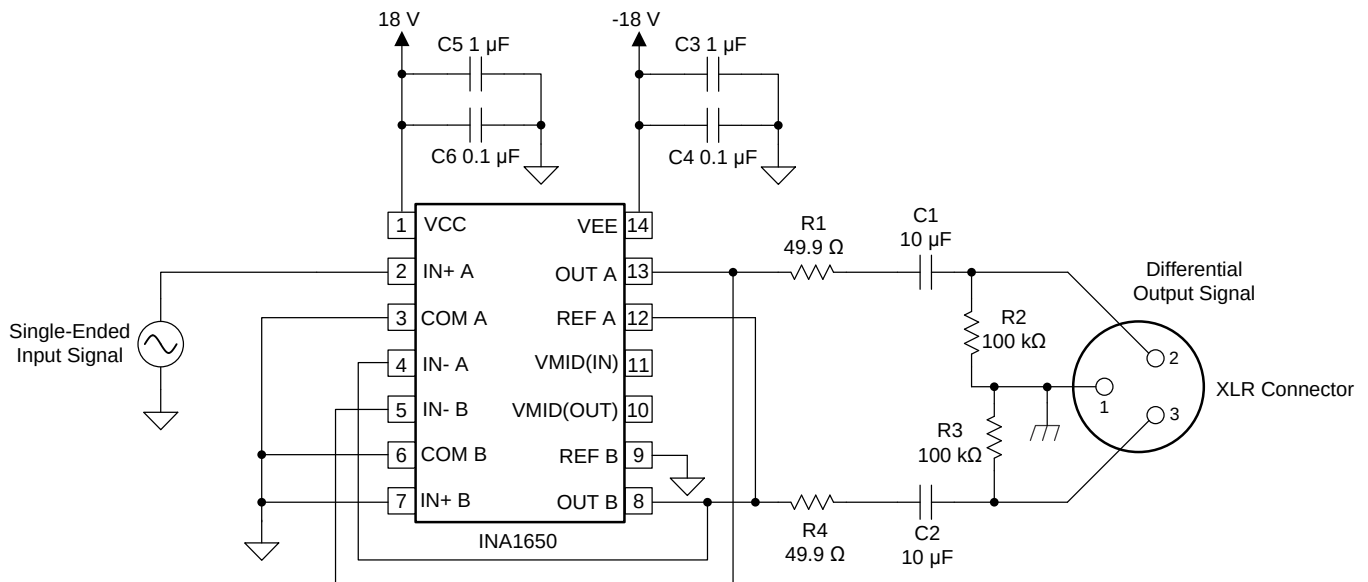


图 64. TRS Audio Interface in Single-Supply Applications

8.3.6 Differential Line Driver With Single-Ended Input

The INA1650-Q1 can be employed in line-driver applications (图 65) where the precision matched internal resistor networks are useful in converting a single-ended signal to a balanced signal. Resistors R1 and R4 (shown in 图 65) isolate the large cable capacitance from the outputs of the INA1650-Q1 to maintain stability. TI recommends AC-coupling capacitors C1 and C2 because the DC voltages of the connected equipment may be unknown. Resistors R2 and R3 dissipate any charge collected on the capacitors due to connecting equipment with a DC voltage present.

Other Applications (接下页)



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图 65. INA1650-Q1 Used as a Balanced Audio Line Driver

9 Power Supply Recommendations

The INA1650-Q1 operates from ± 2.25 -V to ± 18 -V supplies while maintaining excellent performance. However, some applications do not require equal positive and negative output voltage swing. With the INA1650-Q1, power-supply voltages do not need to be equal. For example, the positive supply can be set to 25 V with the negative supply at -5 V.

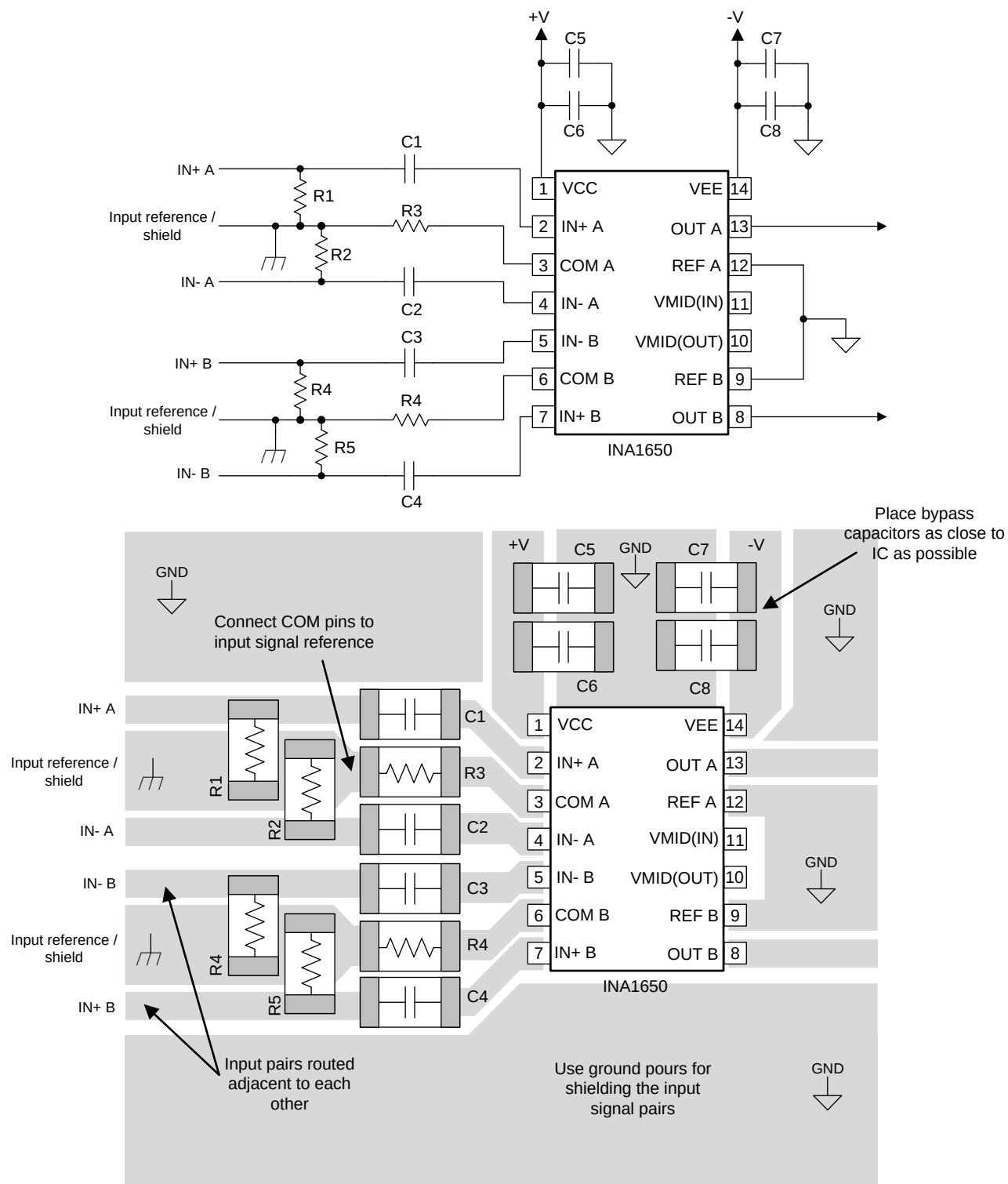
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 1- μ F and 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. Connecting bypass capacitors only from V+ to ground is acceptable in single-supply applications. Noise can propagate into analog circuitry through the power pins of this device. The bypass capacitors reduce the coupled noise by providing low-impedance pathways to ground.
- Connect the device REF pins to a low-impedance, low-noise, system reference point (such as an analog ground or the VMID(OUT) pin) with the shortest trace possible.
- Place the external components as close to the device as possible, as shown in [图 66](#) and [图 67](#).
- Use ground pours and planes to shield input signal traces and minimize additional noise introduced into the signal path.
- Keep the length of input traces equal and as short as possible. Route the input traces as a differential pair with as minimal spacing between them as possible.

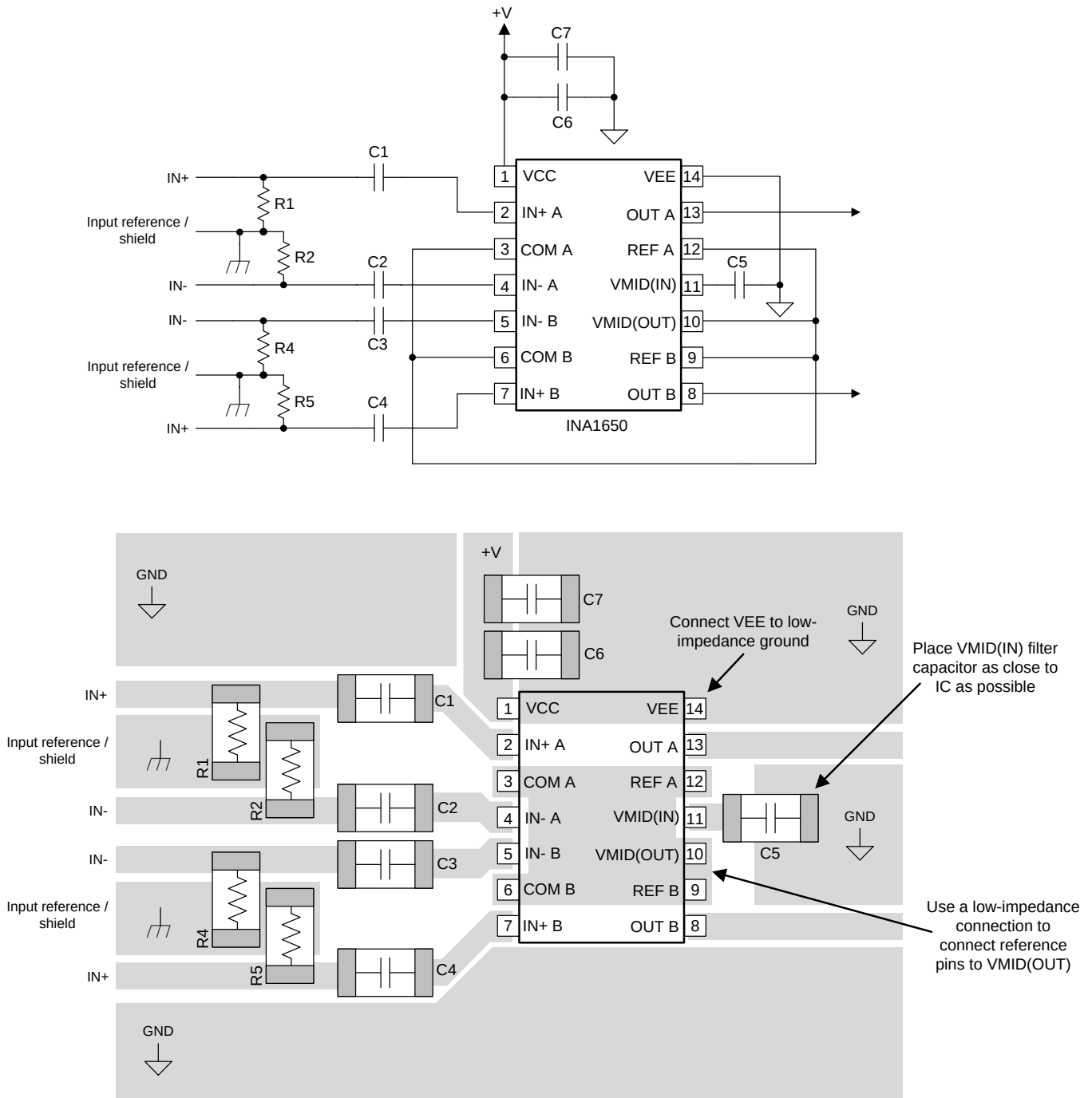
10.2 Layout Example



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图 66. Layout Example for a Dual-Supply Line Receiver

Layout Example (接下页)



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图 67. Layout Example for a Single-Supply Line Receiver

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™ (免费软件下载)

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11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- [《电路板布局布线技巧》](#)

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA1650QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IN1650A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

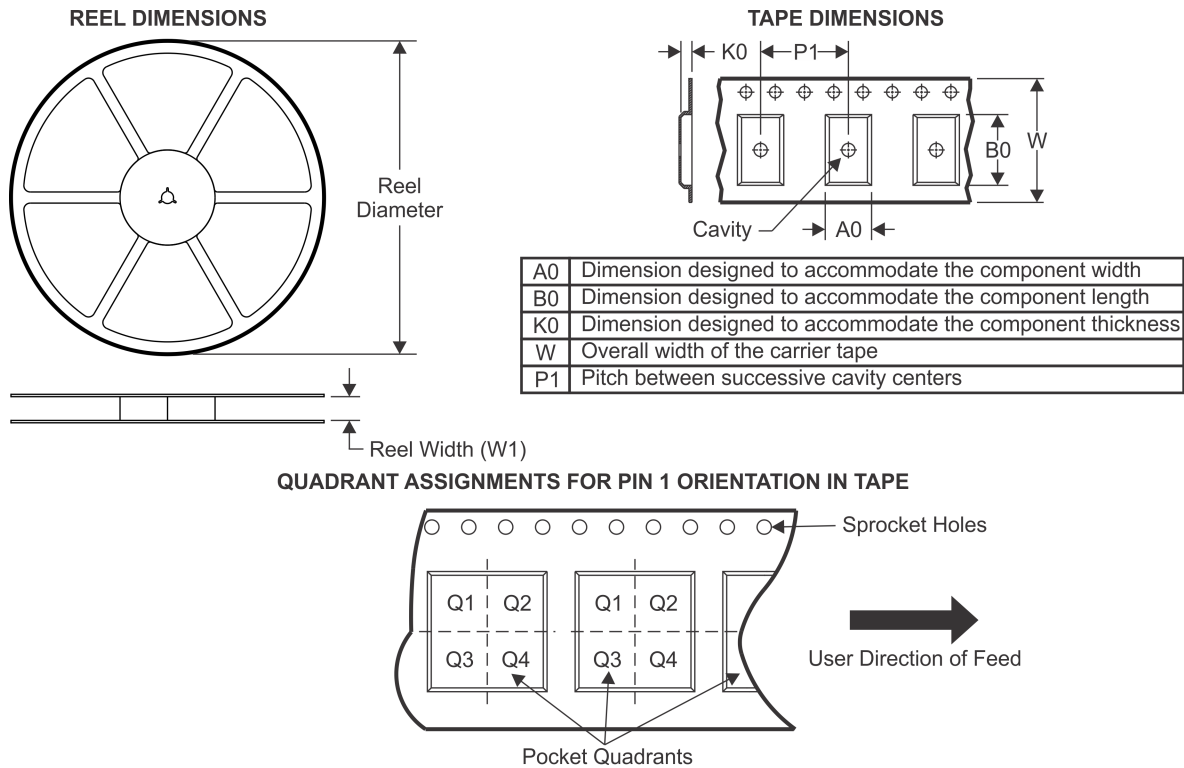
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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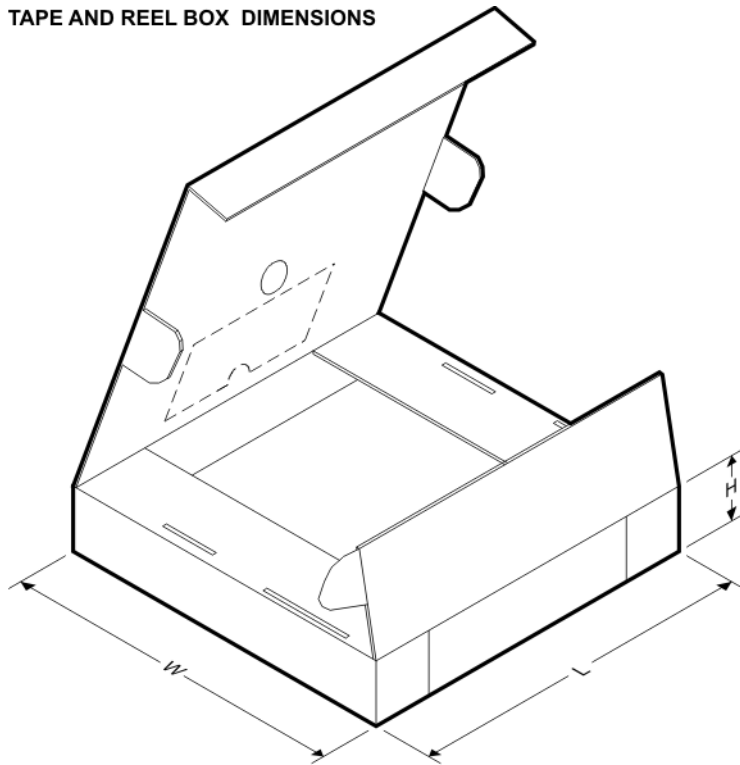
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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA1650QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

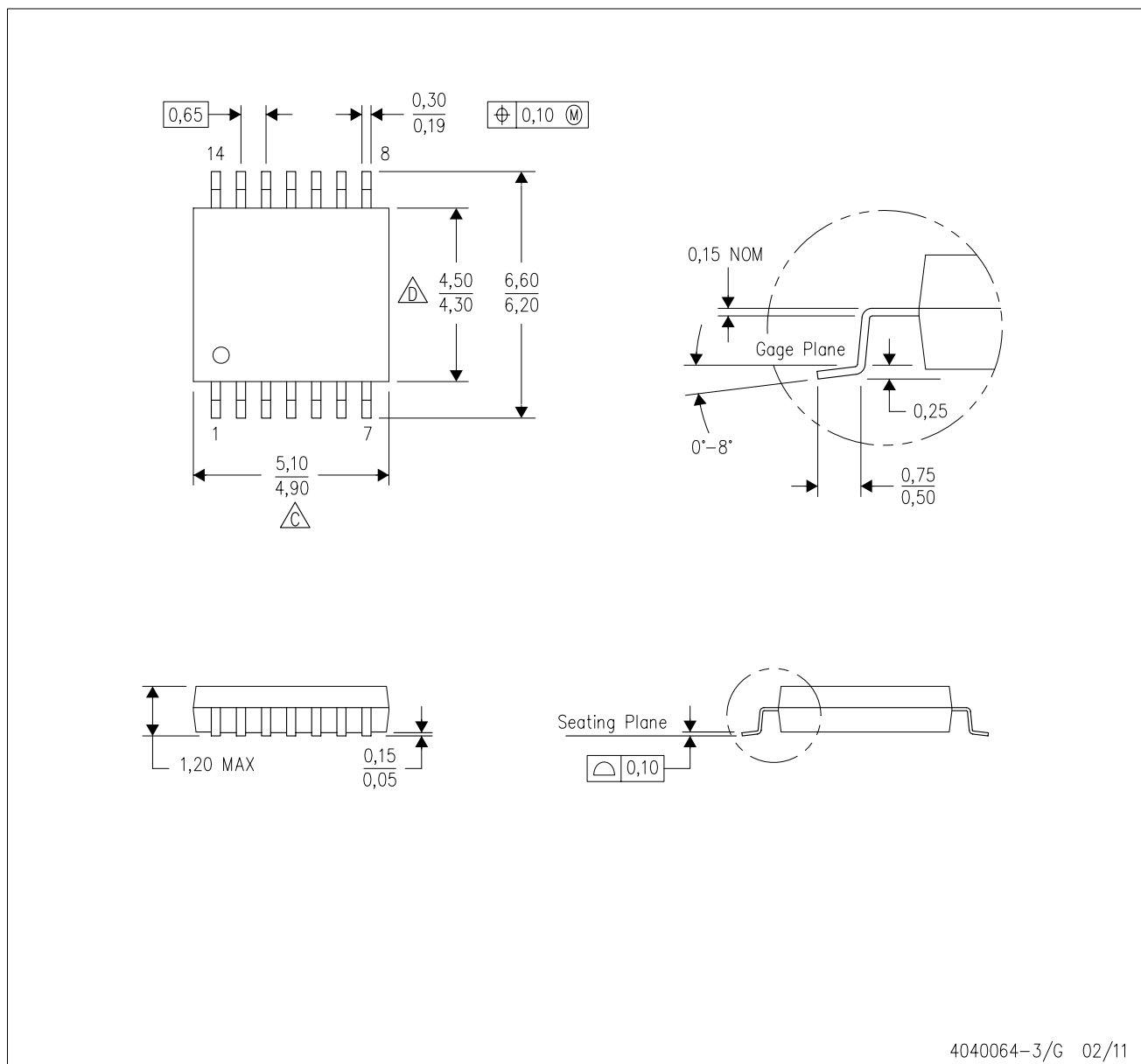


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA1650QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14)

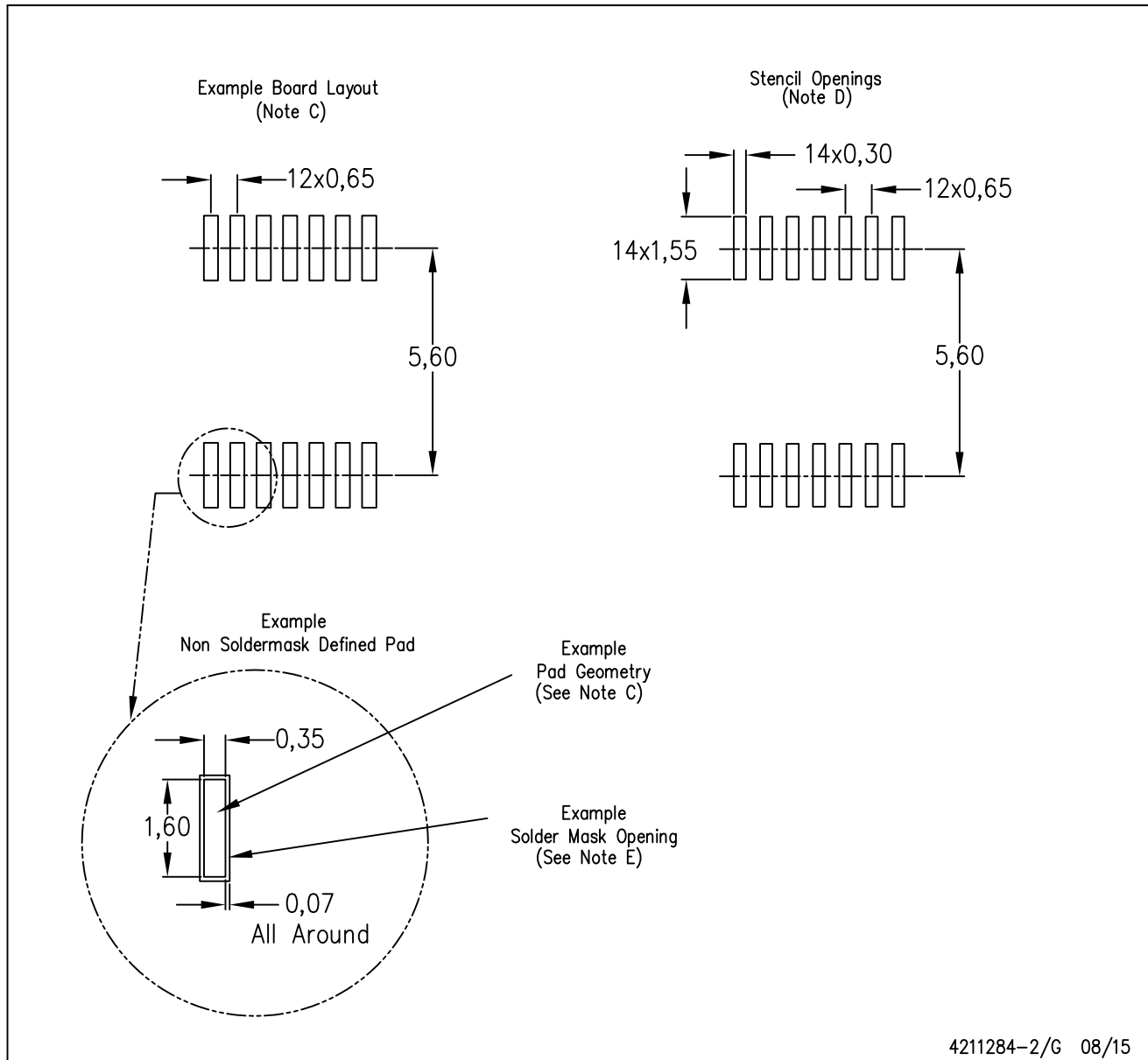
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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
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 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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