

INA592 高精度、宽带宽 e-trim™ 差分放大器

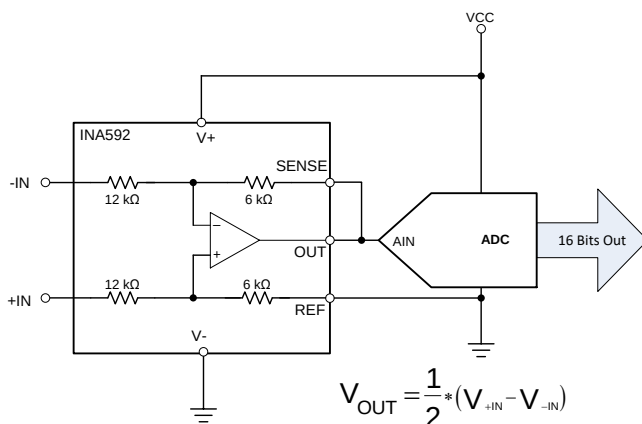
1 特性

- 低失调电压：40μV（最大值）
- 低失调电压漂移：±2μV/°C（最大值）
- 低噪声：1kHz 时为 18nV/√Hz
- 低增益误差：±0.03%（最大值）
- 高共模抑制：88dB（最小值）
- 宽带宽：2MHz GBW
- 低静态电流：每个放大器 1.1mA
- 高转换率：18V/μs
- 高电容负载驱动能力：500pF
- 宽电源范围：
 - 单电源：4.5 V 至 36 V
 - 双电源：±2.25V 至 ±18V
- 额定温度范围：-40°C 至 +125°C
- 8 引脚 VSSOP 封装

2 应用

- 交流驱动器位置反馈
- 伺服驱动器位置反馈
- 状态监控（电压、电流）
- 保护继电器
- 电源模块
- 差分到单端信号转换
- 仪表放大器构建块
- G = 1/2 放大器
- G = 2 放大器
- 自动测试设备

INA592 在差分输入数据采集应用中



3 说明

INA592 器件是一款低功耗、宽带宽差分放大器，由精密运算放大器和精密电阻器网络组成。电阻器的出色 (TCR) 跟踪在全温度范围内保持增益精度和共模抑制。INA592 拥有诸如低失调电压 40μV（最大值）、低失调电压温漂（最大值 2μV/°C）、高转换率 (18V/μs) 和高达 500pF 的高电容负载驱动等独特的特性，从而使其成为稳健耐用的高性能差分放大器，适用于各种高压的工业级应用。内部运算放大器的共模范围扩展至负电源，从而使器件能够在单电源应用中运行。该器件采用单电源（4.5V 至 36V）或双电源（±2.25V 至 ±18V）运行。

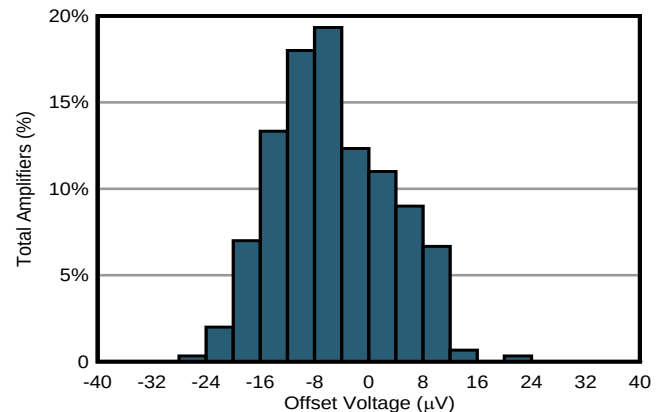
差分放大器是许多常用电路的基础。INA592 提供此电路功能，而无需使用昂贵的精密电阻器网络。INA592 采用 8 引脚 VSSOP 表面贴装封装，规定在 -40°C 至 +125°C 的扩展工业温度范围内运行。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
INA592	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

失调电压的典型分布 (RTO)
G = 1/2, V_S = ±18V



目录

1	特性	1	8.1	Overview	23
2	应用	1	8.2	Functional Block Diagram	23
3	说明	1	8.3	Feature Description	23
4	修订历史记录	2	8.4	Device Functional Modes	23
5	Device Comparison Table	3	9	Application and Implementation	24
6	Pin Configuration and Functions	4	9.1	Application Information	24
7	Specifications	5	9.2	Typical Application	24
7.1	Absolute Maximum Ratings	5	10	Power Supply Recommendations	29
7.2	ESD Ratings	5	11	Layout	30
7.3	Recommended Operating Conditions	5	11.1	Layout Guidelines	30
7.4	Thermal Information	5	11.2	Layout Example	31
7.5	Electrical Characteristics: $G = 1/2, V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$	6	12	器件和文档支持	32
7.6	Electrical Characteristics: $G = 2, V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$	7	12.1	接收文档更新通知	32
7.7	Typical Characteristics - Table of Graphs	8	12.2	社区资源	32
7.8	Typical Characteristics	10	12.3	商标	32
8	Detailed Description	23	12.4	静电放电警告	32
			12.5	术语表	32
			13	机械、封装和可订购信息	32

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (October 2018) to Revision A

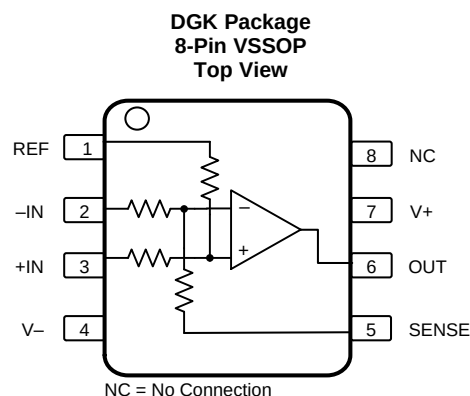
Page

• 首次发布生产数据数据表	1
---------------	---

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION
INA592	High-Precision, Wide-Bandwidth e-trim™ Difference Amplifier	$G = 0.5 \text{ V/V or } 2 \text{ V/V}$
INA159	$G = 0.2 \text{ V}$ differential amplifier for $\pm 10\text{-V}$ to 3-V and 5-V conversion	$G = 0.2 \text{ V/V}$
INA137	Audio Differential Line Receiver $\pm 6\text{dB}$ ($G = 1/2$ or 2)	$G = 0.5 \text{ V/V or } 2 \text{ V/V}$
INA132	Low Power, Single-Supply Difference Amplifier	$G = 1 \text{ V/V}$
INA819	$35\text{-}\mu\text{V}$ Offset, $0.4 \mu\text{V}/^\circ\text{C}$ V_{OS} drift, $8\text{-nV}/\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50\text{k}\Omega\text{hms} / R_G$
INA821	$35\text{-}\mu\text{V}$ Offset, $0.4 \mu\text{V}/^\circ\text{C}$ V_{OS} drift, $7\text{-nV}/\sqrt{\text{Hz}}$ Noise, High-Bandwidth, Precision Instrumentation Amplifier	$G = 1 + 49.4\text{k}\Omega\text{hms} / R_G$
INA333	$25\text{-}\mu\text{V}$ V_{OS} , $0.1 \mu\text{V}/^\circ\text{C}$ V_{OS} drift, 1.8-V to 5-V , RRO, $50\text{-}\mu\text{A}$ I_Q , chopper-stabilized INA	$G = 1 + 100\text{k}\Omega\text{hms} / R_G$
PGA280	20-mV to $\pm 10\text{-V}$ programmable gain IA with 3-V or 5-V differential output; analog supply up to $\pm 18 \text{ V}$	digital programmable
PGA112	Precision programmable gain op amp with SPI	digital programmable

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DGK (VSSOP)		
+IN	3	I	12-kΩ resistor to non-inverting terminal of op amp. Used as positive input in $G = \frac{1}{2}$ configuration. Used as reference pin in $G = 2$ configuration.
-IN	2	I	12 kΩ resistor to inverting terminal of op amp. Used as negative input in $G = \frac{1}{2}$ configuration. Connect to output in $G = 2$ configuration.
OUT	6	O	Output
REF	1	I	6-kΩ resistor to non-inverting terminal of op amp. Used as reference pin in $G = \frac{1}{2}$ configuration. Used as positive input in $G = 2$ configuration.
SENSE	5	I	6-kΩ resistor to inverting terminal of op amp. Connect to output in $G = \frac{1}{2}$ configuration. Used as negative input in $G = 2$ configuration.
V+	7	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply
NC	8	—	No internal connection (can be left floating)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V+ to V–		36	V
Input voltage	(3V–) – 0.3 V	(3V+)	V
Output short circuit (to ground)		Continuous	
Operating temperature	–55	125	°C
Junction temperature	–55	125	°C
Storage temperature, T _{stg}		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V _S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA592	UNIT
		DGK (VSSOP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	158	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	48.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	78.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	3.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	77.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: $G = 1/2, V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$

At $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10 \text{ k}\Omega$ connected to ground, and REF pin connected to ground, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE (RTO) ⁽¹⁾							
V _{OS}	Input offset voltage	G = 1/2, RTO, T _A = 25°C, V _S = ±2.25 V to ±3 V, V _{CM} = -3V			±14	±40	μV
V _{OS}	Input offset voltage	G = 1/2, RTO, T _A = 25°C, V _S = ±3 V to ±18 V, V _{CM} = V _S / 2			±14	±40	μV
dV _{OS} /dT	Input offset voltage drift				±0.7	±2.0	μV/°C
PSRR	Power-supply rejection ratio	V _S = ±3V to ±18 V			±0.5	±5	μV/V
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range	V _O = 0 V			(3V–) – 0.3 V	(3V+)	V
CMRR	Common-mode rejection ratio	RTO, 3 [(V–) – 0.1 V]] ≤ V _{CM} ≤ 3 [(V+) – 3 V]	T _A = 25°C	88	100		dB
			T _A = –40°C to 125°C	82	90		dB
CMRR	Common-mode rejection ratio	RTO, 3 [(V+) - 1.5 V)] ≤ V _{CM} ≤ 3 [(V+)]	T _A = 25°C	88	100		dB
			T _A = –40°C to 125°C	72	90		dB
INPUT IMPEDANCE ⁽²⁾							
GAIN							
G	Initial				1/2		V/V
GE	Gain Error	V _O = –10 V to 10 V, V _S = ±15 V			±0.01%	±0.03%	
	Gain vs temperature ⁽³⁾				±0.2	±0.5	ppm/°C
	Gain nonlinearity	V _O = –10 V to 10 V, V _S = ±15 V			1		ppm
OUTPUT							
V _O	Voltage output swing from rail	positive rail, R _L = 10 kΩ to ground			170	220	mV
		negative rail, R _L = 10 kΩ to ground			190	220	mV
I _{SC}	Short-circuit current				±65		mA
C _{LOAD}	Capacitive load (stable operation)	See 图 49					
NOISE							
E _n	Output voltage noise	f = 0.1 Hz to 10 Hz, RTO			3		μVpp
e _n	Output voltage noise density	f = 1 kHz, RTO			18		nV/√Hz
FREQUENCY RESPONSE							
GBW	Small signal bandwidth	–3 dB			2.0		MHz
SR	Slew rate				18		V/μs
t _S	Settling time: 0.1%	V _O = 10-V step			1		μs
	Settling time: 0.01%				1.3		μs
THD+N	Total harmonic distortion + noise	f = 1 kHz, V _O = 2.8 V _{RMS}			0.00038 %		
	Noise floor, RTO	80kHz bandwidth, V _O = 3.5 V _{RMS}			-116		dB
t _{DR}	Overload recovery time				200		ns
POWER SUPPLY							
I _Q	Quiescent current	I _O = 0 mA	T _A = 25°C	1.1		1.2	mA
			T _A = –40°C to 125°C			1.5	mA

(1) Includes effects of input bias and offset currents of amplifier.

(2) Resistors are ratio matched but have $\pm 20\%$ absolute value.

(3) Specified by wafer test to 95% confidence level.

7.6 Electrical Characteristics: $G = 2, V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$

At $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10 \text{ k}\Omega$ connected to ground, and REF pin connected to ground, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE (RTO) ⁽¹⁾							
V _{OS}	Input offset voltage	G = 2, RTO, T _A = 25°C, V _S = ±2.25 V to ±3 V, V _{CM} = -1.5V			±28	±80	μV
V _{OS}	Input offset voltage	G = 2, RTO, T _A = 25°C, V _S = ±3 V to ±18 V, V _{CM} = V _S / 2			±28	±80	μV
dV _{OS} /dT	Input offset voltage drift				±1.4	±4	μV/°C
PSRR	Power-supply rejection ratio	V _S = ±2.25 V to ±18 V			±1	±5	μV/V
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range	V _O = 0 V		1.5 (V-) - 0.15	1.5 (V+)		V
CMRR	Common-mode rejection ratio	RTO, 1.5 [(V-) – 0.1 V)] ≤ V _{CM} ≤ 1.5 [(V+) – 3 V)]	T _A = 25°C	82	94		dB
			T _A = –40°C to 125°C	80	84		dB
CMRR	Common-mode rejection ratio	RTO, 1.5 [(V+) - 1.5 V)] ≤ V _{CM} ≤ 1.5 [(V+)]	T _A = 25°C	82	94		dB
			T _A = –40°C to 125°C	65	84		dB
INPUT IMPEDANCE ⁽²⁾							
GAIN							
G	Initial			2			V/V
GE	Gain Error	V _O = –10 V to 10 V, V _S = ±15 V		±0.01%	±0.03%		
	Gain vs temperature ⁽³⁾			±0.25	±0.5		ppm/°C
	Gain nonlinearity	V _O = –10 V to 10 V, V _S = ±15 V		1			ppm
OUTPUT							
V _O	Voltage output swing from rail	positive rail, R _L = 10 kΩ to ground		130		180	mV
		negative rail, R _L = 10 kΩ to ground		140		180	mV
I _{SC}	Short-circuit current			±65			mA
C _{LOAD}	Capacitive load (stable operation)	see 图 50					
NOISE							
E _n	Output voltage noise	f = 0.1 Hz to 10 Hz, RTO		6			μVpp
e _n	Output voltage noise density	f = 1 kHz, RTO		36			nV/√Hz
FREQUENCY RESPONSE							
GBW	Small signal bandwidth	–3 dB		0.8			MHz
SR	Slew rate			18			V/μs
t _S	Settling time: 0.1%	V _O = 10-V step		1.0			μs
	1.7				μs		
THD+N	Total harmonic distortion + noise	f = 1 kHz, V _O = 2.8 V _{RMS}		0.00066 %			
	Noise floor, RTO	80kHz bandwidth, V _O = 3.5 V _{RMS}		-110			dB
t _{DR}	Overload recovery time			200			ns
POWER SUPPLY							
I _Q	Quiescent current	I _O = 0 mA	T _A = 25°C	1.1		1.2	mA
			T _A = –40°C to 125°C			1.5	mA

(1) Includes effects of input bias and offset currents of amplifier.

(2) Resistors are ratio matched but have $\pm 20\%$ absolute value.

(3) Specified by wafer test to 95% confidence level.

7.7 Typical Characteristics - Table of Graphs

表 1. Table of Graphs

DESCRIPTION	FIGURE
Typical Distribution of Offset Voltage (RTO) $G = 1/2$, $V_s = \pm 2.25V$	图 1
Typical Distribution of Offset Voltage (RTO) $G = 2$, $V_s = \pm 2.25V$	图 2
Typical Distribution of Offset Voltage (RTO) $G = 1/2$, $V_s = \pm 18V$	图 3
Typical Distribution of Offset Voltage (RTO) $G = 2$, $V_s = \pm 18V$	图 4
Typical Distribution of Offset Voltage Drift (RTO) $G = 1/2$	图 5
Typical Distribution of Offset Voltage Drift (RTO) $G = 2$	图 6
Output Offset Voltage vs Temperature $G = 1/2$	图 7
Output Offset Voltage vs Temperature $G = 2$	图 8
Offset Voltage vs Common-Mode Voltage $G = 1/2$	图 9
Offset Voltage vs Common-Mode Voltage $G = 2$	图 10
Input Bias Current vs Temperature $G = 1/2$ and $G = 2$	图 11
Input Offset Current vs Temperature	图 12
Input Bias Current vs Common Mode Voltage $G = 1/2$	图 13
Input Bias Current vs Common Mode Voltage $G = 2$	图 14
Typical CMRR Distribution $G = 1/2$, $V_s = \pm 2.25V$	图 15
Typical CMRR Distribution $G = 2$, $V_s = \pm 2.25V$	图 16
Typical CMRR Distribution $G = 1/2$, $V_s = \pm 18V$	图 17
Typical CMRR Distribution $G = 2$, $V_s = \pm 18V$	图 18
CMRR vs Temperature $G = 1/2$	图 19
CMRR vs Temperature $G = 2$	图 20
Common-Mode Rejection Ratio vs Frequency (RTI) $G = 1/2$ and $G = 2$	图 21
Maximum Output Voltage vs Frequency	图 22
PSRR vs Temperature $G = 1/2$	图 23
PSRR vs Temperature $G = 2$	图 24
PSRR vs Frequency (RTI) $G = 1/2$	图 25
PSRR vs Frequency (RTI) $G = 2$	图 26
Typical Distribution of Gain Error $G = 1/2$, $V_s = \pm 2.25V$	图 27
Typical Distribution of Gain Error $G = 2$, $V_s = \pm 2.25V$	图 28
Gain Error vs Temperature $G = 1/2$	图 29
Gain Error vs Temperature $G = 2$	图 30
Closed-Loop Gain vs Frequency $G = 1/2$	图 31
Closed-Loop Gain vs Frequency $G = 2$	图 32
Voltage Noise Spectral Density vs Frequency (RTI) $G = 1/2$	图 33
Voltage Noise Spectral Density vs Frequency (RTI) $G = 2$	图 34
0.1-Hz to 10-Hz RTI Voltage Noise $G = 1/2$	图 35
0.1-Hz to 10-Hz RTI Voltage Noise $G = 2$	图 36
Integrated Output Voltage Noise vs Noise Bandwidth $G = 1/2$	图 37
Integrated Output Voltage Noise vs Noise Bandwidth $G = 2$	图 38
Positive Output Voltage vs Output Current (sourcing) $G = 1/2$	图 39
Positive Output Voltage vs Output Current (sourcing) $G = 2$	图 40
Negative Output Voltage vs Output Current (sinking) $G = 1/2$	图 41
Negative Output Voltage vs Output Current (sinking) $G = 2$	图 42
Settling Time $G = 1/2$	图 43
Settling Time $G = 2$	图 44
Large Signal Step Response $G = 1/2$	图 45
Large Signal Step Response $G = 2$	图 46

Typical Characteristics - Table of Graphs (接下页)

表 1. Table of Graphs (接下页)

DESCRIPTION	FIGURE
Slew Rate over Temperature	图 47
Overload Recovery (Normalized to 0V)	图 48
Small-Signal Overshoot vs Capacitive Load $G = 1/2$	图 49
Small-Signal Overshoot vs Capacitive Load $G = 2$	图 50
Small-Signal Step Response $G = 1/2$	图 51
Small-Signal Step Response $G = 2$	图 52
THD+N vs Frequency $G = 1/2$	图 53
THD+N vs Frequency $G = 2$	图 54
THD+N Ratio vs Output Amplitude $G = 1/2$	图 55
THD+N Ratio vs Output Amplitude $G = 2$	图 56
Supply Current vs Temperature $G = 1/2$	图 57
Supply Current vs Temperature $G = 2$	图 58
Supply Current vs Supply Voltage $G = 1/2$	图 59
Supply Current vs Supply Voltage $G = 2$	图 60
Short Circuit Current vs Temperature $G = 1/2$	图 61
Short Circuit Current vs Temperature $G = 2$	图 62
Differential-Mode EMI Rejection Ratio $G = 1/2$	图 63
Differential-Mode EMI Rejection Ratio $G = 2$	图 64
Common-Mode EMI Rejection Ratio $G = 1/2$	图 65
Common-Mode EMI Rejection Ratio $G = 2$	图 66
Input Common-Mode Voltage vs Output Voltage $G = 1/2$, Bipolar Supply	图 67
Input Common-Mode Voltage vs Output Voltage $G = 2$, Bipolar Supply	图 68
Input Common-Mode Voltage vs Output Voltage $G = 1/2$, 5V Supply	图 69
Input Common-Mode Voltage vs Output Voltage $G = 2$, 5V Supply	图 70
Input Common-Mode Voltage vs Output Voltage $G = 1/2$, 36V Supply	图 71
Input Common-Mode Voltage vs Output Voltage $G = 2$, 36V Supply	图 72
Closed-Loop Output Impedance vs Frequency	图 73

7.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

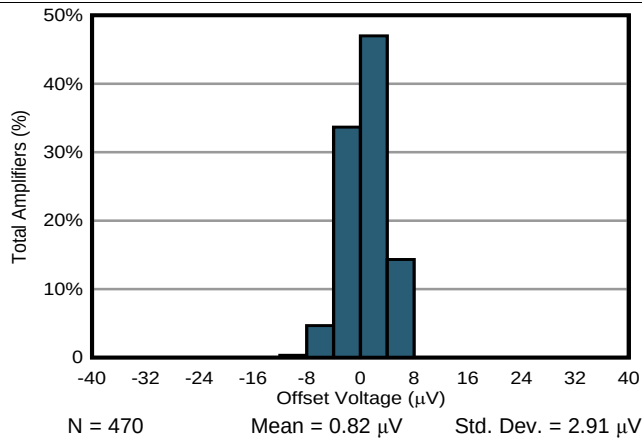


图 1. Typical Distribution of Offset Voltage (RTO)
 $G = 1/2$, $V_S = \pm 2.25\text{ V}$, $V_{CM} = -3\text{ V}$

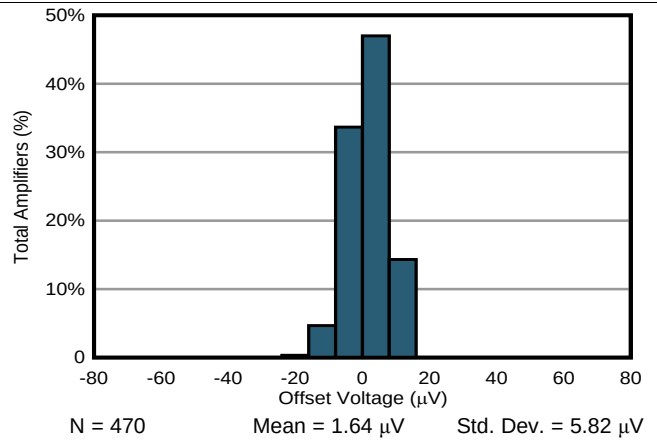


图 2. Typical Distribution of Offset Voltage (RTO) $G = 2$, $V_S = \pm 2.25\text{ V}$, $V_{CM} = -3\text{ V}$

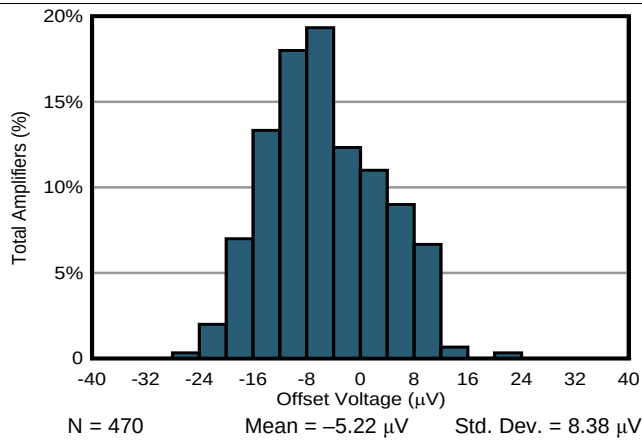


图 3. Typical Distribution of Offset Voltage (RTO)
 $G = 1/2$, $V_S = \pm 18\text{ V}$

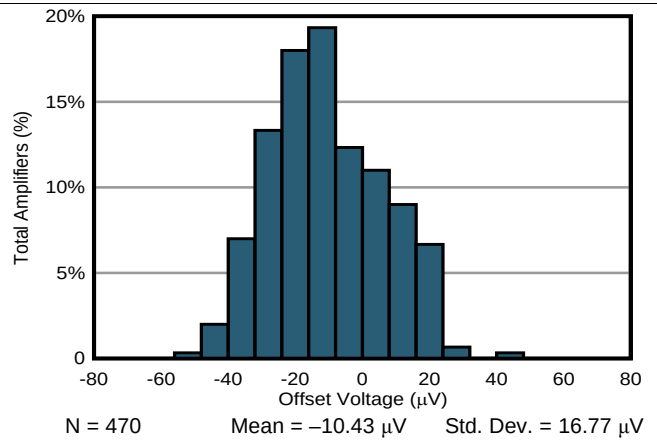


图 4. Typical Distribution of Offset Voltage (RTO) $G = 2$, $V_S = \pm 18\text{ V}$

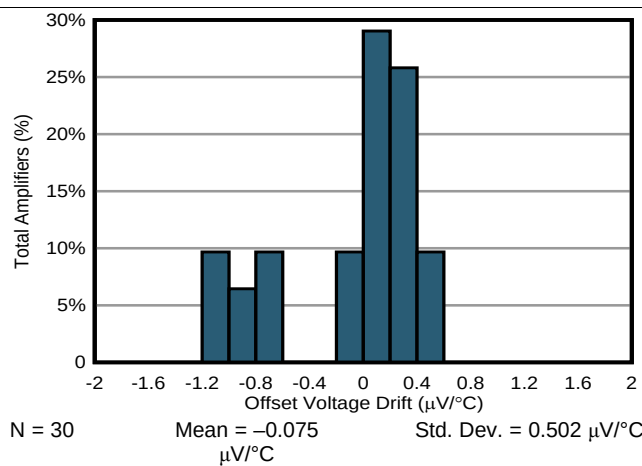


图 5. Typical Distribution of Offset Voltage Drift (RTO) $G = 1/2$

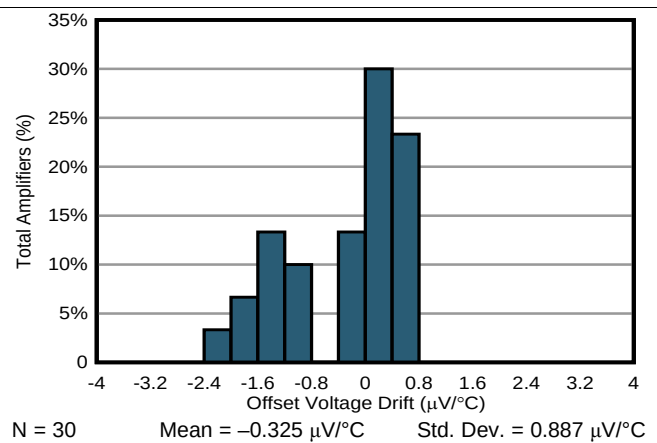


图 6. Typical Distribution of Offset Voltage Drift (RTO) $G = 2$

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

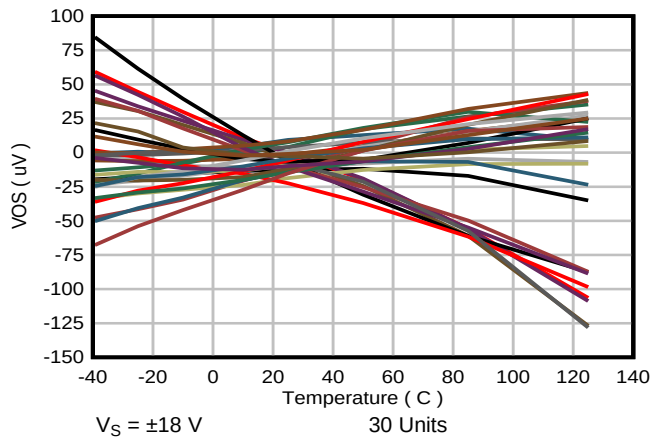


图 7. Output Offset Voltage vs Temperature $G = 1/2$

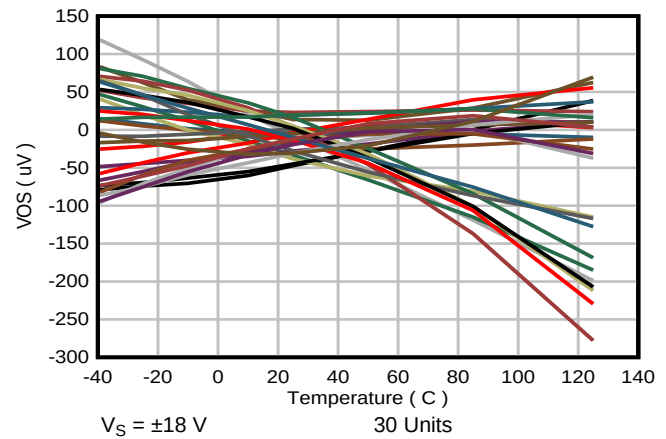


图 8. Output Offset Voltage vs Temperature $G = 2$

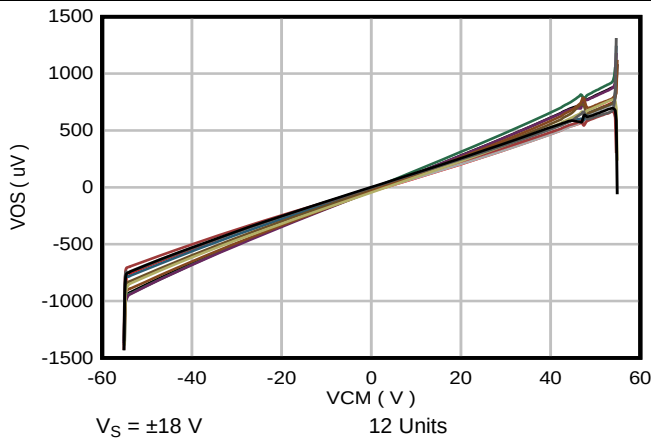


图 9. Offset Voltage vs Common-Mode Voltage $G = 1/2$

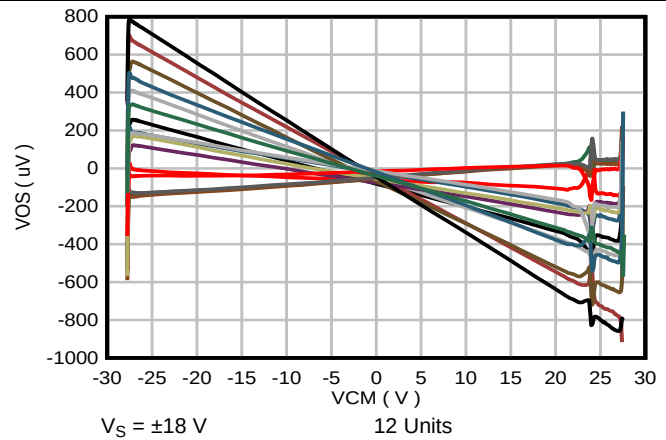


图 10. Offset Voltage vs Common-Mode Voltage $G = 2$

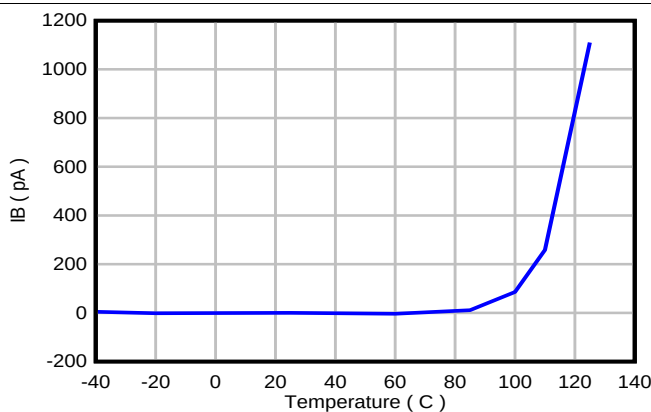


图 11. Input Bias Current vs Temperature

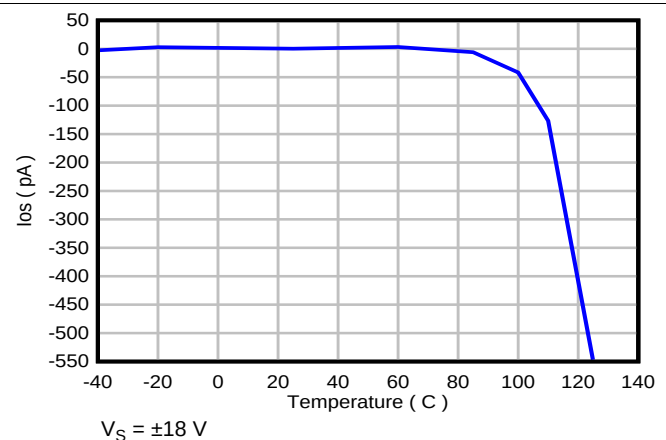


图 12. Input Offset Current vs Temperature

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

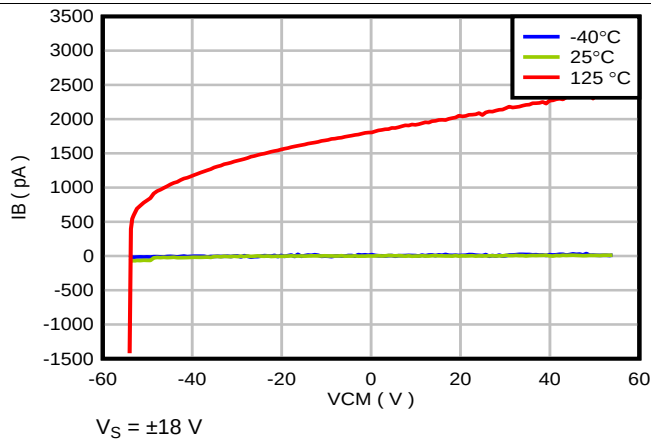


图 13. Input Bias Current vs Common Mode Voltage
 $G = 1/2$

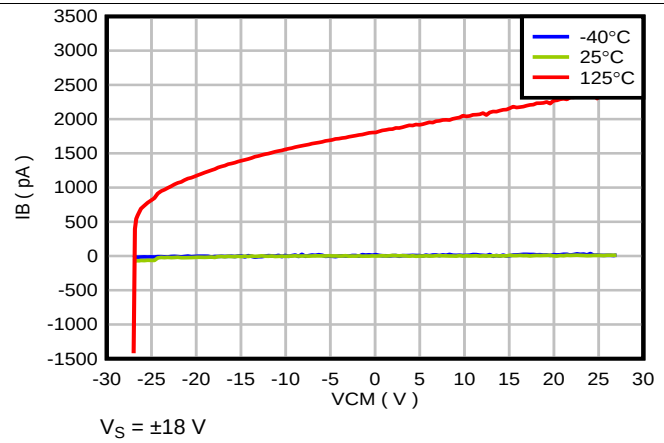


图 14. Input Bias Current vs Common Mode Voltage
 $G = 2$

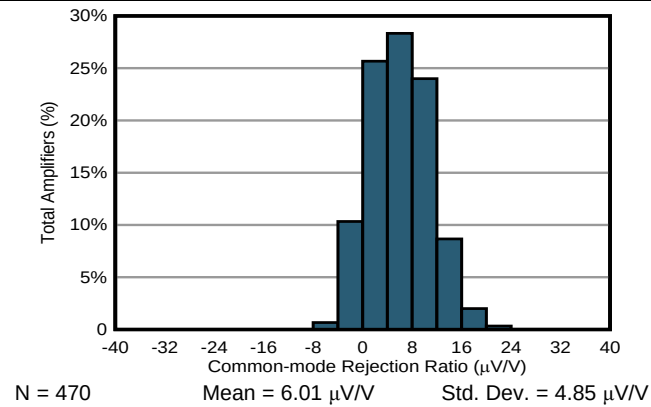


图 15. Typical CMRR Distribution $G = 1/2$, $V_S = \pm 2.25\text{ V}$

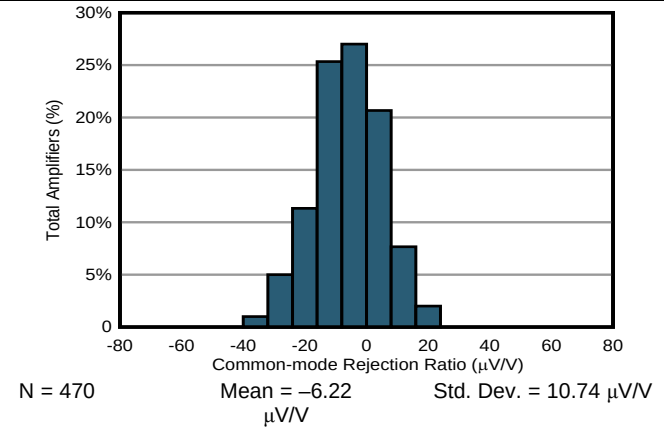


图 16. Typical CMRR Distribution $G= 2$, $V_S = \pm 2.25\text{ V}$

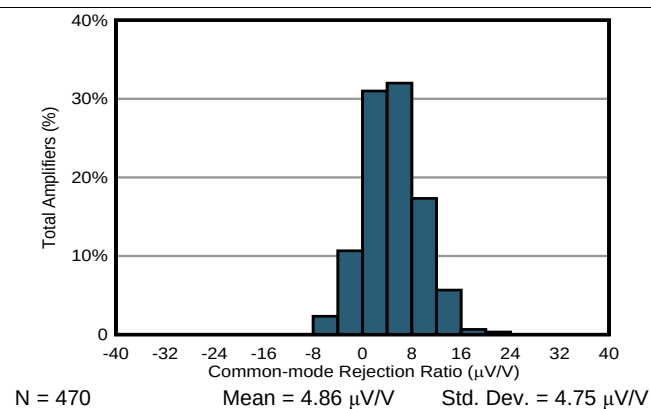


图 17. Typical CMRR Distribution $G = 1/2$, $V_S = \pm 18\text{ V}$

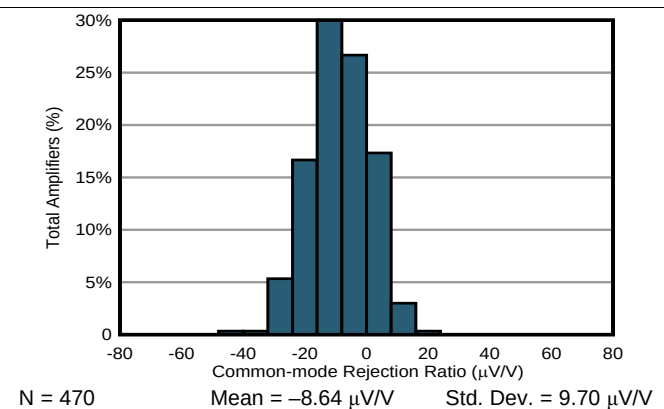
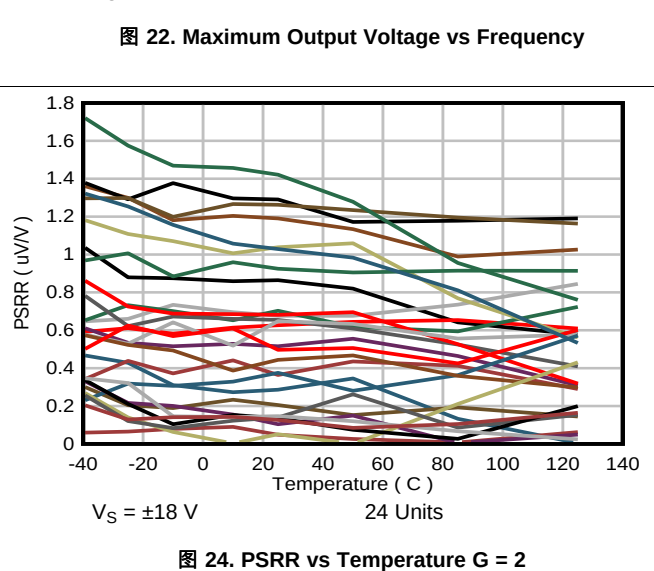
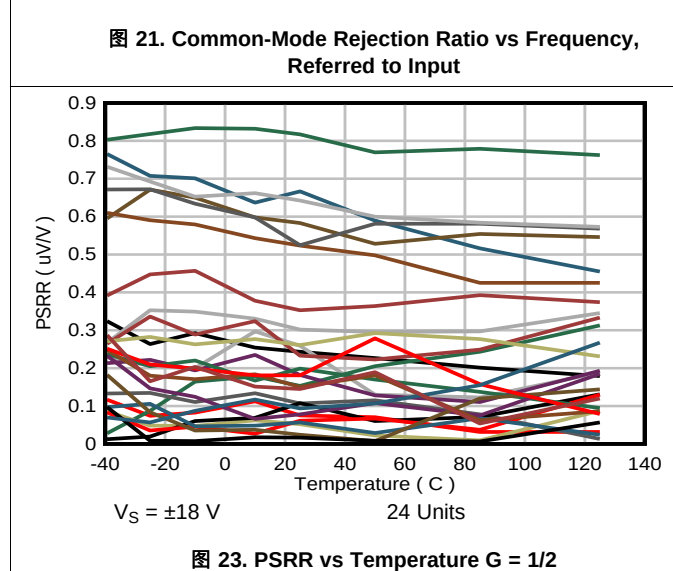
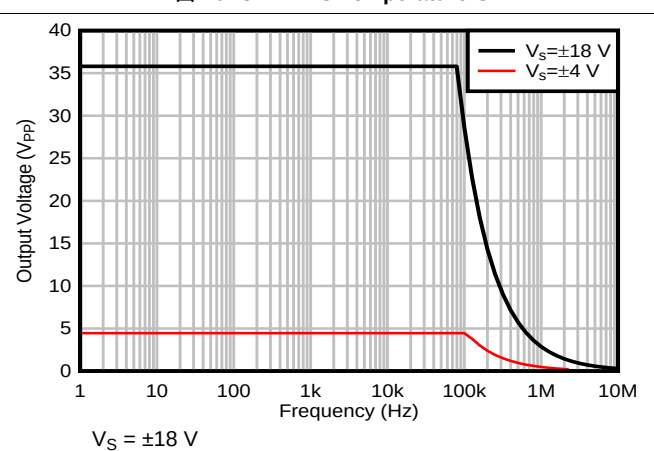
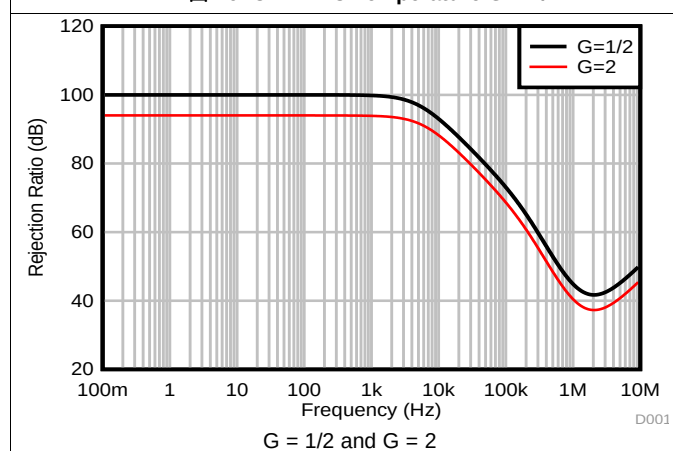
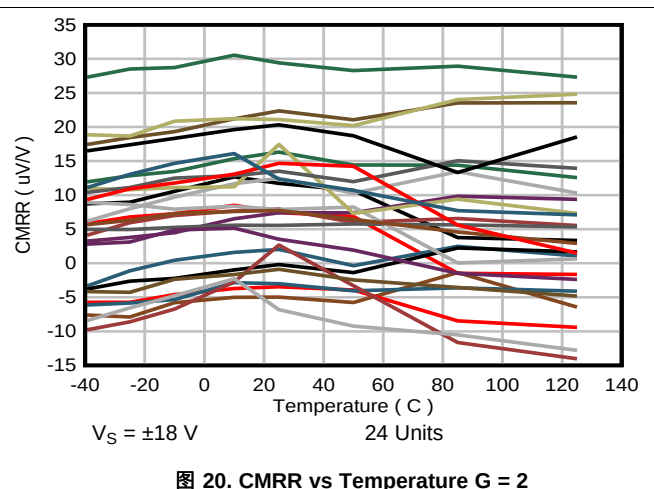
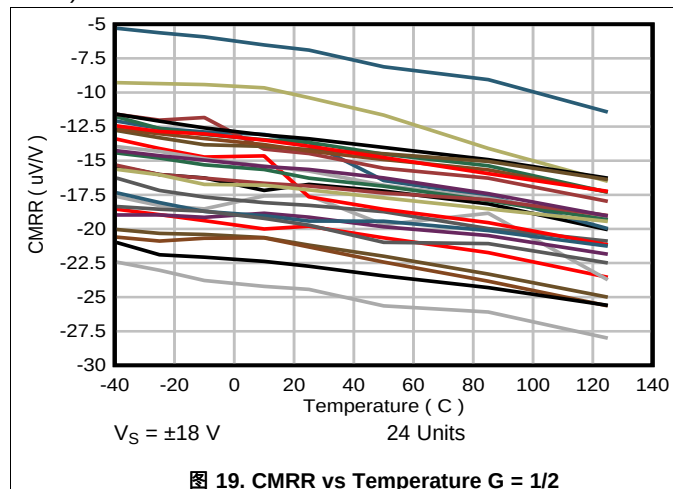


图 18. Typical CMRR Distribution $G= 2$, $V_S = \pm 18\text{ V}$

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).



Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

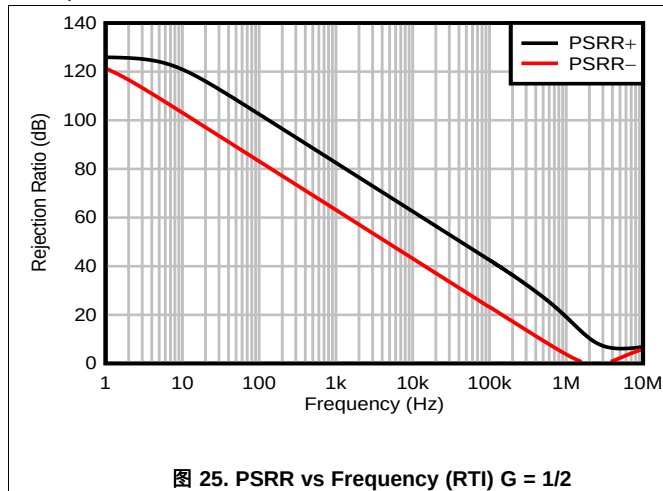


图 25. PSRR vs Frequency (RTI) G = 1/2

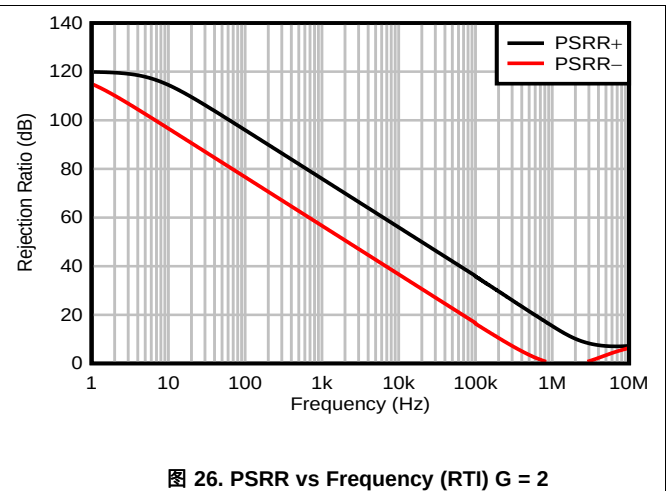


图 26. PSRR vs Frequency (RTI) G = 2

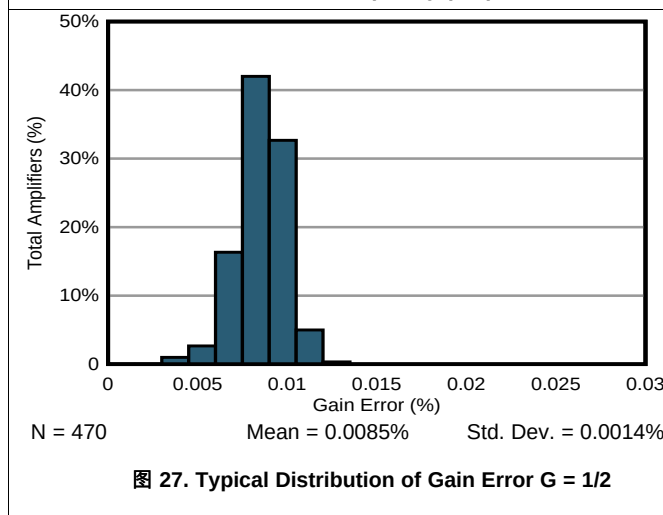


图 27. Typical Distribution of Gain Error G = 1/2

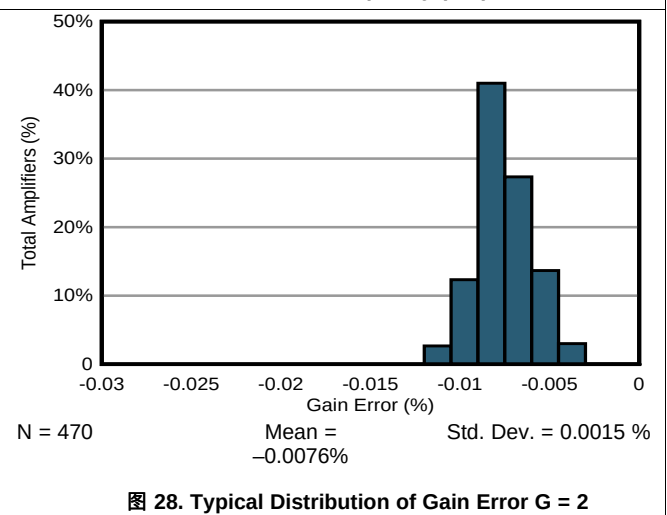


图 28. Typical Distribution of Gain Error G = 2

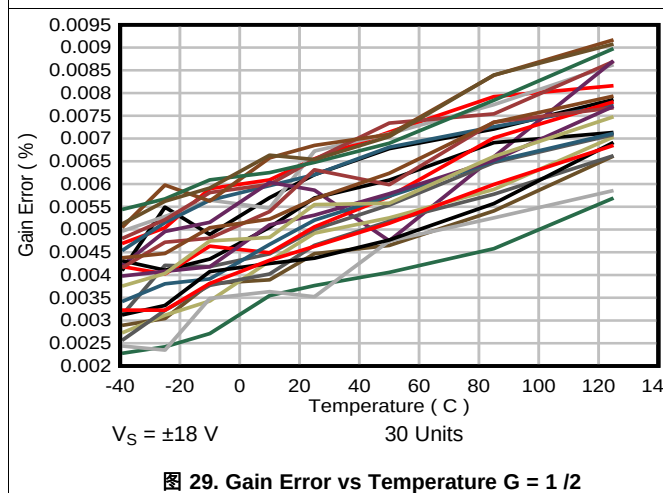


图 29. Gain Error vs Temperature G = 1/2

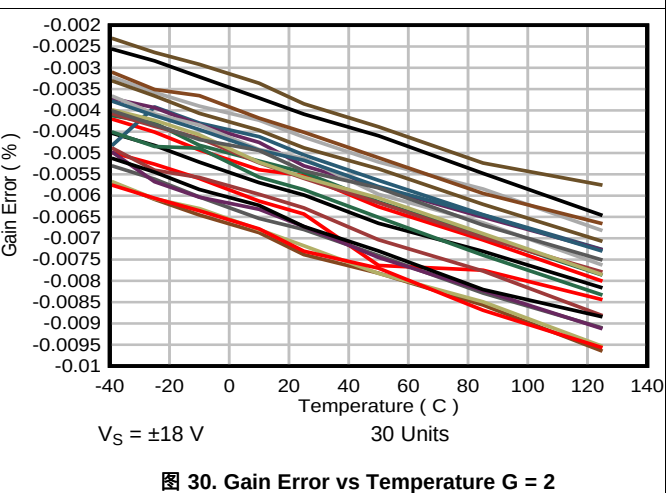
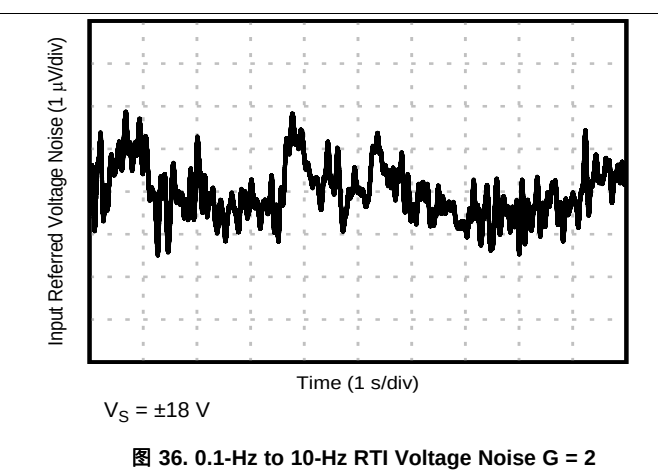
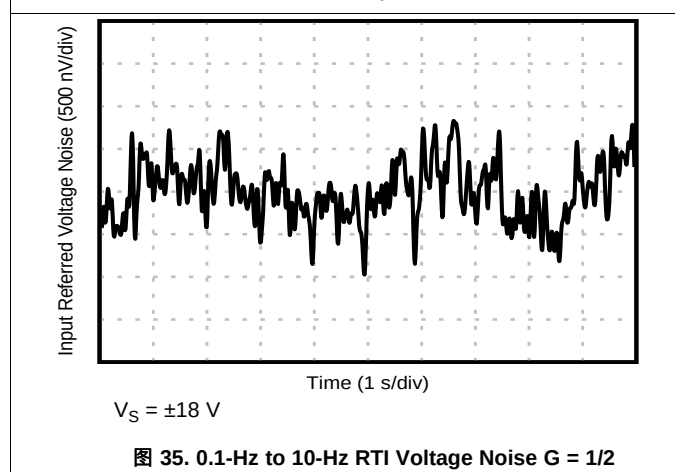
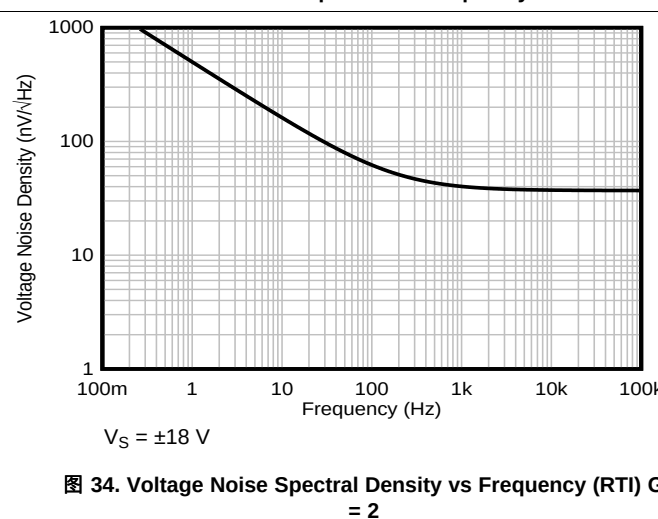
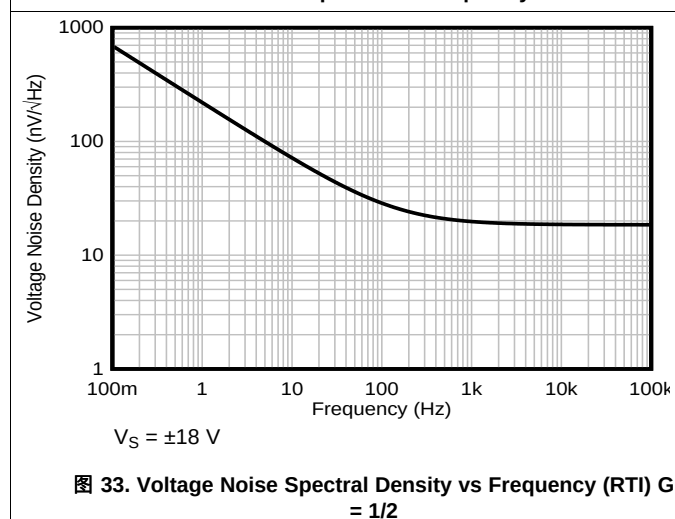
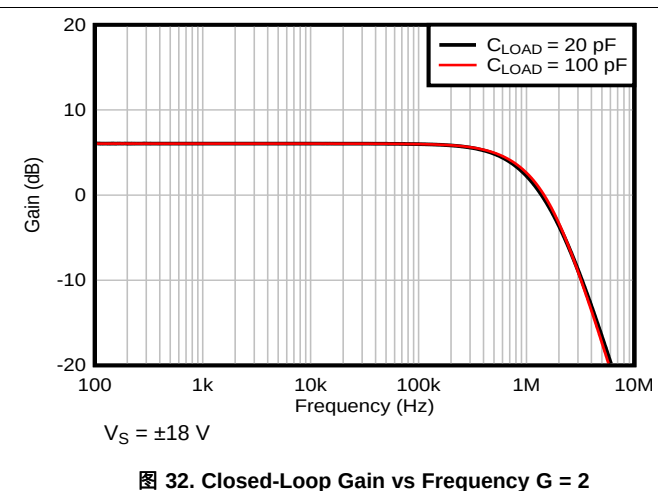
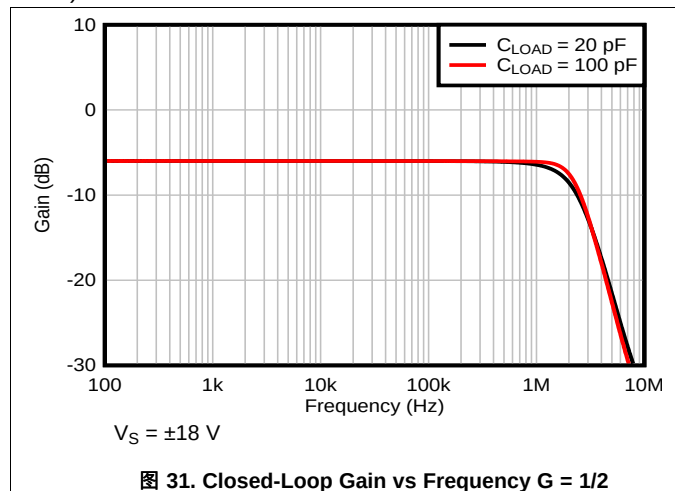


图 30. Gain Error vs Temperature G = 2

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).



Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

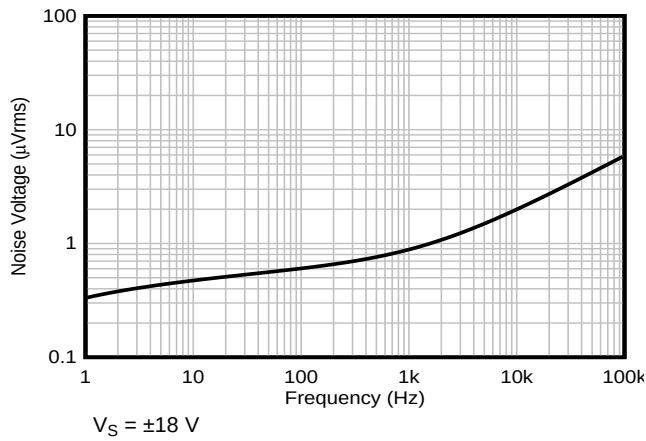


图 37. Integrated Output Voltage Noise vs Noise Bandwidth
 $G = 1/2$

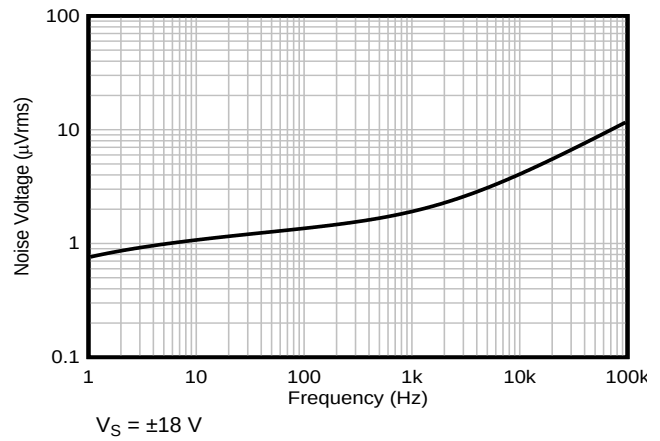


图 38. Integrated Output Voltage Noise vs Noise Bandwidth
 $G = 2$

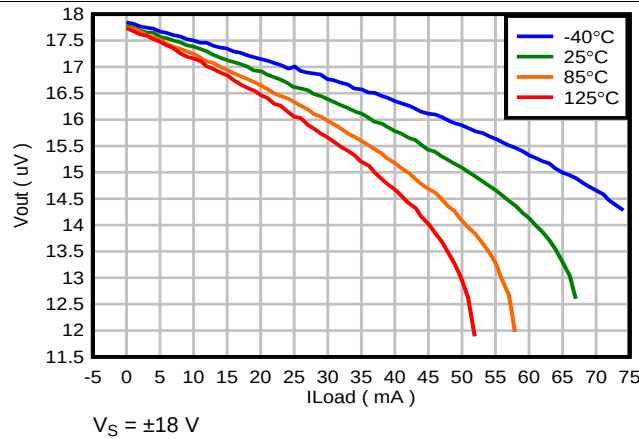


图 39. Positive Output Voltage vs Output Current (sourcing)
 $G = 1/2$

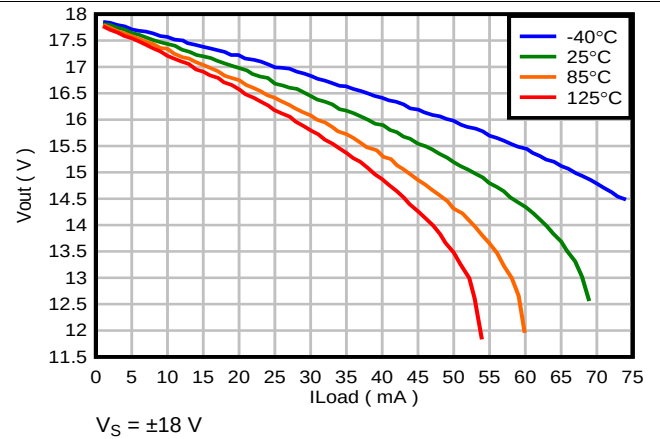


图 40. Positive Output Voltage vs Output Current (sourcing)
 $G = 2$

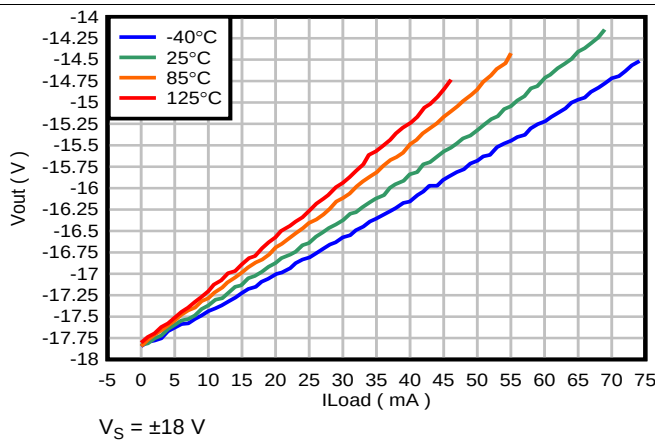


图 41. Negative Output Voltage vs Output Current (sinking)
 $G = 1/2$

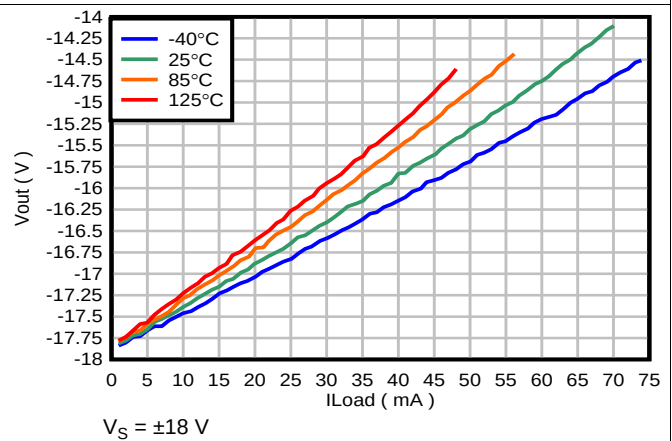
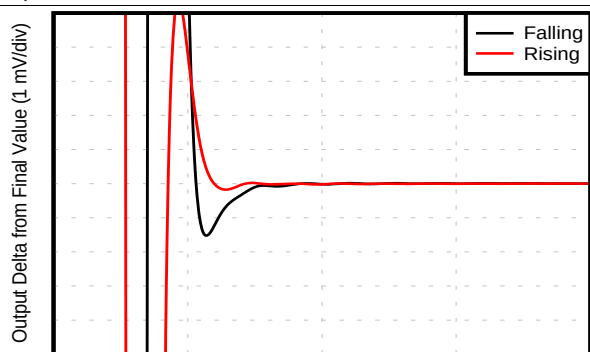


图 42. Negative Output Voltage vs Output Current (sinking)
 $G = 2$

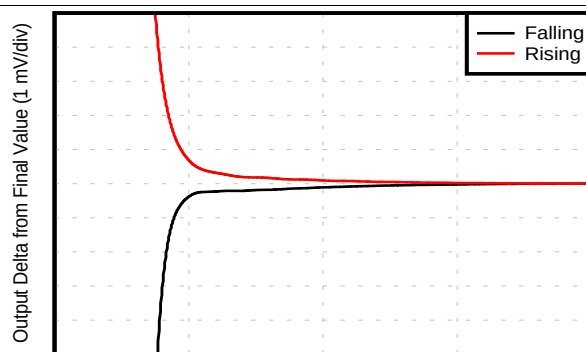
Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).



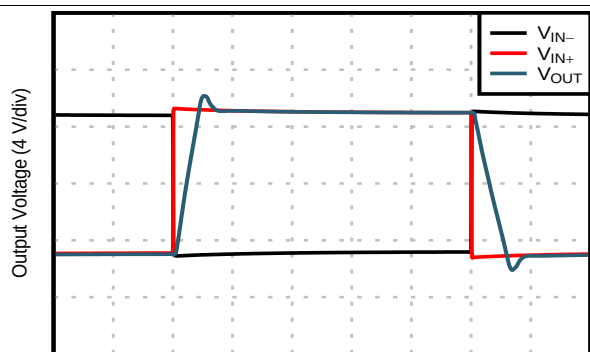
$V_S = \pm 18\text{ V}$

图 43. Settling Time $G = 1/2$



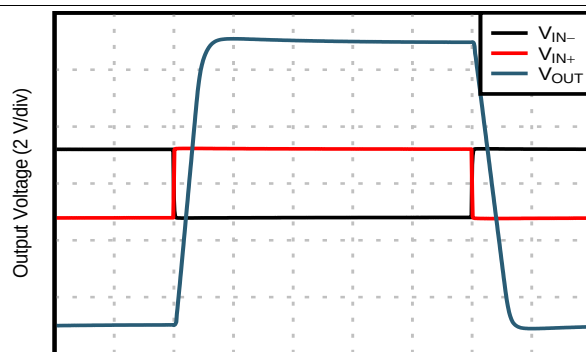
$V_S = \pm 18\text{ V}$

图 44. Settling Time $G = 2$



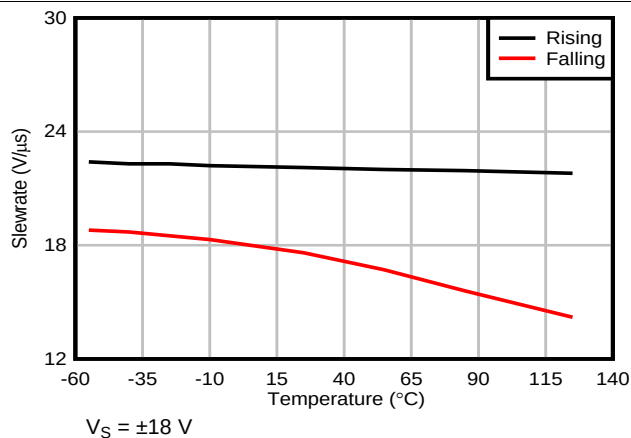
$V_S = \pm 18\text{ V}$

图 45. Large Signal Step Response $G = 1/2$



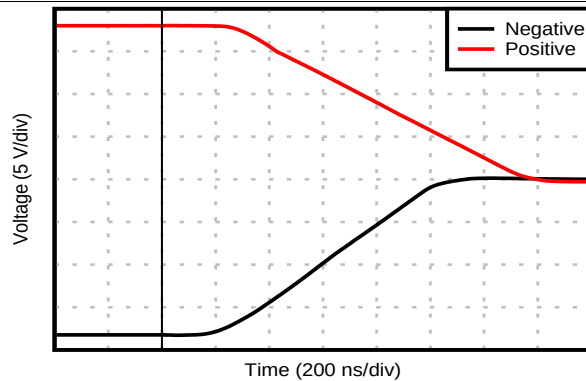
$V_S = \pm 18\text{ V}$

图 46. Large Signal Step Response $G = 2$



$V_S = \pm 18\text{ V}$

图 47. Slew Rate over Temperature

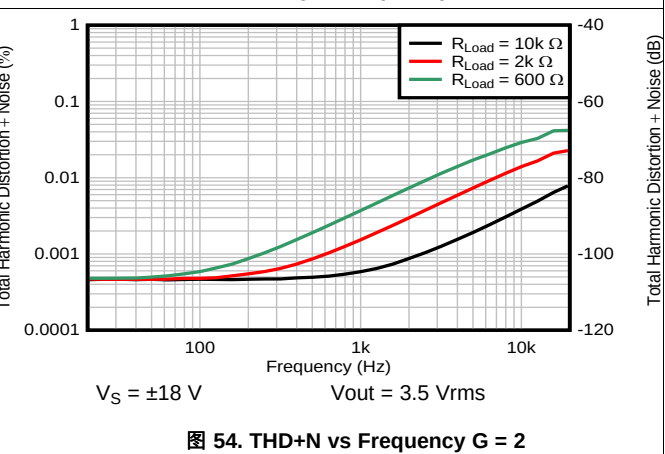
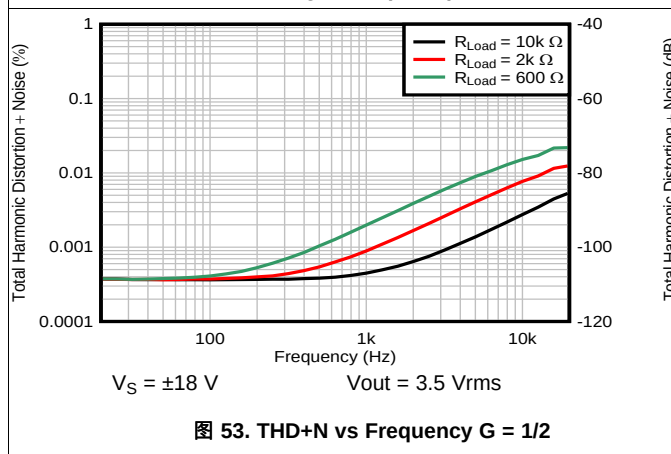
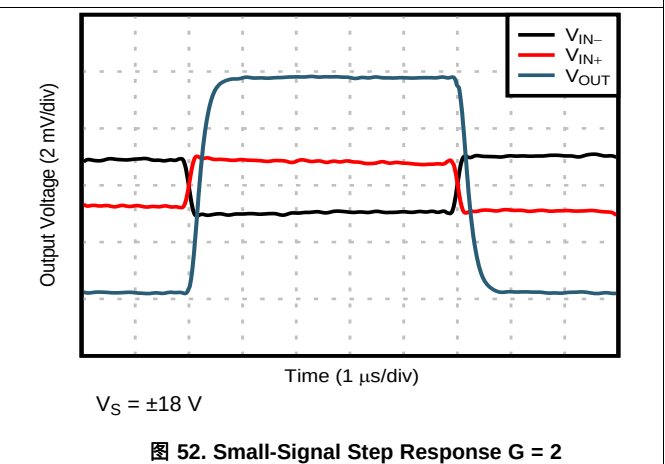
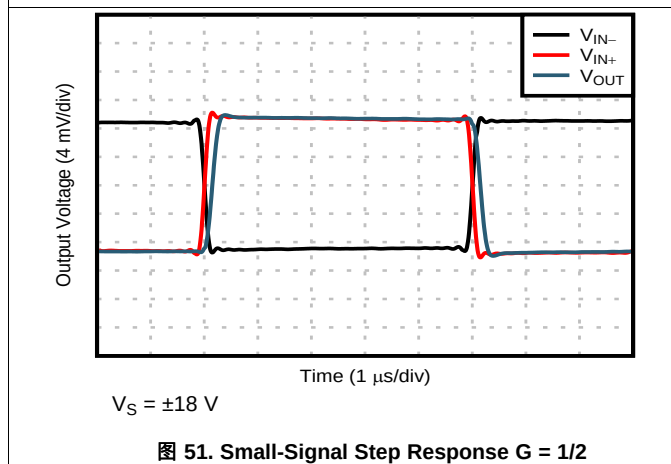
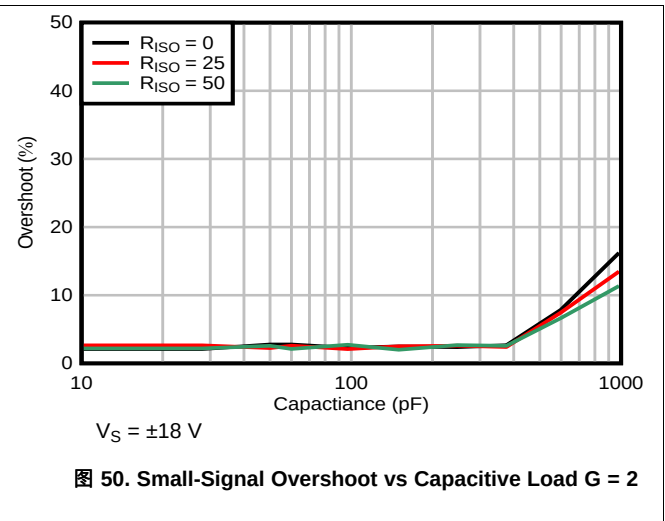
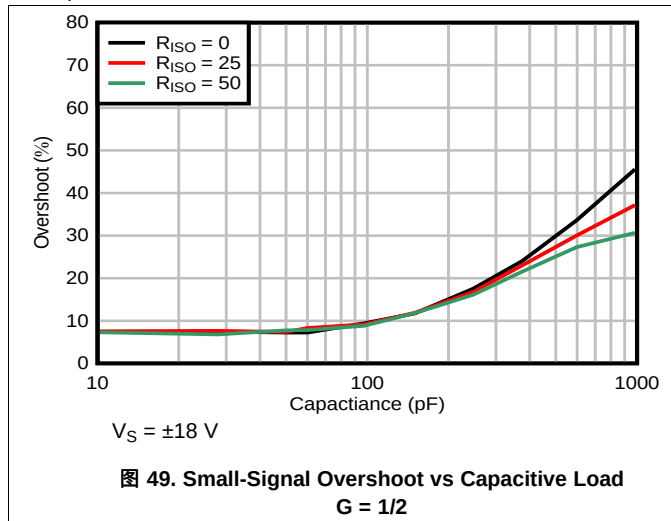


$V_S = \pm 18\text{ V}$

图 48. Overload Recovery (Normalized to 0 V)

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).



Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

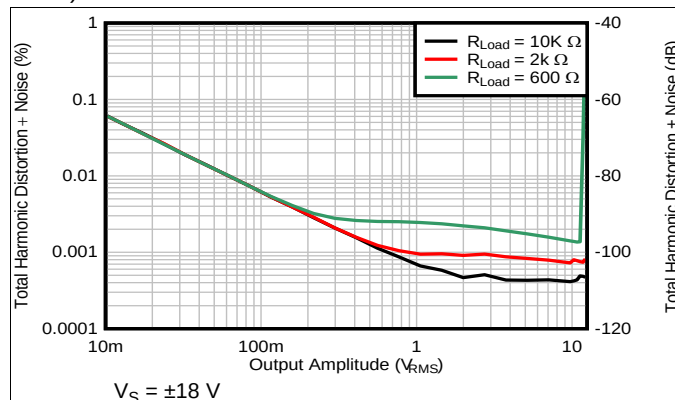


图 55. THD+N Ratio vs Output Amplitude $G = 1/2$

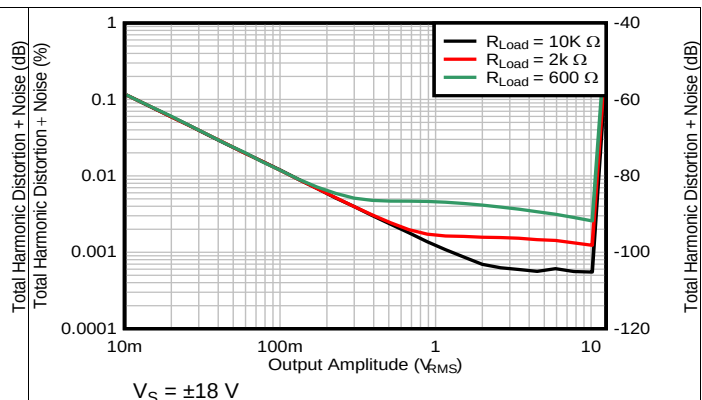


图 56. THD+N Ratio vs Output Amplitude $G = 2$

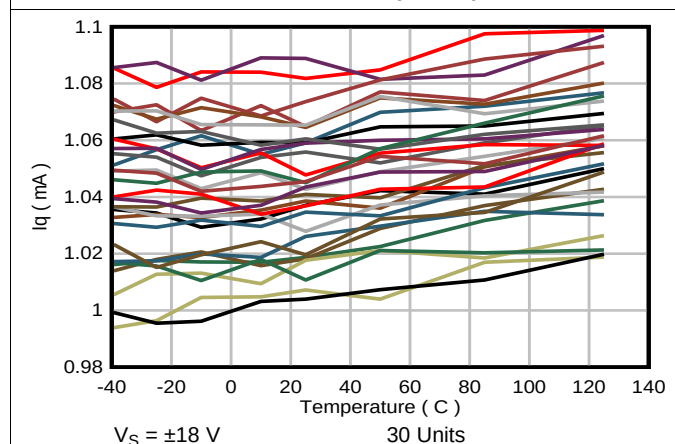


图 57. Supply Current vs Temperature $G = 1/2$

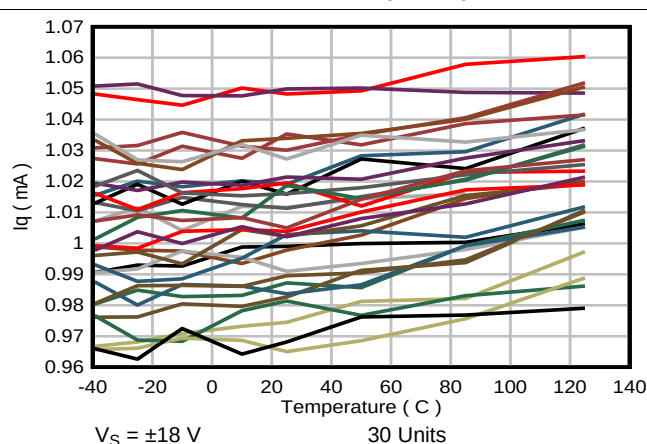


图 58. Supply Current vs Temperature $G = 2$

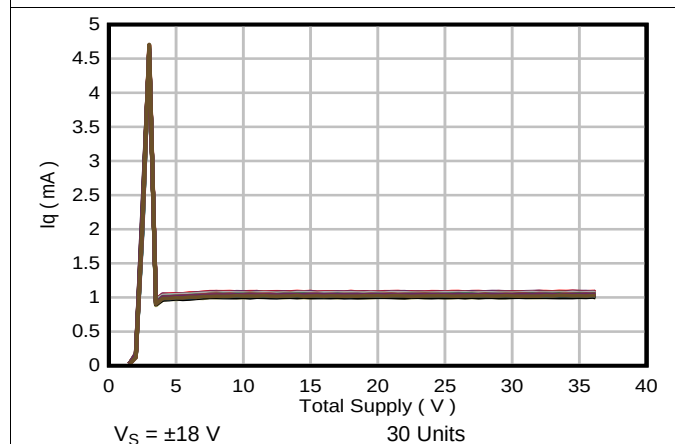


图 59. Supply Current vs Supply Voltage $G = 1/2$

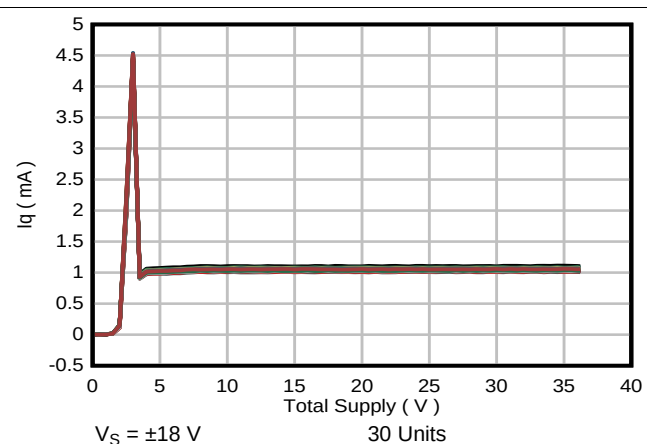
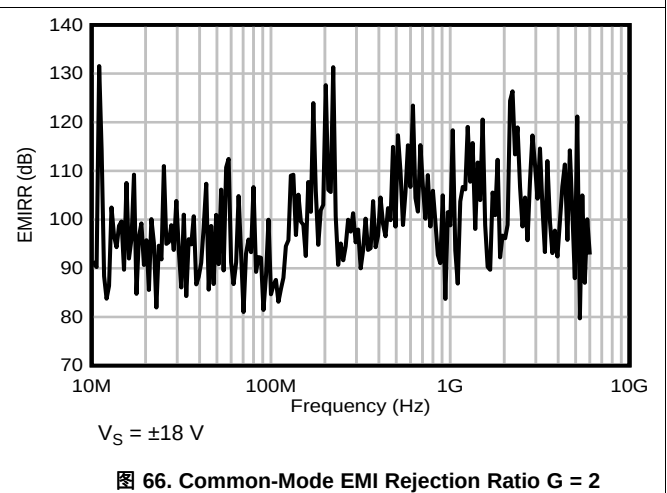
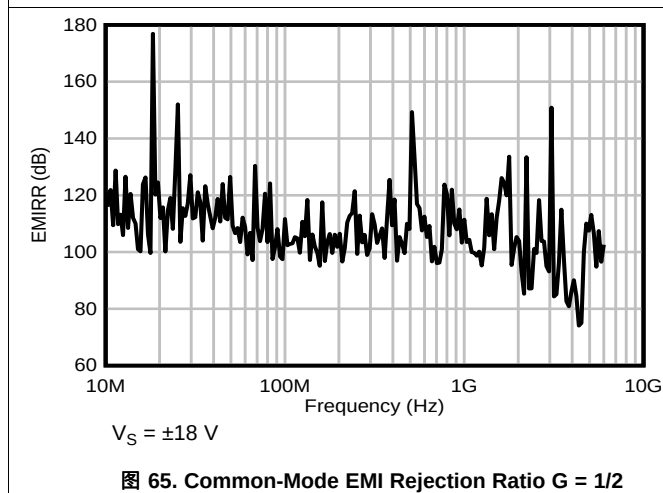
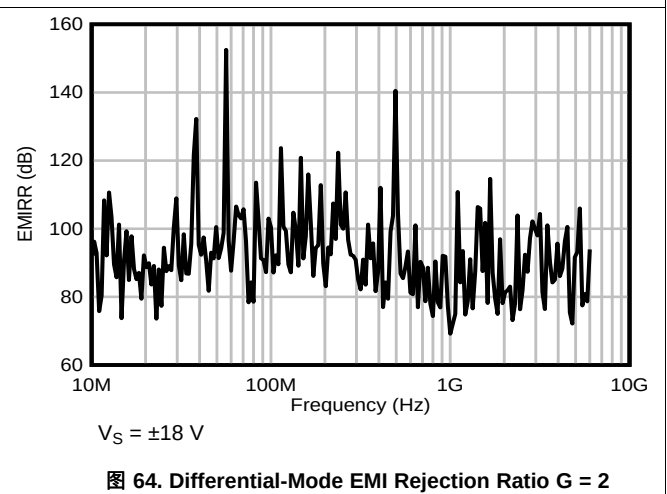
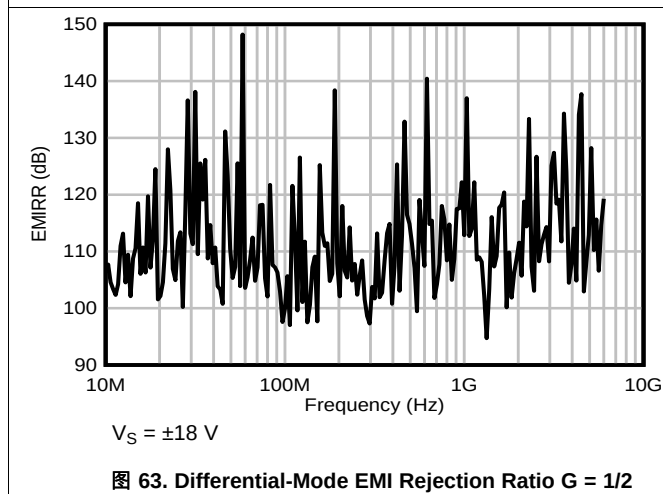
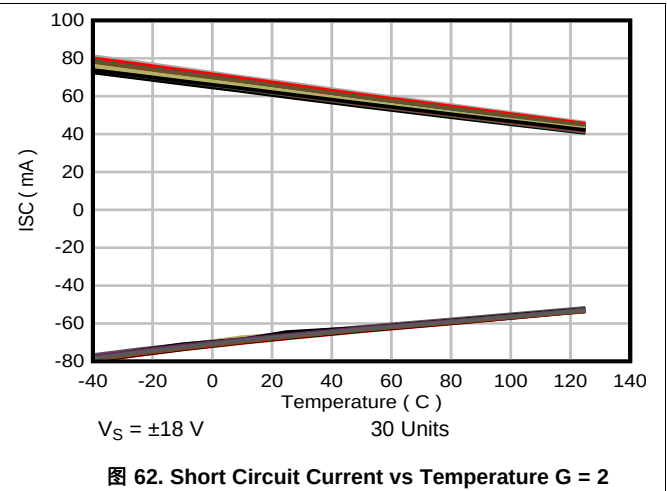
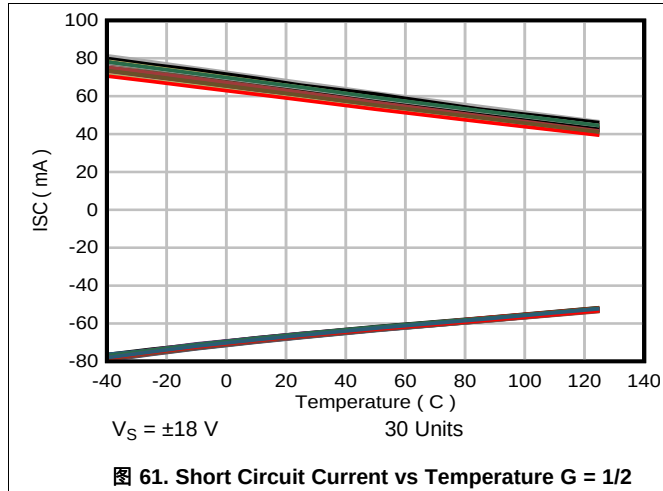


图 60. Supply Current vs Supply Voltage $G = 2$

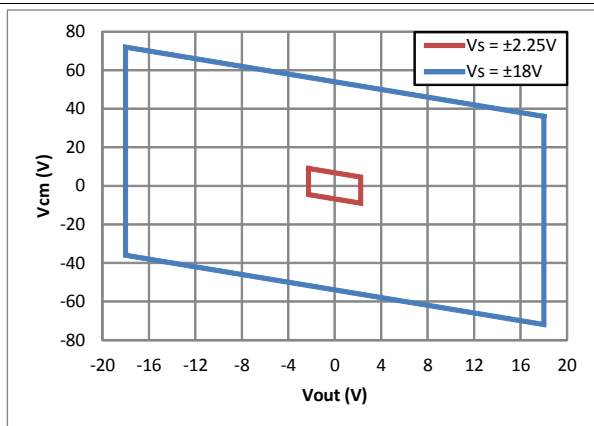
Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).



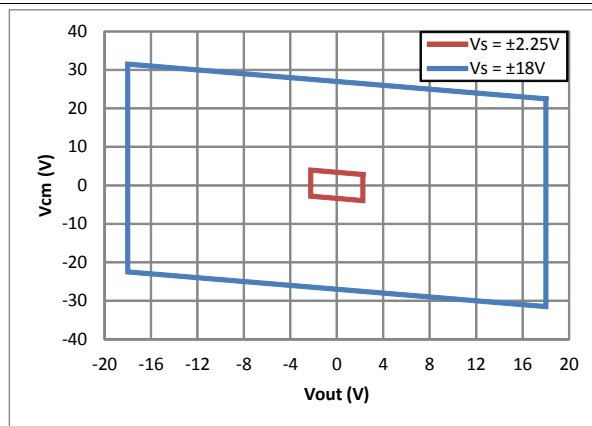
Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).



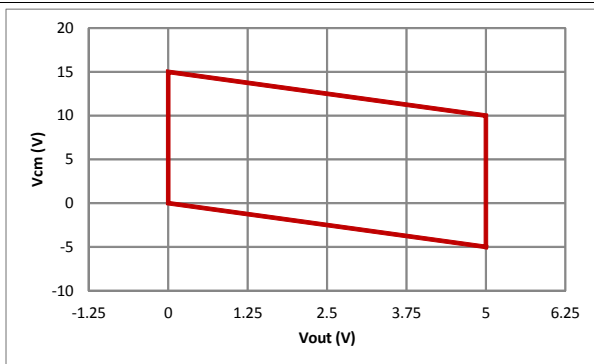
Vref = 0 V

图 67. Input Common-Mode Voltage vs Output Voltage $G = 1/2$, Bipolar Supply



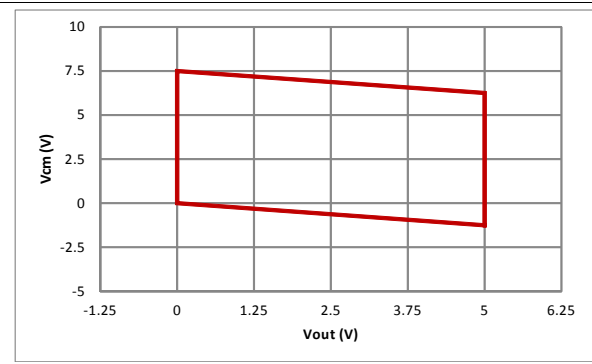
Vref = 0 V

图 68. Input Common-Mode Voltage vs Output Voltage $G = 2$, Bipolar Supply



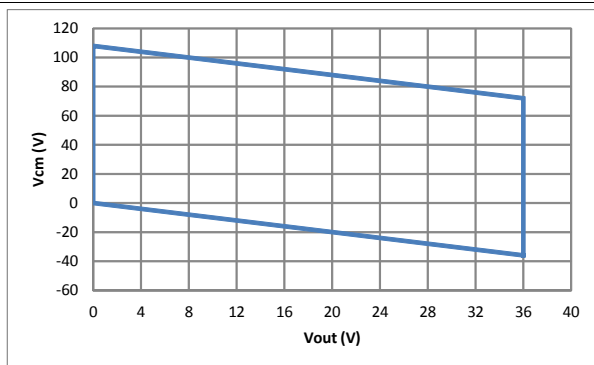
Vref = 0 V

图 69. Input Common-Mode Voltage vs Output Voltage $G = 1/2$, 5V Supply



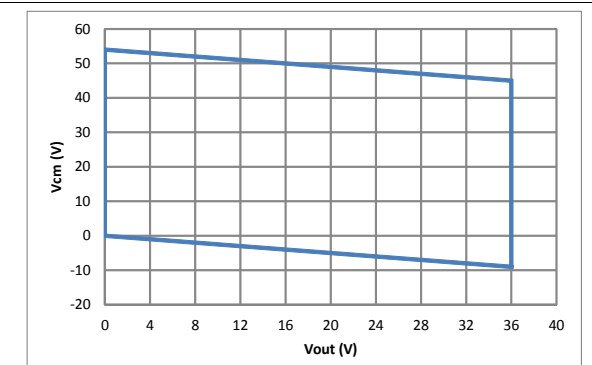
Vref = 0 V

图 70. Input Common-Mode Voltage vs Output Voltage $G = 2$, 5V Supply



Vref = 0 V

图 71. Input Common-Mode Voltage vs Output Voltage $G = 1/2$, 36V Supply



Vref = 0 V

图 72. Input Common-Mode Voltage vs Output Voltage $G = 2$, 36V Supply

INA592

ZHCSY1A –OCTOBER 2018–REVISED DECEMBER 2018

www.ti.com.cn

Typical Characteristics (接下页)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$, REF pin connected to ground and $G = 1/2$ (unless otherwise noted).

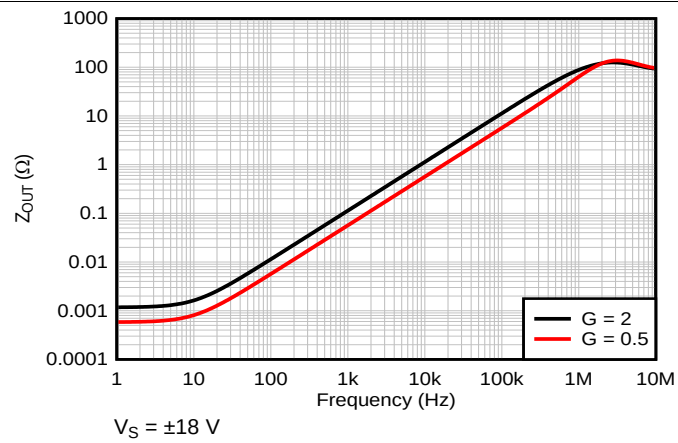


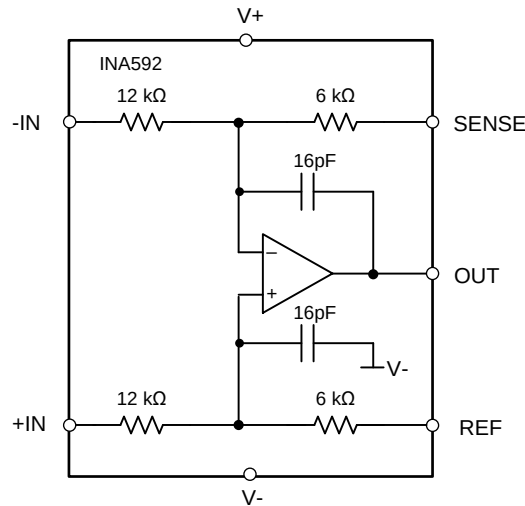
图 73. Closed-Loop Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The INA592 consists of a high precision, e-trim™ op amp and four trimmed resistors. These resistors can be connected to make a wide variety of amplifier configurations, including difference, noninverting, and inverting configurations. Using the on-chip resistors of the INA592 provides the designer with several advantages over a discrete design. Note that the INA592 includes internal compensation capacitors as shown in [Functional Block Diagram](#).

8.2 Functional Block Diagram



8.3 Feature Description

Much of the dc performance of op amp circuits depends on the accuracy of the surrounding resistors. The resistors on the INA592 are laid out to be tightly matched. The resistors of each part are matched on-chip and tested for their matching accuracy. Because of this trimming and testing, the INA592 can provide high accuracy for specifications such as gain drift, common-mode rejection, and gain error.

8.4 Device Functional Modes

The INA592 can measure voltages beyond the rails. For the $G = \frac{1}{2}$ and $G = 2$ difference amplifier configurations, see the input voltage range in [Specifications](#) for details. The INA592 can be configured in several ways; see [Figure 77](#) to [Figure 81](#). Because these configurations rely on the internal, matched resistors, all of these configurations have excellent gain accuracy and gain drift.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

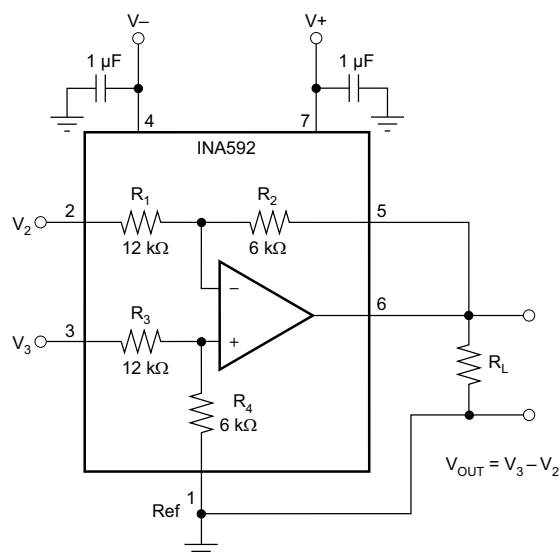
9.1 Application Information

图 74 shows the basic connections required for operation of the INA592. Connect power supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. The source impedances connected to the inputs must be nearly equal to provide good common-mode rejection. An 8-Ohms mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 80 dB. Gain accuracy is also slightly affected. If the source has a known impedance mismatch, an additional resistor in series with one input can be used to preserve good common-mode rejection.

As shown in 图 74, sense measurements at the load.

9.2 Typical Application



Copyright © 2018, Texas Instruments Incorporated

图 74. Basic Power Supply and Signal Connections

9.2.1 Design Requirements

For the application shown in 图 74, the design requirements are:

- Gain of $G = \frac{1}{2}$
- Offset of output voltage $V_{out_{OS}} = 0V$

Typical Application (接下页)

9.2.2 Detailed Design Procedure

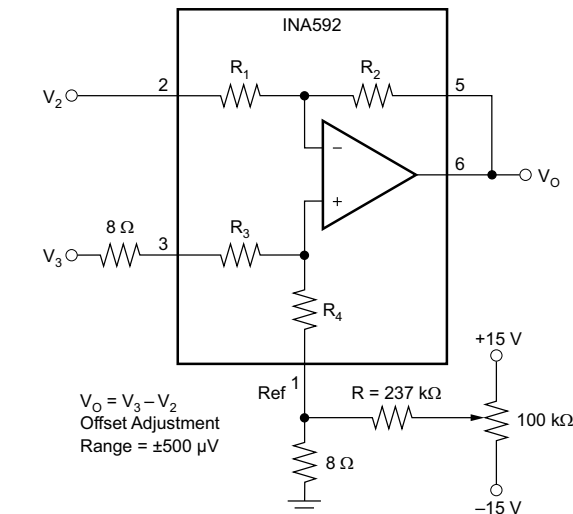
9.2.2.1 Operating Voltage

The INA592 operates from single (4.5 V to 36 V) or dual (± 2.25 V to ± 18 V) supplies with excellent performance. Specifications are production tested with +5-V and ± 15 -V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves. The internal op amp in the INA592 is a single-supply design. This allows linear operation with the op amp's common-mode voltage equal to, or slightly below V^- (or single supply ground). Although input voltages on pins 2 and 3 that are below the negative supply voltage do not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal below the negative supply can cause a positive feedback condition that could lock the device output to the negative rail.

The INA592 can accurately measure differential signals that are above the positive power supply. For example in $G = \frac{1}{2}$, the linear common-mode range extends to nearly three times the positive power supply voltage — see typical performance curves as well as [Input Voltage Range](#).

9.2.2.2 Offset Voltage Trim

The INA592 is production trimmed for low offset voltage and drift. Most applications require no external offset adjustment. 图 75 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the REF terminal is summed with the output signal. This can be used to null offset voltage. The source impedance of a signal applied to the REF terminal should be less than 8 Ohms to maintain good common-mode rejection. For low impedance at the REF terminal, the trim voltage can be buffered with an op amp, such as the OPA177.



NOTE: For $\pm 750 \mu V$ range, $R = 158 k\Omega$.

Copyright © 2017, Texas Instruments Incorporated

图 75. Offset Adjustment

9.2.2.3 Input Voltage Range

The INA592 is able to measure input voltages beyond the supply rails. The internal resistors divide down the voltage before it reaches the internal op amp and provide protection to the op amp inputs. 图 76 shows an example of how the voltage division works in a difference amplifier configuration. For the INA592 to measure correctly, the input voltages at the input nodes of the internal op amp must stay below 0.1 V of the positive supply rail and can exceed the negative supply rail by 0.1 V. Refer to the [Power Supply Recommendations](#) section for more details.

Typical Application (接下页)

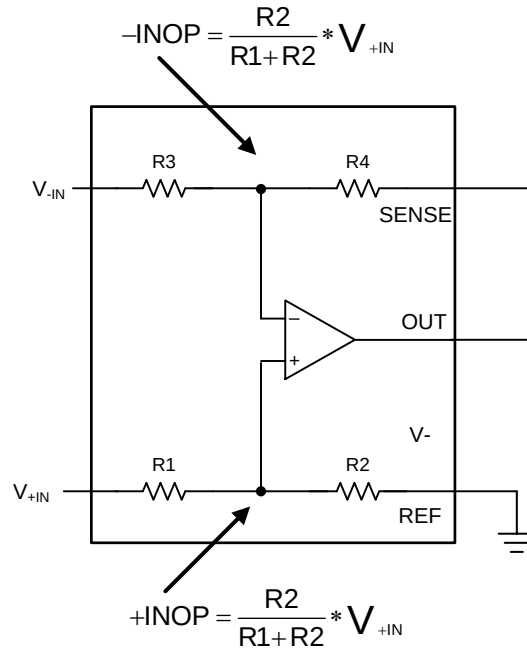


图 76. Voltage Division in the Difference Amplifier Configuration

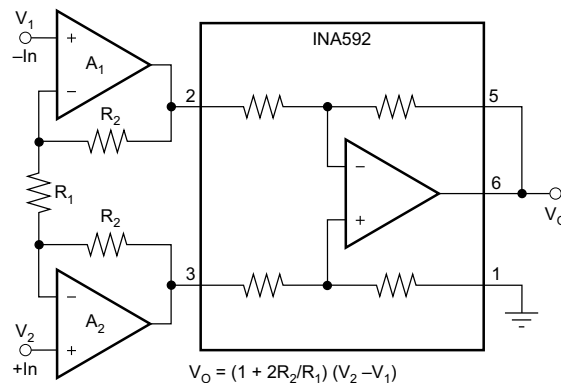
The INA592 has integrated ESD diodes at the inputs that provide overvoltage protection. This feature simplifies system design by eliminating the need for additional external protection circuitry, and enables a more robust system. The voltages at any of the inputs of the parts in $G = \frac{1}{2}$ configuration with ± 18 V supplies can safely range from $+V_S - 54$ V up to $-V_S + 54$ V. For example, on ± 10 V supplies, input voltages can go as high as ± 30 V.

9.2.2.4 Capacitive Load Drive Capability

The INA592 can drive large capacitive loads, even at low supplies. It is stable with a 500-pF load. Refer to the [Typical Characteristics](#).

9.2.2.5 Other Examples for Difference Amplifier Configurations

The INA592 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics, as shown in [图 77](#).



Copyright © 2017, Texas Instruments Incorporated

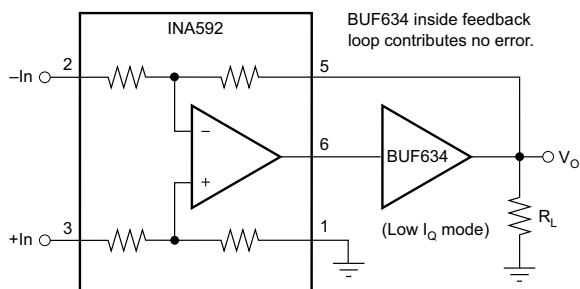
图 77. Precision Instrumentation Amplifier

Typical Application (接下页)

Texas Instruments offers many complete high-performance IAs. See 表 2 for some of the products with related performance.

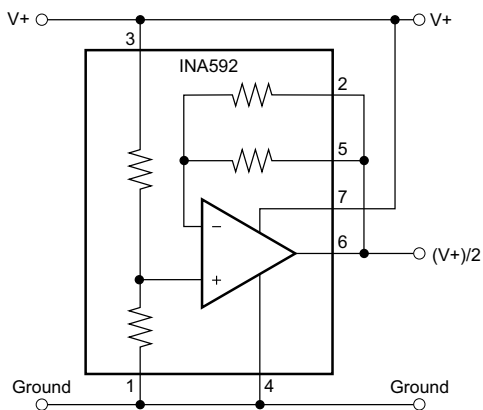
表 2. Recommendations for Op Amp Products to be Used Together With INA592

A1, A2	FEATURE	SIMILAR TI IA
OPA27	Low noise	INA103
OPA129	Ultra-low bias current (fA)	INA116
OPA177	Low offset drift, low noise	INA114, INA128
OPA2130	Low power, FET-input (pA)	INA111
OPA2234	Single supply, precision, low power	INA122, INA118
OPA2237	Single supply, low power, 8-pin MSOP	INA122, INA126



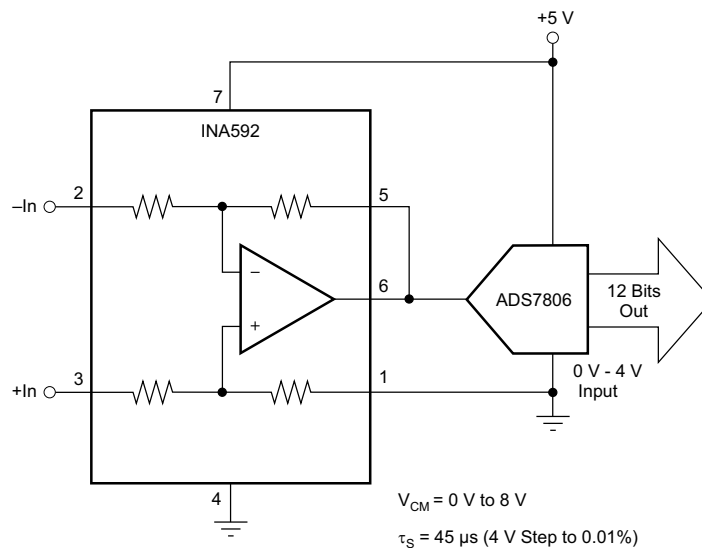
Copyright © 2017, Texas Instruments Incorporated

图 78. Low Power, High-Output Current Precision Difference Amplifier

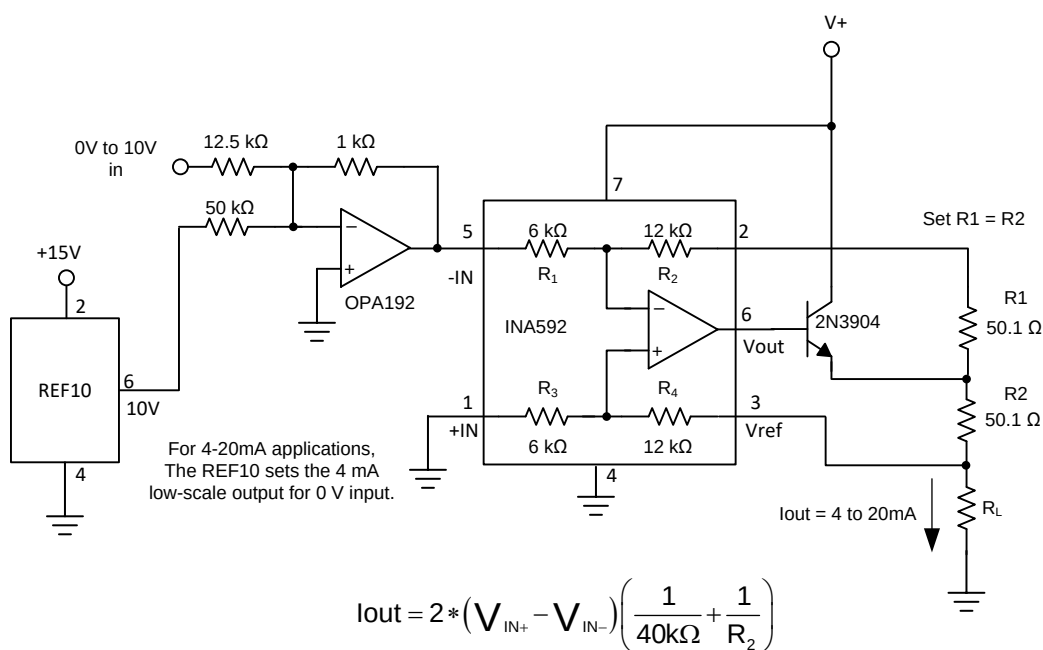


Copyright © 2017, Texas Instruments Incorporated

图 79. Pseudoground Generator



Copyright © 2017, Texas Instruments Incorporated

图 80. Differential Input Data Acquisition

图 81. Precision Voltage-to-Current Conversion

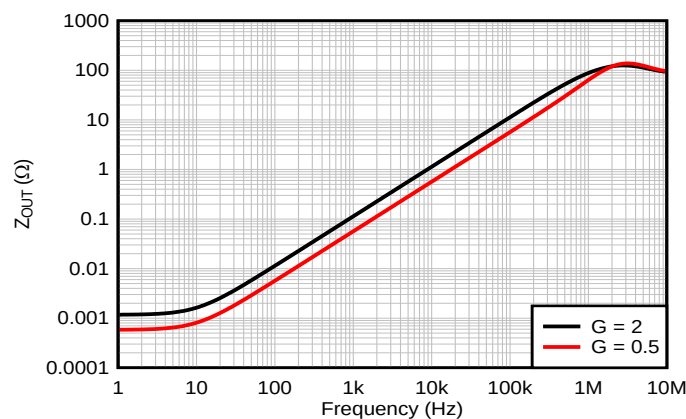
The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the [INA105](#) data sheet for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- $\pm 10\text{-V}$ Precision Voltage Reference
- $\pm 5\text{-V}$ Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision $G = 2$ Amplifier

- Precision Summing Amplifier
- Precision $G = 1/2$ Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low IOUT
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ± 1 Amplifier

9.2.3 Application Curve

The interaction between the output stage of an operational amplifier (op amp) and capacitive loads can impact the stability of the circuit. Throughout the industry, op-amp output-stage requirements have changed greatly since their original creation. Classic output stages with the class-AB common-emitter bipolar junction transistor (BJT) have now been replaced with common-collector BJT and common-drain complementary metal-oxide semiconductor (CMOS) devices. Both of these technologies enable rail-to-rail output voltages for single-supply and battery-powered applications. A result of changing these output-stage structures is that the op-amp open-loop output impedance (Z_o) changed from the largely resistive behavior of early BJT op amps to a frequency-dependent Z_o that features capacitive, resistive, and inductive portions. Proper understanding of Z_o over frequency - and also the resulting closed-loop output impedance over frequency - is crucial for the understanding of loop gain, bandwidth, and stability analysis. 图 82 shows the INA592 closed-loop output impedance and how it varies over frequency.



$$V_S = \pm 18 \text{ V}$$

图 82. Closed-Loop Output Impedance vs Frequency

10 Power Supply Recommendations

The nominal performance of the INA592 is specified with a supply voltage of $\pm 15 \text{ V}$ and midsupply reference voltage. The device operates using power supplies from $\pm 2.25 \text{ V}$ (4.5 V) to $\pm 18 \text{ V}$ (36 V) and non midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in [Typical Characteristics](#).

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

11.2 Layout Example

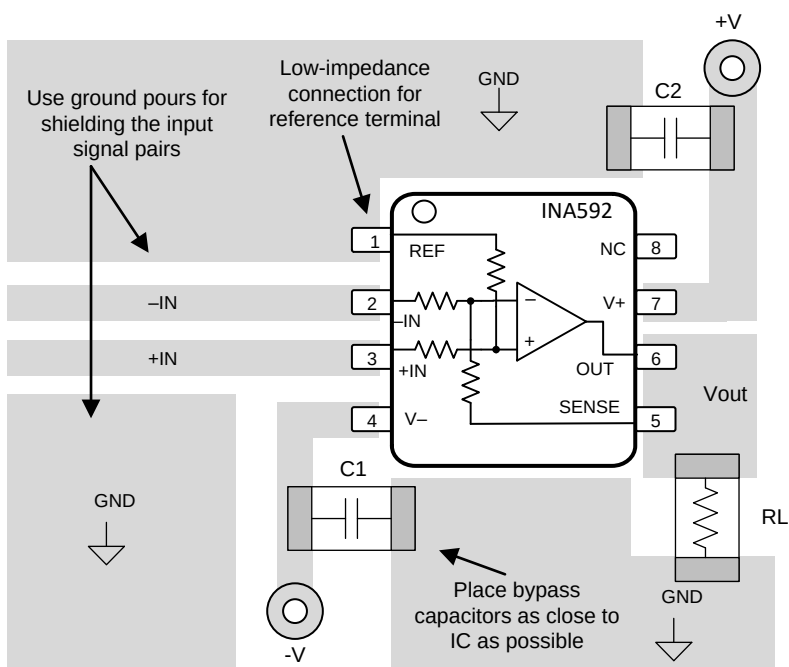
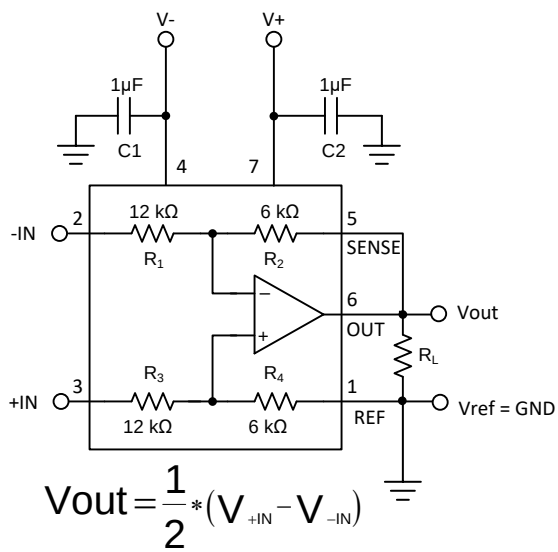


图 83. Example Schematic and Associated PCB Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 商标

e-trim, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA592IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OK6	Samples
INA592IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1OK6	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

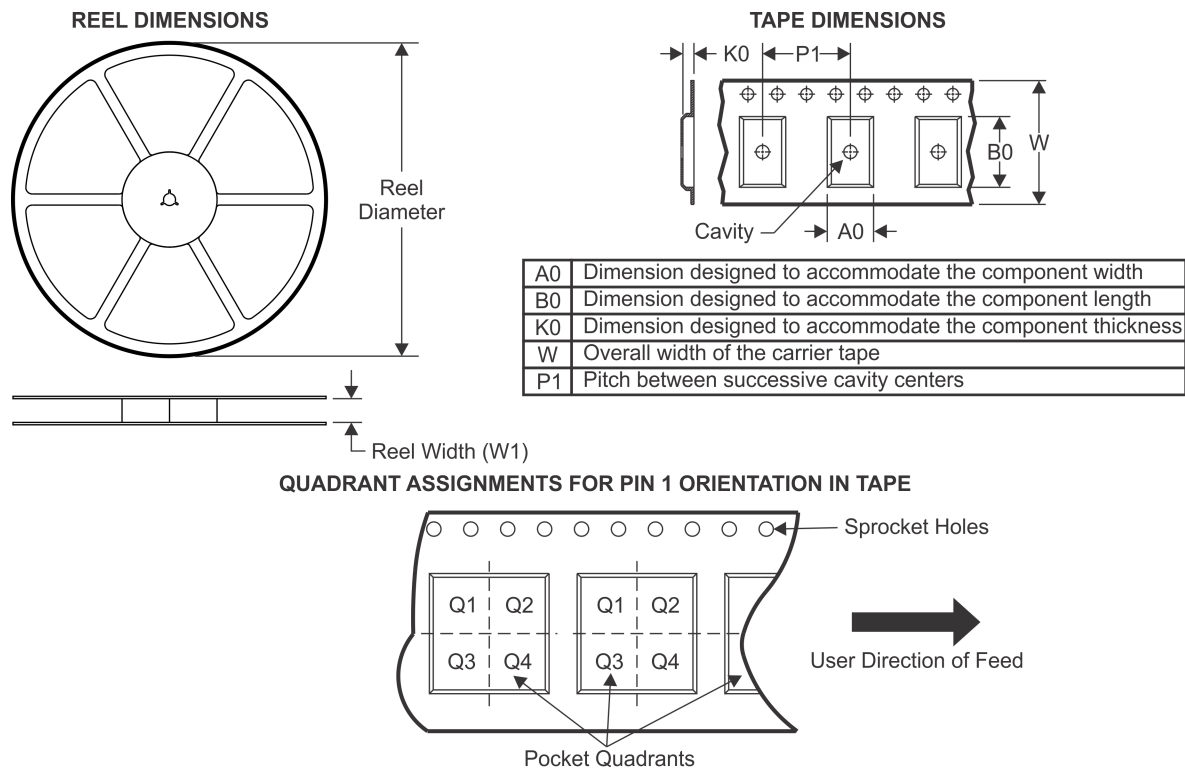
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

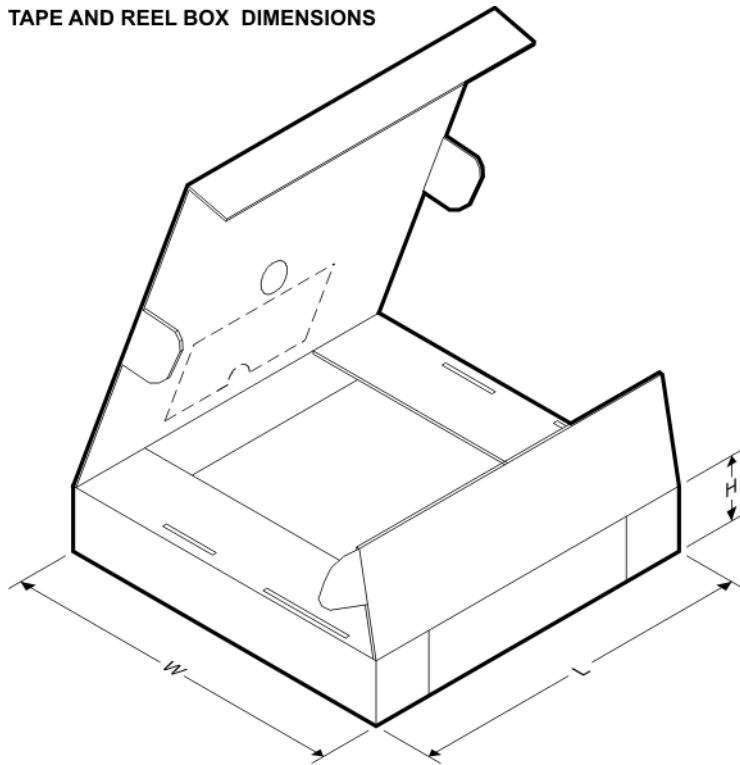
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA592IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA592IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

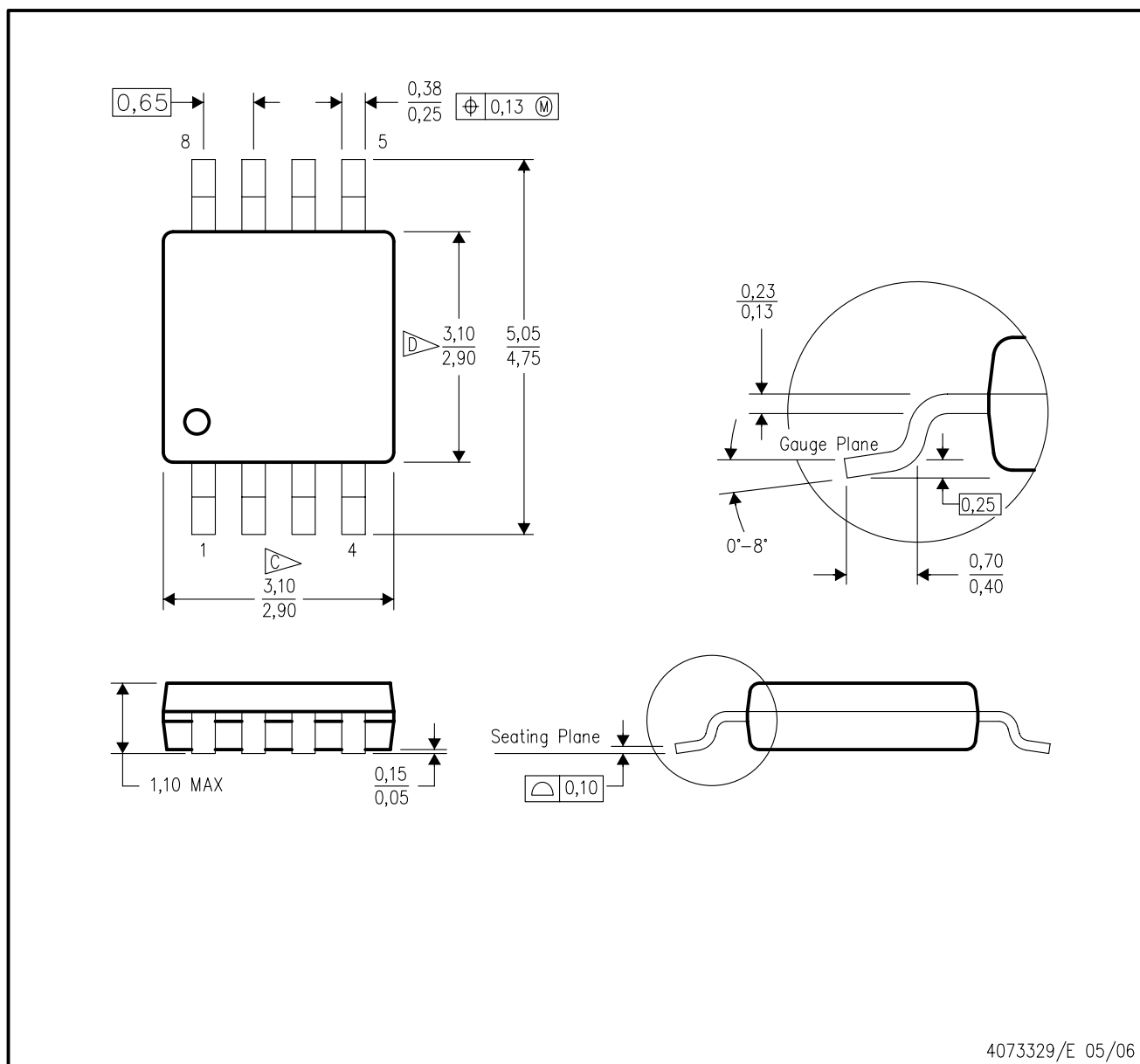


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA592IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA592IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

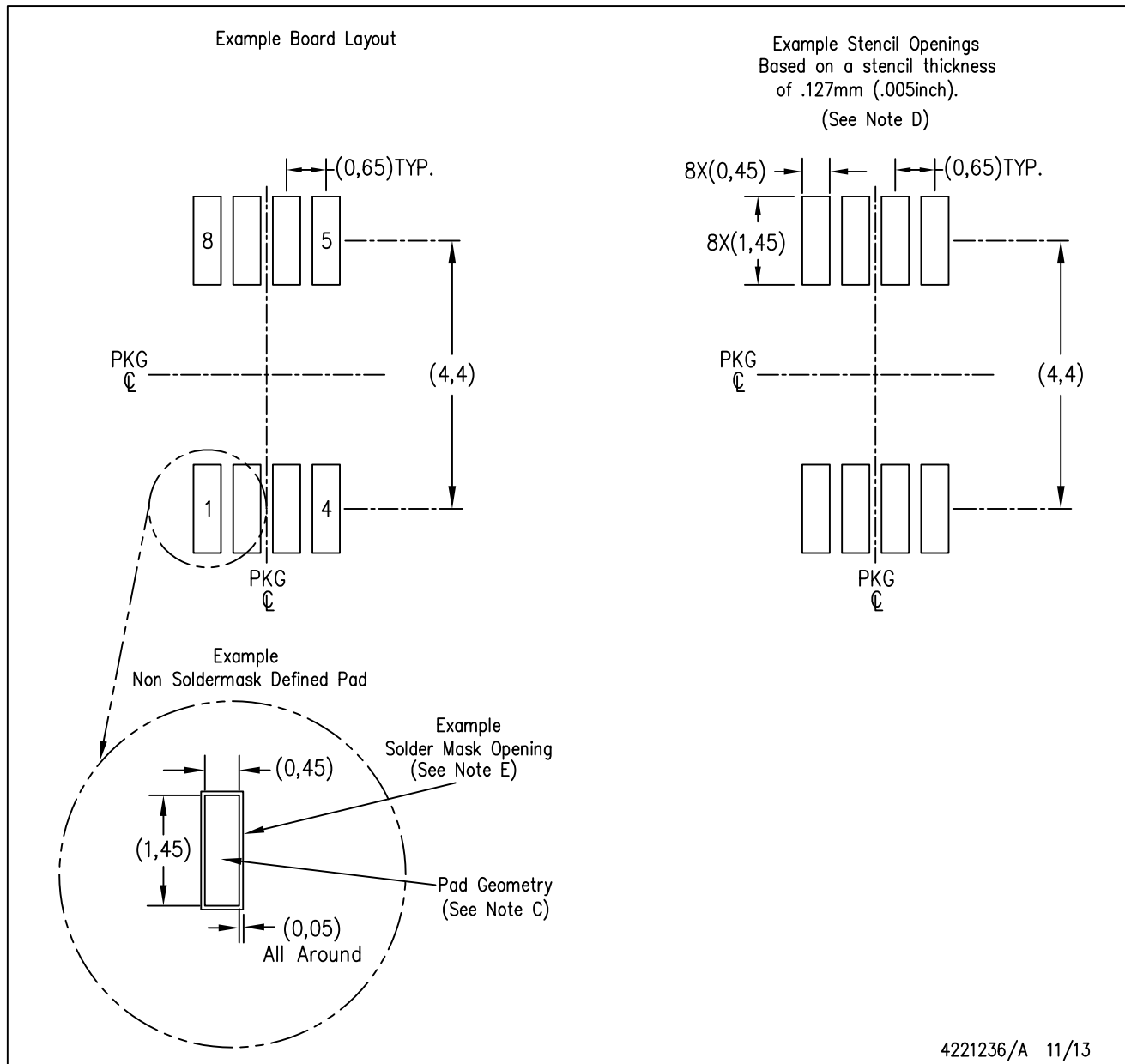


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司