# OPA858 5.5GHz 增益带宽积、7V/V 增益稳定型 FET 输入放大器

## 1 特性

- 高增益带宽积：5.5GHz
- 解补偿，增益 ≥ 7V/V（稳定）
- 超低偏置电流 MOSFET 输入：10pA
- 低输入电压噪声：2.5nV/√Hz
- 压摆率：2000V/µs
- 低输入电容：
  - 共模：0.6pF
  - 差动：0.2pF
- 宽输入共模范围：
  - 与正电源相差 1.4V
  - 包括负电源
- TIA 配置下的输出摆幅为 $2.5V_{PP}$
- 电源电压范围：3.3V 至 5.25V
- 静态电流：20.5mA
- 采用 8 引脚 WSON 封装
- 温度范围：–40 至 +125°C

## 2 应用

- 高速跨阻放大器
- 激光测距
- 激光雷达接收器
- 液位变送器（光学）
- 光学时域反射法 (OTDR)
- 分布式温度检测
- 3D 扫描仪
- 飞行时间 (ToF) 系统
- 自主驾驶系统

## 3 说明

OPA858 是一款具有 CMOS 输入的低噪声运算放大器，适用于宽带跨阻和电压放大器 应用。当将该器件配置为跨阻放大器 (TIA) 时，5.5GHz 增益带宽积 (GBWP) 可为 需要 在数十至数百千欧范围内的跨阻增益下实现高闭环带宽的应用提供支持。

下图展示了当将 OPA858 配置为 TIA 时，该放大器的带宽和噪声性能与光电二极管电容的函数关系。计算总噪声时所依据的带宽范围为：从直流到左轴上计算得出的 $f_{-3dB}$ 频率。OPA858 封装 具有 反馈引脚 (FB)，可简化输入和输出之间的反馈网络连接。

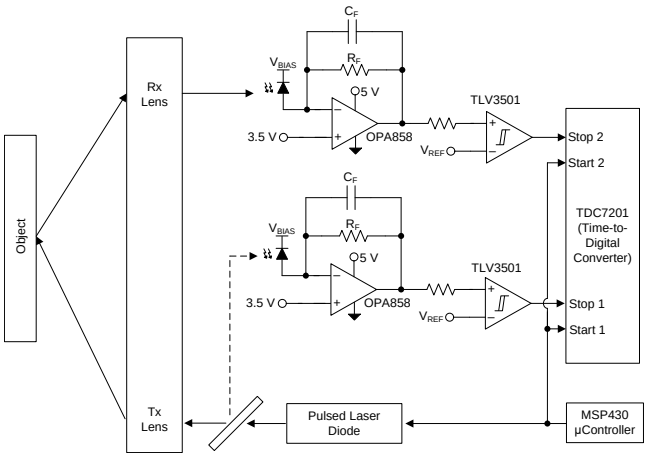
OPA858 经过优化，可用于光学飞行时间 (ToF) 系统，下图所示系统便是一个例子，其中 OPA858 是与 TDC7201 时数转换器搭配使用。OPA858 可搭配高速模数转换器 (ADC) 和用以驱动该 ADC 的差动输出放大器（如 THS4541 或 LMH5401），用于高分辨率激光雷达系统。

器件信息(1)

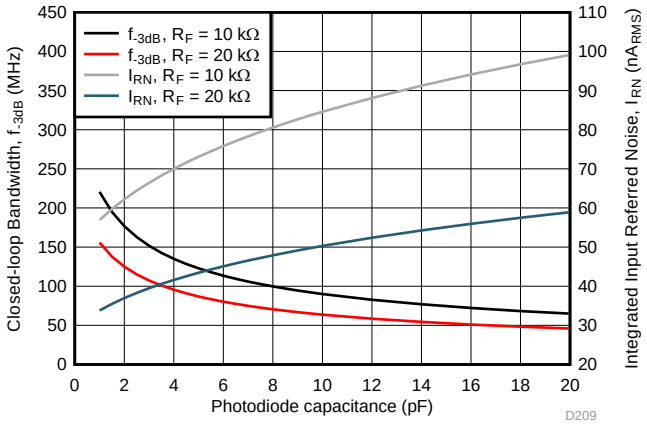
| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| OPA858 | WSON (8) | 2.00mm × 2.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

高速飞行时间接收器




光电二极管电容与带宽和噪声




本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Original (April 2018) to Revision A** **Page**

- 已更改 将器件状态从“预告信息”更改为“生产数据” ... 1

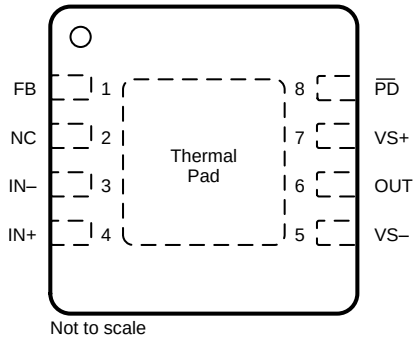

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# 5 Device Comparison Table

| DEVICE | INPUT TYPE | MINIMUM STABLE GAIN | VOLTAGE NOISE (nV/√Hz) | INPUT CAPACITANCE (pF) | GAIN BANDWIDTH (GHz) |
|---|---|---|---|---|---|
| OPA858 | CMOS | 7 V/V | 2.5 | 0.8 | 5.5 |
| OPA855 | Bipolar | 7 V/V | 0.98 | 0.8 | 8 |
| LMH6629 | Bipolar | 10 V/V | 0.69 | 5.7 | 4 |

# 6 Pin Configuration and Functions

**DSG Package**
**8-Pin WSON With Exposed Thermal Pad**
**Top View**




Not to scale

NC - no internal connection

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| FB | 1 | I | Feedback connection to output of amplifier |
| IN– | 3 | I | Inverting input |
| IN+ | 4 | I | Noninverting input |
| NC | 2 | — | Do not connect |
| OUT | 6 | O | Amplifier output |
| $\overline{PD}$ | 8 | I | Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation |
| VS– | 5 | — | Negative voltage supply |
| VS+ | 7 | — | Positive voltage supply |
| Thermal pad | | — | Connect the thermal pad to VS– |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Total supply voltage ($V_{S+}$ – $V_{S–}$) | | 5.5 | V |
| $V_{IN+}$, $V_{IN–}$ | Input voltage | ($V_{S–}$) – 0.5 | ($V_{S+}$) + 0.5 | |
| $V_{ID}$ | Differential input voltage | | 1 | |
| $V_{OUT}$ | Output voltage | ($V_{S–}$) – 0.5 | ($V_{S+}$) + 0.5 | |
| $I_{IN}$ | Continuous input current | | ±10 | mA |
| $I_{OUT}$ | Continuous output current(2) | | ±100 | |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_A$ | Operating free-air temperature | | 125 | |
| $T_{STG}$ | Storage temperature | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term continuous output current for electromigration limits.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Total supply voltage ($V_{S+}$ – $V_{S–}$) | 3.3 | 5 | 5.25 | V |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | OPA858 DSG (WSON) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 80.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 100 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 45 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 45.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 22.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 7.5 Electrical Characteristics

$V_{S+}$ = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, $R_F$ = 453 Ω, input common-mode biased at midsupply, $R_L$ = 200 Ω, output load is referenced to midsupply, and $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | | |
| SSBW | Small-signal bandwidth | $V_{OUT}$ = 100 $mV_{PP}$ | | 1.2 | | GHz | C |
| LSBW | Large-signal bandwidth | $V_{OUT}$ = 2 $V_{PP}$ | | 600 | | MHz | C |
| GBWP | Gain-bandwidth product | | | 5.5 | | GHz | C |
| | Bandwidth for 0.1-dB flatness | | | 130 | | MHz | C |
| SR | Slew rate (10% - 90%) | $V_{OUT}$ = 2-V step | | 2000 | | V/µs | C |
| $t_r$ | Rise time | $V_{OUT}$ = 100-mV step | | 0.3 | | ns | C |
| $t_f$ | Fall time | $V_{OUT}$ = 100-mV step | | 0.3 | | ns | C |
| | Settling time to 0.1% | $V_{OUT}$ = 2-V step | | 8 | | ns | C |
| | Settling time to 0.001% | $V_{OUT}$ = 2-V step | | 3000 | | ns | C |
| | Overshoot or undershoot | $V_{OUT}$ = 2-V step | | 7% | | | C |
| | Overdrive recovery | 2x output overdrive (0.1% recovery) | | 200 | | ns | C |
| HD2 | Second-order harmonic distortion | f = 10 MHz, $V_{OUT}$ = 2 $V_{PP}$ | | 88 | | dBc | C |
| | | f = 100 MHz, $V_{OUT}$ = 2 $V_{PP}$ | | 64 | | | |
| HD3 | Third-order harmonic distortion | f = 10 MHz, $V_{OUT}$ = 2 $V_{PP}$ | | 86 | | dBc | C |
| | | f = 100 MHz, $V_{OUT}$ = 2 $V_{PP}$ | | 68 | | | |
| $e_n$ | Input-referred voltage noise | f = 1 MHz | | 2.5 | | nV/√Hz | C |
| $Z_{OUT}$ | Closed-loop output impedance | f = 1 MHz | | 0.15 | | Ω | C |
| **DC PERFORMANCE** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | | 72 | 75 | | dB | A |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C | –5 | ±0.8 | 5 | mV | A |
| $\Delta V_{OS}/\Delta T$ | Input offset voltage drift | $T_A$ = –40°C to +125°C | | ±2 | | µV/°C | B |
| $I_{BN}$, $I_{BI}$ | Input bias current | $T_A$ = 25°C | | ±0.4 | 5 | pA | A |
| $I_{BOS}$ | Input offset current | $T_A$ = 25°C | | ±0.01 | 5 | pA | A |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = ±0.5 V, referenced to midsupply | 70 | 90 | | dB | A |
| **INPUT** | | | | | | | |
| | Common-mode input resistance | | | 1 | | GΩ | C |
| $C_{CM}$ | Common-mode input capacitance | | | 0.62 | | pF | C |
| | Differential input resistance | | | 1 | | GΩ | C |
| $C_{DIFF}$ | Differential input capacitance | | | 0.2 | | pF | C |
| $V_{IH}$ | Common-mode input range (high) | CMRR > 66 dB, $V_{S+}$ = 3.3 V | 1.7 | 1.9 | | V | A |
| $V_{IL}$ | Common-mode input range (low) | CMRR > 66 dB, $V_{S+}$ = 3.3 V | | 0 | 0.4 | V | A |
| $V_{IH}$ | Common-mode input range (high) | CMRR > 66 dB | 3.4 | 3.6 | | V | A |
| | | $T_A$ = –40°C to +125°C, CMRR > 66 dB | | 3.4 | | | B |
| $V_{IL}$ | Common-mode input range (low) | CMRR > 66 dB | | 0 | 0.4 | V | A |
| | | $T_A$ = –40°C to +125°C, CMRR > 66 dB | | 0.35 | | | B |
| **OUTPUT** | | | | | | | |
| $V_{OH}$ | Output voltage (high) | $T_A$ = 25°C, $V_{S+}$ = 3.3 V | 2.3 | 2.4 | | V | A |
| $V_{OH}$ | Output voltage (high) | $T_A$ = 25°C | 3.95 | 4.1 | | V | A |
| | | $T_A$ = –40°C to +125°C | | 3.9 | | | B |
| $V_{OL}$ | Output voltage (low) | $T_A$ = 25°C, $V_{S+}$ = 3.3 V | | 1.05 | 1.15 | V | A |

(1) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.

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## Electrical Characteristics (continued)

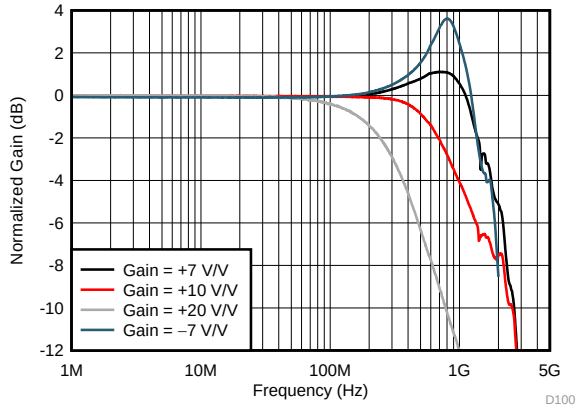
$V_{S+}$ = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, $R_F$ = 453 Ω, input common-mode biased at midsupply, $R_L$ = 200 Ω, output load is referenced to midsupply, and $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output voltage (low) | $T_A$ = 25°C | | 1.05 | 1.15 | V | A |
| | | $T_A$ = –40°C to +125°C | | 1.2 | | | B |
| | Linear output drive (sink and source) | $R_L$ = 10 Ω, $A_{OL}$ > 60 dB | 65 | 80 | | mA | A |
| | | $T_A$ = –40°C to +125°C, $R_L$ = 10 Ω, $A_{OL}$ > 60 dB | | 64 | | | B |
| $I_{SC}$ | Output short-circuit current | | 85 | 105 | | mA | A |
| **POWER SUPPLY** | | | | | | | |
| $V_S$ | Operating voltage | | 3.3 | | 5.25 | V | A |
| $I_Q$ | Quiescent current | $V_{S+}$ = 5 V | 18 | 20.5 | 24 | mA | A |
| $I_Q$ | Quiescent current | $V_{S+}$ = 3.3 V | 17.5 | 20 | 23.5 | mA | A |
| $I_Q$ | Quiescent current | $V_{S+}$ = 5.25 V | 18 | 21 | 24 | mA | A |
| $I_Q$ | Quiescent current | $T_A$ = 125°C | | 24.5 | | mA | B |
| $I_Q$ | Quiescent current | $T_A$ = –40°C | | 18.5 | | mA | B |
| PSRR+ | Positive power-supply rejection ratio | | 74 | 84 | | dB | A |
| PSRR– | Negative power-supply rejection ratio | | 70 | 80 | | | |
| **POWER DOWN** | | | | | | | |
| | Disable voltage threshold | Amplifier OFF below this voltage | 0.65 | 1 | | V | A |
| | Enable voltage threshold | Amplifier ON above this voltage | | 1.5 | 1.8 | V | A |
| | Power-down quiescent current | | | 70 | 140 | µA | A |
| | $\overline{PD}$ bias current | | | 70 | 200 | µA | A |
| | Turnon time delay | Time to $V_{OUT}$ = 90% of final value | | 13 | | ns | C |
| | Turnoff time delay | | | 120 | | ns | C |


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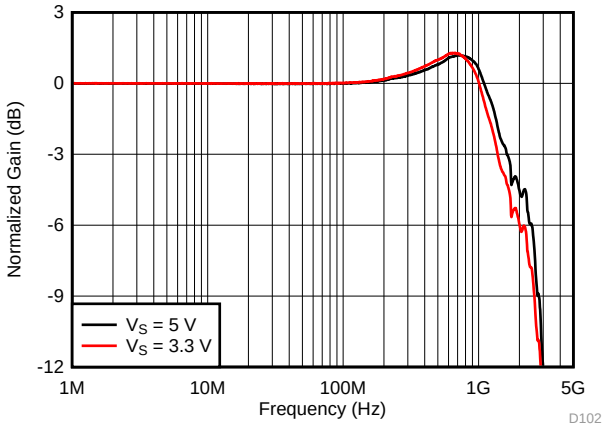
## 7.6 Typical Characteristics

$V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)



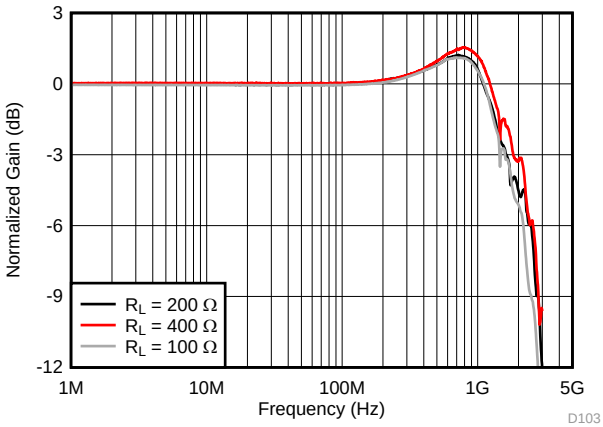

$V_{OUT}$ = 100 $mV_{PP}$; see 图 43 and 图 44 for circuit configuration

**图 1. Small-Signal Frequency Response vs Gain**



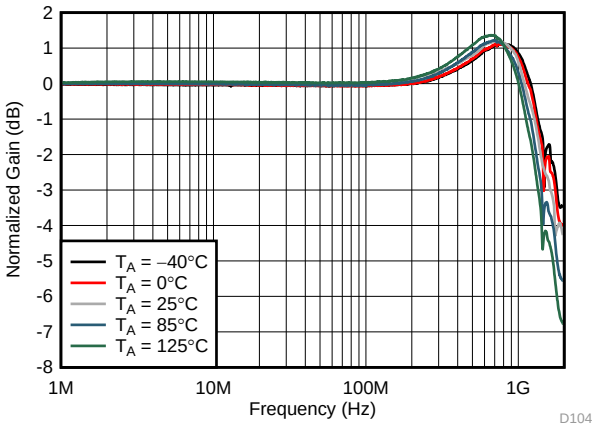

$V_{OUT}$ = 100 $mV_{PP}$

**图 2. Small-Signal Frequency Response vs Supply Voltage**



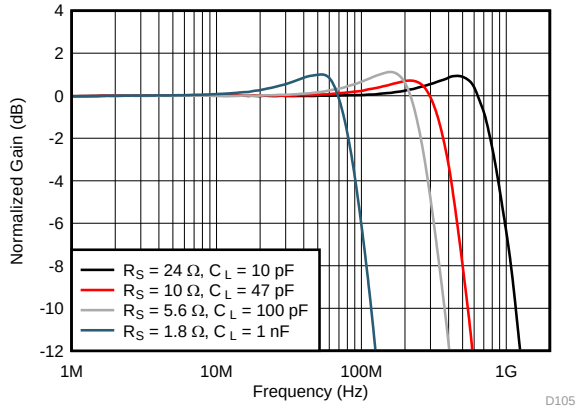

$V_{OUT}$ = 100 $mV_{PP}$

**图 3. Small-Signal Frequency Response vs Output Load**



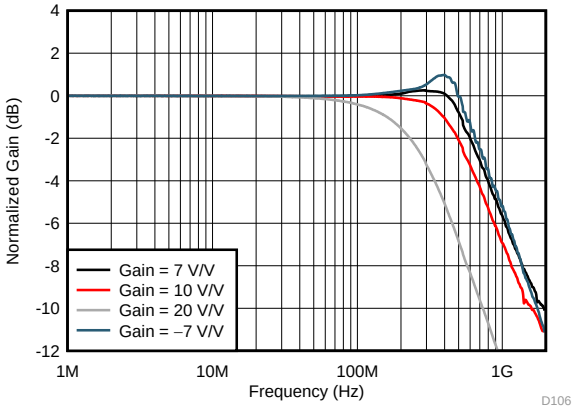

$V_{OUT}$ = 100 $mV_{PP}$

**图 4. Small-Signal Frequency Response vs Ambient Temperature**




$V_{OUT}$ = 100 $mV_{PP}$; see 图 45 for circuit configuration

**图 5. Small-Signal Frequency Response vs Capacitive Load**




$V_{OUT}$ = 2 $V_{PP}$

**图 6. Large-Signal Frequency Response vs Gain**

## Typical Characteristics（接下页）

$V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)

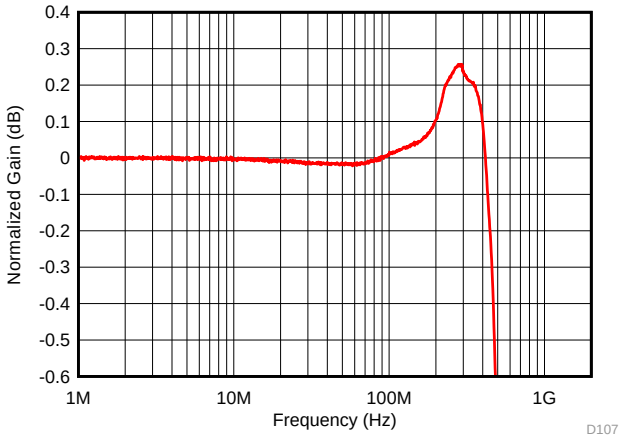



**图 7. Large-Signal Response for 0.1-dB Gain Flatness**

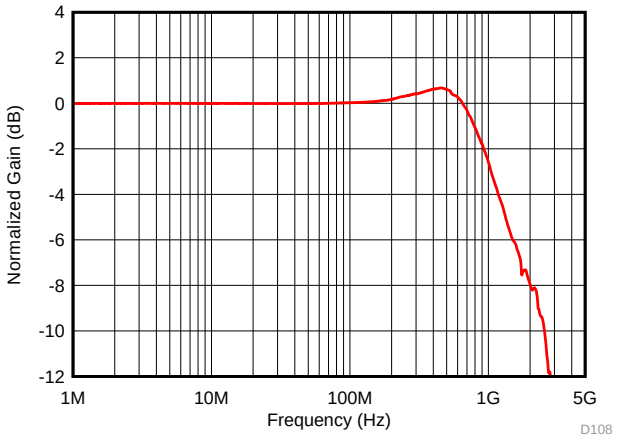



**图 8. Large-Signal Frequency Response**

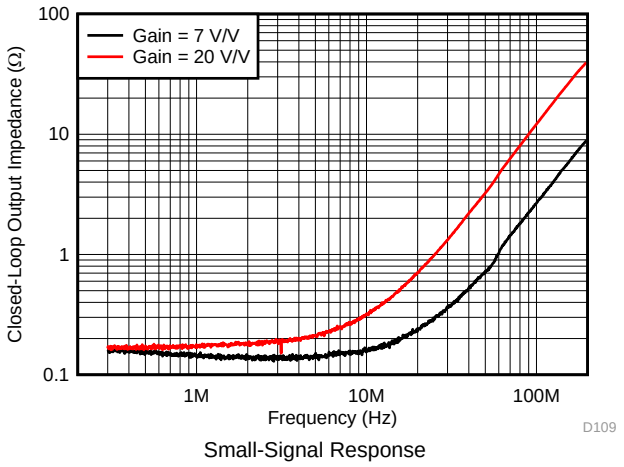



**图 9. Closed-Loop Output Impedance vs Frequency**

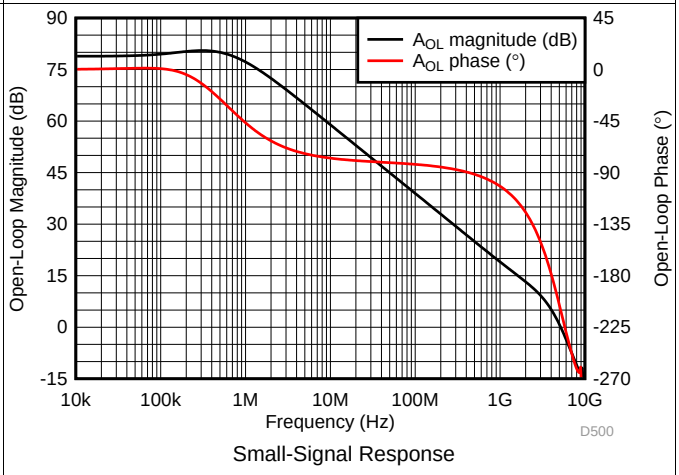



**图 10. Open-Loop Magnitude and Phase vs Frequency**

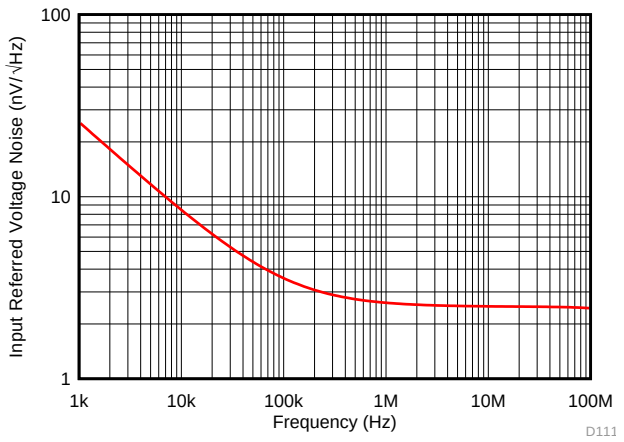



**图 11. Voltage Noise Density vs Frequency**

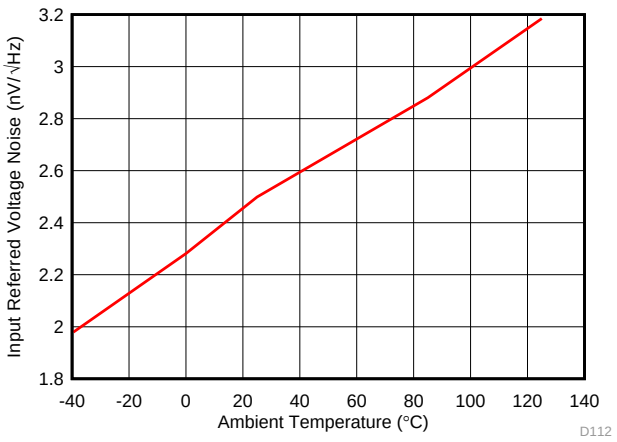



**图 12. Voltage Noise Density vs Ambient Temperature**


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## Typical Characteristics（接下页）

$V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)

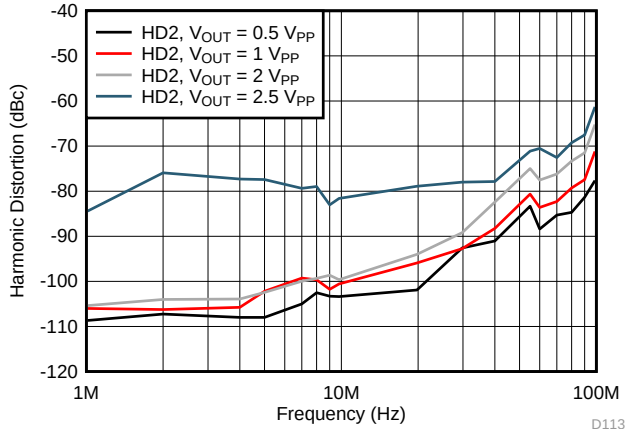



**图 13. Harmonic Distortion (HD2) vs Output Swing**

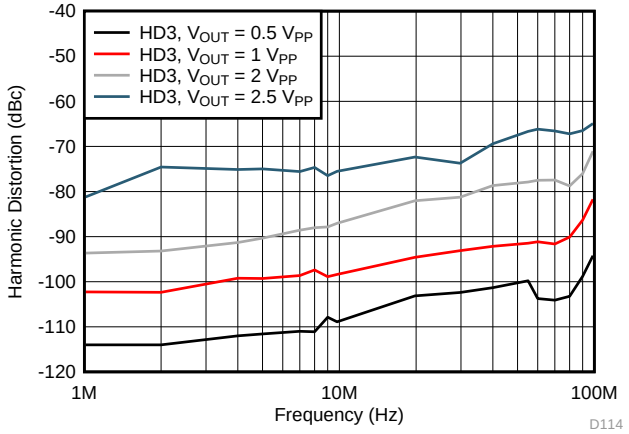



**图 14. Harmonic Distortion (HD3) vs Output Swing**

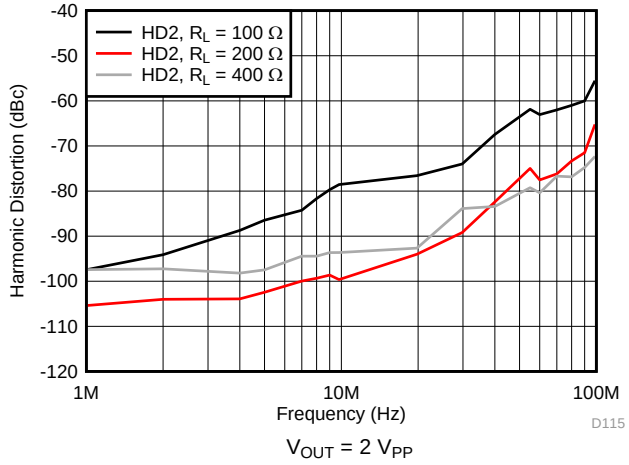



**图 15. Harmonic Distortion (HD2) vs Output Load**

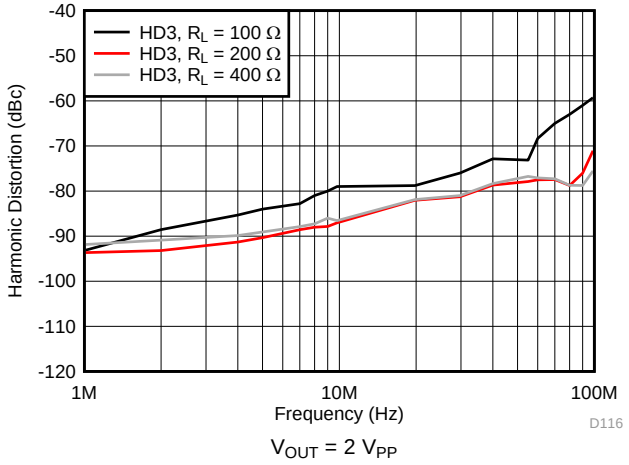



**图 16. Harmonic Distortion (HD3) vs Output Load**

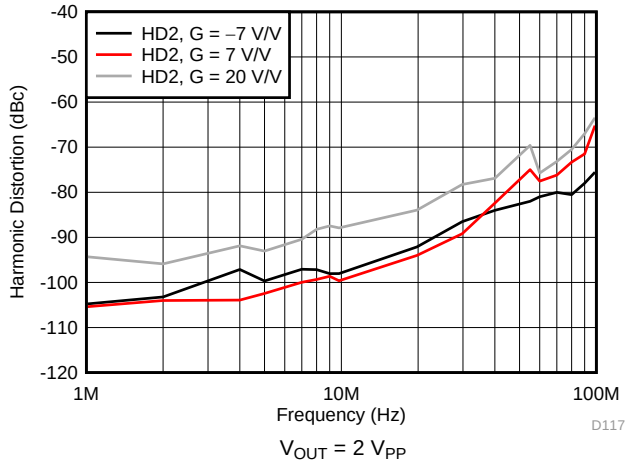



**图 17. Harmonic Distortion (HD2) vs Gain**

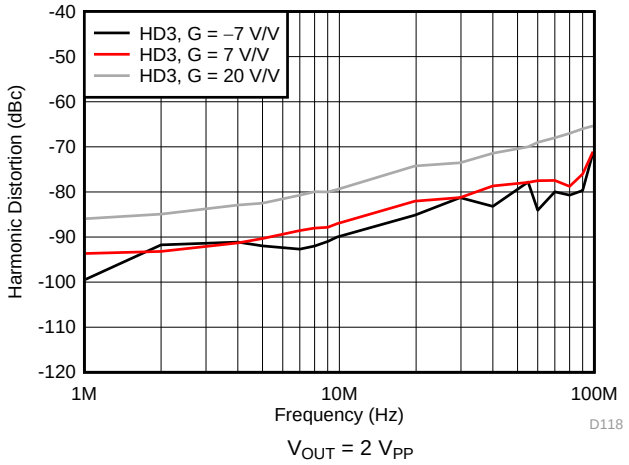
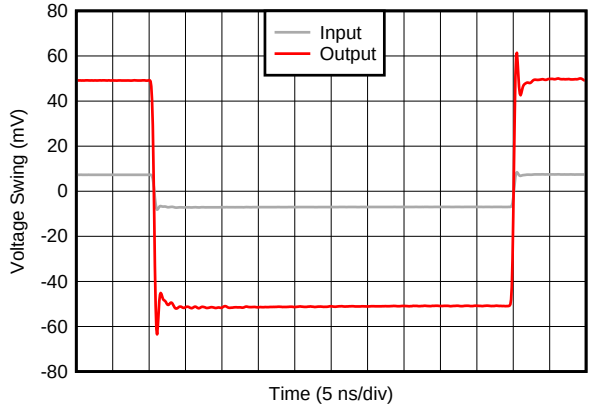



**图 18. Harmonic Distortion (HD3) vs Gain**

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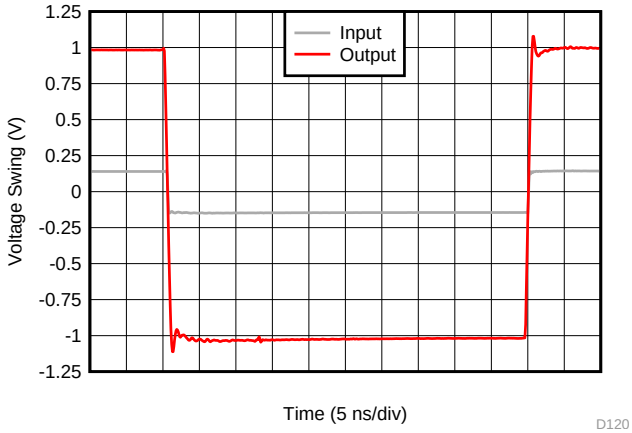
## Typical Characteristics（接下页）

$V_{S+}$ = 2.5 V, $V_{S-}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)




Average Rise and Fall Time (10% - 90%) = 450 ps

**图 19. Small-Signal Transient Response**




Average Rise and Fall Time (10% - 90%) = 750 ps

**图 20. Large-Signal Transient Response**

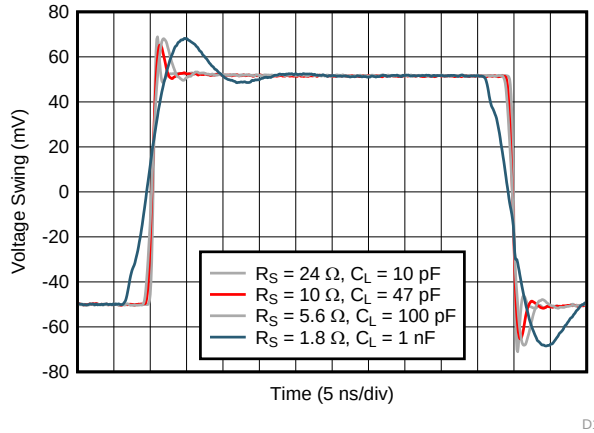
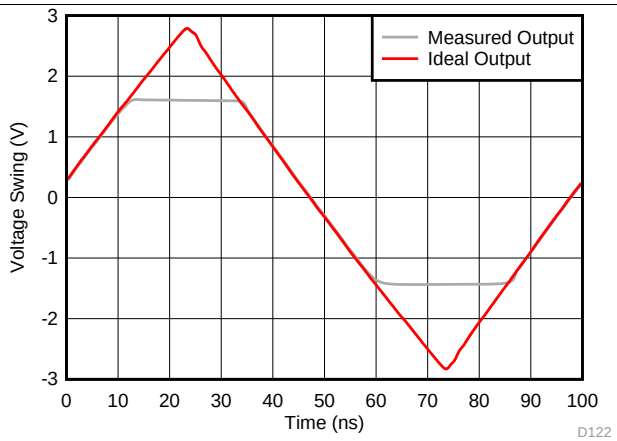
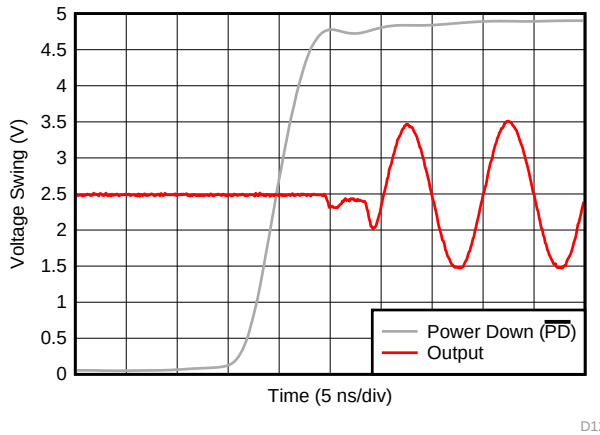



**图 21. Small-Signal Transient Response vs Capacitive Load**



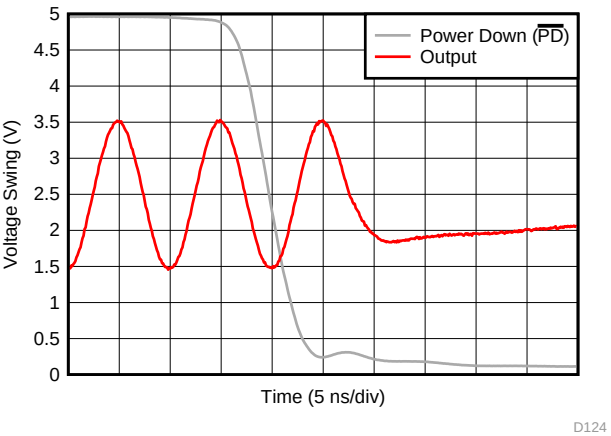

2x Output Overdrive

**图 22. Output Overload Response**




$V_{S+}$ = 5 V, $V_{S-}$ = Ground

**图 23. Turnon Transient Response**




$V_{S+}$ = 5 V, $V_{S-}$ = Ground

**图 24. Turnoff Transient Response**


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## Typical Characteristics（接下页）

$V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)

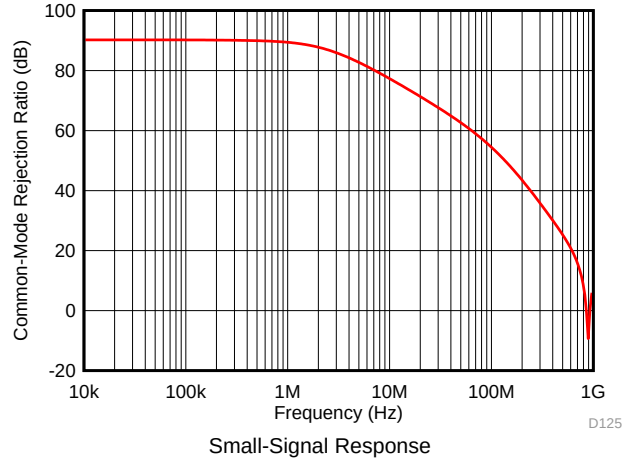



**图 25. Common-Mode Rejection Ratio vs Frequency**

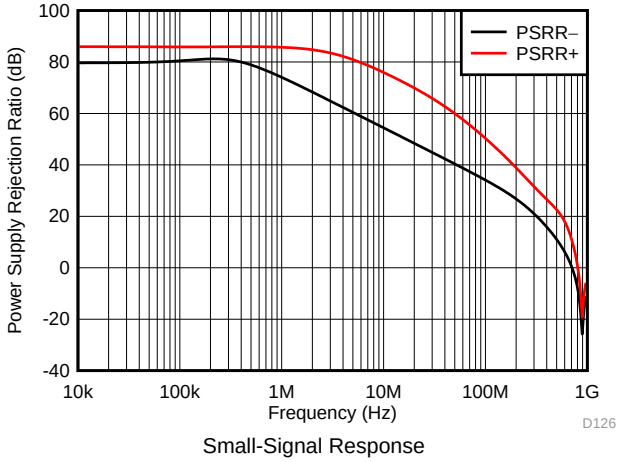



**图 26. Power Supply Rejection Ratio vs Frequency**

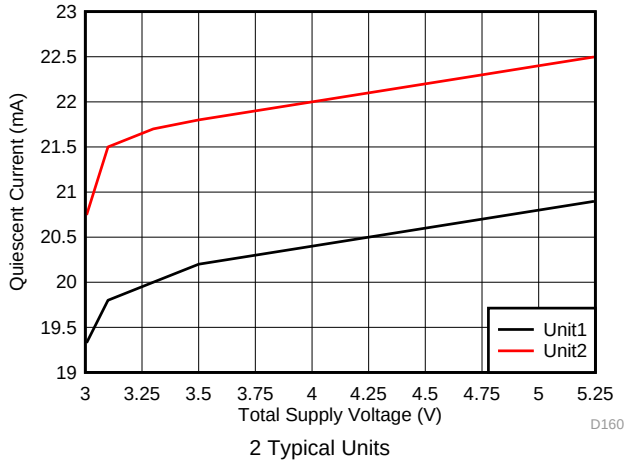



**图 27. Quiescent Current vs Supply Voltage**

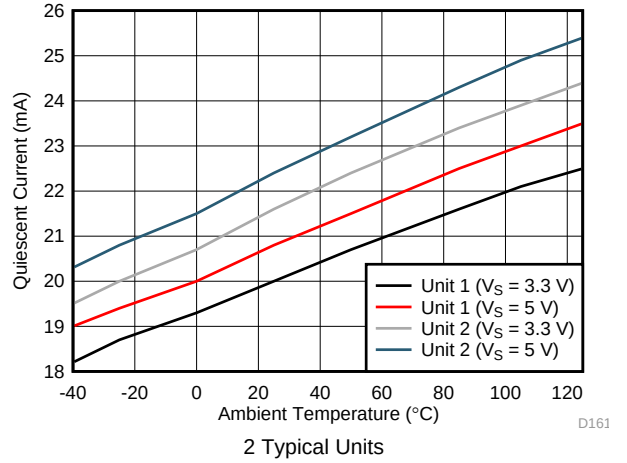



**图 28. Quiescent Current vs Ambient Temperature**

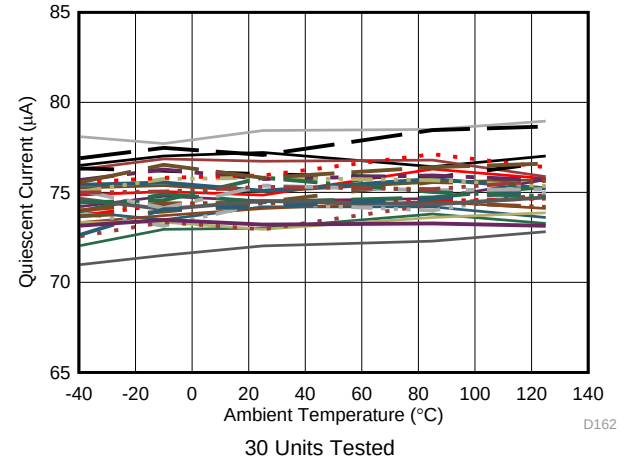



**图 29. Quiescent Current (Amplifier Disabled) vs Ambient Temperature**

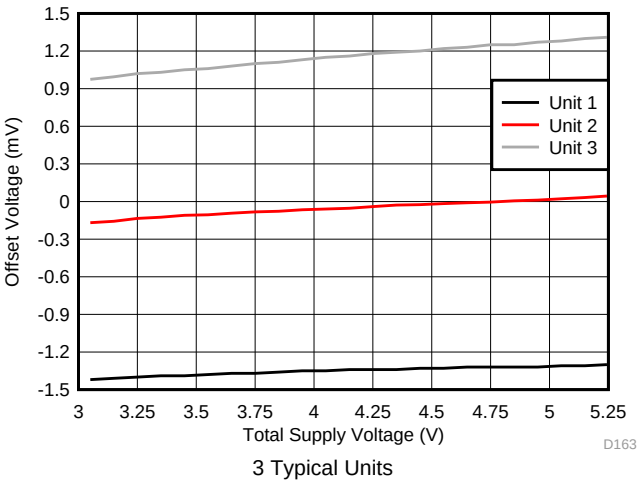
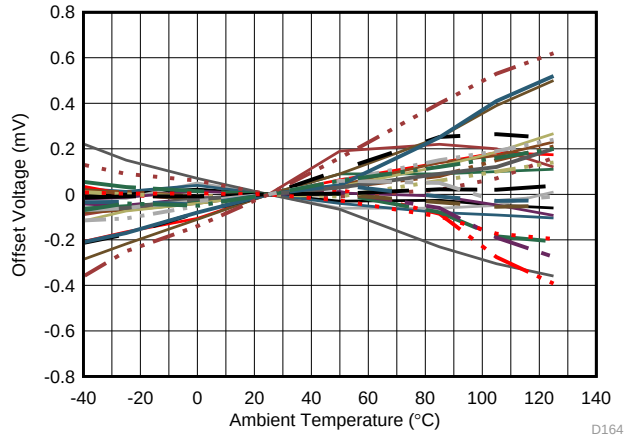



**图 30. Offset Voltage vs Supply Voltage**

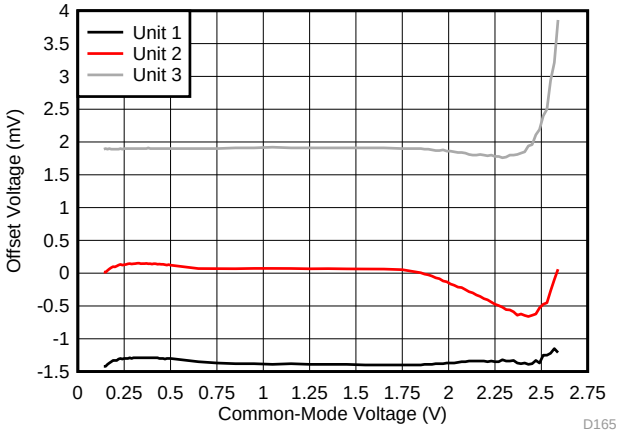
## Typical Characteristics（接下页）

$V_{S+}$ = 2.5 V, $V_{S–}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)



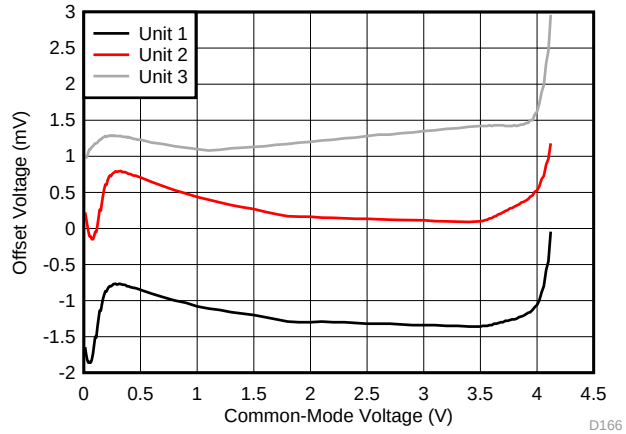

μ = 1 μV/°C　　σ = 2.2 μV/°C　　28 Units Tested

**图 31. Offset Voltage vs Ambient Temperature**




$V_S$ = 3.3 V　　3 Typical Units

**图 32. Offset Voltage vs Input Common-Mode Voltage**




$V_S$ = 5 V　　3 Typical Units

**图 33. Offset Voltage vs Input Common-Mode Voltage**

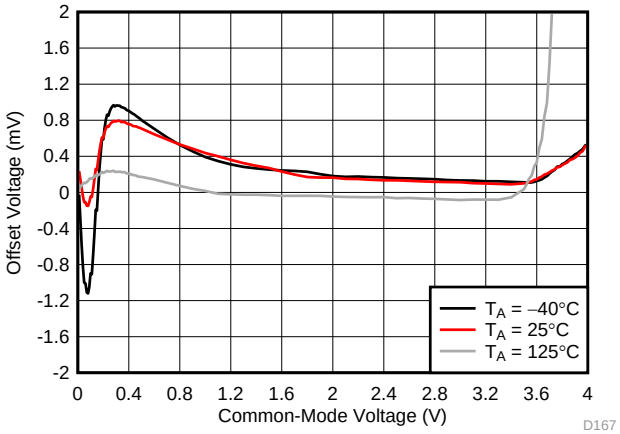
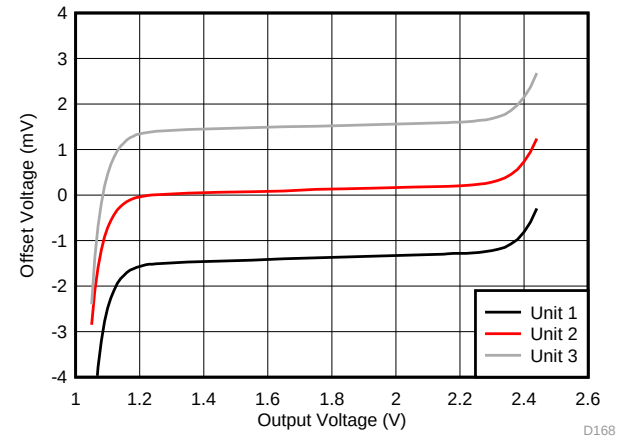
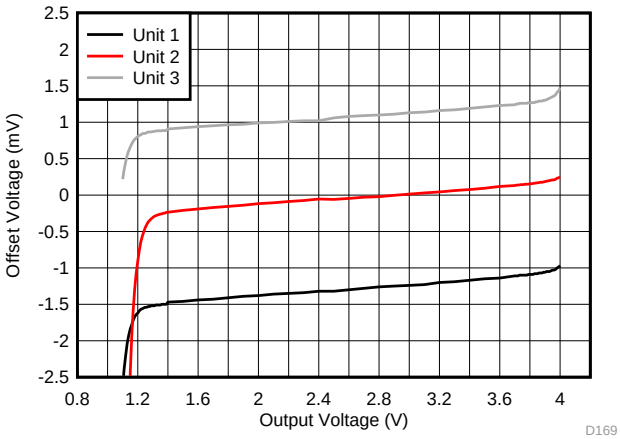



**图 34. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature**




$V_S$ = 3.3 V　　3 Typical Units

**图 35. Offset Voltage vs Output Swing**




$V_S$ = 5 V　　3 Typical Units

**图 36. Offset Voltage vs Output Swing**


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## Typical Characteristics（接下页）

$V_{S+}$ = 2.5 V, $V_{S-}$ = –2.5 V, $V_{IN+}$ = 0 V, $R_F$ = 453 Ω, Gain = 7 V/V, $R_L$ = 200 Ω, output load referenced to midsupply, and $T_A$ = 25°C (unless otherwise noted)

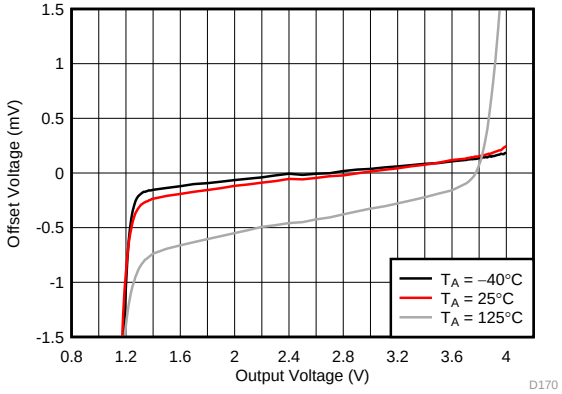
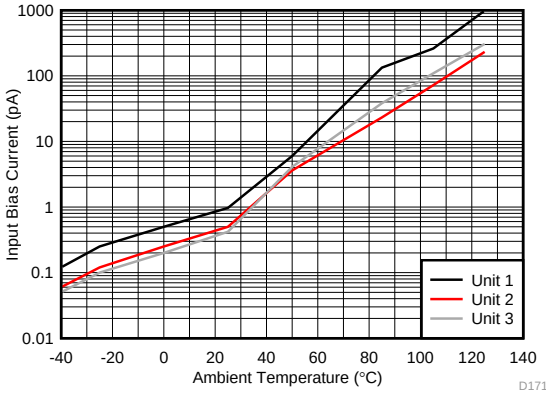



**图 37. Offset Voltage vs Output Swing vs Ambient Temperature**




3 Typical Units

**图 38. Input Bias Current vs Ambient Temperature**

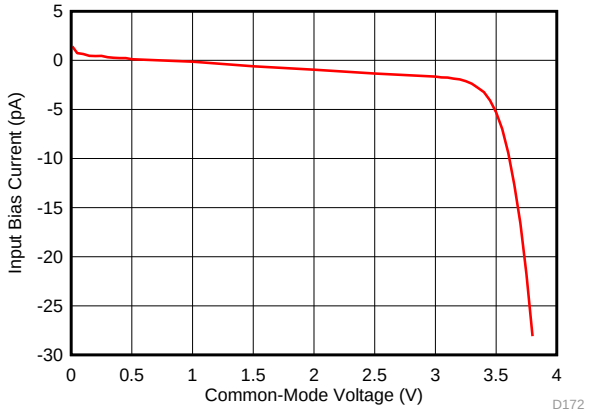
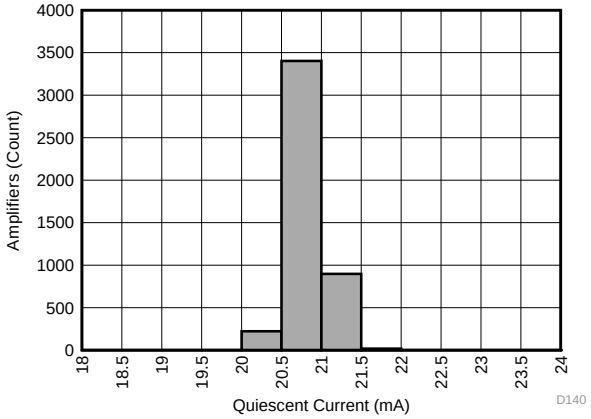
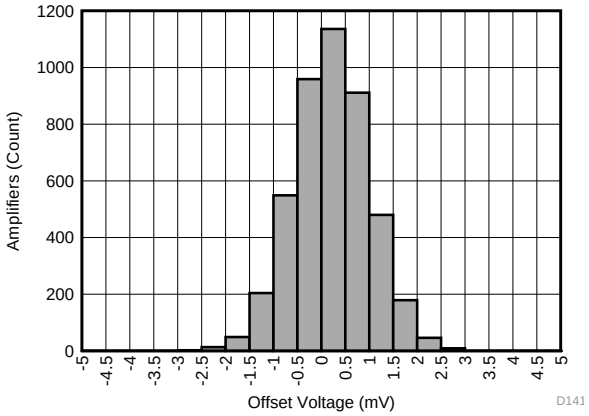



**图 39. Input Bias Current vs Input Common-Mode Voltage**



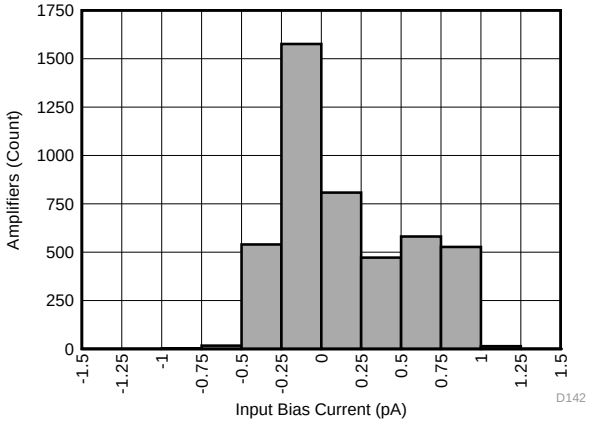

μ = 20.35 mA σ = 0.2 mA 4555 units tested

**图 40. Quiescent Current Distribution**




μ = –0.28 mV σ = 0.8 mV 4555 units tested

**图 41. Offset Voltage Distribution**



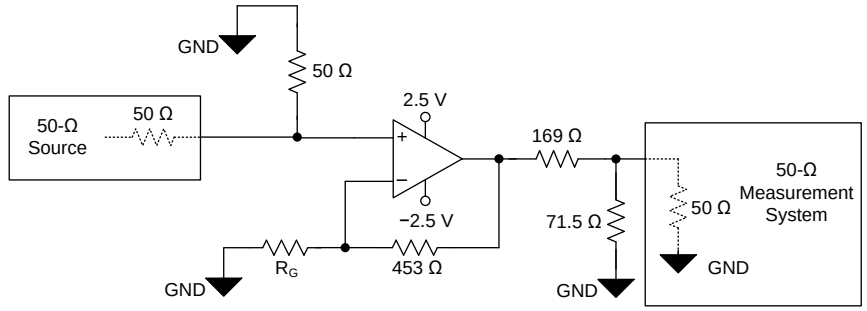

μ = –0.1 pA σ = 0.39 pA 4555 units tested

**图 42. Input Bias Current Distribution**

# 8 Parameter Measurement Information

## 8.1 Parameter Measurement Information

The various test setup configurations for the OPA858 are shown below




*$R_G$ values depend on gain configuration*

**图 43. Noninverting Configuration**

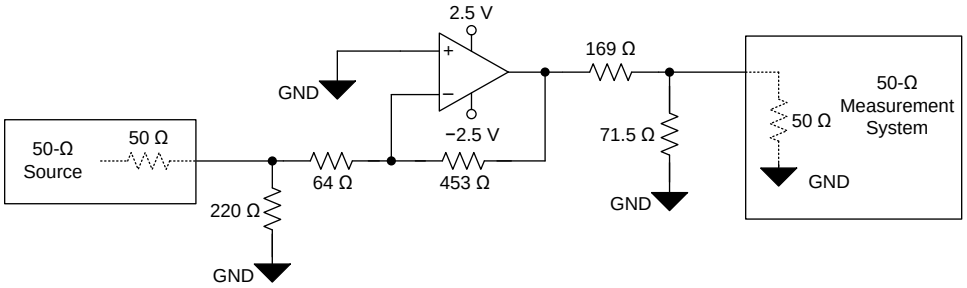



**图 44. Inverting Configuration (Gain = –7 V/V)**

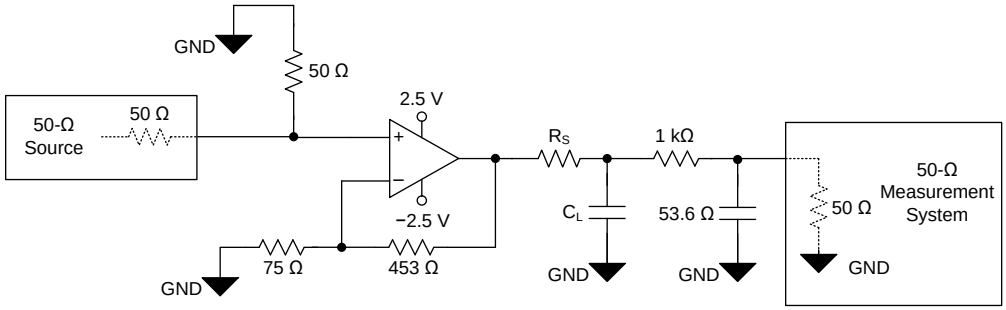



**图 45. Capacitive Load Driver Configuration**


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# 9 Detailed Description

## 9.1 Overview

The ultra-wide, 5.5-GHz gain bandwidth product (GBWP) of the OPA858, combined with the broadband voltage noise of 2.5 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA858 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA858 has 600 MHz of large signal bandwidth ($V_{OUT}$ = 2 $V_{PP}$) and a slew rate of 2000 V/µs.

The OPA858 is offered in a 2-mm × 2-mm, 8-pin WSON package that features a feedback (FB) pin for a simple feedback network connection between the amplifiers output and inverting input. Excess capacitance on an amplifiers input pin can reduce phase margin causing instability. This problem is exacerbated in the case of very wideband amplifiers like the OPA858. To reduce the effects of stray capacitance on the input node, the OPA858 pinout features an isolation pin (NC) between the feedback and inverting input pins that increases the physical spacing between them thereby reducing parasitic coupling at high frequencies. The OPA858 also features a very low capacitance input stage with only 0.8-pF of total input capacitance.

## 9.2 Functional Block Diagram

The OPA858 is a classic, voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in 图 46 and 图 47. The DC operating point for each configuration is level-shifted by the reference voltage ($V_{REF}$), which is typically set to midsupply in single-supply operation. $V_{REF}$ is typically connected to ground in split-supply applications.

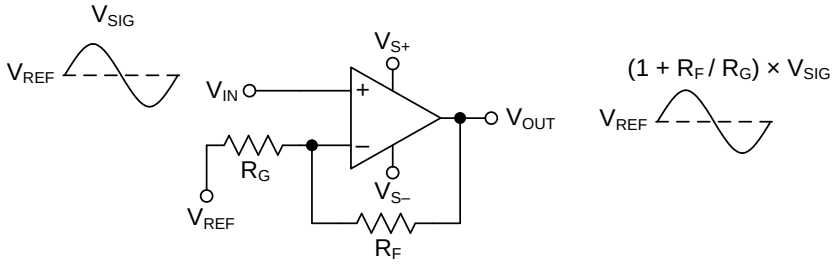



**图 46. Noninverting Amplifier**

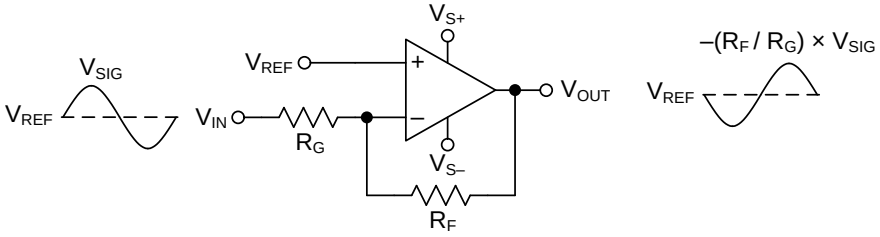



**图 47. Inverting Amplifier**

## 9.3 Feature Description

### 9.3.1 Input and ESD Protection

The OPA858 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as 图 48 shows. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

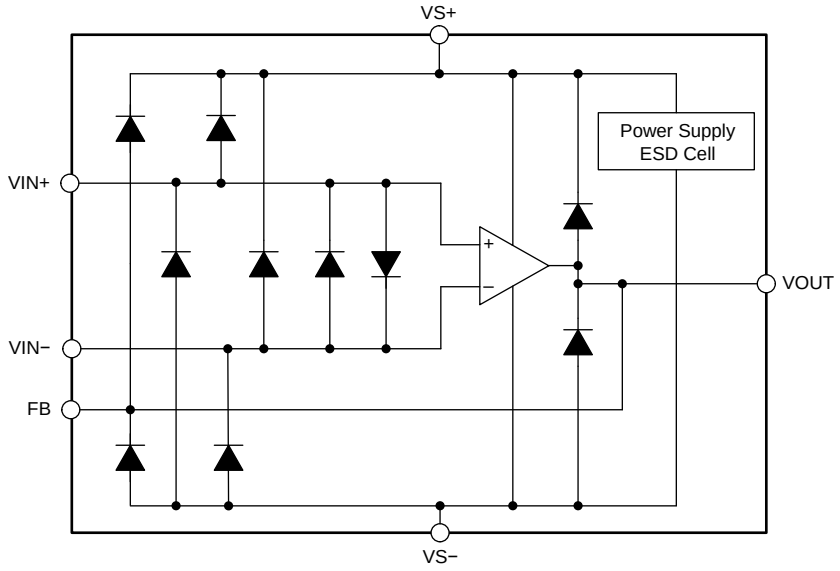



**图 48. Internal ESD Structure**

### 9.3.2 Feedback Pin

The OPA858 pin layout is optimized to minimize parasitic inductance and capacitance, which is critical in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor ($R_F$) can connect between the FB and IN– pin on the same side of the package (see 图 49) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

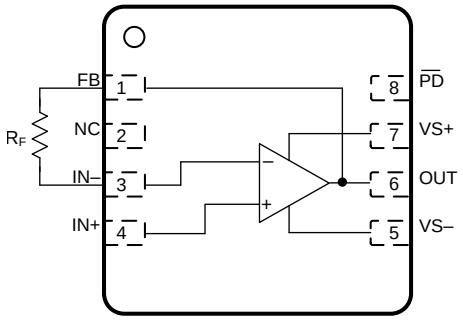



**图 49. $R_F$ Connection Between FB and IN– Pins**


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## Feature Description (接下页)

### 9.3.3 Wide Gain-Bandwidth Product

图 10 shows the open-loop magnitude and phase response of the OPA858. Calculate the gain bandwidth product of any op amp by determining the frequency at which the $A_{OL}$ is 60 dB and multiplying that frequency by a factor of 1000. The second pole in the $A_{OL}$ response occurs before the magnitude crosses 0 dB, and the resultant phase margin is less than 0°. This indicates instability at a gain of 0 dB (1 V/V). Amplifiers that are not unity-gain stable are known as decompensated amplifiers. Decompensated amplifiers typically have higher gain-bandwidth product, higher slew rate, and lower voltage noise, compared to a unity-gain stable amplifier with the same amount of quiescent power consumption.

图 50 shows the open-loop magnitude ($A_{OL}$) of the OPA858 as a function of temperature. The results show minimal variation over temperature. The phase margin of the OPA858 configured in a noise gain of 7 V/V (16.9 dB) is close to 55° across temperature. Similarly 图 51 shows the $A_{OL}$ magnitude of the OPA858 as a function of process variation. The results show the $A_{OL}$ curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results suggest less than 1° of phase margin difference within a standard deviation of process variation when the amplifier is configured in a gain of 7 V/V.

One of the primary applications for the OPA858 is as a high-speed transimpedance amplifier (TIA), as 图 59 shows. The low-frequency noise gain of a TIA is 0 dB (1 V/V). At high frequencies the ratio of the total input capacitance and the feedback capacitance set the noise gain. To maximize the TIA closed-loop bandwidth, the feedback capacitance is typically smaller than the input capacitance, which implies that the high-frequency noise gain is greater than 0 dB. As a result, op amps configured as TIAs are not required to be unity-gain stable, which makes a decompensated amplifier a viable option for a TIA. *What You Need To Know About Transimpedance Amplifiers – Part 1* and *What You Need To Know About Transimpedance Amplifiers – Part 2* describe transimpedance amplifier compensation in greater detail.

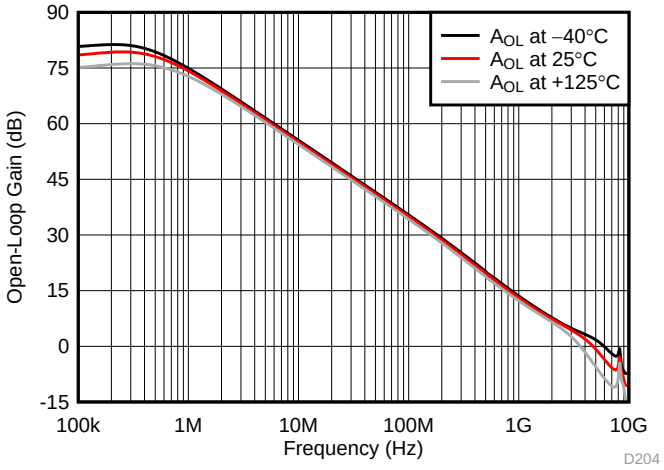



图 50. Open-Loop Gain vs Temperature

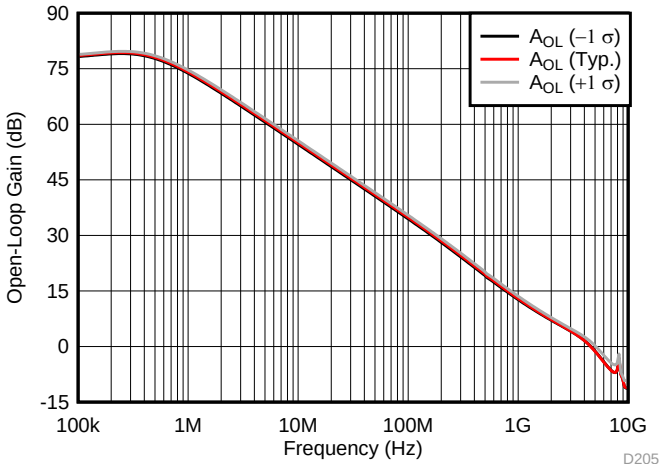



图 51. Open-Loop Gain vs Process Variation

### 9.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA858 features a high slew rate of 2000 V/µs . The slew rate is a critical parameter in high-speed pulse applications with narrow sub 10-ns pulses such as Optical Time-Domain Reflectometry (OTDR) and LIDAR. The high slew rate of the OPA858 implies that the device accurately reproduces a 2-V, sub-ns pulse edge as seen in 图 20. The wide bandwidth and slew rate of the OPA858 make it an ideal amplifier for high-speed, signal-chain front ends.

图 52 shows the open-loop output impedance of the OPA858 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA858 is limited to approximately 3 V. The OPA858 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA858 output swing range coupled with the class-leading voltage noise specification maximizes the overall dynamic range of the signal chain.

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## Feature Description (接下页)

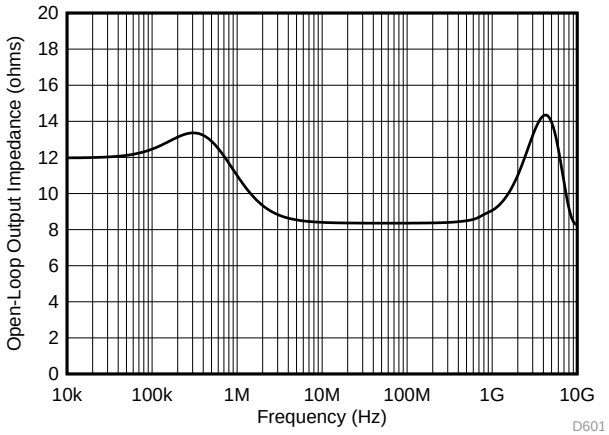



**图 52. Open-Loop Output Impedance ($Z_{OL}$) vs Frequency**

### 9.3.5 Current Noise

The input impedance of CMOS and JFET input amplifiers at low frequencies exceed several GΩs. However, at higher frequencies, the transistors parasitic capacitance to the drain, source, and substrate reduces the impedance. The high impedance at low frequencies eliminates any bias current and the associated shot noise. At higher frequencies, the input current noise increases (see 图 53) as a result of capacitive coupling between the CMOS gate oxide and the underlying transistor channel. This phenomenon is a natural artifact of the construction of the transistor and is unavoidable.

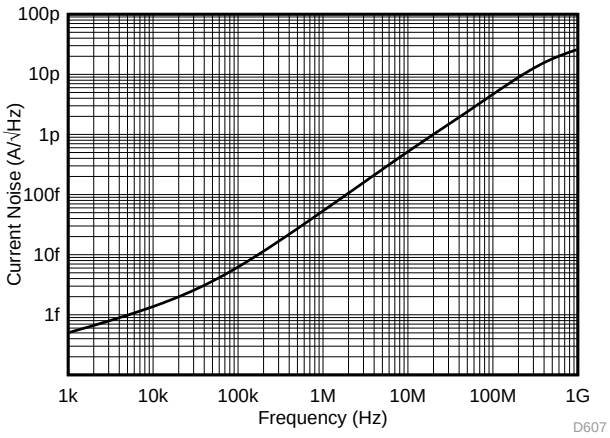



**图 53. Input Current Noise ($I_{BN}$ and $I_{BI}$) vs Frequency**


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## 9.4 Device Functional Modes

### 9.4.1 Split-Supply and Single-Supply Operation

The OPA858 can be configured with single-sided supplies or split-supplies as shown in 图 63. Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. Split-supply operation is preferred in systems where the signals swing around ground. However, the system requires two supply rails. In split-supply operation, the thermal pad must be connected to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA858 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. To change the circuit from a split-supply to a single-supply configuration, level shift all the voltages by half the difference between the power supply rails. In this case, the thermal pad must be connected to ground.

### 9.4.2 Power-Down Mode

The OPA858 features a power-down mode to reduce the quiescent current to conserve power. 图 23 and 图 24 show the transient response of the OPA858 as the $\overline{PD}$ pin toggles between the disabled and enabled states.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.65 V and 1.8 V, respectively. If the amplifier is configured with ±1.65-V supplies, then the disable and enable threshold voltages are at –1 V and 0.15 V, respectively. If the amplifier is configured with ±2.5-V supplies, then the threshold voltages are at –1.85 V and –0.7 V.

图 54 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept down from the enabled state to the disabled state. Similarly 图 55 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept up from the disabled state to the enabled state. The small difference in the switching thresholds between the down sweep and the up sweep is due to the hysteresis designed into the amplifier to increase its immunity to noise on the $\overline{PD}$ pin.

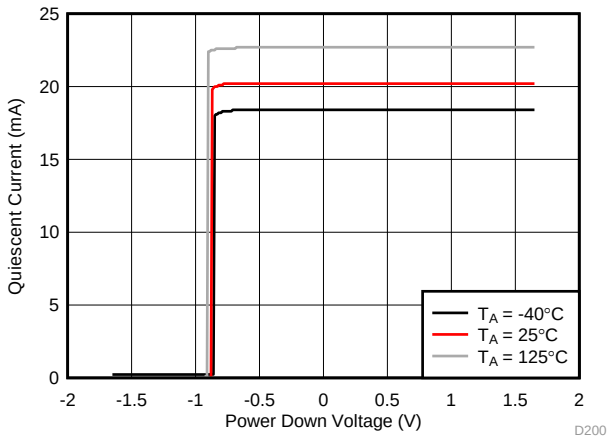



**图 54. Switching Threshold ($\overline{PD}$ Pin Swept from HIGH to LOW)**

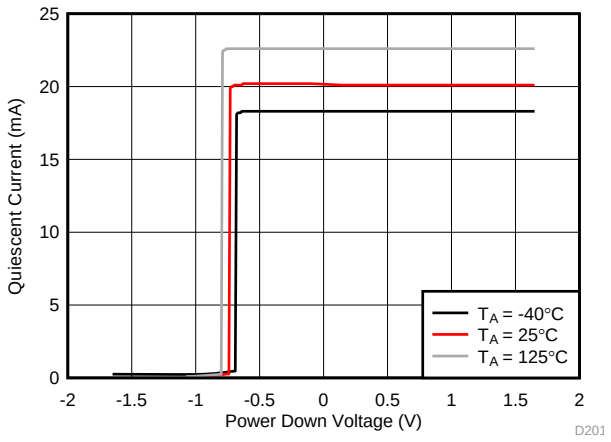



**图 55. Switching Threshold ($\overline{PD}$ Pin Swept from LOW to HIGH)**

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback ($R_F$) and gain ($R_G$) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA858 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as 图 48 shows. When the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the inputs.

# 10 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Using the OPA858 as a Transimpedance Amplifier

The OPA858 design has been optimized to meet the industry's growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance. This includes the photodiode capacitance, input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP), and,
3. The transimpedance gain $R_F$.

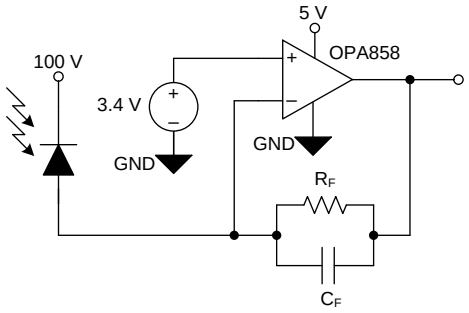



**图 56. Transimpedance Amplifier Circuit**

图 56 shows the OPA858 configured as a TIA with the avalanche photodiode (APD) reverse biased such that its cathode is tied to a large positive bias voltage. In this configuration the APD sources current into the op amp feedback loop so that the output swings in a negative direction relative to the input common-mode voltage. To maximize the output swing in the negative direction, the OPA858 common-mode is set close to the positive limit, 1.6 V from the positive supply rail.

The feedback resistance $R_F$ and the input capacitance form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted by adding the feedback capacitor ($C_F$.) into the noise gain transfer function. The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft Excel ™ calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator.


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## Application Information (接下页)

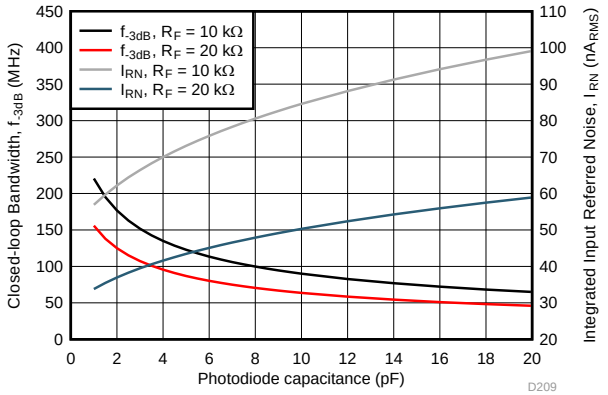



**图 57. Bandwidth and Noise Performance vs Photodiode Capacitance**

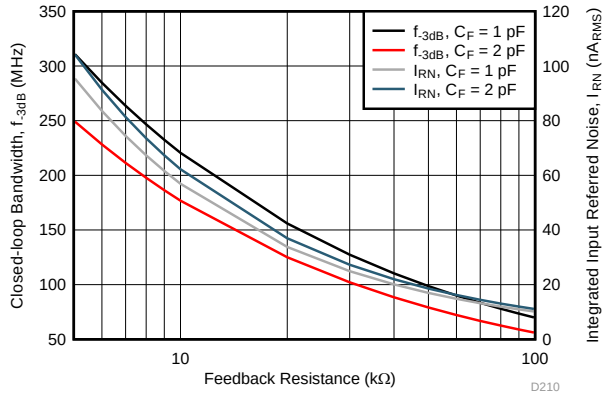



**图 58. Bandwidth and Noise Performance vs Feedback Resistance**

The equations and calculators in the application report and blog posts referenced above are used to model the bandwidth ($f_{-3dB}$) and noise ($I_{RN}$) performance of the OPA858 configured as a TIA. The resultant performance is shown in 图 57 and 图 58. The left side Y-axis shows the closed-loop bandwidth performance, while the right side of the graph shows the integrated input referred noise. The noise bandwidth to calculate $I_{RN}$, for a fixed $R_F$ and $C_{PD}$ is set equal to the $f_{-3dB}$ frequency.

图 57 shows the amplifier performance as a function of photodiode capacitance ($C_{PD}$) for $R_F$ = 10 kΩ and 20 kΩ. Increasing $C_{PD}$ decreases the closed-loop bandwidth. It is vital to reduce any stray parasitic capacitance from the PCB to maximize bandwidth. The OPA858 is designed with 0.8 pF of total input capacitance to minimize the effect on system performance.

图 58 shows the amplifier performance as a function of $R_F$ for $C_{PD}$ = 1 pF and 2 pF. Increasing $R_F$ results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage. Increasing $R_F$ by a factor of "X" increases the signal level by "X", but only increases the resistor noise contribution by "$\sqrt{X}$", thereby improving SNR.

## 10.2 Typical Application

The high GBWP, low input voltage noise and high slew rate of the OPA858 makes the device a viable wideband, high input impedance voltage amplifier.

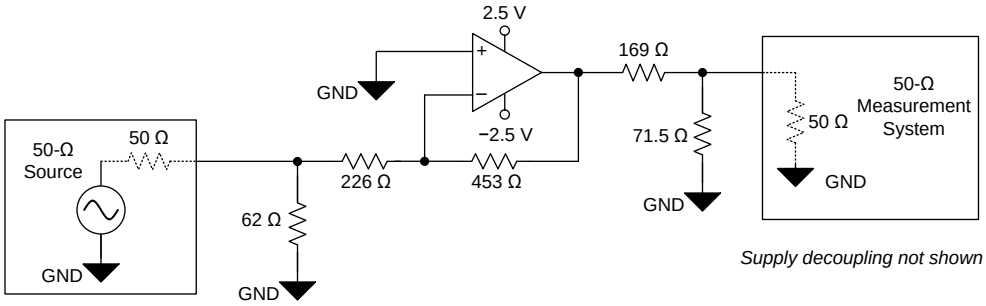



**图 59. OPA858 in a Gain of –2V/V (No Noise Gain Shaping)**

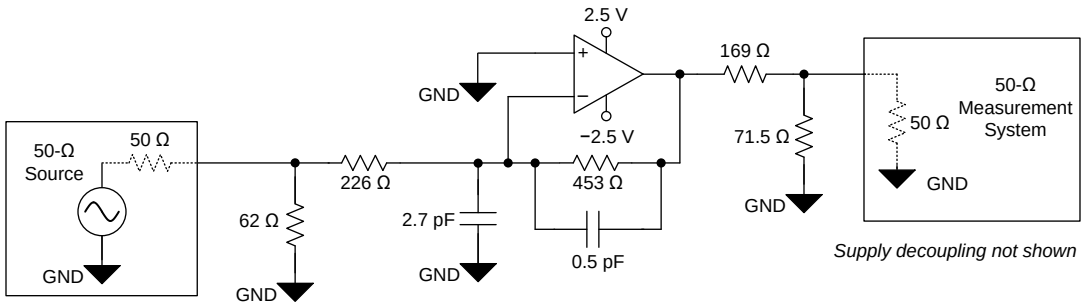



**图 60. OPA858 in a Gain of –2V/V (With Noise Gain Shaping)**

### 10.2.1 Design Requirements

Design a high-bandwidth, high-gain, voltage amplifier with the design requirements listed in 表 1. An inverting amplifier configuration is chosen here; however, the theory is applicable to a noninverting configuration as well. In an inverting configuration the signal gain and noise gain transfer functions are not equal, unlike the noninverting configuration.

**表 1. Design Requirements**

| TARGET BANDWIDTH (MHz) | SIGNAL GAIN (V/V) | FEEDBACK RESISTANCE (Ω) | FREQUENCY PEAKING (dB) |
|---|---|---|---|
| > 750 | –2 | 453 | < 2 |

### 10.2.2 Detailed Design Procedure

The OPA858 is compensated to have less than 1 dB of peaking in a gain of 7 V/V. Using the device in lower gains results in increased peaking and potential instability. 图 59 shows the OPA858 configured in a signal gain of –2 V/V. The DC noise gain (1/β) of the amplifier is affected by the 62-Ω termination resistor and the 50-Ω source resistor and is given by 公式 1. At higher frequencies the noise gain is affected by reactive elements such as inductors and capacitors. These include both discrete board components as well as printed circuit board (PCB) parasitics.

$$\text{Noise Gain} = \frac{1}{\beta} = \left(1 + \frac{453\ \Omega}{226\ \Omega + (62\ \Omega \parallel 50\ \Omega)}\right) = 2.79\ \text{V/V} = 5.04\ \text{dB} \quad (1)$$


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The stability and phase margin of the amplifier depend on the loop gain of the amplifier, which is the product of the $A_{OL}$ and the feedback factor ($\beta$) of the amplifier. The $\beta$ of a negative-feedback loop system is the portion of the output signal that is fed back to the input, and in the case of an amplifier is the inverse of the noise gain. The noise gain of the amplifier at high frequencies can be increased by adding an input capacitor and a feedback capacitor as 图 60 shows. If done carefully, increasing $1/\beta$ improves the phase margin just as any amplifier is more stable in a high gain configuration versus a unity-gain buffer configuration. The modified network with the added capacitors alters the high-frequency noise gain, but does not alter the signal gain. The *AN-1604 Decompensated Operational Amplifiers* application report provides a detailed analysis of noise gain-shaping techniques for decompensated amplifiers and shows how to choose external resistors and capacitor values.

图 61 shows the uncompensated frequency response of the OPA858 configured as shown in 图 59. Without any added noise gain shaping components, the OPA858 shows approximately 13 dB of peaking.

图 62 shows the noise gain compensated frequency response of the OPA858 configured as shown in 图 60. The noise gain shaping elements reduce the peaking to less than 1.5 dB. The 2.7-pF input capacitor, the input capacitance of the amplifier, the gain resistor, and the feedback resistor create a zero in the noise gain at a frequency *f*, as 公式 2 shows.

$$f = \frac{1}{2\pi\left(R_F \,||\, R_G\right)C_{IN}}$$

where

- $R_F$ is the feedback resistor
- $R_G$ is the input or gain resistor (includes the effect of the source and termination resistor)
- $C_{IN}$ is the total input capacitance, which includes the external 2.7-pF capacitor, the amplifier input capacitance, and any parasitic PCB capacitance. (2)

The zero in 公式 2 increases the noise gain at higher frequencies, which is important when compensating a decompensated amplifier. However, the noise gain zero reduces the loop gain phase which results in a lower phase margin. To counteract the phase reduction due to the noise gain zero, add a pole to the noise gain curve by inserting the 0.5-pF feedback capacitor. The pole occurs at a frequency shown in 公式 3. The noise gain pole and zero locations must be selected so that the rate-of-closure between the magnitude curves of $A_{OL}$ and $1/\beta$ is approximately 20 dB. To ensure this, the noise gain pole must occur before the $1/\beta$ magnitude curve intersects the $A_{OL}$ magnitude curve. In other words, the noise gain pole must occur before $|A_{OL}| = |1/\beta|$. The point at which the two curves intersect is known as the loop gain crossover frequency.

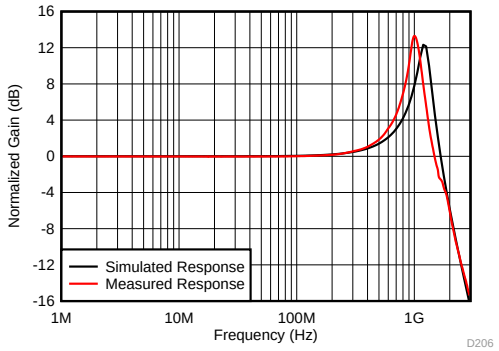
$$f = \frac{1}{2\pi R_F C_F}$$

where

- $C_F$ is the feedback capacitor (includes any added PCB parasitic) (3)

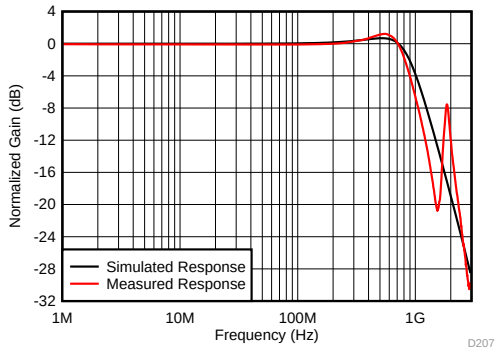
For more information on op amp stability, watch the *TI Precision Lab series on stability* video.

### 10.2.3 Application Curves




$V_{OUT}$ = 100 $mV_{PP}$

**图 61. Gain = –2 V/V, Uncompensated Frequency Response**



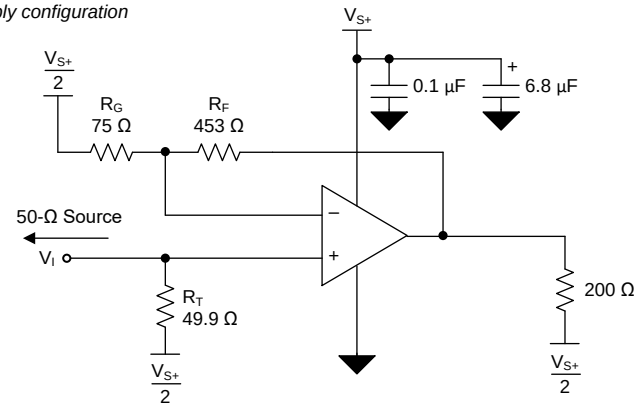

$V_{OUT}$ = 100 $mV_{PP}$

**图 62. Gain = –2 V/V, Compensated Frequency Response**

## 11 Power Supply Recommendations

The OPA858 operates on supplies from 3.3 V to 5.25 V. The OPA858 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA858 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

*a) Single supply configuration*




*b) Split supply configuration*

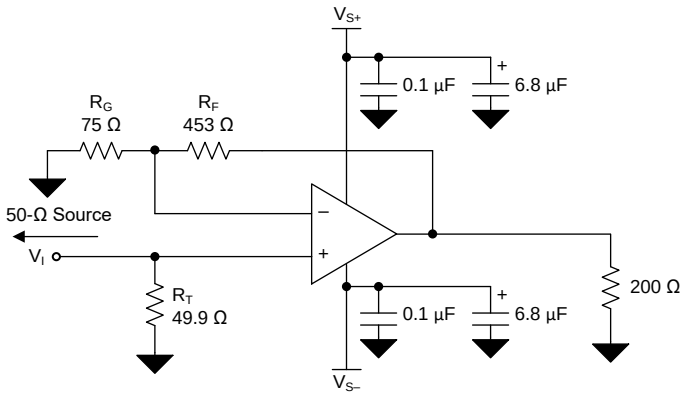



**图 63. Split and Single Supply Circuit Configuration**


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# 12 Layout

## 12.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA858 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. Minimize parasitic capacitance from the signal I/O pins to AC ground. Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, TI recommends cutting out the power and ground traces underneath the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is under 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
2. Minimize the distance (less than 0.25") from the power-supply pins to high-frequency bypass capacitors. Use high quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies to ensure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must be used on the supply pins. These are placed further from the device and are shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA858 .** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA858 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because $R_F$ and $R_G$ become part of the output load network of the amplifier.

## 12.2 Layout Example

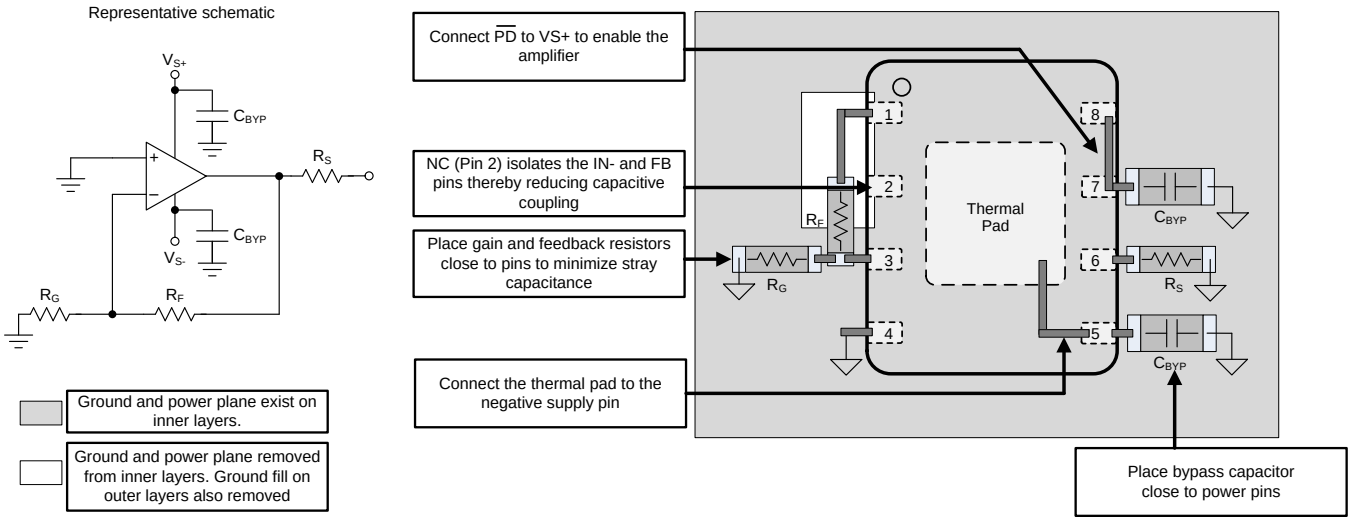



**图 64. Layout Recommendation**

## Layout Example (接下页)

When configuring the OPA858 as a transimpedance amplifier additional care must be taken to minimize the inductance between the avalanche photodiode (APD) and the amplifier. Always place the photodiode on the same side of the PCB as the amplifier. Placing the amplifier and the APD on opposite sides of the PCB increases the parasitic effects due to via inductance. APD packaging can be quite large which often requires the APD to be placed further away from the amplifier than ideal. The added distance between the two device results in increased inductance between the APD and op amp feedback network as shown in 图 65. The added inductance is detrimental to a decompensated amplifiers stability since it isolates the APD capacitance from the noise gain transfer function. The noise gain is given by 公式 4. The added PCB trace inductance between the feedback network increases the denominator in 公式 4 thereby reducing the noise gain and the phase margin. In cases where a leaded APD in a TO can is used inductance should be further minimized by cutting the leads of the TO can as short as possible.

The layout shown in 图 65 can be improved by following some of the guidelines shown in 图 66. The two key rules to follow are:

- Add an isolation resistor $R_{ISO}$ as close as possible to the inverting input of the amplifier. Select the value of $R_{ISO}$ to be between 10 Ω and 20 Ω. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.
- Close the loop between the feedback elements ($R_F$ and $C_F$) and $R_{ISO}$ as close to the APD pins as possible. This ensures a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

$$\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{IN}}\right) \quad (4)$$

where

- $Z_F$ is the total impedance of the feedback network.
- $Z_{IN}$ is the total impedance of the input network.

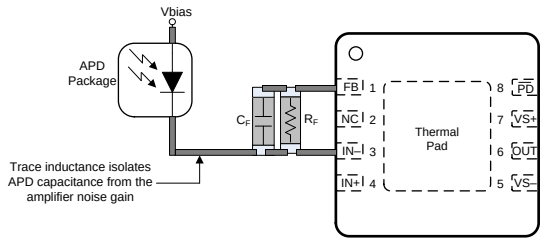



图 65. Non-Ideal TIA Layout

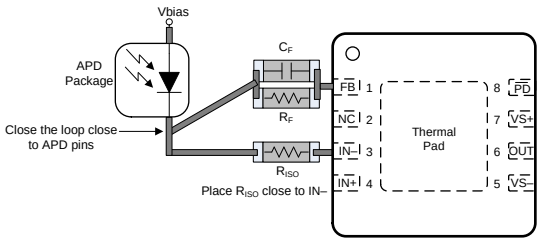



图 66. Improved TIA Layout


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# 13 器件和文档支持

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## 13.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA858IDSGR | ACTIVE | WSON | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | X858 | Samples |
| OPA858IDSGT | ACTIVE | WSON | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | X858 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

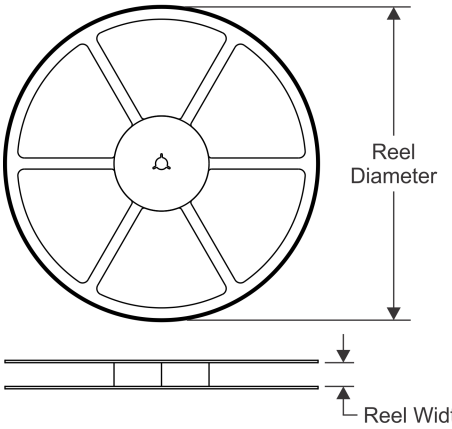
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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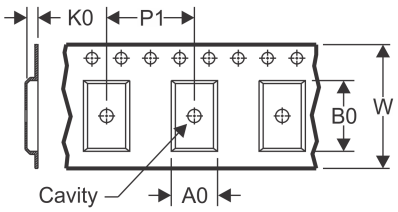
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

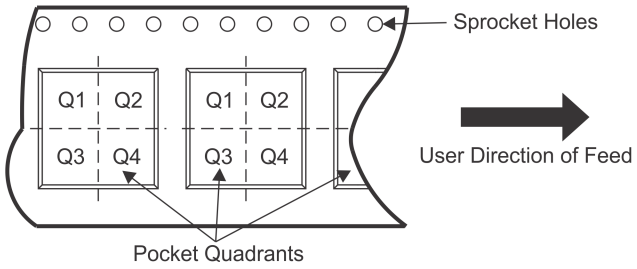



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

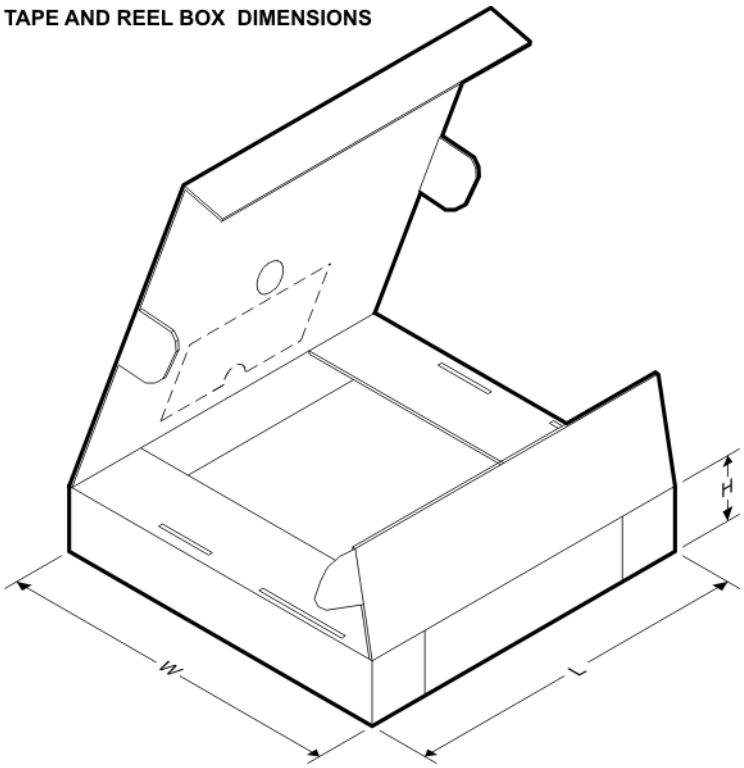
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA858IDSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| OPA858IDSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA858IDSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA858IDSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

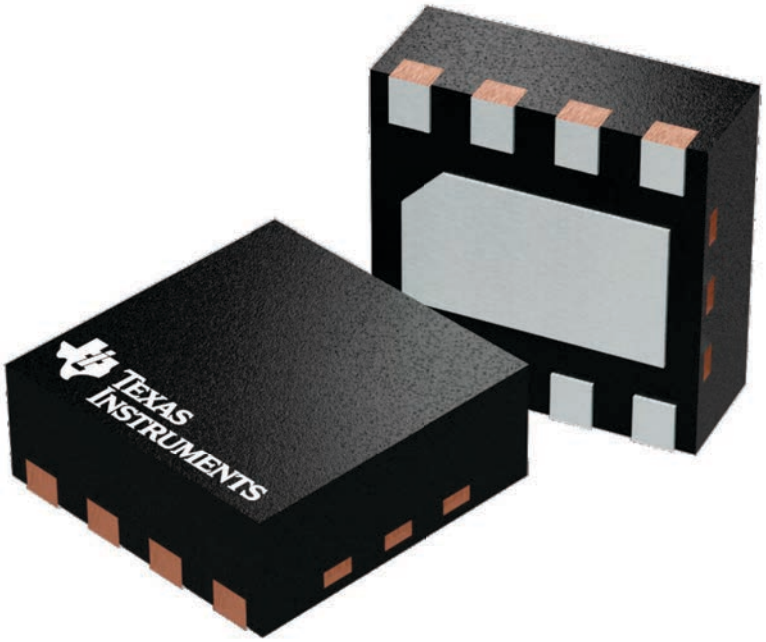
## DSG 8

## WSON - 0.8 mm max height

**2 x 2, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



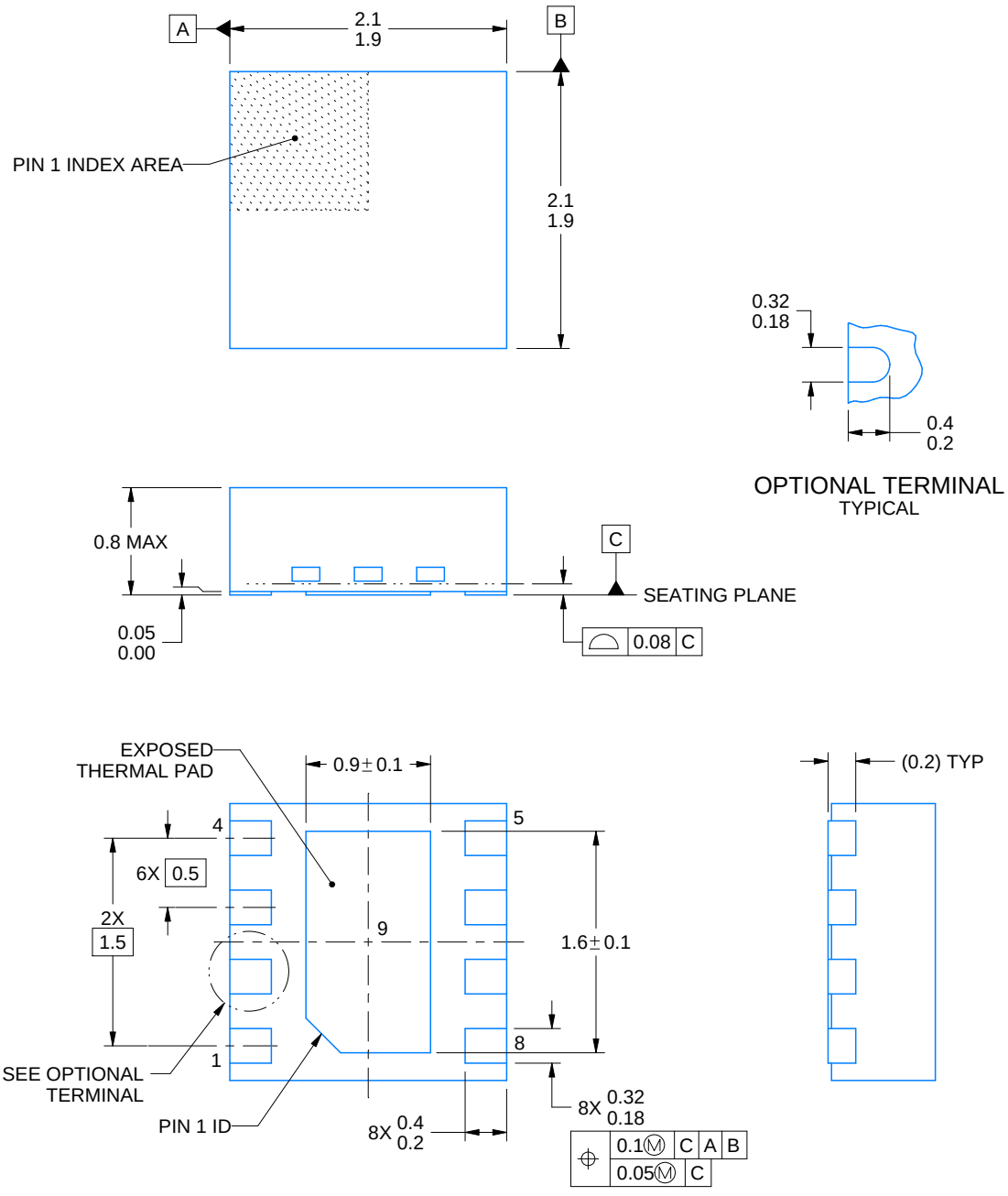

4224783/A

# PACKAGE OUTLINE

## DSG0008A

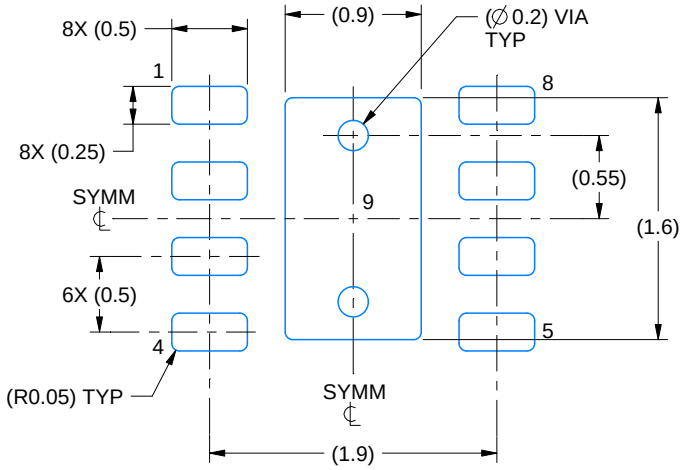
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

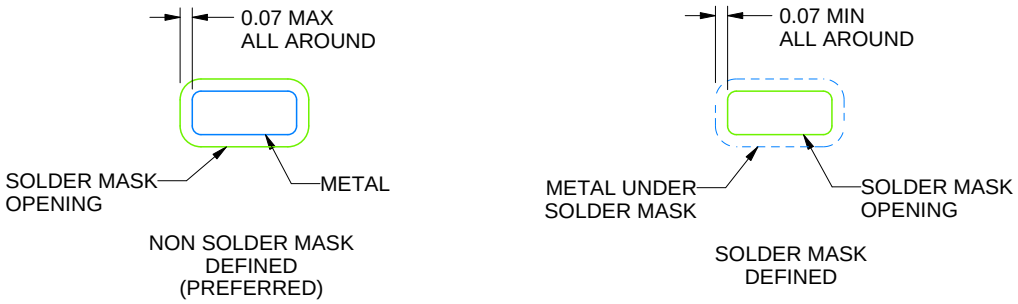



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

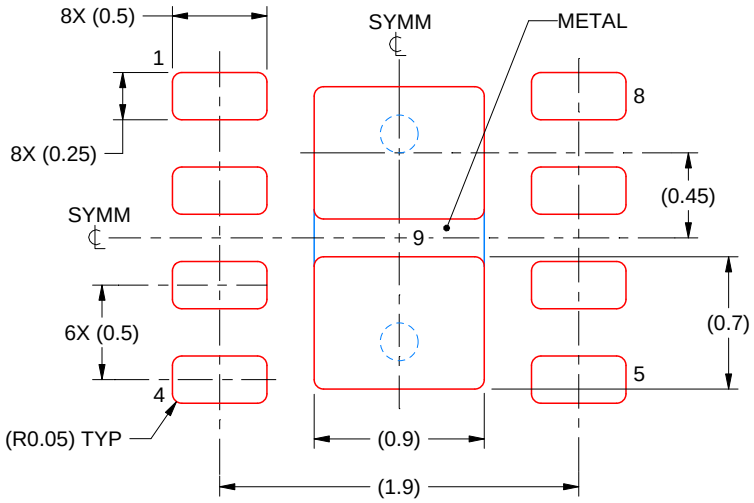



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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