OPA2356-EP 200MHz CMOS 运算放大器

1 特性

- 单位增益带宽：450MHz
- 宽带宽：200MHz GBW
- 高压摆率：360V/µs
- 低噪声：5.8nV/√Hz
- 出色的视频性能：
  - 差分增益：0.02%
  - 差分相位：0.05°
  - 0.1dB 增益平坦度：75MHz
- 输入范围包括接地电压
- 轨至轨输出（在 100mV 以内）
- 低输入偏置电流：3pA
- 热关断
- 单电源工作电压范围：2.5V 至 5.5V
- 微型封装
- 支持国防、航天和医疗 应用：
  - 受控基线
  - 支持军用（–55°C 至 125°C）温度范围
  - 延长了产品生命周期
  - 延长了产品变更通知
  - 产品可追溯性

2 应用

- 视频处理
- 光纤网络，可调激光
- 光电二极管跨阻放大器
- 有源滤波器
- 高速集成器
- 模数转换器 (ADC) 输入缓冲器
- 数模转换器 (DAC) 输出放大器
- 通信

3 说明

OPA2356-EP 高速电压反馈 CMOS 运算放大器设计专为视频应用和其他需要宽带宽的 应用 而设计。OPA2356-EP 具有单位增益稳定性，并且可以驱动大输出电流。差分增益为 0.02%，差分相位为 0.05°。静态电流仅为每通道 8.3mA。

OPA2356-EP 针对低至 2.5V (±1.25V) 和高达 5.5V (±2.75V) 的单电源或双电源供电运行进行了优化。OPA2356-EP 的共模输入范围的下限可扩展至低于接地电压 100mV，上限可扩展至高于 V+ 电压 1.5V。输出摆幅控制在电源轨的 100mV 以内，支持宽动态范围。

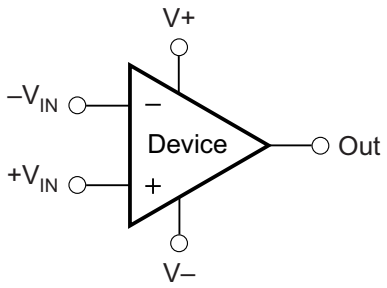
OPA2356-EP 提供两种 VSSOP-8 封装版本。这些版本具有完全独立的电路，可将串扰降到最低并彻底消除相互干扰。OPA2356-EP 的额定扩展工作温度范围为 –55°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA2356MDGKREP	VSSOP (8)	3.00mm × 3.00mm
OPA2356MDGKTEP		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

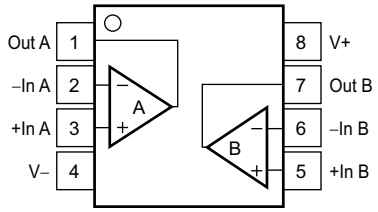
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 2 月	*	初始发行版。

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5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



NOTE: NC means no internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–In A	2	I	Inverting input pin, channel A.
–In B	6	I	Inverting input pin, channel B.
+In A	3	I	Noninverting input pin, channel A.
+In B	5	I	Noninverting input pin, channel B.
Out A	1	O	Output pin, channel A.
Out B	7	O	Output pin, channel B.
V–	4	—	Negative power supply.
V+	8	—	Positive power supply.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V+ to V–		7.5	V
	Signal input pins, voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Signal input pins, current(2)		10	mA
	Output short-circuit(3)	Continuous		
T_A	Operating temperature	–55	150	°C
T_J	Junction temperature		160	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.7	5.5	V
T_A	Operating free-air temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2356-EP DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at T_A = –55°C to 125°C, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		V_S = 5 V		±2	±9	mV
			T_A = –55°C to 125°C			±15	
$\Delta V_{OS}/\Delta T$	Offset voltage drift over temperature		T_A = –55°C to 125°C		±7		µV/°C
PSRR	Offset voltage drift vs power supply		V_S = 2.7 V to 5.5 V, V_{CM} = V_S / 2 – 0.15 V		±80	±350	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				3	±50	pA
I_{OS}	Input offset current				±1	±50	pA
NOISE							
V_n	Input voltage noise density		f = 1 MHz		5.8		nV/√Hz
I_n	Current noise density		f = 1 MHz		50		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Input common-mode voltage range			(V–) – 0.1		(V+) – 1.5	V
CMRR	Input common-mode rejection ratio		V_S = 5.5 V, –0.1 V < V_{CM} < 4 V	66	80		dB
			T_A = –55°C to 125°C	66			
INPUT IMPEDANCE							
	Differential input impedance				10^{13} || 1.5		Ω || pF
	Common-mode input impedance				10^{13} || 1.5		Ω || pF
OPEN-LOOP GAIN							
	Open-loop gain		V_S = 5 V, 0.4 V < V_O < 4.6 V, T_A = –55°C to 125°C	80			dB
FREQUENCY RESPONSE							
$f_{–3dB}$	Small-signal bandwidth		G = 1, V_O = 100 mVp-p, R_F = 0 Ω		450		MHz
			G = 2, V_O = 100 mVp-p, R_L = 50 Ω		100		
			G = 2, V_O = 100 mVp-p, R_L = 150 Ω		170		
			G = 2, V_O = 100 mVp-p, R_L = 1 kΩ		200		
GBW	Gain-bandwidth product		G = 10, R_L = 1 kΩ		200		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness		G = 2, V_O = 100 mVp-p, R_F = 560 Ω		75		MHz
SR	Slew rate		V_S = 5 V, G = 2, 4-V output step		300		V/µs
					–360		
	Rise and fall times		G = 2, V_O = 200 mVp-p, 10% to 90%		2.4		ns
			G = 2, V_O = 2 Vp-p, 10% to 90%		8		
	Settling time	0.1%	V_S = 5 V, G = 2, 2-V output step		30		ns
		0.01%			120		
	Overload recovery time		V_{IN} × Gain = V_S		8		ns
	Harmonic distortion	Second harmonic	G = 2, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω		–81		dBc
		Third harmonic			–93		
	Differential gain error		NTSC, R_L = 150 Ω		0.02%		
	Differential phase error		NTSC, R_L = 150 Ω		0.05		°
	Channel-to-channel crosstalk		f = 5 MHz		–90		dB

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Electrical Characteristics (continued)

at T_A = –55°C to 125°C, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	V_S = 5 V, R_L = 150 Ω, A_{OL} > 84 dB		0.2	0.3	V
		V_S = 5 V, R_L = 1 kΩ		0.1		
		I_O = ±100 mA		0.8	1	
I_O	Continuous output current(1)		±60			mA
I_O	Peak output current(1)	V_S = 5 V	±100			mA
		V_S = 3 V		±80		
	Short-circuit current			250		mA
				–200		
	Closed-loop output impedance			0.02		Ω
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	V_S = 5 V, I_O = 0 V		8.3	11	mA
		T_A = –55°C to 125°C			14	
THERMAL SHUTDOWN						
	Junction temperature	Shutdown		160		°C
		Reset from shutdown		140		

(1) See Figure 20.

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6.6 Typical Characteristics

at T_A = –55°C to 125°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

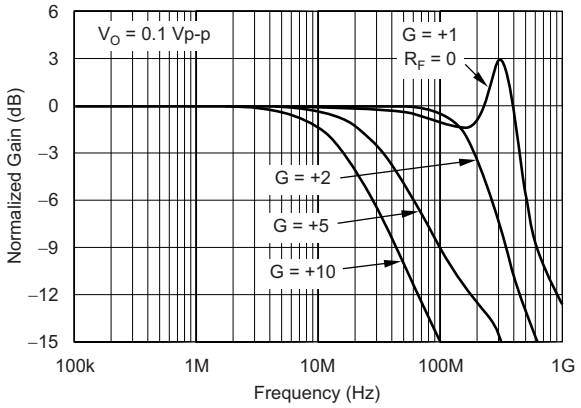


Figure 1. Noninverting Small-Signal Frequency Response

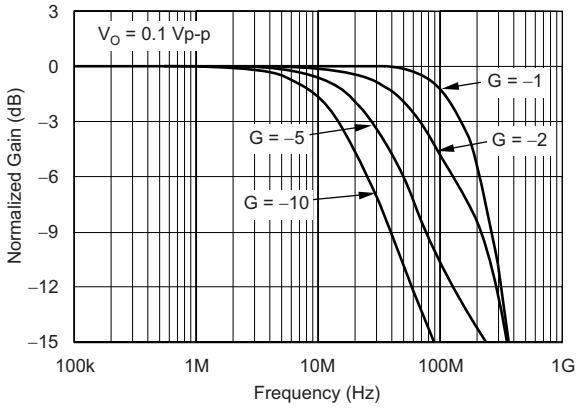


Figure 2. Inverting Small-Signal Frequency Response

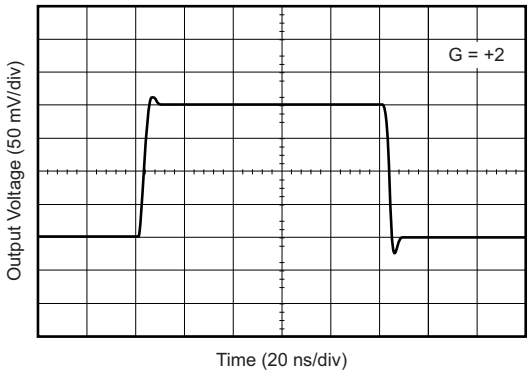


Figure 3. Noninverting Small-Signal Step Response

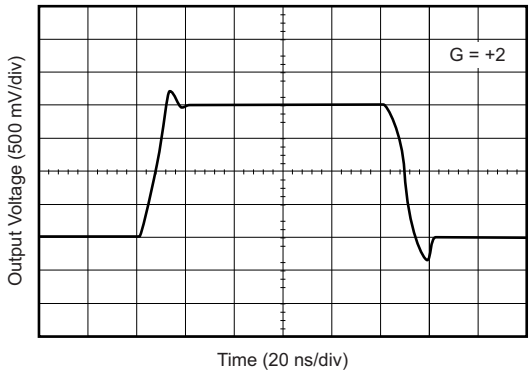


Figure 4. Noninverting Large-Signal Step Response

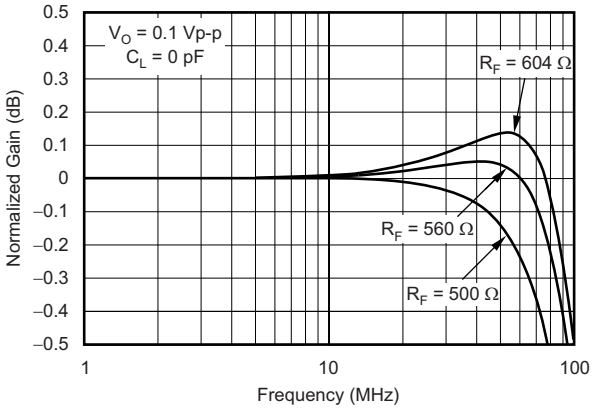


Figure 5. 0.1-dB Gain Flatness for Various R_F

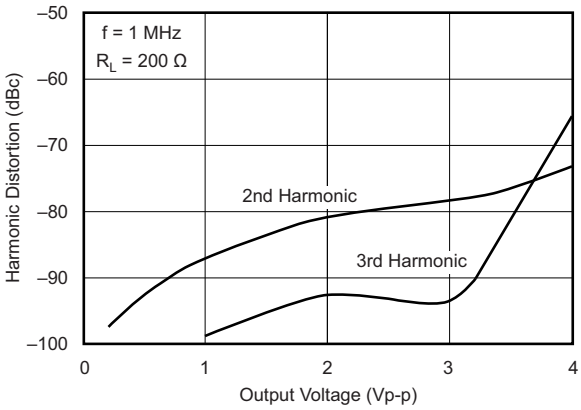


Figure 6. Harmonic Distortion vs Output Voltage

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Typical Characteristics (continued)

at T_A = –55°C to 125°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

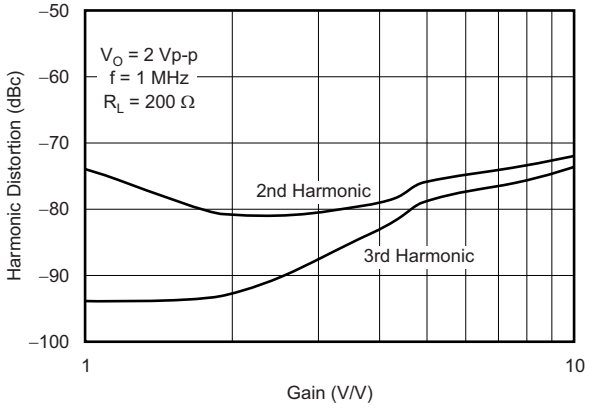


Figure 7. Harmonic Distortion vs Noninverting Gain

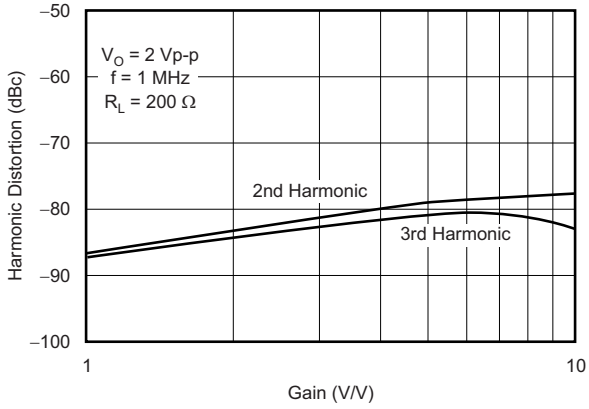


Figure 8. Harmonic Distortion vs Inverting Gain

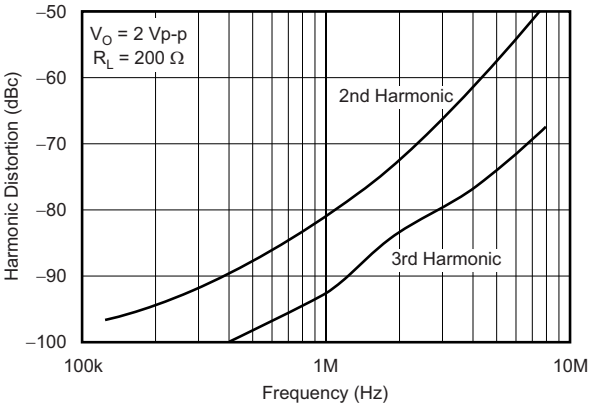


Figure 9. Harmonic Distortion vs Frequency

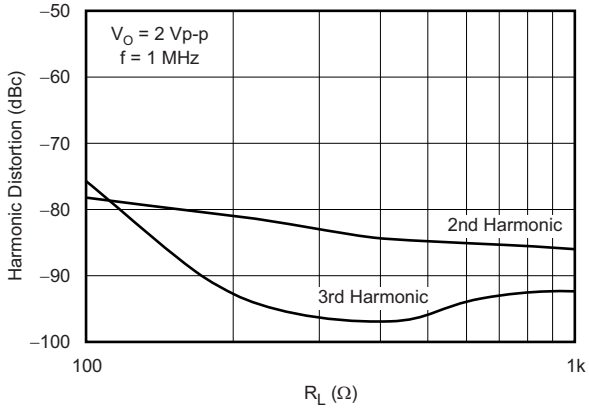


Figure 10. Harmonic Distortion vs Load Resistance

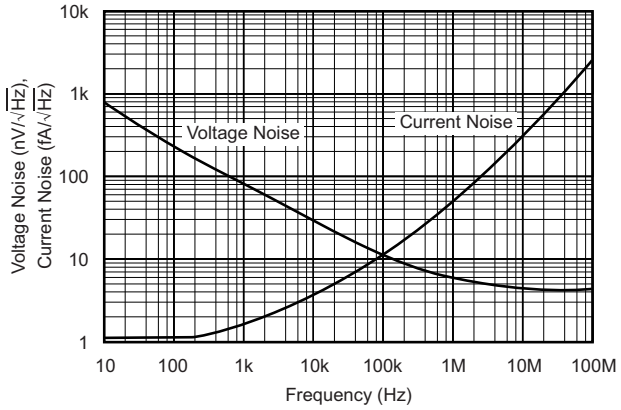


Figure 11. Input Voltage and Current Noise Spectral Density vs Frequency

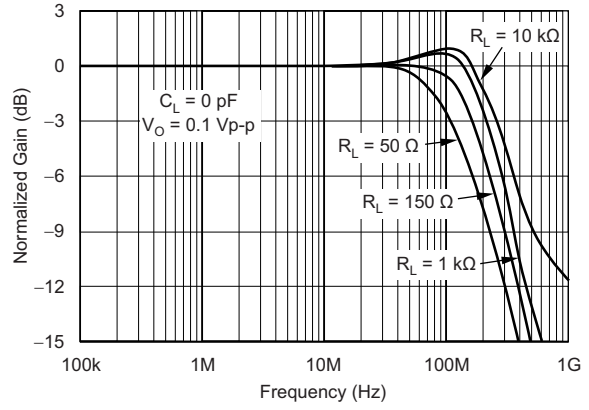


Figure 12. Frequency Response for Various R_L

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Typical Characteristics (continued)

at T_A = –55°C to 125°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

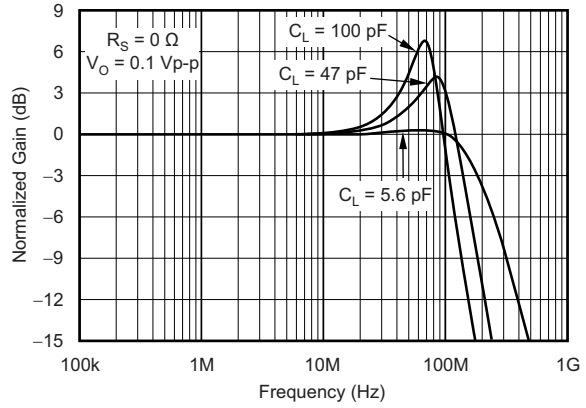


Figure 13. Frequency Response for Various C_L

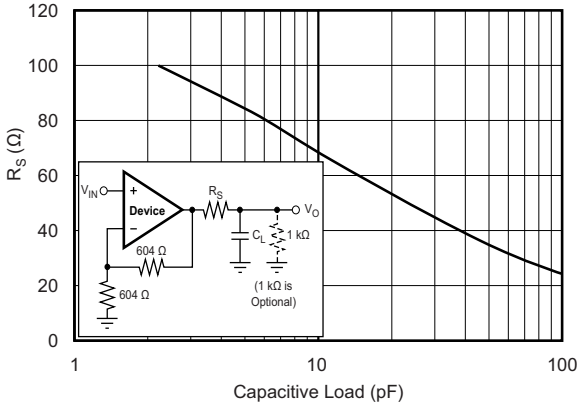


Figure 14. Recommended R_S vs Capacitive Load

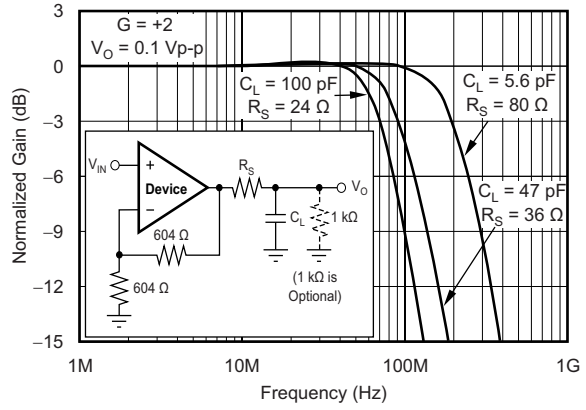


Figure 15. Frequency Response vs Capacitive Load

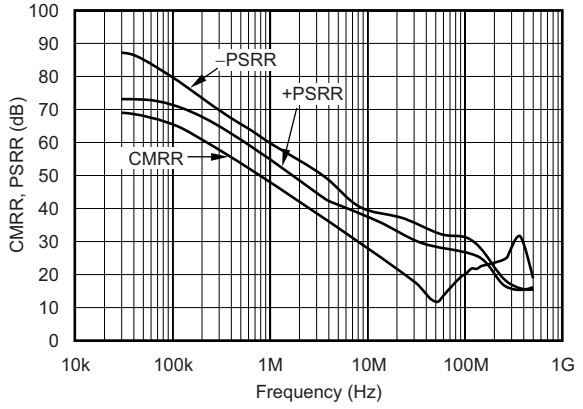


Figure 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

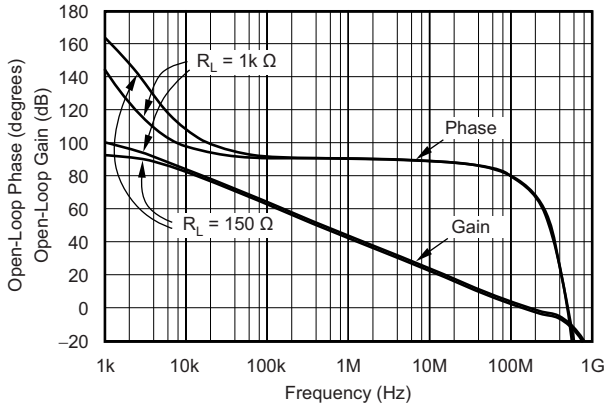


Figure 17. Open-Loop Gain and Phase

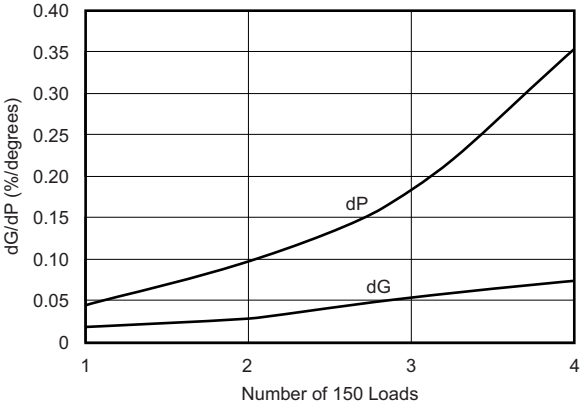


Figure 18. Composite Video Differential Gain and Phase

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Typical Characteristics (continued)

at T_A = –55°C to 125°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

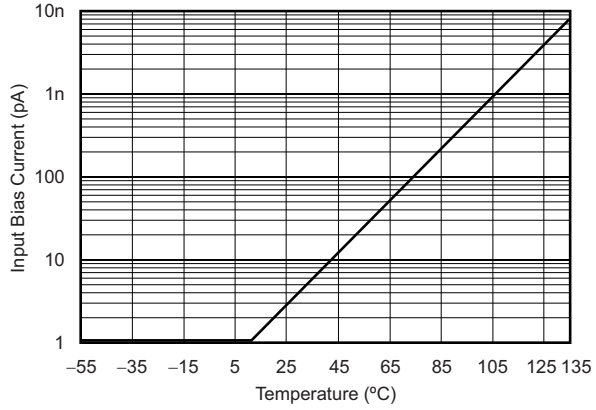


Figure 19. Input Bias Current vs Temperature

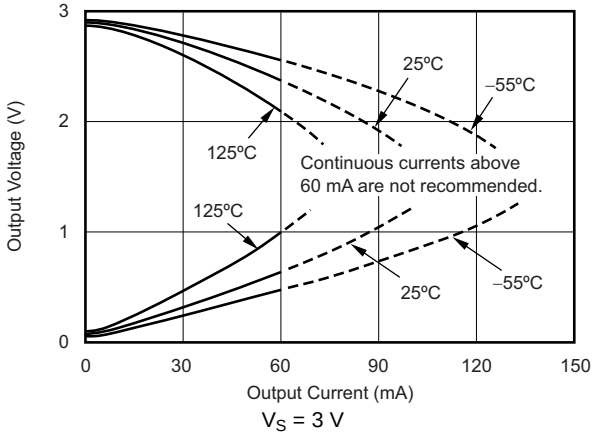


Figure 20. Output Voltage Swing vs Output Current

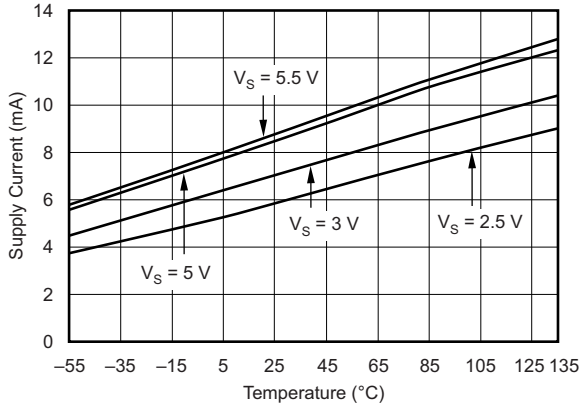


Figure 21. Supply Current vs Temperature

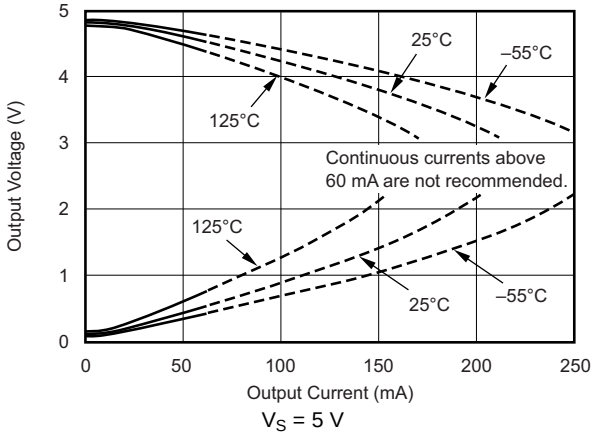


Figure 22. Output Voltage Swing vs Output Current

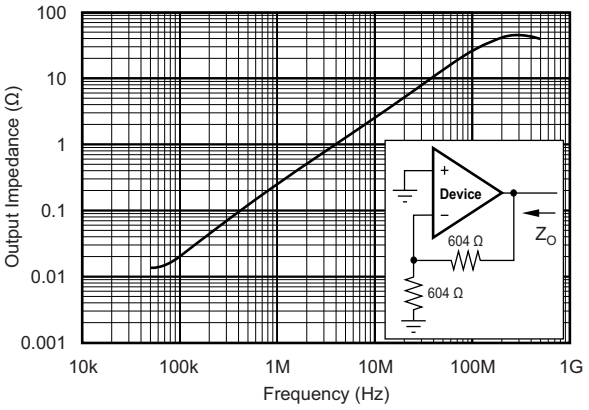


Figure 23. Closed-Loop Output Impedance vs Frequency

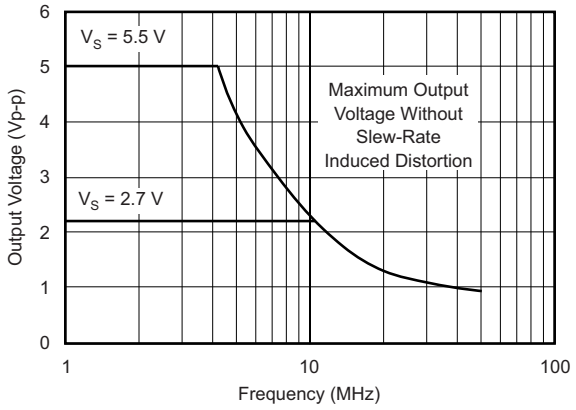


Figure 24. Maximum Output Voltage vs Frequency

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Typical Characteristics (continued)

at T_A = –55°C to 125°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2 (unless otherwise noted)

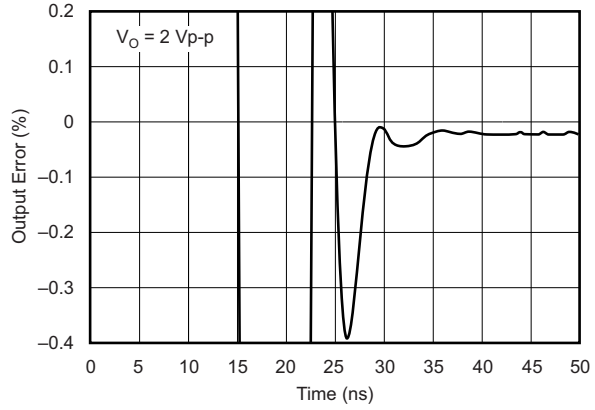


Figure 25. Output Settling Time to 0.1%

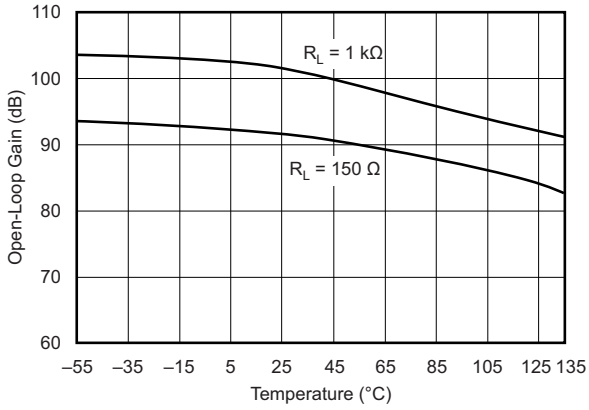


Figure 26. Open-Loop Gain vs Temperature

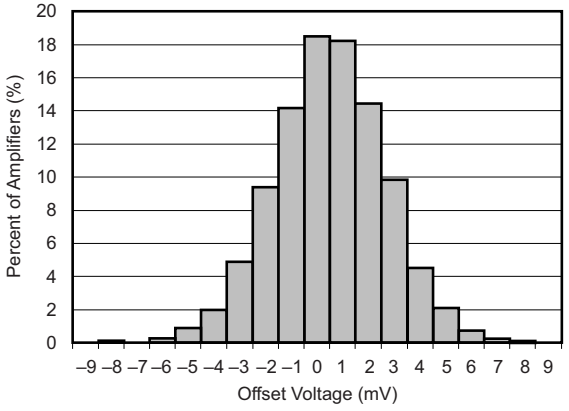


Figure 27. Offset Voltage Production Distribution

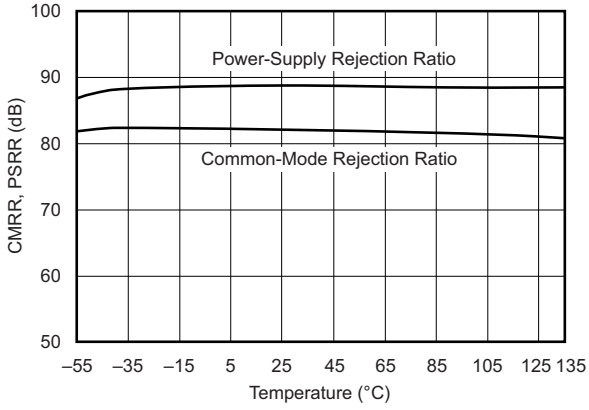


Figure 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

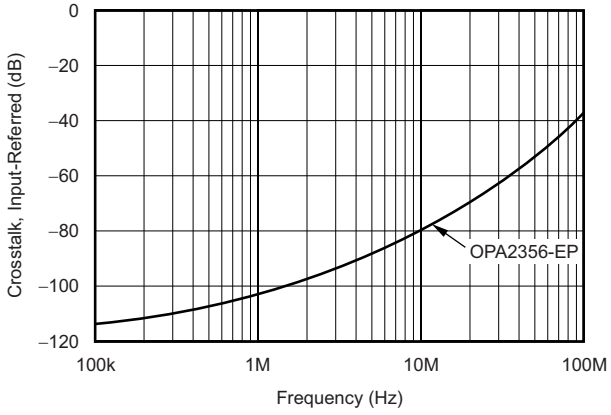


Figure 29. Channel-to-Channel Crosstalk

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7 Detailed Description

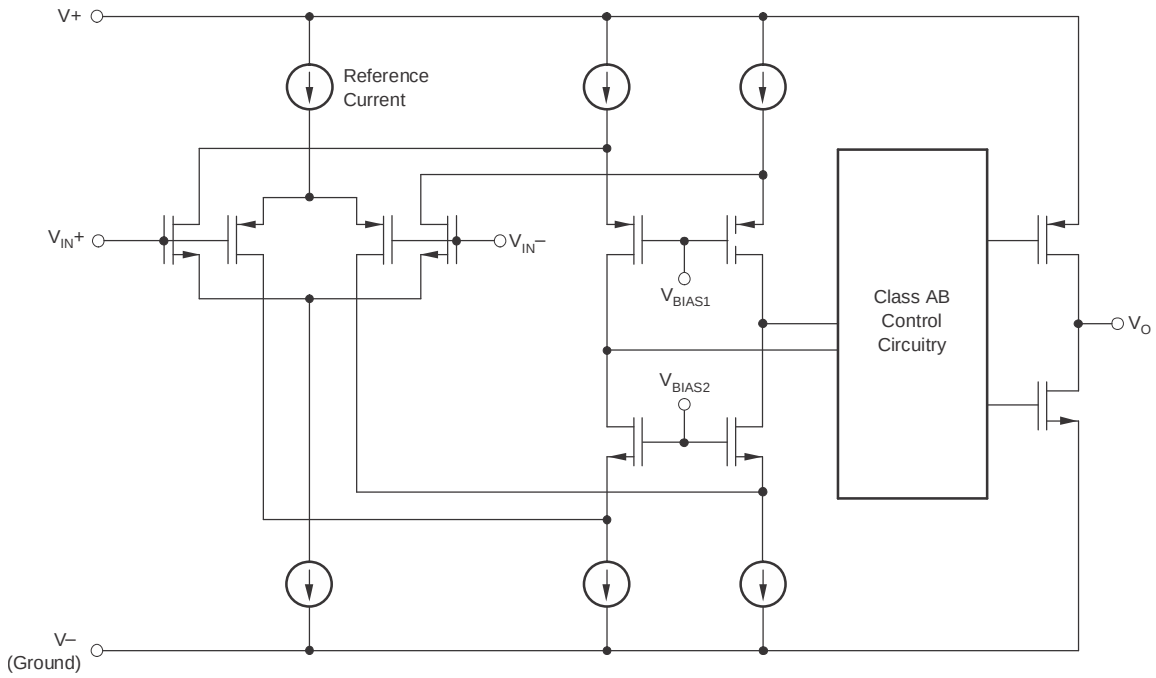
7.1 Overview

The OPA2356-EP is a CMOS, high-speed, voltage feedback, operational amplifier designed for video and other general-purpose applications. The OPA2356-EP is available as a dual op amp.

The amplifier features a 200-MHz gain bandwidth and 360-V/µs slew rate, but is unity-gain stable and can be operated as a 1-V/V voltage follower.

The OPA2356-EP input common-mode voltage range includes ground, allowing the amplifier to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Operating Voltage

The OPA2356-EP is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

7.3.2 Output Drive

The output stage of the OPA2356-EP is capable of driving a standard back-terminated 75-Ω video cable. A back-terminated transmission line does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents only a 150-Ω resistive load to the OPA2356-EP output.

The output stage can supply high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA2356-EP from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

NOTE

TI does not recommend running a continuous dc current in excess of ±60 mA. See Figure 20 in the *Typical Characteristics* section.

7.4 Device Functional Modes

The OPA2356-EP is powered on when the supply is connected. The device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application. The device can also be used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (for example, V– is set to –3.5 V and V+ is set to 1.5 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2356-EP is a CMOS, high-speed, voltage-feedback, operational amplifier (op amp) designed for general-purpose applications.

The amplifier features a 200-MHz gain bandwidth and 300-V/μs slew rate, but the device is unity-gain stable and operates as a 1-V/V voltage follower.

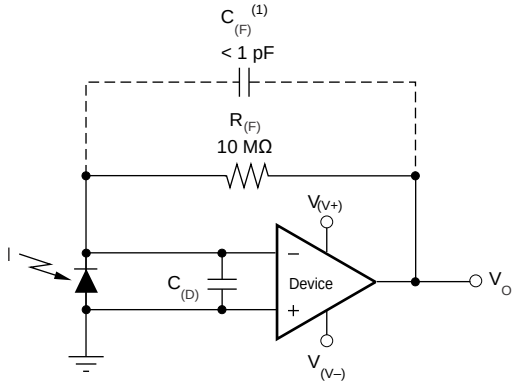
The input common-mode voltage range of the device includes ground, which allows the OPA2356-EP to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPA2356-EP a preferred wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 30, are the expected diode capacitance ($C_{(D)}$), which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF), the desired transimpedance gain ($R_{(FB)}$), and the gain-bandwidth (GBW) for the OPA2356-EP (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) is set to control the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 30. Dual-Supply Transimpedance Amplifier

8.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage $V_{(V+)}$	2.5 V
Supply voltage $V_{(V–)}$	–2.5 V

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the OPA2356 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 OPA2356-EP Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole must be set to:

$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (1)$$

Use Equation 2 to calculate the bandwidth.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (2)$$

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 31. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

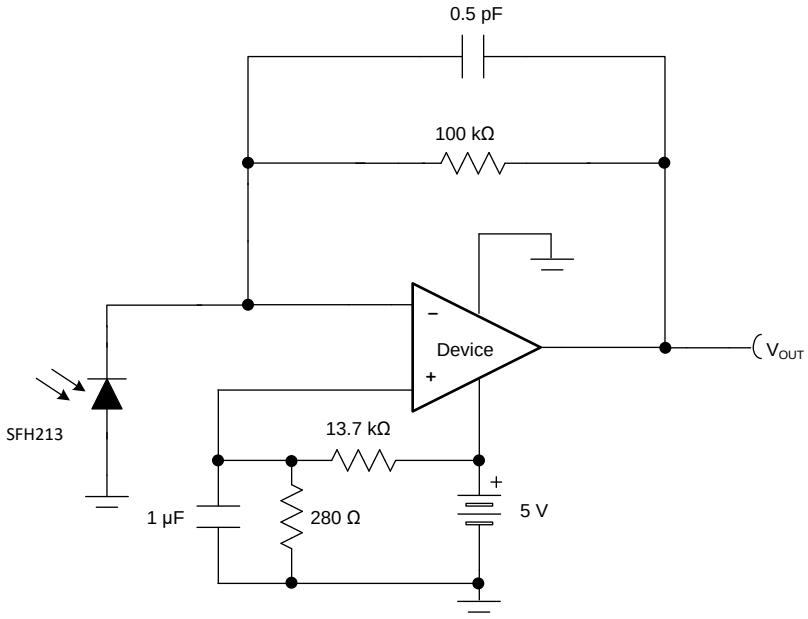


Figure 31. Single-Supply Transimpedance Amplifier

For additional information, see the *Compensate transimpedance amplifiers intuitively* application report.

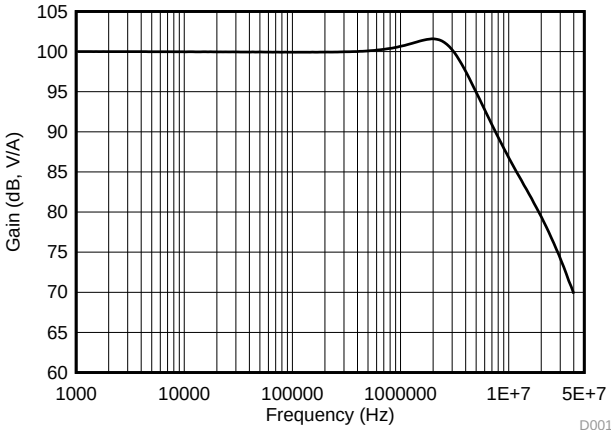
8.2.1.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, select components according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(FB)}$ increases with the square-root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, see the *Noise analysis of FET transimpedance amplifiers* and *Noise analysis for high-speed op amps* application reports.

8.2.1.3 Application Curve



–3-dB bandwidth is 4.56 MHz

Figure 32. AC Transfer Function

8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 33, where ($V_{(+INx)} = V_S – I_{(BIAS)} \times R_{(S)}$). The last term, $I_{(BIAS)} \times R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} \times R_{(S)}$ less than the input voltage noise of the amplifier, so that the input voltage noise does not become the dominant noise factor. The OPA2356-EP op amp features very low input bias current (typically 200 fA) and is therefore a preferred choice for such applications.

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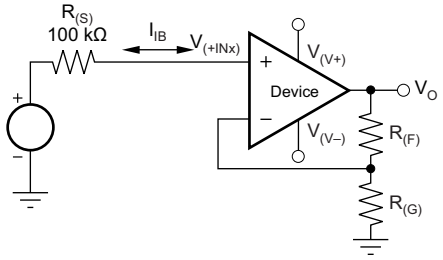
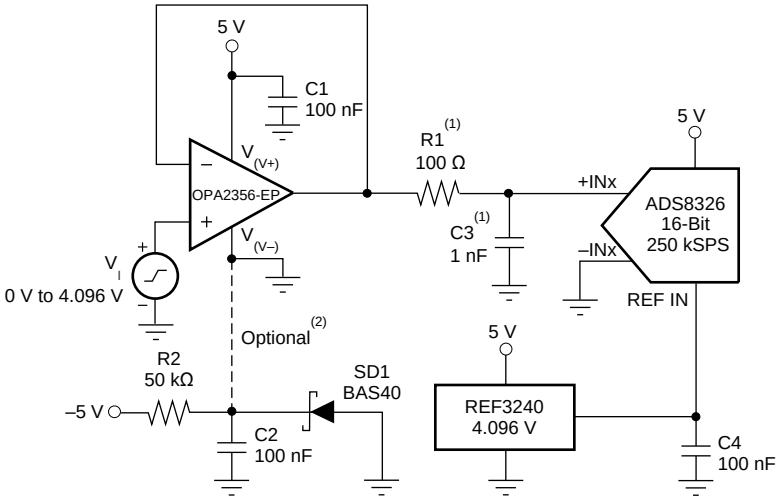


Figure 33. Noise as a Result of $I_{(BIAS)}$

8.2.3 Driving ADCs

The OPA2356-EP op amps are designed for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPA2356-EP to drive ADCs without degradation of differential linearity and THD.

The OPA2356-EP can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 34 shows the OPA2356-EP configured to drive the ADS8326.



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

Figure 34. Driving the ADS8326

8.2.4 Active Filter

The OPA2356-EP is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 35 depicts a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is preferred for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier,
2. Adding an additional second-order MFB stage,
3. Using a noninverting filter topology, such as the Sallen-Key (see Figure 36).

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MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's *FilterPro™* program. This software is available as a free download at www.ti.com.

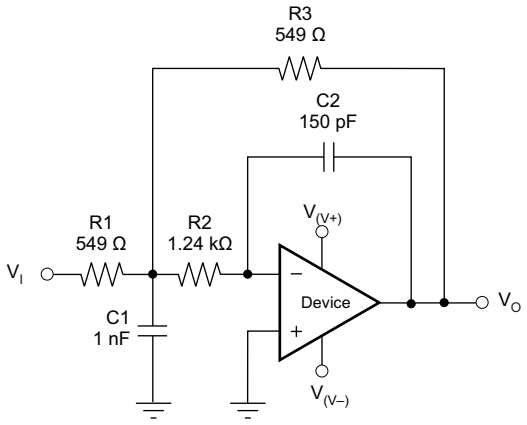


Figure 35. Second-Order Butterworth 500-kHz Low-Pass Filter

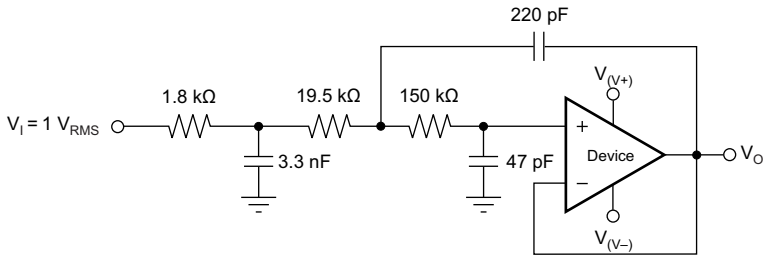


Figure 36. OPA2356-EP Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

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9 Power Supply Recommendations

The OPA2356-EP is specified for operation from 2.7 to 5.5 V (±1.35 to ±2.75 V); many specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

Power dissipation depends on power-supply voltage, signal, and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S – V_O$. Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

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10 Layout

10.1 Layout Guidelines

Good high-frequency PC board layout techniques should be employed for the OPA2356-EP. Generous use of ground planes, short direct signal traces, and a suitable bypass capacitor located at the V+ pin assure clean, stable operation. Large areas of copper also provide a means of dissipating heat that is generated within the amplifier in normal operation.

Sockets are not recommended for use with any high-speed amplifier.

A 10-µF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

10.2 Layout Example

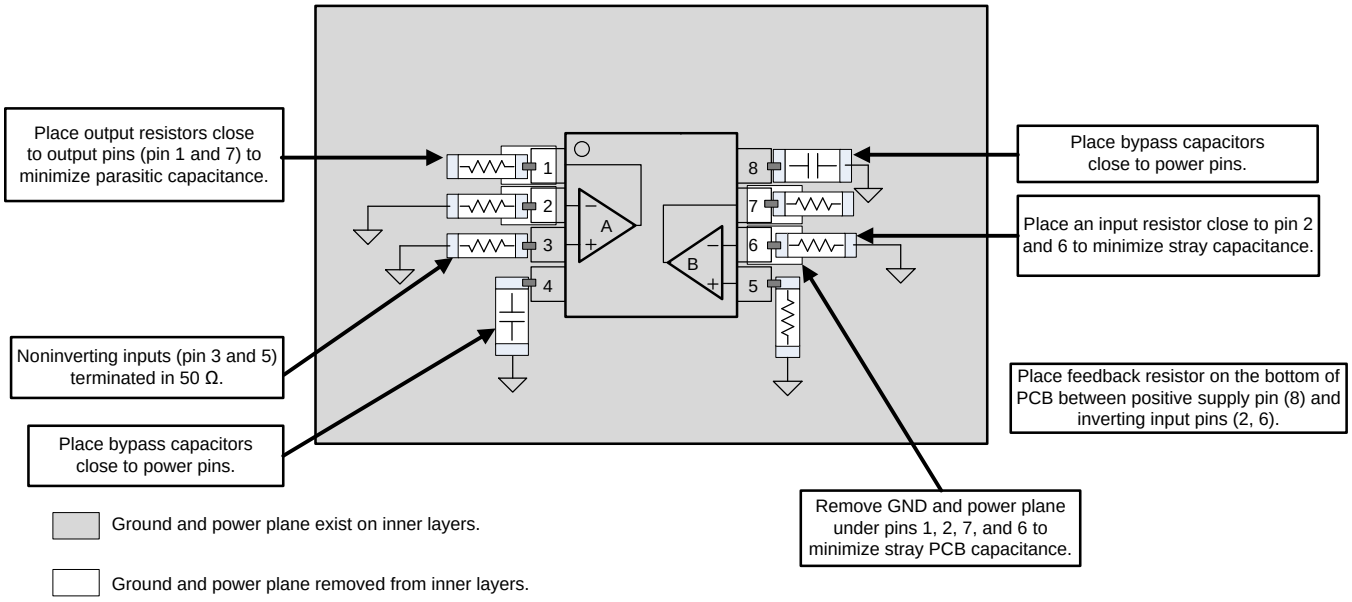


Figure 37. Example Layout

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《用直观方式补偿跨阻放大器》*应用报告
- 德州仪器 (TI)，*《FET 跨阻放大器噪声分析》*应用报告
- 德州仪器 (TI)，*《高速运算放大器噪声分析》*应用报告
- 德州仪器 (TI)，*《FilterPro™ 用户指南》*

11.2 接收文档更新通知

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2356MDGKREP	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-55 to 125	AYIH	Samples
OPA2356MDGKTEP	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-55 to 125	AYIH	Samples
V62/18609-01XE	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-55 to 125	AYIH	Samples
V62/18609-01XE-R	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-55 to 125	AYIH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

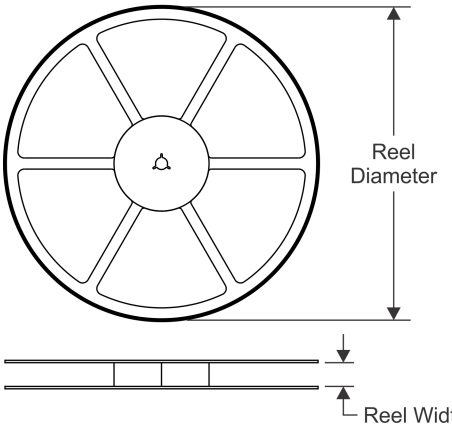
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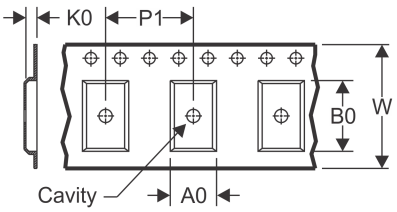
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

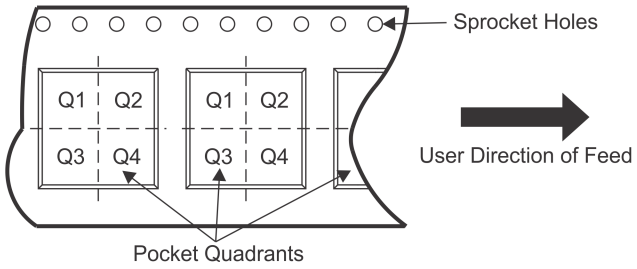


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

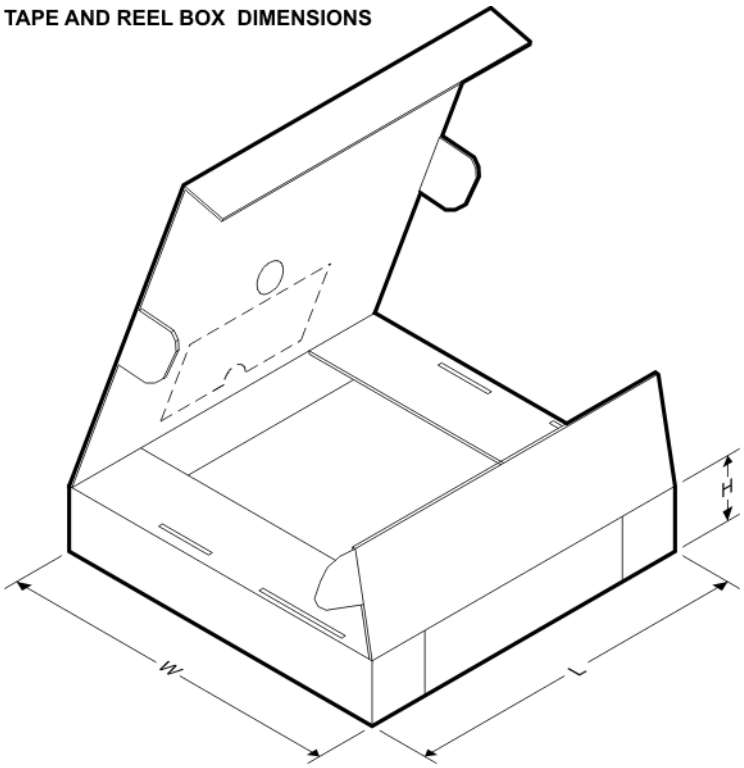
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2356MDGKREP	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

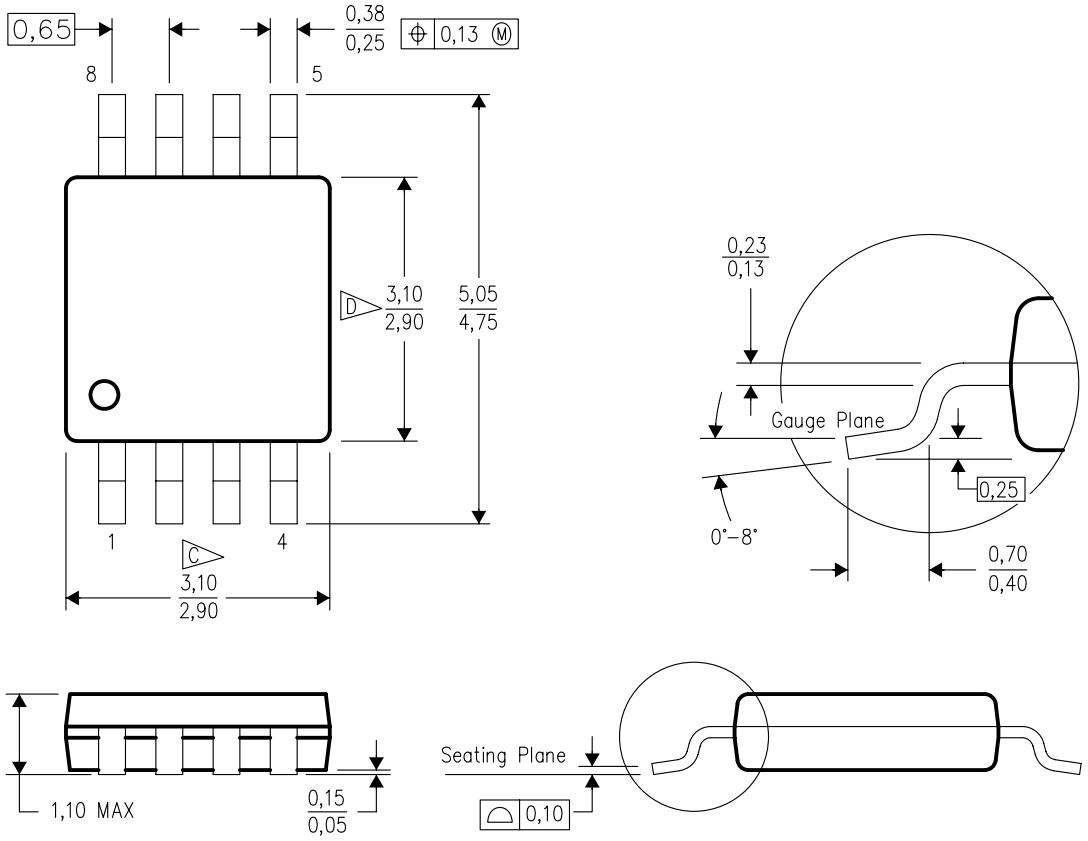
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2356MDGKREP	VSSOP	DGK	8	2500	367.0	367.0	35.0

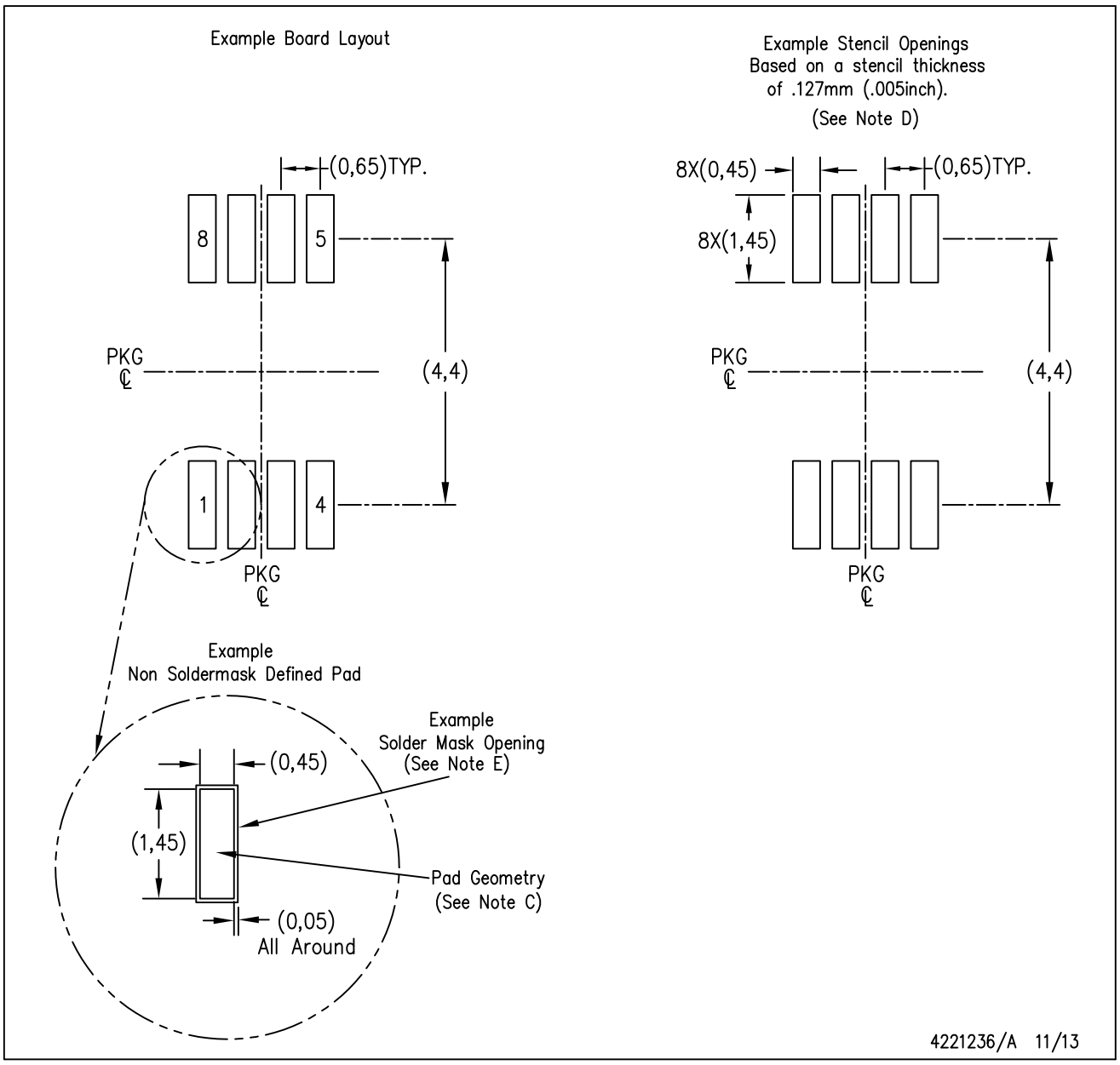
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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