BUF634A 210MHz、250mA 高速缓冲器

1 特性

- 引脚选择带宽：35MHz 至 210MHz
- 压摆率：3750V/µs
- 高输出电流：250mA
- 低静态电流：1.5mA（35MHz BW）
- 宽电源范围：±2.25V 至 ±18V
- 内部输出电流限制
- 热关断保护
- 采用 SOIC-8 封装
- 扩展工作温度范围：
  –40°C 至 +125°C

2 应用

- 存储器、显示器测试仪
- 耳机驱动器
- 运算放大器电流提升器
- 阀驱动器
- 电磁阀驱动器
- 线路驱动器
- 视频驱动器
- 电机驱动器
- 测试设备

3 说明

BUF634A 是一款建议用于各种应用的高速、单位增益、开环 缓冲器。BUF634A 是一款 36V 器件，通过在 V– 和 BW 引脚之间连接一个电阻器，可以在 35MHz 至 210MHz 范围内调节其带宽。BUF634A 可用于运算放大器的反馈环路内，以增大输出电流，消除热反馈，以及提高容性负载驱动能力。

对于低功耗 应用，BUF634A 具有 1.5mA 的工作静态电流以及 250mA 的输出、3750V/µs 的压摆率和 35MHz 带宽。该器件在宽带宽模式（带宽为 210MHz）下消耗 8.5mA 的静态电流。

BUF634A 支持 250mA 的大输出电流，并通过其输出级中的内部电流限制和热关断受到全面保护，使该器件非常耐用且易于使用。

BUF634A 是 BUF634 的升级版，与后者相比，前者具有 1.2 倍的带宽、更高的压摆率以及 4/7 的电源电流。如需了解如何选择德州仪器 (TI) 提供的单位增益开环缓冲器，请参阅*Device Comparison Table*。该器件可在 –40°C 至 +125°C 的扩展工业温度范围内正常运行。

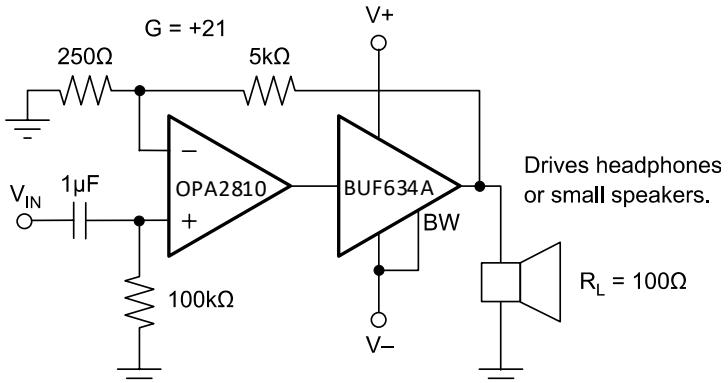
器件信息(1)

器件型号	封装	封装尺寸（标称值）
BUF634A	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADVANCE INFORMATION

提升任何运算放大器的输出电流



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年2 月	*	初始发行版。

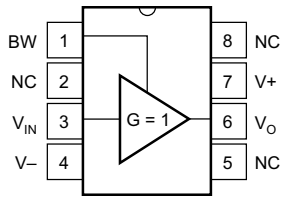
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5 Device Comparison Table

DEVICE	$V_{S\pm}$ (V)	I_Q / Channel (mA)	BW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
BUF634A	±18	1.5 – 8.5	35 – 210	3750	3.4	Unity-gain, open-loop buffer
BUF634	±18	1.5 – 15	30 – 180	2000	4	Unity-gain, open-loop buffer
LMH6321	±18	11	110	1800	2.8	Unity-gain, open-loop buffer with adjustable current limit

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BW	1	I	Bandwidth adjust pin. Connect the BW pin to the V– pin for wide-BW mode and leave the BW pin floating for low-I_Q mode.
NC	2, 5, 8	—	No internal connection
V–	4	I	Negative power supply
V+	7	I	Positive power supply
V_{IN}	3	I	Input
V_O	6	O	Output

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage		±20	V
V_{IN}	Input voltage		Vs ± 0.5	V
	Output short-circuit (to ground)		Continuous	
T_A	Operating ambient temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage	±2.25	±15	±18	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		BUF634A D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics: Wide-Bandwidth Mode

at T_A = 25°C, V_S = ±15 V, BW pin connected to V–, and R_L = 100 Ω connected to mid-supply (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	Bandwidth, –3 dB	R_L = 1 kΩ		210		MHz
		R_L = 100 Ω		200		
	Bandwidth for 0.1-dB flatness	V_O = 10 mV_{PP}, R_L = 100 Ω, R_S = 50 Ω		150		MHz
SR	Slew rate	V_O = 20-V step, R_L = 100 Ω, V_{IN}-SR = 4000 V/µs		3750		V/µs
	Rise and fall time	V_O = 200-mV step, R_L = 100 Ω		1		ns
	Settling time to 0.1%	V_O = 20-V step, R_L = 100 Ω, V_{IN}-SR = 2500 V/µs		90		ns
	Settling time to 1%	V_O = 20-V step, R_L = 100 Ω, V_{IN}-SR = 2500 V/µs		20		ns
e_n	Voltage noise	f = 10 kHz		3.4		nV/√Hz
e_i	Current noise	f = 10 kHz		0.85		pA/√Hz
HD2	2nd-harmonic distortion	V_O = 2 V_{PP}, f = 20 kHz, R_L = 100 Ω		–77		dBc
		V_O = 10 V_{PP}, f = 20 kHz, R_L = 100 Ω		–69		
HD3	3rd-harmonic distortion	V_O = 2 V_{PP}, f = 20 kHz, R_L = 100 Ω		–79		dBc
		V_O = 10 V_{PP}, f = 20 kHz, R_L = 100 Ω		–58		
DC PERFORMANCE						
V_{OS}	Input offset voltage	T_A = 25°C		35	60	mV
I_B	Input bias current	V_{IN} = 0 V		0.3	1.6	µA
G	Gain	V_O = ±10 V, R_L = 1 kΩ	0.95	0.99		V/V
		V_O = ±10 V, R_L = 100 Ω	0.92	0.95		
		V_O = ±10 V, R_L = 67 Ω	0.90	0.94		
INPUT						
	Linear input voltage range	R_L = 1 kΩ, I_B < 10 µA	–13		13	V
Z_{IN}	Input impedance	R_L = 100 Ω		150 || 5		MΩ || pF
OUTPUT						
V_{OH}	Output voltage range (high)	I_O = 10 mA	(V+)–1.9	(V+)–1.8		V
		I_O = 100 mA	(V+)–2.4	(V+)–2.3		
		I_O = 150 mA	(V+)–2.7	(V+)–2.6		
V_{OL}	Output voltage range (low)	I_O = –10 mA		(V–)+1.8	(V–)+1.9	V
		I_O = –100 mA		(V–)+2.3	(V–)+2.4	
		I_O = –150 mA		(V–)+2.6	(V–)+2.7	
I_O	Current output, continuous			±250		mA
I_{SC}	Short-circuit current			±400	±550	mA
Z_O	Output impedance	I_O = 10 mA		7		Ω
POWER SUPPLY						
V_S	Operating voltage range		±2.25		±18	V
I_Q	Quiescent current	I_O = 0 mA		8.5	12	mA
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V	60	80		dB
THERMAL SHUTDOWN						
T_J	Thermal shutdown temperature			175		°C

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7.6 Electrical Characteristics: Low-Quiescent Current Mode

at T_A = 25°C, V_S = ±15 V, BW pin left open, and R_L = 100 Ω connected to mid-supply (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	Bandwidth, –3 dB	R_L = 1 kΩ		35		MHz
		R_L = 100 Ω		31		
	Bandwidth for 0.1-dB flatness	V_O = 10 mV_{PP}, R_L = 100 Ω, R_S = 50 Ω		2.3		MHz
SR	Slew rate	V_O = 20-V step, R_L = 100 Ω, V_{IN}-SR = 4000 V/µs		3750		V/µs
	Rise and fall time	V_O = 200-mV step, R_L = 100 Ω		3		ns
	Settling time to 0.1%	V_O = 20-V step, R_L = 100 Ω, V_{IN}-SR = 2500 V/µs		400		ns
	Settling time to 1%	V_O = 20-V step, R_L = 100 Ω, V_{IN}-SR = 2500 V/µs		90		ns
e_n	Voltage noise	f = 10 kHz		8.1		nV/√Hz
e_i	Current noise	f = 10 kHz		0.3		pA/√Hz
HD2	2nd-harmonic distortion	V_O = 2 V_{PP}, f = 20 kHz, R_L = 100 Ω		–54		dBc
		V_O = 10 V_{PP}, f = 20 kHz, R_L = 100 Ω		–65		
HD3	3rd-harmonic distortion	V_O = 2 V_{PP}, f = 20 kHz, R_L = 100 Ω		–40		dBc
		V_O = 10 V_{PP}, f = 20 kHz, R_L = 100 Ω		–45		
DC PERFORMANCE						
V_{OS}	Input offset voltage	T_A = 25°C		35	60	mV
I_B	Input bias current	V_{IN} = 0 V		0.03	0.25	µA
G	Gain	V_O = ±10 V, R_L = 1 kΩ	0.95	0.99		V/V
		V_O = ±10 V, R_L = 100 Ω	0.92	0.95		
		V_O = ±10 V, R_L = 67 Ω	0.90	0.94		
INPUT						
	Linear input voltage range	R_L = 1 kΩ, I_B < 10 µA	–13		13	V
Z_{IN}	Input impedance	R_L = 100 Ω		1000 || 5		MΩ || pF
OUTPUT						
V_{OH}	Output voltage range (high)	I_O = 10 mA	(V+)–1.9	(V+)–1.8		V
		I_O = 100 mA	(V+)–2.4	(V+)–2.3		
		I_O = 150 mA	(V+)–2.7	(V+)–2.6		
V_{OL}	Output voltage range (low)	I_O = –10 mA		(V–)+1.8	(V–)+1.9	V
		I_O = –100 mA		(V–)+2.3	(V–)+2.4	
		I_O = –150 mA		(V–)+2.6	(V–)+2.7	
I_O	Current output, continuous			±250		mA
I_{SC}	Short-circuit current			±350	±550	mA
Z_O	Output impedance	I_O = 10 mA		7		Ω
POWER SUPPLY						
V_S	Operating voltage range		±2.25		±18	V
I_Q	Quiescent current	I_O = 0		1.5	2.3	mA
PSRR	Power-supply rejection ratio	V_S = ±2.25 V to ±18 V	60	80		dB
THERMAL SHUTDOWN						
T_J	Thermal shutdown temperature			175		°C

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8 Detailed Description

8.1 Overview

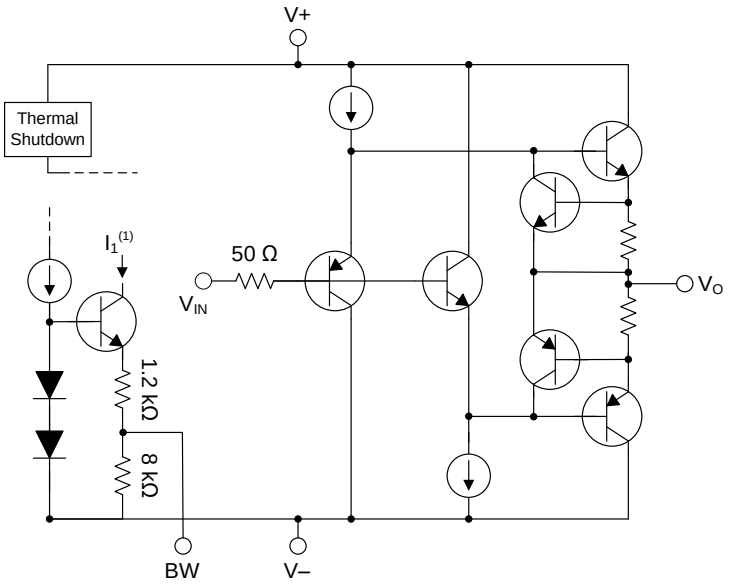
The BUF634A is a high-speed, unity-gain, open-loop buffer recommended for a wide range of applications with large output current and large slew rate requirements. The device is a 36-V buffer with bandwidth adjustable from 35 MHz to 210 MHz by connecting a resistor between the V– and BW pins. See the *Adjustable Bandwidth* section for a description of the relationship between bandwidth adjustment resistance and the device –3-dB bandwidth.

The BUF634A consumes only 1.5 mA of quiescent current with a 35-MHz bandwidth in low-quiescent current mode and 8.5 mA of quiescent current with a 210-MHz bandwidth in wide-bandwidth mode. This power scaling with bandwidth makes the device suitable for use in portable battery-powered applications. The BUF634A is suitable for use in applications requiring large output drive and slew rate, and includes an internal current limit and thermal shutdown, making the device rugged for such applications.

The BUF634A can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive. With a large slew rate of 3750 V/µs, the BUF634A can quickly reproduce its input signal at its output without adding considerable delay when used in a composite loop with another amplifier. When used in such a circuit, the outer amplifier controls the circuit precision and distortion performance and the buffer augments the circuit output current drive capability and only introduces a small additional phase shift for an overall acceptable phase margin.

See the *Functional Block Diagram* section for a simplified circuit diagram of the open-loop complementary follower design of the BUF634A.

8.2 Functional Block Diagram



(1) Stage currents are set by I_1.

ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Output Current

The BUF634A can deliver up to ±250-mA continuous output current. Internal circuitry limits output current to approximately ±350 mA. For many applications, however, the continuous output current is limited by thermal effects. The output voltage swing capability varies with junction temperature and output current. Care must be taken to operate the device below the maximum-recommended junction temperature in applications using this buffer in wide-bandwidth mode with a wide supply voltage and large output current to avoid permanent damage to the device.

8.3.2 Adjustable Bandwidth

The BUF634A –3-dB bandwidth can be adjusted from 35 MHz to 210 MHz for a 1-kΩ load resistance, as shown in 图 1 by connecting a resistor between the V– and BW pins. The bandwidth is set to 210 MHz with the BW pin connected to V– and to 35 MHz with the BW pin left floating. The –3-dB bandwidth also changes with the value of the load resistance for a given bandwidth adjustment resistance. The device quiescent current varies from 1.5 mA (typ) to 8.5 mA (typ) as the bandwidth varies 35 MHz to 210 MHz, respectively.

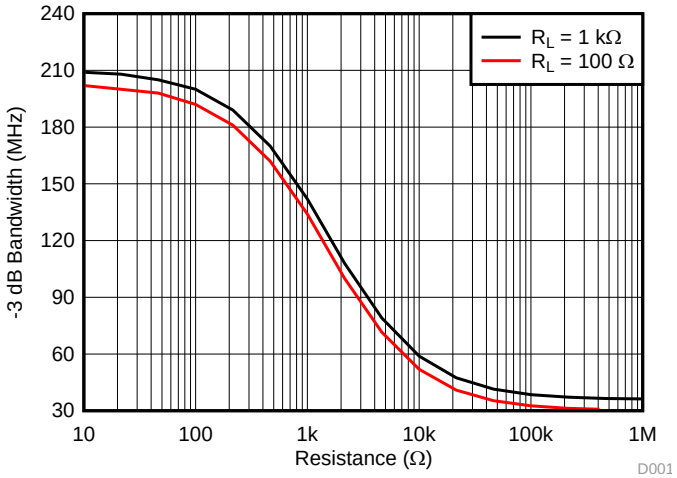


图 1. Small-Signal Bandwidth vs Bandwidth Adjustment Resistance

8.3.3 ESD Protection

As shown in 图 2, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous currents. Current limiting series resistors must be added at the inputs if common-mode voltages higher than the supply voltages are possible. Keep these resistor values as low as possible because using high values degrades noise performance and frequency response.

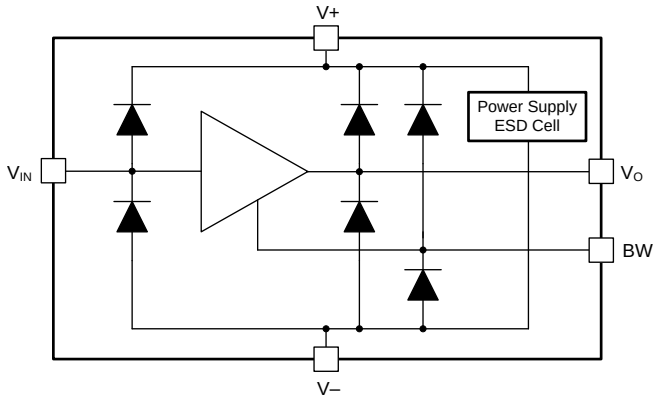


图 2. Internal ESD Protection

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8.4 Device Functional Modes

The BUF634A is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum-recommended supply voltage for the BUF634A is 36 V (±18 V). At low power-supply conditions, such as ±2.25 V, the output swing may be limited. See the output voltage range specifications in the *Electrical Characteristics: Wide-Bandwidth Mode* and *Electrical Characteristics: Low-Quiescent Current Mode* tables for additional information.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

图 3 shows the BUF634A connected as an open-loop buffer. The source impedance and optional input resistor, R_S, influence frequency response. Bypass power supplies with capacitors connected close to the device pins. Capacitor values as low as 0.1 µF assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies. Solid tantalum 10-µF capacitors are recommended. High-frequency, open-loop applications can benefit from special bypassing and layout considerations. See the *High-Frequency Applications* section for more information.

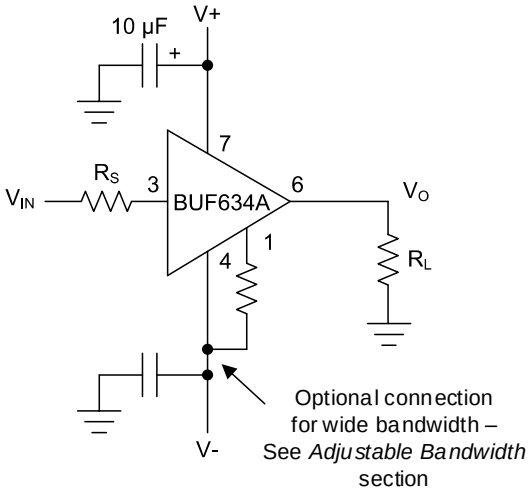


图 3. Buffer Connections

9.1.1 High-Frequency Applications

The excellent bandwidth and fast slew rate of the BUF634A are useful in a variety of high-frequency, open-loop applications. When operated in an open-loop application, printed circuit board (PCB) layout and bypassing techniques can affect dynamic performance. 图 4 through 图 8 illustrate various application circuit examples for the BUF634A.

For best results, use a ground-plane-type circuit board layout and bypass the power supplies with 0.1-µF ceramic chip capacitors at the device pins in parallel with solid tantalum 10-µF capacitors. Source resistance affects high-frequency peaking, step-response overshoot, and ringing. Best response is usually achieved with a series input resistor of 25 Ω to 200 Ω, depending on the signal source. Response with some loads (especially capacitive) can be improved with a resistor of 10 Ω to 150 Ω in series with the output. When driving multiple device under test (DUT) inputs in automatic test equipment (ATE) testers (large capacitive load), as illustrated in 图 5, place an isolation resistor at the output of the BUF634A for adequate phase margin and stability.

ADVANCE INFORMATION

Application Information (接下页)

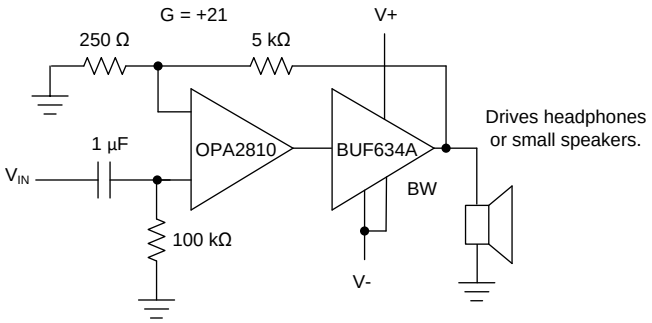


图 4. High-Performance Headphone Driver

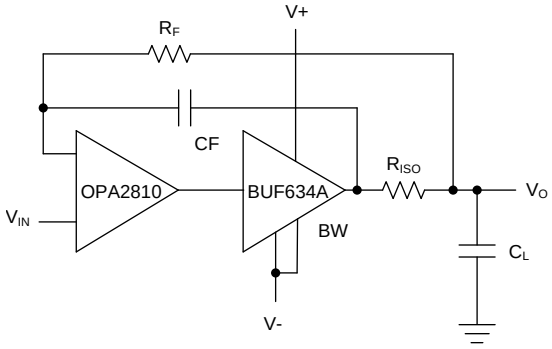


图 5. ATE and Test Pin Driver

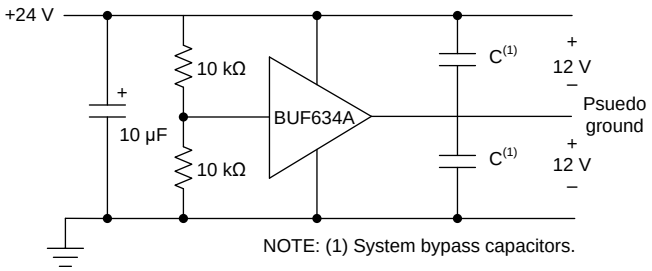


图 6. Pseudo-Ground Driver

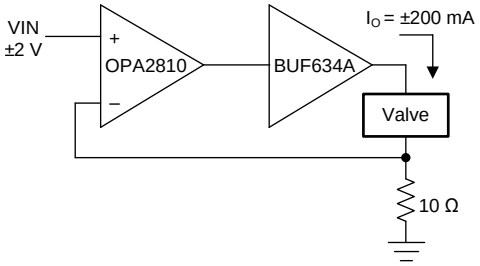


图 7. Current-Output Valve Driver

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Application Information (接下页)

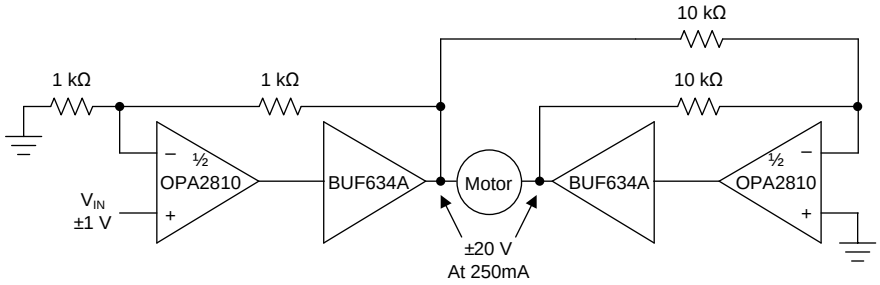
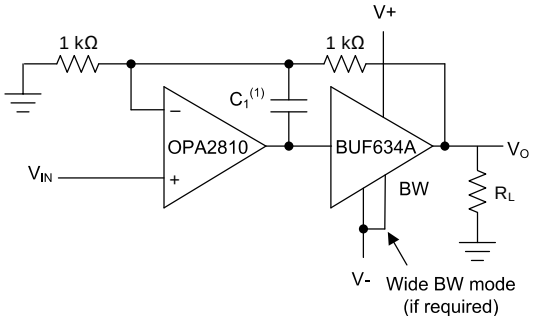


图 8. Bridge-Connected Motor Driver

9.2 Typical Application

The BUF634A can be connected inside the feedback loop, as shown in 图 9, of most op amps to increase output current. When connected inside the feedback loop, the offset voltage of the BUF634A and other errors are corrected by the open-loop gain and feedback of the op amp.



(1) C_1 is not required for most common op amps. Use C_1 with unity-gain stable, high-speed op amps.

图 9. Boosting Op Amp Output Current

9.2.1 Design Requirements

- Boost the output current of an OPA2810
- Operate from ±12-V power supplies
- Operate from –40°C to +125°C
- Gain = 2 V/V
- Output current = ±250 mA
- Bandwidth greater than 100 kHz

9.2.2 Detailed Design Procedure

To assure that the composite amplifier remains stable, the phase shift of the BUF634A must remain small throughout the loop gain of the circuit. For a G = +1 op-amp circuit, the BUF634A must contribute little additional phase shift (approximately 20° or less) at the unity-gain frequency of the op amp. Phase shift is affected by various operating conditions that can affect the stability of the op amp.

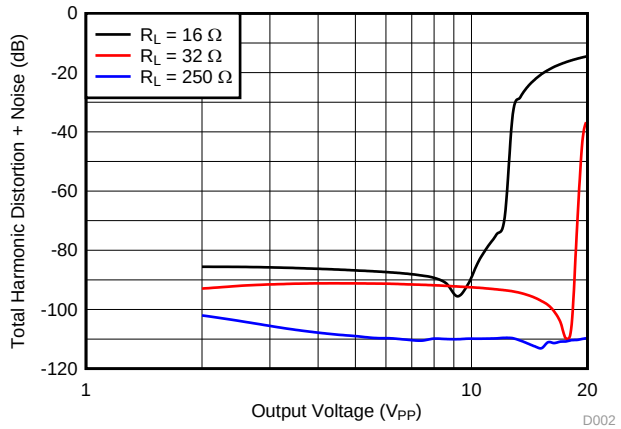
For the circuit in 图 9, most general-purpose or precision op amps remain unity-gain stable with the BUF634A connected inside the feedback loop. Large capacitive loads may require the BUF634A to be connected for wide bandwidth for stable operation. High-speed or fast-settling op amps generally require wide-bandwidth mode to remain stable and to assure good dynamic performance. Check for oscillations or excessive ringing on signal pulses with the intended load and worst-case conditions that affect phase response of the buffer to determine stability with an op amp. Connect the circuit as illustrated in 图 9. Choose resistors to provide a voltage gain of 2 V/V. Select the feedback resistor to be 1 kΩ. Choose the input resistor to be 1 kΩ and C_1 to be 10 pF. 图 10 and 图 11 show the THD+N plots for the BUF634A used with the OPA2810 in a gain of

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Typical Application (接下页)

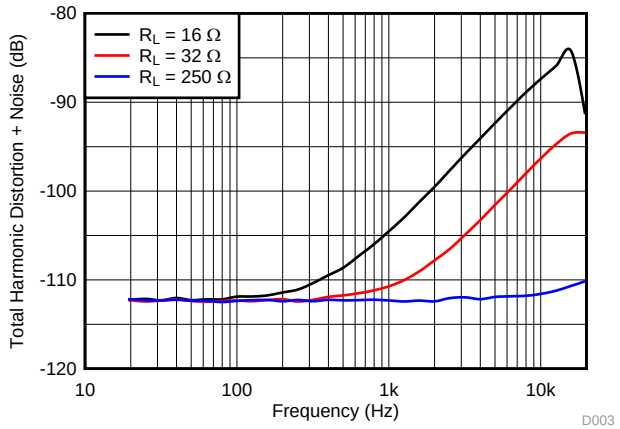
2-V/V composite loop. The THD+N performance is superior in a composite loop when compared with a standalone BUF634A because of the negative feedback and open-loop gain of the OPA2810. In 图 10, the signal distortion degrades for large output voltages with 16-Ω and 32-Ω loads because of the device internal short-circuit protection.

9.2.3 Application Curves



f = 20 kHz, 90-kHz measurement bandwidth

图 10. THD+N vs Output Voltage Using the BUF634A With the OPA2810



V_O = 10 V_{PP}, 90-kHz measurement bandwidth

图 11. THD+N vs Frequency Using the BUF634A With the OPA2810

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10 Power Supply Recommendations

The BUF634A is intended for operation on supplies ranging from 4.5 V to 36 V (±2.25 V to ±18 V). The BUF634A can be operated on single-sided supplies, split, and balanced bipolar supplies or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors resulting from the –PSRR term can be minimized. Minimize the distance (< 0.1") from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. A larger capacitor (10 µF typical) is used along with a high-frequency, 0.1-µF supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split-supply is used, use these capacitors from each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the PCB.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see the *Circuit board layout techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible, as illustrated in 图 12.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Power dissipated in the BUF634A causes the junction temperature to rise. A thermal protection circuit in the BUF634A disables the output when the junction temperature reaches approximately 175°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. Quiescent current is approximately 12 mA during thermal shutdown. When the junction temperature cools to approximately 160°C, the output circuitry is again enabled. This process can cause the protection circuit to cycle on and off with a period ranging from a fraction of a second to several minutes or more, depending on package type, signal, load, and thermal environment.

The thermal protection circuit is designed to prevent damage during abnormal conditions. Any tendency to activate the thermal protection circuit during normal operation is a sign of an inadequate heat sink or excessive power dissipation for the package type.

The SOIC-8 surface-mount package is excellent for applications requiring high output current with low average power dissipation. To achieve the best possible thermal performance with the SOIC-8 package, solder the device directly to a circuit board. Sockets degrade thermal performance because much of the heat is dissipated by conduction through the package pins. Use wide circuit board traces on all device pins, including pins that are not connected. For more information on designing the circuit board, see the *BUF634AD Evaluation module* user's guide.

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Layout Guidelines (接下页)

11.1.1 Power Dissipation

Power dissipation depends on power-supply voltage, signal, and load conditions. A part of this dissipation is because of the device quiescent current. There is additional power dissipation in the buffer output stage because of the output current. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S – V_O$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power supply voltage. Dissipation with AC signals is lower. The *Power amplifier stress and power handling limitations* application note explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered. The thermal protection must trigger more than 45°C above the maximum expected ambient condition of your application.

11.2 Layout Example

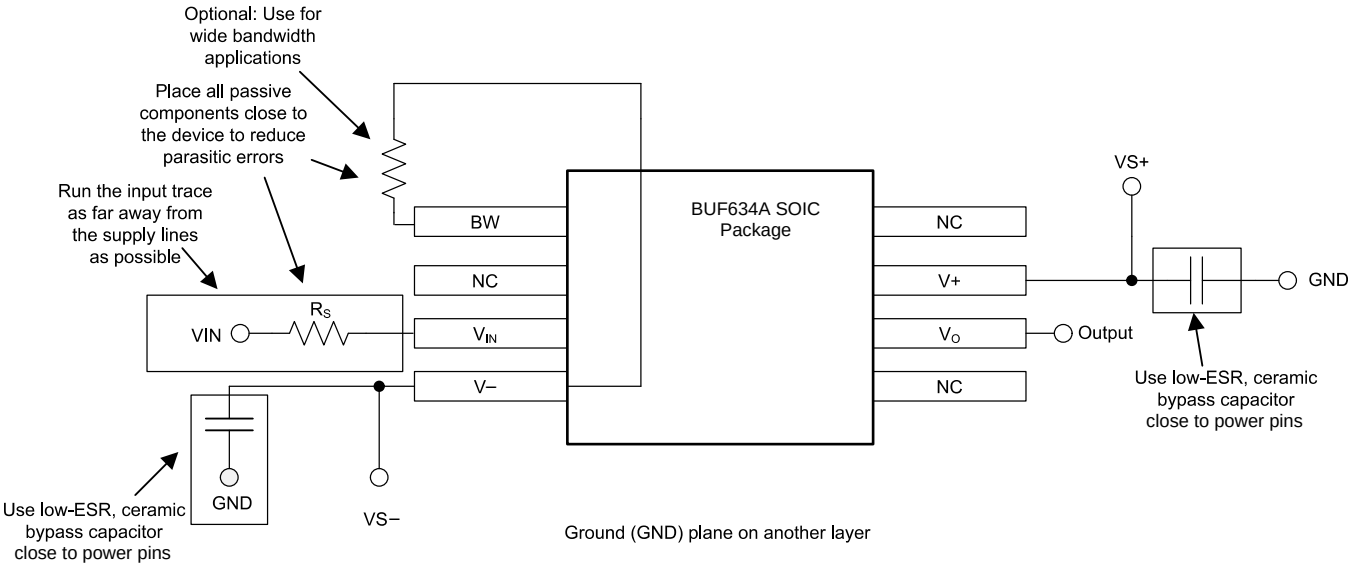


图 12. BUF634A Layout Example

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12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流 (DC)、瞬态和频域分析以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

12.1.1.2 TI 高精度设计

BUF634A 采用多种 TI 高精度设计，有关内容，请访问 www.ti.com.cn。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《OPA2810 双通道、27V、轨至轨输入/输出 FET 输入运算放大器》数据表*
- 德州仪器 (TI)，*《BUF634AD 评估模块》用户指南*
- 德州仪器 (TI)，*《电路板布局技巧》应用手册*
- 德州仪器 (TI)，*《组合放大器与 BUF634》应用手册*
- 德州仪器 (TI)，*《向 BUF634 添加电流限制》应用手册*
- 德州仪器 (TI)，*《功率放大器应力和功率处理限制》应用手册*
- 德州仪器 (TI)，*《无铅组件涂层的储存寿命评估》应用报告*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

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12.6 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF634AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BF634A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

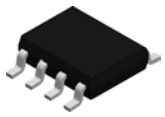
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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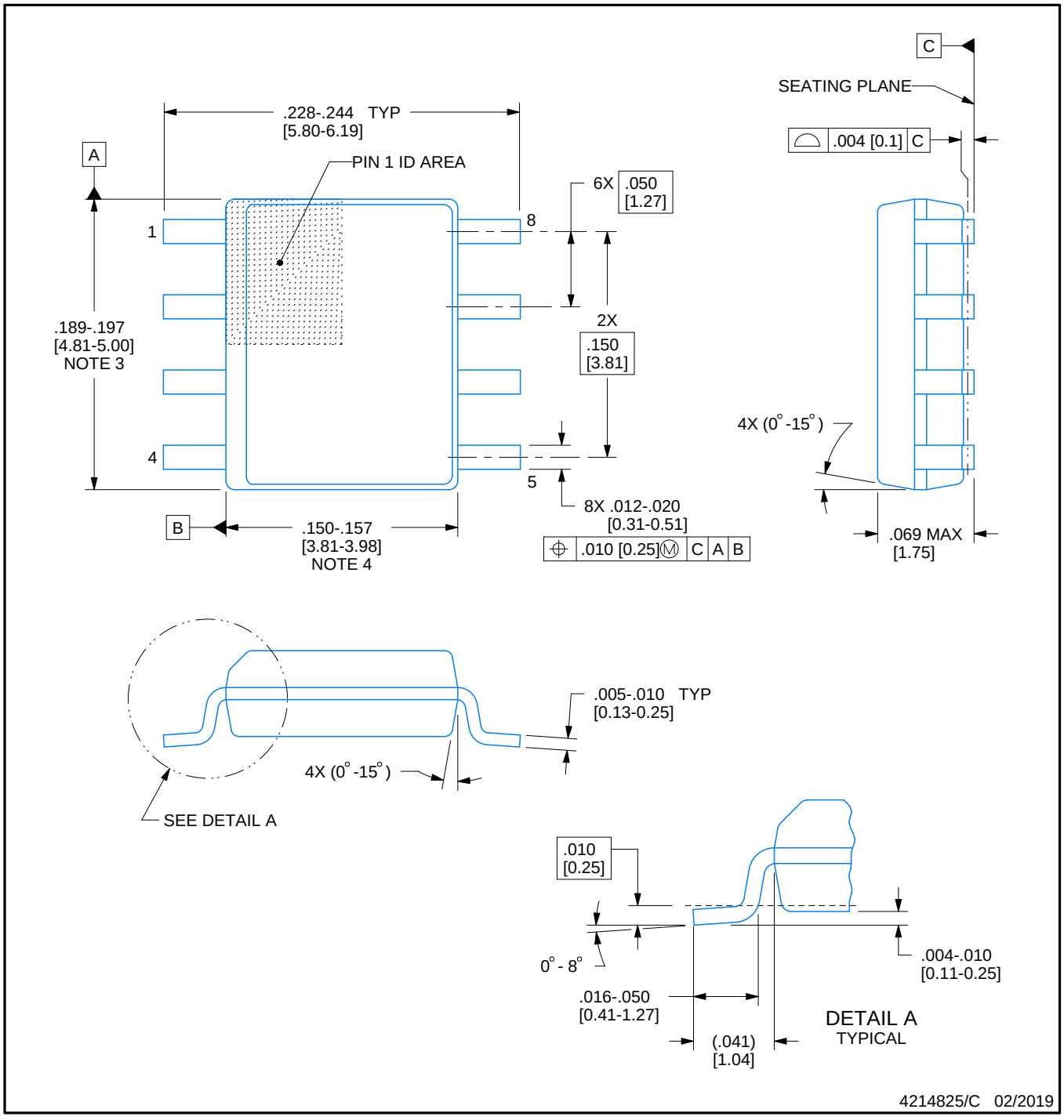


PACKAGE OUTLINE

D0008A

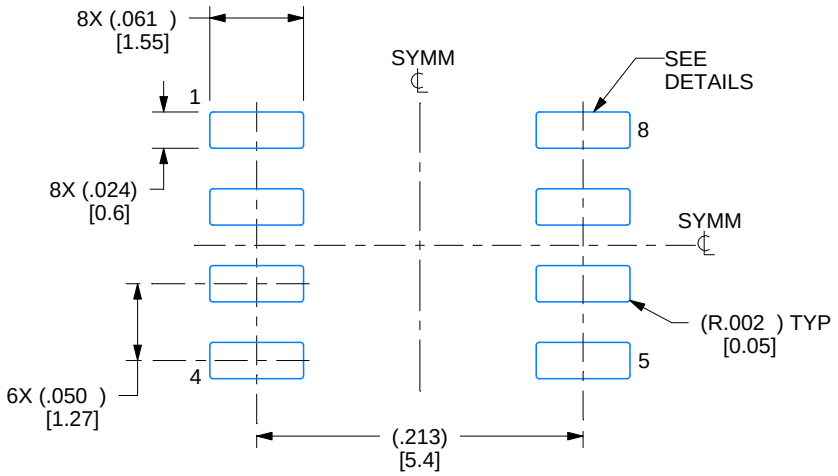
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

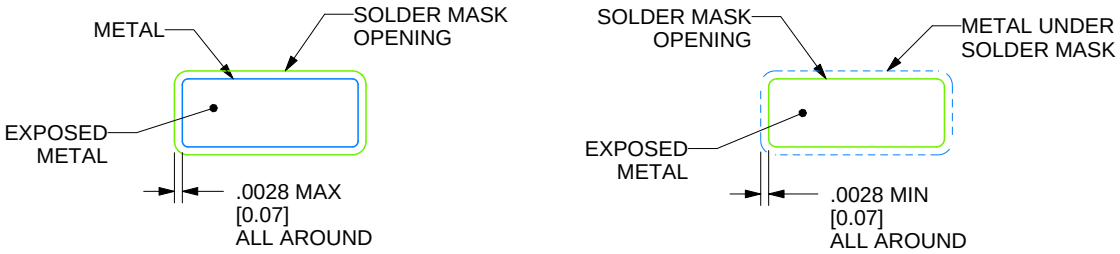


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

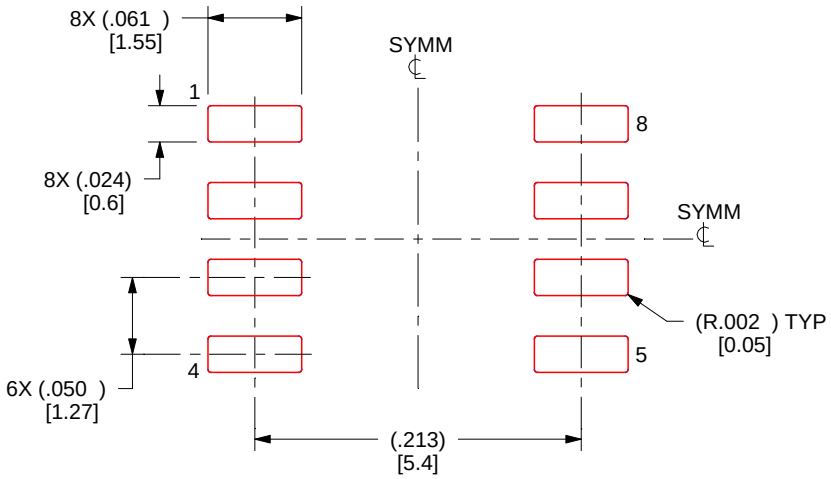
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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