

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

TLV2352, TLV2352Y

SLCS011B – MAY 1992 – REVISED MARCH 1999

- Wide Range of Supply Voltages
2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Very-Low Supply-Current Drain
120 μ A Typ at 3 V
- Output Compatible With TTL, MOS, and CMOS
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- High Input Impedance . . . $10^{12} \Omega$ Typ
- Extremely Low Input Bias Current
5 pA Typ
- Common-Mode Input Voltage Range
Includes Ground
- Built-In ESD Protection

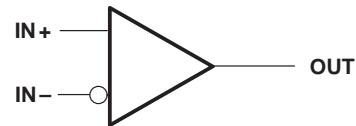
description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and operates with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μ A.

The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352I is fully characterized at 3 V and 5 V for operation from -40°C to 85°C . The TLV2352M is fully characterized at 3 V and 5 V for operation from -55°C to 125°C .

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 1000-V ESD rating using Human Body Model testing. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

symbol (each comparator)



AVAILABLE OPTIONS

T _A	V _{IO} max at 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D) [†]	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW) [‡]	PLASTIC DIP (U)	
-40°C to 85°C	5 mV	TLV2352ID	—	—	TLV2352IP	TLV2352IPWLE	—	TLV2352Y
-55°C to 125°C	5 mV	—	TLV2352MFK	TLV2352MJG	—	—	TLV2352MU	

[†] The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).

[‡] The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE)



These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

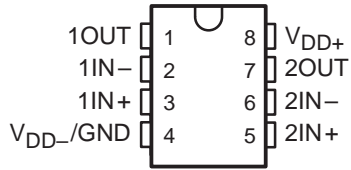
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

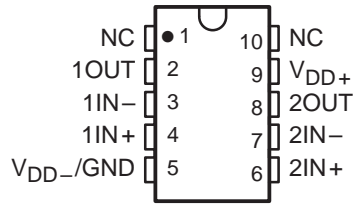
TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

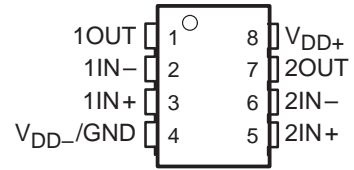
**TLV2352I . . . D OR P PACKAGE
TLV2352M . . . JG PACKAGE
(TOP VIEW)**



**TLV2254M
U PACKAGE
(TOP VIEW)**

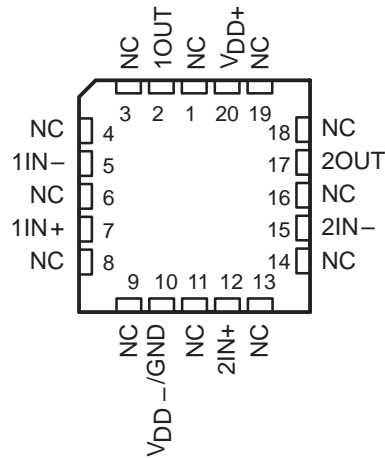


**TLV2352I . . . PW PACKAGE
(TOP VIEW)**



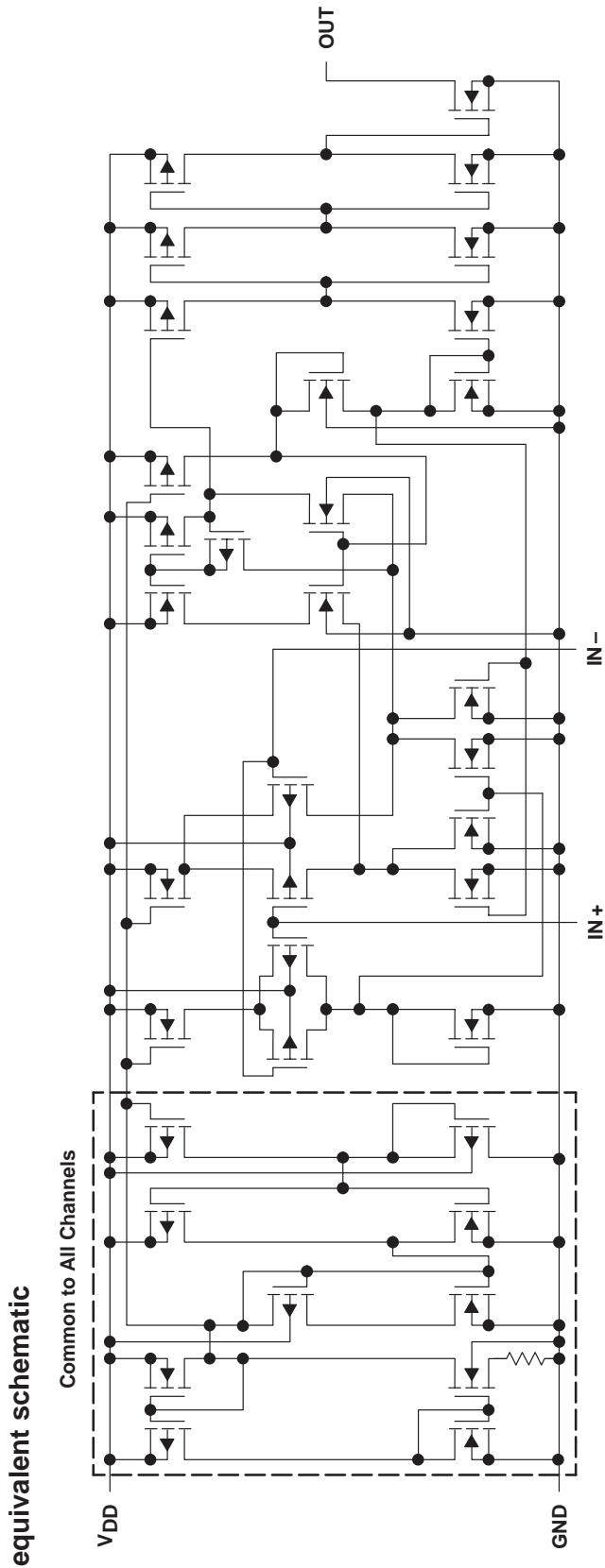
NC – No internal connection

**TLV2352M
FK PACKAGE
(TOP VIEW)**



TLV2352, TLV2352Y
LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

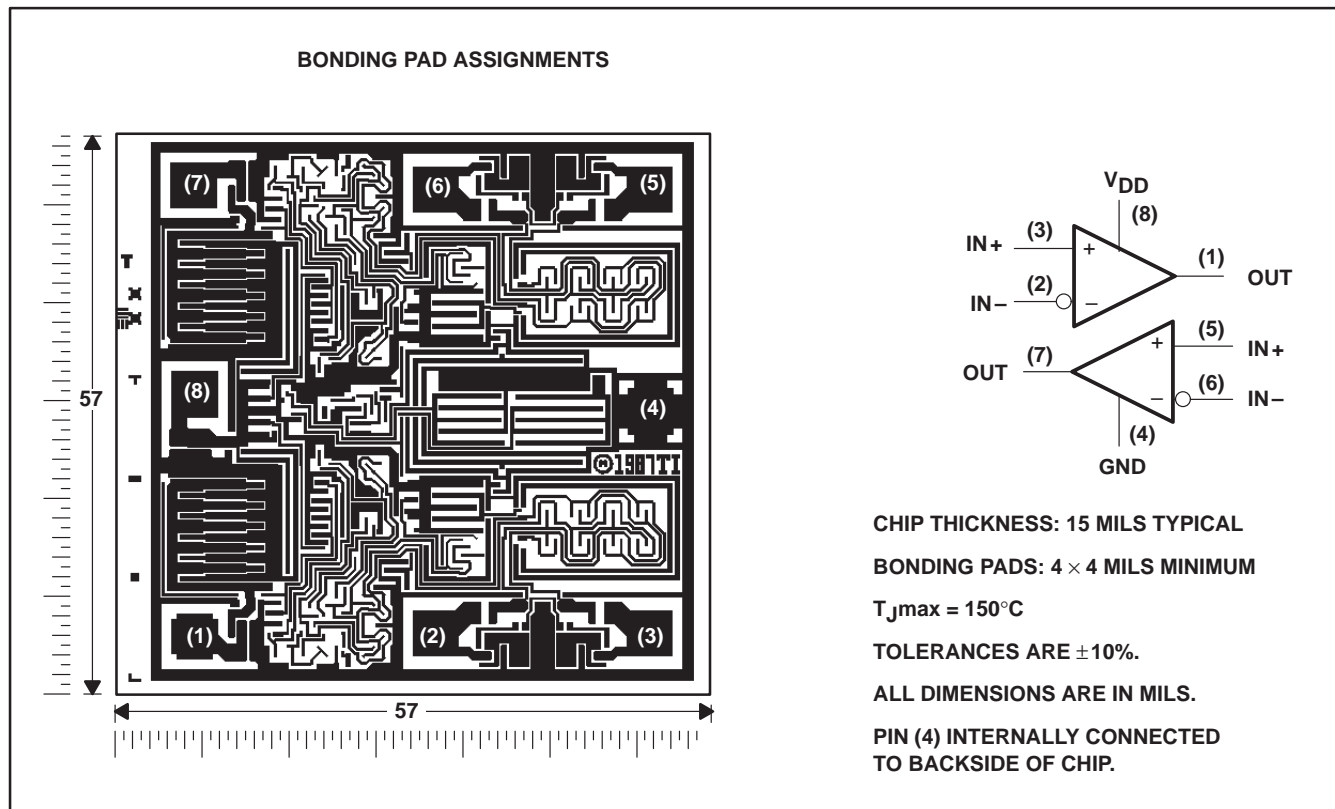


TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip can be mounted with conductive epoxy or a gold-silicon preform.



TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	± 8 V
Input voltage range, V_I	–0.3 to 8 V
Output voltage, V_O	8 V
Input current, I_I	± 5 mA
Output current, I_O	20 mA
Duration of output short-circuit current to GND (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2352I	–40°C to 85°C
TLV2352M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, and PW Packages	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FK, JG, and U Packages	300°C

† Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 2. Differential voltages are at IN+ with respect to IN–.
 3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	—
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	—
PW	525 mW	4.2 mW/°C	273 mW	—
U	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	0	1.75	V
	$V_{DD} = 5$ V	0	3.75	
Operating free-air temperature, T_A	TLV2352I	–40	85	°C
	TLV2352M	–55	125	



TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T _A ‡	TLV2352I						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = V _{ICRmin} , See Note 4	25°C	1		5	1		5	mV
		Full range	7			7			
I _{IO} Input offset current		25°C	1			1			pA
		85°C			1			1	nA
I _{IB} Input bias current		25°C	5			5			pA
		85°C			2			2	nA
V _{ICR} Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I _{OH} High-level output current	V _{ID} = 1 V	25°C	0.1			0.1			nA
		Full range	1			1			μA
V _{OL} Low-level output voltage	V _{ID} = -1 V, I _{OL} = 2 mA	25°C	115		300	150		400	mV
		Full range	600			700			
I _{OL} Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	6	16		6	16		mA
I _{DD} Supply current	V _{ID} = 1 V, No load	25°C	120		250	140		300	μA
		Full range	350			400			

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

‡ Full range is -40°C to 85°C. IMPORTANT: See *Parameter Measurement Information*.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352I			UNIT
		MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, C _L = 15 pF§, See Note 5 100-mV input step with 5-mV overdrive	640			ns

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352I			UNIT
		MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, C _L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive			ns
		TTL-level input step			

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.



TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T _A ‡	TLV2352M						UNIT
			V _{DD} = 3 V			V _{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = V _{ICRmin} , See Note 4	25°C	1		5	1		5	mV
		Full range				10			
I _{IO} Input offset current		25°C	1			1			pA
		125°C				10			nA
I _{IB} Input bias current		25°C	5			5			pA
		125°C				20			nA
V _{ICR} Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I _{OH} High-level output current	V _{ID} = 1 V	25°C	0.1			0.1			nA
		Full range				1			μA
V _{OL} Low-level output voltage	V _{ID} = -1 V, I _{OL} = 2 mA	25°C	115		300	150		400	mV
		Full range				700			
I _{OL} Low-level output current	V _{ID} = -1 V, V _{OL} = 1.5 V	25°C	6	16		6	16	mA	
I _{DD} Supply current	V _{ID} = 1 V, No load	25°C	120		250	140		300	μA
		Full range				400			

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

‡ Full range is -55°C to 125°C. IMPORTANT: See *Parameter Measurement Information*.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352M			UNIT
		MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, C _L = 100 pF§, See Note 5 100-mV input step with 5-mV overdrive	1400			ns

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2352M			UNIT
		MIN	TYP	MAX	
Response time	R _L = 5.1 kΩ, C _L = 100 pF§, See Note 5	100-mV input step with 5-mV overdrive			ns
		TTL-level input step			

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.



TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

electrical characteristics at specified free-air temperature, $T_A = 25^\circ\text{C}^\dagger$

PARAMETER	TEST CONDITIONS	TLV2352Y						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICRmin}$, See Note 4		1	5		1	5	mV
I_{IO} Input offset current			1			1		pA
I_{IB} Input bias current			5			5		pA
V_{ICR} Common-mode input voltage range		0 to 2			0 to 4			V
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$		0.1			0.1		nA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 2\text{ mA}$		115	300		150	400	mV
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	6	16		6	16		mA
I_{DD} Supply current	$V_{ID} = 1\text{ V}$ No load		120	250		140	300	μA

[†] All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with $V_{DD} = 5\text{ V}$, 2 V with $V_{DD} = 3\text{ V}$, or below 400 mV with a 10-k Ω resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

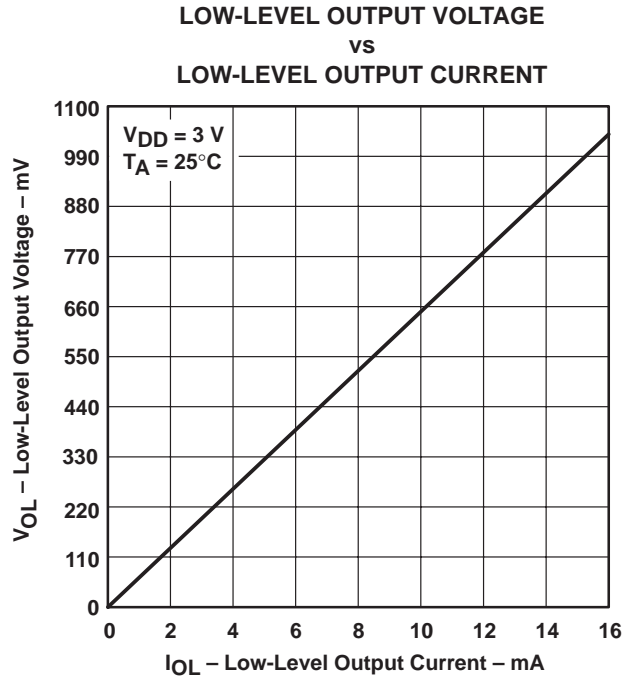


Figure 1

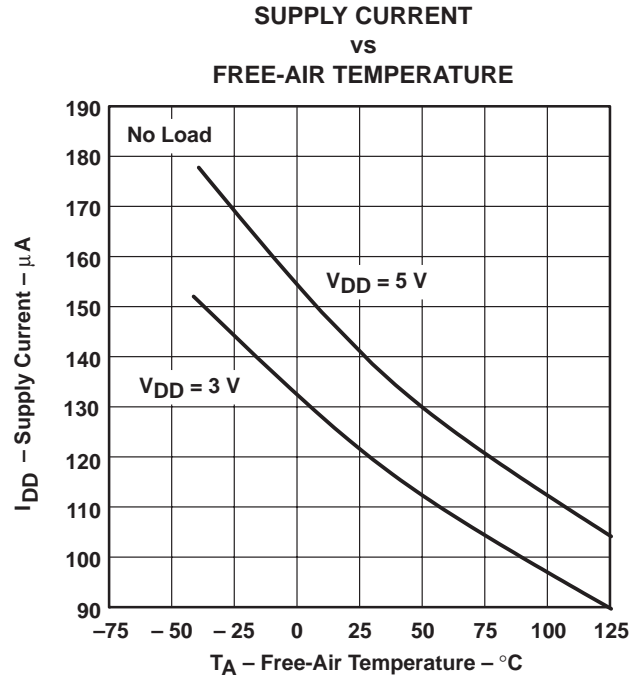


Figure 2

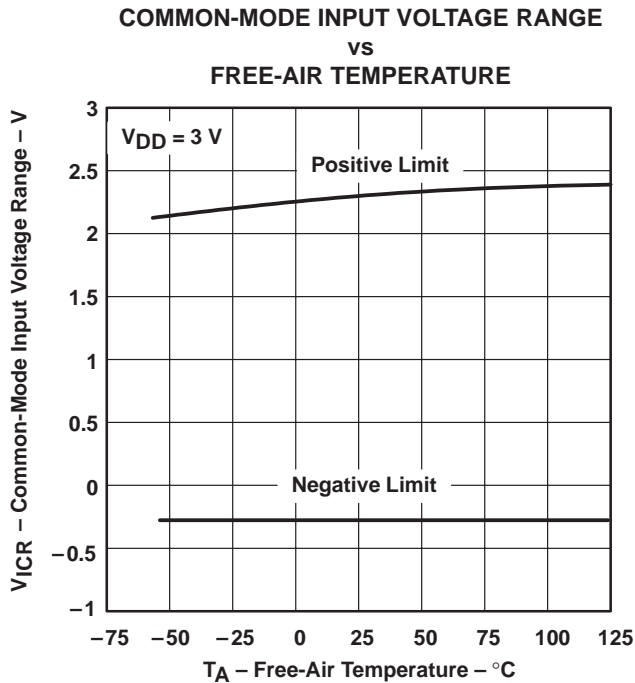


Figure 3

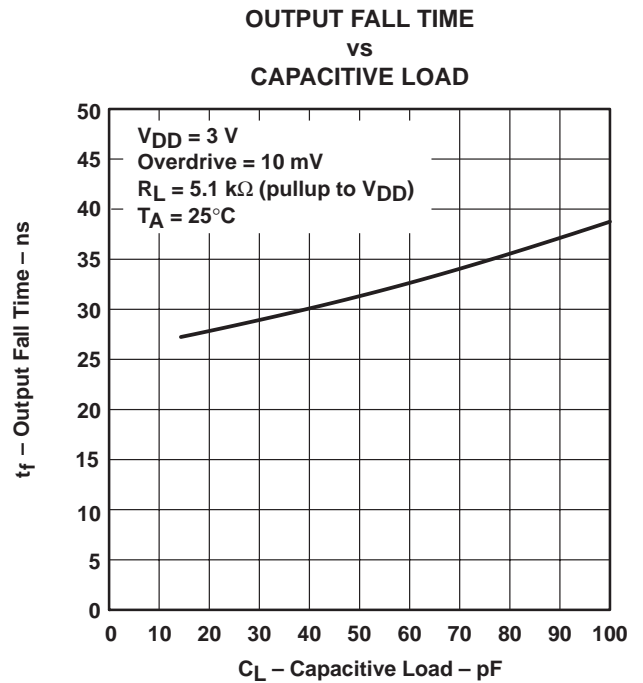


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS OVERDRIVE VOLTAGES

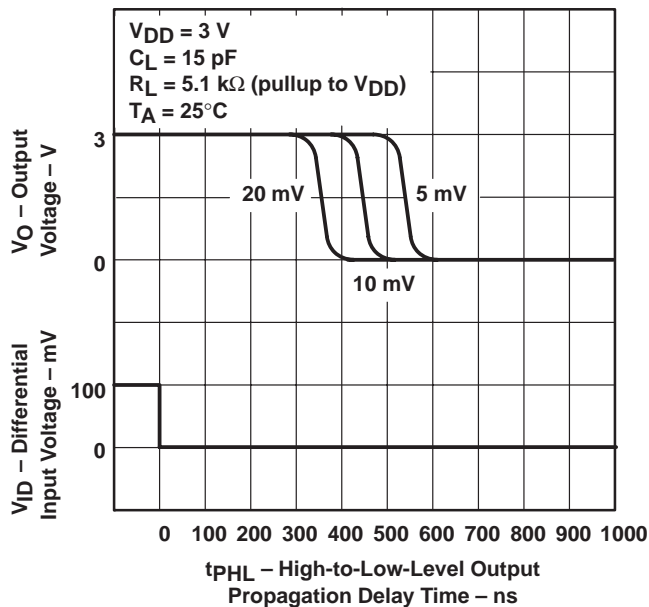


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS CAPACITIVE LOADS

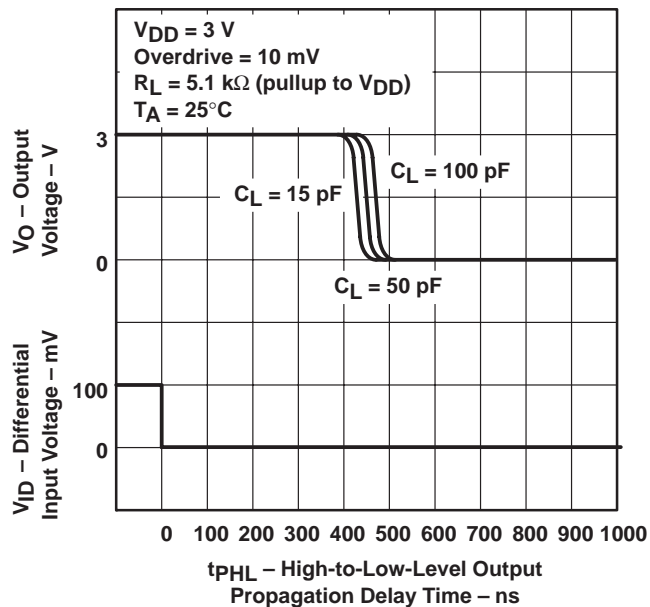


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS OVERDRIVE VOLTAGES

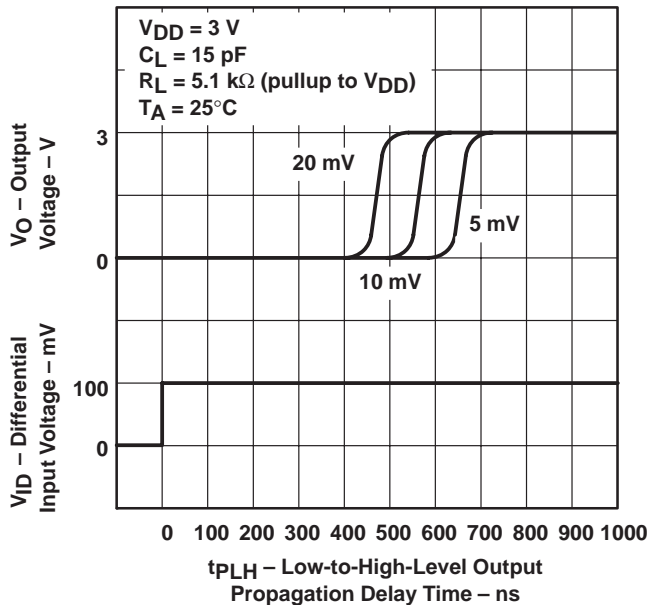


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
 PROPAGATION DELAY
 FOR VARIOUS CAPACITIVE LOADS

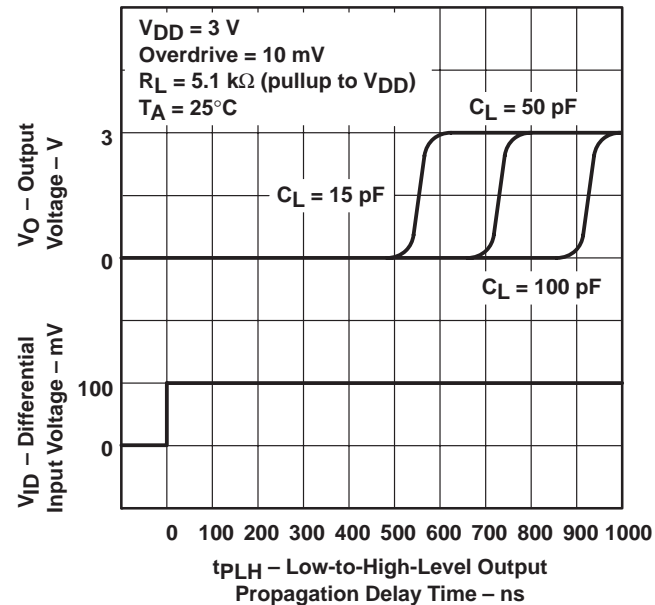


Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.

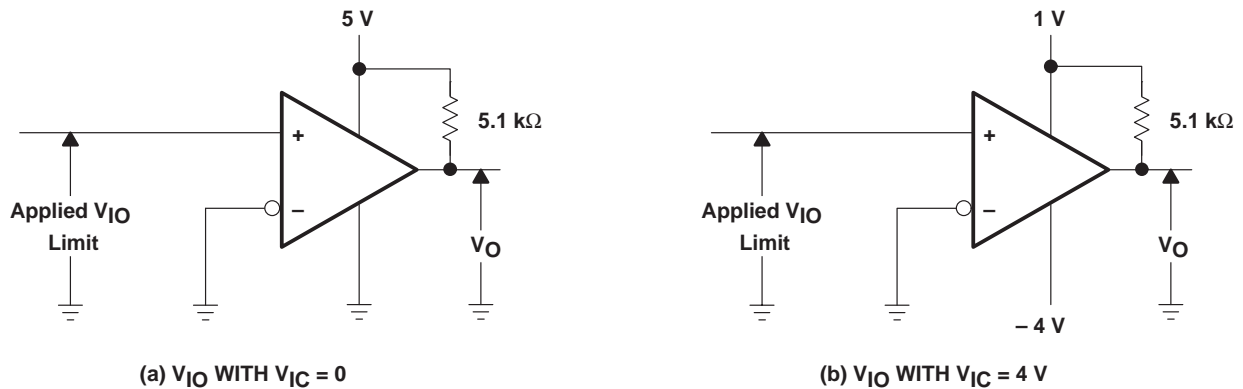


Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

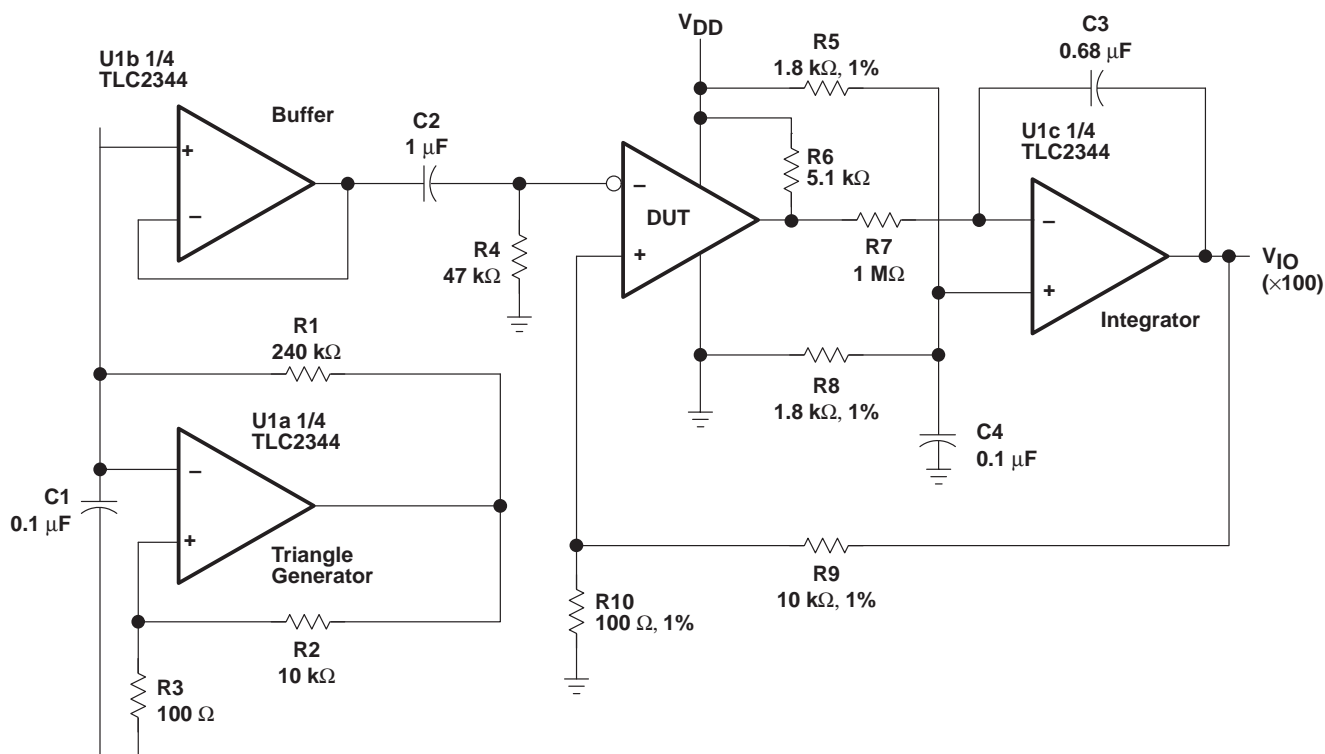
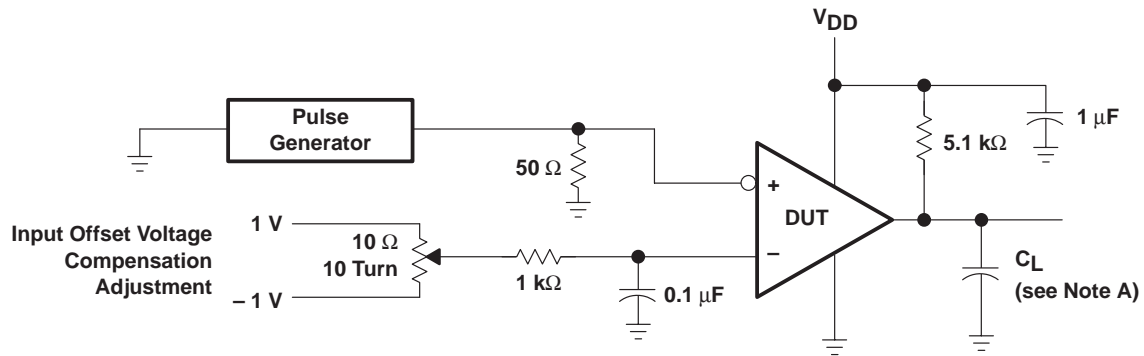


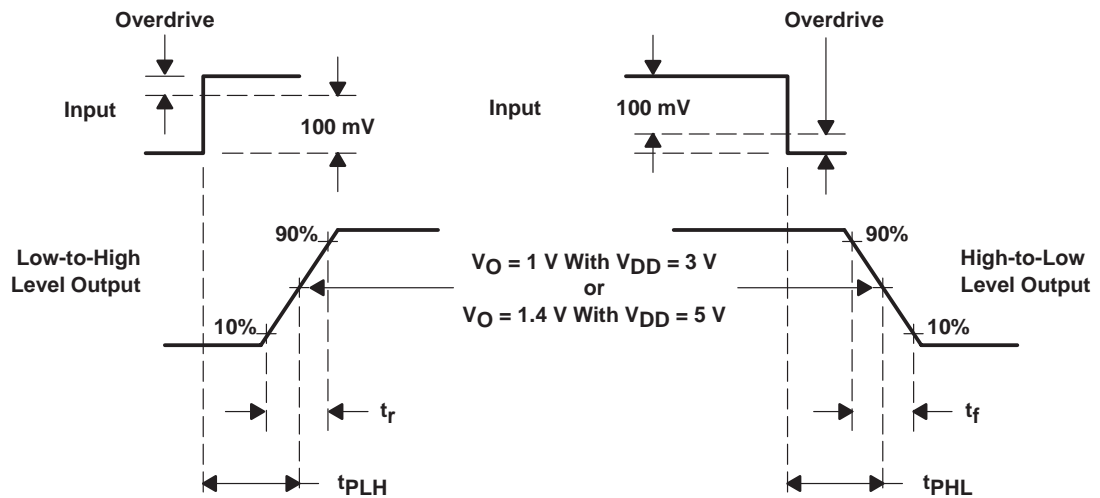
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses $V_O = 1\text{ V}$ with $V_{DD} = 3\text{ V}$ or when the output crosses $V_O = 1.4\text{ V}$ with $V_{DD} = 5\text{ V}$. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

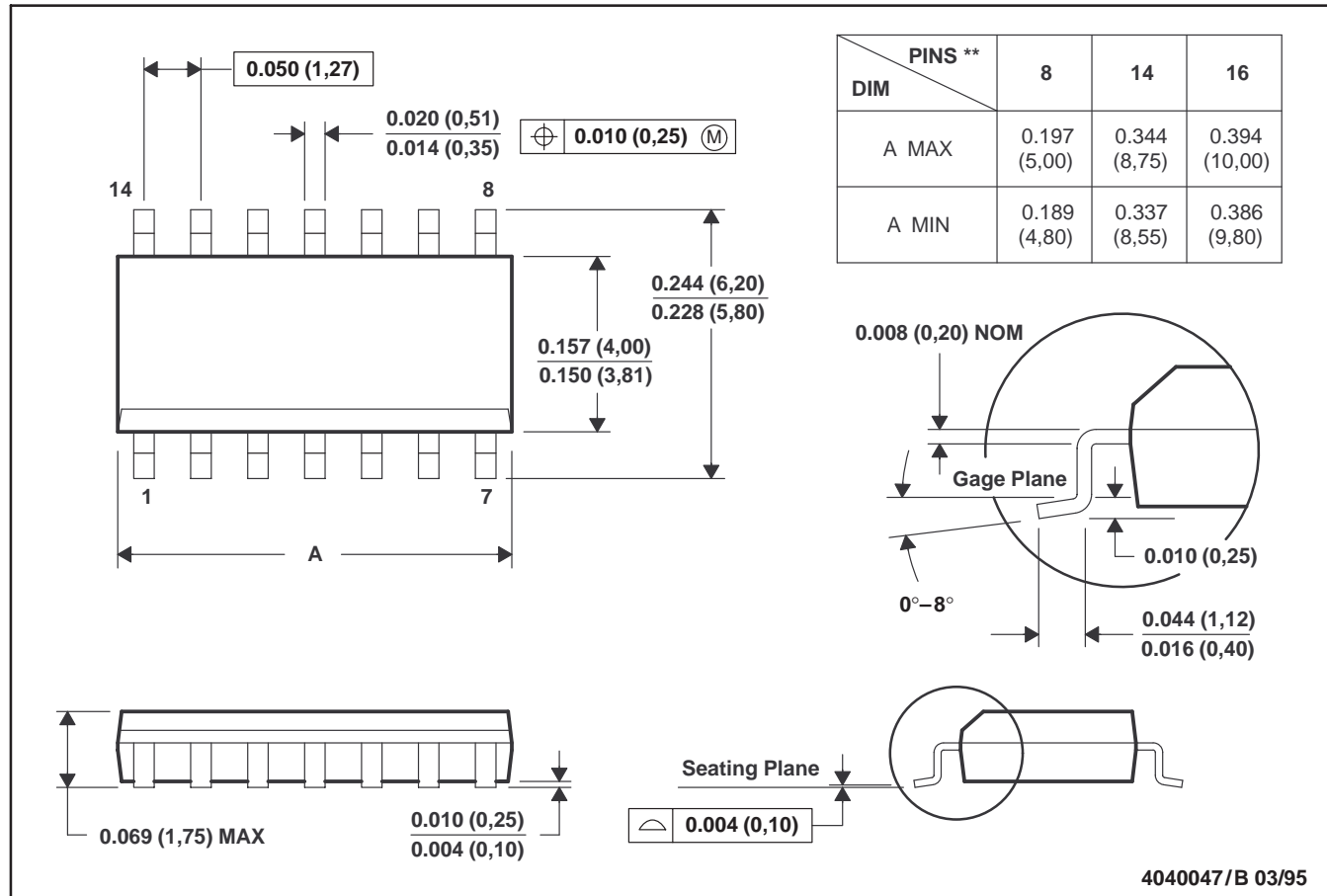
SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Four center pins are connected to die mount pad.
 - E. Falls within JEDEC MS-012

TLV2352, TLV2352Y

LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

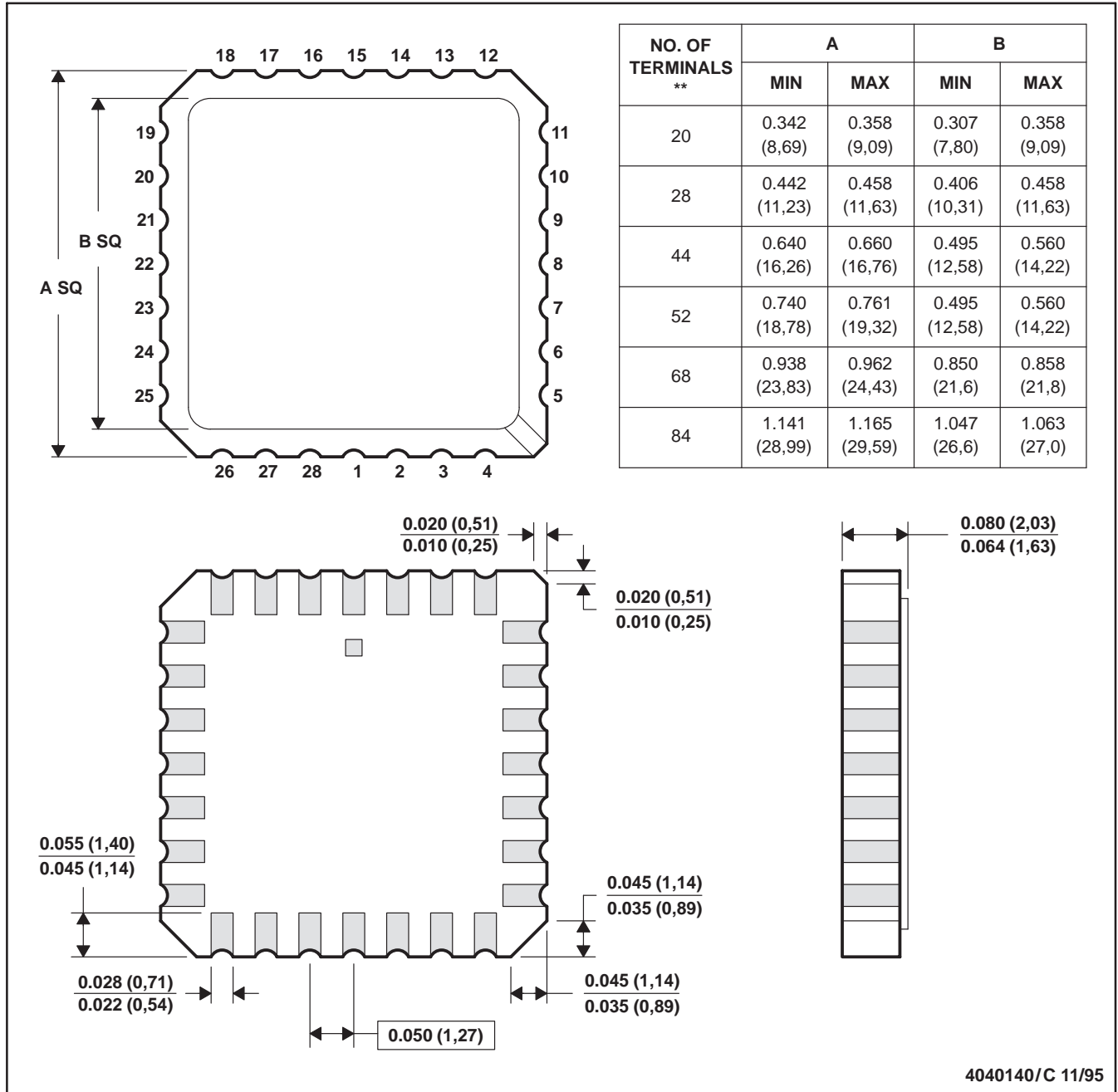
SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

FK (S-CQCC-N)**

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

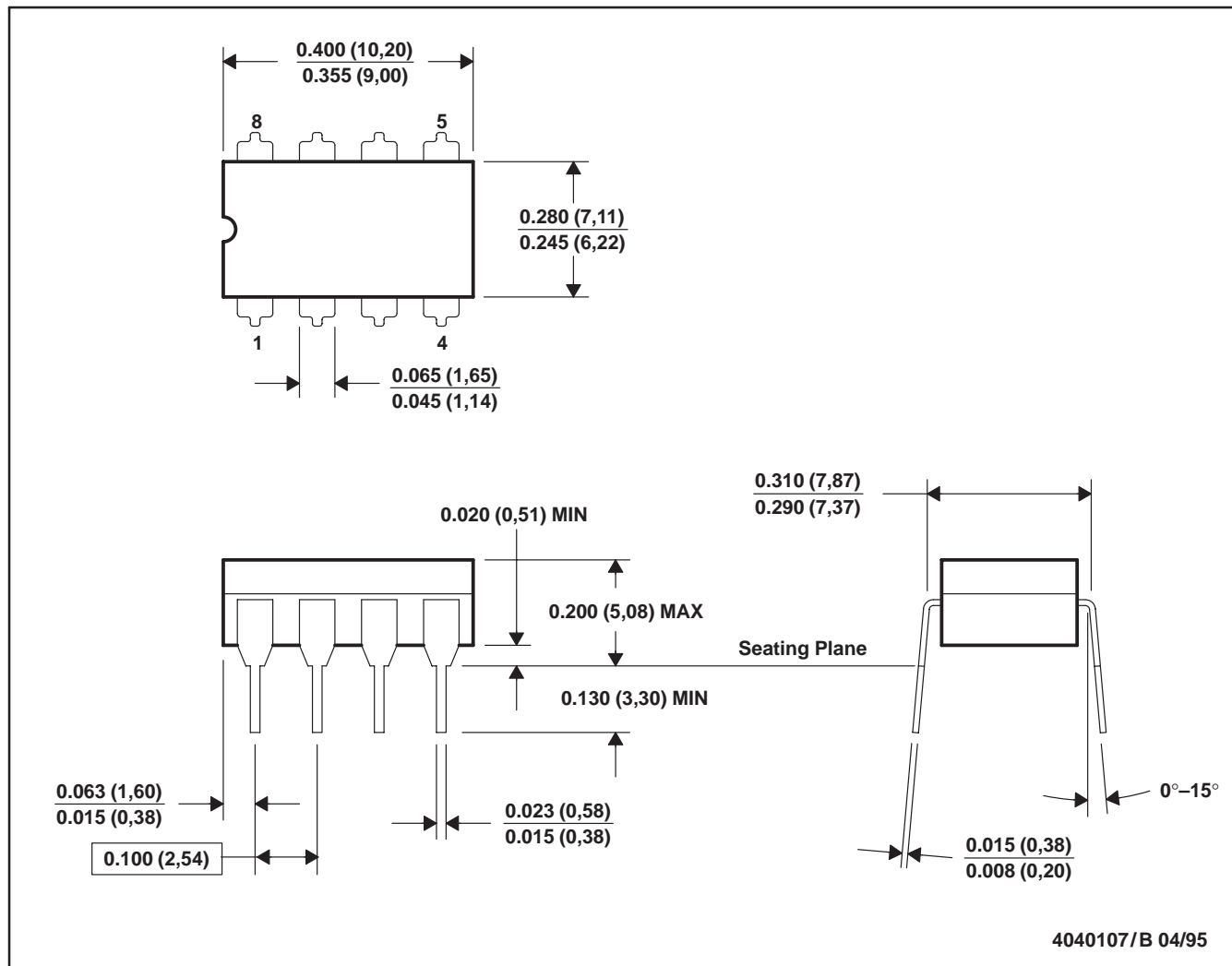
TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE

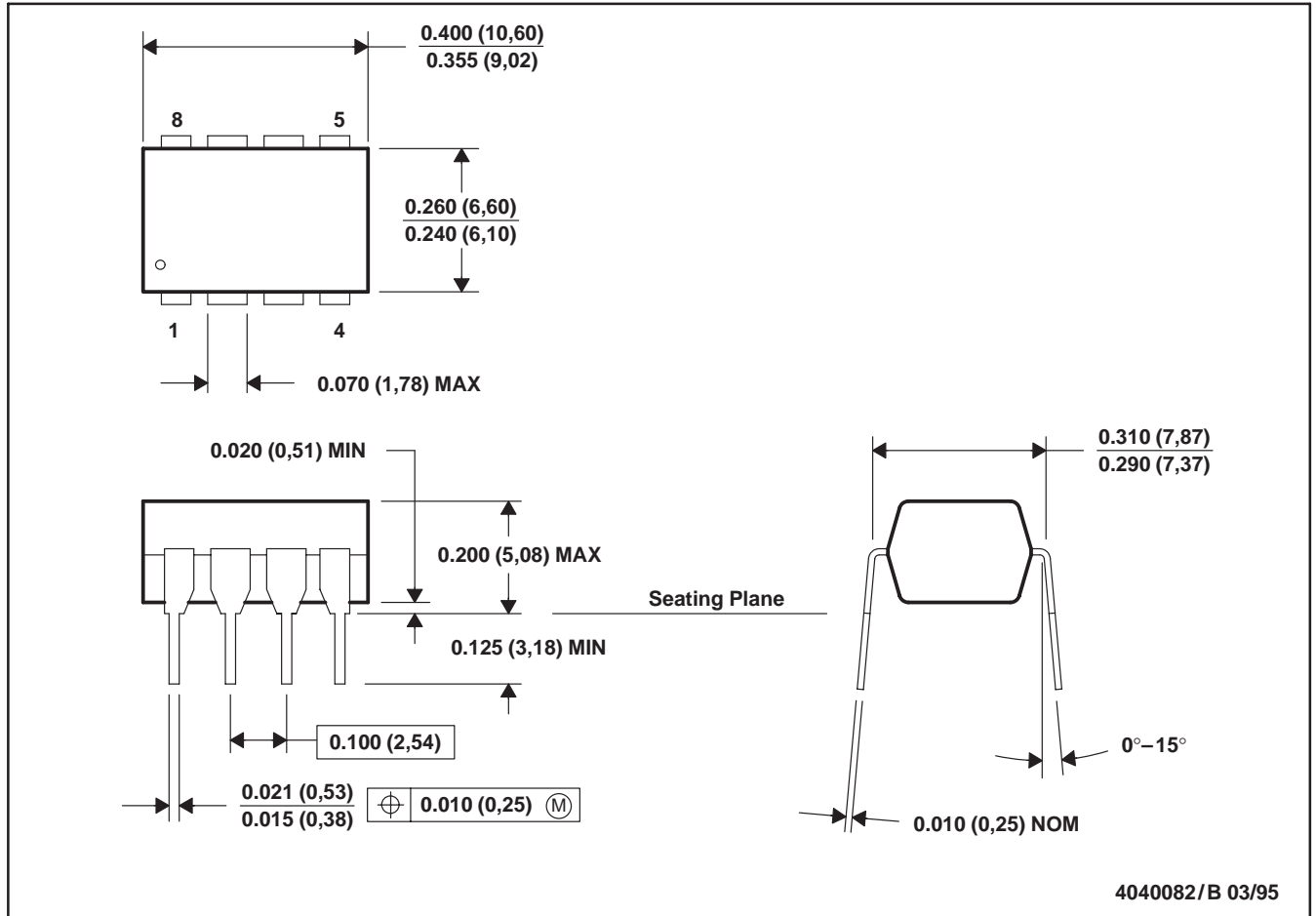


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
 E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

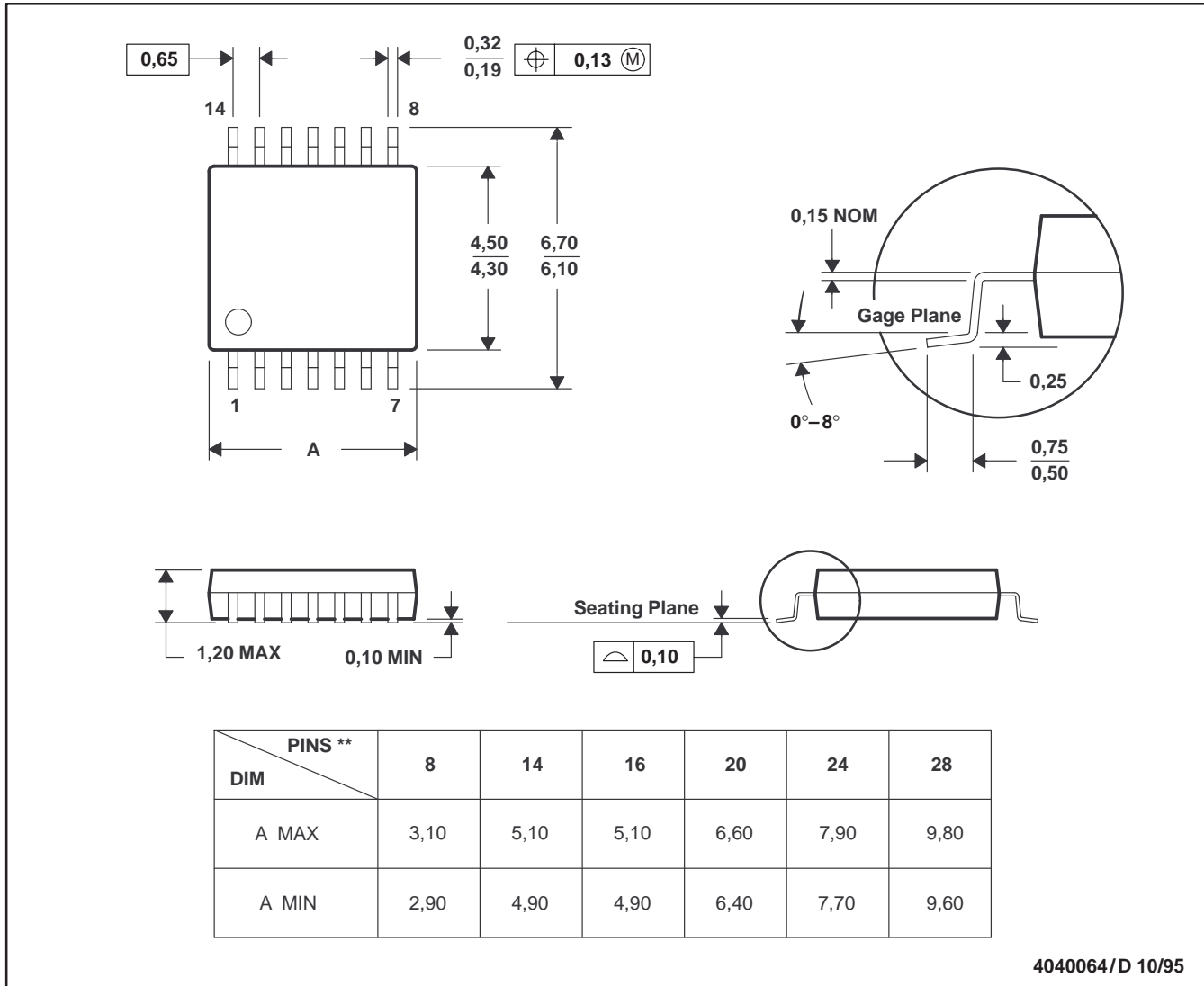
SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

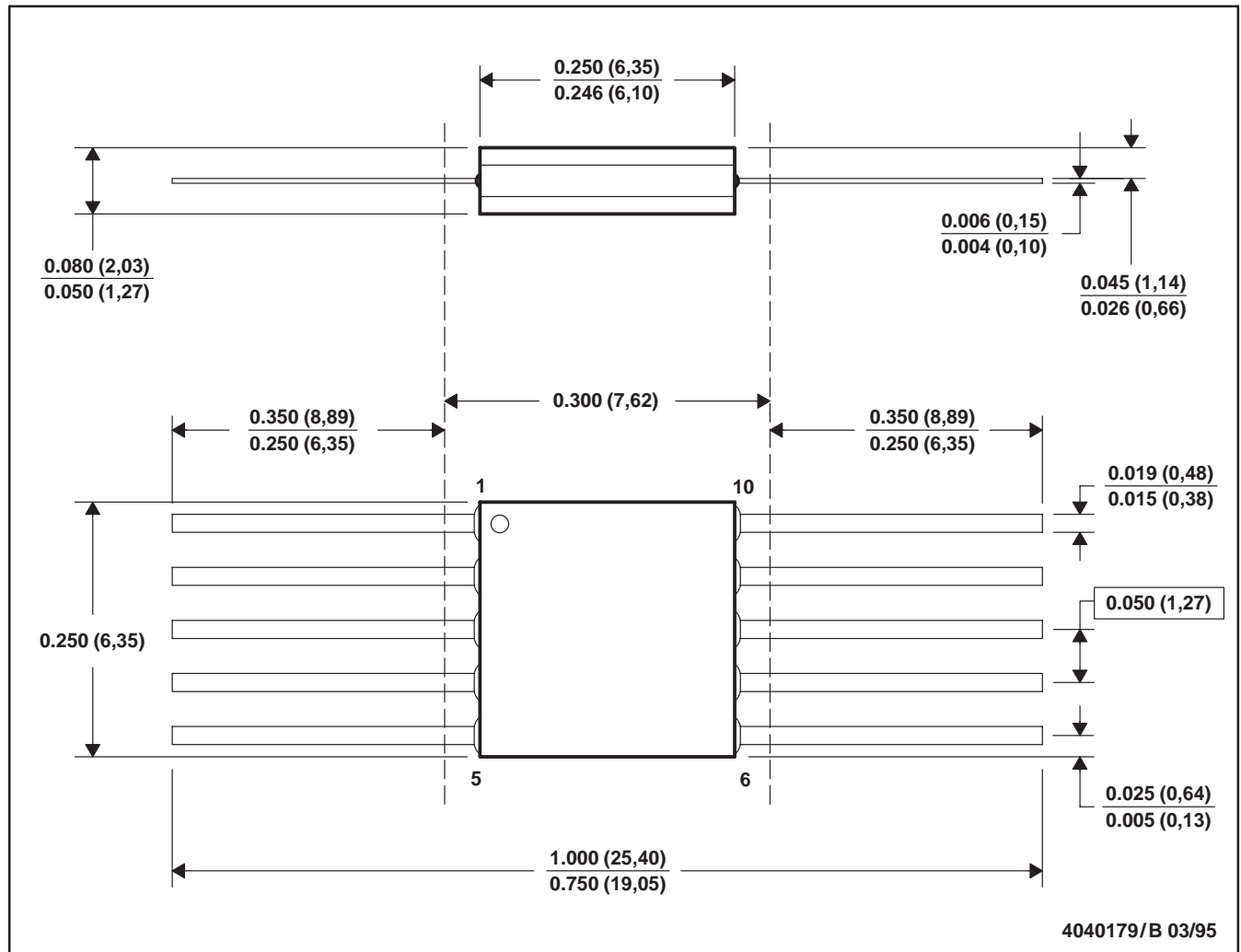
TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

MECHANICAL INFORMATION

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9688101QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9688101QPA TLV2352M	Samples
TLV2352ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I	Samples
TLV2352IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I	Samples
TLV2352IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLV2352IP	Samples
TLV2352IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	Samples
TLV2352IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	Samples
TLV2352IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	Samples
TLV2352MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLV2352MJG	Samples
TLV2352MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9688101QPA TLV2352M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

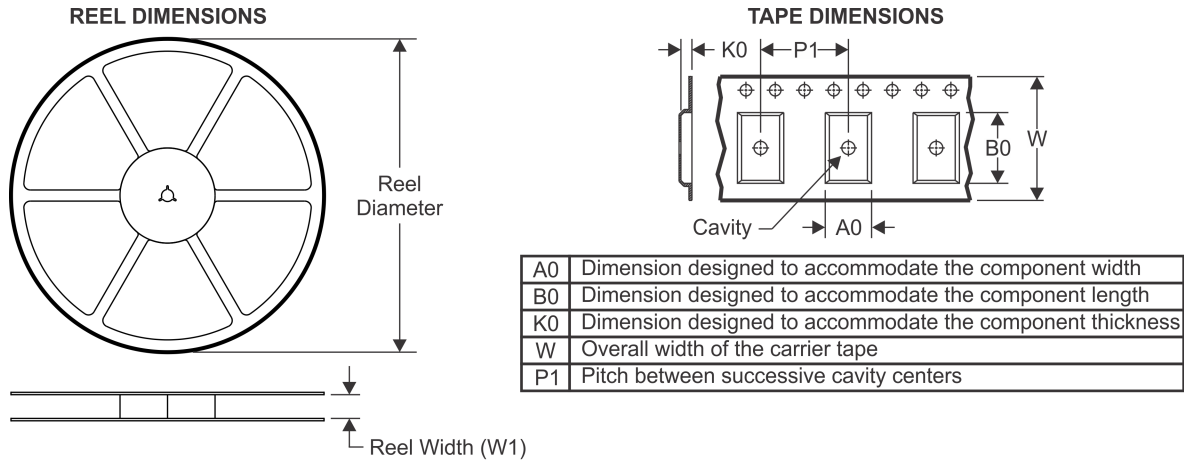
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2352, TLV2352M :

- Catalog: [TLV2352](#)
- Military: [TLV2352M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2352IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2352IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.