TEXAS INSTRUMENTS

TLV4021, TLV4041

ZHCSIW5 – OCTOBER 2018

具有精密基准电压的 TLV40x1 小尺寸、低功耗比较器

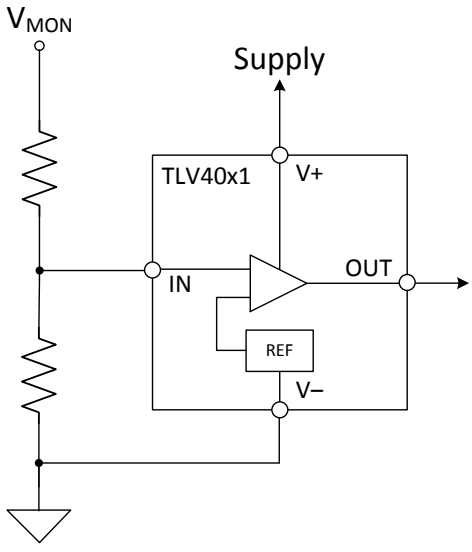
1 特性

- 宽电源电压范围：1.6V 至 5.5V
- 0.2V、1.2V 内部基准电压
- 高阈值精度
  - 工作温度范围内精度为 1%
- 低静态电流：2.5µA
- 传播延迟：450ns
- 推挽和开漏输出选项
- 内部迟滞：20mV
- 温度范围：-40°C 至 +125°C
- 封装：
  - 0.73mm × 0.73mm DSBGA（4 凸点）

2 应用

- 自诊断
- 监控
- 电池管理和保护
- 电流和电压检测
- 模拟前端
- 电机驱动
- 电源管理
- 非隔离电源
- 负载点稳压器
- 直流/直流电源
- 交流/直流电源
- 系统控制和监控

电压监控器



3 说明

TLV40x1 器件是低功耗高精度比较器，具有 1.2V 或 0.2V 内部基准电压，传播延迟为 450ns。这些比较器采用 0.73mm × 0.73mm 超小型 DSBGA 封装，使得 TLV40x1 适用于空间关键型设计，例如要求低功耗和对工作条件变化作出快速响应的便携式或电池供电设计。

经过出厂修整的开关阈值和内部迟滞相结合，使得 TLV40x1 非常适合在必须将慢速输入信号转换为纯净数字输出的严苛、嘈杂环境中进行精密电压和电流监测。同样地，输入端的短暂毛刺也得以抑制，因此可确保稳定的输出运行，不会引起误触发。

TLV40x1 提供多种配置，从而使系统设计人员可实现他们所需的输出响应和性能。例如，TLV4021 具有 漏极开路输出级，而 TLV4041 具有 推挽式输出级。此外，TLV4021/TLV4041 提供同相输入。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TLV40x1R1/2	DSBGA (4)	0.73mm × 0.73mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

TLV40x1 系列内部基准比较器

器件	基准电压	输出拓扑
TLV4021R2 TLV4021R1	0.2V 1.2V	漏极开路
TLV4041R2 TLV4041R1	0.2V 1.2V	推挽

ADVANCE INFORMATION

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

日期	修订版本	说明
最初发布版本	*	最初发布版本

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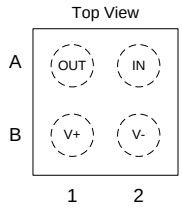
5 Pin Configuration and Functions

YKA Package
4-Bump DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	A1	O	Comparator output: OUT is push-pull on TLV4041 and open-drain on TLV4021
V+	B1	P	Positive (highest) power supply
V–	B2	P	Negative (lowest) power supply
IN	A2	I	Comparator input

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)			6	V
Input voltage (IN) from (V-) (2)		-0.3	6	V
Input Current (IN)(2)			±10	mA
Output voltage (OUT) from (V-)	TLV4021	-0.3	6	V
	TLV4041	-0.3	(V+) + 0.3	V
Output short-circuit duration(3)			10	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3 V below (V–) must be current-limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.6	5.5	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV40x1 YKA (DSBGA) 4 BUMPS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_S = 1.8 V to 5 V, typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃	TLV40x1R2	0.192		0.208	V
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃	TLV40x1R1	1.188		1.212	V
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C	TLV40x1R2	0.1728		0.1872	V
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C	TLV40x1R1	1.1682		1.1918	V
V_{HYS}	Input hysteresis voltage	V_S = 1.8 V and 5 V, T_A = 25℃			20		mV
V_{IN}	Input voltage range	T_A = -40℃ to +125℃		V–		5.5	V
I_{BIAS}	Input bias current	Over V_{IN} range			10		pA
V_{OL}	Voltage output swing from (V–)	I_{SINK} = 200 µA, OUT asserted low, V_S = 5 V, T_A = –40°C to +125°C				100	mV
		I_{SINK} = 3 mA, OUT asserted low, V_S = 5 V, T_A = –40°C to +125°C				400	mV
I_{O-LKG}	Open-drain output leakage current (TLV4021 only)	V_S = 5 V, OUT asserted high V_{PULLUP} =V_{CC} , T_A = 25°C			20		pA
I_{SC}	Short-circuit current	V_S = 5 V, sinking, T_A = 25°C			55		mA
I_Q	Quiescent current	No load, T_A = 25°C, Output Low, V_S = 1.8 V			2.5	8	µA
		No load, T_A = –40°C to +125°C, Output Low, V_S = 1.8 V				10	µA
V_{POR} (1)	Power-on reset voltage				1.45		V

(1) Below V_{POR}, the output cannot be determined; for V_{POR} > 1.45 V & V_{POR} < V_S = 1.6 V, the output is low or determined by the input level (see Start-uP Timing Diagram)

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6.6 Switching Characteristics

Typical values are at T_A = 25°C, V_S = 3.3 V, C_L = 15 pF; Input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay, high-to-low (1)	Midpoint of input to midpoint of output (R_P=4.99 kΩ, TLV4021 only)		450		ns
t_{PLH}	Propagation delay, low-to-high (1)	Midpoint of input to midpoint of output (R_P=4.99 kΩ, TLV4021 only)		450		ns
t_F	Fall time	20% to 80%		4		ns
t_{ON}	Power-up time (2)			500		µs

(1) High-to-low and low-to-high refers to the transition at the input.
(2) During power on cycle, V_S must exceed 1.4 V for t_{ON} before the output is in a correct state. Prior to t_{ON} elapsing, the output is held low (TLV4041) or held at V_{PULLUP} (TLV4021).

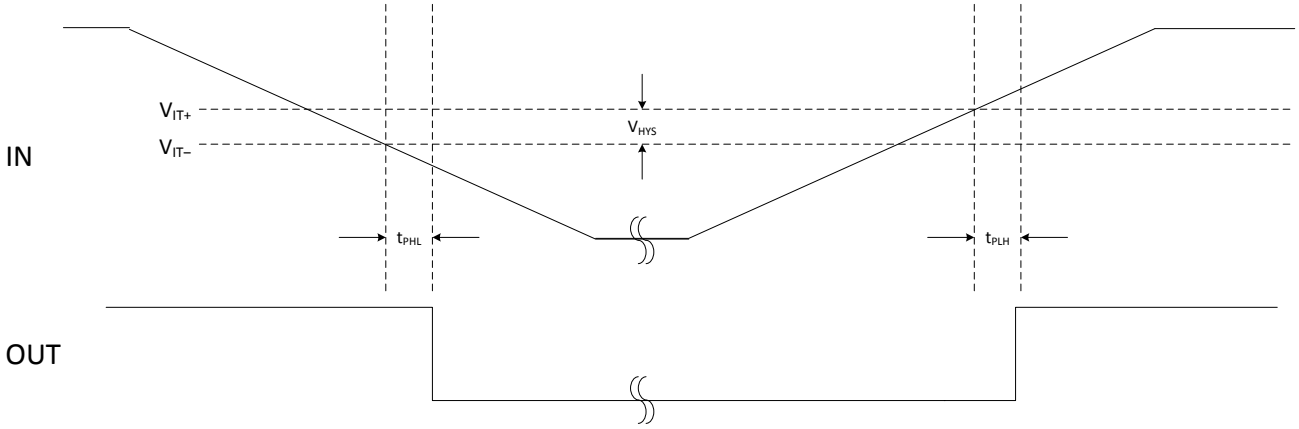

Figure 1. Timing Diagram

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7 Detailed Description

7.1 Overview

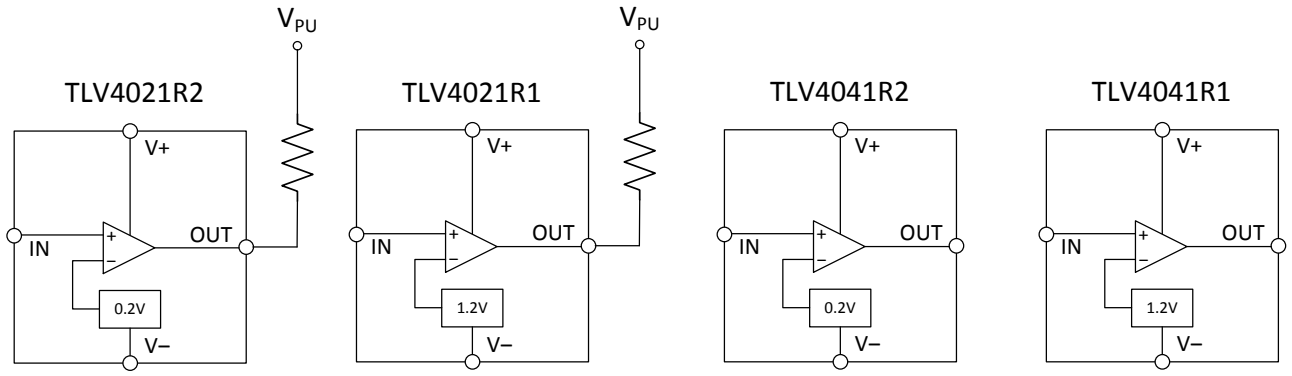
The TLV40x1 devices are MicroPower comparators that are well suited for compact, low-current, precision voltage detection applications. With high-accuracy, internal reference options of 0.2V or 1.2V, 2.5uA of quiescent current, and propagation delay of 450ns, the TLV40x1 comparator family enables power conscious systems to monitor and respond quickly to fault conditions. The last digit in the part number scheme following the "R" indicates the internal reference voltage option ("2" represents 0.2V and "1" is 1.2V).

The TLV40x1 asserts the output signal as shown in Table 1. V_{IT+} represents the positive-going input threshold that causes the comparator output to change state, while V_{IT-} represents the negative-going input threshold that causes the output to change state. Since V_{IT+} and V_{IT-} are factory trimmed and warranted over temperature, the TLV40x1 is equally suited for undervoltage and overvoltage applications. In order to monitor any voltage above the internal reference voltage, an external resistor divider network is required.

Table 1. TLV40x1 Truth Table

Device	Reference Voltage	Output Topology	Input Voltage Condition	Output Logic Level
TLV4021R2 TLV4021R1	0.2V 1.2V	Open-Drain	IN > V_{IT+}	Output high impedance
			IN < V_{IT-}	Output asserted low
TLV4041R2 TLV4041R1	0.2V 1.2V	Push-Pull	IN > V_{IT+}	Output asserted high
			IN < V_{IT-}	Output asserted low

7.2 Functional Block Diagram



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7.3 Feature Description

The TLV40x1 is a family of 4-pin, precision, low-power comparators with a precision integrated reference. The TLV40x1 comparators feature a rail-to-rail input stage with factory programmed switching thresholds for both rising and falling input waveforms. The comparator family also supports open-drain and push-pull output configurations.

7.4 Device Functional Modes

The TLV40x1 comparators have a Power-on-Reset (POR) circuit. When the power supply (V_S) is ramping up or ramping down, POR will be activated if V_S is below the recommended operating voltage range. For the TLV4021, the POR circuit will force the output to a high impedance state. For the TLV4041, the POR circuit will hold the output low (at V-) while activated. When V_S is greater than, or equal to, the recommended operating voltage range, the comparator output reflects the state of the input (IN).

7.4.1 Input (IN)

The TLV40x1 comparators have two inputs: one external input (IN) and one internal input that is connected to the integrated voltage reference. The comparator rising threshold is trimmed to the reference voltage (V_{IT+}). The comparator falling threshold is trimmed to the reference voltage minus 20 mV (V_{IT-}). Since the rising and falling threshold are both trimmed and warranted in the Electrical Characteristics Table, the TLV40x1 is equally suited for undervoltage and overvoltage detection. The difference between (V_{IT+}) and (V_{IT-}) is referred to as the comparator hysteresis and is typically 20 mV. The integrated hysteresis makes the TLV40x1 less sensitive to supply-rail noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis.

The comparator input (IN) is able to swing 5.5 V above (V-) regardless of the device supply voltage. This includes the instance when no supply voltage is applied to the comparator (V_S = 0 V). As a result, the TLV40x1 is referred to as fault tolerant, meaning it maintains the same high input impedance when V_S is unpowered or ramping up. While not required in most cases, in order to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor at the comparator input.

The input bias current is typically TBD pA for input voltages between (V-) and (V+) and the value typically doubles for every 10°C temperature increase. The comparator input is protected from voltages below (V-) by an internal diode connected to (V-). As the input voltage goes below (V-), the protection diode becomes forward biased and begins to conduct causing the input bias current to increase exponentially. A series resistor is recommended to limit the input current when sources have signal content that is less than (V-).

7.4.2 Switching Thresholds and Hysteresis (V_{HYS})

The TLV40x1 transfer curve is shown in Figure 2.

- V_{IT+} represents the positive-going input threshold that causes the comparator output to change from a logic low state to a logic high state.
- V_{IT-} represents the negative-going input threshold that causes the comparator output to change from a logic high state to a logic low state.
- V_{HYS} represents the difference between V_{IT+} and V_{IT-} and is typically 20 mV.

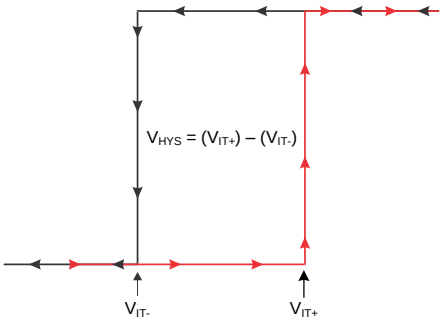

Figure 2. Transfer Curve

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Device Functional Modes (continued)

7.4.3 Output (OUT)

The TLV4041 features a push-pull output stage which eliminates the need for an external pull-up resistor while providing a low impedance output driver. Likewise, the TLV4021 features an open-drain output stage which enables the output logic levels to be pulled-up to an external source as high as 5.5 V independent of the supply voltage.

In a typical TLV40x1 application, OUT is connected to an enable input of a processor or a voltage regulator such as a dc-dc converter or low-dropout regulator (LDO). The open-drain output version (TLV4021) is used if the power supply of the comparator is different than the supply voltage of the device being controlled. In this usage case, a pull-up resistor holds OUT high when the comparator output goes high impedance. The correct interface-voltage level is provided (also known as level-shifting) by connecting the pull-up resistor on OUT to the appropriate voltage rail. The TLV4021 output can be pulled up to 5.5 V, independent of the device supply voltage (V_S). However, if level-shifting is not required, the push-pull output version (TLV4041) should be utilized in order to eliminate the need for the pull-up resistor.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV40x1 is a 4-pin, low-power comparator with a precision, integrated reference. The comparators in this family are well suited for monitoring voltages and currents in portable, battery powered devices.

8.1.1 Monitoring (V+)

Many applications monitor the same rail that is powering the comparator. In these applications the resistor divider is simply connected to the (V+) rail.

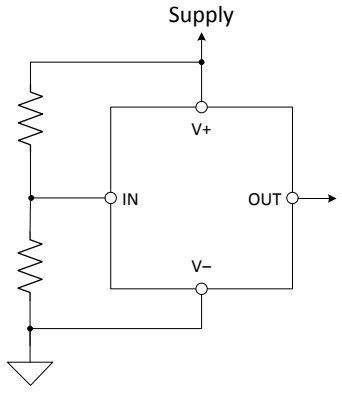

Figure 3. Supply Monitoring

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Application Information (continued)

8.1.2 Monitoring a Voltage Other than (V+)

Some applications monitor rails other than the one that is powering the comparator. In these applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.

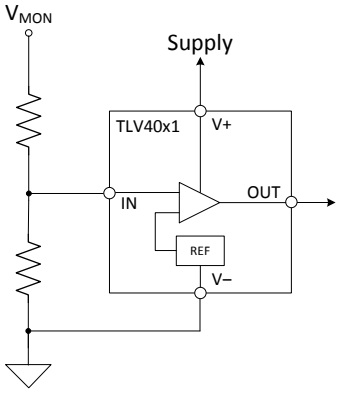

Figure 4. Monitoring a Voltage Other than the Supply

The TLV40x1 can monitor a voltage greater than the maximum (V+) with the use of an external resistor divider network. Likewise, the TLV40x1 can monitor voltages as low as the internal reference voltage (0.2 V or 1.2 V). The TLV40x1 also has the advantage of being able to monitor high impedance sources since the input bias current of the input (IN) is low. This provides an advantage over voltage supervisors that can only monitor the voltage rail that is powering them. Supervisors configured in this fashion have limitations in source impedance and minimum sensing voltage.

8.1.3 V_{PULLUP} to a Voltage Other than (V+)

For applications where the output of the comparator needs to interface with a reset/enable pin that operates from a different supply voltage, the open-drain comparators (TLV4021) should be selected. In these usage cases, the output can be pulled up to any voltage that is lower than 5.5V (independent of (V+)). This technique is commonly referred to as "level-shifting."

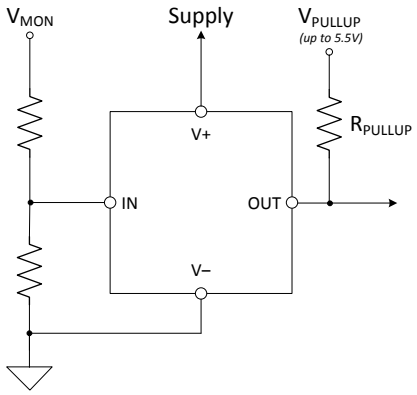

Figure 5. Level-Shifting

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8.2 Typical Application

8.2.1 Under-Voltage Detection

Under-voltage detection is frequently required in battery-powered, portable electronics to alert the system that a battery voltage has dropped below the usable voltage level. Figure 6 shows a simple under-voltage detection circuit using the TLV4041R1 which is a non-inverting comparator with an integrated 1.2 V reference and a push-pull output stage.

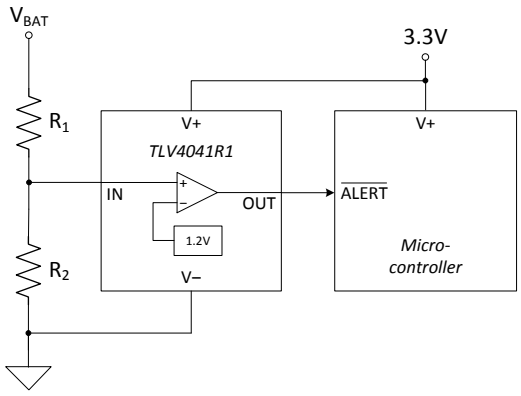

Figure 6. Under-Voltage Detection

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from 3.3 V power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 6. Connect (V+) to 3.3 V which also powers the microcontroller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0 V. When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses the (V_{IT-}) threshold of the TLV4041R1. This causes the comparator output to transition from a logic high to a logic low. The push-pull option of the TLV40x1 family is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal. The TLV4041 option with the 1.2 V internal reference is selected because it is the closest internal reference option that is less than the critical under-voltage level of 2.0 V. Choosing the internal reference option that is closest to the critical under-voltage level minimizes the resistor divider ratio which optimizes the accuracy of the circuit. Error at the falling edge threshold of (V_{IT-}) is amplified by the inverse of the resistor divider ratio. So minimizing the resistor divider ratio is a way of optimizing voltage monitoring accuracy.

Equation 1 is derived from the analysis of Figure 6.

$$V_{IT-} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \tag{1}$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to IN
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{IT-} is the falling edge threshold where the comparator output changes state from high to low

Rearranging Equation 1 and solving for R_1 yields Equation 2.

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Typical Application (continued)

$$R_1 = \frac{(V_{BAT} - V_{IT-})}{V_{IT-}} \times R_2 \quad (2)$$

For the specific undervoltage detection of 2.0 V using the TLV4041R1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.18)}{1.18} \times 1M = 695\ k\Omega \quad (3)$$

where

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{IT-} is set to1.18 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

8.2.1.3 Application Curve

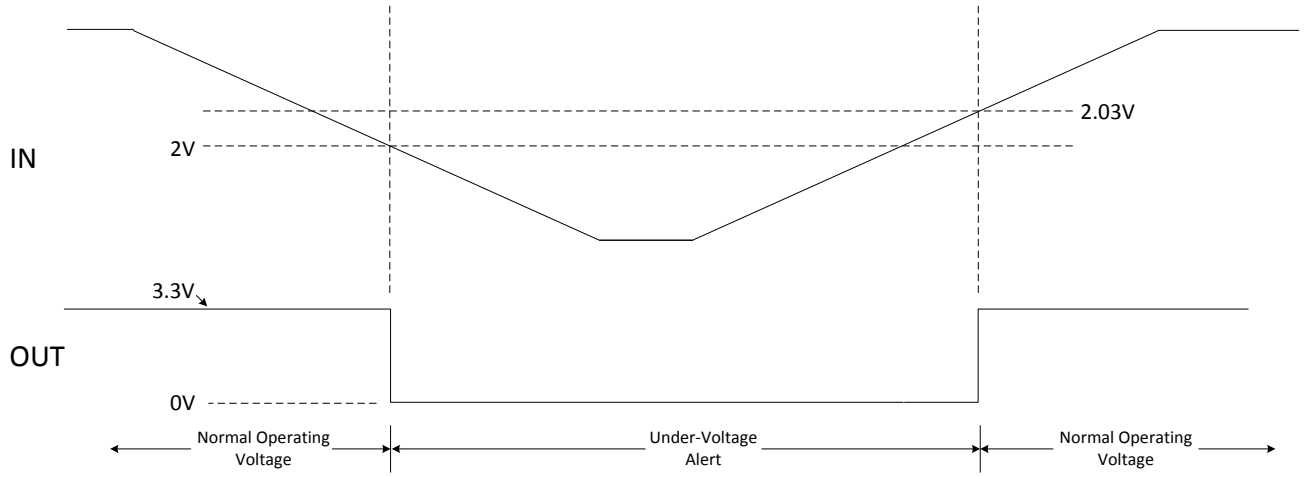

Figure 7. Under-Voltage Detection

8.2.2 Additional Application Information

8.2.2.1 Pull-up Resistor Selection

For the TLV4021 (open-drain output versions of the TLV40x1 family), care should be taken in selecting the pull-up resistor (R_{PU}) value to ensure proper output voltage levels. First, consider the required output high logic level requirement of the logic device that is being driven by the comparator when calculating the maximum R_{PU} value. When in a logic high output state, the output impedance of the comparator is very high but there is a finite amount of leakage current that needs to be accounted for. Use I_{O-LKG} from the EC Table and the V_{IH} minimum from the logic device being driven to determine R_{PU} maximum using Equation 4.

$$R_{PU}(max) = \frac{(V_{PU} - V_{IH(min)})}{I_{O-LKG}} \quad (4)$$

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Typical Application (continued)

Next, determine the minimum value for R_{PU} by using the V_{IL} maximum from the logic device being driven. In order for the comparator output to be recognized as a logic low, V_{IL} maximum is used to determine the upper boundary of the comparator's V_{OL}. V_{OL} maximum for the comparator is available in the EC Table for specific sink current levels and can also be found from the V_{OUT} versus I_{SINK} curve in the Typical Application curves. A good design practice is to choose a value for V_{OL} maximum that is 1/2 the value of V_{IL} maximum for the input logic device. The corresponding sink current and V_{OL} maximum value will be needed to calculate the minimum R_{PU}. This method will ensure enough noise margin for the logic low level. With V_{OL} maximum determined and the corresponding I_{SINK} obtained, the minimum R_{PU} value is calculated with Equation 5.

$$R_{PU}(\text{min}) = \frac{\left(V_{PU} - V_{OL(\text{max})}\right)}{I_{SINK}} \tag{5}$$

Since the range of possible R_{PU} values is large, a value between 5 kΩ and 100 kΩ is generally recommended. A smaller R_{PU} value provides faster output transition time and better noise immunity, while a larger R_{PU} value consumes less power when in a logic low output state.

8.2.2.2 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 100 nF low equivalent series resistance (ESR) capacitor from (V+) to (V-).

8.2.2.3 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor from the comparator input (IN) to the (V-) for good analog design practice. This capacitor placement reduces device sensitivity to transients.

8.3 What to Do and What Not to Do

Do connect a 100 nF decoupling capacitor from (V+) to (V-) for best system performance.

If the monitored voltage is noisy, do connect a decoupling capacitor from the comparator input (IN) to (V-).

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the impact on accuracy.

Don't use a pull-up resistor that is too small because the larger current sunk by the output may exceed the desired low-level output voltage (V_{OL}).

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9 Power-Supply Recommendations

These devices operate from an input voltage supply range between 1.7 V and 5.5 V.

10 Layout

10.1 Layout Guidelines

A power supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV40x1 output stage, higher than normal quiescent current can be drawn from the power supply when the output transitions. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

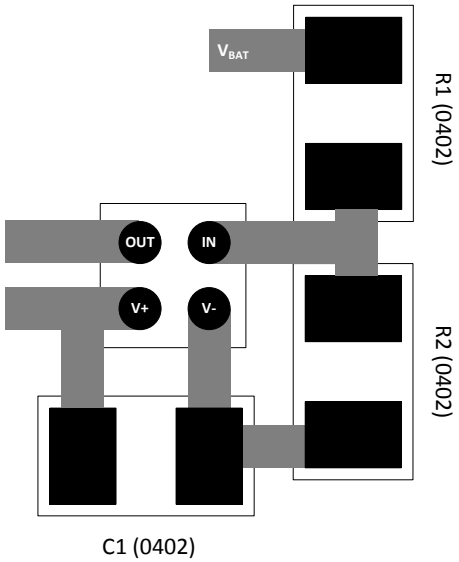

Figure 8. Layout Example

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11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

Table 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TLV4021	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV4041	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航栏。

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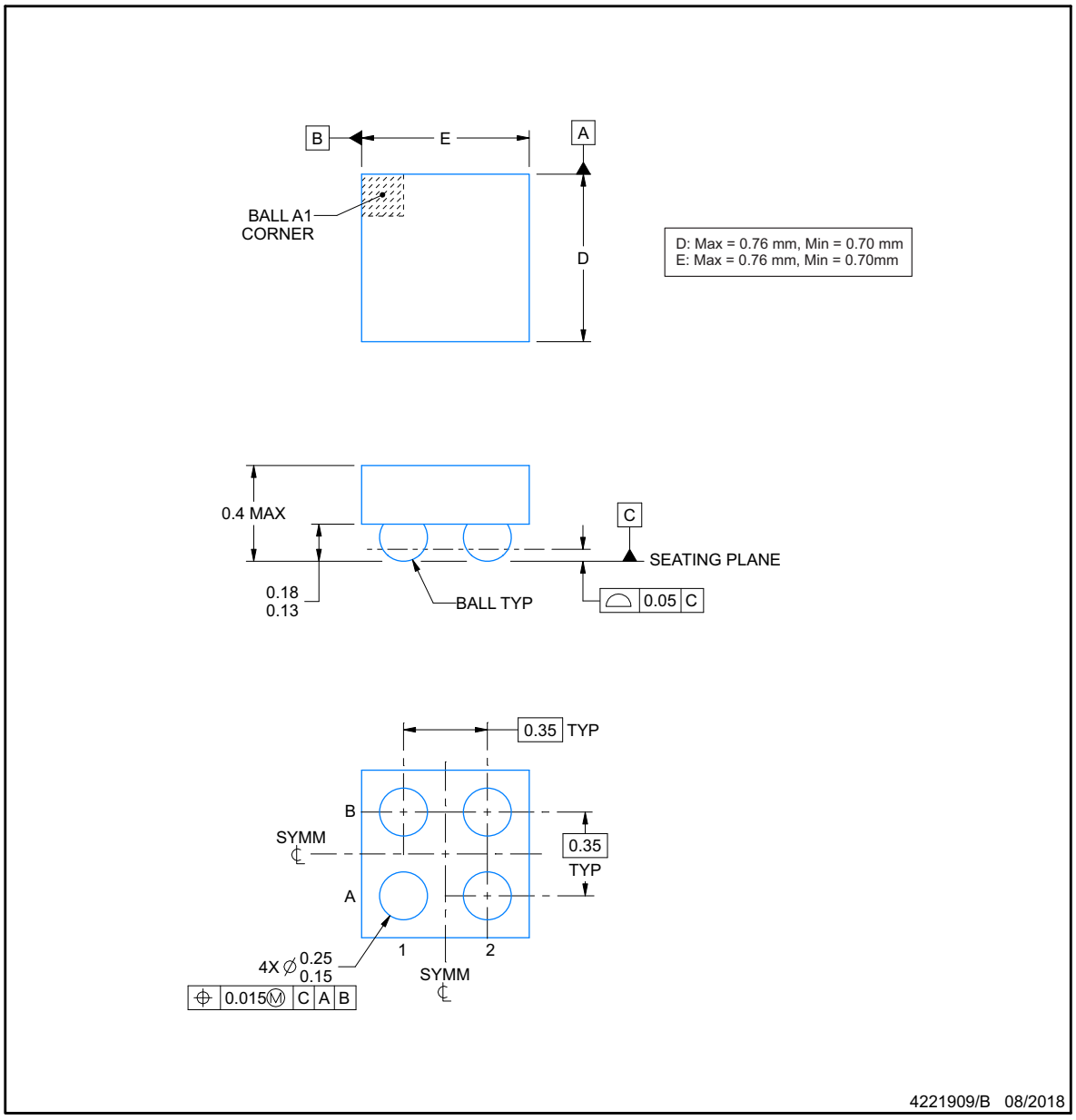
PACKAGE OUTLINE

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



4221909/B 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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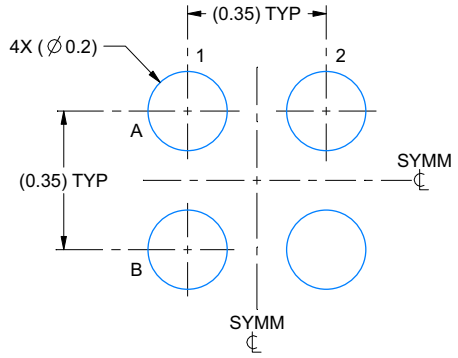
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

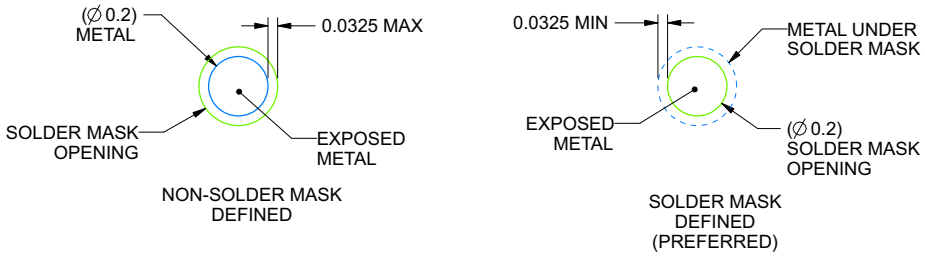
YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

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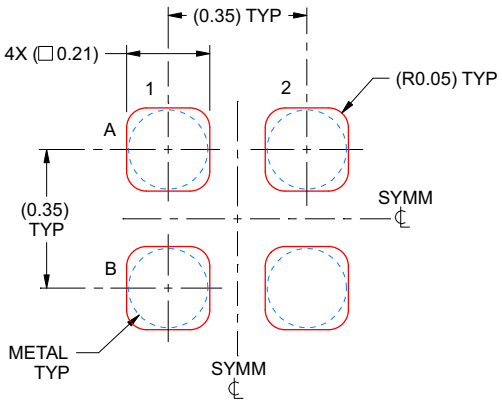
EXAMPLE STENCIL DESIGN

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4021R1YKAR	PREVIEW	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	
TLV4021R2YKAR	PREVIEW	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	6	
TLV4021S5YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	Call TI | SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
TLV4041R2YKAR	ACTIVE	DSBGA	YKA	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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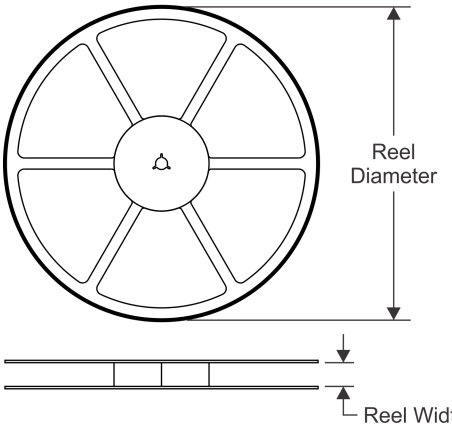
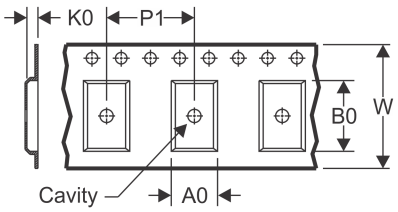
TAPE AND REEL INFORMATION

REEL DIMENSIONS

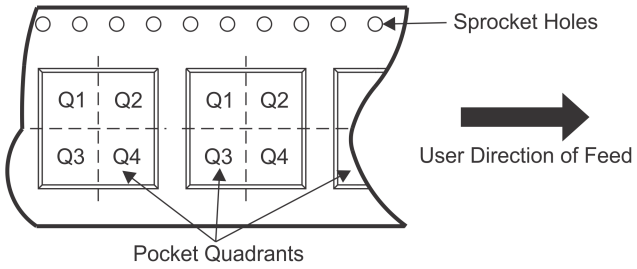


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

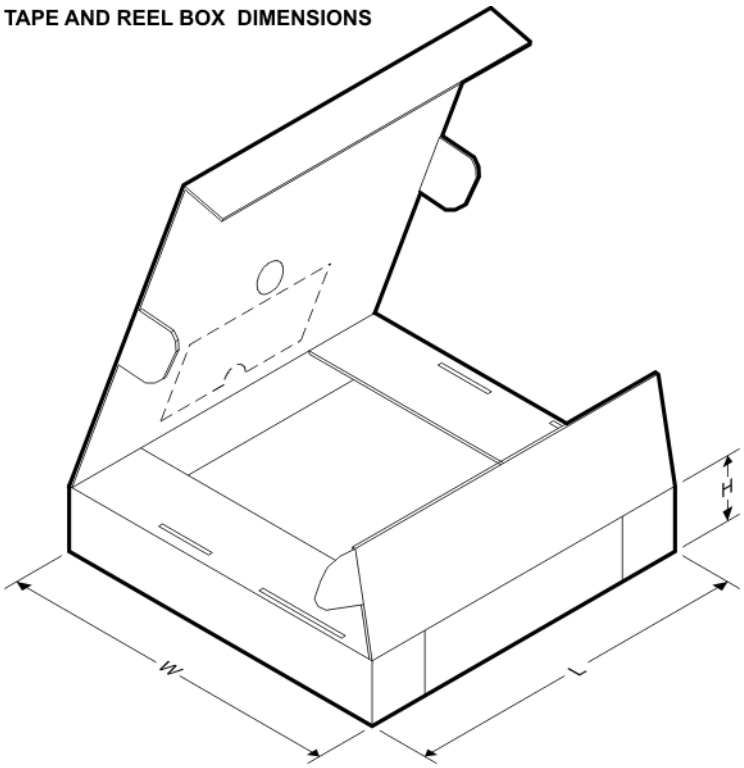
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4021S5YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.5	4.0	8.0	Q1
TLV4041R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.5	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

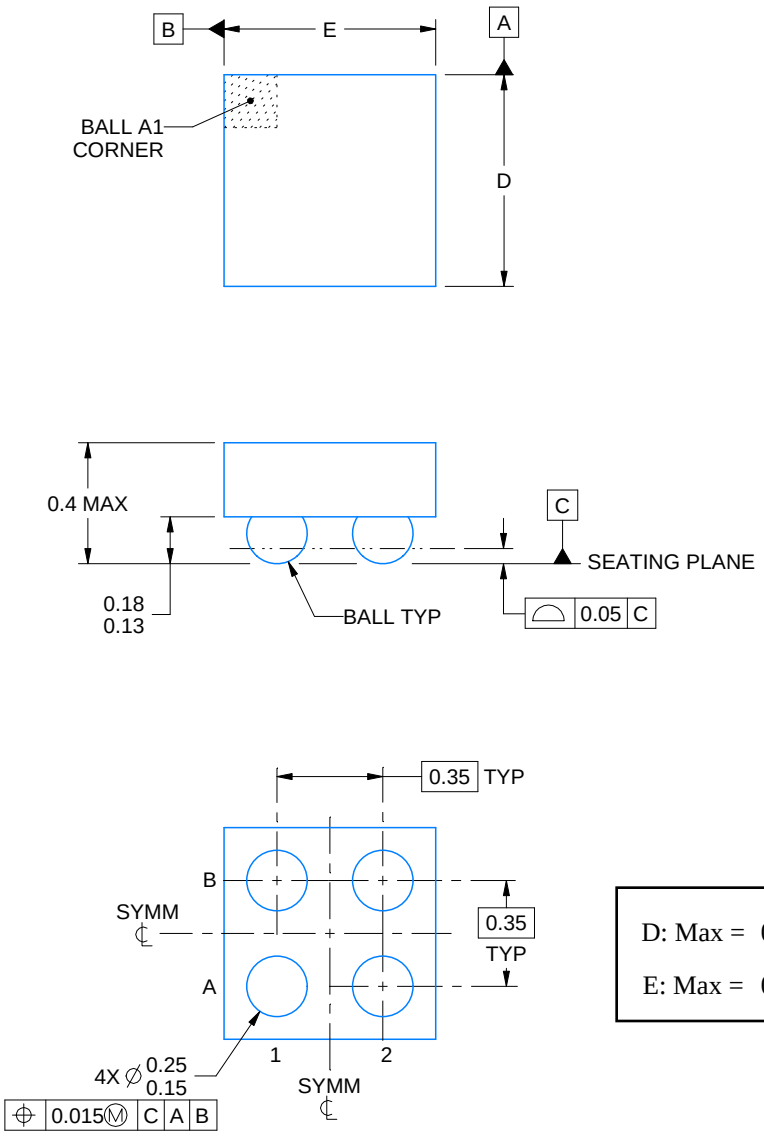
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4021S5YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.76 mm, Min = 0.7 mm

E: Max = 0.76 mm, Min = 0.7 mm

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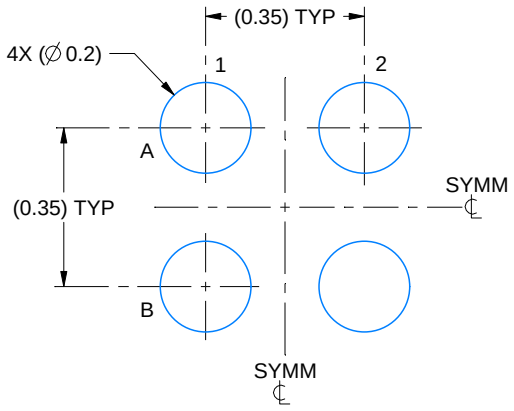
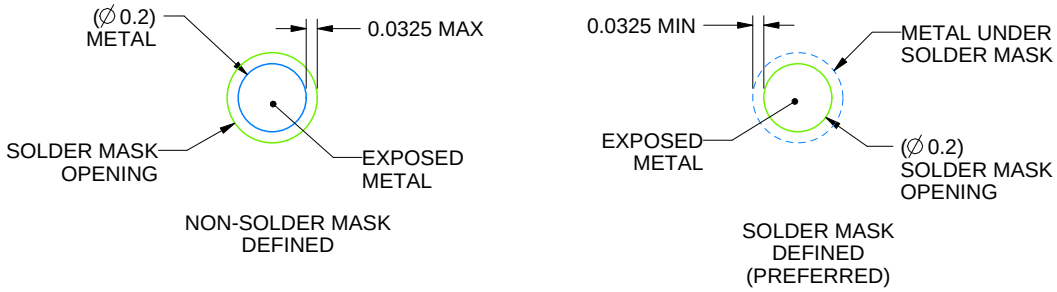
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
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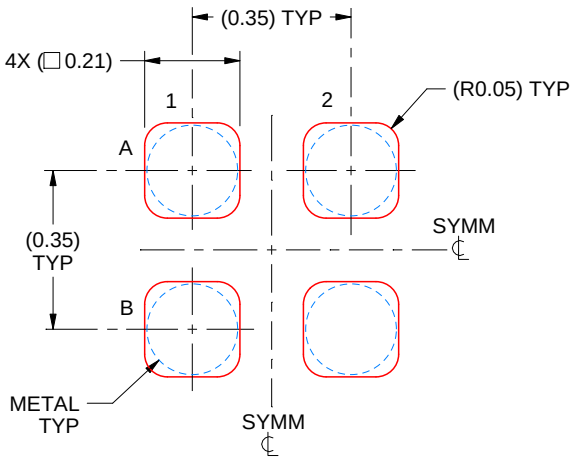

SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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