# Four-ADC, Two-DAC, Low Power Codec with Audio Processor

Data Sheet

# ADAU1777

## FEATURES

- Programmable audio processing engine
  - Fast (up to 768 kHz) and slow processing paths
  - Biquad filters, limiters, volume controls, and mixing
- Low latency, 24-bit ADCs and DACs
  - 102 dB SNR (through PGA and ADC with A weighted filter)
  - 108 dB combined SNR (through DAC and headphone with A weighted filter)
- Serial port sampling rate from 8 kHz to 192 kHz
- 5 µs analog-to-analog latency
- 4 single-ended analog inputs, configurable as microphone or line inputs
- Dual stereo digital microphone inputs
- Stereo analog audio output, single-ended or differential, configurable as either line output or headphone driver
- PLL supporting any input clock rate from 8 MHz to 27 MHz
- Full duplex, asynchronous sample rate converters (ASRCs)
- Power supplies
  - Analog and digital input/output of 1.8 V to 3.3 V
  - Digital signal processing (DSP) core of 1.1 V to 1.8 V
- Low power
- I²C and SPI control interfaces, self boot from I²C EEPROM
- 7 multipurpose (MPx) pins for digital controls and outputs

## APPLICATIONS

- Noise canceling handsets, headsets, and headphones
- Bluetooth® active noise canceling (ANC) handsets, headsets, and headphones
- Personal navigation devices
- Digital still and video cameras

## GENERAL DESCRIPTION

The ADAU1777 is a codec with four inputs and two outputs that incorporates a digital processing engine to perform filtering, level control, signal level monitoring, and mixing. The path from the analog input to the DSP core to the analog output is optimized for low latency and is ideal for noise canceling headsets. With the addition of just a few passive components, a crystal, and an EEPROM for booting, the ADAU1777 provides a complete headset solution.

Note that throughout this data sheet, multifunction pins, such as SCL/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

## FUNCTIONAL BLOCK DIAGRAM

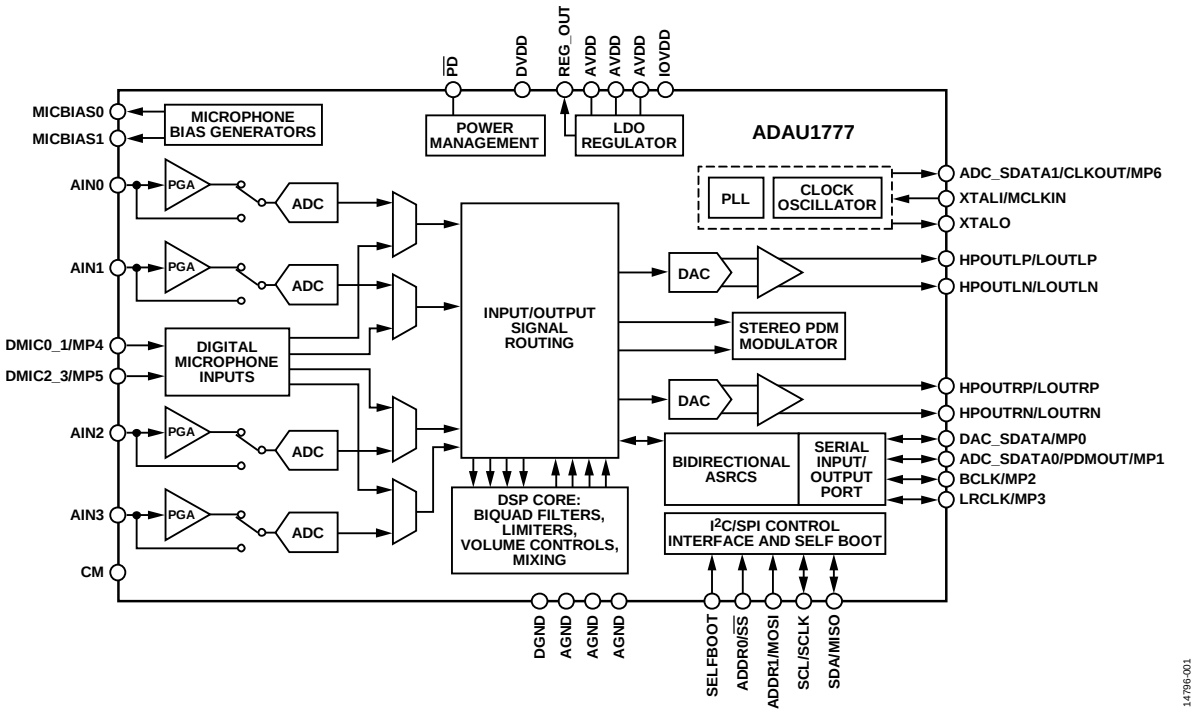



*Figure 1.*


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## REVISION HISTORY

**12/2016—Revision 0: Initial Version**

# SPECIFICATIONS

Master clock = 12.288 MHz, serial input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, $T_A$ = 25°C, outputs line loaded with 10 kΩ.

## ANALOG PERFORMANCE SPECIFICATIONS

AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted. Phase-locked loop (PLL) disabled, direct master clock.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ANALOG-TO-DIGITAL CONVERTERS (ADCs) | | | | | |
| ADC Resolution | All ADCs | | 24 | | Bits |
| Digital Attenuation Step | | | 0.375 | | dB |
| Digital Attenuation Range | | | 95 | | dB |
| INPUT RESISTANCE | Gain settings do not include 10 dB gain from PGA_x_BOOST settings; this additional gain does not affect input impedance; PGA_POP_DISx = 1 | | | | |
| Single-Ended Line Input | 0 dB gain | | 14.3 | | kΩ |
| Programmable Gain Amplifier (PGA) Inputs | −12 dB gain | | 32.0 | | kΩ |
| | 0 dB gain | | 20 | | kΩ |
| | +35.25 dB gain | | 0.68 | | kΩ |
| LINE INPUT | PGA_ENx = 0, PGA_x_BOOST = 0, PGA_POP_DISx = 1 | | | | |
| Full-Scale Input Voltage | Scales linearly with AVDD | | AVDD/3.3 | | V rms |
| | AVDD = 1.8 V | | 0.55 | | V rms |
| | AVDD = 1.8 V | | 1.54 | | V p-p |
| | AVDD = 3.3 V | | 1.00 | | V rms |
| | AVDD = 3.3 V | | 2.83 | | V p-p |
| Dynamic Range[1] | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 95 | 97 | | dB |
| | AVDD = 3.3 V | 99 | 102 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 92 | 94 | | dB |
| | AVDD = 3.3 V | 96 | 99 | | dB |
| Signal-to-Noise Ratio (SNR)[2] | | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 96 | 98 | | dB |
| | AVDD = 3.3 V | 100 | 103 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 92 | 96 | | dB |
| | AVDD = 3.3 V | 96 | 100 | | dB |
| Interchannel Gain Mismatch | | 0 | 40 | 200 | mdB |
| Total Harmonic Distortion + Noise (THD + N) | 20 Hz to 20 kHz, −1 dB from full-scale input | | | | |
| | AVDD = 1.8 V | | −90 | −83 | dB |
| | AVDD = 3.3 V | | −94 | −87 | dB |
| Offset Error | | −0.11 | | +0.12 | mV |
| Gain Error | | −0.4 | | +0.2 | dB |
| Interchannel Isolation | CM capacitor = 22 µF | | 95 | | dB |
| Power Supply Rejection Ratio (PSRR) | CM capacitor = 22 µF, 100 mV p-p at 1 kHz | | 55 | | dB |
| PGA INPUT | PGA_ENx = 1, PGA_x_BOOST = 0 | | | | |
| Full-Scale Input Voltage | Scales linearly with AVDD | | AVDD/3.3 | | V rms |
| | AVDD = 1.8 V | | 0.55 | | V rms |
| | AVDD = 1.8 V | | 1.54 | | V p-p |
| | AVDD = 3.3 V | | 1.00 | | V rms |
| | AVDD = 3.3 V | | 2.83 | | V p-p |
| Dynamic Range[1] | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 94 | | dB |
| | AVDD = 3.3 V | | 102 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 92 | | dB |
| | AVDD = 3.3 V | | 98 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| THD + N | 20 Hz to 20 kHz, −1 dB from full-scale input | | | | |
| | AVDD = 1.8 V | | −88 | | dB |
| | AVDD = 3.3 V | | −90 | | dB |
| SNR[2] | | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 94 | | dB |
| | AVDD = 3.3 V | | 102 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 93 | | dB |
| | AVDD = 3.3 V | | 98 | | dB |
| PGA Gain Variation | Standard deviation | | | | |
| With −12 dB Setting | | | 0.05 | | dB |
| With +35.25 dB Setting | | | 0.15 | | dB |
| PGA Boost | PGA_x_BOOST | | 10 | | dB |
| PGA Mute Attenuation | PGA_MUTEx | | −63 | | dB |
| Interchannel Gain Mismatch | | | 0.04 | | dB |
| Offset Error | | −0.12 | | +0.12 | mV |
| Gain Error | | | −0.05 | | dB |
| Interchannel Isolation | | | 100 | | dB |
| PSRR | CM capacitor = 20 µF, 100 mV p-p at 1 kHz | | 63 | | dB |
| MICROPHONE BIAS | MIC_ENx = 1 | | | | |
| Bias Voltage | | | | | |
| 0.65 × AVDD | AVDD = 1.8 V, MIC_GAINx = 1 | 1.14 | 1.16 | 1.17 | V |
| | AVDD = 3.3 V, MIC_GAINx = 1 | 2.10 | 2.12 | 2.14 | V |
| 0.90 × AVDD | AVDD = 1.8 V, MIC_GAINx = 0 | 1.61 | 1.63 | 1.65 | V |
| | AVDD = 3.3 V, MIC_GAINx = 0 | 2.95 | 2.97 | 2.99 | V |
| Bias Current Source | | | | 3 | mA |
| Output Impedance | | | 1 | | Ω |
| MICBIASx Isolation | MIC_GAINx = 0 | | 95 | | dB |
| | MIC_GAINx = 1 | | 99 | | dB |
| Noise in the Signal Bandwidth | 20 Hz to 20 kHz, 4.7 µF decoupling capacitor, 5.0 kΩ load on the MICBIASx pins | | | | |
| AVDD = 1.8 V | MIC_GAINx = 0 | | 27 | | nV/√Hz |
| | MIC_GAINx = 1 | | 16 | | nV/√Hz |
| AVDD = 3.3 V | MIC_GAINx = 0 | | 35 | | nV/√Hz |
| | MIC_GAINx = 1 | | 19 | | nV/√Hz |
| DIGITAL-TO-ANALOG CONVERTERS (DACs) | | | | | |
| Resolution | All DACs | | 24 | | Bits |
| Digital Attenuation Step | | | 0.375 | | dB |
| Digital Attenuation Range | | | 95 | | dB |
| DAC SINGLE-ENDED OUTPUT | Single-ended operation, HPOUTLP/LOUTLP and HPOUTRP/LOUTRP pins | | | | |
| Full-Scale Output Voltage | Scales linearly with AVDD | | AVDD/3.4 | | V rms |
| | AVDD = 1.8 V | | 0.53 | | V rms |
| | AVDD = 1.8 V | | 1.5 | | V p-p |
| | AVDD = 3.3 V | | 0.97 | | V rms |
| | AVDD = 3.3 V | | 2.74 | | V p-p |
| Mute Attenuation | | | −72 | | dB |
| Line Output Mode | | | | | |
| Dynamic Range[1] | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 97 | 100 | | dB |
| | AVDD = 3.3 V | 102 | 104 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 95 | 97 | | dB |
| | AVDD = 3.3 V | 99 | 101 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SNR[2] | 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 98 | 100 | | dB |
| | AVDD = 3.3 V | 102 | 104 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 96 | 98 | | dB |
| | AVDD = 3.3 V | 99 | 102 | | dB |
| Interchannel Gain Mismatch | | 0 | 50 | 200 | mdB |
| THD + N | 20 Hz to 20 kHz, −1 dBFS input | | | | dB |
| | AVDD = 1.8 V | | −93 | −89 | dB |
| | AVDD = 3.3 V | | −94 | −90 | dB |
| Gain Error | | −0.13 | | +0.13 | dB |
| Headphone Mode | | | | | |
| Dynamic Range[1] | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 97 | 100 | | dB |
| | AVDD = 3.3 V | 102 | 104 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 95 | 97 | | dB |
| | AVDD = 3.3 V | 99 | 101 | | dB |
| SNR[2] | 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 98 | 100 | | dB |
| | AVDD = 3.3 V | 102 | 104 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 96 | 98 | | dB |
| | AVDD = 3.3 V | 100 | 102 | | dB |
| Interchannel Gain Mismatch | | 0 | 50 | 230 | mdB |
| THD + N | 20 Hz to 20 kHz, −1 dBFS input | | | | |
| 32 Ω Load | AVDD = 1.8 V, output power = 6.3 mW | | −79 | −67 | dB |
| | AVDD = 3.3 V, output power = 20.5 mW | | −84 | −67 | dB |
| 24 Ω Load | AVDD = 1.8 V, output power = 8.4 mW | | −79 | −65 | dB |
| | AVDD = 3.3 V, output power = 27 mW | | −80 | −64 | dB |
| 16 Ω Load | AVDD = 1.8 V, output power = 13 mW | | −74 | −61 | dB |
| | AVDD = 3.3 V, output power = 30 mW | | −77 | −67 | dB |
| Gain Error | | −0.13 | | +0.13 | dB |
| Headphone Output Power | | | | | |
| 32 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 8.0 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 28.1 | | mW |
| 24 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 11.1 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 30.5 | | mW |
| 16 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 16.5 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 32.7 | | mW |
| Offset Error | | −0.11 | | +0.09 | mV |
| Interchannel Isolation | 1 kHz, 0 dBFS input signal | | 100 | | dB |
| PSRR | CM capacitor = 22 µF, 100 mV p-p at 1 kHz | | 70 | | dB |
| DAC DIFFERENTIAL OUTPUT | Differential operation | | | | |
| Full-Scale Output Voltage | Scales linearly with AVDD | | AVDD/1.7 | | V rms |
| | AVDD = 1.8 V | | 1.06 | | V rms |
| | AVDD = 1.8 V | | 3.00 | | V p-p |
| | AVDD = 3.3 V | | 1.94 | | V rms |
| | AVDD = 3.3 V | | 5.49 | | V p-p |
| Mute Attenuation | | | −72 | | dB |
| Line Output Mode | | | | | |
| Dynamic Range[1] | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 102 | 105 | | dB |
| | AVDD = 3.3 V | 105 | 107 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 100 | 102 | | dB |
| | AVDD = 3.3 V | 102 | 105 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SNR[2] | 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 103 | 105 | | dB |
| | AVDD = 3.3 V | 106 | 108 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 100 | 102 | | dB |
| | AVDD = 3.3 V | 103 | 105 | | dB |
| Interchannel Gain Mismatch | | 0 | 50 | 200 | mdB |
| THD + N | 20 Hz to 20 kHz, −1 dBFS input | | | | dB |
| | AVDD = 1.8 V | | −96 | −90 | dB |
| | AVDD = 3.3 V | | −96 | −90 | dB |
| Gain Error | | −0.1 | | +0.16 | dB |
| Headphone Mode | | | | | |
| Dynamic Range[1] | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 102 | 105 | | dB |
| | AVDD = 3.3 V | 105 | 107 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 100 | 102 | | dB |
| | AVDD = 3.3 V | 102 | 104 | | dB |
| SNR[2] | 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | 103 | 106 | | dB |
| | AVDD = 3.3 V | 106 | 108 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | 101 | 103 | | dB |
| | AVDD = 3.3 V | 104 | 106 | | dB |
| Interchannel Gain Mismatch | | 0 | 75 | 370 | mdB |
| THD + N | | | | | |
| 32 Ω Load | −1 dBFS, AVDD = 1.8 V, output power = 26 mW | | −75 | −64 | dB |
| | −1 dBFS, AVDD = 3.3 V, output power = 87 mW | | −83 | −75 | dB |
| 24 Ω Load | −2 dBFS, AVDD = 1.8 V, output power = 27 mW | | −75 | −64 | dB |
| | −1 dBFS, AVDD = 3.3 V, output power = 115 mW | | −82 | −75 | dB |
| 16 Ω Load | −3 dBFS, AVDD = 1.8 V, output power = 32 mW | | −75 | −65 | dB |
| | −1 dBFS, AVDD = 3.3 V, output power = 168 mW | | −77 | −68 | dB |
| Gain Error | Headphone mode | −0.25 | | +0.25 | dB |
| Headphone Output Power | | | | | |
| 32 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 29.1 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 111.8 | | mW |
| 24 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 31.8 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 148.3 | | mW |
| 16 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 32.3 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 193.0 | | mW |
| Offset Error | | −0.12 | 0 | +0.08 | mV |
| Interchannel Isolation | 1 kHz, 0 dBFS input signal | | 100 | | dB |
| PSRR | CM capacitor = 22 µF, 100 mV p-p at 1 kHz | | 73 | | dB |
| ANALOG-TO-ANALOG LATENCY | $f_S$ = 768 kHz | | 5 | | µs |
| | $f_S$ = 192 kHz | | 38 | | µs |
| CM REFERENCE | CM pin | | | | |
| Common-Mode Reference Output | | | AVDD/2 | | V |
| Common-Mode Source Impedance | | | 5 | | kΩ |
| REGULATOR | | | | | |
| Line Regulation | | | 1 | | mV/V |
| Load Regulation | | | 6 | | mV/mA |

[1] Dynamic range is the ratio of the sum of the noise and harmonic power in the band of interest with a −60 dBFS signal present vs. the full-scale power level in decibels.
[2] SNR is the ratio of the sum of all noise power in the band of interest with no signal present vs. the full-scale power level in decibels.

## CRYSTAL AMPLIFIER SPECIFICATIONS

AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| CRYSTAL AMPLIFIER | | | | |
| Jitter | | 270 | 500 | ps rms |
| Frequency Range | 8 | | 27 | MHz |
| Load Capacitance | | | 20 | pF |

## DIGITAL INPUT/OUTPUT SPECIFICATIONS

−40°C < $T_A$ < +85°C, IOVDD = 3.3 V ± 10% and 1.8 V − 5% to 1.8 V + 10%, unless otherwise noted.

**Table 3.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| INPUT/OUTPUT | | | | | |
| Input Voltage | | | | | |
| High ($V_{IH}$) | IOVDD = 3.3 V | 2.0 | | | V |
| | IOVDD = 1.8 V | 1.1 | | | V |
| Low ($V_{IL}$) | IOVDD = 3.3 V | | | 0.8 | V |
| | IOVDD = 1.8 V | | | 0.45 | V |
| Input Leakage | IOVDD = 3.3 V, $I_{IH}$[1] at $V_{IH}$ = 2.0 V | | | 10 | µA |
| | $I_{IL}$[1] at $V_{IL}$ = 0.8 V | | | 10 | µA |
| | IOVDD = 1.8 V, $I_{IH}$[1] at $V_{IH}$ = 1.1 V | | | 10 | µA |
| | $I_{IL}$[1] at $V_{IL}$ = 0.45 V | | | 10 | µA |
| Output Voltage High ($V_{OH}$) | | | | | |
| Low Drive Strength | $I_{OH}$[1] = 1 mA | IOVDD − 0.6 | | | V |
| High Drive Strength | $I_{OH}$[1] = 3 mA | IOVDD − 0.6 | | | V |
| Output Voltage Low ($V_{OL}$) | | | | | |
| Low Drive Strength | $I_{OL}$[1] = 1 mA | | | 0.4 | V |
| High Drive Strength | $I_{OL}$[1] = 3 mA | | | 0.4 | V |
| Input Capacitance | | | | 5 | pF |

[1] $I_{IH}$ is the current when the input is high; $I_{IL}$ is the current when the input is low; $I_{OH}$ is the current when the output is high; and $I_{OL}$ is the current when the output is low.

## POWER SUPPLY SPECIFICATIONS

AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted.

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SUPPLIES | | | | | |
| AVDD Voltage | | 1.71 | 1.8 | 3.63 | V |
| DVDD Voltage | | 1.045 | 1.1 | 1.98 | V |
| IOVDD Voltage | | 1.71 | 1.8 | 3.63 | V |
| Analog Current ($I_{AVDD}$) | | | | | |
| Normal Operation | See Table 5 | | | | |
| Power-Down | | | 1.6 | | µA |
| Digital Input/Output Current ($I_{IOVDD}$) | | | | | |
| Normal Operation | See Table 5 | | | | |
| Power-Down | | | 1.3 | | µA |
| POWER CONSUMPTION | | | | | |
| All Supplies | See Table 5 | | | | |
| Power-Down, All Supplies | | | 1 | | µW |

## TYPICAL POWER MANAGEMENT SETTINGS

Typical ANC settings, master clock = 12.288 MHz, PLL disabled, crystal oscillator enabled, core $f_S$ = DAC = ADC = 768 kHz. On-board regulator enabled. Two ADCs with PGA enabled and two ADCs configured for line input, no input signal. Two DACs are configured for differential headphone (HP) operation; DAC outputs are unloaded. Both MICBIAS0 and MICBIAS1 enabled at 0.9 × AVDD. ASRCs and pulse density modulation (PDM) modulator disabled. Core running 26 out of 32 possible instructions. Serial port set to slave. See Register 0x46 and Register 0x47 for settings.

**Table 5.**

| Operating Voltage | Power Management Setting | Typical AVDD Current Consumption (mA) | Typical IOVDD Current Consumption (mA) | Typical ADC THD + N (dB) | Typical HP Output THD + N (dB) | Total Power Consumption (mW) |
|---|---|---|---|---|---|---|
| AVDD = IOVDD = 3.3 V | Normal | 9.71 | 2.58 | −91 | −97 | 40.56 |
| | Extreme power saving | 7.55 | 2.57 | −86 | −96 | 33.40 |
| | Power saving | 7.99 | 2.57 | −87 | −96 | 34.85 |
| | Enhanced performance | 10.97 | 2.58 | −91 | −98 | 44.72 |
| AVDD = IOVDD = 1.8 V | Normal | 7.29 | 0.37 | −87 | −95 | 13.79 |
| | Extreme power saving | 5.38 | 0.37 | −81 | −89 | 10.35 |
| | Power saving | 5.73 | 0.37 | −81 | −90 | 10.98 |
| | Enhanced Performance | 8.62 | 0.37 | −87 | −95 | 16.18 |

## DIGITAL FILTERS SPECIFICATIONS

**Table 6.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC INPUT TO DAC OUTPUT PATH | | | | | |
| Pass-Band Ripple | DC to 20 kHz, $f_S$ = 768 kHz | −0.03 | | +0.01 | dB |
| | DC to 20 kHz, $f_S$ = 192 kHz | | | ±0.02 | dB |
| SAMPLE RATE CONVERTER | | | | | |
| Pass Band | LRCLK < 63 kHz | 0 | | 0.475 × $f_S$ | kHz |
| | 63 kHz < LRCLK <130 kHz | 0 | | 0.4286 × $f_S$ | kHz |
| | LRCLK > 130 kHz | 0 | | 0.4286 × $f_S$ | kHz |
| Pass-Band Ripple | Upsampling, 96 kHz | −0.27 | | +0.05 | dB |
| | Upsampling, 192 kHz | −0.06 | | +0.05 | dB |
| | Downsampling, 96 kHz | 0 | | 0.07 | dB |
| | Downsampling, 192 kHz | 0 | | 0.07 | dB |
| Input/Output Frequency Range | | 8 | | 192 | kHz |
| Dynamic Range | | | 100 | | dB |
| THD + N | | | −90 | | dB |
| Start-Up Time | | | | 15 | ms |
| PDM MODULATOR | | | | | |
| Dynamic Range (A-Weighted) | | | 112 | | dB |
| THD + N | | | −92 | | dB |

## DIGITAL TIMING SPECIFICATIONS

−40°C < $T_A$ < +85°C, IOVDD = 1.71 V to 3.63 V, DVDD = 1.045 V to 1.98 V.

**Table 7. Digital Timing**

| | Limit | | | |
|---|---|---|---|---|
| **Parameter** | **$t_{MIN}$** | **$t_{MAX}$** | **Unit** | **Description** |
| MASTER CLOCK (MCLK) | | | | |
| $t_{MP}$ | 37 | 125 | ns | MCLKIN period; 8 MHz to 27 MHz input clock using PLL |
| $t_{MCLK}$ | 77 | 82 | ns | Internal MCLK period; direct MCLK and PLL output divided by 2 |
| SERIAL PORT | | | | |
| $t_{BL}$ | 40 | | ns | BCLK low pulse width (master and slave modes) |
| $t_{BH}$ | 40 | | ns | BCLK high pulse width (master and slave modes) |
| $t_{LS}$ | 10 | | ns | LRCLK setup; time to BCLK rising (slave mode) |
| $t_{LH}$ | 10 | | ns | LRCLK hold; time from BCLK rising (slave mode) |
| $t_{SS}$ | 5 | | ns | DAC_SDATA setup; time to BCLK rising (master and slave modes) |
| $t_{SH}$ | 5 | | ns | DAC_SDATA hold; time from BCLK rising (master and slave modes) |
| $t_{TS}$ | | 10 | ns | BCLK falling to LRCLK timing skew (master mode) |
| $t_{SOD}$ | 0 | 34 | ns | ADC_SDATAx delay; time from BCLK falling (master and slave modes) |
| $t_{SOTD}$ | | 30 | ns | BCLK falling to ADC_SDATAx driven in time-division multiplexing (TDM) tristate mode |
| $t_{SOTX}$ | | 30 | ns | BCLK falling to ADC_SDATAx tristate in TDM tristate mode |
| SERIRAL PERIPHERAL INTERFACE (SPI) PORT | | | | |
| $f_{SCLK}$ | | 6.25 | MHz | SCLK frequency |
| $t_{CCPL}$ | 80 | | ns | SCLK pulse width low |
| $t_{CCPH}$ | 80 | | ns | SCLK pulse width high |
| $t_{CLS}$ | 5 | | ns | $\overline{SS}$ setup; time to SCLK rising |
| $t_{CLH}$ | 100 | | ns | $\overline{SS}$ hold; time from SCLK rising |
| $t_{CLPH}$ | 80 | | ns | $\overline{SS}$ pulse width high |
| $t_{CDS}$ | 10 | | ns | MOSI setup; time to SCLK rising |
| $t_{CDH}$ | 10 | | ns | MOSI hold; time from SCLK rising |
| $t_{COD}$ | | 101 | ns | MISO delay; time from SCLK falling |
| I²C PORT | | | | |
| $f_{SCL}$ | | 400 | kHz | SCL frequency |
| $t_{SCLH}$ | 0.6 | | µs | SCL high |
| $t_{SCLL}$ | 1.3 | | µs | SCL low |
| $t_{SCS}$ | 0.6 | | µs | SCL rise setup time (to SDA falling), relevant for repeated start condition |
| $t_{SCR}$ | | 250 | ns | SCL and SDA rise time, $C_{LOAD}$ = 400 pF |
| $t_{SCH}$ | 0.6 | | µs | SCL fall hold time (from SDA falling), relevant for start condition |
| $t_{DS}$ | 100 | | ns | SDA setup time (to SCL rising) |
| $t_{SCF}$ | | 250 | ns | SCL and SDA fall time; $C_{LOAD}$ = 400 pF |
| $t_{BFT}$ | 0.6 | | µs | SCL rise setup time (to SDA rising), relevant for stop condition |
| I²C EEPROM SELF BOOT | | | | |
| $t_{SCHE}$ | $26 \times t_{MP} - 70$ | | ns | SCL fall hold time (from SDA falling), relevant for start condition; $t_{MP}$ is the input clock on the MCLKIN pin |
| $t_{SCSE}$ | $38 \times t_{MP} - 70$ | | ns | SCL rise setup time (to SDA falling), relevant for repeated start condition |
| $t_{BFTE}$ | $70 \times t_{MP} - 70$ | | ns | SCL rise setup time (to SDA rising), relevant for stop condition |
| $t_{DSE}$ | $6 \times t_{MP} - 70$ | | ns | Delay from SCL falling to SDA changing |
| $t_{BHTE}$ | $32 \times t_{MP}$ | | ns | SDA rising in self boot stop condition to SDA falling edge for external master start condition |

| Parameter | Limit $t_{MIN}$ | Limit $t_{MAX}$ | Unit | Description |
|---|---|---|---|---|
| MULTIPURPOSE AND POWER-DOWN PINS | | | | |
| $t_{GIL}$ | | 1.5 × 1/$f_S$ | µs | MPx input latency; time until high or low value is read by core |
| $t_{RLPW}$ | 20 | | ns | $\overline{PD}$ low pulse width |
| DIGITAL MICROPHONE | | | | |
| $t_{CF}$ | | 20 | ns | Digital microphone clock fall time |
| $t_{CR}$ | | 20 | ns | Digital microphone clock rise time |
| $t_{DS}$ | 40 | | | Digital microphone valid data start time |
| $t_{DE}$ | | 0 | ns | Digital microphone valid data end time |
| PDM OUTPUT | | | | |
| $t_{DCF}$ | | 20 | ns | PDM clock fall time |
| $t_{DCR}$ | | 20 | ns | PDM clock rise time |
| $t_{DDV}$ | 0 | 30 | ns | PDM delay time for valid data |

### *Digital Timing Diagrams*

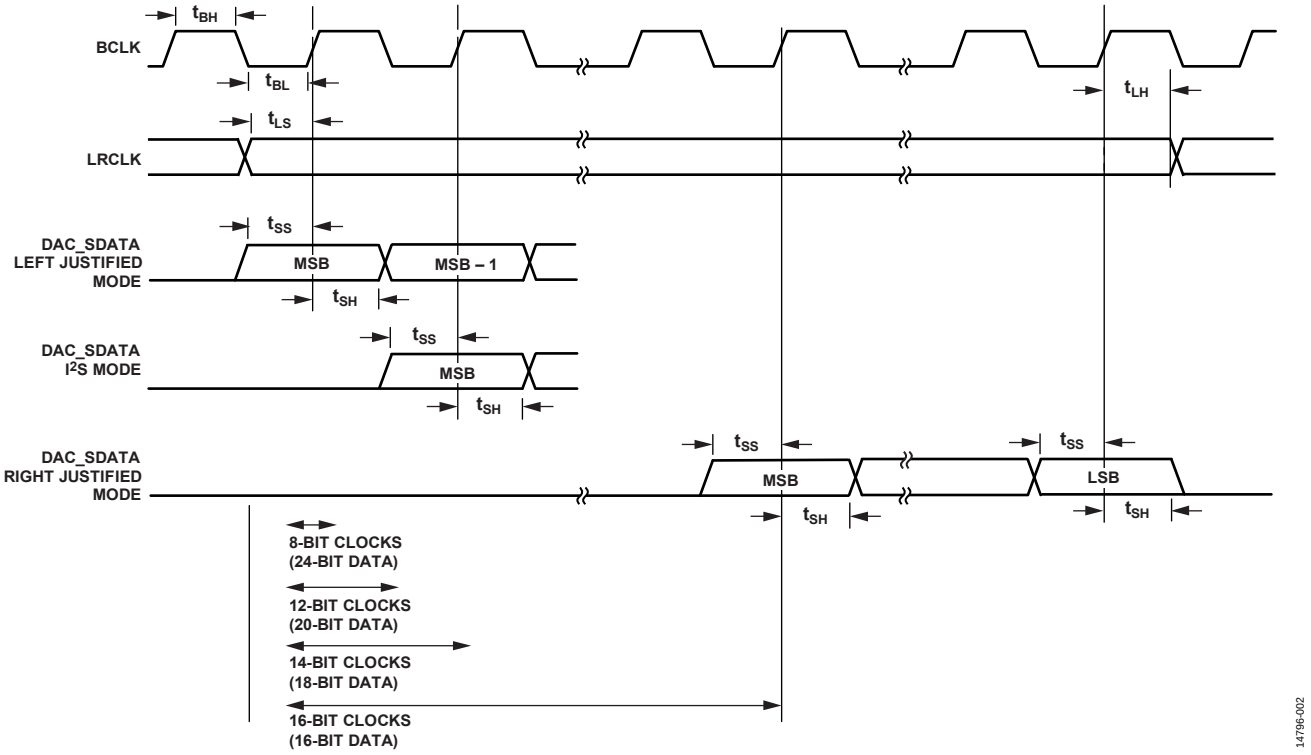



*Figure 2. Serial Input Port Timing*

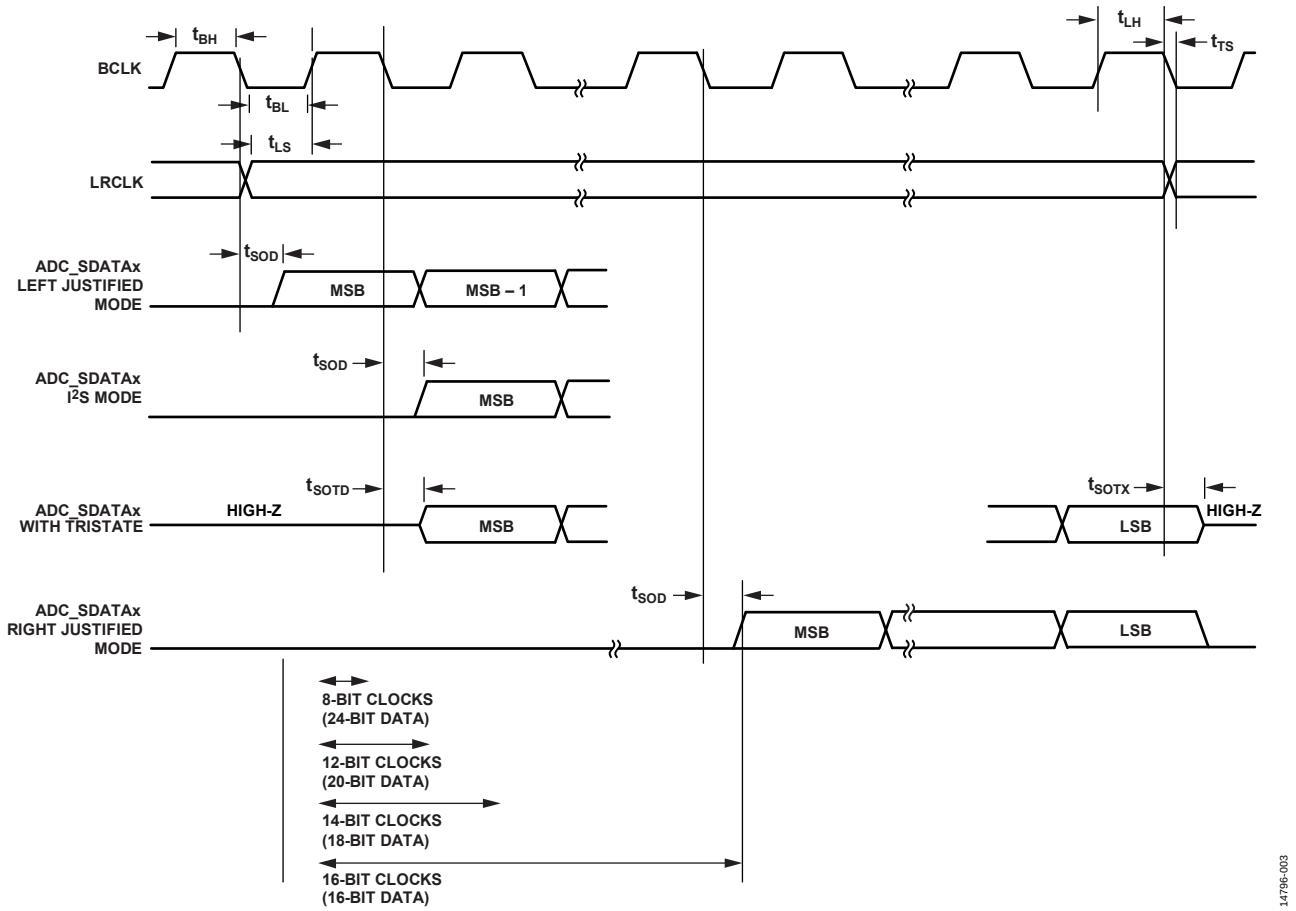



*Figure 3. Serial Output Port Timing*

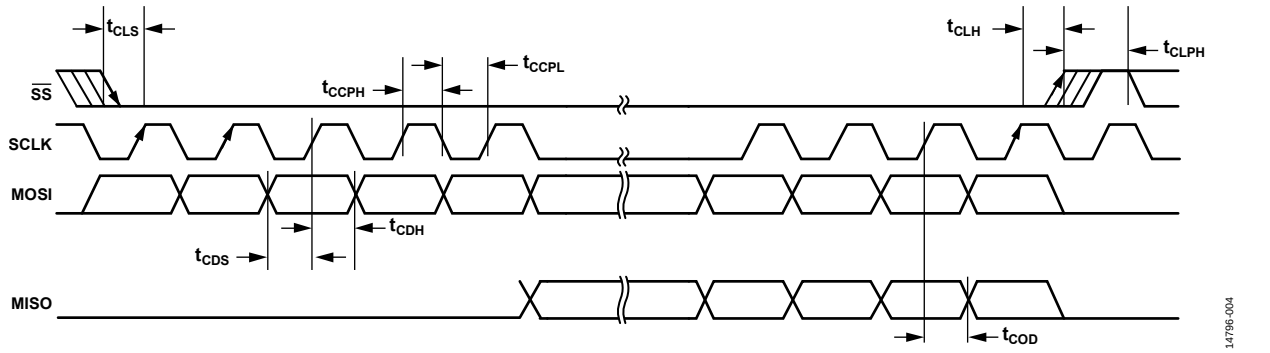



*Figure 4. SPI Port Timing*

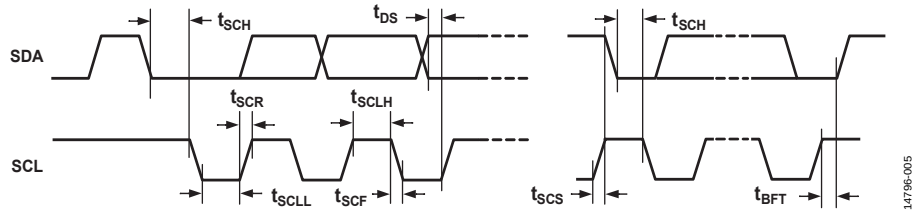



*Figure 5. I²C Port Timing*

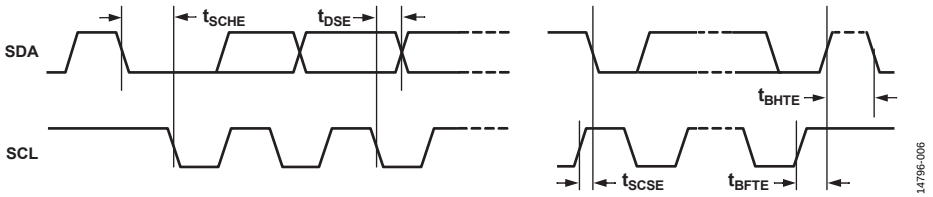



*Figure 6. I²C EEPROM Self Boot Timing*

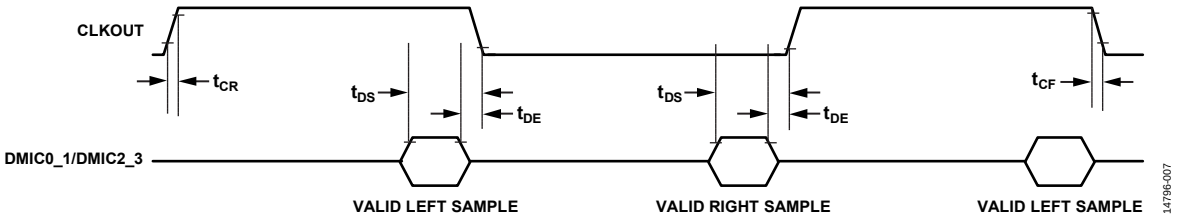



*Figure 7. Digital Microphone Timing*

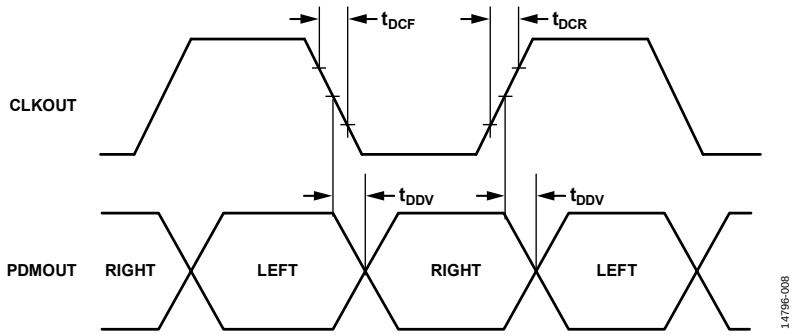



*Figure 8. PDM Output Timing*

# ABSOLUTE MAXIMUM RATINGS

**Table 8.**

| Parameter | Rating |
|---|---|
| Power Supplies (AVDD, IOVDD) | −0.3 V to +3.63 V |
| Digital Supply (DVDD) | −0.3 V to +1.98 V |
| Input Current (Except Supply Pins) | ±20 mA |
| Analog Input Voltage (Signal Pins) | −0.3 V to AVDD + 0.3 V |
| Digital Input Voltage (Signal Pins) | −0.3 to IOVDD + 0.3 V |
| Operating Temperature Range (Case) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. $\theta_{JA}$ is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure

For more information, see the AN-617 Application Note, *Wafer Level Chip Scale Package*.

**Table 9. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| CB-36-4[1] | 36 | °C/W |

[1] Thermal impedance simulated values are based on a 4-layer PCB with two signal layers and two power planes using natural convection cooling. See JEDEC JESD51-9.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

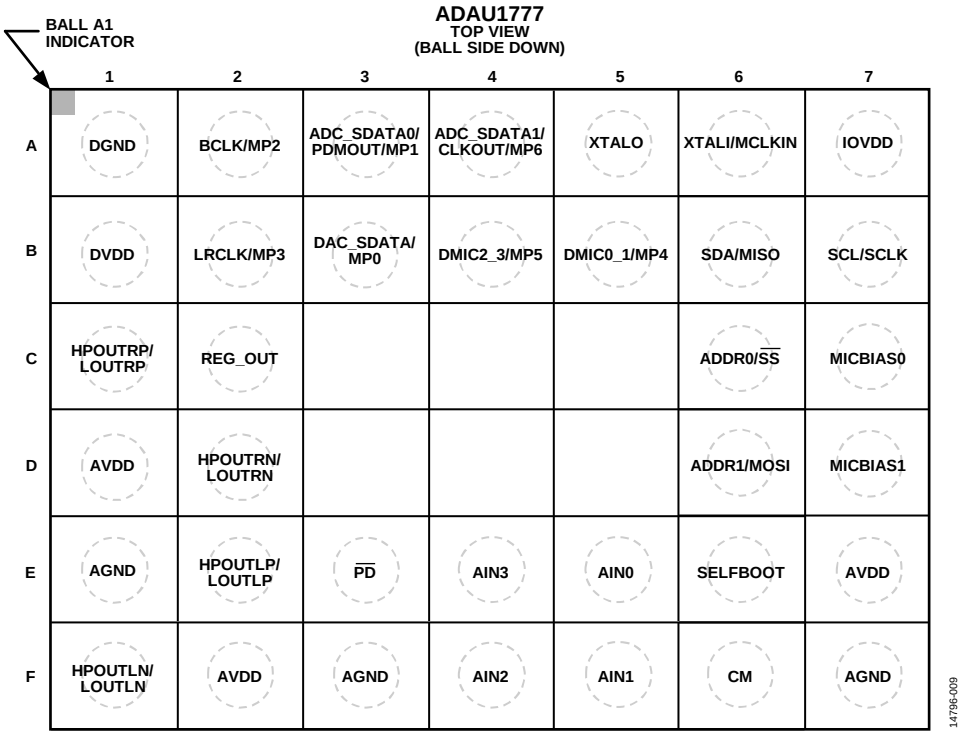



*Figure 9. Pin Configuration*

**Table 10. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| A1 | DGND | PWR | Digital Ground. Tie the AGND and DGND pins directly together in a common ground plane. |
| A2 | BCLK/MP2 | D_IO | Serial Data Port Bit Clock (BCLK).<br>Multipurpose Pin (MP2). |
| A3 | ADC_SDATA0/PDMOUT/MP1 | D_IO | ADC Serial Data Output 0 (ADC_SDATA0).<br>Stereo PDM Output to Drive a High Efficiency Class-D Amplifier (PDMOUT).<br>Multipurpose Pin (MP1). |
| A4 | ADC_SDATA1/CLKOUT/MP6 | D_IO | Serial Data Output 1 (ADC_SDATA1).<br>Master Clock Output/Clock for the Digital Microphone Input and PDM Output (CLKOUT).<br>Multipurpose Pin (MP6). |
| A5 | XTALO | A_OUT | Crystal Clock Output. This pin is the output of the crystal amplifier; do not use this pin to provide a clock to other ICs in the system. If a master clock output is needed, use CLKOUT (Pin A4). |
| A6 | XTALI/MCLKIN | D_IN | Crystal Clock Input (XTALI).<br>Master Clock Input (MCLKIN). |
| A7 | IOVDD | PWR | Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD; thus, the IOVDD voltage level is the highest input voltage that can be present on the digital input pins. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. Decouple IOVDD to DGND with a 0.1 µF capacitor. |
| B1 | DVDD | PWR | Digital Core Supply. The digital supply can be generated from an on-board regulator or supplied directly from an external supply. In each case, decouple DVDD to DGND with a 0.1 µF capacitor. |
| B2 | LRCLK/MP3 | D_IO | Serial Data Port Frame Clock (LRCLK).<br>Multipurpose Pin (MP3). |
| B3 | DAC_SDATA/MP0 | D_IO | DAC Serial Input Data (DAC_SDATA).<br>Multipurpose Pin (MP0). |
| B4 | DMIC2_3/MP5 | D_IN | Digital Microphone Stereo Input 2 and Digital Microphone Stereo Input 3 (DMIC2_3).<br>Multipurpose Pin (MP5). |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| B5 | DMIC0_1/MP4 | D_IN | Digital Microphone Stereo Input 0 and Digital Microphone Stereo Input 1 (DMIC0_1). |
| | | | Multipurpose Pin (MP4). |
| B6 | SDA/MISO | D_IO | I²C Data (SDA). This pin is a bidirectional open-collector. The line connected to this pin must have a 2.0 kΩ pull-up resistor. |
| | | | SPI Data Output (MISO). This SPI data output reads back registers and memory locations. It is tristated when an SPI read is not active. |
| B7 | SCL/SCLK | D_IN | I²C Clock (SCL). This pin is always an open-collector input when the device is in I²C control mode. When the device is in self boot mode, this pin is an open-collector output (I²C master). The line connected to this pin must have a 2.0 kΩ pull-up resistor. |
| | | | SPI Clock (SCLK). This pin either can run continuously or be gated off between SPI transactions. |
| C1 | HPOUTRP/LOUTRP | A_OUT | Right Headphone Output Noninverted (HPOUTRP). |
| | | | Line Output Noninverted, Single-Ended Line Output (LOUTRP). |
| C2 | REG_OUT | A_OUT | Regulator Output Voltage. Connect this pin to DVDD if the internal voltage regulator is being used to generate the DVDD voltage. |
| C6 | ADDR0/$\overline{SS}$ | D_IN | I²C Address 0 (ADDR0). |
| | | | SPI Latch Signal ($\overline{SS}$). This pin must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of SCLK cycles to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction. |
| C7 | MICBIAS0 | A_OUT | Bias Voltage for Electret Microphone. Decouple this pin with a 1 µF capacitor. |
| D1 | AVDD | PWR | Headphone Amplifier Power, 1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor. The PCB trace to this pin must have the capacity to supply the higher current necessary for driving the headphone outputs. |
| D2 | HPOUTRN/LOUTRN | A_OUT | Right Headphone Output Inverted (HPOUTRN). |
| | | | Line Output Inverted (LOUTRN). |
| D6 | ADDR1/MOSI | D_IN | I²C Address 1 (ADDR1). |
| | | | SPI Data Input (MOSI). |
| D7 | MICBIAS1 | A_OUT | Bias Voltage for Electret Microphone. Decouple this pin with a 1 µF capacitor. |
| E1 | AGND | PWR | Headphone Amplifier Ground. |
| E2 | HPOUTLP/LOUTLP | A_OUT | Left Headphone Output Noninverted (HPOUTLP). |
| | | | Line Output Noninverted, Single-Ended Line Output (LOUTLP). |
| E3 | $\overline{PD}$ | D_IN | Active Low Power-Down. All digital and analog circuits are powered down. An internal pull-down resistor is on this pin; therefore, the ADAU1777 is held in power-down mode if its input signal is floating while power is applied to the supply pins. |
| E4 | AIN3 | A_IN | ADC3 Input. |
| E5 | AIN0 | A_IN | ADC0 Input. |
| E6 | SELFBOOT | D_IN | Self Boot Enable. Pull this pin up to IOVDD at power-up to enable the self boot mode. |
| E7 | AVDD | PWR | 1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor. |
| F1 | HPOUTLN/LOUTLN | A_OUT | Left Headphone Output Inverted (HPOUTLN). |
| | | | Line Output Inverted (LOUTLN). |
| F2 | AVDD | PWR | 1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor. |
| F3 | AGND | PWR | Analog Ground. |
| F4 | AIN2 | A_IN | ADC2 Input. |
| F5 | AIN1 | A_IN | ADC1 Input. |
| F6 | CM | A_OUT | AVDD/2 V Common-Mode Reference. Connect a 10 µF to 47 µF decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp). |
| F7 | AGND | PWR | Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane. Decouple AGND to AVDD with a 0.1 µF capacitor. |

[1] PWR is power; D_IO is digital input/output; A_OUT is analog output; D_IN is digital input; and A_IN is analog input.

# TYPICAL PERFORMANCE CHARACTERISTICS

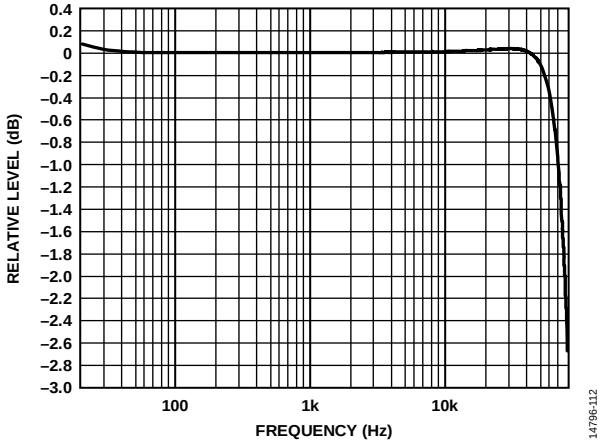



Figure 10. Relative Level vs. Frequency, $f_S$ = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

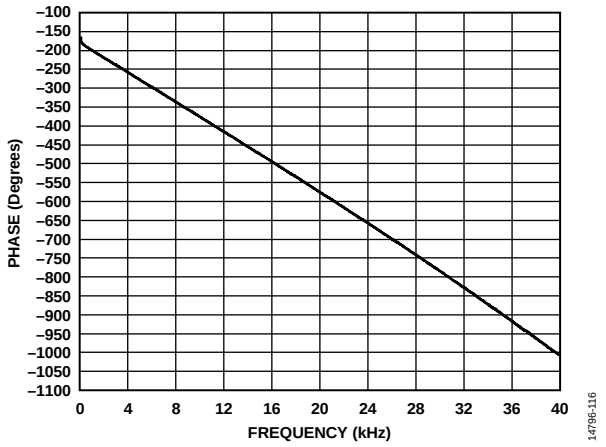



Figure 11. Phase vs. Frequency, 40 kHz Bandwidth, $f_S$ = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

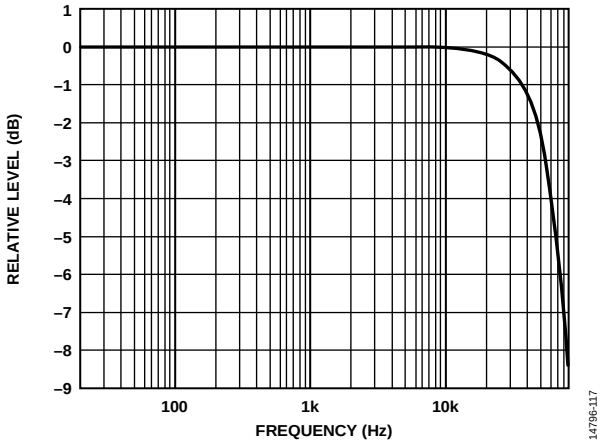



Figure 12. Relative Level vs. Frequency, $f_S$ = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

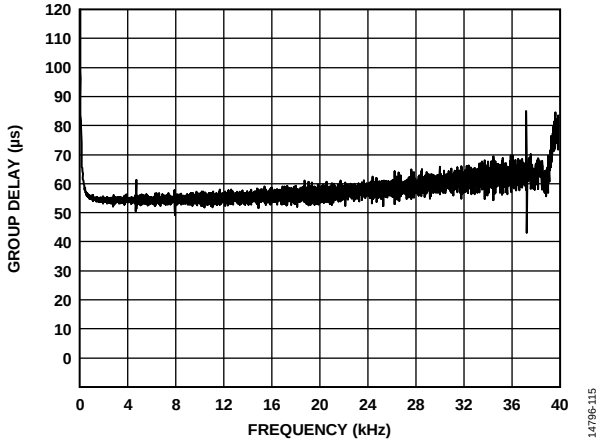



Figure 13. Group Delay vs. Frequency, $f_S$ = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

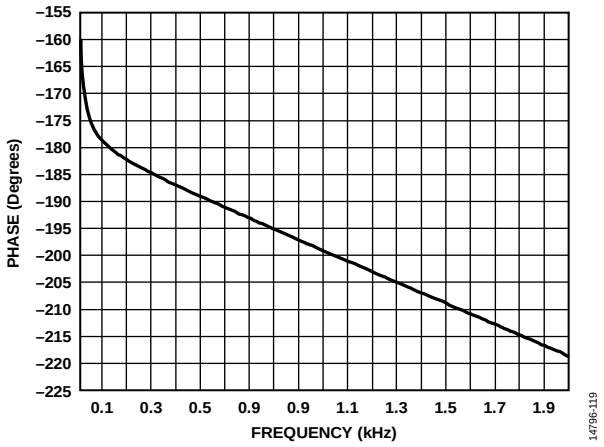



Figure 14. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

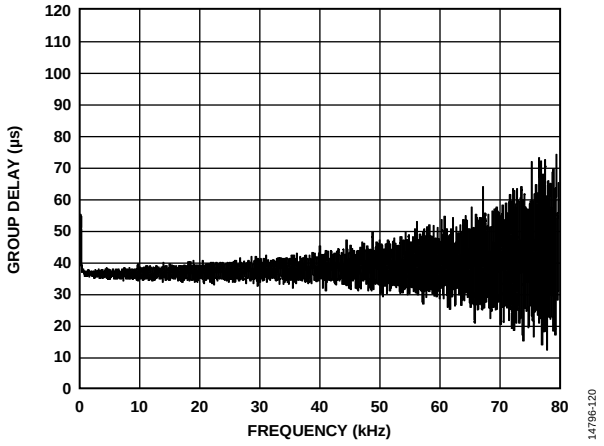



Figure 15. Group Delay vs. Frequency, $f_S$ = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

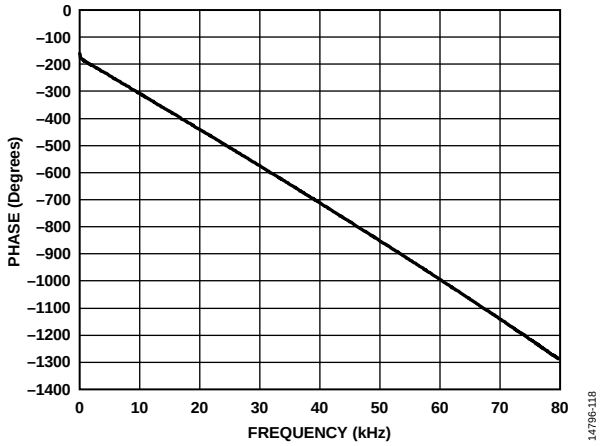



*Figure 16. Phase vs. Frequency, 80 kHz Bandwidth, $f_S$ = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx*

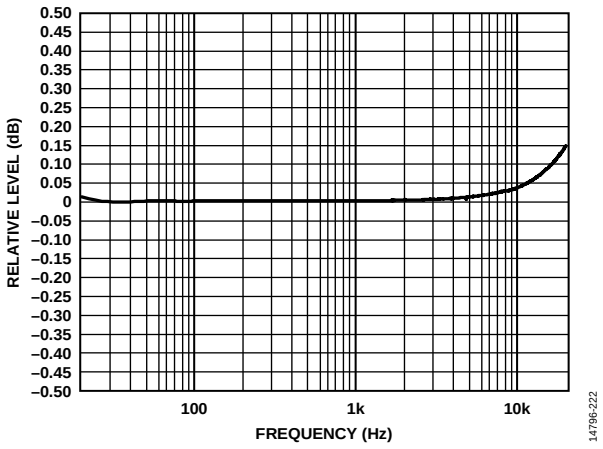



*Figure 17. Relative Level vs. Frequency, $f_S$ =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx*

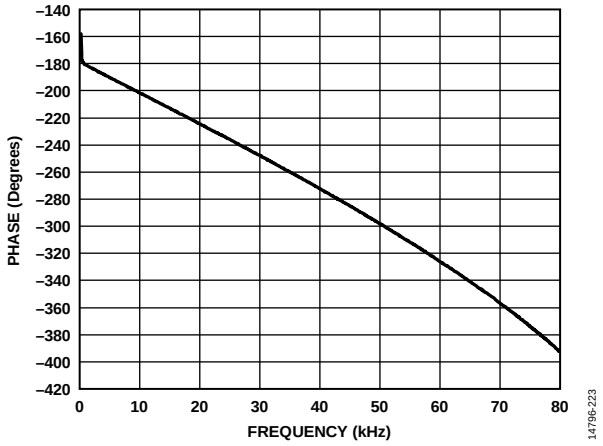



*Figure 18. Phase vs. Frequency, 80 kHz Bandwidth, $f_S$ =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx*

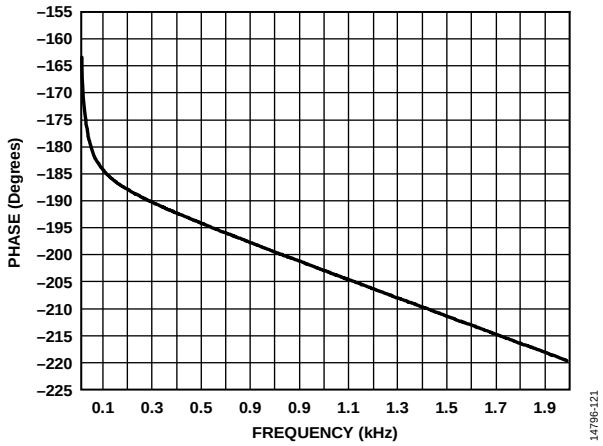



*Figure 19. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx*

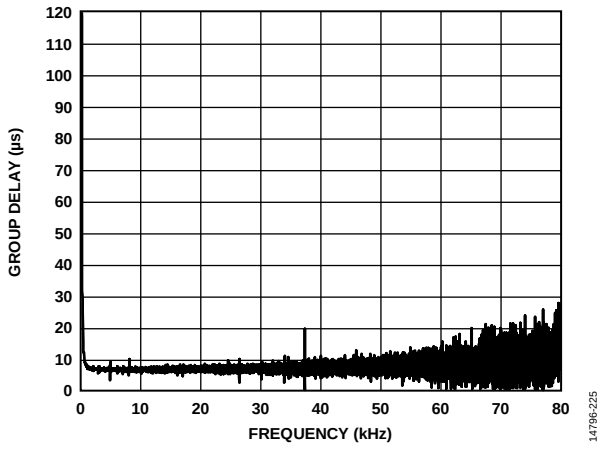



*Figure 20. Group Delay vs. Frequency, $f_S$ =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx*

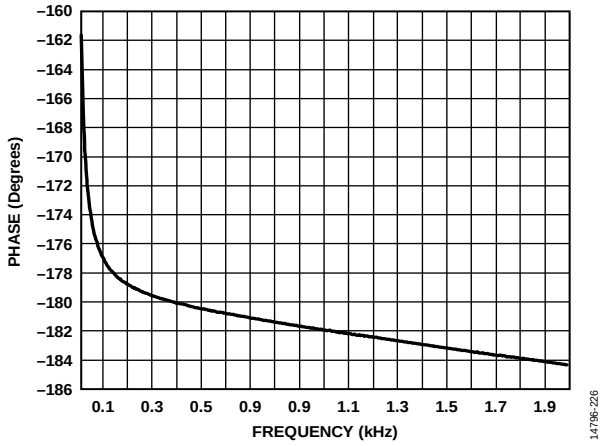



*Figure 21. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx*

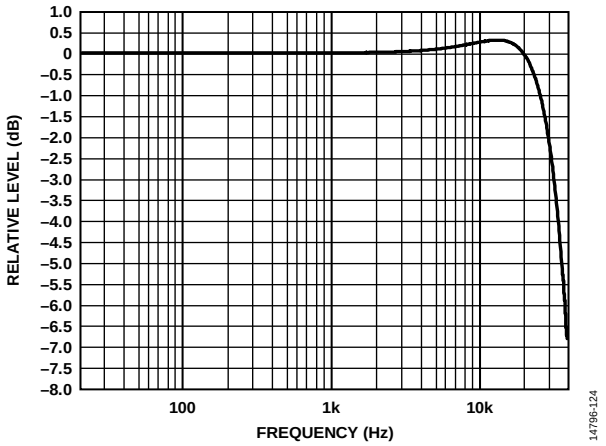



*Figure 22. Relative Level vs. Frequency, $f_S$ = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0*

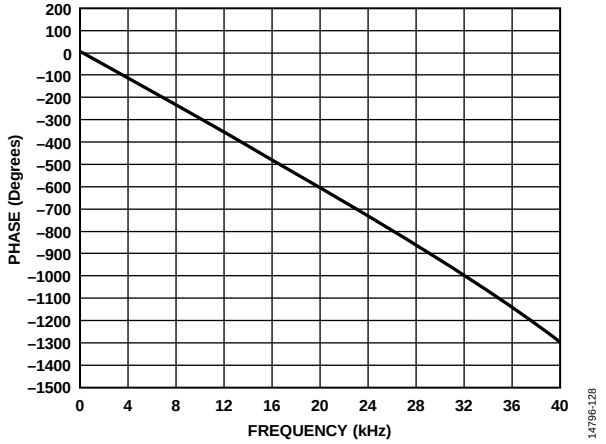



*Figure 23. Phase vs. Frequency, 40 kHz Bandwidth, $f_S$ = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0*

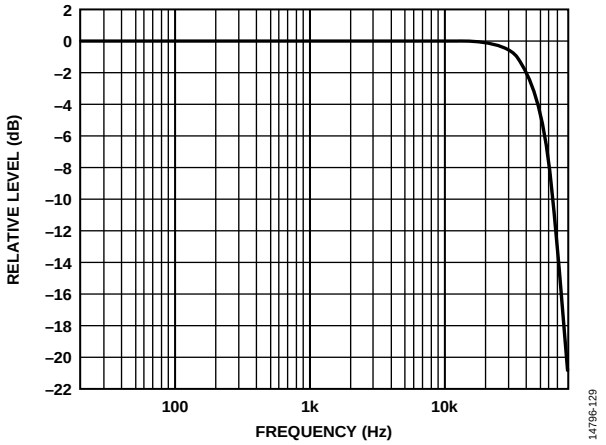



*Figure 24. Relative Level vs. Frequency, $f_S$ = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0*

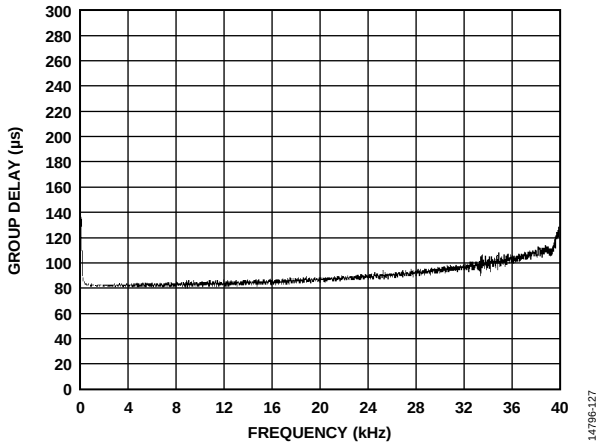



*Figure 25. Group Delay vs. Frequency, $f_S$ = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0*

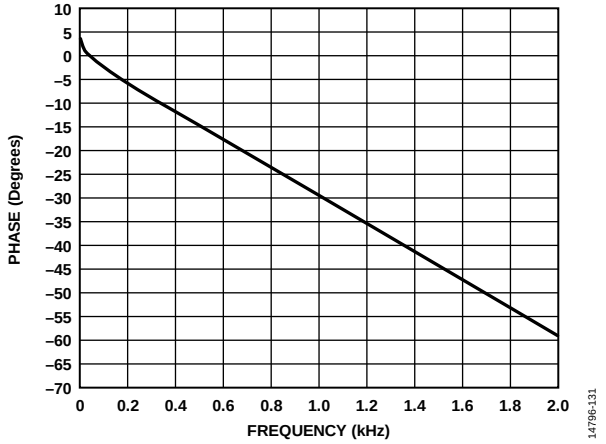



*Figure 26. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0*

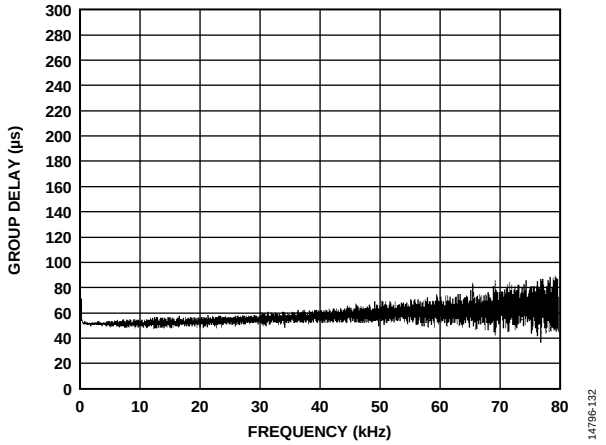



*Figure 27. Group Delay vs. Frequency, $f_S$ = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0*

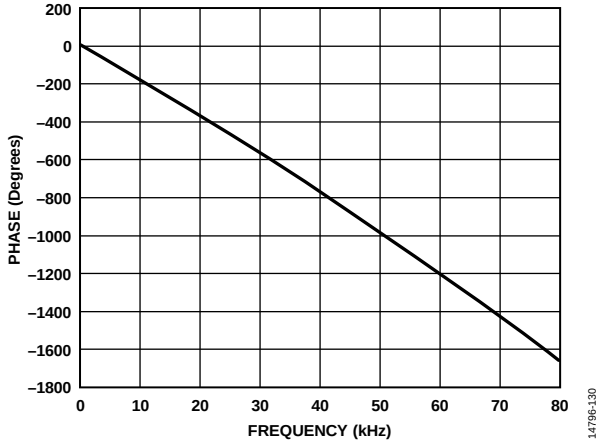



Figure 28. Phase vs. Frequency, 80 kHz Bandwidth, $f_S$ = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

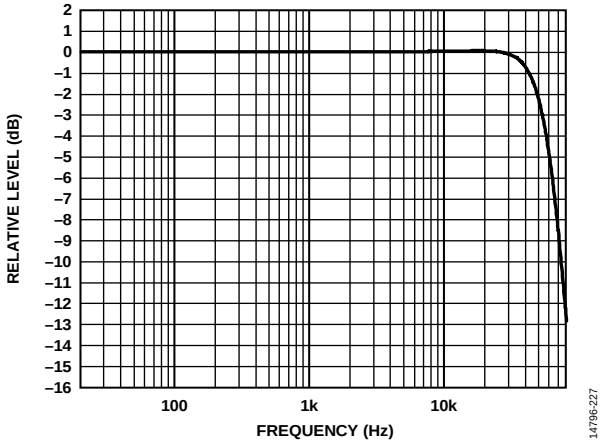



Figure 29. Relative Level vs. Frequency, $f_S$ = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

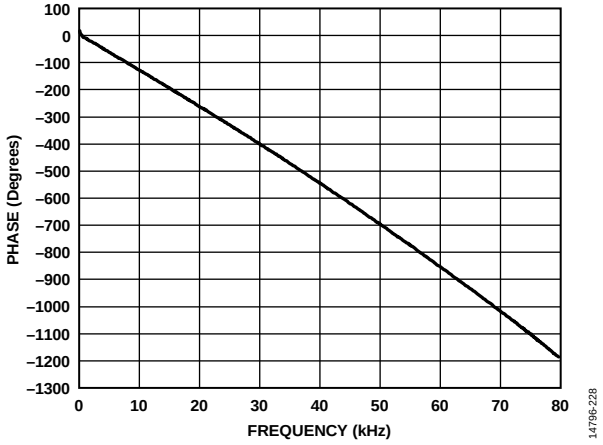



Figure 30. Phase vs. Frequency, 80 kHz Bandwidth, $f_S$ = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

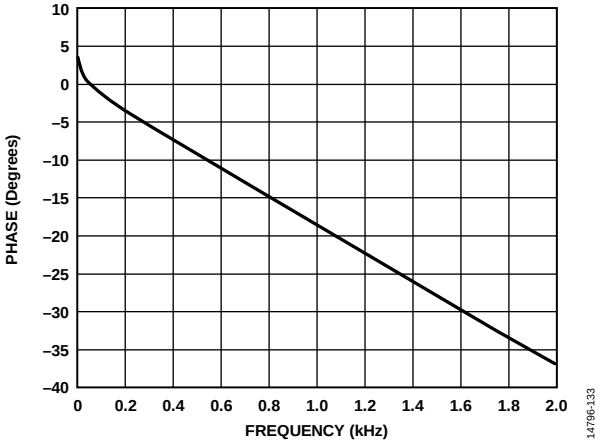



Figure 31. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

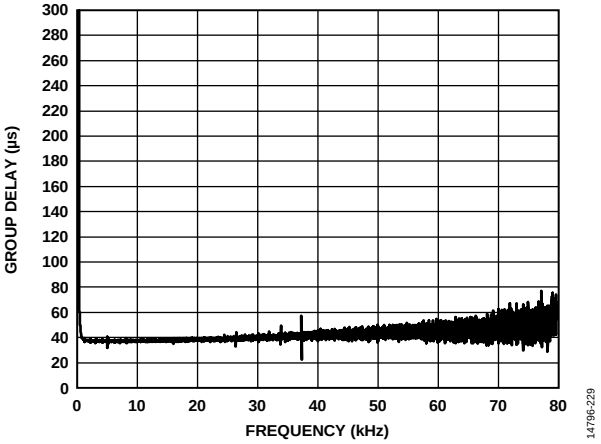



Figure 32. Group Delay vs. Frequency, $f_S$ = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

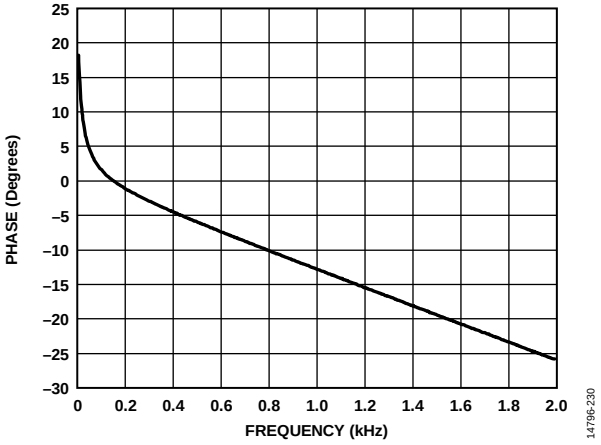



Figure 33. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

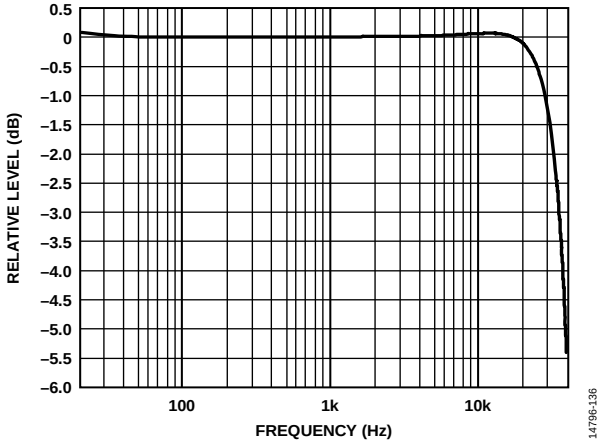



Figure 34. Relative Level vs. Frequency, $f_S$ = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

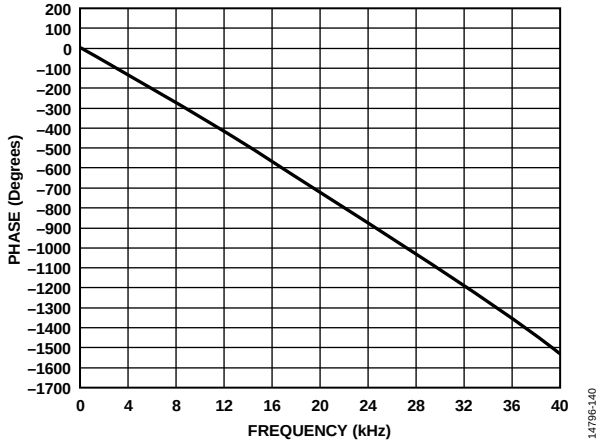



Figure 35. Phase vs. Frequency, 40 kHz Bandwidth, $f_S$ = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

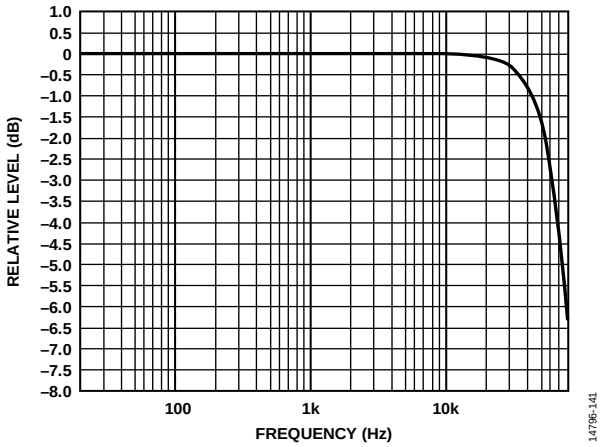



Figure 36. Relative Level vs. Frequency, $f_S$ = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

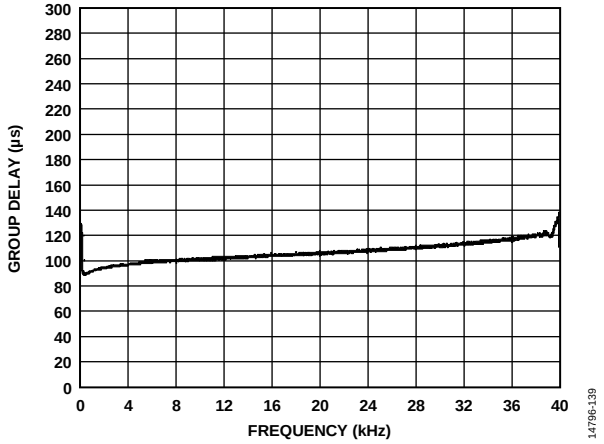



Figure 37. Group Delay vs. Frequency, $f_S$ = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

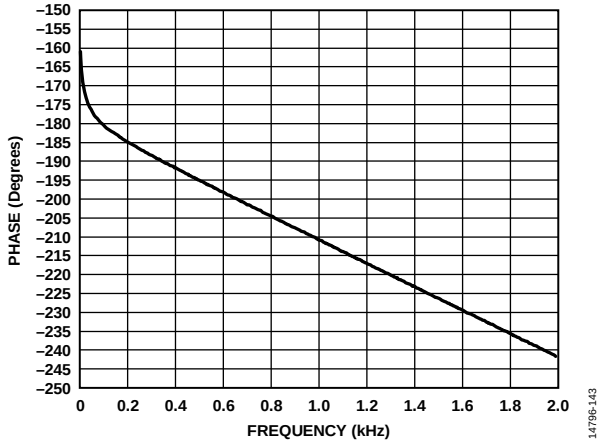



Figure 38. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

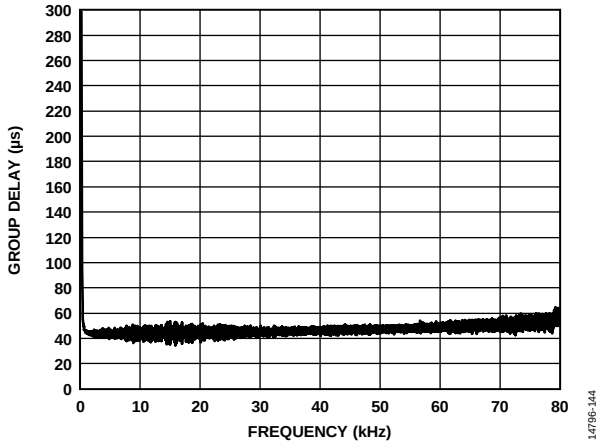



Figure 39. Group Delay vs. Frequency, $f_S$ = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

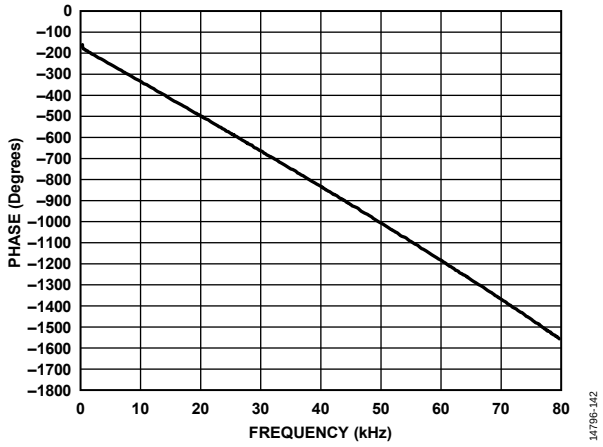



Figure 40. Phase vs. Frequency, 80 kHz Bandwidth, $f_S$ = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

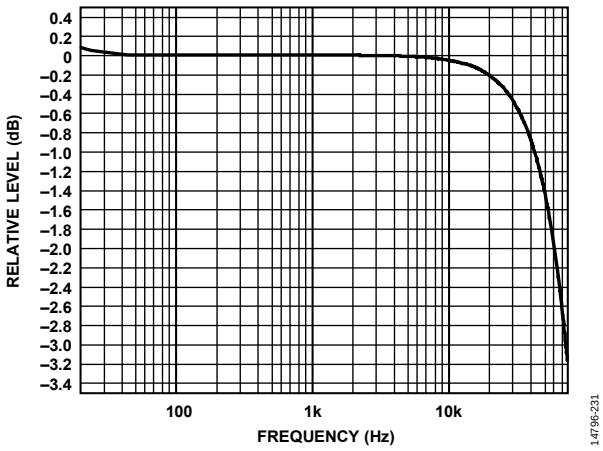



Figure 41. Relative Level vs. Frequency, $f_S$ = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx




Figure 42. Phase vs. Frequency, 20 kHz Bandwidth, $f_S$ = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

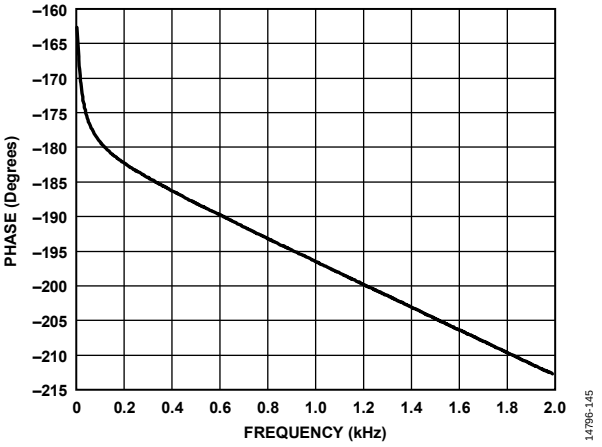



Figure 43. Phase vs. Frequency, 2 kHz Bandwidth, $f_S$ = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

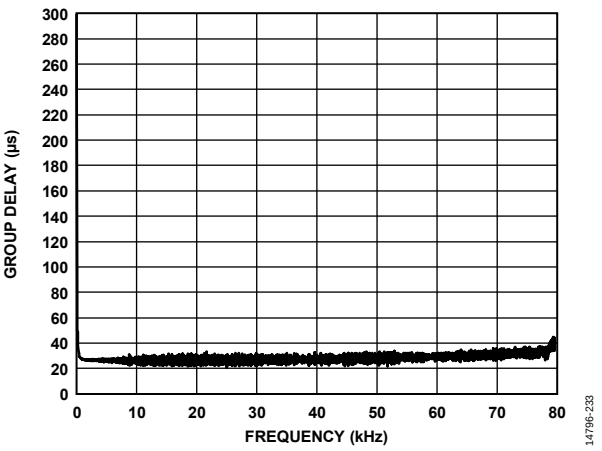



Figure 44. Group Delay vs. Frequency, $f_S$ = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

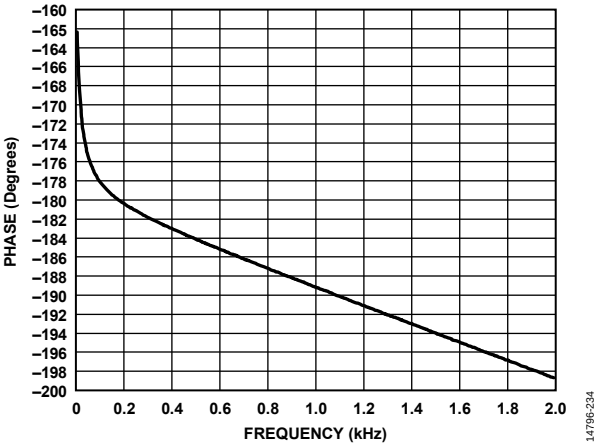



Figure 45. Phase vs. Frequency, 2 kHz Bandwidth $f_S$ = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

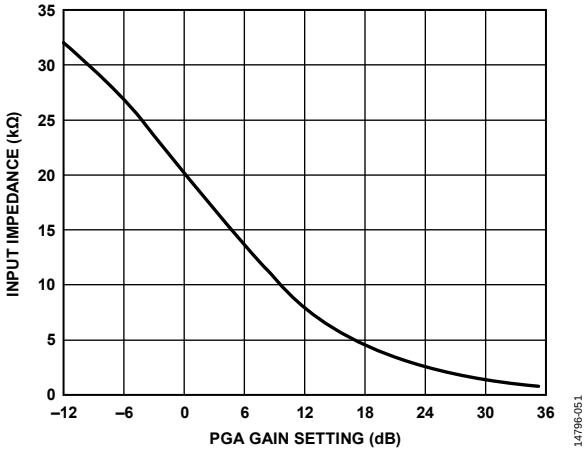



*Figure 46. Input Impedance vs. PGA Gain Setting (See the Input Impedance Section)*

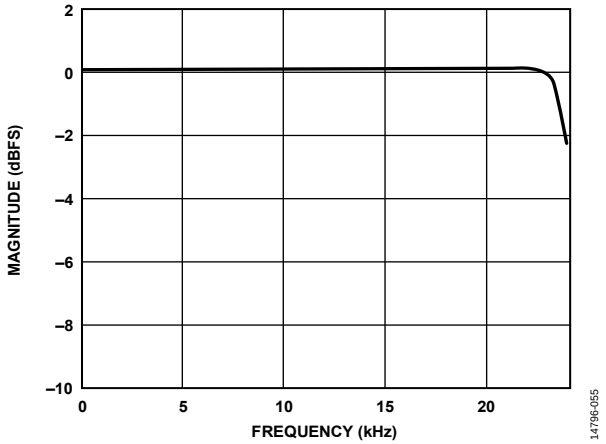



*Figure 47. Decimation Pass Band Response, $f_S$ = 768 kHz*

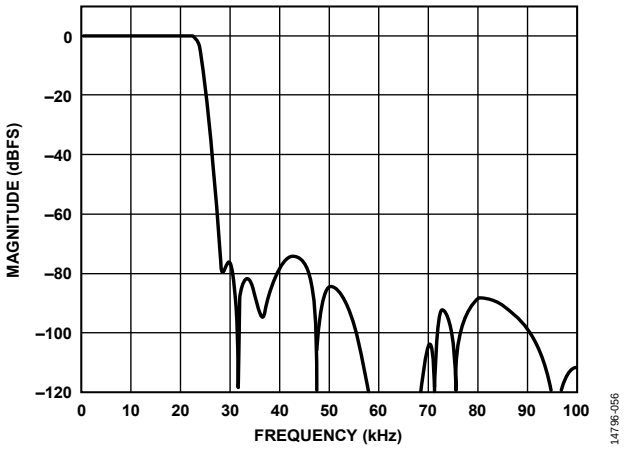



*Figure 48. Total Decimation Response, $f_S$ = 768 kHz*

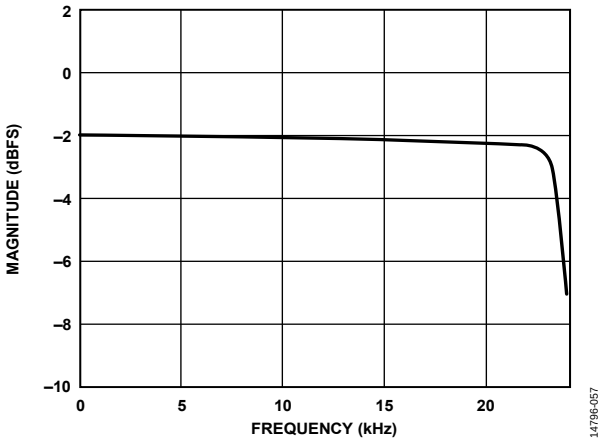



*Figure 49. Interpolation Pass Band Response, $f_S$ = 768 kHz*

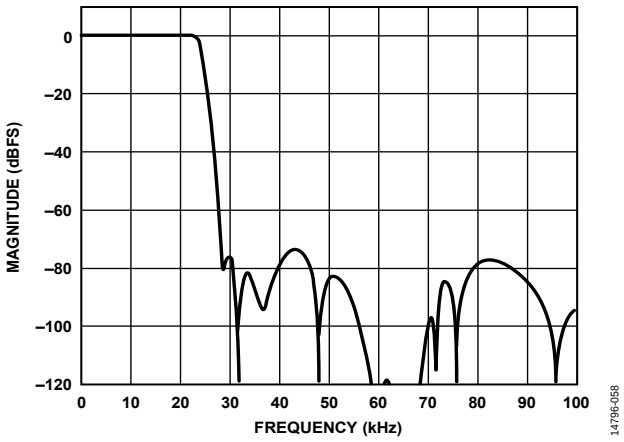



*Figure 50. Total Interpolation Response, $f_S$ = 768 kHz*

# THEORY OF OPERATION

The ADAU1777 is a low power audio codec with a streamlined audio processing core, making it ideal for noise canceling applications that require high quality audio, low power, small size, and low latency. The operating voltage range is 1.71 V to 3.63 V, with an on-board regulator optionally generating the internal digital supply voltage. By enabling low latency settings, the ADAU1777 can reach latencies as low as 5 µs.

The ADCs and DACs are high quality, 24-bit, Σ-Δ converters that operate at a selectable 768 kHz, 192 kHz, or 96 kHz sampling rate. The ADCs have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz. The ADCs and DACs also include fine step digital volume controls.

The stereo DAC output can differentially drive a headphone earpiece speaker with 16 Ω or higher impedance. One side of the differential output can be powered down if single-ended operation is required. There is also the option to change to line output mode when the output has a low load.

The input signal path is flexible and can accept single-ended analog microphone inputs, serial audio inputs, and digital microphone inputs. Two microphone bias pins provide seamless interfacing to electret microphones. Each analog input has an independent PGA that can be used for volume adjustment. The serial data port is compatible with I²S, left justified, right justified, and TDM modes, with tristating for interfacing to digital audio data streams.

The core has a reduced instruction set that is optimized for active noise cancellation. The program and parameter RAMs can be loaded with custom audio processing signal flows built using the SigmaStudio™ graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks. The ADAU1777 also has a self boot function that can load the program RAM, parameter RAM, and register settings on power-up using an external EEPROM.

The SigmaStudio software programs and controls the core through the I²C or SPI control port. Along with aiding in the design and tuning of a signal flow, SigmaStudio can configure all of the ADAU1777 registers. The SigmaStudio graphical interface allows anyone with digital or analog audio processing knowledge to easily design the DSP signal flow and port it to a target application. The interface also provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can connect graphical blocks (such as biquad filters, volume controls, and arithmetic operations), compile the design, and load the program and parameter files into the ADAU1777 memory through the control port. SigmaStudio also allows the user to download the design to an external EEPROM for self boot operation. Signal processing blocks available in the provided libraries include the following:

- Single-precision biquad filters
- Second-order filters
- Absolute value and two-input adder
- Volume controls
- Limiter

The ADAU1777 can generate its internal clocks from a wide range of input clocks by using the on-board fractional PLL. The PLL accepts inputs from 8 MHz to 27 MHz. For standalone operation, the clock can be generated using the on-board crystal oscillator.

# SYSTEM CLOCKING AND POWER-UP

## CLOCK INITIALIZATION

The ADAU1777 can generate its clocks either from an externally provided clock or from a crystal oscillator. In both cases, the on-board PLL can be used or the clock can be fed directly to the core. When a crystal oscillator is used, it is desirable to use a 12.288 MHz crystal, and the crystal oscillator function must be enabled in the COREN bit (Address 0x00, Bit 0). If the PLL is used, it must always be set to output 24.576 MHz. The PLL can be bypassed if a clock of 12.288 MHz or 24.576 MHz is available in the system. Bypassing the PLL saves system power.

The CC_MDIV and CC_CDIV bits must not be changed after setup, but the CLKSRC bit can be switched while the core is running.

Set the CC_MDIV and CC_CDIV bits so that the core and internal master clock are always 12.288 MHz; for example, when using a 24.576 MHz external source clock or if using the PLL, it is necessary to use the internal divide by 2 (see Table 11).

**Table 11. Clock Configuration Settings**

| CC_MDIV | CC_CDIV | Description |
|---|---|---|
| 1 | 1 | Divide the PLL/external clock by 1. Use these settings for a 12.288 MHz direct input clock source. |
| 0 | 0 | Divide the PLL/external clock by 2. Use these settings for a 24.576 MHz direct input clock source or if using the PLL. |

### *PLL Bypass Setup*

On power-up, the ADAU1777 exits an internal reset after 15 ms. The rate of the internal master clock must be set properly using the CC_MDIV bit in the clock control register (Address 0x00). When bypassing the PLL, the clock associated with MCLKIN must be either 12.288 MHz or 24.576 MHz. The internal master clock of the ADAU1777 is disabled until the COREN bit is asserted.

### *PLL Enabled Setup*

The core clock of the ADAU1777 is disabled by the default setting of the COREN bit and must remain disabled during the PLL lock acquisition period. The user can poll the lock bit to determine when the PLL has locked. After lock is acquired, the ADAU1777 can be started by asserting the COREN bit. This bit enables the core clock for all the internal blocks of the ADAU1777.

To program the PLL during initialization or reconfiguration of the codec, use the following procedure:

1. Ensure that PLL_EN (Bit 7, Address 0x00) is set low.
2. Set or reset the PLL control registers (Address 0x01 to Address 0x05).
3. Enable the PLL using the PLL_EN bit.
4. Poll the PLL lock bit in Register 0x06.
5. Set the COREN bit in Register 0x00 after the PLL lock is acquired.

### *Control Port Access During Initialization*

During the lock acquisition period, only Register 0x00 to Register 0x06 are accessible through the control port. A read or write to any other register is prohibited until the core clock enable bit and the lock bit are both asserted. After the CORE_RUN bit (Address 0x09) is set high, the following register bits must not be changed:

- ADC_0_1_SINC and ADC_2_3_SINC
- DAC_SOURCE0 and DAC_SOURCE1

If these bits must be changed after the ADAU1777 is running, the CORE_RUN bit first must be disabled.

## PLL

The PLL uses the MCLKIN signal as a reference to generate the core clock. The PLL settings are set in Register 0x00 to Register 0x05. Depending on the MCLK frequency, the PLL must be set for either integer or fractional mode. The PLL can accept input frequencies in the range of 8 MHz to 27 MHz.

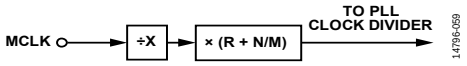



*Figure 51. PLL Block Diagram*

### *Input Clock Divider*

Before reaching the PLL, the input clock signal goes through an integer clock divider to ensure that the clock frequency is within a suitable range for the PLL. The X bits in the PLL_CTRL4 register (Address 0x05, Bits[2:1]) set the PLL input clock divide ratio.

### *Integer Mode*

Use integer mode when the clock input is an integer multiple of the PLL output.

For example, if MCLKIN = 12.288 MHz, (X + 1) = 1, and $f_S$ = 48 kHz,

*PLL Required Output* = 24.576 MHz

*R*/2 = 24.576 MHz/12.288 MHz = 2

where *R*/2 = 2 or *R* = 4.

In integer mode, the values set for N and M are ignored. Table 12 lists common integer PLL parameter settings for 48 kHz sampling rates.

### *Fractional Mode*

Use fractional mode when the clock input is a fractional multiple of the PLL output.

For example, if MCLKIN = 13 MHz, (X + 1) = 1, and $f_S$ = 48 kHz,

*PLL Required Output* = 24.576 MHz

(1/2) × (*R* + (*N*/*M*)) = 24.576 MHz/13 MHz = (1/2) × (3 + (1269/1625))

where:
*R* = 3.
*N* = 1269.
*M* = 1625.

Table 13 lists common fractional PLL parameter settings for 48 kHz sampling rates. When the PLL is used in fractional mode, the N/M fraction must be kept in the range of 0.1 to 0.9 to ensure correct operation of the PLL.

The PLL output clock must be kept in the range of 20.5 MHz to 27 MHz, which must be taken into account when calculating PLL values and MCLK frequencies.

## CLOCK OUTPUT

Use the CLKOUT pin as a master clock output to clock other ICs in the system or as the clock for the digital microphone inputs and PDM output. This clock can be generated from the 12.288 MHz master clock of the ADAU1777 by factors of 2, 1, ½, ¼, and ⅛. If PDM mode is enabled, only the ½, ¼, and ⅛ settings produce a clock signal on CLKOUT. The factor of 2 multiplier works properly only if the input clock was previously divided by 2 using the CC_MDIV bit.

## POWER SEQUENCING

AVDD and IOVDD can each be set to any voltage between 1.8 V and 3.3 V, and DVDD can be set between 1.1 V and 1.8 V or between 1.1 V and 1.2 V if using the on-board regulator.

On power-up, AVDD must be powered up before or at the same time as IOVDD. Do not power up IOVDD when power is not applied to AVDD.

Enabling the $\overline{\text{PD}}$ pin powers down all analog and digital circuits. Before enabling $\overline{\text{PD}}$ (that is, setting it low), be sure to mute the outputs to avoid any pops when the IC is powered down. Tie $\overline{\text{PD}}$ directly to IOVDD for normal operation.

### *Power-Down Considerations*

When powering down the ADAU1777, mute the outputs before AVDD power is removed; otherwise, pops or clicks may be heard. The easiest way to achieve this is to use a regulator that has a power-good (PGOOD) signal to power the ADAU1777 or to generate a power-good signal using additional circuitry external to the regulator itself. Typically, on such regulators, the power-good signal changes state when the regulated voltage drops below ~90% of its target value. Connect this power-good signal to one of the ADAU1777 multipurpose pins and mute the DAC outputs by setting the multipurpose pin functionality to mute both DACs in Register 0x38 to Register 0x3E. Taking these precautions ensures that the outputs are muted before power is completely removed.

**Table 12. Integer PLL Parameter Settings for PLL Output = 24.576 MHz**

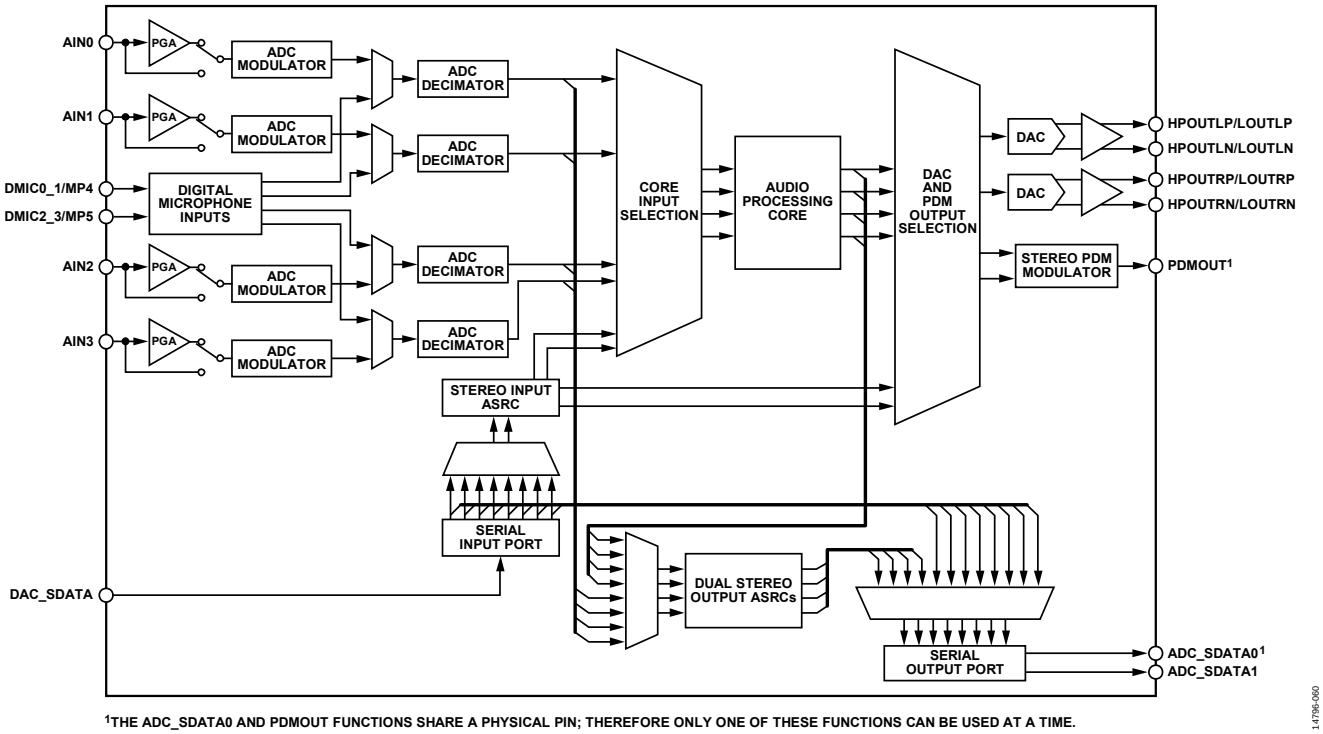
| MCLK Input (MHz) | Input Divider (X + 1) | Integer (R) | Denominator (M) | Numerator (N) | PLL_CTRL4 Settings (Address 0x05) |
|---|---|---|---|---|---|
| 12.288 | 1 | 4 | Don't care | Don't care | 0x20 |
| 24.576 | 1 | 2 | Don't care | Don't care | 0x10 |

**Table 13. Fractional PLL Parameter Settings for PLL Output = 24.576 MHz**

| MCLK Input (MHz) | Input Divider (X + 1) | Integer (R) | Denominator (M) | Numerator (N) | PLL Parameter Register Settings (Address 0x05 to Address 0x01) | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | PLL_CTRL4 (Addr. 0x05) | PLL_CTRL3 (Addr. 0x04) | PLL_CTRL2 (Addr. 0x03) | PLL_CTRL1 (Addr. 0x02) | PLL_CTRL0 (Addr. 0x01) |
| 8 | 1 | 6 | 125 | 18 | 0x31 | 0x12 | 0x00 | 0x7D | 0x00 |
| 13 | 1 | 3 | 1625 | 1269 | 0x19 | 0xF5 | 0x04 | 0x59 | 0x06 |
| 14.4 | 2 | 6 | 75 | 62 | 0x33 | 0x3E | 0x00 | 0x4B | 0x00 |
| 19.2 | 2 | 5 | 25 | 3 | 0x2B | 0x03 | 0x00 | 0x19 | 0x00 |
| 26 | 2 | 3 | 1625 | 1269 | 0x1B | 0xF5 | 0x04 | 0x59 | 0x06 |
| 27 | 2 | 3 | 1125 | 721 | 0x1B | 0xD1 | 0x02 | 0x65 | 0x04 |

# SIGNAL ROUTING

The ADAU1777 features flexible signal routing. The signal routing is specified by Register 0x0F through Register 0x1A.




1THE ADC_SDATA0 AND PDMOUT FUNCTIONS SHARE A PHYSICAL PIN; THEREFORE ONLY ONE OF THESE FUNCTIONS CAN BE USED AT A TIME.

*Figure 52. Input and Output Signal Routing*

# INPUT SIGNAL PATHS

Four input paths, from either an ADC or a digital microphone, can be routed to the core. The input sources (ADC or digital microphone) must be configured in pairs (for example, 0 and 1, or 2 and 3), but each channel can be routed individually. The core inputs can also be sourced from a stereo input ASRC.

## ANALOG INPUTS

The ADAU1777 can accept both line level and microphone inputs. Each of the four analog input channels can be configured in single-ended mode or a single-ended with PGA mode. There are also inputs for up to four digital microphones. The analog inputs are biased at AVDD/2 V. Connect unused input pins to the CM pin or ac-couple them to ground.

### *Signal Polarity*

Signals routed through the PGAs are inverted. As a result, signals input through the PGA are output from the ADCs with a polarity that is opposite that of the input. Single-ended inputs are not inverted. The ADCs are noninverting.

### *Input Impedance*

The input impedance of the analog inputs varies with the gain of the PGA. This impedance ranges from 0.68 kΩ at the +35.25 dB gain setting to 32.0 kΩ at the −12 dB setting. The resistors inside the ADAU1777 are precisely matched to each other, resulting in very little gain error. However, the exact value of the resistors depends on various conditions in the silicon manufacturing process and can vary by as much as ±20%. The input impedance ($R_{IN}$) on each pin can be calculated as follows:

$$R_{IN} = \frac{40}{10^{(Gain/20)} + 1} \text{k}\Omega$$

where *Gain* is set by PGA_GAINx.

The optional 10 dB PGA boost, set in the PGA_x_BOOST bits, does not affect the input impedance. This setting is an alternative way of increasing gain without decreasing input impedance; however, it causes some degradation in performance.

### *Analog Microphone Inputs*

For microphone signals, the ADAU1777 analog inputs can be configured as single-ended with PGA mode.

The PGA settings are controlled in Register 0x23 to Register 0x26. The PGA is enabled by setting the PGA_ENx bits.

Connect the microphone signal to the inverting inputs of the PGAs (AINx), as shown in Figure 53.

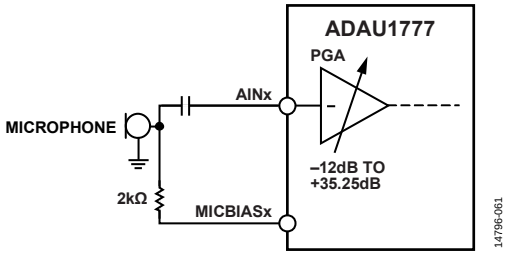



*Figure 53. Single-Ended Microphone Configuration*

### *Analog Line Inputs*

Line level signals can be input on the AINx pins of the analog inputs. Figure 54 shows a single-ended line input using the AINx pins.

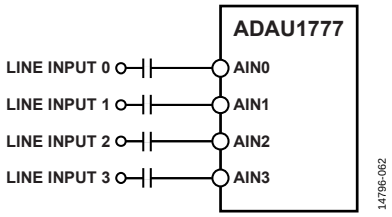



*Figure 54. Single-Ended Line Inputs*

### *Precharging Input Capacitors*

Precharge amplifiers are enabled by default to charge large series capacitors quickly on the inputs and outputs. Precharging these capacitors prevents pops in the audio signal. The precharge circuits are powered up by default on startup and can be disabled in the POP_SUPPRESS register. The precharge amplifiers are automatically disabled when the PGA or headphone amplifiers are enabled. For unused PGAs and headphone outputs, disable these precharge amplifiers using the POP_SUPPRESS register. The precharging time is dependent on the input/output series capacitors. The impedance looking into the AINx pin is 500 Ω in this mode. However, at startup, the impedance looking into the pin is dominated by the time constant of the CM pin because the precharge amplifiers reference the CM voltage.

### *Microphone Bias*

The ADAU1777 includes two microphone bias outputs: MICBIAS0 and MICBIAS1. These pins provide a voltage reference for electret analog microphones. The MICBIASx pins also cleanly supply voltage to digital or analog microelectromechanical systems (MEMS) microphones with separate power supply pins. The MICBIASx voltage is set in the microphone bias control register (Address 0x2D). Using this register, the MICBIAS0 or MICBIAS1 output can be enabled or disabled. The gain options provide two possible voltages: 0.65 × AVDD or 0.90 × AVDD.

Many applications require enabling only one of the two bias outputs. The two bias outputs must both be enabled when many microphones are used in the system or when the positioning of the microphones on the PCB does not allow one pin to bias all microphones.

## DIGITAL MICROPHONE INPUT

When using a digital microphone connected to the DMIC0_1/MP4 and DMIC2_3/MP5 pins, the DCM_0_1 and DCM_2_3 bits in Register 0x1D and Register 0x1E must be set to enable the digital microphone signal paths. Set the pin functions to digital microphone input in the corresponding pin mode registers (Address 0x3C and Address 0x3D). The DMIC0/DMIC2 and DMIC1/DMIC3 channels can be swapped (left/right swap) by writing to the DMIC_SW0 and DMIC_SW1 bits in the ADC_CONTROL2 and ADC_CONTROL3 registers (Address 0x1D and Address 0x1E, respectively). In addition, the microphone polarity can be reversed by setting the DMIC_POLx bits, which reverses the phase of the incoming audio by 180°.

The digital microphone inputs are clocked from the CLKOUT pin. The digital microphone data stream must be clocked by this pin and not by a clock from another source, such as another audio IC, even if the other clock is of the same frequency as CLKOUT.

The digital microphone signal bypasses the analog input path and the ADCs and is routed directly into the decimation filters. The digital microphone and the ADCs share digital filters and, therefore, both cannot be used simultaneously. The digital microphone inputs are enabled in pairs. The ADAU1777 inputs can be set for either four analog inputs, four digital microphone inputs, or two analog inputs and two digital microphone inputs. Figure 55 shows the digital microphone interface and signal routing.

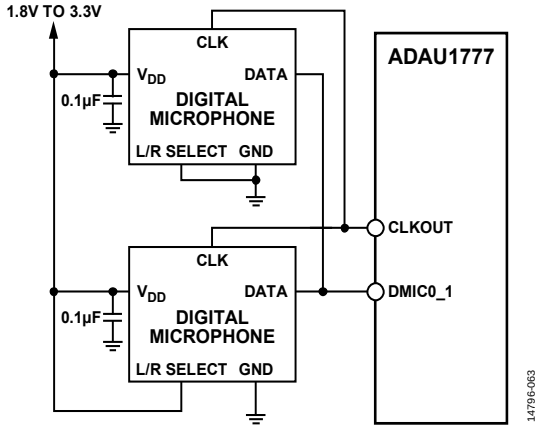



*Figure 55. Digital Microphone Interface Block Diagram*

Figure 55 shows two digital microphones connected to the DMIC0_1/MP4 pin. These microphones can also be connected to DMIC2_3/MP5 if that signal path is to be used for digital microphones. If more than two digital microphones are to be used in a system, then up to two microphones are connected to both DMIC0_1/MP4 and DMIC2_3/MP5 and the CLKOUT signal is fanned out to the clock input of all of the microphones.

## ANALOG-TO-DIGITAL CONVERTERS (ADCs)

The ADAU1777 includes four 24-bit, Σ-Δ ADCs, each with a selectable sample rate of 768 kHz, 192 kHz, or 96 kHz.

### *ADC Full-Scale Level*

The full-scale input to the ADCs (0 dBFS) scales linearly with AVDD. At AVDD = 3.3 V, the full-scale input level is 1 V rms. Signal levels greater than the full-scale value cause the ADCs to clip.

### *Digital ADC Volume Control*

The volume setting of each ADC can be digitally attenuated in the ADCx_VOLUME registers (Address 0x1F to Address 0x22). The volume can be set between 0 dB and −95.625 dB in 0.375 dB steps. The ADC volume can also be digitally muted in the ADC_CONTROLx registers (Address 0x1B to Address 0x1E).

### *High-Pass Filter*

A high-pass filter is available on the ADC path to remove dc offsets; this filter can be enabled or disabled using the HP_x_y_EN bits. At $f_S$ = 192 kHz, the corner frequency of this high-pass filter can be set to 1 Hz, 4 Hz, or 8 Hz.

# OUTPUT SIGNAL PATHS

Data from the serial input port can be routed to the core, to the output selection multiplexer, or directly to the serial output ports. Data from the core can be routed to the serial output port, the stereo DAC, and the stereo PDM modulator (see Figure 52).

The analog outputs of the ADAU1777 can be configured as differential or single-ended outputs. The analog output pins can drive headphone or earpiece speakers. The line outputs can drive a load of at least 10 kΩ or can be set into headphone mode to drive headphones or earpiece speakers. The analog output pins are biased at AVDD/2.

## ANALOG OUTPUTS

### Headphone Output

The output pins can be driven by either a line output driver or a headphone driver by setting the HP_EN_L and HP_EN_R bits in the headphone line output select register (Address 0x43). The headphone outputs can drive a load of at least 16 Ω.

### Headphone Output Power-Up Sequencing

To prevent pops when turning on the headphone outputs, wait at least 6 ms to unmute these outputs after enabling the headphone output using the HP_EN_x bits. Waiting 6 ms allows an internal capacitor to charge before these outputs are used. Figure 56 illustrates the headphone output power-up sequencing.

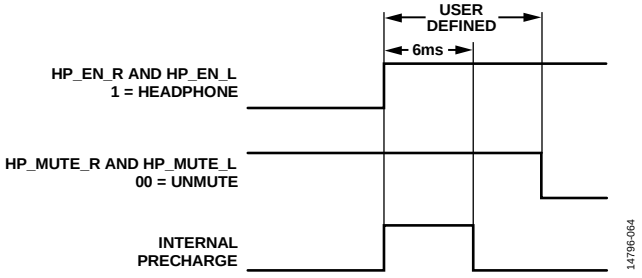



*Figure 56. Headphone Output Power-Up Sequencing*

### Ground Centered Headphone Configuration

The headphone outputs can also be configured as ground centered outputs by connecting coupling capacitors in series with the output pins. Ground centered headphones must use the AGND pin as the ground reference.

When the headphone outputs are configured as ground centered, the capacitors create a high-pass filter on the outputs. The corner frequency of this filter ($f_{3\,dB}$), which has an attenuation of 3 dB, is calculated by the following formula:

$$f_{3\,dB} = 1/(2\pi \times R \times C)$$

where :
*R* is the impedance of the headphones.
*C* is the capacitor value.

For a typical headphone impedance of 32 Ω with a 220 µF capacitor, the corner frequency is 23 Hz.

### Pop and Click Suppression

On power-up, the precharge circuitry is enabled on all four analog output pins to suppress pops and clicks. After power-up, the precharge circuitry can be set to a low power mode using the HP_POP_DISx bits in the POP_SUPRRESS register (Address 0x29).

The precharge time depends on the value of the capacitor connected to the CM pin and the RC time constant of the load on the output pin. For a typical line output load, the precharge time is between 2 ms and 3 ms. After this precharge time, the HP_POP_DISx bits can be set to low power mode.

To avoid clicks and pops, mute all analog outputs that are in use while changing any register settings that may affect the signal path. These outputs can then be unmuted after the changes are made.

### Line Outputs

The analog output pins (HPOUTLP/LOUTLP, HPOUTLN/LOUTLN, HPOUTRP/LOUTRP, and HPOUTRN/LOUTRN) can be used to drive both differential and single-ended loads. In their default settings, these pins can drive typical line loads of 10 kΩ or greater.

When the line output pins are used in single-ended mode, use the HPOUTLP/LOUTLP and HPOUTRP/LOUTRP pins to output the signals, and power down the HPOUTLN/LOUTLN and HPOUTRN/LOUTRN pins.

## DIGITAL-TO-ANALOG CONVERTERS (DACs)

The ADAU1777 includes two 24-bit, Σ-Δ DACs.

### DAC Full-Scale Level

The full-scale output from the DACs (0 dBFS) scales linearly with AVDD. At AVDD = 3.3 V, the full-scale output level is 1.94 V rms for a differential output or 0.97 V rms for a single-ended output.

### Digital DAC Volume Control

The volume of each DAC can be digitally attenuated using the DACx_VOLUME registers (Address 0x2F and Address 0x30). The volume can be set to be between 0 dB and −95.625 dB in 0.375 dB steps.

## PDM OUTPUT

The ADAU1777 includes a 2-channel PDM modulator. The PDMOUT pin can be used to drive a PDM input amplifier, such as the SSM2517 mono 2.4 W amplifier. Two SSM2517 devices can be connected to the PDMOUT data stream to enable a stereo output. The PDM output signal is clocked by the CLKOUT pin output. The PDM output stream must be clocked by this pin and not by a clock from another source, such as another audio IC, even if the other clock is of the same frequency as CLKOUT. The PDM output data is clipped at the −6 dB level to prevent overdriving a connected amplifier like the SSM2517.

The ADAU1777 has the ability to output PDM control patterns to configure devices such as the SSM2517. Each pattern is a byte long and is written with a user defined pattern in the PDM_PATTERN register (Address 0x37). The control pattern is enabled and the output channel selection is configured in the PDM_OUT register (Address 0x36). The PDM pattern must not be changed while the ADAU1777 is outputting the control pattern to the external device. After the external device is configured, the control pattern can be disabled. For the SSM2517, the control pattern must be repeated a minimum of 128 times to configure the device. Table 14 describes typical control patterns for the SSM2517.

**Table 14. SSM2517 PDM Control Pattern Descriptions**

| Pattern | Control Description |
|---|---|
| 0xAC | Power-down. All blocks off except for the PDM interface. Normal start-up time. |
| 0xD8 | Gain optimized for PVDD = 5 V operation. Overrides GAIN_FS pin setting. |
| 0xD4 | Gain optimized for PVDD = 3.6 V operation. Overrides GAIN_FS pin setting. |
| 0xD2 | Gain optimized for PVDD = 2.5 V operation. Overrides GAIN_FS pin setting. |
| 0xD1 | $f_S$ set to opposite value determined by GAIN_FS pin. |
| 0xE1 | Ultralow electromagnetic interference (EMI) mode. |
| 0xE2 | Half clock cycle pulse mode for power savings. |
| 0xE4 | Special 32 kHz,128 × $f_S$ operation mode. |

## ASYNCHRONOUS SAMPLE RATE CONVERTERS

The ADAU1777 includes ASRCs to enable synchronous, full duplex operation of the serial ports. Two stereo ASRCs are available for the digital outputs, and one stereo ASRC is available for the digital input signals.

The ASRCs can convert serial output data from the core rates to the serial port rates of 192 kHz down to less than 8 kHz. All intermediate frequencies and ratios are also supported.

## SIGNAL LEVELS

The ADCs, DACs, and ASRCs have fixed gain settings that must be considered when configuring the system. These settings are chosen to maximize performance of the converters and to ensure that there is 0 dB gain for any signal path from the input of the ADAU1777 to its output. Therefore, the full-scale level of a signal in the processing core is slightly different from a full-scale level external to the IC.

Input paths, such as through the ADCs and input ASRCs, are scaled by 0.75, or about −2.5 dB. Output paths, such as through the DACs or output ASRCs, are scaled by 1.33, or about 2.5 dB. This scaling is shown in Figure 57.

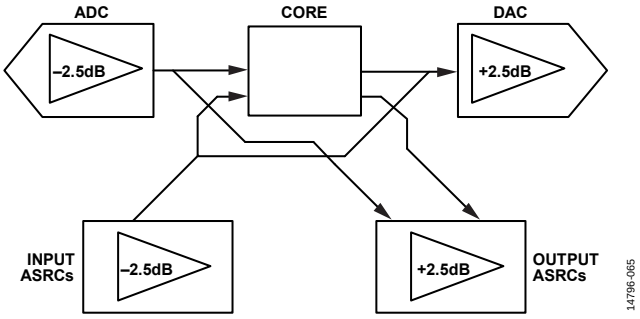



*Figure 57. Signal Level Diagram*

Because of this input and output scaling, output signals from the core must be limited to −2.5 dB full scale to prevent the DACs and ASRCs from clipping.

# SIGNAL PROCESSING

The ADAU1777 processing core is optimized for ANC processing. The processing capabilities of the core include biquad filters, limiters, volume controls, and mixing. The core has four inputs and four outputs. The core is controlled with a 10-bit program word, with a maximum of 32 instructions per frame.

## INSTRUCTIONS

A complete list of instructions/processing blocks along with documentation can be found in the SigmaStudio software for the ADAU1777. The processing blocks available are

- Single precision biquad/second-order filters
- Absolute value
- Two-input addition
- T connection in SigmaStudio
- Limiter with/without external detector loop
- Linear gain
- Volume slider
- Mute
- DBREG level detection

## DATA MEMORY

The ADAU1777 data path is 26 bits (5.21 format). The data memory is 32 words of 2 × 26 bits. The double length memory enables the core to double precision arithmetic with double length data and single length coefficients.

## PARAMETERS

Parameters, such as filter coefficients, limiter settings, and volume control settings, are saved in parameter registers. Each parameter is a 32-bit number. The format of this number depends on whether it is controlling a filter or a limiter. The number formats of different parameters are shown in Table 15. When the parameter formats use less than the full 32-bit memory space, as with the limiter parameters, the data is LSB aligned.

**Table 15. Parameter Number Formats**

| Parameter Type | Format |
|---|---|
| Filter Coefficient (B0, B1, B2) | 5.27 |
| Filter Coefficient (A1) | 2.27 (sign extended) |
| Filter Coefficient (A2) | 1.27 (sign extended) |
| Maximum Gain | 2.23 |
| Minimum Gain | 2.23 |
| Attack Time | 24.0 |
| Decay Time | 24.0 |
| Threshold | 2.23 |

Two parameter banks are available. Each bank can hold a full set of 160 parameters (32 filters × 5 coefficients). Users can switch between Bank A and Bank B, allowing two sets of parameters to be saved in memory and switched on-the-fly while the codec is running. Bank switching can be achieved by writing to the CORE_CONTROL register (Address 0x09) or by using the multipurpose push-button switches, but not by using a combination of the two. Parameters in the active bank must not be updated while the core is running; doing so may result in noises on the outputs.

Parameters are assigned to instructions in the order in which the instructions are instantiated in the code. The instruction types that use parameters are the biquad filters and limiters.

Table 17 shows the addresses of each parameter in Bank A that are associated with each of the 32 instructions, and Table 18 shows the addresses of each parameter in Bank B. Table 16 shows the addresses of the LSB aligned, 10-bit program words.

**Table 16. Program Addresses**

| Instruction | Instruction Address |
|---|---|
| 0 | 0x0080 |
| 1 | 0x0081 |
| 2 | 0x0082 |
| 3 | 0x0083 |
| 4 | 0x0084 |
| 5 | 0x0085 |
| 6 | 0x0086 |
| 7 | 0x0087 |
| 8 | 0x0088 |
| 9 | 0x0089 |
| 10 | 0x008A |
| 11 | 0x008B |
| 12 | 0x008C |
| 13 | 0x008D |
| 14 | 0x008E |
| 15 | 0x008F |
| 16 | 0x0090 |
| 17 | 0x0091 |
| 18 | 0x0092 |
| 19 | 0x0093 |
| 20 | 0x0094 |
| 21 | 0x0095 |
| 22 | 0x0096 |
| 23 | 0x0097 |
| 24 | 0x0098 |
| 25 | 0x0099 |
| 26 | 0x009A |
| 27 | 0x009B |
| 28 | 0x009C |
| 29 | 0x009D |
| 30 | 0x009E |
| 31 | 0x009F |

**Table 17. Parameter Addresses, Bank A**

| Assignment Order | B0/Maximum Gain | B1/Minimum Gain | B2/Attack | A1/Decay | A2/Threshold |
|---|---|---|---|---|---|
| 0 | 0x00E0 | 0x0100 | 0x0120 | 0x0140 | 0x0160 |
| 1 | 0x00E1 | 0x0101 | 0x0121 | 0x0141 | 0x0161 |
| 2 | 0x00E2 | 0x0102 | 0x0122 | 0x0142 | 0x0162 |
| 3 | 0x00E3 | 0x0103 | 0x0123 | 0x0143 | 0x0163 |
| 4 | 0x00E4 | 0x0104 | 0x0124 | 0x0144 | 0x0164 |
| 5 | 0x00E5 | 0x0105 | 0x0125 | 0x0145 | 0x0165 |
| 6 | 0x00E6 | 0x0106 | 0x0126 | 0x0146 | 0x0166 |
| 7 | 0x00E7 | 0x0107 | 0x0127 | 0x0147 | 0x0167 |
| 8 | 0x00E8 | 0x0108 | 0x0128 | 0x0148 | 0x0168 |
| 9 | 0x00E9 | 0x0109 | 0x0129 | 0x0149 | 0x0169 |
| 10 | 0x00EA | 0x010A | 0x012A | 0x014A | 0x016A |
| 11 | 0x00EB | 0x010B | 0x012B | 0x014B | 0x016B |
| 12 | 0x00EC | 0x010C | 0x012C | 0x014C | 0x016C |
| 13 | 0x00ED | 0x010D | 0x012D | 0x014D | 0x016D |
| 14 | 0x00EE | 0x010E | 0x012E | 0x014E | 0x016E |
| 15 | 0x00EF | 0x010F | 0x012F | 0x014F | 0x016F |
| 16 | 0x00F0 | 0x0110 | 0x0130 | 0x0150 | 0x0170 |
| 17 | 0x00F1 | 0x0111 | 0x0131 | 0x0151 | 0x0171 |
| 18 | 0x00F2 | 0x0112 | 0x0132 | 0x0152 | 0x0172 |
| 19 | 0x00F3 | 0x0113 | 0x0133 | 0x0153 | 0x0173 |
| 20 | 0x00F4 | 0x0114 | 0x0134 | 0x0154 | 0x0174 |
| 21 | 0x00F5 | 0x0115 | 0x0135 | 0x0155 | 0x0175 |
| 22 | 0x00F6 | 0x0116 | 0x0136 | 0x0156 | 0x0176 |
| 23 | 0x00F7 | 0x0117 | 0x0137 | 0x0157 | 0x0177 |
| 24 | 0x00F8 | 0x0118 | 0x0138 | 0x0158 | 0x0178 |
| 25 | 0x00F9 | 0x0119 | 0x0139 | 0x0159 | 0x0179 |
| 26 | 0x00FA | 0x011A | 0x013A | 0x015A | 0x017A |
| 27 | 0x00FB | 0x011B | 0x013B | 0x015B | 0x017B |
| 28 | 0x00FC | 0x011C | 0x013C | 0x015C | 0x017C |
| 29 | 0x00FD | 0x011D | 0x013D | 0x015D | 0x017D |
| 30 | 0x00FE | 0x011E | 0x013E | 0x015E | 0x017E |
| 31 | 0x00FF | 0x011F | 0x013F | 0x015F | 0x017F |

**Table 18. Parameter Addresses, Bank B**

| Assignment Order | B0/Maximum Gain | B1/Minimum Gain | B2/Attack | A1/Decay | A2/Threshold |
|---|---|---|---|---|---|
| 0 | 0x0180 | 0x01A0 | 0x01C0 | 0x01E0 | 0x0200 |
| 1 | 0x0181 | 0x01A1 | 0x01C1 | 0x01E1 | 0x0201 |
| 2 | 0x0182 | 0x01A2 | 0x01C2 | 0x01E2 | 0x0202 |
| 3 | 0x0183 | 0x01A3 | 0x01C3 | 0x01E3 | 0x0203 |
| 4 | 0x0184 | 0x01A4 | 0x01C4 | 0x01E4 | 0x0204 |
| 5 | 0x0185 | 0x01A5 | 0x01C5 | 0x01E5 | 0x0205 |
| 6 | 0x0186 | 0x01A6 | 0x01C6 | 0x01E6 | 0x0206 |
| 7 | 0x0187 | 0x01A7 | 0x01C7 | 0x01E7 | 0x0207 |
| 8 | 0x0188 | 0x01A8 | 0x01C8 | 0x01E8 | 0x0208 |
| 9 | 0x0189 | 0x01A9 | 0x01C9 | 0x01E9 | 0x0209 |
| 10 | 0x018A | 0x01AA | 0x01CA | 0x01EA | 0x020A |
| 11 | 0x018B | 0x01AB | 0x01CB | 0x01EB | 0x020B |
| 12 | 0x018C | 0x01AC | 0x01CC | 0x01EC | 0x020C |
| 13 | 0x018D | 0x01AD | 0x01CD | 0x01ED | 0x020D |
| 14 | 0x018E | 0x01AE | 0x01CE | 0x01EE | 0x020E |
| 15 | 0x018F | 0x01AF | 0x01CF | 0x01EF | 0x020F |

| Assignment Order | B0/Maximum Gain | B1/Minimum Gain | B2/Attack | A1/Decay | A2/Threshold |
|---|---|---|---|---|---|
| 16 | 0x0190 | 0x01B0 | 0x01D0 | 0x01F0 | 0x0210 |
| 17 | 0x0191 | 0x01B1 | 0x01D1 | 0x01F1 | 0x0211 |
| 18 | 0x0192 | 0x01B2 | 0x01D2 | 0x01F2 | 0x0212 |
| 19 | 0x0193 | 0x01B3 | 0x01D3 | 0x01F3 | 0x0213 |
| 20 | 0x0194 | 0x01B4 | 0x01D4 | 0x01F4 | 0x0214 |
| 21 | 0x0195 | 0x01B5 | 0x01D5 | 0x01F5 | 0x0215 |
| 22 | 0x0196 | 0x01B6 | 0x01D6 | 0x01F6 | 0x0216 |
| 23 | 0x0197 | 0x01B7 | 0x01D7 | 0x01F7 | 0x0217 |
| 24 | 0x0198 | 0x01B8 | 0x01D8 | 0x01F8 | 0x0218 |
| 25 | 0x0199 | 0x01B9 | 0x01D9 | 0x01F9 | 0x0219 |
| 26 | 0x019A | 0x01BA | 0x01DA | 0x01FA | 0x021A |
| 27 | 0x019B | 0x01BB | 0x01DB | 0x01FB | 0x021B |
| 28 | 0x019C | 0x01BC | 0x01DC | 0x01FC | 0x021C |
| 29 | 0x019D | 0x01BD | 0x01DD | 0x01FD | 0x021D |
| 30 | 0x019E | 0x01BE | 0x01DE | 0x01FE | 0x021E |
| 31 | 0x019F | 0x01BF | 0x01DF | 0x01FF | 0x021F |

# CONTROL PORT

The ADAU1777 has both a 4-wire SPI control port and a 2-wire I²C bus control port. Each port can be used to set the memories and registers. The IC defaults to I²C mode but can be put into SPI control mode by pulling the $\overline{SS}$ pin low three times.

The control port is capable of full read/write operation for all addressable memories and registers. Most signal processing parameters are controlled by writing new values to the parameter memories using the control port. Other functions, such as mute and input/output mode control, are programmed through the registers.

All addresses can be accessed in either single address mode or burst mode. The first byte (Byte 0) of a control port write contains the 7-bit IC address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) are the 16-bit subaddress of the memory or register location within the ADAU1777. All subsequent bytes (starting with Byte 3) contain the data, such as register data, program data, or parameter data. The number of bytes per word depends on the type of data that is being written. Table 19 shows the word length of the different data types of the ADAU1777. The exact formats for specific types of writes are shown in Figure 60 and Figure 61.

**Table 19. Data-Word Sizes**

| Data Type | Word Size (Bytes) |
|---|---|
| Registers | 1 |
| Program | 2 |
| Parameters | 4 |

If large blocks of data must be downloaded to the ADAU1777, halt the output of the core (using the CORE_RUN bit in the core control register (Address 0x09)), load new data, and then restart the core. Halting the core is typically done during the booting sequence at startup or when loading a new program into memory.

Registers and bits shown as reserved in the register map read back 0s. When writing to these registers and bits, such as during a burst write across a reserved register, or when writing to reserved bits in a register with other used bits, write 0s.

The control port pins are multifunctional, depending on the mode in which the device is operating. Table 20 details these multiple functions.

**Table 20. Control Port Pin Functions**

| Pin | I²C Mode | SPI Mode |
|---|---|---|
| SCL/SCLK | SCL, input | SCLK, input |
| SDA/MISO | SDA, open-collector output | MISO, output |
| ADDR1/MOSI | I²C Address Bit 1, input | MOSI, input |
| ADDR0/$\overline{SS}$ | I²C Address Bit 0, input | $\overline{SS}$, input |

## BURST MODE COMMUNICATION

Use burst mode addressing, in which the subaddresses are automatically incremented at word boundaries, for writing large amounts of data to contiguous memory locations. This increment occurs automatically after a single-word write unless the control port communication is stopped; that is, a stop condition is issued for I²C mode, or $\overline{SS}$ is brought high for SPI mode. The registers and RAMs in the ADAU1777 range in width from one to four bytes; therefore, the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location).

## I²C PORT

The ADAU1777 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. I²C mode uses two pins—serial data (SDA) and serial clock (SCL)—to carry data between the ADAU1777 and the system I²C master controller. In I²C mode, the ADAU1777 is always a slave on the bus, except when the IC is self booting. See the Self Boot section for details about using the ADAU1777 in self boot mode.

Each slave device is recognized by a unique 7-bit address. The ADAU1777 I²C address format is shown in Table 21. The LSB of this first byte sent from the I²C master sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

The ADDR0 and ADDR1 pins set the LSBs of the I²C address (see Table 22); therefore, each ADAU1777 can be set to one of four unique addresses. This feature allows multiple ICs to exist on the same I²C bus without address contention. The 7-bit I²C addresses are shown in Table 22.

An I²C data transfer is always terminated by a stop condition.

Both SDA and SCL must have 2.0 kΩ pull-up resistors on the lines connected to them. The voltage on these signal lines must not be higher than IOVDD.

**Table 21. I²C Address Format**

| Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | ADDR1 | ADDR0 |

**Table 22. I²C Addresses**

| ADDR1 | ADDR0 | Slave Address |
|---|---|---|
| 0 | 0 | 0x3C |
| 0 | 1 | 0x3D |
| 1 | 0 | 0x3E |
| 1 | 1 | 0x3F |

### Addressing

Initially, each device on the I²C bus is in an idle state and monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This condition indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte indicates that the master is writing information to the peripheral, whereas a Logic 1 indicates that the master is reading information from the peripheral after writing the subaddress and repeating the start address. A data transfer occurs until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 58 shows the timing of an I²C write, and Figure 59 shows the timing of an I²C read.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the ADAU1777 immediately jumps to the idle condition. During a given SCL high period, the user must issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If the user issues an invalid subaddress, the ADAU1777 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1777 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1777, and the device returns to the idle condition.

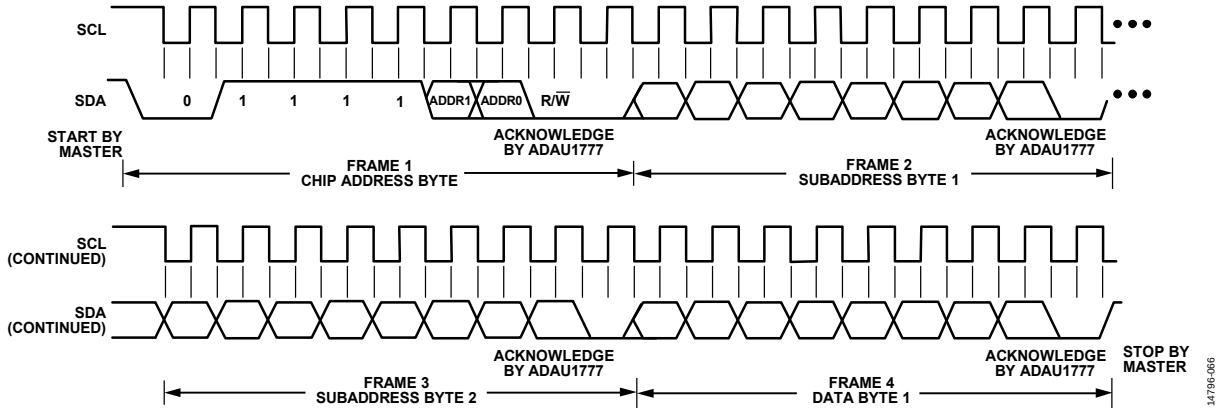



*Figure 58. I²C Write to ADAU1777 Clocking*

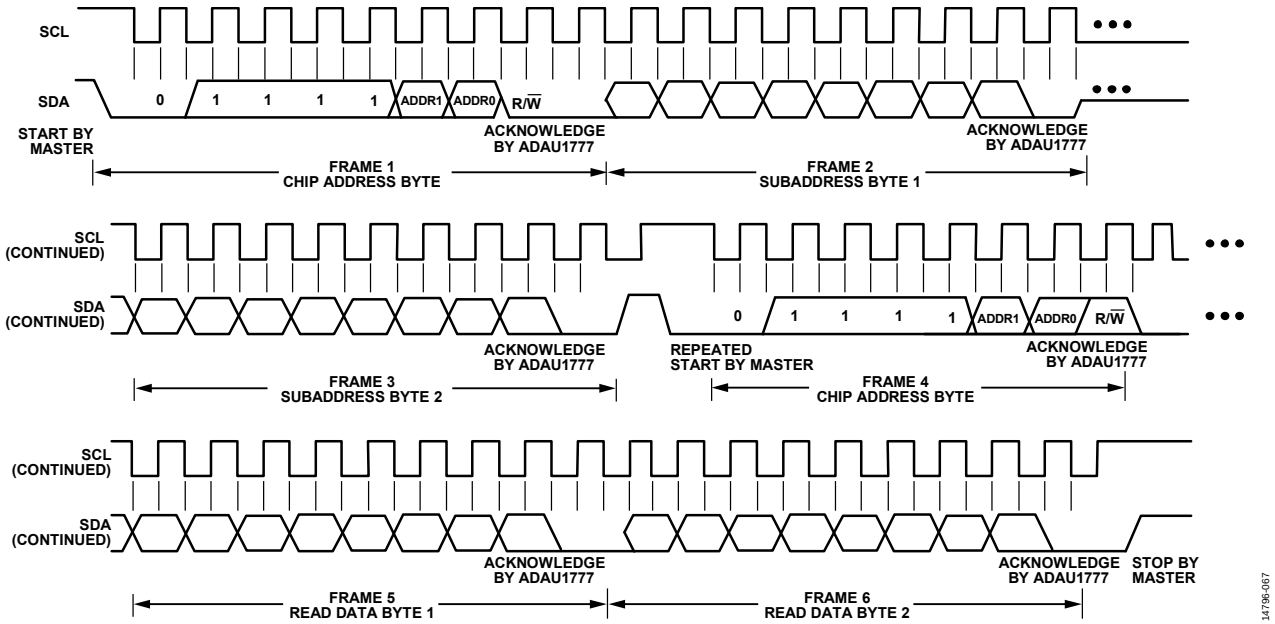



*Figure 59. I²C Read from ADAU1777 Clocking*

### I²C Read and Write Operations

Figure 60 shows the format of a single-word write operation. Every ninth clock pulse, the ADAU1777 issues an acknowledge by pulling SDA low.

Figure 61 shows the format of a burst mode write sequence. This figure shows an example where the target destination words are two bytes, such as the program memory. The ADAU1777 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The format of a single-word read operation is shown in Figure 62. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation because the subaddress still must be written to set up the internal address. After the ADAU1777 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). This command causes the SDA pin to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1777.

Figure 63 shows the format of a burst mode read sequence. This figure shows an example where the target read words are two bytes. The ADAU1777 increments its subaddress every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges may have a variety of word lengths, ranging from one to four bytes. The ADAU1777 always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

Figure 60 to Figure 63 use the following abbreviations:

- S = start bit
- P = stop bit
- AM = acknowledge by master
- AS = acknowledge by slave

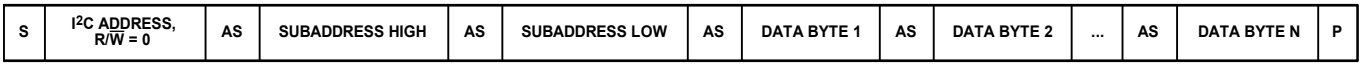



*Figure 60. Single-Word I²C Write Format*




*Figure 61. Burst Mode I²C Write Format*




*Figure 62. Single-Word I²C Read Format*




*Figure 63. Burst Mode I²C Read Format*

## SPI PORT

By default, the ADAU1777 is in I²C mode, but it can be put into SPI control mode by pulling $\overline{SS}$ low three times. The device can be configured for SPI mode by issuing three SPI writes, which are in turn ignored by the ADAU1777. The next (fourth) SPI write is then latched into the SPI port.

The SPI port uses a 4-wire interface—consisting of the $\overline{SS}$, SCLK, MOSI, and MISO signals—and is always a slave port. The $\overline{SS}$ signal goes low at the beginning of a transaction and high at the end of a transaction. The SCLK signal latches MOSI on a low to high transition. MISO data is shifted out of the ADAU1777 on the falling edge of SCLK and must be clocked into a receiving device, such as a microcontroller, on the SCLK rising edge. The MOSI signal carries the serial input data, and the MISO signal is the serial output data. The MISO signal remains tristated until a read operation is requested. Tristating allows other SPI-compatible peripherals to share the same readback line.

All SPI transactions have the same basic format shown in Table 23. Timing diagrams are shown in Figure 64 and Figure 65. All data is written MSB first. The ADAU1777 can be taken out of SPI mode only by pulling the $\overline{PD}$ pin low or by powering down the IC.

### *Read/Write*

The first byte of an SPI transaction indicates whether the communication is a read or a write with the R/$\overline{W}$ bit. The LSB of this first byte determines whether the SPI transaction is a read (Logic Level 1) or a write (Logic Level 0).

### *Subaddress*

The 16-bit subaddress word is decoded into a location of one of the memories or registers. This subaddress is the location of the appropriate memory location or register.

### *Data Bytes*

The number of data bytes varies according to the register or memory being accessed. During a burst mode write, an initial subaddress is written followed by a continuous sequence of data for consecutive memory/register locations.

A sample clocking diagram for a single write SPI operation to the parameter RAM is shown in Figure 64. A sample clocking diagram of a single read SPI operation is shown in Figure 65. The MISO pin goes from tristate to being driven at the beginning of Byte 3. In this example, Byte 0 to Byte 2 contain the addresses and the R/$\overline{W}$ bit and the subsequent bytes carry the data.

**Table 23. Generic SPI Word Format**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4[1] |
|---|---|---|---|---|
| 0000000, R/$\overline{W}$ | Register/Memory Address[15:8] | Register/Memory Address[7:0] | Data | Data |

[1] Continues to the end of data transmission for the burst mode write.

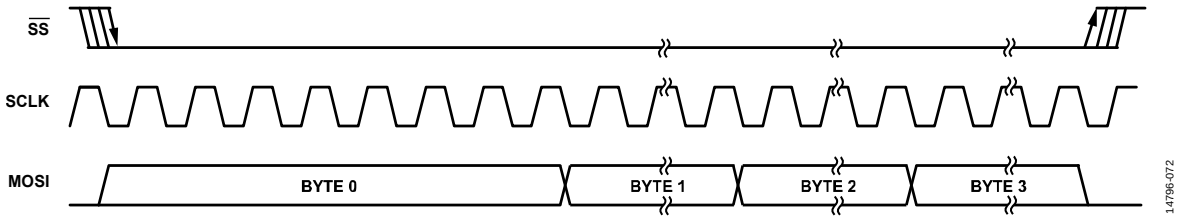



*Figure 64. SPI Write to ADAU1777 Clocking (Single Write Mode)*

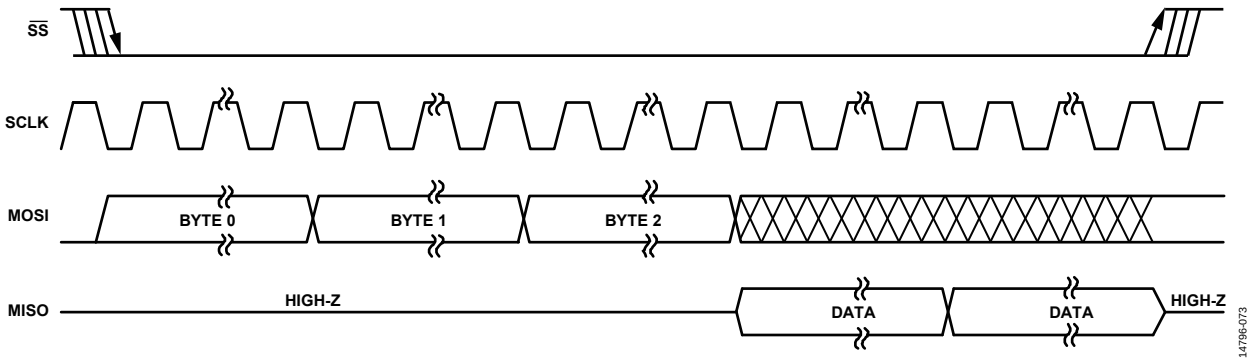



*Figure 65. SPI Read from ADAU1777 Clocking (Single Read Mode)*

## SELF BOOT

The ADAU1777 boots up from an EEPROM over the I²C bus when the SELFBOOT pin is set high at power-up and the $\overline{PD}$ pin is set high. The state of the SELFBOOT pin is checked only when the ADAU1777 exits a reset via the $\overline{PD}$ pin, and when the EEPROM is not used after a self boot is complete. During booting, ensure that a stable DVDD voltage is in the system. The $\overline{PD}$ pin remains high during the self boot operation. The master SCL clock output from the ADAU1777 is derived from the input clock on XTALI/MCLKIN. A divide by 64 circuit ensures that the SCL output frequency during the self boot operation is never greater than 400 kHz for most input clock frequencies. With the external master clock to the ADAU1777 between 12 MHz and 27 MHz, the SCL frequency ranges from 176 kHz to 422 kHz. If the self boot EEPROM is not rated for operation above 400 kHz, use a master clock that is no faster than 25.6 MHz.

Table 25 shows the list of instructions that are possible during an ADAU1777 self boot. The 0x01 and 0x05 instruction bytes load the register, program, and parameter settings.

### *EEPROM Size*

The self boot circuit is compatible with an EEPROM that has a 2-byte address. For most EEPROM families, a 2-byte address is used on devices that are 32 kB or larger. The EEPROM must be set to Address 0x50. Examples of two compatible EEPROMs include the Atmel® AT24C32D and STMicroelectronics M24C32-F.

Table 24 lists the maximum necessary EEPROM size, assuming that there is 100% utilization of the program and parameters (both banks). There is inherently some overhead for instructions to control the self boot procedure.

**Table 24. Maximum EEPROM Size**

| ADAU1777 Memory Blocks | Word Size (Bytes per Word) | Words | Total EEPROM Space Requirement (Bytes) |
|---|---|---|---|
| Program | 2 | 32 | 64 |
| Bank A Parameters | 4 | 160 (32 × 5) | 640 |
| Bank B Parameters | 4 | 160 | 640 |
| Registers | 1 | 65 | 65 |
| Total Bytes | | | 2049 |

### *Cyclic Redundancy Check (CRC)*

An 8-bit CRC validates the content of the EEPROM. This CRC is strong enough to detect single error bursts of up to eight bits in size. The terminate self boot instruction (0x instruction byte) must be followed by a CRC byte. The CRC is generated using all of the EEPROM bytes from Address 0x00 to the last 0x00 instruction byte. The polynomial for the CRC is

$$x^8 + x^2 + x + 1$$

If the CRC is incorrect or if an unrecognized instruction byte is read during self boot, the boot process is immediately stopped and restarted after a 250 ms delay (for a 12.288 MHz input clock). When SigmaStudio is used, the CRC byte is generated automatically when a configuration is downloaded to the EEPROM.

### *Delay*

The delay instruction (0x02 instruction byte) delays by the 16-bit setting × 2048 clock cycles.

### *Boot Time*

The time to self boot the ADAU1777 from an EEPROM can be calculated using the following equation:

$$Boot\ Time = 64/MCLK\ Frequency \times Total\ Bytes + Wait\ Time$$

The self boot operation starts after 16,568 clock cycles are seen on the XTALI/MCLKIN pin after $\overline{PD}$ is set high. With a 12.288 MHz clock, this number of cycles corresponds to approximately a 1.35 ms wait time from power-up. This delay ensures that the crystal used for generating the master clock has ramped up to a stable oscillation.

**Table 25. EEPROM Self Boot Instructions**

| Instruction Byte ID | Instruction Byte Description | Following Bytes |
|---|---|---|
| 0x00 | End self boot | CRC |
| 0x01 | Write multibyte length minus two bytes, starting at target address | Length (high byte), length (low byte), address (high byte), address (low byte), data (0), data (1), …, data (length – 3) |
| 0x02 | Delays by the 16-bit setting × 2048 clock cycles | Delay (high byte), delay (low byte) |
| 0x03 | No operation | None |
| 0x04 | Wait for PLL lock | None |
| 0x05 | Write single byte to target address | Address (high byte), address (low byte), data |

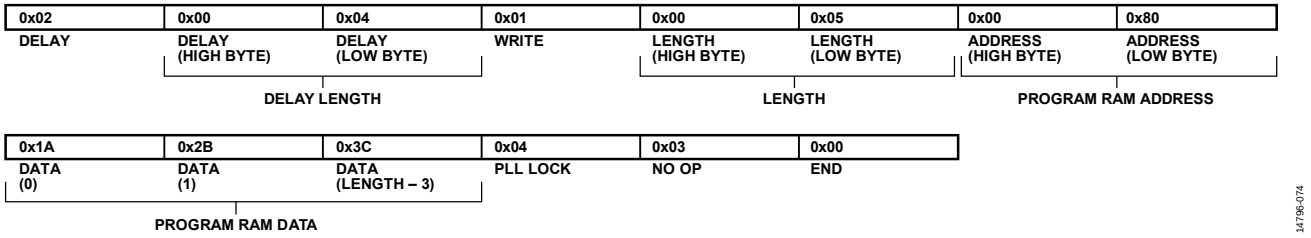



*Figure 66. Example Self Boot EEPROM Instructions*

# MULTIPURPOSE PINS

The ADAU1777 has seven multipurpose (MPx) pins that can be used for serial data input/output, clock outputs, and control in a system without a microcontroller. Each pin can be individually set to either its default or MPx setting. The functions include push-button volume controls, enabling the compressors, parameter bank switching, DSP bypass mode, and muting the outputs.

The function of each of these pins is set in Register 0x38 to Register 0x3E. By default, each pin is configured as an input.

**Table 26. Multipurpose Pin Functions**

| Pin No. | Default Pin Function | Secondary Pin Functions |
|---|---|---|
| A2 | BCLK | Multipurpose control inputs |
| A3 | MP1 acts as push-button volume up | ADC_SDATA0, PDM output, multipurpose control inputs |
| A4 | MP6 acts as push-button volume down | ADC_SDATA1, CLKOUT, multipurpose control inputs |
| B2 | LRCLK | Multipurpose control inputs |
| B3 | DAC_SDATA | Multipurpose control inputs |
| B4 | DMIC2_3 | Multipurpose control inputs |
| B5 | DMIC0_1 | Multipurpose control inputs |

## PUSH-BUTTON VOLUME CONTROLS

The ADC and DAC volume controls can be controlled with two push-buttons: one to increase volume and one to decrease volume. The volume setting can either be changed with a click of the button or can be ramped by holding either button but not both at the same time. The volume settings change when the signal on the pin from the button goes from low to high.

When in push-button mode, the initial volume level is set with the PB_VOL_INIT_VAL bits. By default, MP1 acts as the push-button volume up control and MP6 acts as the push-button volume down control; however, any of the MPx pins can be set to act as the push-button up and push-button down volume controls.

When the ADC and/or DAC volumes are controlled with the push-buttons, the corresponding volume control registers no longer allow control of the volume from the control port. Therefore, writing to these volume control registers has no effect on the codec volume level.

## LIMITER COMPRESSION ENABLE

The limiter compression enable function allows a user to enable limiter compression regardless of the signal level. Setting an MPx pin low when this function is enabled causes the limiter to compress the incoming signal by the minimum gain setting. When the MPx pin is released, the limiter resumes normal behavior.

## PARAMETER BANK SWITCHING

An MPx pin can be used to switch the active parameter bank between Bank A and Bank B. When one of these settings is selected, Bank A is active when the MPx pin is high and Bank B is active when the MPx pin is low. Set the BANK_SL bits in the CORE_CONTROL register (Address 0x09) to the default value of 0x00 before enabling MPx pin control over bank switching. Simultaneous control of bank switching by both register setting and MPx pin selection is not possible.

The ZERO_STATE bit selects whether the data memory of the codec is set to 0 during a bank switch. If the data is not set to 0 when a new set of filter coefficients is enabled via a bank switch, there may be a pop in the audio as the old data is circulated in the new filters.

## MUTE

The MPx pins can be put into a mode to mute the ADCs or DACs. When in this mode, mute is enabled when an MPx pin is set low. The full combination of possible mutes for the ADCs and DACs using the MPx pins are set in Register 0x38 to Register 0x3E.

## DSP BYPASS MODE

When DSP bypass mode is enabled, a direct path from the ADC outputs to the DACs is set up to enable bypassing the core processing to listen to environmental sounds. This mode is useful for listening to someone speaking without having to remove the noise canceling headphones. The DSP bypass path is enabled by setting an MPx pin low. Figure 67 shows the DSP bypass path disabled, and Figure 68 shows the DSP bypass path enabled by pressing the push-button switch. The DSP bypass feature works for both analog and digital microphone inputs.

DSP bypass is enabled when a switch connected to an MPx pin that is set to DSP bypass mode is closed and the MPx pin signal is pulled low. Pressing and holding the switch closed enables the DSP bypass signal path as defined in the TALKTHRU register (Address 0x2A). The DAC volume control setting is switched from the default gain setting to the new TALKTHRU_GAINx register setting (Address 0x2B and Address 0x2C). DSP bypass is enabled only on ADC0 and ADC1. The DSP bypass signal path is from the output of ADCx to the input of the DAC(s).

When DSP bypass is enabled, the current DAC volume setting is ramped down to −95.625 dB and the DSP bypass volume setting is ramped up to avoid pops when switching paths.

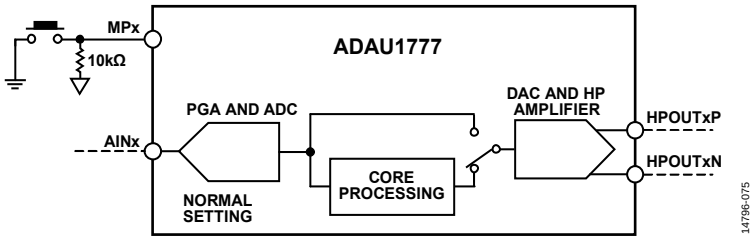



*Figure 67. DSP Bypass Path Disabled*

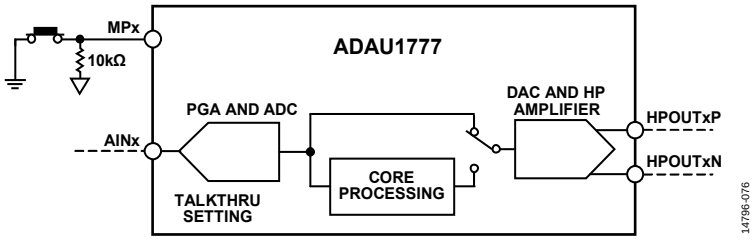



*Figure 68. DSP Bypass Path Enabled*

# SERIAL DATA INPUT/OUTPUT PORTS

The serial data input and output ports of the ADAU1777 can be set to accept or transmit data in a 2-channel format or in a 4-channel or 8-channel TDM stream mode to interface to external ADCs, DACs, DSPs, and systems on chip (SOCs). Data is processed in twos complement, MSB first format. The left channel data field always precedes the right channel data field in the 2-channel streams. In 8-channel TDM mode, the data channels are output sequentially, starting with the channel set by the ADC_SDATA0_ST and ADC_SDATA1_ST bits. The serial modes and the position of the data in the frame are set in the serial data port (SAI_0, SAI_1) and serial output control registers (SOUT_SOURCE_x_y, Address 0x13 to Address 0x16).

The serial data clocks do not need to be synchronous with the ADAU1777 master clock input, but the LRCLK and BCLK pins must be synchronous to each other. The LRCLK and BCLK pins both clock the serial input and output ports. The ADAU1777 can be set to be either the master or the slave in a system. Because there is only one set of serial data clocks, the input and output ports must always both be either master or slave.

The serial data control registers allow control of the clock polarity and the data input modes. The valid data formats are I²S, left justified, right justified (24- or 16-bit), PCM, and TDM. In all modes except for the right justified modes, the serial port inputs an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but they are truncated internally.

The serial port can operate with an arbitrary number of BCLK transitions in each LRCLK frame. The LRCLK in TDM mode can be input to the ADAU1777 either as a 50% duty cycle clock or as a 1-bit wide pulse. Table 27 lists the modes in which the serial input/output port can function. When using low IOVDD (1.8 V) with a high BCLK rate (12.288 MHz), a sample rate of 192 kHz, or a 8-channel TDM mode operating at a sample rate of 48 kHz, it is recommended to use the high drive settings on the serial port pins. The high drive strength effectively speeds up the transition times of the waveforms, thereby improving the signal integrity of the clock and data lines. These can be set in the PAD_CONTROL4 register (Address 0x4C).

**Table 27. Serial Input/Output Port Master/Slave Mode Capabilities**

| Serial Data Sample Rate | 2-Channel Modes (I²S, Left Justified, Right Justified) | 4-Channel TDM | 8-Channel TDM |
|---|---|---|---|
| 48 kHz | Yes | Yes | Yes |
| 96 kHz | Yes | Yes | No |
| 192 kHz | Yes | No | No |

Table 28 describes the proper serial port settings for standard audio data formats. More information about the settings in Table 28 is in the Serial Port Control 0 register and the Serial Port Control 1 register (Address 0x32 and Address 0x33) descriptions in Table 87 and Table 88, respectively.

## TRISTATING UNUSED CHANNELS

Unused outputs can be tristated so that multiple ICs can drive a single TDM line. This function is available only when the serial ports of the ADAU1777 are operating in TDM mode. Set inactive channels in the SOUT_CONTROL0 register (Address 0x34). The tristating of inactive channels is set in the SAI_1 register (Address 0x33), which offers the option of tristating or driving the inactive channel.

In a 32-bit TDM frame with 24-bit data, the eight unused bits are tristated. Inactive channels are also tristated for the full frame.

**Table 28. Serial Port Data Format Settings**

| Format | LRCLK Polarity (LR_POL) | LRCLK Type (LR_MODE) | BCLK Polarity (BCLKEDGE)[1] | MSB Position (SDATA_FMT) |
|---|---|---|---|---|
| I²S (See Figure 69) | 0 | 0 | 0 | 00 |
| Left Justified (See Figure 70) | 1 | 0 | 0 | 01 |
| Right Justified (See Figure 71 and Figure 72) | 1 | 0 | 0 | 10 or 11 |
| TDM (See Figure 73 and Figure 74) | 1 | 0 or 1 | 0 | 00 |
| PCM/DSP Short Frame Sync (See Figure 75) | 1 | 1 | X | 00 |
| PCM/DSP Long Frame Sync (See Figure 76) | 1 | 0 | X | 01 |

[1] X means don't care.

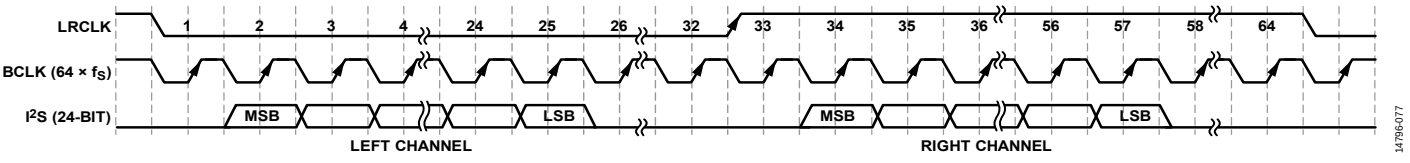



*Figure 69. I²S Mode, 16 Bits to 24 Bits per Channel*

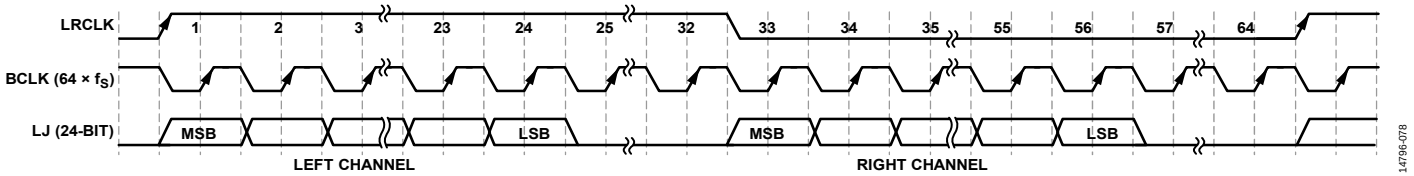



*Figure 70. Left Justified (LJ) Mode, 16 Bits to 24 Bits per Channel*

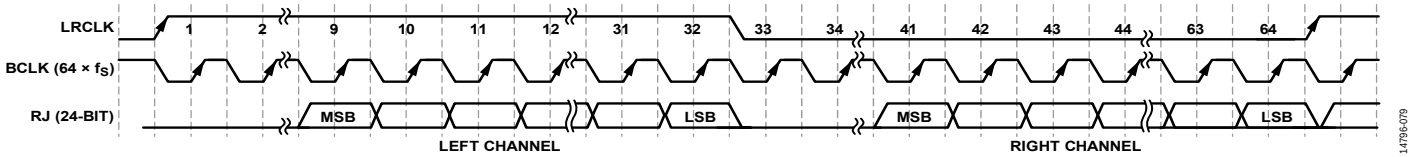



*Figure 71. Right Justified (RJ) Mode, 24 Bits per Channel*

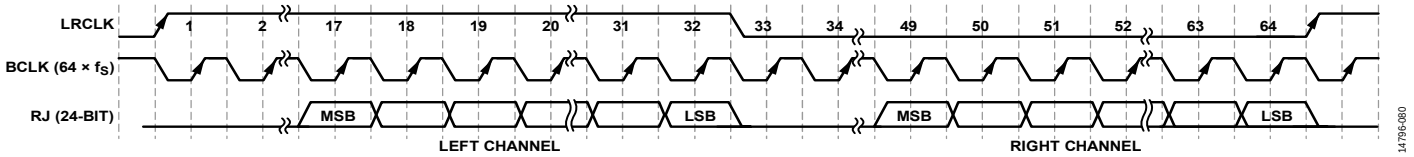



*Figure 72. Right Justified (RJ) Mode, 16 Bits per Channel*

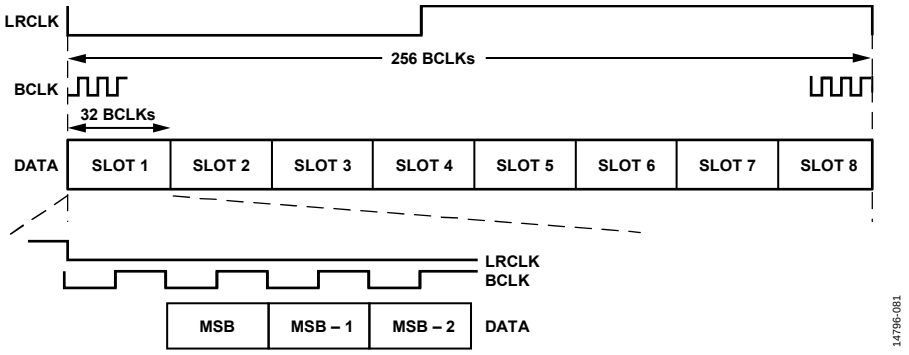



*Figure 73. 8-Channel TDM Mode*

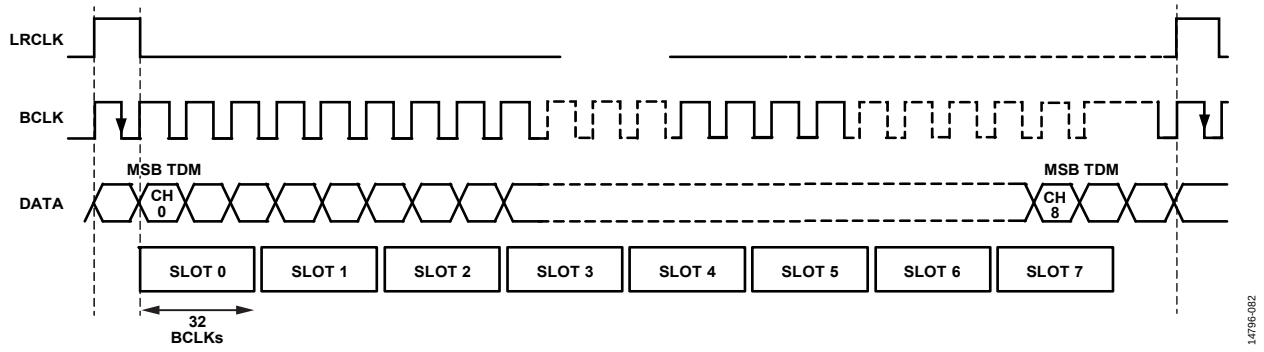



*Figure 74. 8-Channel TDM Mode, Pulse LRCLK*

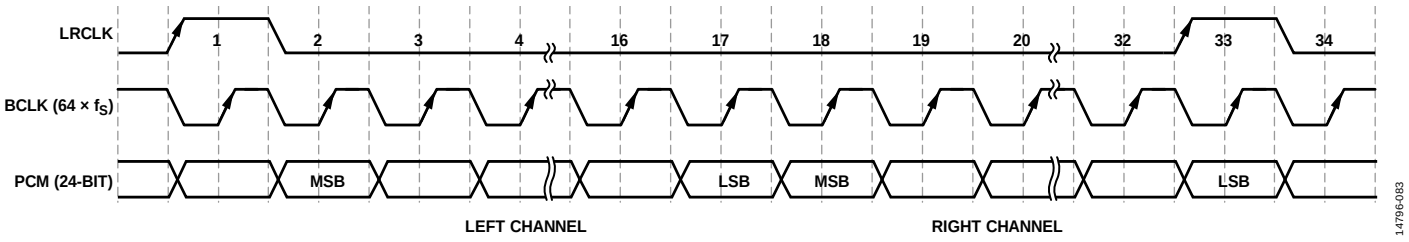



*Figure 75. PCM/DSP Mode, 16 Bits per Channel, Short Frame Sync*

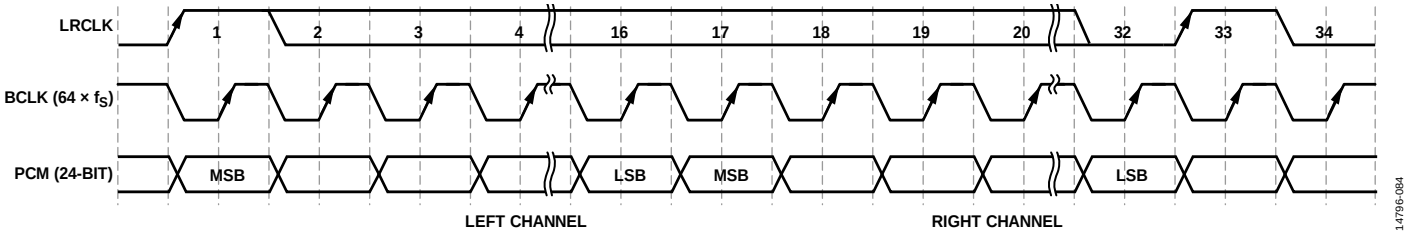



*Figure 76. PCM/DSP Mode, 16 Bits per Channel, Long Frame Sync*

# APPLICATIONS INFORMATION

## POWER SUPPLY BYPASS CAPACITORS

Bypass each analog and digital power supply pin to its nearest appropriate ground pin with a single 0.1 µF capacitor. The connections to each side of the capacitor must be as short as possible, and the trace must be routed on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or slightly closer to the power pin if equidistant placement is not possible. Make thermal connections to the ground planes on the far side of the capacitor.

Bypass each supply signal on the board with a single bulk capacitor (10 µF to 47 µF).

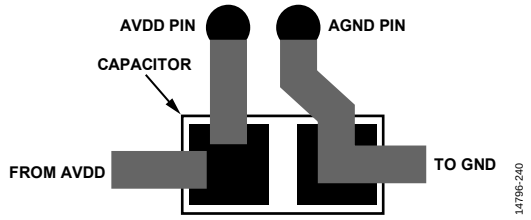



*Figure 77. Recommended Example Power Supply Bypass Capacitor Layout*

## LAYOUT

Pin D1 and Pin F2 are the AVDD supplies for the headphone amplifiers. If the headphone amplifiers are enabled, the PCB trace to these pins must be wider than traces to other pins to increase the current carrying capacity. A wider trace must also be used for the headphone output lines where possible.

## GROUNDING

A ground plane must be used in the application layout. Place components in an analog signal path away from digital signals wherever possible.

## PCB STACKUP

The example PCB stackup in Figure 78 is a 4-layer design. Four is the minimum layer count. The two inner layers are used as power and ground planes. The outer layers are used as signal layers and are flooded with the ground plane. It is recommended to use several 0.1 µF bypass capacitors to decouple the power and ground plane for EMI concerns. Place these capacitors around the edges of the ground plane.

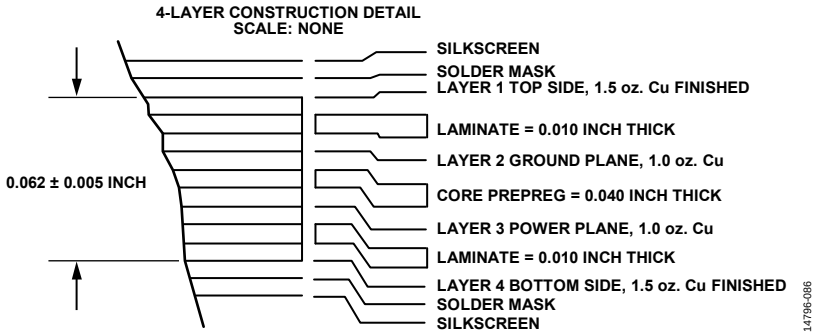



*Figure 78. Example PCB Stackup Details*

# LOW LATENCY REGISTER SETTINGS

The ADAU1777 utilizes the ADAU1772 architecture and incorporates additional register settings for reductions in latency, as shown in Table 29 to Table 35.

**Table 29. Core Control Register (Register 0x0009)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| [4:3] | FAST_SLOW_RATE | | These bits select the speed of the slow rate relative to the fast rate. This setting must not be changed while the core is running. The CORE_RUN bit must be set to 0 for this setting to be updated. |
| | | 00 | Slow rate = fast rate. |
| | | 01 | Slow rate = fast rate/4. |
| | | 10 | Slow rate = fast rate/8. |
| [2:1] | CORE_FS | | These bits select the core sample rate. Note that the ADAU1777 supports an additional 768 kHz sample rate for reduced latency. This setting must not be changed while the core is running. The CORE_RUN bit must be set to 0 for this setting to be updated. |
| | | 00 | Reserved. |
| | | 01 | 96 kHz. |
| | | 10 | 192 kHz. |
| | | 11 | 768 kHz. |

**Table 30. Sleep on Program Address Count Register (Register 0x000A)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| [4:0] | SLEEP | | The sleep on program address count register controls which registers are executed. Subtract 2 from the SLEEP bit setting to indicate the number of addresses that are affected. For example, if SLEEP = 7, only instructions at Address 0x0000 to Address 0x0005 are executed. This setting must not be changed while the core is running. The CORE_RUN bit must be set to 0 for this setting to be updated. |
| | | 00000 | No sleep, all instructions are executed. |
| | | 00001 | Reserved. |
| | | 00010 | Sleep on 0. |
| | | 00011 | Sleep on 1. |
| | | 11111 | Sleep on 29. |

**Table 31. ADC0/ADC1 Control 0 Register (Register 0x001B)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| 5 | ADC_0_1_SINC | | This bit selects either a third-order or fourth-order sinc filter. This setting must not be changed while the core is running. The CORE_RUN bit must be set to 0 for this setting to be updated. |
| | | 0 | Fourth-order sinc. |
| | | 1 | Third-order sinc. |
| [1:0] | ADC_0_1_FS | | These bits set the ADC sample rate. The ADAU1777 supports the option of 768 kHz as well. Note that the frequency selected must match the CORE_FS selected via Bits[2:1] of Register 0x0009. |
| | | 00 | 96 kHz. |
| | | 01 | 192 kHz. |
| | | 10 | 768 kHz. |
| | | 11 | Reserved. |

**Table 32. ADC2/ADC31 Control 0 Register (Register 0x001C)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| 5 | ADC_2_3_SINC | | This bit selects either a third-order or fourth-order sinc filter. This setting must not be changed while the core is running. The CORE_RUN bit must be set to 0 for this setting to be updated. |
| | | 0 | Fourth-order sinc. |
| | | 1 | Third-order sinc. |
| [1:0] | ADC_2_3_FS | | These bits set the ADC sample rate. The ADAU1777 supports the option of 768 kHz as well. |
| | | 00 | 96 kHz. |
| | | 01 | 192 kHz. |
| | | 10 | 768 kHz. |
| | | 11 | Reserved. |

**Table 33. Fast Rate Control Register (Register 0x004E)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| [2:0] | RATE_DIV | | Bits[2:0] set the fast rate division factor. This factor is used to divide the internal master clock (6.144 MHz) when CORE_FS = 11. This setting must not be changed while the core is running. CORE_RUN must be set to 0 for this setting to be updated. The settings for RATE_DIV follow: |
| | | 000 | Divide by 8 (768 kHz). |
| | | 001 | Divide by 9 (683 kHz). |
| | | 010 | Divide by 10 (614 kHz). |
| | | 011 | Divide by 12 (512 kHz). |
| | | 100 | Divide by 14 (439 kHz). |
| | | 101 | Divide by 16 (384 kHz). |

**Table 34. DAC Interpolation Control Register (Register 0x004F)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| [7:6] | DAC_RATE | | These bits set the DAC_RATE value, which sets the sample rate for the DAC only. |
| | | 00 | Core $f_S$. |
| | | 01 | Core $f_S/4$. |
| | | 10 | Core $f_S/8$. |
| | | 11 | Reserved. |
| [5:3] | DAC_INTP | | These bits set the DAC_INTP value, which sets the interpolation mode for the DAC. |
| | | 000 | Both DAC0 and DAC1 set to compensated interpolation. |
| | | 001 | DAC0 set to zero-order hold (ZOH), DAC1 set to compensated interpolation. |
| | | 010 | DAC0 set to compensated interpolation, DAC1 set to ZOH. |
| | | 011 | Both DAC0 and DAC1 set to ZOH. |
| | | 100 | DAC0 set to linear interpolation, DAC1 set to compensated interpolation. |
| | | 101 | DAC0 set to compensated interpolation, DAC1 set to linear interpolation. |
| | | 110 | Both DAC0 and DAC1 set to linear interpolation. |

**Table 35. Volume Control Bypass Register (Register 0x0054)**

| Bits | Bit Name | Settings | Description |
|---|---|---|---|
| 5 | DAC1VOL_BY | | DAC1 volume control bypass. |
| | | 0 | Volume control enabled. |
| | | 1 | Bypassed. |
| 4 | DAC0VOL_BY | | DAC0 volume control bypass. |
| | | 0 | Volume control enabled. |
| | | 1 | Bypassed. |
| 3 | ADC3VOL_BY | | ADC3 volume control bypass. |
| | | 0 | Volume control enabled. |
| | | 1 | Bypassed. |
| 2 | ADC2VOL_BY | | ADC2 volume control bypass. |
| | | 0 | Volume control enabled. |
| | | 1 | Bypassed. |
| 1 | ADC1VOL_BY | | ADC1 volume control bypass. |
| | | 0 | Volume control enabled. |
| | | 1 | Bypassed. |
| 0 | ADC0VOL_BY | | ADC0 volume control bypass. |
| | | 0 | Volume control enabled. |
| | | 1 | Bypassed. |

# REGISTER SUMMARY

**Table 36. Register Summary**

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CLK_CONTROL | [7:0] | PLL_EN | RESERVED | SPK_FLT_DIS | XTAL_DIS | CLKSRC | CC_CDIV | CC_MDIV | COREN | 0x00 | R/W |
| 0x01 | PLL_CTRL0 | [7:0] | M_MSB | | | | | | | | 0x00 | R/W |
| 0x02 | PLL_CTRL1 | [7:0] | M_LSB | | | | | | | | 0x00 | R/W |
| 0x03 | PLL_CTRL2 | [7:0] | N_MSB | | | | | | | | 0x00 | R/W |
| 0x04 | PLL_CTRL3 | [7:0] | N_LSB | | | | | | | | 0x00 | R/W |
| 0x05 | PLL_CTRL4 | [7:0] | RESERVED | R | | | | X | | PLL_TYPE | 0x00 | R/W |
| 0x06 | PLL_CTRL5 | [7:0] | RESERVED | | | | | | | LOCK | 0x00 | R/W |
| 0x07 | CLKOUT_SEL | [7:0] | RESERVED | | | | | CLKOUT_FREQ | | | 0x00 | R/W |
| 0x08 | REGULATOR | [7:0] | RESERVED | | | | | REG_PD | REGV | | 0x00 | R/W |
| 0x09 | CORE_CONTROL | [7:0] | ZERO_ STATE | BANK_SL | | FAST_SLOW_RATE | | CORE_FS | | CORE_RUN | 0x04 | R/W |
| 0x0A | SLEEP_INST | [7:0] | RESERVED | | | SLEEP | | | | | 0x00 | R/W |
| 0x0B | CORE_ENABLE | [7:0] | RESERVED | | | | | | LIM_EN | DSP_CLK_ EN | 0x03 | R/W |
| 0x0C | DBREG0 | [7:0] | DBVAL0 | | | | | | | | 0x00 | R |
| 0x0D | DBREG1 | [7:0] | DBVAL1 | | | | | | | | 0x00 | R |
| 0x0E | DBREG2 | [7:0] | DBVAL2 | | | | | | | | 0x00 | R |
| 0x0F | CORE_IN_MUX_ 0_1 | [7:0] | CORE_IN_MUX_SEL_1 | | | | CORE_IN_MUX_SEL_0 | | | | 0x10 | R/W |
| 0x10 | CORE_IN_MUX_ 2_3 | [7:0] | CORE_IN_MUX_SEL_3 | | | | CORE_IN_MUX_SEL_2 | | | | 0x32 | R/W |
| 0x11 | DAC_SOURCE_ 0_1 | [7:0] | DAC_SOURCE1 | | | | DAC_SOURCE0 | | | | 0x10 | R/W |
| 0x12 | PDM_SOURCE_ 0_1 | [7:0] | PDM_SOURCE1 | | | | PDM_SOURCE0 | | | | 0x32 | R/W |
| 0x13 | SOUT_SOURCE_ 0_1 | [7:0] | SOUT_SOURCE1 | | | | SOUT_SOURCE0 | | | | 0x54 | R/W |
| 0x14 | SOUT_SOURCE_ 2_3 | [7:0] | SOUT_SOURCE3 | | | | SOUT_SOURCE2 | | | | 0x76 | R/W |
| 0x15 | SOUT_SOURCE_ 4_5 | [7:0] | SOUT_SOURCE5 | | | | SOUT_SOURCE4 | | | | 0x54 | R/W |
| 0x16 | SOUT_SOURCE_ 6_7 | [7:0] | SOUT_SOURCE7 | | | | SOUT_SOURCE6 | | | | 0x76 | R/W |
| 0x17 | ADC_SDATA_ CH | [7:0] | RESERVED | | | | ADC_SDATA1_ST | | ADC_SDATA0_ST | | 0x04 | R/W |
| 0x18 | ASRCO_ SOURCE_0_1 | [7:0] | ASRC_OUT_SOURCE1 | | | | ASRC_OUT_SOURCE0 | | | | 0x10 | R/W |
| 0x19 | ASRCO_ SOURCE_2_3 | [7:0] | ASRC_OUT_SOURCE3 | | | | ASRC_OUT_SOURCE2 | | | | 0x32 | R/W |
| 0x1A | ASRC_MODE | [7:0] | RESERVED | | | | ASRC_IN_CH | | ASRC_OUT_EN | ASRC_IN_ EN | 0x00 | R/W |
| 0x1B | ADC_ CONTROL0 | [7:0] | RESERVED | | ADC_0_1_ SINC | ADC1_MUTE | ADC0_MUTE | RESERVED | ADC_0_1_FS | | 0x19 | R/W |
| 0x1C | ADC_ CONTROL1 | [7:0] | RESERVED | | ADC_2_3_ SINC | ADC3_MUTE | ADC2_MUTE | RESERVED | ADC_2_3_FS | | 0x19 | R/W |
| 0x1D | ADC_ CONTROL2 | [7:0] | RESERVED | HP_0_1_EN | | DMIC_POL0 | DMIC_SW0 | DCM_0_1 | ADC_1_EN | ADC_0_EN | 0x00 | R/W |
| 0x1E | ADC_ CONTROL3 | [7:0] | RESERVED | HP_2_3_EN | | DMIC_POL1 | DMIC_SW1 | DCM_2_3 | ADC_3_EN | ADC_2_EN | 0x00 | R/W |
| 0x1F | ADC0_VOLUME | [7:0] | ADC_0_VOL | | | | | | | | 0x00 | R/W |
| 0x20 | ADC1_VOLUME | [7:0] | ADC_1_VOL | | | | | | | | 0x00 | R/W |
| 0x21 | ADC2_VOLUME | [7:0] | ADC_2_VOL | | | | | | | | 0x00 | R/W |
| 0x22 | ADC3_VOLUME | [7:0] | ADC_3_VOL | | | | | | | | 0x00 | R/W |

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x23 | PGA_CONTROL_0 | [7:0] | PGA_EN0 | PGA_MUTE0 | PGA_GAIN0 | | | | | | 0x40 | R/W |
| 0x24 | PGA_CONTROL_1 | [7:0] | PGA_EN1 | PGA_MUTE1 | PGA_GAIN1 | | | | | | 0x40 | R/W |
| 0x25 | PGA_CONTROL_2 | [7:0] | PGA_EN2 | PGA_MUTE2 | PGA_GAIN2 | | | | | | 0x40 | R/W |
| 0x26 | PGA_CONTROL_3 | [7:0] | PGA_EN3 | PGA_MUTE3 | PGA_GAIN3 | | | | | | 0x40 | R/W |
| 0x27 | PGA_STEP_CONTROL | [7:0] | RESERVED | | SLEW_RATE | | SLEW_PD3 | SLEW_PD2 | SLEW_PD1 | SLEW_PD0 | 0x00 | R/W |
| 0x28 | PGA_10DB_BOOST | [7:0] | RESERVED | | | | PGA_3_BOOST | PGA_2_BOOST | PGA_1_BOOST | PGA_0_BOOST | 0x00 | R/W |
| 0x29 | POP_SUPPRESS | [7:0] | RESERVED | | HP_POP_DIS1 | HP_POP_DIS0 | PGA_POP_DIS3 | PGA_POP_DIS2 | PGA_POP_DIS1 | PGA_POP_DIS0 | 0x3F | R/W |
| 0x2A | TALKTHRU | [7:0] | RESERVED | | | | | | TALKTHRU_PATH | | 0x00 | R/W |
| 0x2B | TALKTHRU_GAIN0 | [7:0] | TALKTHRU_GAIN0_VAL | | | | | | | | 0x00 | R/W |
| 0x2C | TALKTHRU_GAIN1 | [7:0] | TALKTHRU_GAIN1_VAL | | | | | | | | 0x00 | R/W |
| 0x2D | MIC_BIAS | [7:0] | RESERVED | | MIC_EN1 | MIC_EN0 | RESERVED | RESERVED | MIC_GAIN1 | MIC_GAIN0 | 0x00 | R/W |
| 0x2E | DAC_CONTROL1 | [7:0] | RESERVED | | DAC_POL | DAC1_MUTE | DAC0_MUTE | RESERVED | DAC1_EN | DAC0_EN | 0x18 | R/W |
| 0x2F | DAC0_VOLUME | [7:0] | DAC_0_VOL | | | | | | | | 0x00 | R/W |
| 0x30 | DAC1_VOLUME | [7:0] | DAC_1_VOL | | | | | | | | 0x00 | R/W |
| 0x31 | OP_STAGE_MUTES | [7:0] | RESERVED | | | | HP_MUTE_R | | HP_MUTE_L | | 0x0F | R/W |
| 0x32 | SAI_0 | [7:0] | SDATA_FMT | | SAI | | SER_PORT_FS | | | | 0x00 | R/W |
| 0x33 | SAI_1 | [7:0] | TDM_TS | BCLK_TDMC | LR_MODE | LR_POL | SAI_MSB | BCLKRATE | BCLKEDGE | SAI_MS | 0x00 | R/W |
| 0x34 | SOUT_CONTROL0 | [7:0] | TDM7_DIS | TDM6_DIS | TDM5_DIS | TDM4_DIS | TDM3_DIS | TDM2_DIS | TDM1_DIS | TDM0_DIS | 0x00 | R/W |
| 0x36 | PDM_OUT | [7:0] | RESERVED | | | PDM_CTRL | PDM_CH | | PDM_EN | | 0x00 | R/W |
| 0x37 | PDM_PATTERN | [7:0] | PATTERN | | | | | | | | 0x00 | R/W |
| 0x38 | MODE_MP0 | [7:0] | RESERVED | | | MODE_MP0_VAL | | | | | 0x00 | R/W |
| 0x39 | MODE_MP1 | [7:0] | RESERVED | | | MODE_MP1_VAL | | | | | 0x10 | R/W |
| 0x3A | MODE_MP2 | [7:0] | RESERVED | | | MODE_MP2_VAL | | | | | 0x00 | R/W |
| 0x3B | MODE_MP3 | [7:0] | RESERVED | | | MODE_MP3_VAL | | | | | 0x00 | R/W |
| 0x3C | MODE_MP4 | [7:0] | RESERVED | | | MODE_MP4_VAL | | | | | 0x00 | R/W |
| 0x3D | MODE_MP5 | [7:0] | RESERVED | | | MODE_MP5_VAL | | | | | 0x00 | R/W |
| 0x3E | MODE_MP6 | [7:0] | RESERVED | | | MODE_MP6_VAL | | | | | 0x11 | R/W |
| 0x3F | PB_VOL_SET | [7:0] | PB_VOL_INIT_VAL | | | | | HOLD | | | 0x00 | R/W |
| 0x40 | PB_VOL_CONV | [7:0] | GAINSTEP | | RAMPSPEED | | | PB_VOL_CONV_VAL | | | 0x87 | R/W |
| 0x41 | DEBOUNCE_MODE | [7:0] | RESERVED | | | | | DEBOUNCE | | | 0x05 | R/W |
| 0x43 | OP_STAGE_CTRL | [7:0] | RESERVED | | HP_EN_R | HP_EN_L | HP_PDN_R | | HP_PDN_L | | 0x0F | R/W |
| 0x44 | DECIM_PWR_MODES | [7:0] | DEC_3_EN | DEC_2_EN | DEC_1_EN | DEC_0_EN | SINC_3_EN | SINC_2_EN | SINC_1_EN | SINC_0_EN | 0x00 | R/W |
| 0x45 | INTERP_PWR_MODES | [7:0] | RESERVED | | | | MOD_1_EN | MOD_0_EN | INT_1_EN | INT_0_EN | 0x00 | R/W |
| 0x46 | BIAS_CONTROL0 | [7:0] | HP_IBIAS | | AFE_IBIAS01 | | ADC_IBIAS23 | | ADC_IBIAS01 | | 0x00 | R/W |
| 0x47 | BIAS_CONTROL1 | [7:0] | RESERVED | CBIAS_DIS | AFE_IBIAS23 | | MIC_IBIAS | | DAC_IBIAS | | 0x00 | R/W |
| 0x48 | PAD_CONTROL0 | [7:0] | RESERVED | DMIC2_3_PU | DMIC0_1_PU | LRCLK_PU | BCLK_PU | ADC_SDATA1_PU | ADC_SDATA0_PU | DAC_SDATA_PU | 0x7F | R/W |
| 0x49 | PAD_CONTROL1 | [7:0] | RESERVED | | | SELFBOOT_PU | SCL_PU | SDA_PU | ADDR1_PU | ADDR0_PU | 0x1F | R/W |

| Reg. | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x4A | PAD_ CONTROL2 | [7:0] | RESERVED | DMIC2_3_ PD | DMIC0_1_PD | LRCLK_PD | BCLK_PD | ADC_SDATA1_ PD | ADC_SDATA0_ PD | DAC_ SDATA_PD | 0x00 | R/W |
| 0x4B | PAD_ CONTROL3 | [7:0] | RESERVED | | | SELFBOOT_ PD | SCL_PD | SDA_PD | ADDR1_PD | ADDR0_ PD | 0x00 | R/W |
| 0x4C | PAD_ CONTROL4 | [7:0] | RESERVED | RESERVED | RESERVED | LRCLK_DRV | BCLK_DRV | ADC_SDATA1_ DRV | ADC_SDATA0_ DRV | RESERVED | 0x00 | R/W |
| 0x4D | PAD_ CONTROL5 | [7:0] | RESERVED | | | RESERVED | SCL_DRV | SDA_DRV | RESERVED | RESERVED | 0x00 | R/W |
| 0x4E | FAST_RATE | [7:0] | RESERVED | | | | | RATE_DIV | | | 0x00 | R/W |
| 0x4F | DAC_ CONTROL0 | [7:0] | DAC_RATE | | DAC_INTP | | | RESERVED | | | 0x00 | R/W |
| 0x54 | VOL_BYPASS | [7:0] | RESERVED | | DAC1VOL_BY | DAC0VOL_ BY | ADC3VOL_BY | ADC2VOL_BY | ADC1VOL_BY | ADC0VOL_ BY | 0x00 | R/W |

# REGISTER DETAILS

## CLOCK CONTROL REGISTER

**Address: 0x00, Reset: 0x00, Name: CLK_CONTROL**

This register enables the internal clocks.

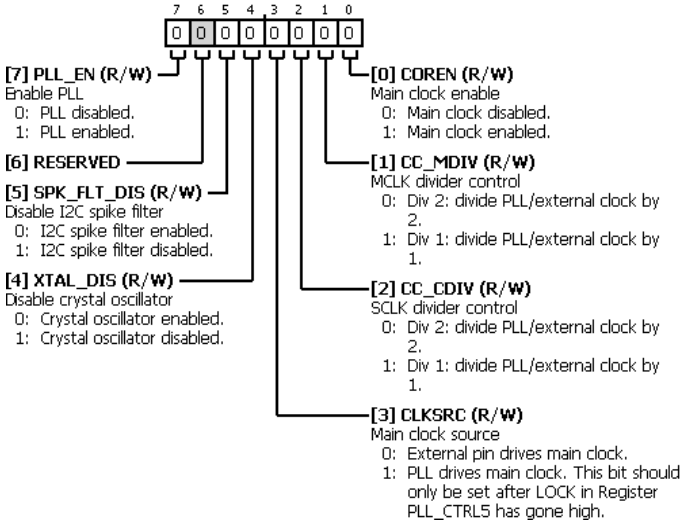



**Table 37. Bit Descriptions for CLK_CONTROL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | PLL_EN | | Enable PLL. When this bit is set to 0, the PLL is powered down and the PLL output clock is disabled. Do not enable the PLL until after all the PLL control settings (Register PLL_CTRL0 to Register PLL_CTRL5) are set. The PLL clock output is active when both PLL_EN = 1 and COREN = 1. | 0x0 | R/W |
| | | 0 | PLL disabled. | | |
| | | 1 | PLL enabled. | | |
| 6 | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | SPK_FLT_DIS | | Disable I²C spike filter. By default, the SDA and SCL inputs have a 50 ns spike suppression filter. When the control interface is in SPI mode, this filter is disabled regardless of this setting. | 0x0 | R/W |
| | | 0 | I²C spike filter enabled. | | |
| | | 1 | I²C spike filter disabled. | | |
| 4 | XTAL_DIS | | Disable crystal oscillator. | 0x0 | R/W |
| | | 0 | Crystal oscillator enabled. | | |
| | | 1 | Crystal oscillator disabled. | | |
| 3 | CLKSRC | | Main clock source. | 0x0 | R/W |
| | | 0 | External pin drives main clock. | | |
| | | 1 | PLL drives main clock. This bit must only be set after LOCK in Register PLL_CTRL5 has gone high. | | |
| 2 | CC_CDIV | | SCLK divider control. The core clock (SCLK) is used only by the core. It must run at 12.288 MHz. | 0x0 | R/W |
| | | 0 | Div 2: divide PLL/external clock by 2. | | |
| | | 1 | Div 1: divide PLL/external clock by 1. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 1 | CC_MDIV | | MCLK divider control. The internal master clock (MCLK) of the IC is used by all digital logic except the core. It must run at 12.288 MHz. | 0x0 | R/W |
| | | 0 | Div 2: divide PLL/external clock by 2. | | |
| | | 1 | Div 1: divide PLL/external clock by 1. | | |
| 0 | COREN | | Main clock enable. When COREN = 0, it is only possible to write to this register and the PLL control registers (PLL_CTRL0 to PLL_CTRL5). This control also enables the PLL clock. If using the PLL, do not set COREN = 1 until LOCK in Register PLL_CTRL5 is 1. Note that, after COREN is enabled, writing to the parameters is disabled until setting DSP_CLK_EN in the CORE_ENABLE register. | 0x0 | R/W |
| | | 0 | Main clock disabled. | | |
| | | 1 | Main clock enabled. | | |

## PLL DENOMINATOR MSB REGISTER

**Address: 0x01, Reset: 0x00, Name: PLL_CTRL0**

Only write to this register when PLL_EN = 0 in Register CLK_CONTROL.

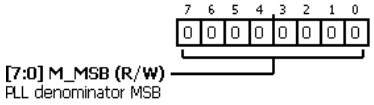



**Table 38. Bit Descriptions for PLL_CTRL0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | M_MSB | | PLL denominator MSB. | 0x0 | R/W |

## PLL DENOMINATOR LSB REGISTER

**Address: 0x02, Reset: 0x00, Name: PLL_CTRL1**

Only write to this register when PLL_EN = 0 in Register CLK_CONTROL.

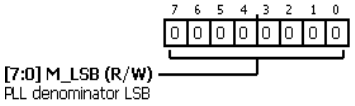



**Table 39. Bit Descriptions for PLL_CTRL1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | M_LSB | | PLL denominator LSB. | 0x0 | R/W |

## PLL NUMERATOR MSB REGISTER

**Address: 0x03, Reset: 0x00, Name: PLL_CTRL2**

Only write to this register when PLL_EN = 0 in Register CLK_CONTROL.

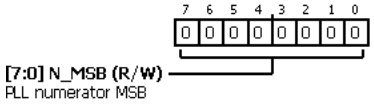



**Table 40. Bit Descriptions for PLL_CTRL2**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | N_MSB | | PLL numerator MSB. | 0x0 | R/W |

## PLL NUMERATOR LSB REGISTER

**Address: 0x04, Reset: 0x00, Name: PLL_CTRL3**

Only write to this register when PLL_EN = 0 in Register CLK_CONTROL.

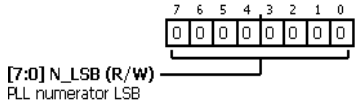



**Table 41. Bit Descriptions for PLL_CTRL3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | N_LSB | | PLL numerator LSB. | 0x0 | R/W |

## PLL INTEGER SETTING REGISTER

**Address: 0x05, Reset: 0x00, Name: PLL_CTRL4**

Only write to this register when PLL_EN = 0 in Register CLK_CONTROL.

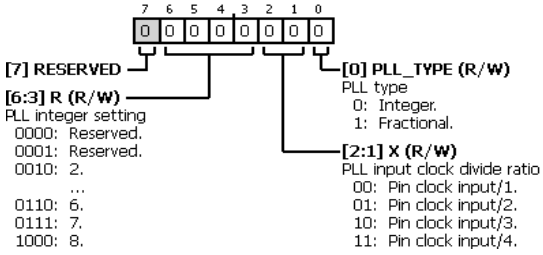



**Table 42. Bit Descriptions for PLL_CTRL4**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| [6:3] | R | | PLL integer setting. | 0x0 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | 2. | | |
| | | 0011 | 3. | | |
| | | 0100 | 4. | | |
| | | 0101 | 5. | | |
| | | 0110 | 6. | | |
| | | 0111 | 7. | | |
| | | 1000 | 8. | | |
| [2:1] | X | | PLL input clock divide ratio. | 0x0 | R/W |
| | | 00 | Pin clock input/1. | | |
| | | 01 | Pin clock input/2. | | |
| | | 10 | Pin clock input/3. | | |
| | | 11 | Pin clock input/4. | | |
| 0 | PLL_TYPE | | PLL type. | 0x0 | R/W |
| | | 0 | Integer. | | |
| | | 1 | Fractional. | | |

## PLL LOCK FLAG REGISTER

**Address: 0x06, Reset: 0x00, Name: PLL_CTRL5**

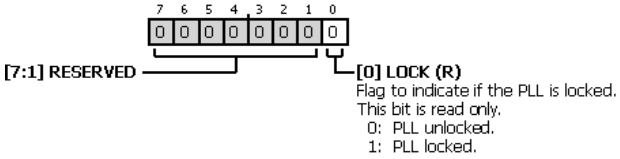



**Table 43. Bit Descriptions for PLL_CTRL5**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:1] | RESERVED | | Reserved. | 0x0 | R/W |
| 0 | LOCK | | Flag to indicate if the PLL is locked. This bit is read only. | 0x0 | R |
| | | 0 | PLL unlocked. | | |
| | | 1 | PLL locked. | | |

## CLKOUT SETTING SELECTION REGISTER

**Address: 0x07, Reset: 0x00, Name: CLKOUT_SEL**

When the ADC_SDATA1/CLKOUT/MP6 pin is set to clock output mode, the frequency of the output clock is set in this register. CLKOUT can be used to provide a master clock to another IC, the clock for digital microphones, or as the clock for the PDM output stream. The 12 MHz/24 MHz setting is used when clocking another IC, 3 MHz/6 MHz is used for PDMOUT, and 1.5 MHz/3 MHz is used when clocking digital microphones. The CLKOUT frequency is derived from the master clock frequency, which is assumed to (and always must) be 12.288 MHz. The 12.288 MHz and 24.576 MHz output modes are not functional if PDM is enabled (Register PDM_OUT, Bits[1:0]).

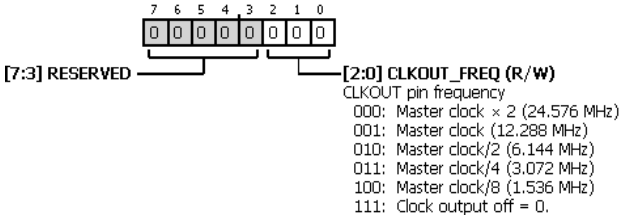



**Table 44. Bit Descriptions for CLKOUT_SEL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:3] | RESERVED | | Reserved. | 0x0 | R/W |
| [2:0] | CLKOUT_FREQ | | CLKOUT pin frequency. | 0x0 | R/W |
| | | 000 | Master clock × 2 (24.576 MHz). | | |
| | | 001 | Master clock (12.288 MHz). | | |
| | | 010 | Master clock/2 (6.144 MHz). | | |
| | | 011 | Master clock/4 (3.072 MHz). | | |
| | | 100 | Master clock/8 (1.536 MHz). | | |
| | | 111 | Clock output off = 0. | | |

## REGULATOR CONTROL REGISTER

**Address: 0x08, Reset: 0x00, Name: REGULATOR**

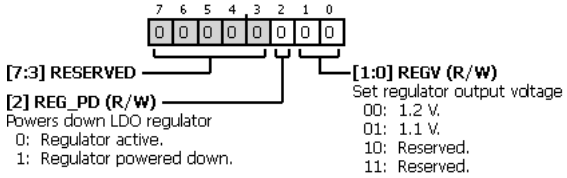



**Table 45. Bit Descriptions for REGULATOR**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:3] | RESERVED | | Reserved. | 0x0 | R/W |
| 2 | REG_PD | | Powers down LDO regulator. | 0x0 | R/W |
| | | 0 | Regulator active. | | |
| | | 1 | Regulator powered down. | | |
| [1:0] | REGV | | Set regulator output voltage. | 0x0 | R/W |
| | | 00 | 1.2 V. | | |
| | | 01 | 1.1 V. | | |
| | | 10 | Reserved. | | |
| | | 11 | Reserved. | | |

## CORE CONTROL REGISTER

**Address: 0x09, Reset: 0x04, Name: CORE_CONTROL**

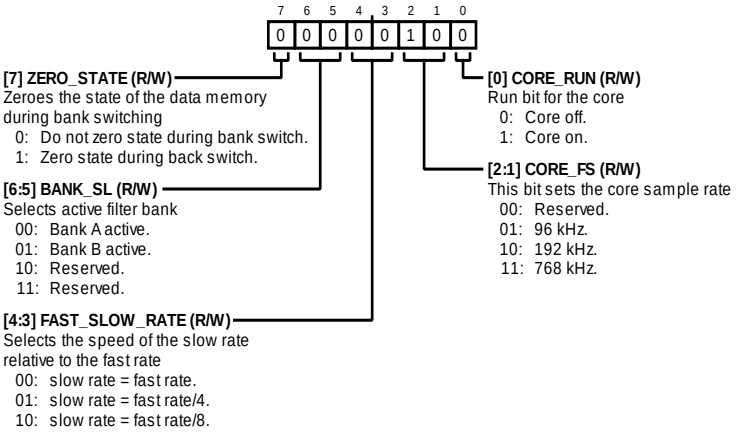



**Table 46. Bit Descriptions for CORE_CONTROL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | ZERO_STATE | | Zeroes the state of the data memory during bank switching. When switching active parameter banks between two settings, zeroing the state of the bank prevents the new filter settings from being active on old data that is recirculating in the filters. Zeroing the state may prevent filter instability or unwanted noises upon bank switching. | 0x0 | R/W |
| | | 0 | Do not zero state during bank switch. | | |
| | | 1 | Zero state during back switch. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [6:5] | BANK_SL | | Selects active filter bank. | 0x0 | R/W |
| | | 00 | Bank A active. | | |
| | | 01 | Bank B active. | | |
| | | 10 | Reserved. | | |
| | | 11 | Reserved. | | |
| [4:3] | FAST_SLOW_RATE | | Selects the speed of the slow rate relative to the fast rate. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x0 | R/W |
| | | 00 | Slow rate = fast rate. | | |
| | | 01 | Slow rate = fast rate/4. | | |
| | | 10 | Slow rate = fast rate/8. | | |
| [2:1] | CORE_FS | | This bit sets the core sample rate. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x2 | R/W |
| | | 00 | Reserved. | | |
| | | 01 | 96 kHz. | | |
| | | 10 | 192 kHz. | | |
| | | 11 | 768 kHz. When this mode is set, the fast rate of the core is set in Bits RATE_DIV in the fast rate control register. | | |
| 0 | CORE_RUN | | Run bit for the core. Enable this bit only when the program and parameters are loaded and the sample rate settings are set. CORE_RUN starts and stops the core at the beginning of the program. | 0x0 | R/W |
| | | 0 | Core off. | | |
| | | 1 | Core on. | | |

## SLEEP ON PROGRAM ADDRESS COUNT REGISTER

**Address: 0x0A, Reset: 0x00, Name: SLEEP_INST**

The SLEEP bits control which registers are sleeping. For example, if SLEEP = 7, only instructions at Address 0x00 to Address 0x05 are executed. SLEEP = 0 disables sleeping.

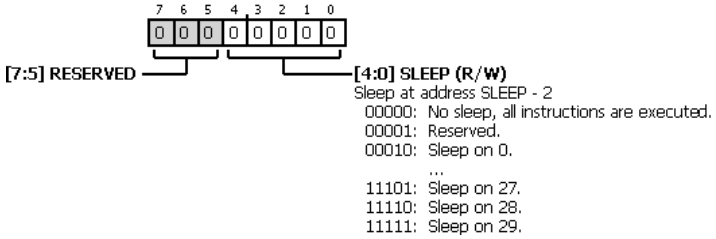


**Table 47. Bit Descriptions for SLEEP_INST**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | SLEEP | | Sleep at Address SLEEP − 2. These bits control which registers are sleeping. Subtracting 2 from the SLEEP setting indicates the number of addresses that are affected. For example, if SLEEP = 7, only instructions at Address 0x00 to Address 0x05 are executed. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x0 | R/W |
| | | 00000 | No sleep, all instructions are executed. | | |
| | | 00001 | Reserved. | | |
| | | 00010 | Sleep on 0 (0x00). | | |
| | | 00011 | Sleep on 1 (0x01). | | |
| | | 00100 | Sleep on 2 (0x02). | | |
| | | 00101 | Sleep on 3 (0x03). | | |
| | | 00110 | Sleep on 4 (0x04). | | |
| | | 00111 | Sleep on 5 (0x05). | | |
| | | 01000 | Sleep on 6 (0x06). | | |
| | | 01001 | Sleep on 7 (0x07). | | |
| | | 01010 | Sleep on 8 (0x08). | | |
| | | 01011 | Sleep on 9 (0x09). | | |
| | | 01100 | Sleep on 10 (0x0A). | | |
| | | 01101 | Sleep on 11 (0x0B). | | |
| | | 01110 | Sleep on 12 (0x0C). | | |
| | | 01111 | Sleep on 13 (0x0D). | | |
| | | 10000 | Sleep on 14 (0x0E). | | |
| | | 10001 | Sleep on 15 (0x0F). | | |
| | | 10010 | Sleep on 16 (0x10). | | |
| | | 10011 | Sleep on 17 (0x11). | | |
| | | 10100 | Sleep on 18 (0x12). | | |
| | | 10101 | Sleep on 19 (0x13). | | |
| | | 10110 | Sleep on 20 (0x14). | | |
| | | 10111 | Sleep on 21 (0x15). | | |
| | | 11000 | Sleep on 22 (0x16). | | |
| | | 11001 | Sleep on 23 (0x17). | | |
| | | 11010 | Sleep on 24 (0x18). | | |
| | | 11011 | Sleep on 25 (0x19). | | |
| | | 11100 | Sleep on 26 (0x1A). | | |
| | | 11101 | Sleep on 27 (0x1B). | | |
| | | 11110 | Sleep on 28 (0x1C). | | |
| | | 11111 | Sleep on 29 (0x1D). | | |

## FILTER ENGINE AND LIMITER CONTROL REGISTER

**Address: 0x0B, Reset: 0x03, Name: CORE_ENABLE**

Disabling the limiter only disables the attack operation. The decay operation is always active; therefore, a limiter can be safely disabled while the decay operation performs gain adjustments.

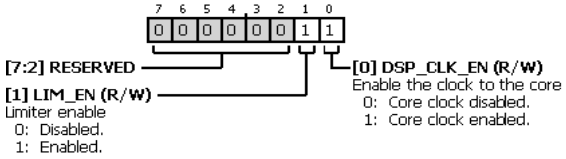



**Table 48. Bit Descriptions for CORE_ENABLE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:2] | RESERVED | | Reserved. | 0x0 | R/W |
| 1 | LIM_EN | | Limiter enable. When the limiter function is disabled, a fixed maximum gain setting is applied to instructions using the limiters. | 0x1 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 0 | DSP_CLK_EN | | Enable the clock to the core. This bit directly controls the clock to the core. Set this bit to 0 when the chip is used in a codec only configuration, in which the core is not used. Writing to any of the biquad coefficient registers (Parameter Memory Address 0x0E0 to Parameter Memory Address 0x2BF) is blocked until this bit is 1. Do not use this bit to start or stop the core while it is running, because it immediately starts or stops the core clock and does not allow the program to finish. Instead, use CORE_RUN in the CORE_CONTROL register to start or stop the core. | 0x1 | R/W |
| | | 0 | Core clock disabled. | | |
| | | 1 | Core clock enabled. | | |

## DB VALUE REGISTER 0 READ

**Address: 0x0C, Reset: 0x00, Name: DBREG0**

The core can write data to this register, and the data is automatically converted to a level in dB. The most common use for this register is to determine the rms value of a signal by taking the absolute value, and then performing low-pass filtering and moving the result to the DBREG0 register.

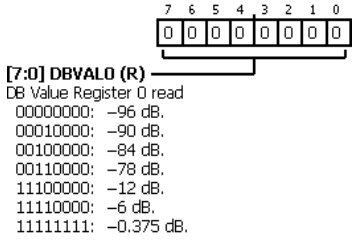



**Table 49. Bit Descriptions for DBREG0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | DBVAL0 | | DB Value Register 0 read. | 0x0 | R |
| | | 00000000 | −96 dB. | | |
| | | 00010000 | −90 dB. | | |
| | | 00100000 | −84 dB. | | |
| | | 00110000 | −78 dB. | | |
| | | 11100000 | −12 dB. | | |
| | | 11110000 | −6 dB. | | |
| | | 11111111 | −0.375 dB. | | |

## DB VALUE REGISTER 1 READ

**Address: 0x0D, Reset: 0x00, Name: DBREG1**

The core can write data to this register, and the data is automatically converted to a level in dB. The most common use for this register is to determine the rms value of a signal by taking the absolute value, and then performing low-pass filtering and moving the result to the DBREG1 register.

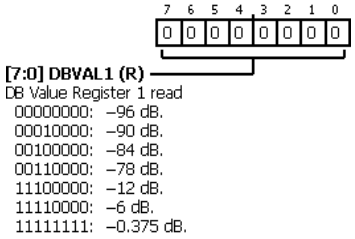



**Table 50. Bit Descriptions for DBREG1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | DBVAL1 | | DB Value Register 1 read. | 0x0 | R |
| | | 00000000 | −96 dB. | | |
| | | 00010000 | −90 dB. | | |
| | | 00100000 | −84 dB. | | |
| | | 00110000 | −78 dB. | | |
| | | 11100000 | −12 dB. | | |
| | | 11110000 | −6 dB. | | |
| | | 11111111 | −0.375 dB. | | |

## DB VALUE REGISTER 2 READ

**Address: 0x0E, Reset: 0x00, Name: DBREG2**

The core can write data to this register, and the data is automatically converted to a level in dB. The most common use for this register is to determine the rms value of a signal by taking the absolute value, and then performing low-pass filtering and moving the result to the DBREG2 register.

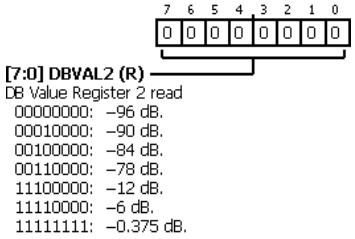



**Table 51. Bit Descriptions for DBREG2**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | DBVAL2 | | DB Value Register 2 read. | 0x0 | R |
| | | 00000000 | −96 dB. | | |
| | | 00010000 | −90 dB. | | |
| | | 00100000 | −84 dB. | | |
| | | 00110000 | −78 dB. | | |
| | | 11100000 | −12 dB. | | |
| | | 11110000 | −6 dB. | | |
| | | 11111111 | −0.375 dB. | | |

## CORE CHANNEL 0/CORE CHANNEL 1 INPUT SELECT REGISTER

**Address: 0x0F, Reset: 0x10, Name: CORE_IN_MUX_0_1**

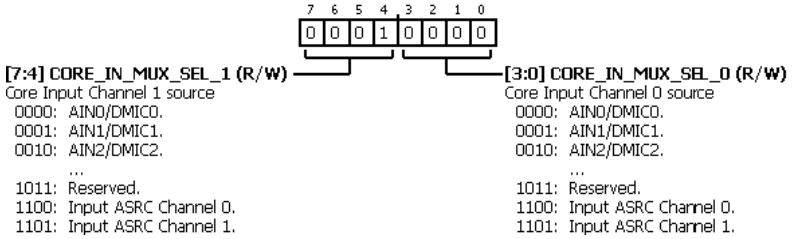



**Table 52. Bit Descriptions for CORE_IN_MUX_0_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | CORE_IN_MUX_SEL_1 | | Core Input Channel 1 source. | 0x1 | R/W |
| | | 0000 | AIN0/DMIC0. | | |
| | | 0001 | AIN1/DMIC1. | | |
| | | 0010 | AIN2/DMIC2. | | |
| | | 0011 | AIN3/DMIC3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |
| [3:0] | CORE_IN_MUX_SEL_0 | | Core Input Channel 0 source. | 0x0 | R/W |
| | | 0000 | AIN0/DMIC0. | | |
| | | 0001 | AIN1/DMIC1. | | |
| | | 0010 | AIN2/DMIC2. | | |
| | | 0011 | AIN3/DMIC3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |

## CORE CHANNEL 2/CORE CHANNEL 3 INPUT SELECT REGISTER

**Address: 0x10, Reset: 0x32, Name: CORE_IN_MUX_2_3**

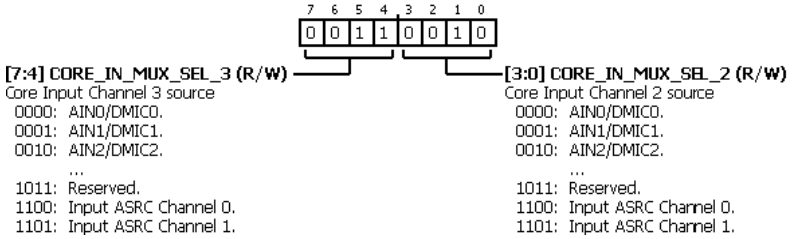



**Table 53. Bit Descriptions for CORE_IN_MUX_2_3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | CORE_IN_MUX_SEL_3 | | Core Input Channel 3 source. | 0x3 | R/W |
| | | 0000 | AIN0/DMIC0. | | |
| | | 0001 | AIN1/DMIC1. | | |
| | | 0010 | AIN2/DMIC2. | | |
| | | 0011 | AIN3/DMIC3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |
| [3:0] | CORE_IN_MUX_SEL_2 | | Core Input Channel 2 source. | 0x2 | R/W |
| | | 0000 | AIN0/DMIC0. | | |
| | | 0001 | AIN1/DMIC1. | | |
| | | 0010 | AIN2/DMIC2. | | |
| | | 0011 | AIN3/DMIC3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |

## DAC INPUT SELECT REGISTER

**Address: 0x11, Reset: 0x10, Name: DAC_SOURCE_0_1**

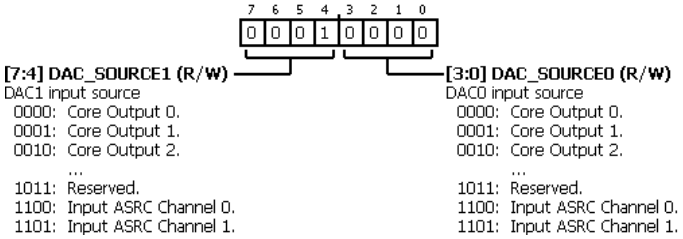



**Table 54. Bit Descriptions for DAC_SOURCE_0_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | DAC_SOURCE1 | | DAC1 input source. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x1 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |
| [3:0] | DAC_SOURCE0 | | DAC0 input source. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x0 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |

## PDM MODULATOR INPUT SELECT REGISTER

**Address: 0x12, Reset: 0x32, Name: PDM_SOURCE_0_1**

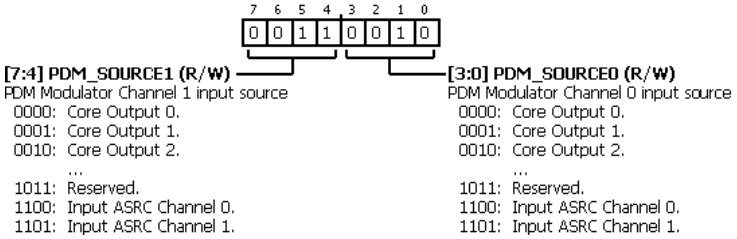



**Table 55. Bit Descriptions for PDM_SOURCE_0_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | PDM_SOURCE1 | | PDM Modulator Channel 1 input source. | 0x3 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |
| [3:0] | PDM_SOURCE0 | | PDM Modulator Channel 0 input source. | 0x2 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | Reserved. | | |
| | | 0101 | Reserved. | | |
| | | 0110 | Reserved. | | |
| | | 0111 | Reserved. | | |
| | | 1000 | Reserved. | | |
| | | 1001 | Reserved. | | |
| | | 1010 | Reserved. | | |
| | | 1011 | Reserved. | | |
| | | 1100 | Input ASRC Channel 0. | | |
| | | 1101 | Input ASRC Channel 1. | | |

## SERIAL DATA OUTPUT 0/SERIAL DATA OUTPUT 1 INPUT SELECT REGISTER

**Address: 0x13, Reset: 0x54, Name: SOUT_SOURCE_0_1**

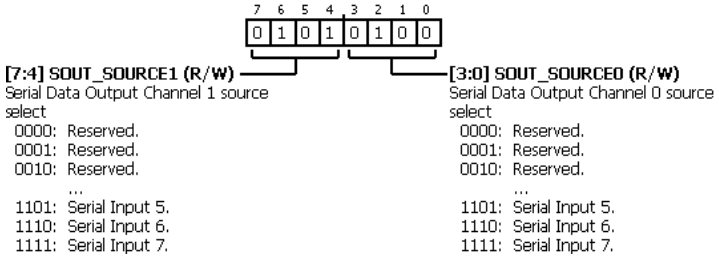



**Table 56. Bit Descriptions for SOUT_SOURCE_0_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | SOUT_SOURCE1 | | Serial Data Output Channel 1 source select. | 0x5 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |
| [3:0] | SOUT_SOURCE0 | | Serial Data Output Channel 0 source select. | 0x4 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |

## SERIAL DATA OUTPUT 2/SERIAL DATA OUTPUT 3 INPUT SELECT REGISTER

**Address: 0x14, Reset: 0x76, Name: SOUT_SOURCE_2_3**

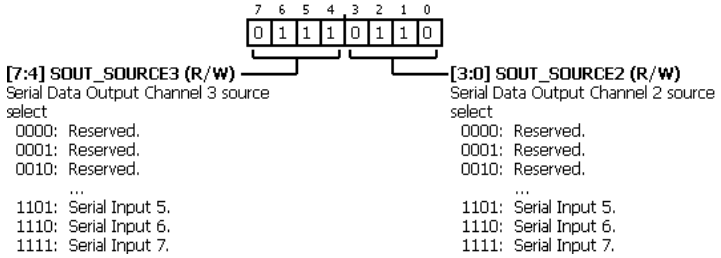



**Table 57. Bit Descriptions for SOUT_SOURCE_2_3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | SOUT_SOURCE3 | | Serial Data Output Channel 3 source select. | 0x7 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |
| [3:0] | SOUT_SOURCE2 | | Serial Data Output Channel 2 source select. | 0x6 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |

## SERIAL DATA OUTPUT 4/SERIAL DATA OUTPUT 5 INPUT SELECT REGISTER

**Address: 0x15, Reset: 0x54, Name: SOUT_SOURCE_4_5**

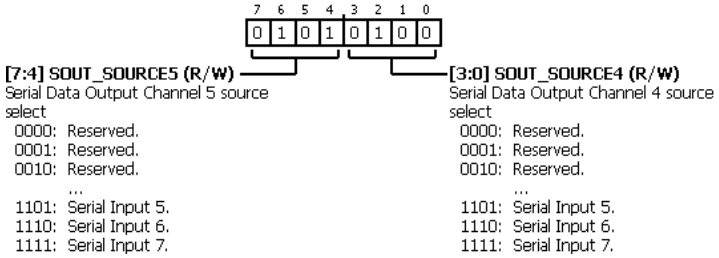



**Table 58. Bit Descriptions for SOUT_SOURCE_4_5**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | SOUT_SOURCE5 | | Serial Data Output Channel 5 source select. | 0x5 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |
| [3:0] | SOUT_SOURCE4 | | Serial Data Output Channel 4 source select. | 0x4 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |

## SERIAL DATA OUTPUT 6/SERIAL DATA OUTPUT 7 INPUT SELECT REGISTER

**Address: 0x16, Reset: 0x76, Name: SOUT_SOURCE_6_7**

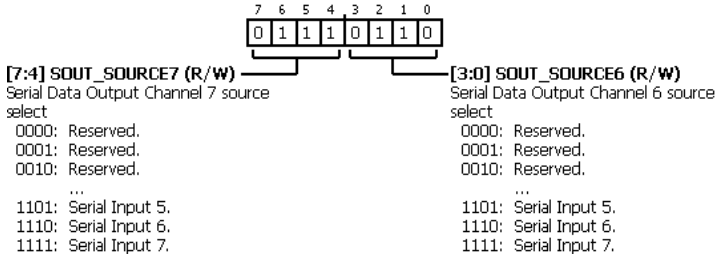



**Table 59. Bit Descriptions for SOUT_SOURCE_6_7**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | SOUT_SOURCE7 | | Serial Data Output Channel 7 source select. | 0x7 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |
| [3:0] | SOUT_SOURCE6 | | Serial Data Output Channel 6 source select. | 0x6 | R/W |
| | | 0000 | Reserved. | | |
| | | 0001 | Reserved. | | |
| | | 0010 | Reserved. | | |
| | | 0011 | Reserved. | | |
| | | 0100 | Output ASRC Channel 0. | | |
| | | 0101 | Output ASRC Channel 1. | | |
| | | 0110 | Output ASRC Channel 2. | | |
| | | 0111 | Output ASRC Channel 3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |

## ADC_SDATA0/ADC_SDATA1 CHANNEL SELECT REGISTER

**Address: 0x17, Reset: 0x04, Name: ADC_SDATA_CH**

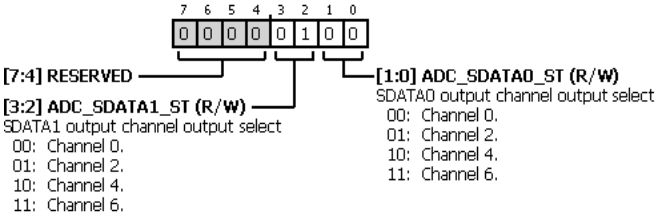



**Table 60. Bit Descriptions for ADC_SDATA_CH**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | RESERVED | | Reserved. | 0x0 | R/W |
| [3:2] | ADC_SDATA1_ST | | SDATA1 output channel output select. These bits select the output channel at which ADC_SDATA1 starts to output data. The output port sequentially outputs data following this start channel according to the setting of Bit SAI. | 0x1 | R/W |
| | | 00 | Channel 0. | | |
| | | 01 | Channel 2. | | |
| | | 10 | Channel 4. | | |
| | | 11 | Channel 6. | | |
| [1:0] | ADC_SDATA0_ST | | SDATA0 output channel output select. These bits select the output channel at which ADC_SDATA0 starts to output data. The output port sequentially outputs data following this start channel according to the setting of Bit SAI. | 0x0 | R/W |
| | | 00 | Channel 0. | | |
| | | 01 | Channel 2. | | |
| | | 10 | Channel 4. | | |
| | | 11 | Channel 6. | | |

## OUTPUT ASRC0/OUTPUT ASRC1 SOURCE REGISTER

**Address: 0x18, Reset: 0x10, Name: ASRCO_SOURCE_0_1**

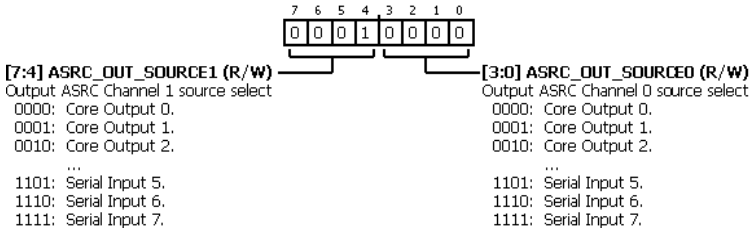



**Table 61. Bit Descriptions for ASRCO_SOURCE_0_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | ASRC_OUT_SOURCE1 | | Output ASRC Channel 1 source select. | 0x1 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | ADC0. | | |
| | | 0101 | ADC1. | | |
| | | 0110 | ADC2. | | |
| | | 0111 | ADC3. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |
| [3:0] | ASRC_OUT_SOURCE0 | | Output ASRC Channel 0 source select. | 0x0 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | ADC0. | | |
| | | 0101 | ADC1. | | |
| | | 0110 | ADC2. | | |
| | | 0111 | ADC3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |

## OUTPUT ASRC2/OUTPUT ASRC3 SOURCE REGISTER

**Address: 0x19, Reset: 0x32, Name: ASRCO_SOURCE_2_3**

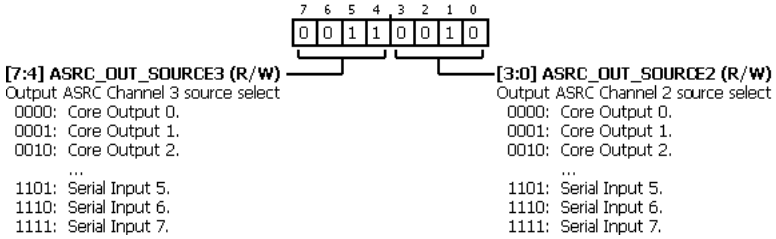



**Table 62. Bit Descriptions for ASRCO_SOURCE_2_3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | ASRC_OUT_SOURCE3 | | Output ASRC Channel 3 source select. | 0x3 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | ADC0. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 0101 | ADC1. | | |
| | | 0110 | ADC2. | | |
| | | 0111 | ADC3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |
| [3:0] | ASRC_OUT_SOURCE2 | | Output ASRC Channel 2 source select. | 0x2 | R/W |
| | | 0000 | Core Output 0. | | |
| | | 0001 | Core Output 1. | | |
| | | 0010 | Core Output 2. | | |
| | | 0011 | Core Output 3. | | |
| | | 0100 | ADC0. | | |
| | | 0101 | ADC1. | | |
| | | 0110 | ADC2. | | |
| | | 0111 | ADC3. | | |
| | | 1000 | Serial Input 0. | | |
| | | 1001 | Serial Input 1. | | |
| | | 1010 | Serial Input 2. | | |
| | | 1011 | Serial Input 3. | | |
| | | 1100 | Serial Input 4. | | |
| | | 1101 | Serial Input 5. | | |
| | | 1110 | Serial Input 6. | | |
| | | 1111 | Serial Input 7. | | |

## INPUT ASRC CHANNEL SELECT REGISTER

**Address: 0x1A, Reset: 0x00, Name: ASRC_MODE**

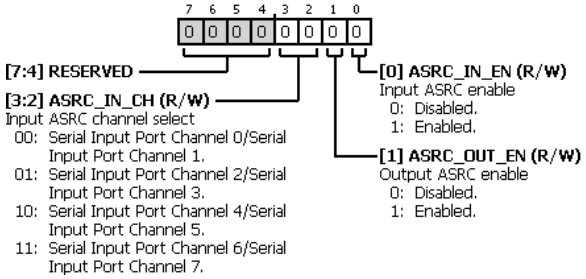


**Table 63. Bit Descriptions for ASRC_MODE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | RESERVED | | Reserved. | 0x0 | R/W |
| [3:2] | ASRC_IN_CH | | Input ASRC channel select. | 0x0 | R/W |
| | | 00 | Serial Input Port Channel 0/Serial Input Port Channel 1. | | |
| | | 01 | Serial Input Port Channel 2/Serial Input Port Channel 3. | | |
| | | 10 | Serial Input Port Channel 4/Serial Input Port Channel 5. | | |
| | | 11 | Serial Input Port Channel 6/Serial Input Port Channel 7. | | |
| 1 | ASRC_OUT_EN | | Output ASRC enable. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 0 | ASRC_IN_EN | | Input ASRC enable. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |

## ADC0/ADC1 CONTROL 0 REGISTER

**Address: 0x1B, Reset: 0x19, Name: ADC_CONTROL0**

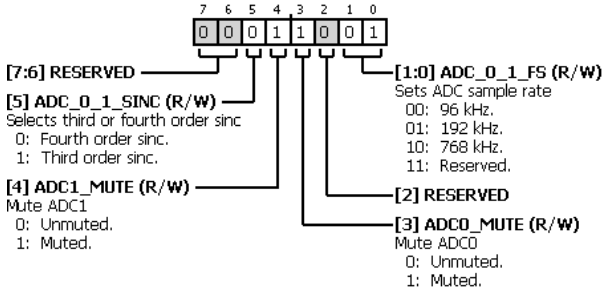



**Table 64. Bit Descriptions for ADC_CONTROL0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | ADC_0_1_SINC | | Selects third- or fourth-order sinc. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x0 | R/W |
| | | 0 | Fourth-order sinc. | | |
| | | 1 | Third-order sinc. | | |
| 4 | ADC1_MUTE | | Mute ADC1. Muting is accomplished by setting the volume control to maximum attenuation. This bit has no effect if volume control is bypassed. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| 3 | ADC0_MUTE | | Mute ADC0. Muting is accomplished by setting the volume control to maximum attenuation. This bit has no effect if volume control is bypassed. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| 2 | RESERVED | | Reserved. | 0x0 | R/W |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [1:0] | ADC_0_1_FS | | Sets ADC sample rate. The settings of these bits must be consistent with the settings of the FAST_ SLOW_RATE bits, and CORE_RUN must be set to 0 for this setting to be updated. | 0x1 | R/W |
| | | 00 | 96 kHz. | | |
| | | 01 | 192 kHz. | | |
| | | 10 | 768 kHz. | | |
| | | 11 | Reserved. | | |

## ADC2/ADC3 CONTROL 0 REGISTER

**Address: 0x1C, Reset: 0x19, Name: ADC_CONTROL1**

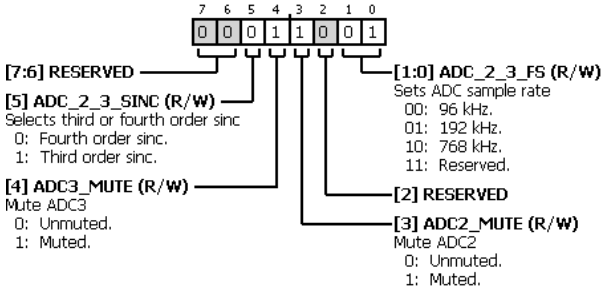



**Table 65. Bit Descriptions for ADC_CONTROL1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | ADC_2_3_SINC | | Selects third- or fourth-order sinc. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x0 | R/W |
| | | 0 | Fourth-order sinc. | | |
| | | 1 | Third-order sinc. | | |
| 4 | ADC3_MUTE | | Mute ADC3. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| 3 | ADC2_MUTE | | Mute ADC2. Muting is accomplished by setting the volume control to maximum attenuation. This bit has no effect if volume control is bypassed. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| 2 | RESERVED | | Reserved. | 0x0 | R/W |
| [1:0] | ADC_2_3_FS | | Sets ADC sample rate. The settings of these bits must be consistent with the settings of the FAST_ SLOW_RATE bits, and CORE_RUN must be set to 0 for this setting to be updated. | 0x1 | R/W |
| | | 00 | 96 kHz. | | |
| | | 01 | 192 kHz. | | |
| | | 10 | 768 kHz. | | |
| | | 11 | Reserved. | | |

## ADC0/ADC1 CONTROL 1 REGISTER

**Address: 0x1D, Reset: 0x00, Name: ADC_CONTROL2**

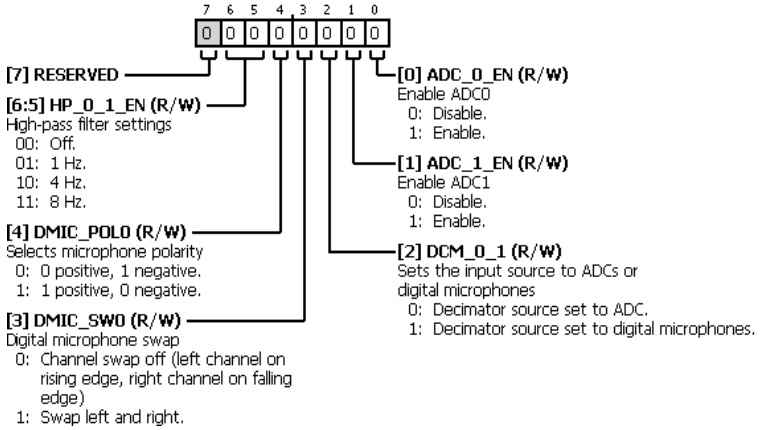



**Table 66. Bit Descriptions for ADC_CONTROL2**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| [6:5] | HP_0_1_EN | | High-pass filter settings. | 0x0 | R/W |
| | | 00 | Off. | | |
| | | 01 | 1 Hz. | | |
| | | 10 | 4 Hz. | | |
| | | 11 | 8 Hz. | | |
| 4 | DMIC_POL0 | | Selects microphone polarity. | 0x0 | R/W |
| | | 0 | 0 positive, 1 negative. | | |
| | | 1 | 1 positive, 0 negative. | | |
| 3 | DMIC_SW0 | | Digital microphone swap. | 0x0 | R/W |
| | | 0 | Channel swap off (left channel on rising edge, right channel on falling edge). | | |
| | | 1 | Swap left and right. | | |
| 2 | DCM_0_1 | | Sets the input source to ADCs or digital microphones. | 0x0 | R/W |
| | | 0 | Decimator source set to ADC. | | |
| | | 1 | Decimator source set to digital microphones. | | |
| 1 | ADC_1_EN | | Enable ADC1. This bit must be set in conjunction with the SINC_1_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. | 0x0 | R/W |
| | | 0 | Disable. | | |
| | | 1 | Enable. | | |
| 0 | ADC_0_EN | | Enable ADC0. This bit must be set in conjunction with the SINC_0_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. | 0x0 | R/W |
| | | 0 | Disable. | | |
| | | 1 | Enable. | | |

## ADC2/ADC3 CONTROL 1 REGISTER

**Address: 0x1E, Reset: 0x00, Name: ADC_CONTROL3**

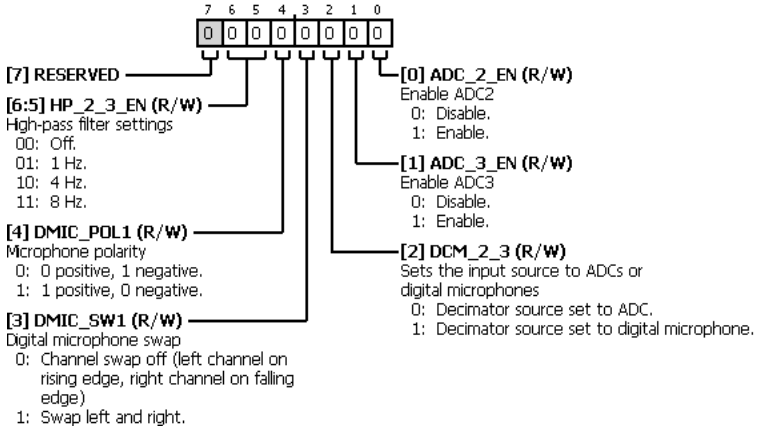



**Table 67. Bit Descriptions for ADC_CONTROL3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| [6:5] | HP_2_3_EN | | High-pass filter settings. | 0x0 | R/W |
| | | 00 | Off. | | |
| | | 01 | 1 Hz. | | |
| | | 10 | 4 Hz. | | |
| | | 11 | 8 Hz. | | |
| 4 | DMIC_POL1 | | Microphone polarity. | 0x0 | R/W |
| | | 0 | 0 positive, 1 negative. | | |
| | | 1 | 1 positive, 0 negative. | | |
| 3 | DMIC_SW1 | | Digital microphone swap. | 0x0 | R/W |
| | | 0 | Channel swap off (left channel on rising edge, right channel on falling edge). | | |
| | | 1 | Swap left and right. | | |
| 2 | DCM_2_3 | | Sets the input source to ADCs or digital microphones. | 0x0 | R/W |
| | | 0 | Decimator source set to ADC. | | |
| | | 1 | Decimator source set to digital microphone. | | |
| 1 | ADC_3_EN | | Enable ADC3. This bit must be set in conjunction with the SINC_3_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. | 0x0 | R/W |
| | | 0 | Disable. | | |
| | | 1 | Enable. | | |
| 0 | ADC_2_EN | | Enable ADC2. This bit must be set in conjunction with the SINC_2_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. | 0x0 | R/W |
| | | 0 | Disable. | | |
| | | 1 | Enable. | | |

## ADC0 VOLUME CONTROL REGISTER

**Address: 0x1F, Reset: 0x00, Name: ADC0_VOLUME**

When SINC_0_EN is set, the volume starts to ramp from −95.625 dB to the value in this register. The volume ramp time is (number of steps) × 16/$f_S$, where there are 256 steps between 0 dB and −95.625 dB. For example, with $f_S$ = 192 kHz, the volume ramps from −95.625 dB to 0 dB in 21 ms.

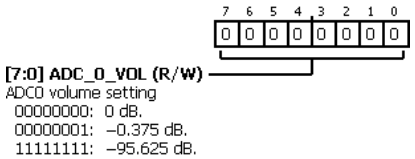



**Table 68. Bit Descriptions for ADC0_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | ADC_0_VOL | | ADC0 volume setting. | 0x0 | R/W |
| | | 00000000 | 0 dB. | | |
| | | 00000001 | −0.375 dB. | | |
| | | 11111111 | −95.625 dB. | | |

## ADC1 VOLUME CONTROL REGISTER

**Address: 0x20, Reset: 0x00, Name: ADC1_VOLUME**

When SINC_1_EN is set, the volume starts to ramp from −95.625 dB to the value in this register. The volume ramp time is (number of steps) × 16/$f_S$, where there are 256 steps between 0 dB and −95.625 dB. For example, with $f_S$ = 192 kHz, the volume ramps from −95.625 dB to 0 dB in 21 ms.

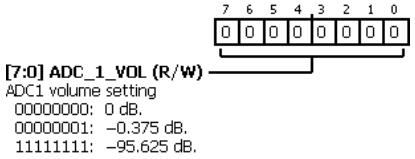



**Table 69. Bit Descriptions for ADC1_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | ADC_1_VOL | | ADC1 volume setting. | 0x0 | R/W |
| | | 00000000 | 0 dB. | | |
| | | 00000001 | −0.375 dB. | | |
| | | 11111111 | −95.625 dB. | | |

## ADC2 VOLUME CONTROL REGISTER

**Address: 0x21, Reset: 0x00, Name: ADC2_VOLUME**

When SINC_2_EN is set, the volume starts to ramp from −95.625 dB to the value in this register. The volume ramp time is (number of steps) × 16/$f_S$, where there are 256 steps between 0 dB and −95.625 dB. For example, with $f_S$ = 192 kHz, the volume ramps from −95.625 dB to 0 dB in 21 ms.

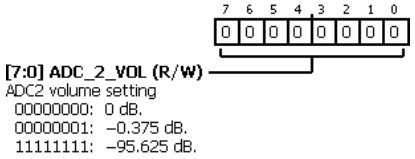



**Table 70. Bit Descriptions for ADC2_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | ADC_2_VOL | | ADC2 volume setting. | 0x0 | R/W |
| | | 00000000 | 0 dB. | | |
| | | 00000001 | −0.375 dB. | | |
| | | 11111111 | −95.625 dB. | | |

## ADC3 VOLUME CONTROL REGISTER

**Address: 0x22, Reset: 0x00, Name: ADC3_VOLUME**

When SINC_3_EN is set, the volume starts to ramp from −95.625 dB to the value in this register. The volume ramp time is (number of steps) × 16/$f_S$, where there are 256 steps between 0 dB and −95.625 dB. For example, with $f_S$ = 192 kHz, the volume ramps from −95.625 dB to 0 dB in 21 ms.

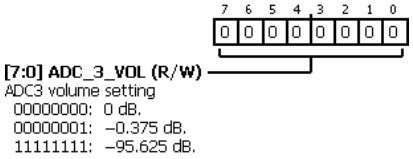



**Table 71. Bit Descriptions for ADC3_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | ADC_3_VOL | | ADC3 volume setting. | 0x0 | R/W |
| | | 00000000 | 0 dB. | | |
| | | 00000001 | −0.375 dB. | | |
| | | 11111111 | −95.625 dB. | | |

## PGA CONTROL 0 REGISTER

**Address: 0x23, Reset: 0x40, Name: PGA_CONTROL_0**

This register controls the PGA connected to AIN0.

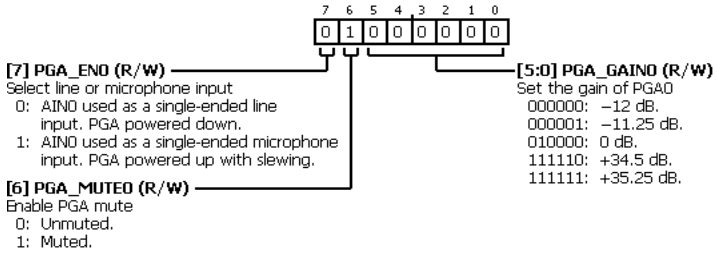



**Table 72. Bit Descriptions for PGA_CONTROL_0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | PGA_EN0 | | Select line or microphone input. Note that the PGA inverts the signal going through it. | 0x0 | R/W |
| | | 0 | AIN0 used as a single-ended line input. PGA powered down. | | |
| | | 1 | AIN0 used as a single-ended microphone input. PGA powered up with slewing. | | |
| 6 | PGA_MUTE0 | | Enable PGA mute. When PGA is muted, PGA_GAIN0 is ignored. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| [5:0] | PGA_GAIN0 | | Set the gain of PGA0. | 0x0 | R/W |
| | | 000000 | −12 dB. | | |
| | | 000001 | −11.25 dB. | | |
| | | 010000 | 0 dB. | | |
| | | 111110 | +34.5 dB. | | |
| | | 111111 | +35.25 dB. | | |

## PGA CONTROL 1 REGISTER

**Address: 0x24, Reset: 0x40, Name: PGA_CONTROL_1**

This register controls the PGA connected to AIN1.

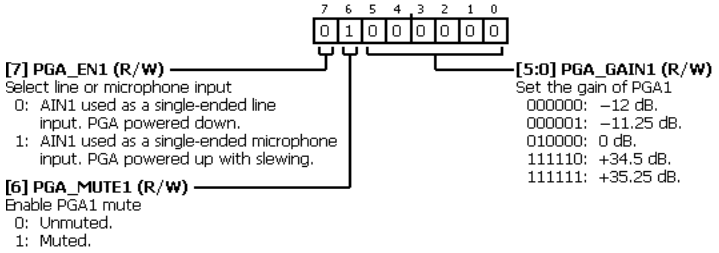



**Table 73. Bit Descriptions for PGA_CONTROL_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | PGA_EN1 | | Select line or microphone input. Note that the PGA inverts the signal going through it. | 0x0 | R/W |
| | | 0 | AIN1 used as a single-ended line input. PGA powered down. | | |
| | | 1 | AIN1 used as a single-ended microphone input. PGA powered up with slewing. | | |
| 6 | PGA_MUTE1 | | Enable PGA1 mute. When PGA is muted, PGA_GAIN1 is ignored. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| [5:0] | PGA_GAIN1 | | Set the gain of PGA1. | 0x0 | R/W |
| | | 000000 | −12 dB. | | |
| | | 000001 | −11.25 dB. | | |
| | | 010000 | 0 dB. | | |
| | | 111110 | +34.5 dB. | | |
| | | 111111 | +35.25 dB. | | |

## PGA CONTROL 2 REGISTER

**Address: 0x25, Reset: 0x40, Name: PGA_CONTROL_2**

This register controls the PGA connected to AIN2.

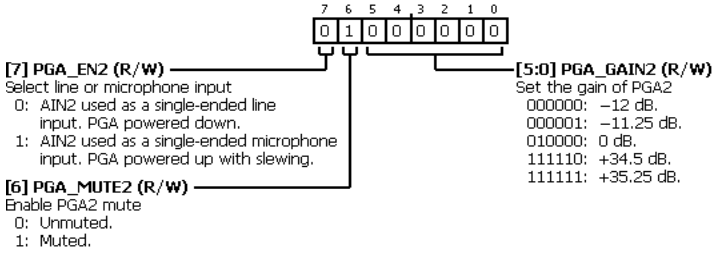



**Table 74. Bit Descriptions for PGA_CONTROL_2**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | PGA_EN2 | | Select line or microphone input. Note that the PGA inverts the signal going through it. | 0x0 | R/W |
| | | 0 | AIN2 used as a single-ended line input. PGA powered down. | | |
| | | 1 | AIN2 used as a single-ended microphone input. PGA powered up with slewing. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 6 | PGA_MUTE2 | | Enable PGA2 mute. When PGA is muted, PGA_GAIN2 is ignored. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| [5:0] | PGA_GAIN2 | | Set the gain of PGA2. | 0x0 | R/W |
| | | 000000 | −12 dB. | | |
| | | 000001 | −11.25 dB. | | |
| | | 010000 | 0 dB. | | |
| | | 111110 | +34.5 dB. | | |
| | | 111111 | +35.25 dB. | | |

## PGA CONTROL 3 REGISTER

**Address: 0x26, Reset: 0x40, Name: PGA_CONTROL_3**

This register controls the PGA connected to AIN3.

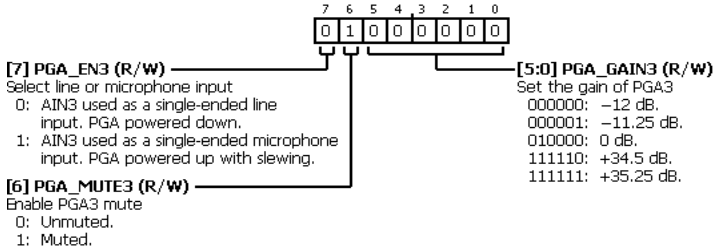



**Table 75. Bit Descriptions for PGA_CONTROL_3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | PGA_EN3 | | Select line or microphone input. Note that the PGA inverts the signal going through it. | 0x0 | R/W |
| | | 0 | AIN3 used as a single-ended line input. PGA powered down. | | |
| | | 1 | AIN3 used as a single-ended microphone input. PGA powered up with slewing. | | |
| 6 | PGA_MUTE3 | | Enable PGA3 mute. When PGA is muted, PGA_GAIN3 is ignored. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| [5:0] | PGA_GAIN3 | | Set the gain of PGA3. | 0x0 | R/W |
| | | 000000 | −12 dB. | | |
| | | 000001 | −11.25 dB. | | |
| | | 010000 | 0 dB. | | |
| | | 111110 | +34.5 dB. | | |
| | | 111111 | +35.25 dB. | | |

## PGA SLEW CONTROL REGISTER

**Address: 0x27, Reset: 0x00, Name: PGA_STEP_CONTROL**

If PGA slew is disabled with the SLEW_PDx controls, the SLEW_RATE parameter is ignored for that PGA block.

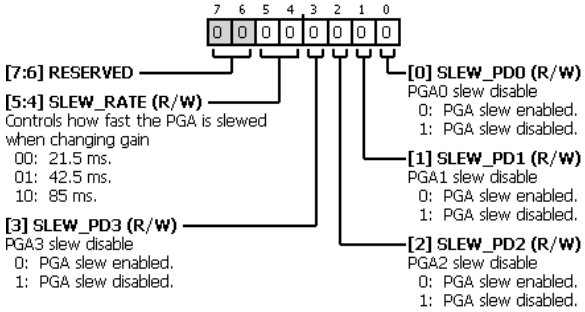



**Table 76. Bit Descriptions for PGA_STEP_CONTROL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| [5:4] | SLEW_RATE | | Controls how fast the PGA is slewed when changing gain. | 0x0 | R/W |
| | | 00 | 21.5 ms. | | |
| | | 01 | 42.5 ms. | | |
| | | 10 | 85 ms. | | |
| 3 | SLEW_PD3 | | PGA3 slew disable. | 0x0 | R/W |
| | | 0 | PGA slew enabled. | | |
| | | 1 | PGA slew disabled. | | |
| 2 | SLEW_PD2 | | PGA2 slew disable. | 0x0 | R/W |
| | | 0 | PGA slew enabled. | | |
| | | 1 | PGA slew disabled. | | |
| 1 | SLEW_PD1 | | PGA1 slew disable. | 0x0 | R/W |
| | | 0 | PGA slew enabled. | | |
| | | 1 | PGA slew disabled. | | |
| 0 | SLEW_PD0 | | PGA0 slew disable. | 0x0 | R/W |
| | | 0 | PGA slew enabled. | | |
| | | 1 | PGA slew disabled. | | |

## PGA 10 DB GAIN BOOST REGISTER

**Address: 0x28, Reset: 0x00, Name: PGA_10DB_BOOST**

Each PGA can have an additional +10 dB gain added, making the PGA gain range −2 dB to +46 dB.

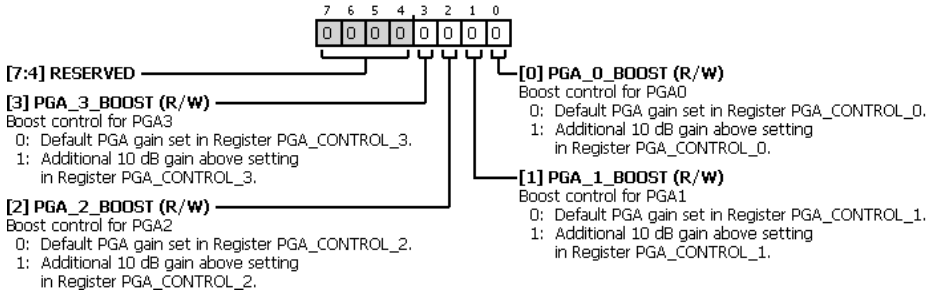


**Table 77. Bit Descriptions for PGA_10DB_BOOST**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | RESERVED | | Reserved. | 0x0 | R/W |
| 3 | PGA_3_BOOST | | Boost control for PGA3. | 0x0 | R/W |
| | | 0 | Default PGA gain set in Register PGA_CONTROL_3. | | |
| | | 1 | Additional 10 dB gain above setting in Register PGA_CONTROL_3. | | |
| 2 | PGA_2_BOOST | | Boost control for PGA2. | 0x0 | R/W |
| | | 0 | Default PGA gain set in Register PGA_CONTROL_2. | | |
| | | 1 | Additional 10 dB gain above setting in Register PGA_CONTROL_2. | | |
| 1 | PGA_1_BOOST | | Boost control for PGA1. | 0x0 | R/W |
| | | 0 | Default PGA gain set in Register PGA_CONTROL_1. | | |
| | | 1 | Additional 10 dB gain above setting in Register PGA_CONTROL_1. | | |
| 0 | PGA_0_BOOST | | Boost control for PGA0. | 0x0 | R/W |
| | | 0 | Default PGA gain set in Register PGA_CONTROL_0. | | |
| | | 1 | Additional 10 dB gain above setting in Register PGA_CONTROL_0. | | |

## INPUT AND OUTPUT CAPACITOR CHARGING REGISTER

**Address: 0x29, Reset: 0x3F, Name: POP_SUPPRESS**

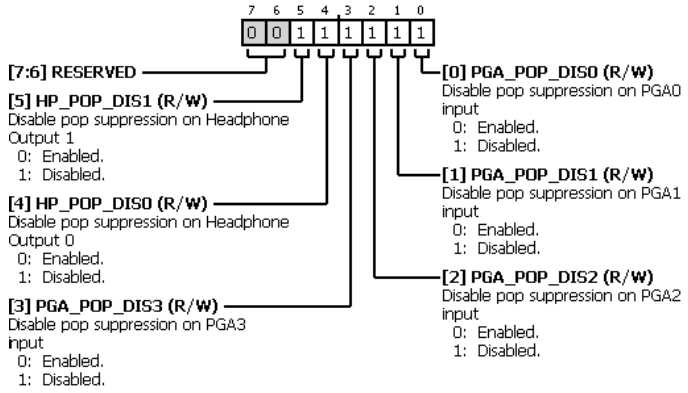



**Table 78. Bit Descriptions for POP_SUPPRESS**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | HP_POP_DIS1 | | Disable pop suppression on Headphone Output 1. | 0x1 | R/W |
| | | 0 | Enabled. | | |
| | | 1 | Disabled. | | |
| 4 | HP_POP_DIS0 | | Disable pop suppression on Headphone Output 0. | 0x1 | R/W |
| | | 0 | Enabled. | | |
| | | 1 | Disabled. | | |
| 3 | PGA_POP_DIS3 | | Disable pop suppression on PGA3 input. | 0x1 | R/W |
| | | 0 | Enabled. | | |
| | | 1 | Disabled. | | |
| 2 | PGA_POP_DIS2 | | Disable pop suppression on PGA2 input. | 0x1 | R/W |
| | | 0 | Enabled. | | |
| | | 1 | Disabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 1 | PGA_POP_DIS1 | | Disable pop suppression on PGA1 input. | 0x1 | R/W |
| | | 0 | Enabled. | | |
| | | 1 | Disabled. | | |
| 0 | PGA_POP_DIS0 | | Disable pop suppression on PGA0 input. | 0x1 | R/W |
| | | 0 | Enabled. | | |
| | | 1 | Disabled. | | |

## DSP BYPASS PATH REGISTER

**Address: 0x2A, Reset: 0x00, Name: TALKTHRU**

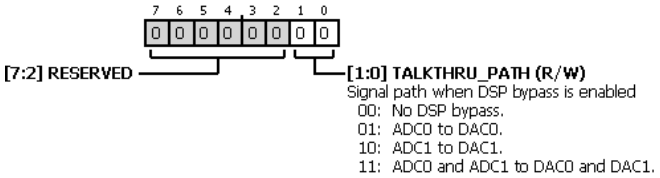



**Table 79. Bit Descriptions for TALKTHRU**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:2] | RESERVED | | Reserved. | 0x0 | R/W |
| [1:0] | TALKTHRU_PATH | | Signal path when DSP bypass is enabled. | 0x0 | R/W |
| | | 00 | No DSP bypass. | | |
| | | 01 | ADC0 to DAC0. | | |
| | | 10 | ADC1 to DAC1. | | |
| | | 11 | ADC0 and ADC1 to DAC0 and DAC1. | | |

## DSP BYPASS GAIN FOR PGA0 REGISTER

**Address: 0x2B, Reset: 0x00, Name: TALKTHRU_GAIN0**

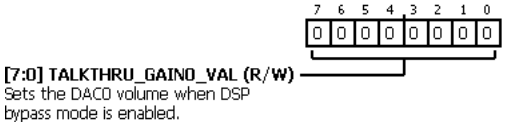



**Table 80. Bit Descriptions for TALKTHRU_GAIN0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | TALKTHRU_GAIN0_VAL | | Sets the DAC0 volume when DSP bypass mode is enabled. | 0x0 | R/W |

## DSP BYPASS GAIN FOR PGA1 REGISTER

**Address: 0x2C, Reset: 0x00, Name: TALKTHRU_GAIN1**

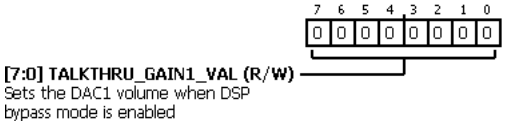



**Table 81. Bit Descriptions for TALKTHRU_GAIN1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | TALKTHRU_GAIN1_VAL | | Sets the DAC1 volume when DSP bypass mode is enabled. | 0x0 | R/W |

## MICBIAS0_1 CONTROL REGISTER

**Address: 0x2D, Reset: 0x00, Name: MIC_BIAS**

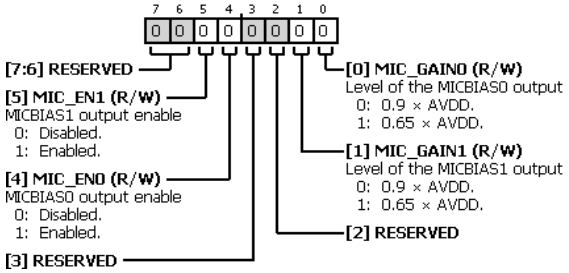



**Table 82. Bit Descriptions for MIC_BIAS**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | MIC_EN1 | | MICBIAS1 output enable. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 4 | MIC_EN0 | | MICBIAS0 output enable. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| 3 | RESERVED | | Reserved. | 0x0 | R/W |
| 2 | RESERVED | | Reserved. | 0x0 | R/W |
| 1 | MIC_GAIN1 | | Level of the MICBIAS1 output. | 0x0 | R/W |
| | | 0 | 0.9 × AVDD. | | |
| | | 1 | 0.65 × AVDD. | | |
| 0 | MIC_GAIN0 | | Level of the MICBIAS0 output. | 0x0 | R/W |
| | | 0 | 0.9 × AVDD. | | |
| | | 1 | 0.65 × AVDD. | | |

## DAC CONTROL REGISTER

**Address: 0x2E, Reset: 0x18, Name: DAC_CONTROL1**

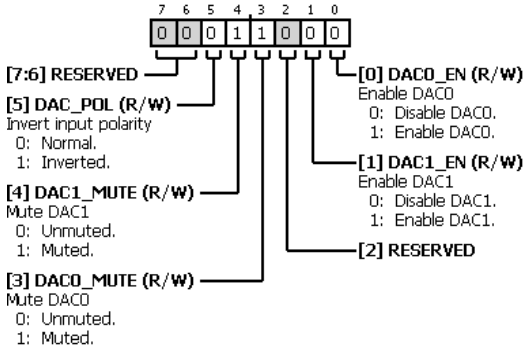



**Table 83. Bit Descriptions for DAC_CONTROL1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 5 | DAC_POL | | Invert input polarity. | 0x0 | R/W |
| | | 0 | Normal. | | |
| | | 1 | Inverted. | | |
| 4 | DAC1_MUTE | | Mute DAC1. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| 3 | DAC0_MUTE | | Mute DAC0. | 0x1 | R/W |
| | | 0 | Unmuted. | | |
| | | 1 | Muted. | | |
| 2 | RESERVED | | Reserved. | 0x0 | R/W |
| 1 | DAC1_EN | | Enable DAC1. | 0x0 | R/W |
| | | 0 | Disable DAC1. | | |
| | | 1 | Enable DAC1. | | |
| 0 | DAC0_EN | | Enable DAC0. | 0x0 | R/W |
| | | 0 | Disable DAC0. | | |
| | | 1 | Enable DAC0. | | |

## DAC0 VOLUME CONTROL REGISTER

**Address: 0x2F, Reset: 0x00, Name: DAC0_VOLUME**

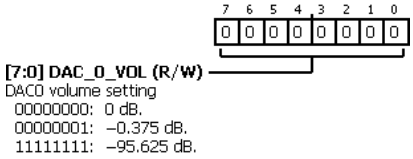



**Table 84. Bit Descriptions for DAC0_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | DAC_0_VOL | | DAC0 volume setting. | 0x0 | R/W |
| | | 00000000 | 0 dB. | | |
| | | 00000001 | −0.375 dB. | | |
| | | 11111111 | −95.625 dB. | | |

## DAC1 VOLUME CONTROL REGISTER

**Address: 0x30, Reset: 0x00, Name: DAC1_VOLUME**

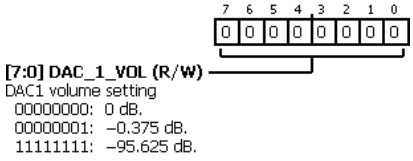


**Table 85. Bit Descriptions for DAC1_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | DAC_1_VOL | | DAC1 volume setting. | 0x0 | R/W |
| | | 00000000 | 0 dB. | | |
| | | 00000001 | −0.375 dB. | | |
| | | 11111111 | −95.625 dB. | | |

## HEADPHONE OUTPUT MUTES REGISTER

**Address: 0x31, Reset: 0x0F, Name: OP_STAGE_MUTES**

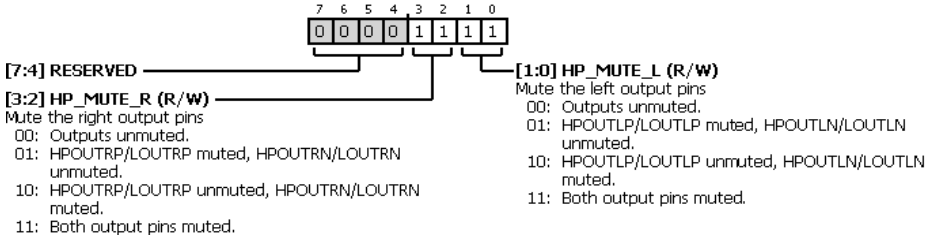



**Table 86. Bit Descriptions for OP_STAGE_MUTES**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | RESERVED | | Reserved. | 0x0 | R/W |
| [3:2] | HP_MUTE_R | | Mute the right output pins. When a pin is muted, it can be used as a common-mode output. | 0x3 | R/W |
| | | 00 | Outputs unmuted. | | |
| | | 01 | HPOUTRP/LOUTRP muted, HPOUTRN/LOUTRN unmuted. | | |
| | | 10 | HPOUTRP/LOUTRP unmuted, HPOUTRN/LOUTRN muted. | | |
| | | 11 | Both output pins muted. | | |
| [1:0] | HP_MUTE_L | | Mute the left output pins. When a pin is muted, it can be used as a common-mode output. | 0x3 | R/W |
| | | 00 | Outputs unmuted. | | |
| | | 01 | HPOUTLP/LOUTLP muted, HPOUTLN/LOUTLN unmuted. | | |
| | | 10 | HPOUTLP/LOUTLP unmuted, HPOUTLN/LOUTLN muted. | | |
| | | 11 | Both output pins muted. | | |

## SERIAL PORT CONTROL 0 REGISTER

**Address: 0x32, Reset: 0x00, Name: SAI_0**

Using 16-bit serial input/output limits device performance.

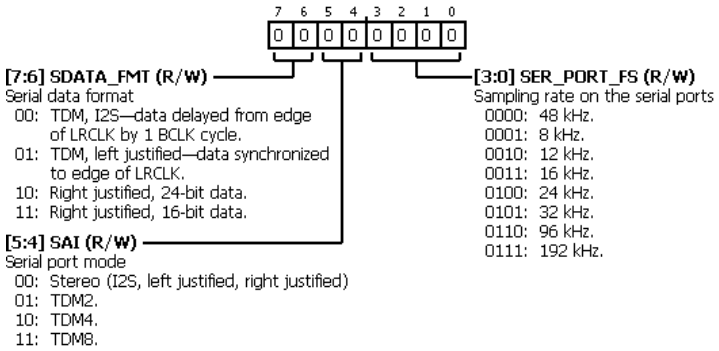


**Table 87. Bit Descriptions for SAI_0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | SDATA_FMT | | Serial data format. | 0x0 | R/W |
| | | 00 | TDM, I²S—data delayed from edge of LRCLK by 1 BCLK cycle. | | |
| | | 01 | TDM, left justified—data synchronized to edge of LRCLK. | | |
| | | 10 | Right justified, 24-bit data. | | |
| | | 11 | Right justified, 16-bit data. | | |
| [5:4] | SAI | | Serial port mode. | 0x0 | R/W |
| | | 00 | Stereo (I²S, left justified, right justified). | | |
| | | 01 | TDM2. | | |
| | | 10 | TDM4. | | |
| | | 11 | TDM8. | | |
| [3:0] | SER_PORT_FS | | Sampling rate on the serial ports. | 0x0 | R/W |
| | | 0000 | 48 kHz. | | |
| | | 0001 | 8 kHz. | | |
| | | 0010 | 12 kHz. | | |
| | | 0011 | 16 kHz. | | |
| | | 0100 | 24 kHz. | | |
| | | 0101 | 32 kHz. | | |
| | | 0110 | 96 kHz. | | |
| | | 0111 | 192 kHz. | | |

## SERIAL PORT CONTROL 1 REGISTER

**Address: 0x33, Reset: 0x00, Name: SAI_1**

Using 16-bit serial input/output limits device performance.

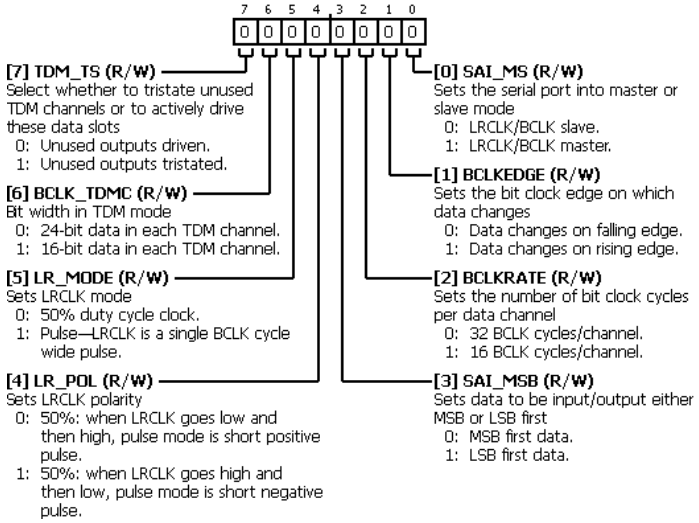



**Table 88. Bit Descriptions for SAI_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | TDM_TS | | Select whether to tristate unused TDM channels or to actively drive these data slots. | 0x0 | R/W |
| | | 0 | Unused outputs driven. | | |
| | | 1 | Unused outputs tristated. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 6 | BCLK_TDMC | | Bit width in TDM mode. | 0x0 | R/W |
| | | 0 | 24-bit data in each TDM channel. | | |
| | | 1 | 16-bit data in each TDM channel. | | |
| 5 | LR_MODE | | Sets LRCLK mode. | 0x0 | R/W |
| | | 0 | 50% duty cycle clock. | | |
| | | 1 | Pulse—LRCLK is a single BCLK cycle wide pulse. | | |
| 4 | LR_POL | | Sets LRCLK polarity. | 0x0 | R/W |
| | | 0 | 50%: when LRCLK goes low and then high, pulse mode is short positive pulse. | | |
| | | 1 | 50%: when LRCLK goes high and then low, pulse mode is short negative pulse. | | |
| 3 | SAI_MSB | | Sets data to be input/output either MSB or LSB first. | 0x0 | R/W |
| | | 0 | MSB first data. | | |
| | | 1 | LSB first data. | | |
| 2 | BCLKRATE | | Sets the number of bit clock cycles per data channel. | 0x0 | R/W |
| | | 0 | 32 BCLK cycles/channel. | | |
| | | 1 | 16 BCLK cycles/channel. | | |
| 1 | BCLKEDGE | | Sets the bit clock edge on which data changes. | 0x0 | R/W |
| | | 0 | Data changes on falling edge. | | |
| | | 1 | Data changes on rising edge. | | |
| 0 | SAI_MS | | Sets the serial port into master or slave mode. | 0x0 | R/W |
| | | 0 | LRCLK/BCLK slave. | | |
| | | 1 | LRCLK/BCLK master. | | |

## TDM OUTPUT CHANNEL DISABLE REGISTER

**Address: 0x34, Reset: 0x00, Name: SOUT_CONTROL0**

This register is for use only in TDM mode.

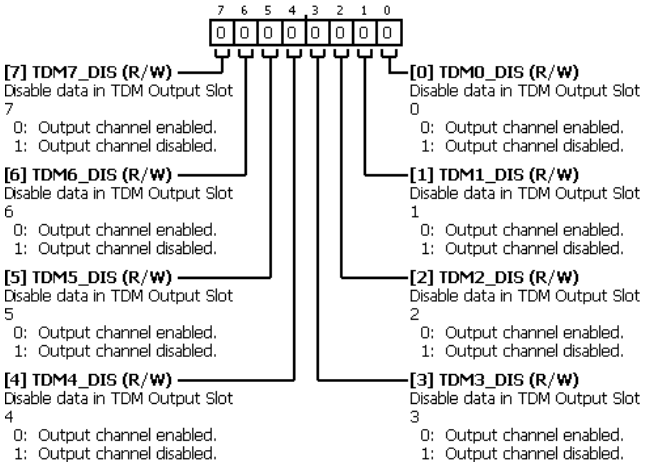



**Table 89. Bit Descriptions for SOUT_CONTROL0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | TDM7_DIS | | Disable data in TDM Output Slot 7. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 6 | TDM6_DIS | | Disable data in TDM Output Slot 6. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |
| 5 | TDM5_DIS | | Disable data in TDM Output Slot 5. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |
| 4 | TDM4_DIS | | Disable data in TDM Output Slot 4. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |
| 3 | TDM3_DIS | | Disable data in TDM Output Slot 3. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |
| 2 | TDM2_DIS | | Disable data in TDM Output Slot 2. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |
| 1 | TDM1_DIS | | Disable data in TDM Output Slot 1. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |
| 0 | TDM0_DIS | | Disable data in TDM Output Slot 0. | 0x0 | R/W |
| | | 0 | Output channel enabled. | | |
| | | 1 | Output channel disabled. | | |

## PDM ENABLE REGISTER

**Address: 0x36, Reset: 0x00, Name: PDM_OUT**

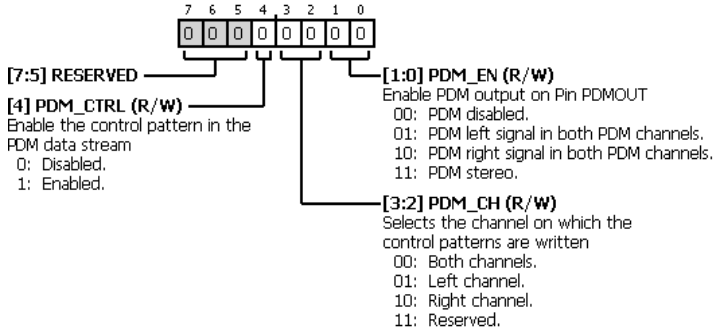



**Table 90. Bit Descriptions for PDM_OUT**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| 4 | PDM_CTRL | | Enable the control pattern in the PDM data stream. | 0x0 | R/W |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [3:2] | PDM_CH | | Selects the channel on which the control patterns are written. Do not change these control bits while the PDM channel is operating and transmitting audio. | 0x0 | R/W |
| | | 00 | Both channels. | | |
| | | 01 | Left channel. | | |
| | | 10 | Right channel. | | |
| | | 11 | Reserved. | | |
| [1:0] | PDM_EN | | Enable PDM output on Pin PDMOUT. | 0x0 | R/W |
| | | 00 | PDM disabled. | | |
| | | 01 | PDM left signal in both PDM channels. | | |
| | | 10 | PDM right signal in both PDM channels. | | |
| | | 11 | PDM stereo. | | |

## PDM PATTERN SETTING REGISTER

**Address: 0x37, Reset: 0x00, Name: PDM_PATTERN**

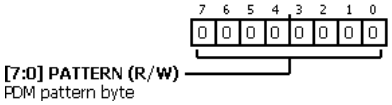



**Table 91. Bit Descriptions for PDM_PATTERN**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | PATTERN | | PDM pattern byte. The PDM pattern byte must not be changed while the PDM channel is operating and transmitting the pattern. | 0x0 | R/W |

## MP0 FUNCTION SETTING REGISTER

**Address: 0x38, Reset: 0x00, Name: MODE_MP0**

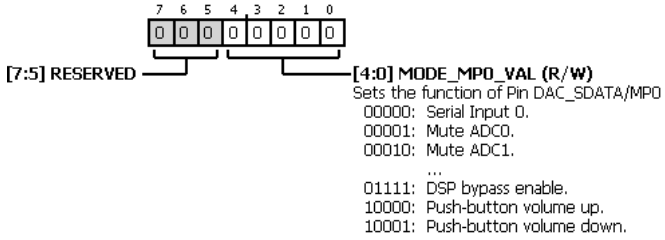



**Table 92. Bit Descriptions for MODE_MP0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | MODE_MP0_VAL | | Sets the function of Pin DAC_SDATA/MP0. | 0x0 | R/W |
| | | 00000 | Serial Input 0. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 01000 | Mute DAC0. | | |
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |

## MP1 FUNCTION SETTING REGISTER

**Address: 0x39, Reset: 0x10, Name: MODE_MP1**

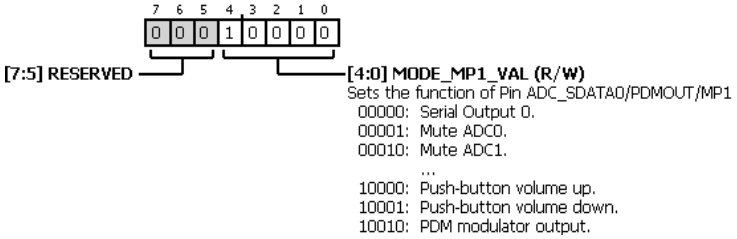



**Table 93. Bit Descriptions for MODE_MP1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | MODE_MP1_VAL | | Sets the function of Pin ADC_SDATA0/PDMOUT/MP1. | 0x10 | R/W |
| | | 00000 | Serial Output 0. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |
| | | 01000 | Mute DAC0. | | |
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |
| | | 10010 | PDM modulator output. | | |

## MP2 FUNCTION SETTING REGISTER

**Address: 0x3A, Reset: 0x00, Name: MODE_MP2**

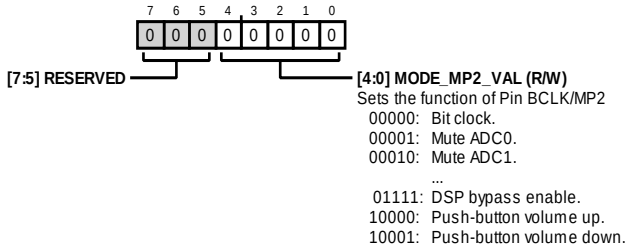



**Table 94. Bit Descriptions for MODE_MP2**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | MODE_MP2_VAL | | Sets the function of Pin BCLK/MP2 | 0x0 | R/W |
| | | 00000 | Bit clock. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |
| | | 01000 | Mute DAC0. | | |
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01100 | Reserved. | | |
| | | 01101 | Reserved. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |

## MP3 FUNCTION SETTING REGISTER

**Address: 0x3B, Reset: 0x00, Name: MODE_MP3**

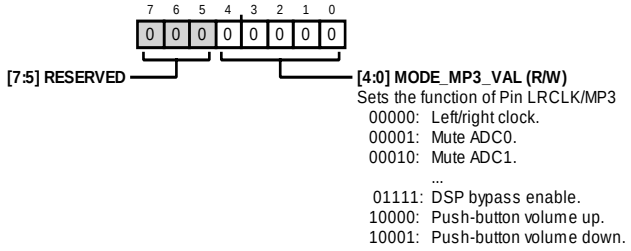



**Table 95. Bit Descriptions for MODE_MP3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [4:0] | MODE_MP3_VAL | | Sets the function of Pin LRCLK/MP3 | 0x0 | R/W |
| | | 00000 | Left/right clock. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |
| | | 01000 | Mute DAC0. | | |
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01100 | Reserved. | | |
| | | 01101 | Reserved. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |

## MP4 FUNCTION SETTING REGISTER

**Address: 0x3C, Reset: 0x00, Name: MODE_MP4**

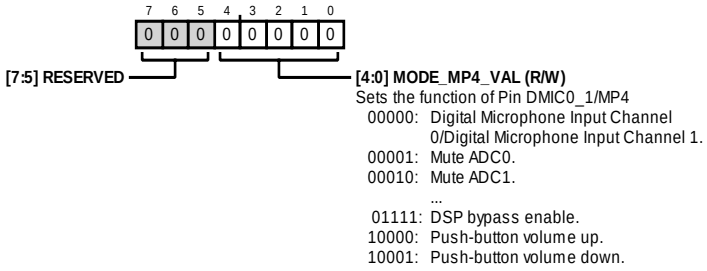



**Table 96. Bit Descriptions for MODE_MP4**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | MODE_MP4_VAL | | Sets the function of Pin DMIC0_1/MP4 | 0x0 | R/W |
| | | 00000 | Digital Microphone Input Channel 0/Digital Microphone Input Channel 1. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |
| | | 01000 | Mute DAC0. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01100 | Reserved. | | |
| | | 01101 | Reserved. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |

## MP5 FUNCTION SETTING REGISTER

**Address: 0x3D, Reset: 0x00, Name: MODE_MP5**

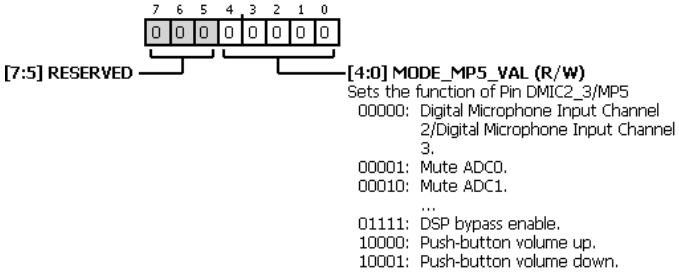



**Table 97. Bit Descriptions for MODE_MP5**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | MODE_MP5_VAL | | Sets the function of Pin DMIC2_3/MP5. | 0x0 | R/W |
| | | 00000 | Digital Microphone Input Channel 2/Digital Microphone Input Channel 3. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |
| | | 01000 | Mute DAC0. | | |
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01100 | Reserved. | | |
| | | 01101 | Reserved. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |

## MP6 FUNCTION SETTING REGISTER

**Address: 0x3E, Reset: 0x11, Name: MODE_MP6**

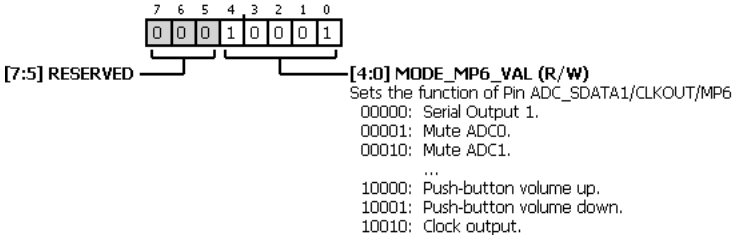



**Table 98. Bit Descriptions for MODE_MP6**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| [4:0] | MODE_MP6_VAL | | Sets the function of Pin ADC_SDATA1/CLKOUT/MP6. | 0x11 | R/W |
| | | 00000 | Serial Output 1. | | |
| | | 00001 | Mute ADC0. | | |
| | | 00010 | Mute ADC1. | | |
| | | 00011 | Mute ADC2. | | |
| | | 00100 | Mute ADC3. | | |
| | | 00101 | Mute ADC0 and ADC1. | | |
| | | 00110 | Mute ADC2 and ADC3. | | |
| | | 00111 | Mute all ADCs. | | |
| | | 01000 | Mute DAC0. | | |
| | | 01001 | Mute DAC1. | | |
| | | 01010 | Mute both DACs. | | |
| | | 01011 | A/B bank switch. | | |
| | | 01100 | Reserved. | | |
| | | 01101 | Reserved. | | |
| | | 01110 | Enable compression. | | |
| | | 01111 | DSP bypass enable. | | |
| | | 10000 | Push-button volume up. | | |
| | | 10001 | Push-button volume down. | | |
| | | 10010 | Clock output. | | |

## PUSH-BUTTON VOLUME SETTINGS REGISTER

**Address: 0x3F, Reset: 0x00, Name: PB_VOL_SET**

This register must be written before Bits PB_VOL_CONV_VAL are set to something other than the default value. Otherwise, the push-button volume control is initialized to −96 dB.

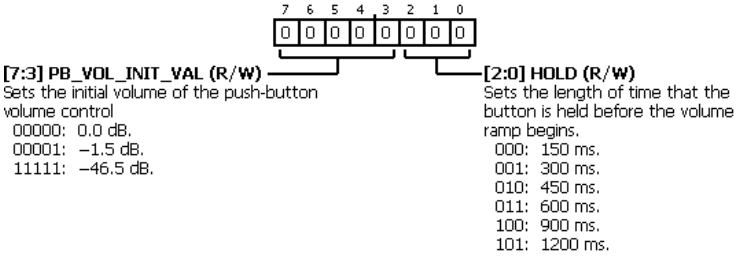


**Table 99. Bit Descriptions for PB_VOL_SET**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:3] | PB_VOL_INIT_VAL | | Sets the initial volume of the push-button volume control. Each increment of this register attenuates the level by 1.5 dB, from 0 dB to −46.5 dB. | 0x0 | R/W |
| | | 00000 | 0.0 dB. | | |
| | | 00001 | −1.5 dB. | | |
| | | 11111 | −46.5 dB. | | |
| [2:0] | HOLD | | Sets the length of time that the button is held before the volume ramp begins. | 0x0 | R/W |
| | | 000 | 150 ms. | | |
| | | 001 | 300 ms. | | |
| | | 010 | 450 ms. | | |
| | | 011 | 600 ms. | | |
| | | 100 | 900 ms. | | |
| | | 101 | 1200 ms. | | |

## PUSH-BUTTON VOLUME CONTROL ASSIGNMENT REGISTER

**Address: 0x40, Reset: 0x87, Name: PB_VOL_CONV**

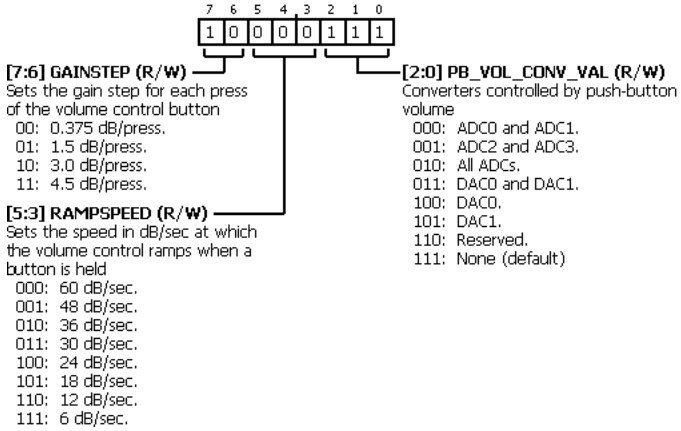



**Table 100. Bit Descriptions for PB_VOL_CONV**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | GAINSTEP | | Sets the gain step for each press of the volume control button. | 0x2 | R/W |
| | | 00 | 0.375 dB/press. | | |
| | | 01 | 1.5 dB/press. | | |
| | | 10 | 3.0 dB/press. | | |
| | | 11 | 4.5 dB/press. | | |
| [5:3] | RAMPSPEED | | Sets the speed in dB/sec at which the volume control ramps when a button is held. | 0x0 | R/W |
| | | 000 | 60 dB/sec. | | |
| | | 001 | 48 dB/sec. | | |
| | | 010 | 36 dB/sec. | | |
| | | 011 | 30 dB/sec. | | |
| | | 100 | 24 dB/sec. | | |
| | | 101 | 18 dB/sec. | | |
| | | 110 | 12 dB/sec. | | |
| | | 111 | 6 dB/sec. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [2:0] | PB_VOL_CONV_VAL | | Converters controlled by push-button volume. The push-button volume control is enabled when these bits are set to something other than the default setting (111). When set to 111, the push-button volume is disabled and the converter volumes are set by the ADCx_VOLUME and DACx_VOLUME registers. | 0x7 | R/W |
| | | 000 | ADC0 and ADC1. | | |
| | | 001 | ADC2 and ADC3. | | |
| | | 010 | All ADCs. | | |
| | | 011 | DAC0 and DAC1. | | |
| | | 100 | DAC0. | | |
| | | 101 | DAC1. | | |
| | | 110 | Reserved. | | |
| | | 111 | None (default). | | |

## DEBOUNCE MODES REGISTER

**Address: 0x41, Reset: 0x05, Name: DEBOUNCE_MODE**

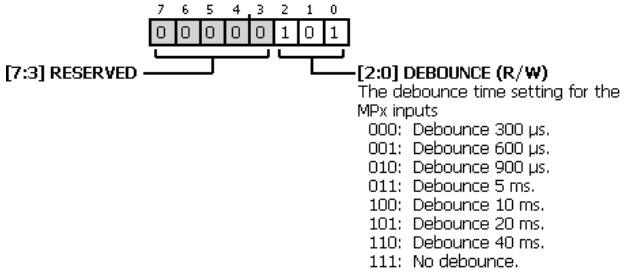



**Table 101. Bit Descriptions for DEBOUNCE_MODE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:3] | RESERVED | | Reserved. | 0x0 | R/W |
| [2:0] | DEBOUNCE | | The debounce time setting for the MPx inputs. | 0x5 | R/W |
| | | 000 | Debounce 300 µs. | | |
| | | 001 | Debounce 600 µs. | | |
| | | 010 | Debounce 900 µs. | | |
| | | 011 | Debounce 5 ms. | | |
| | | 100 | Debounce 10 ms. | | |
| | | 101 | Debounce 20 ms. | | |
| | | 110 | Debounce 40 ms. | | |
| | | 111 | No debounce. | | |

## HEADPHONE LINE OUTPUT SELECT REGISTER

**Address: 0x43, Reset: 0x0F, Name: OP_STAGE_CTRL**

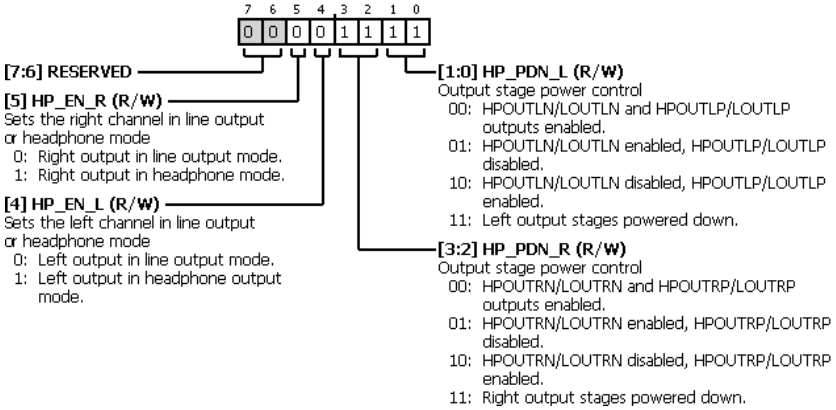



**Table 102. Bit Descriptions for OP_STAGE_CTRL**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | HP_EN_R | | Sets the right channel in line output or headphone mode. | 0x0 | R/W |
| | | 0 | Right output in line output mode. | | |
| | | 1 | Right output in headphone mode. | | |
| 4 | HP_EN_L | | Sets the left channel in line output or headphone mode | 0x0 | R/W |
| | | 0 | Left output in line output mode. | | |
| | | 1 | Left output in headphone output mode. | | |
| [3:2] | HP_PDN_R | | Output stage power control. These bits power down the right output stage, regardless of whether the device is in line output or headphone mode. After enabling the headphone output, wait at least 6 ms before unmuting the headphone output by setting HP_MUTE_R in the OP_STAGE_MUTES register to 00. | 0x3 | R/W |
| | | 00 | HPOUTRN/LOUTRN and HPOUTRP/LOUTRP outputs enabled. | | |
| | | 01 | HPOUTRN/LOUTRN enabled, HPOUTRP/LOUTRP disabled. | | |
| | | 10 | HPOUTRN/LOUTRN disabled, HPOUTRP/LOUTRP enabled. | | |
| | | 11 | Right output stages powered down. | | |
| [1:0] | HP_PDN_L | | Output stage power control. These bits power down the left output stage, regardless of whether the device is in line output or headphone mode. After enabling the headphone output, wait at least 6 ms before unmuting the headphone output by setting HP_MUTE_L in the OP_STAGE_MUTES register to 00. | 0x3 | R/W |
| | | 00 | HPOUTLN/LOUTLN and HPOUTLP/LOUTLP outputs enabled. | | |
| | | 01 | HPOUTLN/LOUTLN enabled, HPOUTLP/LOUTLP disabled. | | |
| | | 10 | HPOUTLN/LOUTLN disabled, HPOUTLP/LOUTLP enabled. | | |
| | | 11 | Left output stages powered down. | | |

## DECIMATOR POWER CONTROL REGISTER

**Address: 0x44, Reset: 0x00, Name: DECIM_PWR_MODES**

The bits in this register enable clocks to the digital filters and the ASRC decimator filters of the ADCs. These bits must be enabled for all channels used in the design. To use the ADCs, these SINC_x_EN bits must be enabled along with the appropriate ADC_x_EN bits in the ADC_CONTROL2 and ADC_CONTROL3 registers. If the digital microphone inputs are used, the SINC_x_EN bits can be set without setting ADC_x_EN.

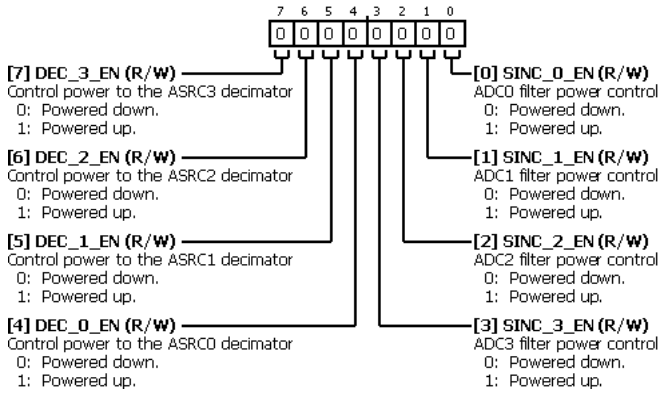



**Table 103. Bit Descriptions for DECIM_PWR_MODES**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | DEC_3_EN | | Control power to the ASRC3 decimator. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 6 | DEC_2_EN | | Control power to the ASRC2 decimator. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 5 | DEC_1_EN | | Control power to the ASRC1 decimator. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 4 | DEC_0_EN | | Control power to the ASRC0 decimator. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 3 | SINC_3_EN | | ADC3 filter power control. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 2 | SINC_2_EN | | ADC2 filter power control. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 1 | SINC_1_EN | | ADC1 filter power control. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 0 | SINC_0_EN | | ADC0 filter power control. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |

## ASRC INTERPOLATOR AND DAC MODULATOR POWER CONTROL REGISTER

**Address: 0x45, Reset: 0x00, Name: INTERP_PWR_MODES**

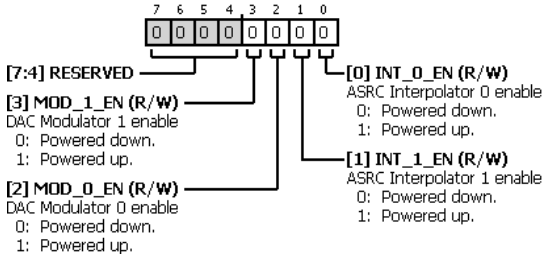



**Table 104. Bit Descriptions for INTERP_PWR_MODES**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:4] | RESERVED | | Reserved. | 0x0 | R/W |
| 3 | MOD_1_EN | | DAC Modulator 1 enable. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 2 | MOD_0_EN | | DAC Modulator 0 enable. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 1 | INT_1_EN | | ASRC Interpolator 1 enable. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |
| 0 | INT_0_EN | | ASRC Interpolator 0 enable. | 0x0 | R/W |
| | | 0 | Powered down. | | |
| | | 1 | Powered up. | | |

## ANALOG BIAS CONTROL 0 REGISTER

**Address: 0x46, Reset: 0x00, Name: BIAS_CONTROL0**

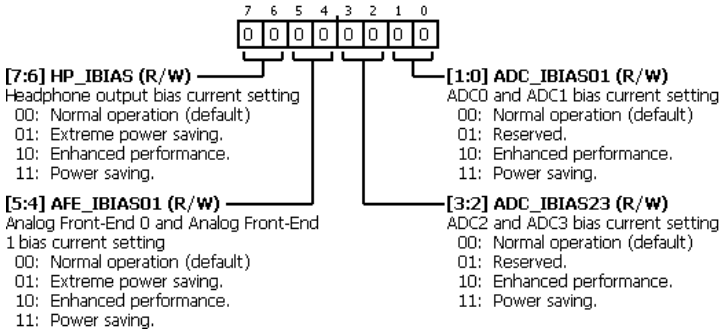



**Table 105. Bit Descriptions for BIAS_CONTROL0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | HP_IBIAS | | Headphone output bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Extreme power saving. | | |
| | | 10 | Enhanced performance. | | |
| | | 11 | Power saving. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [5:4] | AFE_IBIAS01 | | Analog Front-End 0 and Analog Front-End 1 bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Extreme power saving. | | |
| | | 10 | Enhanced performance. | | |
| | | 11 | Power saving. | | |
| [3:2] | ADC_IBIAS23 | | ADC2 and ADC3 bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Reserved. | | |
| | | 10 | Enhanced performance. | | |
| | | 11 | Power saving. | | |
| [1:0] | ADC_IBIAS01 | | ADC0 and ADC1 bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Reserved. | | |
| | | 10 | Enhanced performance. | | |
| | | 11 | Power saving. | | |

## ANALOG BIAS CONTROL 1 REGISTER

**Address: 0x47, Reset: 0x00, Name: BIAS_CONTROL1**

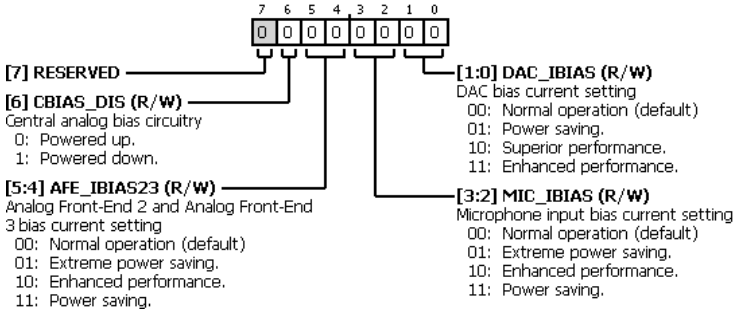



**Table 106. Bit Descriptions for BIAS_CONTROL1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| 6 | CBIAS_DIS | | Central analog bias circuitry. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 0 | Powered up. | | |
| | | 1 | Powered down. | | |
| [5:4] | AFE_IBIAS23 | | Analog Front-End 2 and Analog Front-End 3 bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Extreme power saving. | | |
| | | 10 | Enhanced performance. | | |
| | | 11 | Power saving. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [3:2] | MIC_IBIAS | | Microphone input bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Extreme power saving. | | |
| | | 10 | Enhanced performance. | | |
| | | 11 | Power saving. | | |
| [1:0] | DAC_IBIAS | | DAC bias current setting. Higher bias currents result in higher performance. | 0x0 | R/W |
| | | 00 | Normal operation (default). | | |
| | | 01 | Power saving. | | |
| | | 10 | Superior performance. | | |
| | | 11 | Enhanced performance. | | |

## DIGITAL PIN PULL-UP CONTROL 0 REGISTER

**Address: 0x48, Reset: 0x7F, Name: PAD_CONTROL0**

Enable pull-up resistors for each digital pin.

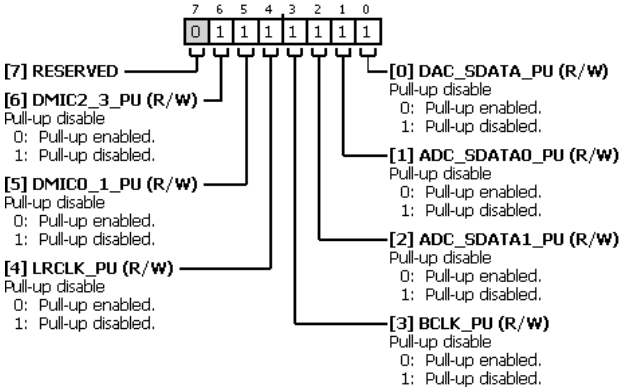



**Table 107. Bit Descriptions for PAD_CONTROL0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| 6 | DMIC2_3_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 5 | DMIC0_1_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 4 | LRCLK_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 3 | BCLK_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 2 | ADC_SDATA1_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 1 | ADC_SDATA0_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 0 | DAC_SDATA_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |

## DIGITAL PIN PULL-UP CONTROL 1 REGISTER

**Address: 0x49, Reset: 0x1F, Name: PAD_CONTROL1**

Enable pull-up resistors for each digital pin.

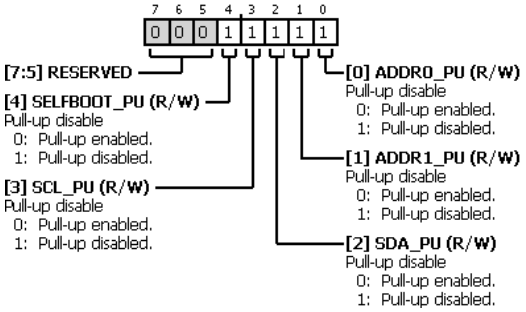



**Table 108. Bit Descriptions for PAD_CONTROL1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| 4 | SELFBOOT_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 3 | SCL_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 2 | SDA_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 1 | ADDR1_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |
| 0 | ADDR0_PU | | Pull-up disable. | 0x1 | R/W |
| | | 0 | Pull-up enabled. | | |
| | | 1 | Pull-up disabled. | | |

## DIGITAL PIN PULL-DOWN CONTROL 0 REGISTER

**Address: 0x4A, Reset: 0x00, Name: PAD_CONTROL2**

Enable pull-down resistors for each digital pin.

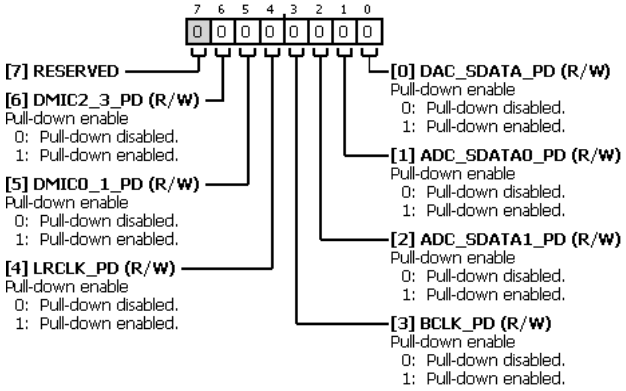



**Table 109. Bit Descriptions for PAD_CONTROL2**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| 6 | DMIC2_3_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 5 | DMIC0_1_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 4 | LRCLK_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 3 | BCLK_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 2 | ADC_SDATA1_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 1 | ADC_SDATA0_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 0 | DAC_SDATA_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |

## DIGITAL PIN PULL-DOWN CONTROL 1 REGISTER

**Address: 0x4B, Reset: 0x00, Name: PAD_CONTROL3**

Enable pull-down resistors for each digital pin.

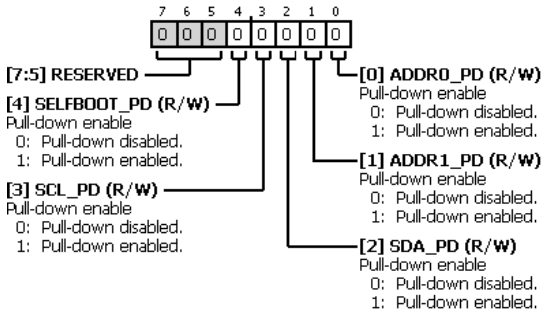



**Table 110. Bit Descriptions for PAD_CONTROL3**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| 4 | SELFBOOT_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 3 | SCL_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 2 | SDA_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 1 | ADDR1_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |
| 0 | ADDR0_PD | | Pull-down enable. | 0x0 | R/W |
| | | 0 | Pull-down disabled. | | |
| | | 1 | Pull-down enabled. | | |

## DIGITAL PIN DRIVE STRENGTH CONTROL 0 REGISTER

**Address: 0x4C, Reset: 0x00, Name: PAD_CONTROL4**

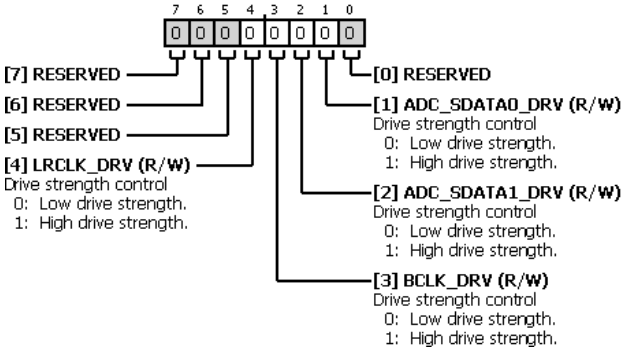



**Table 111. Bit Descriptions for PAD_CONTROL4**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | RESERVED | | Reserved. | 0x0 | R/W |
| 6 | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | RESERVED | | Reserved. | 0x0 | R/W |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 4 | LRCLK_DRV | | Drive strength control. | 0x0 | R/W |
| | | 0 | Low drive strength. | | |
| | | 1 | High drive strength. | | |
| 3 | BCLK_DRV | | Drive strength control. | 0x0 | R/W |
| | | 0 | Low drive strength. | | |
| | | 1 | High drive strength. | | |
| 2 | ADC_SDATA1_DRV | | Drive strength control. | 0x0 | R/W |
| | | 0 | Low drive strength. | | |
| | | 1 | High drive strength. | | |
| 1 | ADC_SDATA0_DRV | | Drive strength control. | 0x0 | R/W |
| | | 0 | Low drive strength. | | |
| | | 1 | High drive strength. | | |
| 0 | RESERVED | | Reserved. | 0x0 | R/W |

## DIGITAL PIN DRIVE STRENGTH CONTROL 1 REGISTER

**Address: 0x4D, Reset: 0x00, Name: PAD_CONTROL5**

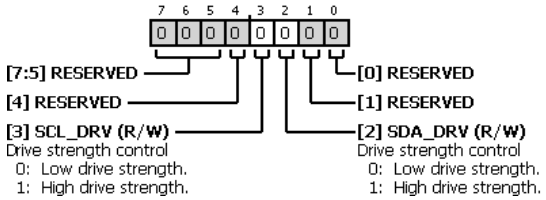



**Table 112. Bit Descriptions for PAD_CONTROL5**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | RESERVED | | Reserved. | 0x0 | R/W |
| 4 | RESERVED | | Reserved. | 0x0 | R/W |
| 3 | SCL_DRV | | Drive strength control. | 0x0 | R/W |
| | | 0 | Low drive strength. | | |
| | | 1 | High drive strength. | | |
| 2 | SDA_DRV | | Drive strength control. | 0x0 | R/W |
| | | 0 | Low drive strength. | | |
| | | 1 | High drive strength. | | |
| 1 | RESERVED | | Reserved. | 0x0 | R/W |
| 0 | RESERVED | | Reserved. | 0x0 | R/W |

## FAST RATE CONTROL REGISTER

**Address: 0x4E, Reset: 0x00, Name: FAST_RATE**

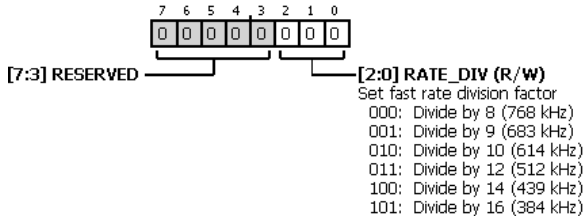


**Table 113. Bit Descriptions for FAST_RATE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:3] | RESERVED | | Reserved. | 0x0 | R/W |
| [2:0] | RATE_DIV | | Set fast rate division factor. This factor is used to divide the internal master clock (6.144 MHz) when CORE_FS = 11. Do not change this setting while the core is running. CORE_RUN must be set to 0 for this setting to be updated. | 0x0 | R/W |
| | | 000 | Divide by 8 (768 kHz). | | |
| | | 001 | Divide by 9 (683 kHz). | | |
| | | 010 | Divide by 10 (614 kHz). | | |
| | | 011 | Divide by 12 (512 kHz). | | |
| | | 100 | Divide by 14 (439 kHz). | | |
| | | 101 | Divide by 16 (384 kHz). | | |

## DAC INTERPOLATION CONTROL REGISTER

**Address: 0x4F, Reset: 0x00, Name: DAC_CONTROL0**

The lowest interpolator latency is achieved with a zero-order hold (ZOH) selection. ZOH can be used for both 768 kHz and 192 kHz data. For 96 kHz data, use the linear interpolation to attain the lowest latency.

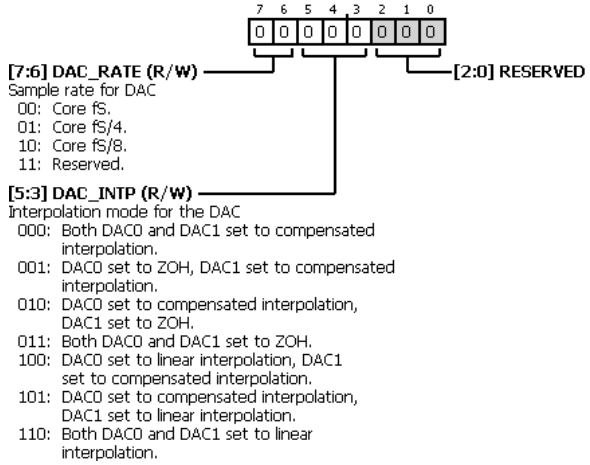



**Table 114. Bit Descriptions for DAC_CONTROL0**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | DAC_RATE | | Sample rate for DAC. | 0x0 | R/W |
| | | 00 | Core $f_S$. | | |
| | | 01 | Core $f_S/4$. | | |
| | | 10 | Core $f_S/8$. | | |
| | | 11 | Reserved. | | |
| [5:3] | DAC_INTP | | Interpolation mode for the DAC. | 0x0 | R/W |
| | | 000 | Both DAC0 and DAC1 set to compensated interpolation. | | |
| | | 001 | DAC0 set to ZOH, DAC1 set to compensated interpolation. | | |
| | | 010 | DAC0 set to compensated interpolation, DAC1 set to ZOH. | | |
| | | 011 | Both DAC0 and DAC1 set to ZOH. | | |
| | | 100 | DAC0 set to linear interpolation, DAC1 set to compensated interpolation. | | |
| | | 101 | DAC0 set to compensated interpolation, DAC1 set to linear interpolation. | | |
| | | 110 | Both DAC0 and DAC1 set to linear interpolation. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [2:0] | RESERVED | | Reserved. | 0x0 | R/W |

## VOLUME CONTROL BYPASS REGISTER

**Address: 0x54, Reset: 0x00, Name: VOL_BYPASS**

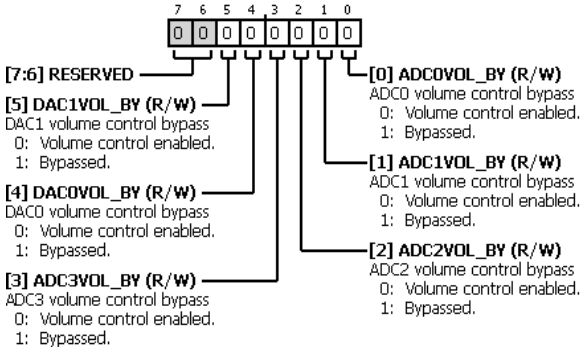



**Table 115. Bit Descriptions for VOL_BYPASS**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R/W |
| 5 | DAC1VOL_BY | | DAC1 volume control bypass. | 0x0 | R/W |
| | | 0 | Volume control enabled. | | |
| | | 1 | Bypassed. | | |
| 4 | DAC0VOL_BY | | DAC0 volume control bypass. | 0x0 | R/W |
| | | 0 | Volume control enabled. | | |
| | | 1 | Bypassed. | | |
| 3 | ADC3VOL_BY | | ADC3 volume control bypass. | 0x0 | R/W |
| | | 0 | Volume control enabled. | | |
| | | 1 | Bypassed. | | |
| 2 | ADC2VOL_BY | | ADC2 volume control bypass. | 0x0 | R/W |
| | | 0 | Volume control enabled. | | |
| | | 1 | Bypassed. | | |
| 1 | ADC1VOL_BY | | ADC1 volume control bypass. | 0x0 | R/W |
| | | 0 | Volume control enabled. | | |
| | | 1 | Bypassed. | | |
| 0 | ADC0VOL_BY | | ADC0 volume control bypass. | 0x0 | R/W |
| | | 0 | Volume control enabled. | | |
| | | 1 | Bypassed. | | |

# OUTLINE DIMENSIONS

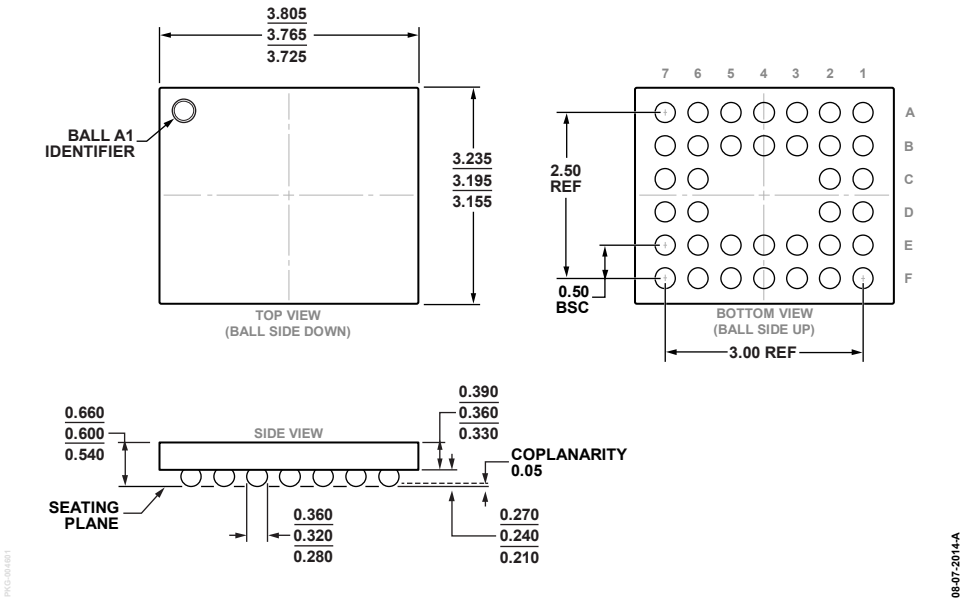



*Figure 79. 36-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-36-4)*
*Dimension shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADAU1777BCBZRL | −40°C to +85°C | 36-Ball Wafer Level Chip Scale Package [WLCSP], 13" Tape and Reel | CB-36-4 |
| EVAL-ADAU1777Z | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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