# OPA521 2.5A 窄带线路驱动器

## 1 特性

- 支持：
  - CENELEC 频带 A、B、C、D
  - ARIB STD-T84、FCC
  - FSK、SFSK 和 NB-OFDM
- 符合：
  - EN50065-1、-2、-3、-7
  - FCC 第 15 部分
  - ARIB STD-T84
- 标准：
  - G3、PRIME、P1901.2、ITU-G.hnem
- 具有集成式热保护和过流保护功能的线路驱动器
- 引脚可选静态电流消耗：
  - 待机模式时电流为 58 µA（典型值）
  - CENELEC 频带 A、B、C、D 的电流为 51mA（典型值）
  - FCC、ARIB STD-T84 的电流为 78mA（典型值）
- 封装：5mm × 5mm 20 引脚 VQFN
- 工作结温范围：
  $T_A$ = –40°C 至 +125°C

## 2 应用

- 电能质量监测仪
- 商用网络和服务器 PSU
- 照明
- 太阳能电弧保护
- 中央逆变器

## 3 说明

OPA521 是一种线路驱动器功率放大器，符合 CENELEC 频带 A、B、C、D 和 ARIB STD-T84、FCC 第 15 部分的电力线通信 (PLC) 传导发射要求。此器件在高电流、低阻抗且具有无功负载的线路上最高可提供 2.5A 电流。OPA521 具备优化的内部保护结构，因此它只需极少的外部保护组件，实现具有经济效益且节省空间的系统。

OPA521 带宽为 3.8MHz，可提供 –7V/V 的闭环增益。此单片集成型电路为电源线通信应用提供 高可靠性。

OPA521 线路驱动器由 7V 至 24V 电压的单电源供电。在典型负载电流情况下（$I_{OUT}$ = 2.5A，最大值），宽输出摆幅能够以 24V 的标称电源电压提供 $10V_{PP}$ 电压。

此器件具有过热和短路保护。故障检测标志显示电流和热限值。提供有一个关断引脚，利用该引脚可将器件置于低功耗状态，消耗电流为 58µA（典型值）。

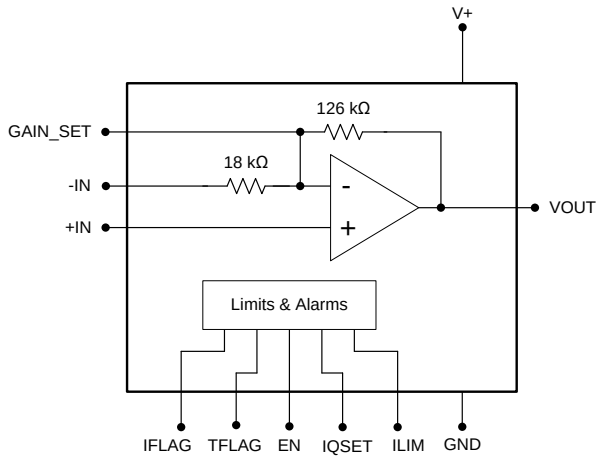
OPA521 可提供表面贴装式 5mm × 5mm 20 引脚 VQFN (RGW) 封装。此器件可在 -40°C 至 +125°C 的扩展工业结温范围内正常运行。

**器件信息(1)**

| 器件编号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| OPA521 | VQFN (20) | 5.00mm × 5.00mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

**OPA521 方框图**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 修订历史记录

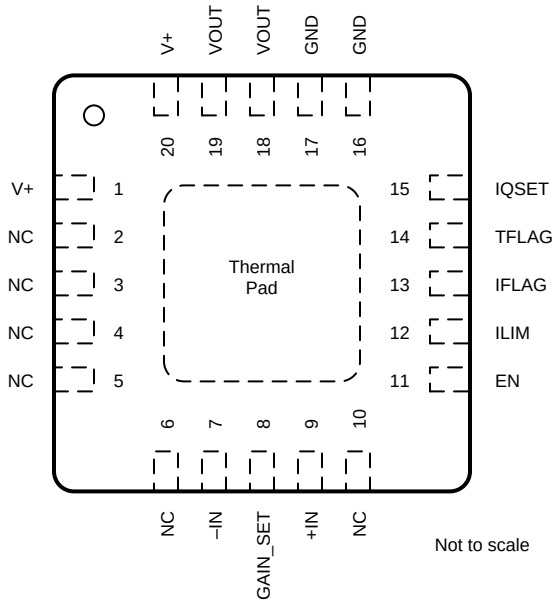
注：之前版本的页码可能与当前版本有所不同。

| **Changes from Original (May 2018) to Revision A** | **Page** |
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# 5 Pin Configuration and Functions

**RGW Package**
**20-Pin VQFN With Exposed Thermal Pad**
**Top View**




NC - no internal connection

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 11 | I | Enables the amplifier (active high, high enables the OPA521) |
| GAIN_SET | 8 | I | Connect an external resistor to Gain_Set and -IN to increase the gain beyond -7 V/V |
| GND | 16, 17 | — | Ground |
| IFLAG | 13 | O | Current limit warning flag (open-drain, active high, high signifies current limit condition) |
| ILIM | 12 | I | Resistor programmable current limit |
| +IN | 9 | I | Non-inverting input (connect to a voltage equal to (V+)/2) |
| –IN | 7 | I | Inverting input for closed loop gain = –7 V/V |
| IQSET | 15 | I | Quiescent current select (active high, high configures the OPA521 to operate in FCC/ARIB bands, low configures the OPA521 to operate in CENELEC Bands A, B, C, D) |
| NC | 2, 3, 4, 5, 6, 10 | — | No internal connection |
| TFLAG | 14 | O | Thermal limit warning flag (open-drain, active high, high signifies thermal limit condition) |
| V+ | 1, 20 | — | Positive power supply |
| VOUT | 18. 19 | O | Output |
| Thermal pad | | — | Must be soldered to PCB and connected to GND |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, V+ | | Pins 1, 20 | | 26 | V |
| Signal input pins | Voltage(2) | Pins 7, 8, 9, 12 | –0.4 | (V+) + 0.4 | V |
| | | Pins 11, 15 | –0.4 | 3.3 | |
| | Current(2) | Pins 7, 8, 9, 11, 12, 15 | | ±10 | mA |
| Signal output terminals | Voltage | Pins 18, 19 | –0.4 | (V+) + 0.4 | V |
| | | Pins 13, 14 | –0.4 | 3.3 | |
| | Current; short-circuit to GND | Pins 13, 14, 18, 19 | Continuous | | |
| Operating junction temperature(3) | | | –40 | 125 | °C |
| Storage temperature, $T_{stg}$ | | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.4 V beyond the supply rails should be current limited to 10 mA or less.
(3) The device automatically goes into shutdown above +140℃ junction temperature

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, V+ | 7 | | 24 | V |
| Output current, DC(1) | | | 1.9 | A |
| Operating junction temperature | –40 | | 125 | °C |

(1) Under safe operating conditions. See *Power Amplifier Stress and Power Handling Limitations* safe operating area (SOA) information.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | OPA521 RGW (QFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 33.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 24.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 12.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 12.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 6.5 Electrical Characteristics

At $T_{CASE}$ = 25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **NOISE** | | | | | | | |
| | Integrated output noise | CEN-A | 35 kHz to 95 kHz | | 45 | | $\mu V_{RMS}$ |
| | | CEN-B | 95 kHz to 125 kHz | | 32 | | $\mu V_{RMS}$ |
| | | CEN-C | 125 kHz to 140 kHz | | 23 | | $\mu V_{RMS}$ |
| | | CEN-D | 140 kHz to 148 kHz | | 16.5 | | $\mu V_{RMS}$ |
| | | ARIB STD-T84 | 35 kHz to 420 kHz | | 114 | | $\mu V_{RMS}$ |
| | | FCC-LOW | 35 kHz to 125 kHz | | 55 | | $\mu V_{RMS}$ |
| | | G3-FCC | 150 kHz to 490 kHz | | 107 | | $\mu V_{RMS}$ |
| **INPUT** | | | | | | | |
| | Input voltage range, IN- | | For linear operation, +IN = V+/2 | (GND + 0.4)/7 | | (V+ – 0.4)/7 | V |
| | Input impedance | | | | 18 | | kΩ |
| **FREQUENCY RESPONSE** | | | | | | | |
| BW | Bandwidth | | $I_{LOAD}$ = 0 mA | | 3.82 | | MHz |
| SR | Slew rate | | V+ = 24 V, $V_{OUT}$ = 20-V step | | 75 | | V/µs |
| | Full-power bandwidth | | V+ = 24 V, $V_{OUT}$ = 15 $V_{PP}$ | | 800 | | kHz |
| PSRR | Power-supply rejection ratio | | RTI, DC | 80 | 94 | | dB |
| | | | RTI, DC to f = 50 kHz | | See Typical Curves | | |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | From V+ | $I_O$ = 200-mA sourcing, 1-ms pulse | | | 0.5 | V |
| | | | $I_O$ = 1.5-A sourcing, 1-ms pulse | | | 2.25 | V |
| | | From GND | $I_O$ = 200 mA sinking, 1-ms pulse | | | 0.5 | V |
| | | | $I_O$ = 1.5-A sinking, 1-ms pulse | | | 1.5 | V |
| | Max continuous current, DC | | ILIM (pin 12) connected to ground | See *Recommended Operating Conditions* | | | A |
| | Output resistance | | $I_O$ = 1.9 A, f = 500 kHz | | 0.1 | | Ω |
| | Disabled output impedance | | f = 100 kHz | | 145 \|\| 125 | | kΩ \|\| pF |
| | Max output current | Resistor-selectable | ILIM (pin 12) connected to ground | | 2.5 | | A |
| **GAIN** | | | | | | | |
| G | Nominal gain | | $V_{OUT}/V_{IN}$ | | –7 | | V/V |
| $G_E$ | Gain error | | $T_J$ = -40°C to +125°C | –2% | 0.1% | 2% | |
| | Gain error drift | | $T_J$ = -40°C to +125°C | | ±5 | | ppm/°C |
| **THERMAL SHUTDOWN** | | | | | | | |
| | Junction temperature at shutdown | | | | 140 | | °C |
| | Hysteresis | | | | 10 | | °C |
| | Return to normal operation | | | | 130 | | °C |

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## 6.6 Electrical Characteristics: Digital

At $T_{CASE}$ = 25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (ENABLE, IQSET)** | | | | | | | |
| | Leakage input current | | GND ≤ $V_{IN}$ ≤ 3.3 | –1 | 0.01 | 1 | µA |
| $V_{IH}$ | High-level input voltage | | | | 2 | 3.3 | V |
| $V_{IL}$ | Low-level input voltage | | | GND | | 0.8 | V |
| | EN pin function (active high) | EN pin high | 2 < EN < 3.3 | Device in normal operation | | | |
| | | EN pin low | EN < 0.8 | Device in shutdown | | | |
| | IQSET pin function (active high) | IQSET pin high | IQSET > 2 | Device in FCC/ARIB mode ($I_Q$ = 78 mA (typ)) | | | |
| | | IQSET pin low | IQSET < 0.8 | Device in CENELEC mode ($I_Q$ = 51 mA (typ)) | | | |
| **DIGITAL OUTPUTS (TFLAG, IFLAG)** | | | | | | | |
| $I_{OH}$ | High-level output current | | $V_{OH}$ = 3.3 V | | | 1 | µA |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $I_{OL}$ | Low-level output current | | $V_{OL}$ = 400 mV | 4 | | | mA |
| | TFLAG (active high, open-drain) | TFLAG pin high | TFLAG sink high < 1 µA | Device is in thermal shutdown | | | |
| | | TFLAG pin low | TFLAG < 0.4 V | Device is not in thermal shutdown | | | |
| | IFLAG (active high, open-drain) | IFLAG pin high | IFLAG sink high < 1 µA | Device is in current limit | | | |
| | | IFLAG pin low | IFLAG < 0.4 V | Device is not in current limit | | | |
| **SHUTDOWN MODE TIMING** | | | | | | | |
| | Enable time | | SD pin transitions from low to high | | 3 | | ms |
| | Disable time | | SD pin transitions from high to low | | 2 | | ms |

## 6.7 Electrical Characteristics: Power Supply

At $T_{CASE}$ = 25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING SUPPLY RANGE** | | | | | | |
| V+ | Power amplifier | | 7 | 15 | 24 | V |
| **QUIESCENT CURRENT (ENABLE pin high)** | | | | | | |
| $I_Q$ | FCC/ARIB mode | $I_O$ = 0 A, IQSET pin high | 64 | 78 | 88 | mA |
| | CENELEC mode | $I_O$ = 0 A, IQSET pin low | 41 | 51 | 61 | mA |
| **SHUTDOWN (ENABLE pin low)** | | | | | | |
| EN | Power amplifier | EN pin low | | 58 | 130 | µA |


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## 6.8 Typical Characteristics

At $T_{CASE}$ = +25°C, V+ = 24 V, IN+ = (V+)/2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

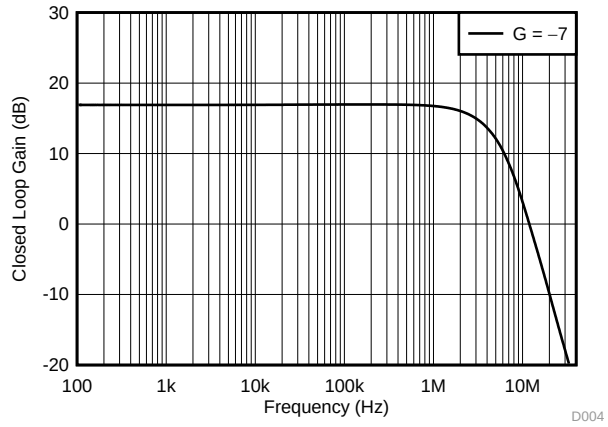



图 1. Closed Loop Gain vs Frequency

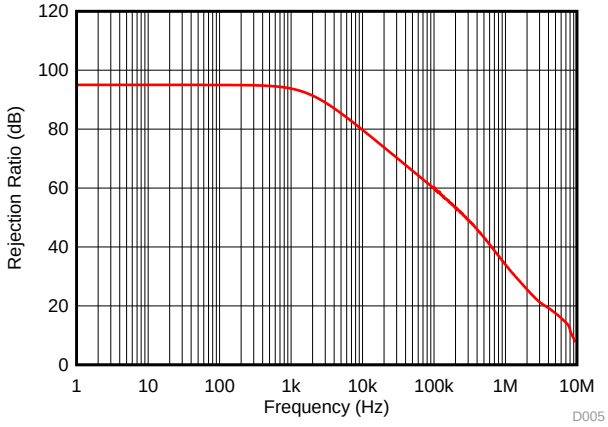
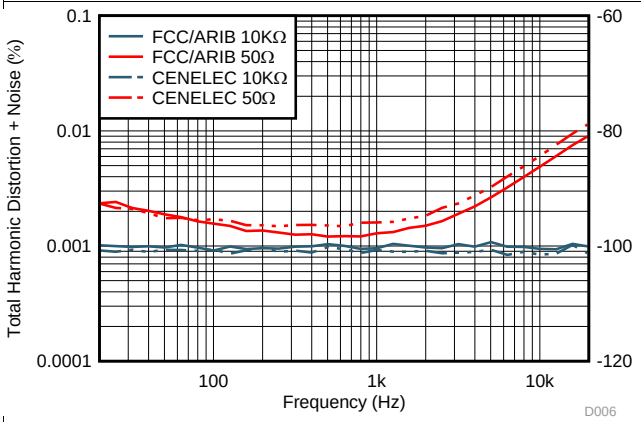
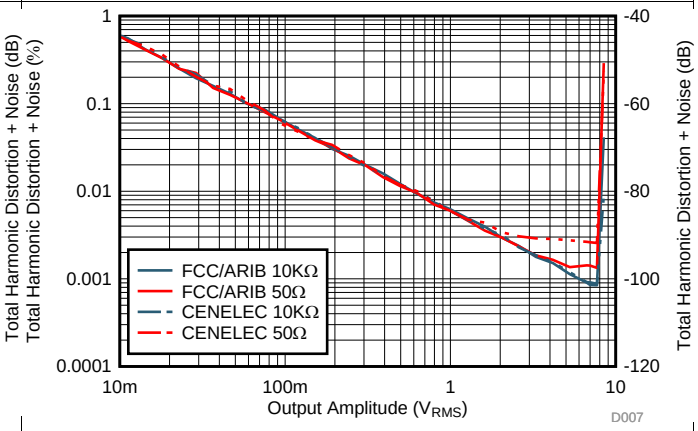



图 2. PSRR+ vs Frequency




$V_{OUT}$ = 7 $V_{RMS}$

图 3. THD+N vs Frequency




$f$ = 1 kHz

图 4. THD+N vs Output Amplitude

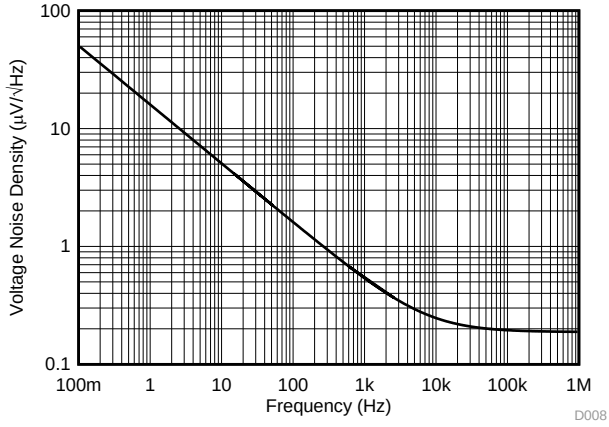



图 5. Input Voltage Noise Spectral Density

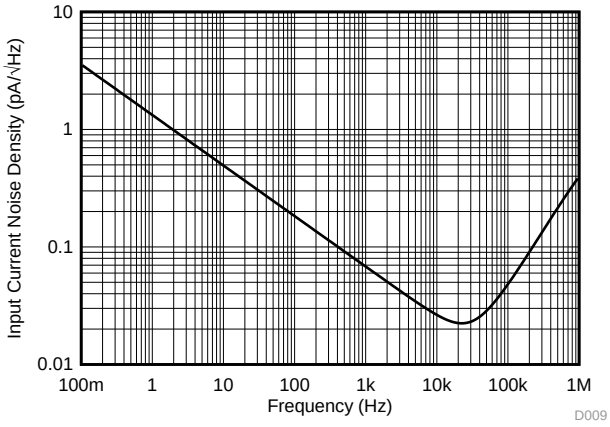



图 6. Input Current Noise Density

## Typical Characteristics (接下页)

At $T_{CASE}$ = +25°C, V+ = 24 V, IN+ = (V+)/2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

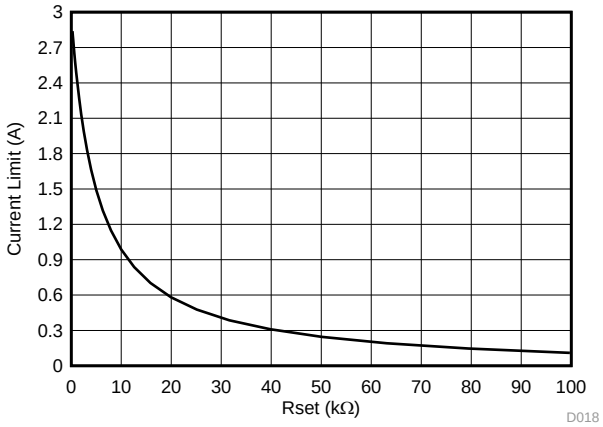



图 7. Maximum Output Current Limit vs $R_{SET}$

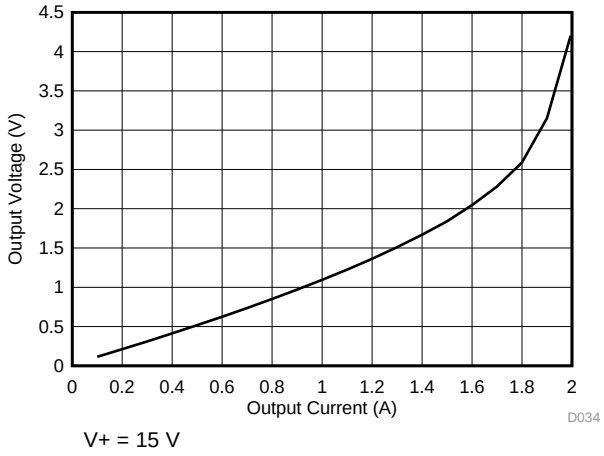



图 8. Output Swing from V+ vs Output Current (Sourcing)

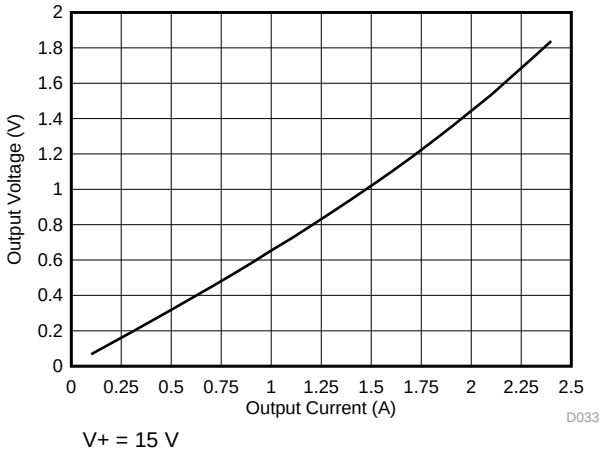



图 9. Output Swing from GND vs Output Current (Sinking)

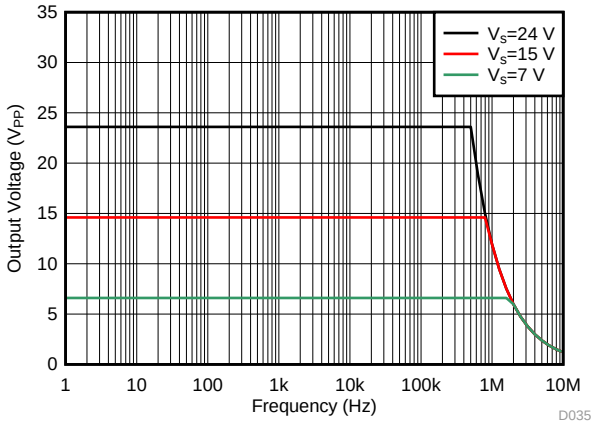



图 10. Maximum Output Voltage vs Frequency

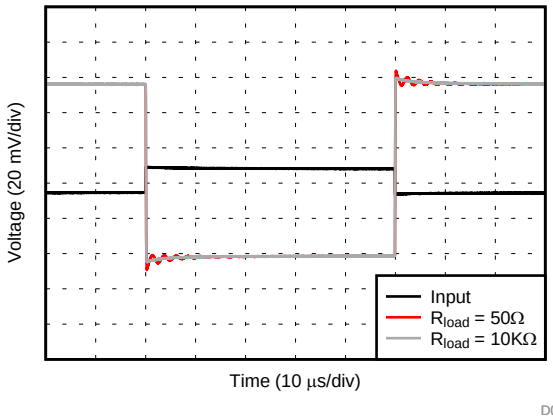



图 11. Small-Signal Step Response

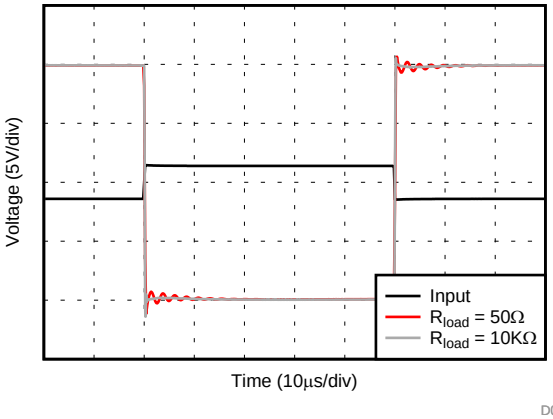



图 12. Large-Signal Step Response



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## Typical Characteristics (接下页)

At $T_{CASE}$ = +25°C, V+ = 24 V, IN+ = (V+)/2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

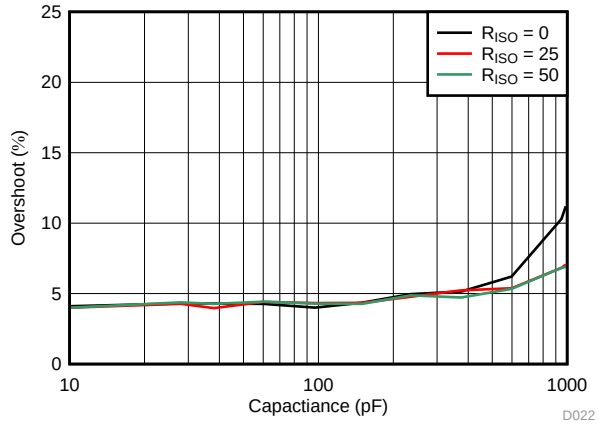



图 13. Small-Signal Overshoot vs Capacitive Load

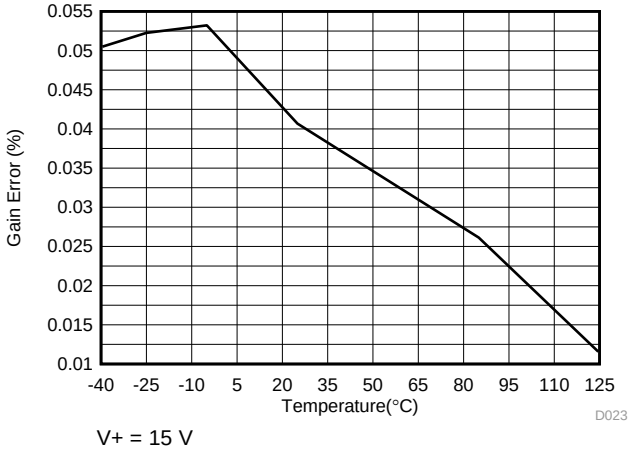



图 14. Gain Error vs Temperature

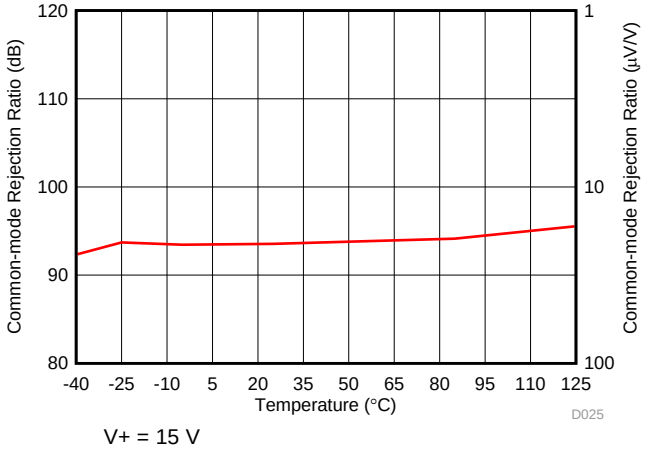



图 15. CMRR vs Temperature

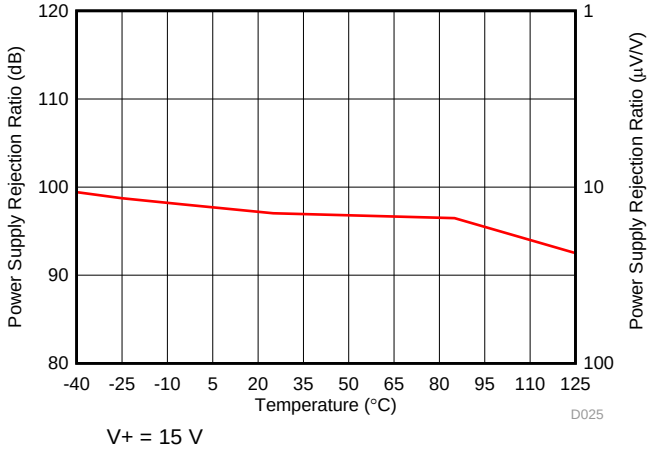



图 16. PSRR vs Temperature

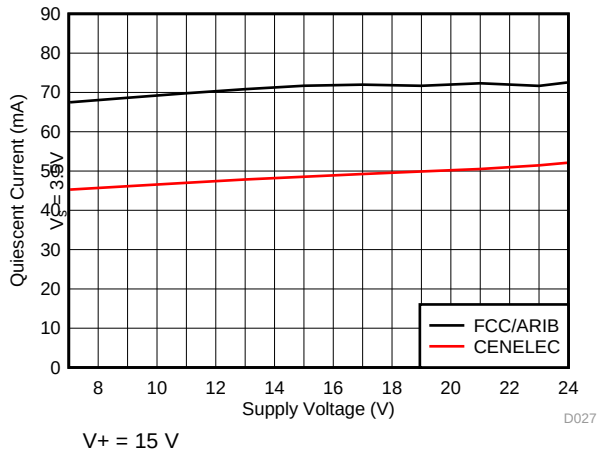



图 17. Iq vs Supply Voltage

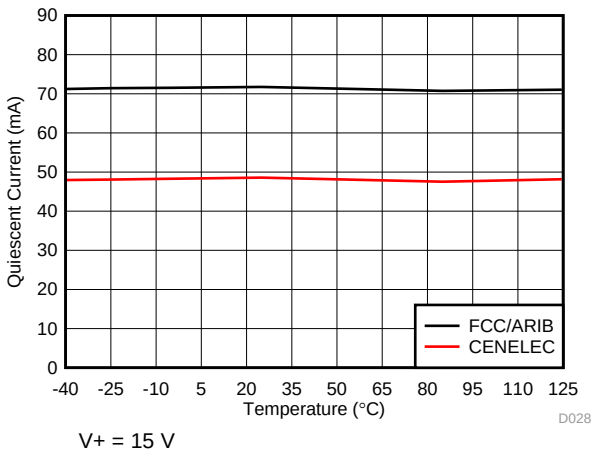



图 18. Iq vs Temperature

## Typical Characteristics (接下页)

At $T_{CASE}$ = +25°C, V+ = 24 V, IN+ = (V+)/2, $R_{LOAD}$ = 50 Ω unless otherwise noted.

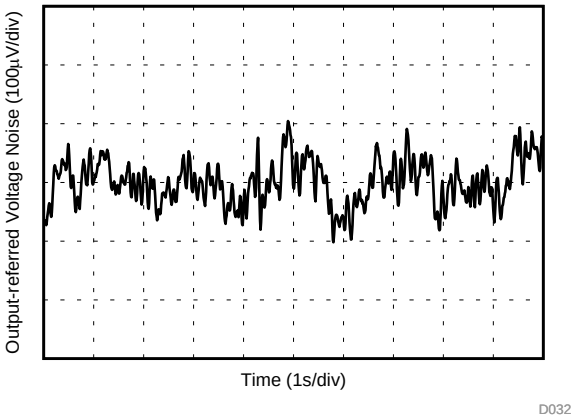



**图 19. 0.1-Hz to 10-Hz Noise**

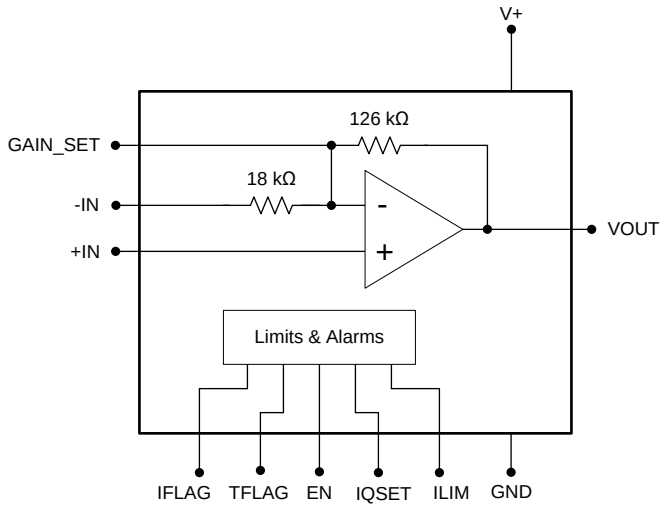

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# 7 Detailed Description

## 7.1 Overview

The OPA521 is a power amplifier (PA) designed for power-line communication (PLC) applications. The device features a fixed gain of –7 V/V, low-pass filter response, excellent linearity and low distortion through the bandwidth. The amplifier operates with 7-V to 24-V supplies, and can deliver up to ±1.9 A of continuous current from –40°C to +125°C.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The OPA521 offers an optional output current limit (ILIM), quiescent current (IQSET) selection pins, and a device enable pin. The IFLAG output alarm pin indicates an output current warning and the TFLAG alarm triggers when the internal temperature of the device forces the devices to shut down.

### 7.3.1 IQSET Pin

This pin sets the operating band of the amplifier by adjusting the quiescent current.

- IQSET > 2 V sets the device to operate in the FCC or ARIB bands
- IQSET < 0.8 V sets the device to operate in the CENELEC bands

### 7.3.2 EN Pin

When the transmitter is not in use, the output is disabled and placed in a high-impedance state when the EN pin decreases. For typical operation, connect the EN pin to 3.3 V. In disabled mode, the entire device draws 58 μA (typical) of current.

### 7.3.3 ILIM Pin Current Limiting

The ILIM pin (pin 12) provides a resistor-programmable output current limit. 图 6 shows the typical current limit for a given external $R_{SET}$ resistor attached to this pin.

Several typical target values and the approximate corresponding $R_{SET}$ are provided in 表 1.

**表 1. Typical Current Limit and $R_{SET}$ Values**

| CURRENT LIMIT (A) | $R_{SET}$ (approximate, kΩ) |
|---|---|
| Maximum Output | Grounded |
| 1 | 10 |
| 0.5 | 25 |

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### 7.3.4 IFLAG and TFLAG Pins

The IFLAG and TFLAG pins are active-high, open-drain outputs that indicate if the OPA521 is in current or thermal limit. Connect these pins to 3.3 V through pullup resistors (for example 10 kΩ).

The maximum output current from the power amplifier is programmed with the external $I_{LIM}$ resistor that is connected between ILIM (pin 12) and ground. IFLAG is set if the amplifier goes to a current limit state if a fault condition occurs. This causes the power amplifier to source or sink more current than the programmed limit value. IFLAG exhibits transient pulses under typical operation. An IFLAG true state for greater than 100 ms is a definite indication of a fault current condition.

The device contains internal thermal shutdown protection circuitry that automatically disables the output stage if the junction temperature exceeds 140°C. The device thermal shutdown protection circuitry lets the amplifier typical normal operation only when the junction temperature falls below 130°C. The TFLAG is active when the device is in thermal shut down mode.

## 7.4 Device Functional Modes

The OPA521 operates from a single power rail from 7 V to 24 V. The gain is fixed at –7 V/V and can increase with an external resistor that is connected to the GAIN_SET and –IN pins.


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# 8 Application and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The application circuit shown in 图 20 is an AC mains-line driver over 40-kHz-to-90-kHz utility band and is based around the European standard (EN56065–1) describing utility and consumer applications. This example shows a possible implementation for differential transmission on the mains line. This applications circuit is designed around the requirements of a domestic electricity meter operating over a utility band of 40 kHz to 90 kHz.

## 8.2 Typical Application

The impedance of the mains network at these signaling frequencies is relatively low (< 1 Ω to 30 Ω). This circuit has been designed to drive a 2-Ω mains line over the 40-kHz-to-90-kHz bandwidth. The signaling impedance of the mains network fluctuates as different loads are switched on during the day or over a season and it is influenced by many factors such as:

- Localized loading from appliances connected to the mains supply near to the connection of the communication equipment; for example, heavy loads such as cookers and immersion heaters and reactive loads such as EMC filters and power factor corrections.
- Distributed loading from consumers connected to the same mains cable, where their collective loading reduces the mains signaling impedance during times of peak electricity consumption; for example, meal times.
- Network parameters; for example, transmission properties of cables and the impedance characteristics of distribution transformers and other system elements.

With such a diversity of factors, the signaling environment fluctuates enormously, irregularly, and can differ greatly from one installation to another. Design the signaling system for reliable communications over a wide range of mains impedances and signaling conditions. Consequently, the transmitter must be able to drive sufficient signal into the mains network under these loading conditions.

The OPA521 amplifier has 1.9-A output drive capability with short-circuit protection; hence, it adequately copes with the high current demands required for implementing mains signaling systems.

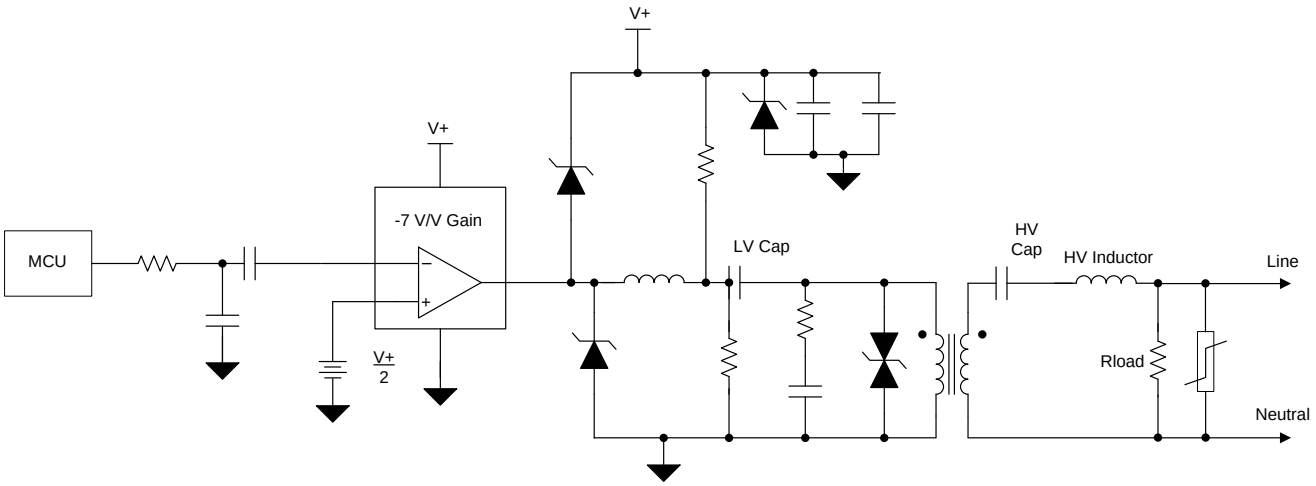



**图 20. OPA521 Interface to the AC Mains**

## Typical Application (接下页)

### 8.2.1 Design Requirements

The primary subsystems of a power-line communication mains-line driver system include the line coupling circuit, circuit protection, and power supply. The following sections detail the design of each.

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Interfacing the OPA521 to the AC Mains*

The line coupling circuit is one of the most critical segments of a power-line modem. The line coupling circuit has two primary functions: first, to prevent the high voltage, low frequency of the mains (commonly 50 Hz or 60 Hz) from damaging the low-voltage modem circuitry; and second, as the name implies, to couple the modem signal to and from the ac mains.

##### 8.2.2.1.1 Low-Voltage Capacitor

The low-voltage capacitor (LV Cap) couples the time-varying components of the power amplifier output signal into the line coupling transformer. The LV Cap must have a large enough capacitance to appear as a low impedance throughout the signal band of interest; 10-μF is a common value for signals in the range of 35 kHz to 150 kHz. The voltage rating of the LV cap should be sufficient to withstand the clamping voltage of the TVS diode (that is, the transient voltage suppressor (see Circuit Protection more information) operating under surge conditions. Generally, this limit must be equal to the power amplifier supply voltage or slightly higher.

##### 8.2.2.1.2 High-Voltage Capacitor

The high-voltage capacitor (HV Cap) blocks the low-frequency mains voltage by forming a voltage divider with the winding inductance of the line coupling transformer. In many applications, a maximum reactive power (VA limit) on the HV Cap may be required. To meet this requirement, the HV Cap value is calculated by 公式 1.

$$HV_{CAP} = \frac{VA_{LIMIT}}{V_{AC^2} \times 2\pi \times f} \tag{1}$$

For a 240-VAC, 50-Hz application with a 10-VA limit, the maximum value for the HV Cap is shown in 公式 2.

$$HV_{CAP} \leq \frac{10}{240^2 \times 2\pi \times f} = 550 \text{ nF} \tag{2}$$

A 470-nF capacitor is frequently used in these types of applications. A metallized polypropylene electromagnetic interference and radio frequency interference (EMI/RFI) suppression capacitor is recommended because of the low loss factor associated with the dielectric, which results in minimal internal self-heating. Operating the capacitor at approximately 80% of its ac-rated voltage ensures a long component operating life. See Circuit Protection of this document for additional discussion on selecting the correct HV Cap value to withstand impulses on the mains.

##### 8.2.2.1.3 Inductor

The inductor that is connected in series with the HV Cap is required when driving low line impedances and the HV Cap is restricted to approximately 470 nF for the reasons previously stated. In applications that operate in the CENELEC A band, the impedance of the 470-nF capacitance at 40 kHz is approximately 8.5 Ω. If the application requires the ability to drive a 2-Ω load, for example, this series impedance is restrictive. Adding the series inductor can mitigate this effect. To properly select the value of the inductance, the operating frequency range of the system must be known. A common example would be the PRIME frequency band, which is approximately 40 kHz to 90 kHz. Selecting the HV Cap and inductor to have a resonant frequency in the center of the frequency band is recommended, and results in a series inductor value of 12.8 μH and HV Cap value of 470 nF. The inductor must be sized to be capable of withstanding the maximum load current without saturation, using this 公式 3 as a guideline.

$$L = \frac{1}{\left(HV_{CAP} \times 2\pi \times f\right)^2} \tag{3}$$


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## Typical Application (接下页)

#### 8.2.2.1.4 Line Coupling Transformer

Most power-line communication transformers are compact, with turns ratios between 1:1 and 4:1, low leakage inductance, and approximately 1-mH of winding inductance. It is the voltage divider formed by the HV Cap and winding inductance that divides down the ac mains voltage and reduces it to negligible levels at the modem output. 图 21 shows the equivalent circuit formed with the HV Cap and the line coupling transformer.

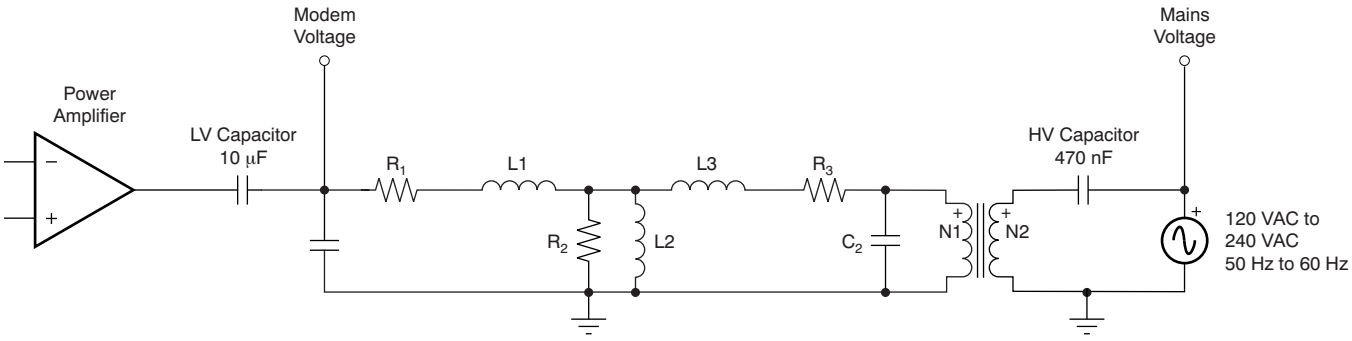
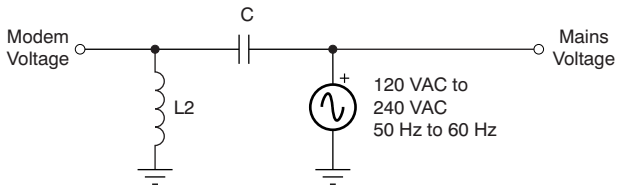



**图 21. Voltage Divider with HV Cap and Transformer Equivalent Circuit**

Where:

1. R1 is the series dc resistance of the primary winding
2. R2 is the shunt resistance reflecting losses in the core
3. R3 is the series dc resistance of the secondary winding, reflected to the primary side
4. L1 is the primary leakage inductance
5. L2 is the open circuit inductance of the primary winding
6. L3 is the secondary leakage inductance reflected to the primary side
7. C1 is the self-capacitance of the primary winding
8. C2 is the self-capacitance of the secondary winding reflected to the primary side

For the purposes of analysis, this circuit can be simplified as shown in 图 22.




HVCap reflected to the primary side

**图 22. Simplified AC Mains Voltage Divider**

Where:

1. L2 = OCL of the transformer primary
2. C = HV Cap reflected to the primary side

In a typical line coupling circuit the ac mains voltage injected into the modem is approximately 20 mVPP.

Determining the optimal turns ratio (N1/N2) for the power-line communication transformer is simple, and based on the principle of using the maximum output swing capability of the power amplifier together with the maximum output current capability of the power amplifier to achieve maximum power transfer efficiency into the load. Assuming the power-supply voltage and target load impedance are known, the turns ratio is determined as shown in Figure 17, and calculated with Equation 11 and Equation 12.

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## Typical Application (接下页)

### *8.2.2.2 Circuit Protection*

Power-line communications are often located in operating environments that are harsh for electrical components connected to the ac line. Noise or surges from electrical anomalies (such as lightning, capacitor bank switching, inductive switching, or other grid fault conditions) can damage high-performance integrated circuits if proper protection is not provided. The OPA521, however, can survive even the harshest conditions by using a variety of techniques to protect the device. Layout the protection circuitry in order to dissipate as much of the electrical disturbance as possible with a multilayer approach using metal-oxide varistors (MOVs), transient voltage suppression diodes (TVSs), Schottky diodes, and a Zener diode. These components dissipate the electrical disturbance before the anomaly reaches the device. shows the recommended strategy for transient overvoltage protection.

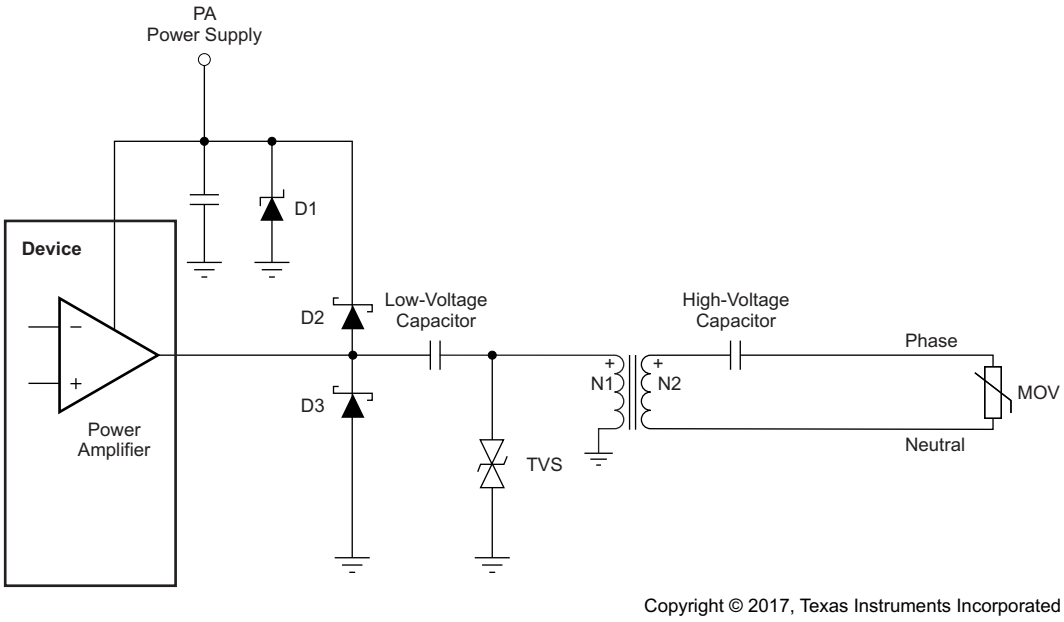



**图 23. Transient Overvoltage Protection for OPA521**

Note that the high-voltage coupling capacitor must be able to withstand pulses up to the clamping protection provided by the MOV. A metalized polypropylene capacitor, such as the 474MKP275KA from Illinois Capacitor, is rated for 50 Hz to 60 Hz and 250 VAC to 310 VAC, and can withstand 24 impulses of 2.5 kV. 表 2 lists several recommended transient protection components.

**表 2. Recommended Transient Protection Components**

| COMPONENT | DESCRIPTION | MANUFACTURER | MFR PART NO (OR EQUIVALENT) |
|---|---|---|---|
| D1 | Zener diode | Diodes, Inc. | 1SMB59xxB |
| D2, D3 | Schottky diode | Diodes, Inc. | 1N5819HW |
| TVS | Transient voltage suppressor | Diodec Semiconductor | P6SMBJxxC |
| MOV | Varistor (for 120 VAC, 60 Hz) | LittleFuse | TMOV20RP140E |
| MOV | Varistor (for 240 VAC, 50 Hz) | LittleFuse | TMOV20RP300E |
| HV Cap | High-voltage capacitor | Illinois Capacitor, Inc | 474MKP275KA |


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### 8.2.3 Application Curves

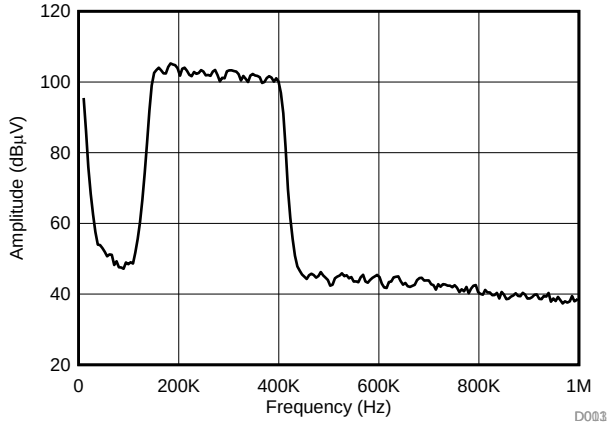



**图 24. Measured ARIB Emissions**

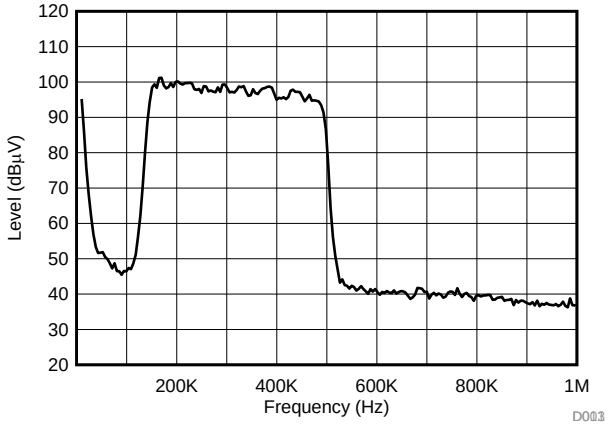



**图 25. Measured FCC Emissions**

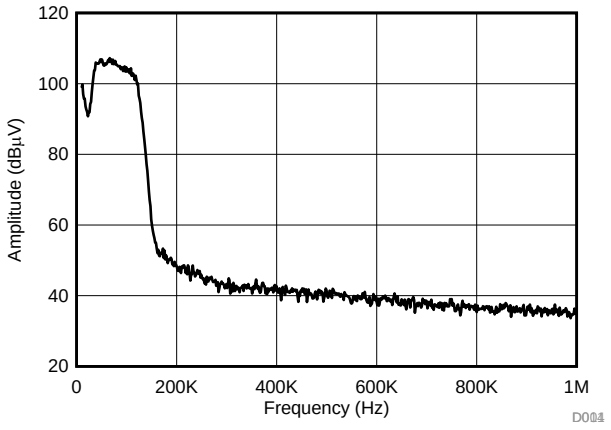



**图 26. Measured CENELEC Emissions**

## 9 Power Supply Recommendations

Determining the power-supply requirements requires only a straightforward analysis. The desired load voltage, load impedance, and available power-supply voltage or desired transformer ratio are all the parameters that must be known. In many power-line communication applications, such as PRIME, it is required to drive a 1-$V_{RMS}$ signal into a 2-Ω load. Using 图 27, calculate the minimum power-supply voltage required by adding the peak-to-peak load voltage; the voltage dropped across the HV Cap and inductor, V2; the voltage dropped across the LV Cap, V1; and twice the output swing to rail limit of the power amplifier, VSWING. For FSK and SFSK systems, the peak to average ratio is $\sqrt{2}$, while for OFDM systems this ratio is approximately 3:1.

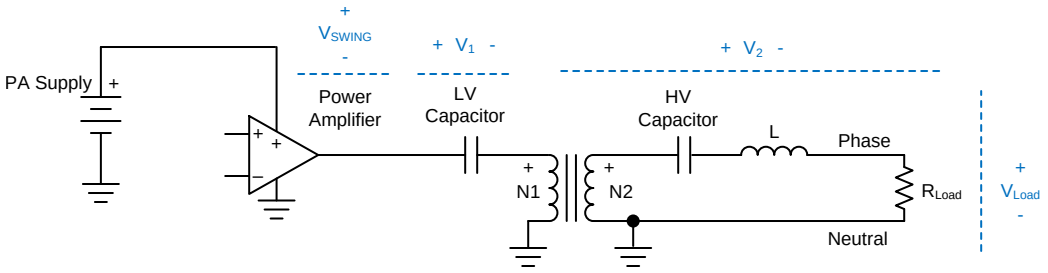



**图 27. Typical Line Coupling Circuit**

These ratios must be considered when performing calculations that relate the RMS voltages and peak voltages during an analysis. Choosing a large value for the LV Cap results in the voltage drop (V1) becoming negligible in most circumstances. The losses in the transformer are also negligible, even at high load currents, if the proper transformer with a low DCR is used. For FSK and SFSK systems, the voltage drop across the HV Cap and inductor, V2, is also usually negligible; in OFDM systems, because of the wider operating bandwidth, voltage drop V2 can be ignored and accounted for by using a 1.5× multiplier on the load voltage as an approximation.

**注**

This approximation is only valid with a load impedance of 2 Ω for PRIME and G3. Voltage drop V2 becomes negligible with increasing load impedance. These assumptions greatly simplify the analysis.

**表 3. Power-Supply Requirements**

| PARAMETER | FSK OR SFSK | PRIME OR G3 OFDM | UNIT |
|---|---|---|---|
| Frequency range | 63 to 74 | 35 to 95 | kHz |
| $R_{LOAD}$ | 2 | 2 | Ω |
| $V_{LOAD}$ | 1 | 1 | $V_{RMS}$ |
| $V_{LOAD}$ | 1.414 | 3 | $V_{PEAK}$ |
| $V_{LOAD}$ | 2.828 | 6 | $V_{PP}$ |
| OFDM multiplier | — | 1.5 | — |
| $V_{SWING}$ | 2 | 2 | V |
| Turns ration, N1/N2 | 1.5 | 1.5 | — |
| PA supply | 8.25 | 17.5 | V |

表 3 summarizes the power-supply requirements for various power-line communication systems.

Example:

For PRIME or G3 using an OFDM signal with a 2-Ω load and 1-$V_{RMS}$load voltage:

$PA_{Supply} = V_{LOAD} \times \text{OFDM Multiplier} \times \text{Turns Ration} + (2 \times V_{SWING})$

$PA_{Supply} = 6\ V \times 1.5 \times 1.5 + (2 \times 2\ V)$

$PA_{Supply} = 17.5\ V$

Power consumption


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Calculating the power dissipation in the load and in OPA521 also requires some direct calculations. The desired load voltage, load impedance, available power-supply voltage, and the transformer ratio are the only parameters required. In many power-line communication applications, such as PRIME, it is required to drive a 1-VRMS signal into a 2-Ω load. The power dissipation in the power amplifier is determined by calculating the RMS value of the OPA521's output current, and the voltage difference between the power amplifier supply and RMS value of the output voltage. These two values are multiplied, and the quiescent power of the power amplifier is added.

The power in the load is given as 公式 4 shows.

$$\text{PA output voltage (RMS)} = \frac{PA_{SUPPLY}}{2} + V_{LOAD_RMS} \times \frac{N_1}{N_2} \quad (4)$$

The power amplifier output current is given as calculated by 公式 5.

$$\text{PA power dissipation} = \text{voltage drop across PA} \times PA_{IOUT_RMS} \quad (5)$$

Because the output of the power amplifier is always symmetric around PASupply/2, only the voltage difference between the amplifier supply and the RMS values of the PA output must be considered. 图 28 illustrates this concept for an OFDM signal. 表 4 shows example power dissipation values.

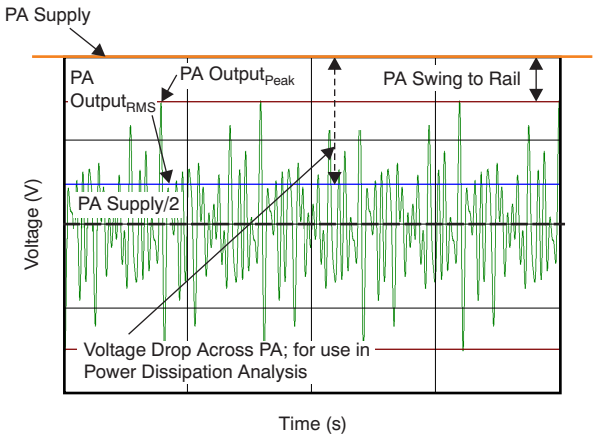



**图 28. Typical OFDM Output Waveforms**

**表 4. Power Dissipation**

| PARAMETER | FSK OR SFSK | PRIME OR G3 OFDM | UNITS |
|---|---|---|---|
| Turns ration, N1/N2 | 1.5 | 1.5 | - |
| $R_{LOAD}$ | 2 | 2 | Ω |
| $V_{LOAD}$ | 1 | 1 | $V_{RMS}$ |
| $I_{LOAD}$ | 0.5 | 0.5 | $A_{RMS}$ |
| PA output voltage | 6 | 10.75 | $V_{RMS}$ |
| Voltage drop across PA | 3 | 6.25 | $V_{RMS}$ |
| PA output current | 0.333 | 0.333 | $A_{RMS}$ |
| PA supply | 9 | 17 | V |
| PA power dissipation | 1 | 2.1 | W |
| Load power dissipation | 0.5 | 0.5 | W |
| Total | 1.5 | 2.6 | W |

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The power supply itself does not need to be designed to supply the peak power amplifier current continuously. The peak demand for current is supplied by the power-supply bypass capacitance. The power-supply voltage is shown in 图 29 on channel 2, along with the signal voltage at the 2-Ω load on channel 1.

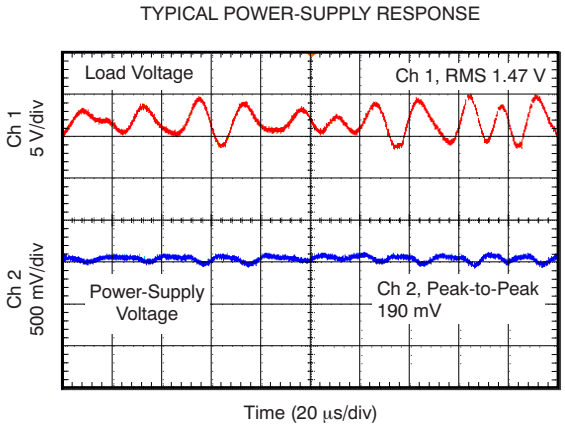



**图 29. Typical Power-Supply AC Response**

Two power-supply pins and two ground pins are available to provide a path for the high currents associated with driving the low impedance of the ac mains. Connecting the two supply pins together is recommended. Placing a 47-μF to 100-μF bypass capacitor in parallel with a 100-nF capacitor as close as possible to the device is also recommended. Care must be taken when routing the high-current ground lines on the PCB to avoid creating voltage drops in the PCB ground that may vary with changes in load current. /


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# 10 Layout

## 10.1 Layout Guidelines

### 10.1.1 Thermal Considerations

In a typical power line communications application, the device dissipates 2 W of power when transmitting to the low-impedance AC line. This amount of power dissipation can increase the junction temperature, which can lead to a thermal overload that results in signal transmission interruptions if the PCB thermal design is not implemented properly. Proper management of heat flow from the device and good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend the operating life of the device.

The device is assembled in a 5-mm × 5-mm, QFN-20 package. This QFN package has a large exposed thermal pad on the underside that conducts heat away from the device and to the underlying PCB.

Some heat is conducted from the silicon die surface through the plastic packaging material and is transferred to the ambient environment. However, this route is not the primary thermal path for heat flow because plastic is a relatively poor conductor of heat. Heat flows across the silicon die surface to the bond pads through the wire bonds to the package leads, to the top layer of the PCB. While these paths for heat flow are important, the majority (nearly 80%) of the heat flows downward through the silicon die to the thermally-conductive die-attach epoxy and to the exposed thermal pad on the underside of the package (as shown in 图 30). Minimizing the thermal resistance of this downward path to the ambient environment maximizes the life and performance of the device.

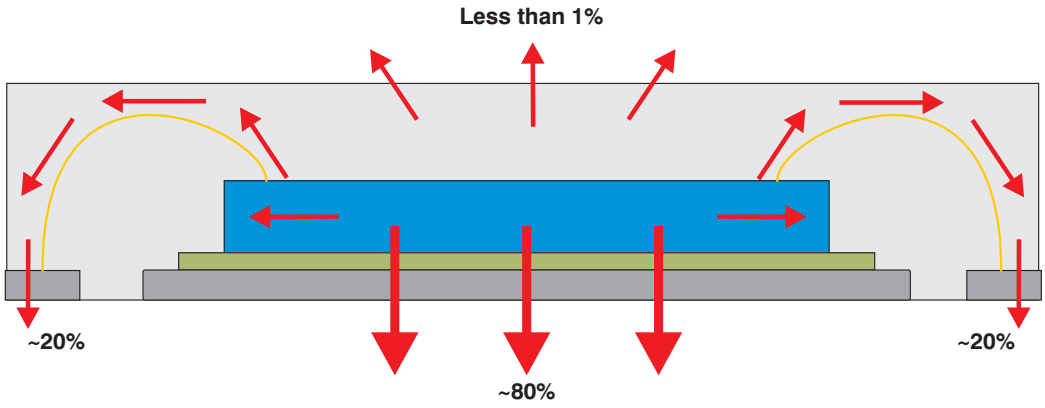



**图 30. Heat Flow in the QFN Package**

The exposed thermal pad must be soldered to the PCB thermal pad. The thermal pad on the PCB must be the same size as the exposed thermal pad on the underside of the QFN package. See *QFN/SON PCB Attachment* for recommendations on attaching the thermal pad to the PCB. 图 31 shows the direction of heat spreading to the PCB from the device.

## Layout Guidelines (接下页)

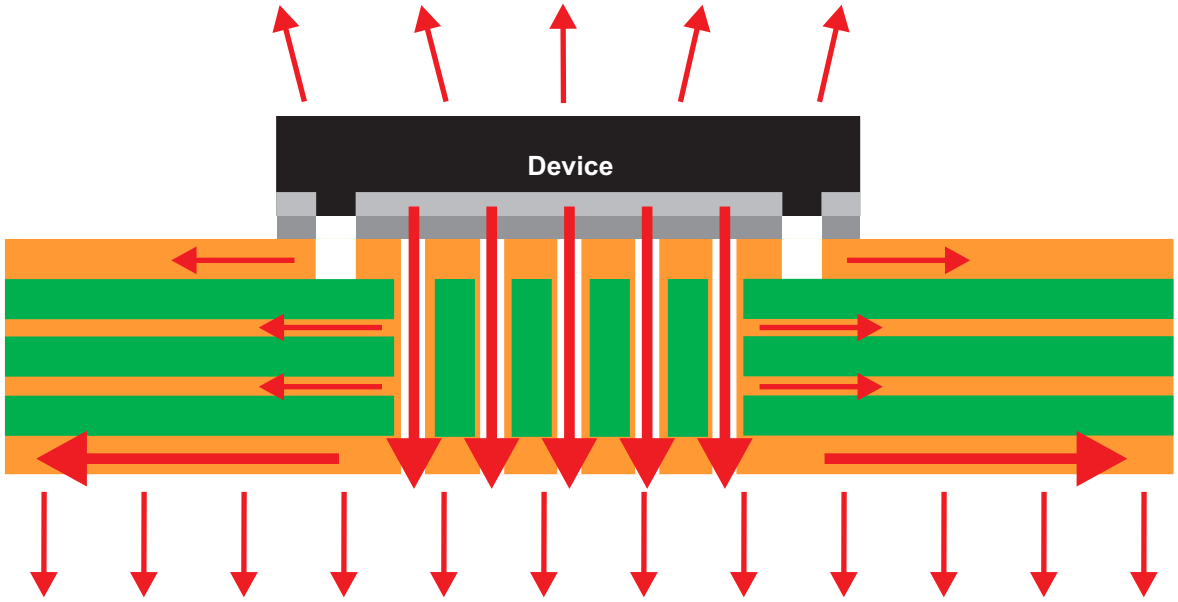



**图 31. Heat Spreading to PCB**

The heat spreading to the PCB is maximized if the thermal path is uninterrupted. Best results are achieved if the heat-spreading surfaces are filled with copper to the greatest extent possible, which maximizes the percentage of area covered on each layer. As an example, a thermally robust, multilayer PCB design consists of four layers with copper (Cu) coverage of 60% in the top layer, 85% and 90% in the inner layers (respectively), and 95% on the bottom layer.

Increasing the number of layers in the PCB, using thicker copper, and increasing the PCB area are all factors that improve the spread of heat. 图 32 through 图 34 show thermal resistance performance as a function of each of these factors.

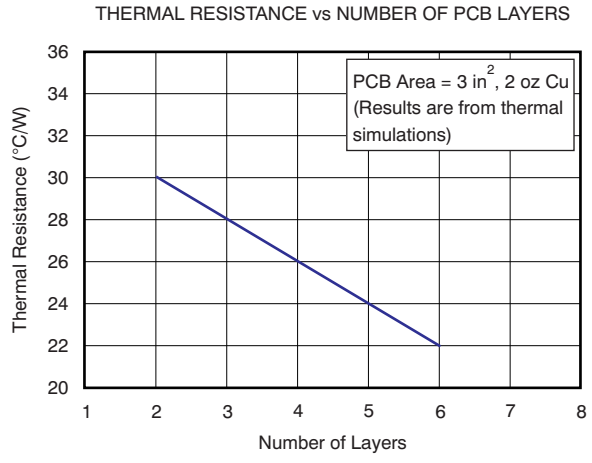



**图 32. Thermal Resistance as a Function of the Number of Layers in the PCB**

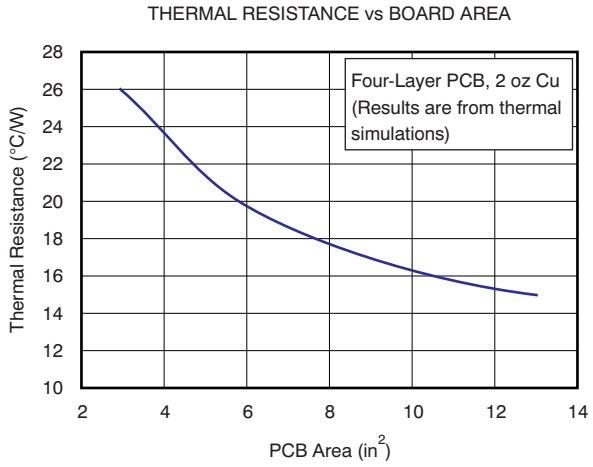



**图 33. Thermal Resistance as a Function of PCB Area**



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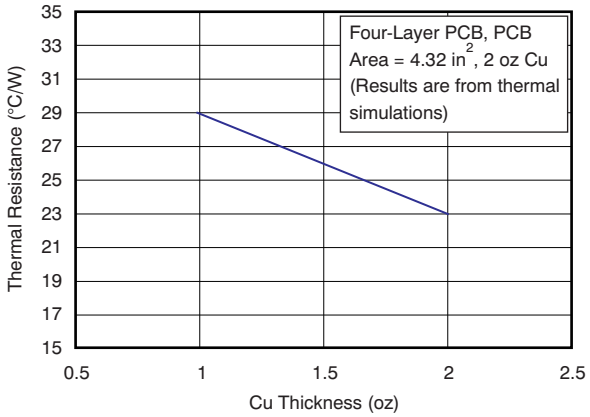



**图 34. Thermal Resistance as a Function of Copper Thickness**

For additional information on thermal PCB design using exposed thermal pad packages, see *PowerPAD™ Thermally-Enhanced Package* (available for download at www.ti.com).

## 10.2 Layout Example

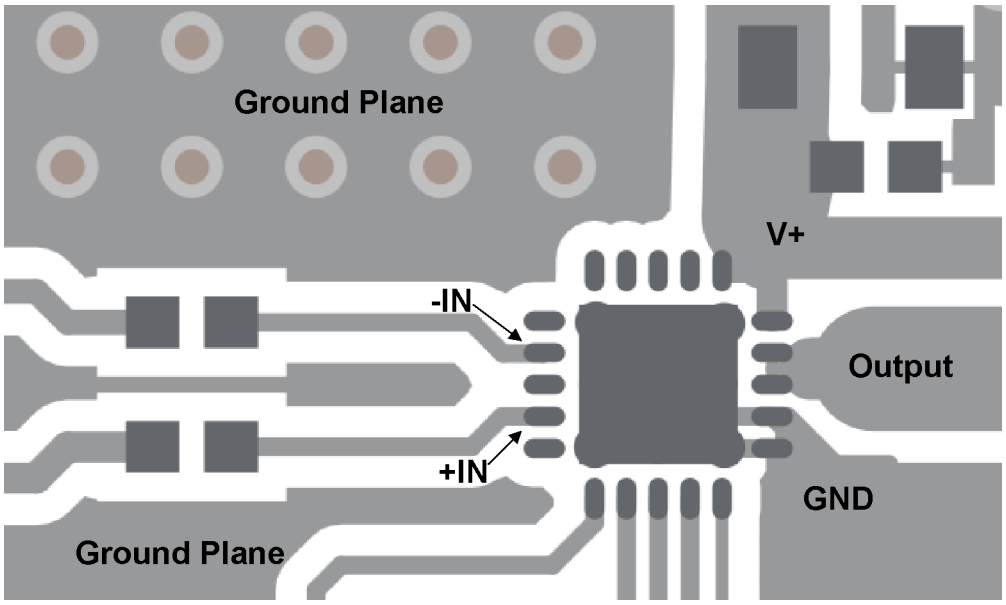



**图 35. Recommended Layout for Typical Transformer Coupling Application**

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 第三方产品免责声明

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## 11.2 文档支持

### 11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《PowerPAD™ 热增强型封装》*
- 德州仪器 (TI)*《QFN/SON PCB 连接》*

## 11.3 接收文档更新通知

要接收文档更新通知，请在 ti.com.cn 上查找器件产品文件夹。请单击右上角的*通知我* 进行注册，即可接收产品信息更改每周摘要。有关更改的详细信息，请阅读任何已修订文档中包含的修订历史记录。

## 11.4 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

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**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 11.5 商标

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## 11.6 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 12 "机械、封装和可订购信息

以下页面显示机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航栏。


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA521IRGWR | ACTIVE | VQFN | RGW | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 521 | Samples |
| OPA521IRGWT | ACTIVE | VQFN | RGW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA 521 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

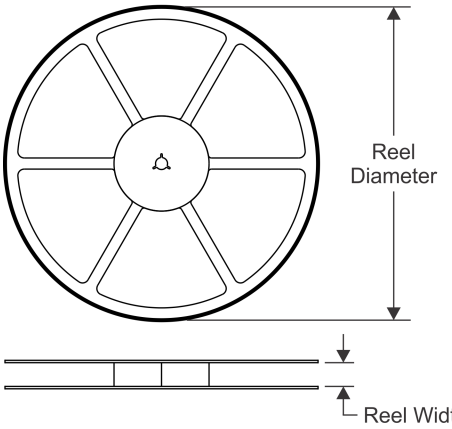
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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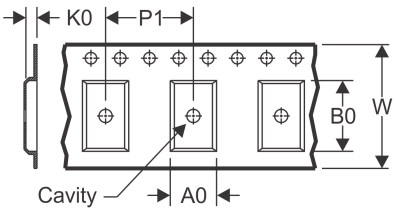
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

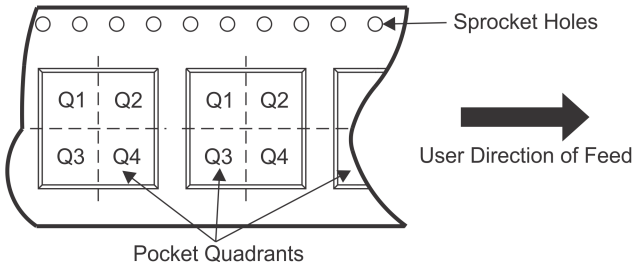



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

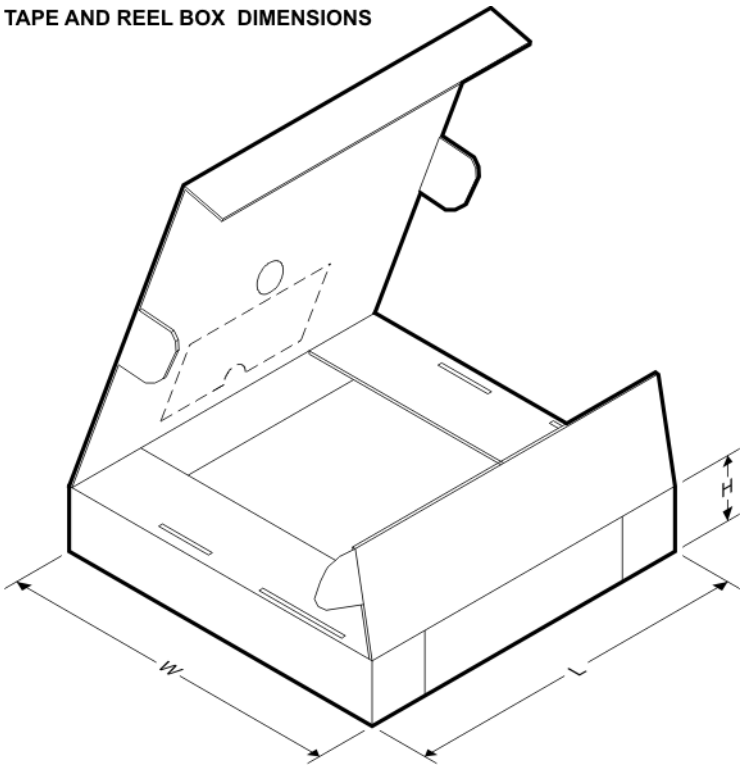
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA521IRGWR | VQFN | RGW | 20 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| OPA521IRGWT | VQFN | RGW | 20 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

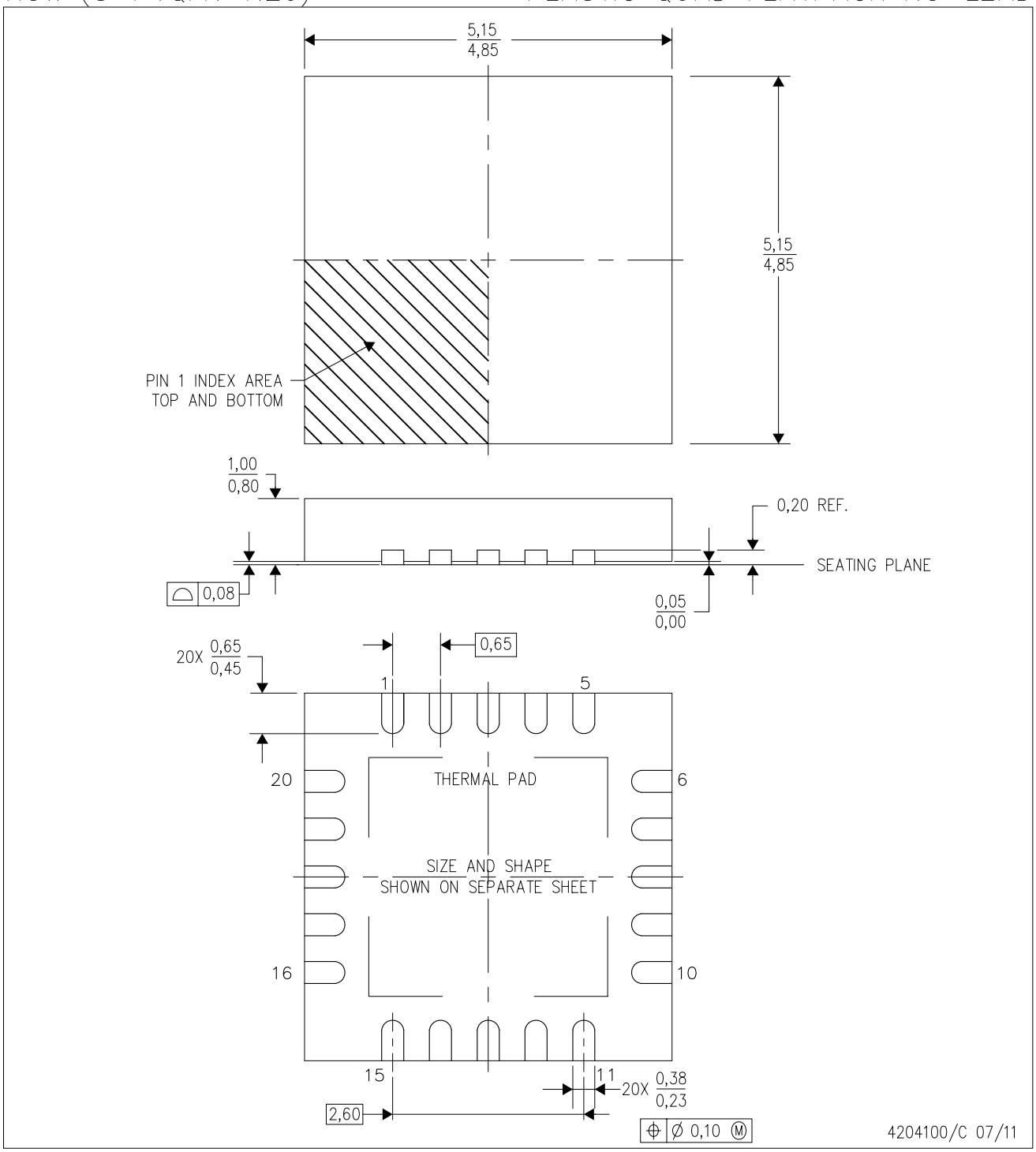
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA521IRGWR | VQFN | RGW | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| OPA521IRGWT | VQFN | RGW | 20 | 250 | 210.0 | 185.0 | 35.0 |

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

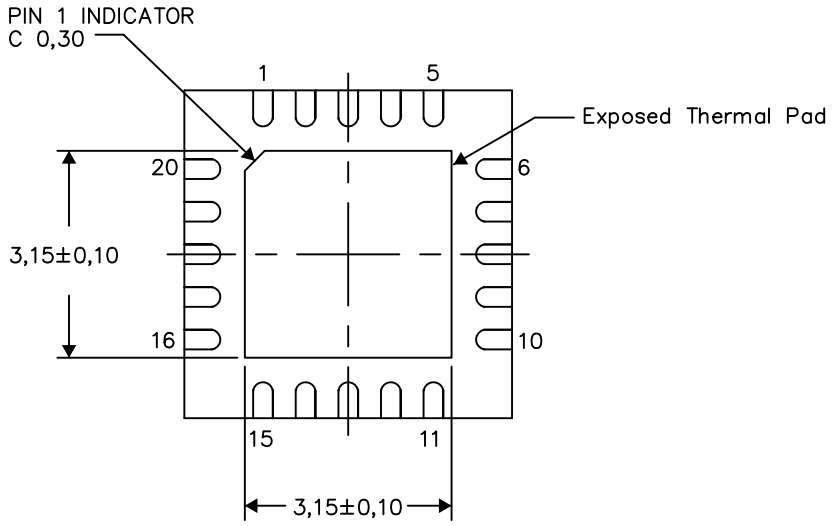
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



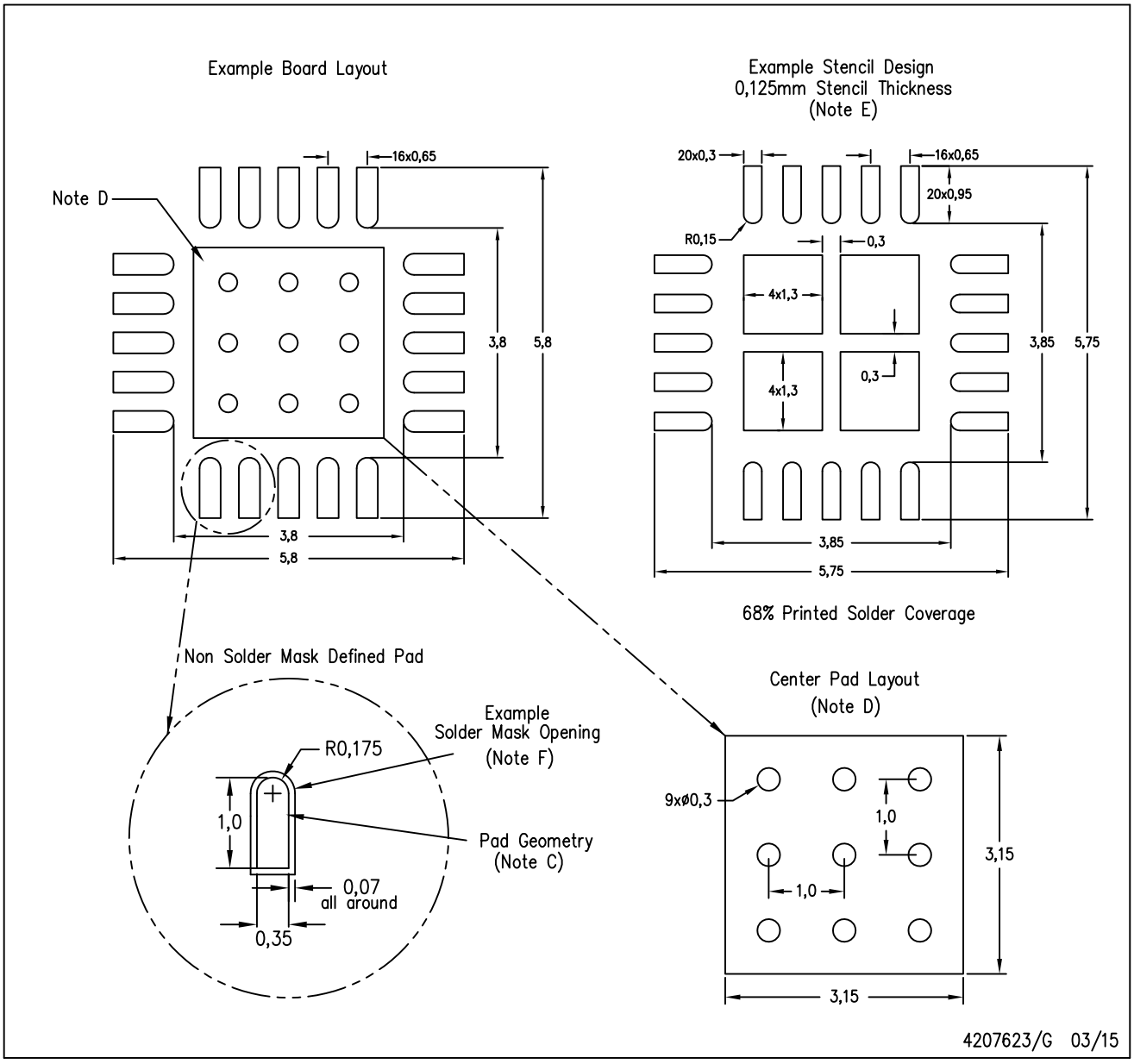

Bottom View

Exposed Thermal Pad Dimensions

4206352–2/M 06/15

NOTE: All linear dimensions are in millimeters

# RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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