High Voltage, Isolated IGBT Gate Driver with Fault Detection

Data Sheet

ADuM4137

FEATURES

- 6 A peak drive output capability
- Internal turn off NFET, on resistance: <0.95 Ω
- Internal turn on PFET, on resistance: <1.18 Ω
- Split emitter overcurrent detection
- Miller clamp output with gate sense input
- Isolated fault output
- Isolated temperature sensor read back
- Propagation delay
  - Rising: 105 ns typical
  - Falling: 107 ns typical
- Minimum pulse width: 70 ns
- Operating junction temperature range (−40°C to +150°C)
- V_{DD1} and V_{DD2} UVLO
- ASC input
- 8.3 mm creepage distance
- Safety and regulatory approvals
  - 5 kV rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
- V_{IORM} = 849 V_{PEAK} (reinforced/basic)
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- MOSFET/IGBT gate drivers
- Photovoltaic (PV) inverters
- Motor drives
- Power supplies

GENERAL DESCRIPTION

The ADuM4137[1] is a single-channel gate driver specifically optimized for driving insulated gate bipolar transistors (IGBTs). Analog Devices, Inc., *i*Coupler® technology provides isolation between the input signal and the output gate drive.

The Analog Devices chip scale transformers also provide isolated communication of control information between the high voltage and low voltage domains of the chip. Information on the status of the chip can be read back from the dedicated fault outputs. The ADuM4137 provides isolated fault reporting for overcurrent events, remote temperature overheating events, undervoltage lockout (UVLO), and thermal shutdown (TSD).

Integrated onto the ADuM4137 is an overcurrent detection feature that protects the IGBT in case of overcurrent events. The split emitter overcurrent detection is coupled with a high speed, two-level turn off in case of faults.

The ADuM4137 provides a Miller clamp control signal for the external metal-oxide semiconductor field effect transistor (MOSFET) to provide robust IGBT turn off with a single rail supply when the gate voltage drops below 2.0 V (typical) and above GND_2. Operation with unipolar secondary supplies is possible, with or without the Miller clamp operation.

A low gate voltage detection circuit can trigger a fault if the gate voltage does not go above the internal threshold (V_{DVL}) within the time allowed from turn on (t_{DVL}). This circuit allows detection of IGBT device failures that exhibit gate shorts or other causes of weak drive.

The secondary falling UVLO is set to 11.24 V (typical) for common IGBT two-level plateau voltage levels.

The ADuM4137 provides for in field programming of temperature. Two temperature sensor pins allow isolated monitoring of system temperatures at the IGBTs, sensing diode gains and offsets by means of a serial port interface (SPI) bus on the primary side of the device. Values are stored on an EEPROM located on the secondary side. Additionally, programming is available for specific voltage offsets, temperature sensing reporting frequencies, and important delays.

The ASC pin on the secondary side on the ADuM4137 allows the driver to be switched on from the secondary side if no faults are present.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents pending.

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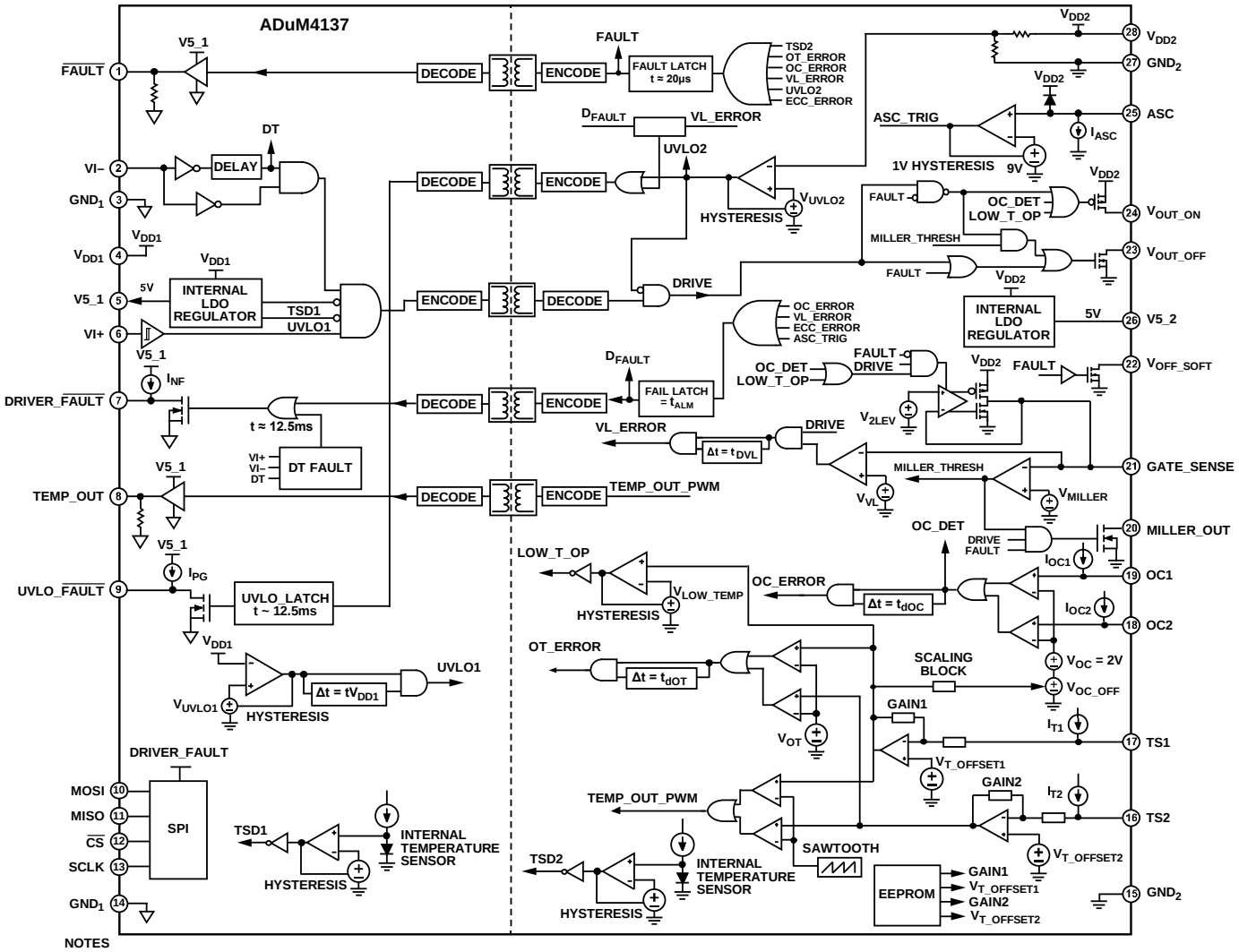
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REVISION HISTORY

2/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. VL_ERROR IS THE VOLTAGE LOW ERROR INTERNAL CONNECTION.
2. TEMP_OUT_PWM IS THE TEMPERATURE SENSE INTERNAL CONNECTION.
3. OC_ERROR IS THE OVERCURRENT ERROR INTERNAL CONNECTION.
4. OC_DET IS THE OVERCURRENT DETECTION INTERNAL CONNECTION.
5. V_{VL} IS THE GATE LOW VOLTAGE REFERENCE VOLTAGE.
6. ASC_TRIG IS THE ASC SIGNAL INTERNAL CONNECTION.
7. MILLER_THRESH IS THE MILLER CLAMP ACTIVATION INTERNAL CONNECTION.
8. OT_ERROR IS THE OVERTEMPERATURE ERROR INTERNAL CONNECTION.
9. $V_{T_OFFSET1}$ IS THE TEMPERATURE SENSE OFFSET VOLTAGE FOR THE TS1 PIN.
10. $V_{T_OFFSET2}$ IS THE TEMPERATURE SENSE OFFSET VOLTAGE FOR TS2 PIN.
11. I_{T1} IS THE INTERNAL CURRENT REFERENCE FOR TS1 PIN.
12. I_{T2} IS THE INTERNAL CURRENT REFERENCE FOR TS2 PIN.
13. V_{OC_OFF} IS THE OVERCURRENT VOLTAGE OFFSET DUE TO TEMPERATURE RAMP.
14. V_{OC} IS THE OVERCURRENT REFERENCE VOLTAGE.
15. I_{OC1} IS THE OC1 INTERNAL PULL-UP CURRENT SOURCE.
16. I_{OC2} IS THE OC2 INTERNAL PULL-UP CURRENT SOURCE.
17. V_{UVLO1} IS THE VDD1 UVLO REFERENCE.
18. V_{UVLO2} IS THE VDD2 UVLO REFERENCE.
19. V_{LOW_TEMP} IS THE LOW TEMPERATURE OPERATION REFERENCE.
20. V_{2LEV} IS THE TARGET VOLTAGE REFERENCE FOR TWO LEVEL OPERATION.
21. LOW_T_OP IS THE LOW TEMPERATURE OPERATION TRIGGER.
22. DT IS THE DEADTIME INTERNAL CONNECTION.
23. D_{FAULT} IS THE DRIVE FAULT INTERNAL CONNECTION.
24. UVLO_LATCH IS THE UNDERVOLTAGE LOCKOUT LATCH TIMER.
25. GAIN1 IS THE REMOTE TEMPERATURE SENSE USER TRIMMABLE GAIN FOR TS1.
26. GAIN2 IS THE REMOTE TEMPERATURE SENSE USER TRIMMABLE GAIN FOR TS2.
27. TSD1 IS THE PRIMARY SIDE THERMAL SHUTDOWN COMMAND.
28. TSD2 IS THE SECONDARY SIDE THERMAL SHUTDOWN COMMAND.
29. V_{MILLER} IS THE MILLER CLAMP REFERENCE VOLTAGE.
30. I_{NF} IS THE DRIVER_FAULT INTERNAL PULL-UP CURRENT SOURCE.
31. I_{PG} IS THE UVLO_FAULT INTERNAL PULL-UP CURRENT SOURCE.
32. V_{OT} IS THE TEMPERATURE SENSE OVERTEMPERATURE REFERENCE.
33. I_{ASC} IS THE ASC PIN INTERNAL PULL-UP CURRENT SOURCE.
34. ECC_ERROR IS THE ERROR CORRECTING CODE INTERNAL CONNECTION.
35. t_{ALM} IS THE FAULT LATCH HOLD TIME.
36. UVLO1 IS THE PRIMARY SIDE UVLO INTERNAL CONNECTION.
37. UVLO2 IS THE SECONDARY SIDE UVLO INTERNAL CONNECTION.

Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to GND_1, high-side voltages referenced to GND_2, V_{DD1} = 12 V, V_{DD2} = 15 V, T_J = −40°C to +150°C, unless otherwise noted. All minimum and maximum specifications apply over the entire recommended operating temperature range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 12 V, and V_{DD2} = 15 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
High-Side Power Supply						
Input Voltage, Secondary Side	V_{DD2}	12		25	V	
V_{DD2} Input Current, Quiescent	$I_{DD2\ (Q)}$	9.8	11.5	16.0	mA	TS1 = TS2 = open, VI+ = 0 V, VI− = 5 V, V_{DD2} = 25 V
		12.8	15.2	20.0	mA	TS1 = TS2 = 2 V, VI+ = 5 V, VI− = 0 V, V_{DD2} = 25 V
V5_2 Regulated Output Voltage	V_{V5_2}	4.9	5.0	5.1	V	Unloaded
Logic Supply						
Input Voltage, Primary Side	V_{DD1}	4.5		25	V	
V_{DD1} Input Current	I_{DD1}	2.8	3.8	4.7	mA	TS1 = TS2 = open, VI+ = 0 V, VI− = 5 V, TEMP_OUT floating, V_{DD1} = 4.5 V, V_{DD2} = 15 V
		3.3	6.3	8.5	mA	TS1 = TS2 = 2 V, VI+ = 5 V, VI− = 0 V, TEMP_OUT floating, V_{DD1} = 25 V, V_{DD2} = 15 V
V5_1 Regulated Output Voltage	V_{V5_1}	4.9	5.0	5.1	V	Unloaded
Logic Inputs, VI+, VI−, $\overline{CS}$, MOSI, SCLK						
Input Current (VI+, VI−, $\overline{CS}$, MOSI, SCLK Only)	I_I	−0.1	+0.01	+0.1	µA	
Input Voltage						
Logic High	V_{IH}			2.5	V	V_{DD1} ≥ 6 V
				2.2	V	4.5 V ≤ V_{DD1} ≤ 6 V
Logic Low Input Voltage	V_{IL}	0.9			V	V_{DD1} ≥ 6 V
		0.85			V	4.5 V ≤ V_{DD1} ≤ 6 V
Logic Input Hysteresis	V_{HYST}		1.11		V	V_{DD1} ≥ 6 V
			1.02		V	4.5 V ≤ V_{DD1} ≤ 6 V
UVLO_$\overline{FAULT}$						
Logic High Input Voltage	$V_{IH_\overline{F}}$			2.82	V	V_{DD1} ≥ 6 V
				2.56	V	4.5 V ≤ V_{DD1} ≤ 6 V
Logic Low Input Voltage	$V_{IL_\overline{F}}$	1.62			V	V_{DD1} ≥ 6 V
		1.46			V	4.5 V ≤ V_{DD1} ≤ 6 V
Logic Input Hysteresis	$V_{HYS_\overline{F}}$		0.93		V	V_{DD1} ≥ 6 V
			0.84		V	4.5 V ≤ V_{DD1} ≤ 6 V
MISO Logic Output						
MISO N Channel Field Effect Transistor (NFET) Drain to Source On Resistance (R_{DSON})	$R_{DSON_MISO_N}$		9	20	Ω	MISO current (I_{MISO}) = 5 mA, V_{DD1} = 4.5 V
MISO P Channel Field Effect Transistor (PFET) R_{DSON}	$R_{DSON_MISO_P}$		13	30	Ω	I_{MISO} = 5 mA, V_{DD1} = 4.5 V
MISO NFET High-Z Leakage	$I_{MISO_LK_N}$	−0.1	+0.01	+0.1	µA	MISO = 0 V
MISO PFET High-Z Leakage	$I_{MISO_LK_P}$	−0.1	+0.01	+0.1	µA	MISO = 5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
UVLO						
Positive Going Threshold						
V_{DD1}	$V_{VDD1UV+}$		4.25	4.50	V	
V_{DD2}	$V_{VDD2UV+}$		11.57	11.72	V	
Negative Going Threshold						
V_{DD1}	$V_{VDD1UV-}$	4.0	4.17		V	
V_{DD2}	$V_{VDD2UV-}$	11.0	11.24		V	
Hysteresis						
V_{DD1}	$V_{VDD1UVH}$		0.1		V	
V_{DD2}	$V_{VDD2UVH}$		0.33		V	
PROTECTION FEATURES						
DRIVER_$\overline{\text{FAULT}}$						
DRIVER_$\overline{\text{FAULT}}$ Pull-Up Current Source	$I_{PU_D\overline{F}}$	71	78	84	µA	Tested at 0 V
DRIVER_$\overline{\text{FAULT}}$ R_{DSON}	$R_{ON_D\overline{F}}$		17	40	Ω	Tested at 5 mA, V_{DD1} = 4.5 V
UVLO_$\overline{\text{FAULT}}$						
UVLO_$\overline{\text{FAULT}}$ Pull-Up Current Source	$I_{PU_U\overline{F}}$	71	78	85	µA	Tested at 0 V
UVLO_$\overline{\text{FAULT}}$ R_{DSON}	$R_{ON_U\overline{F}}$		14	34	Ω	Tested at 5 mA, V_{DD1} = 4.5 V
$\overline{\text{FAULT}}$						
$\overline{\text{FAULT}}$ P Type Metal-Oxide Semiconductor (PMOS)	$R_{\overline{F}LT_PMOS}$		4.18	8.35	Ω	Tested at 20 mA, V_{DD1} = 4.5 V
$\overline{\text{FAULT}}$ N Type Metal-Oxide Semiconductor (NMOS)	$R_{\overline{F}LT_NMOS}$		5.11	10.15	Ω	Tested at 20 mA, V_{DD1} = 4.5 V
Pull-Down	$R_{\overline{F}LT_PD}$	0.84	1.11	1.38	MΩ	
Low Gate Voltage						
Reference Voltage	V_{VL}	9.68	9.92	10.11	V	V_{DD2} = 15 V
Fault Delay Time	t_{DVL}	11.18	12.73	14.67	µs	V_{DD2} = 15 V
Fault Delay Time	t_{DVL_FLT}	570	723	890	ns	To $\overline{\text{FAULT}}$
		560	721	920	ns	To DRIVER_$\overline{\text{FAULT}}$
		4740	6767	9700	ns	To UVLO_$\overline{\text{FAULT}}$
Overcurrent						
Voltage						
Temperature Ramp Disabled	V_{OCD_TH}	1.9	2	2.1	V	T_RAMP_OP = 1
Temperature Ramp Enabled	$V_{OCD_TH_EN}$	2.59	2.7	2.8	V	T_RAMP_OP = 0, TS1 = 1.55 V
		1.85	1.96	2.1	V	T_RAMP_OP = 0, TS1 = 2.25 V
		1.65	1.75	1.82	V	T_RAMP_OP = 0, TS1 = 2.45 V
Hysteresis						
Temperature Ramp Disabled	V_{OCD_HYST}		0.17		V	T_RAMP_OP = 1
Temperature Ramp Enabled	$V_{OCD_HYST_EN}$		0.17		V	T_RAMP_OP = 0, TS1 = 1.55 V
			0.17		V	T_RAMP_OP = 0, TS1 = 2.25 V
			0.17		V	T_RAMP_OP = 0, TS1 = 2.45 V
OC1 Pull-Up Current Source	I_{OC1_PU}	3.8	5	6.2	µA	
OC2 Pull-Up Current Source	I_{OC2_PU}	3.8	5	6.2	µA	
Detect Delay Time	t_{dOC}	650	787	936	ns	OC_2LEV_OP = 0, OC_TIME_OP = 0
Time to Report Overcurrent Fault to $\overline{\text{FAULT}}$ Pin	t_{REPORT}	570	725	900	ns	OC_2LEV_OP = 1, to $\overline{\text{FAULT}}$
		420	724	1020	ns	OC_2LEV_OP = 1, to DRIVER_$\overline{\text{FAULT}}$
Detect Blanking	t_{BLANK}	300	360	445	ns	t_{BLANK} bits = 0001

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ASC						
ASC Detect Comparator Voltage	V_{ASC}	8.43	8.93	9.34	V	
Hysteresis	V_{ASC_HYS}		0.85		V	
Internal Current Source	I_{ASC}	130	153	178	µA	ASC = 2 V
ASC Filter	t_{ASC_F}		53	104	ns	
Time to Report ASC	t_{ASC}	360	537	820	ns	
TSD						
Primary Side TSD						
Positive Edge	t_{TSD_POS1}		154		°C	
Negative Edge	t_{TSD_NEG1}		135		°C	
Secondary Side TSD						
Positive Edge	t_{TSD_POS2}		150		°C	
Negative Edge	t_{TSD_NEG2}		130		°C	
Isolated Temperature Sensor						
Temperature Sense						
Bias Current Source	I_{T1}	0.90	1.0	1.11	mA	TS1 = 2.2 V
	I_{T2}	0.92	1.0	1.12	mA	TS2 = 2.2 V
Matching	I_{T_MATCH}		0.011	0.074	mA	TSx = 2.2 V
Pulse-Width Modulation (PWM) Output Frequency	f_{PWM}	9.3	10.0	10.7	kHz	PWM_OSC = 0, TSx = 2.25 V
		46.4	50.0	53.0	kHz	PWM_OSC = 1, TSx = 2.25 V
PWM Duty Cycle						
		8.1	10.2	11.4	%	PWM_OSC = 0, TSx = 2.45 V
		26.5	28.4	29.8	%	PWM_OSC = 0, TSx = 2.25 V
		90.6	92.1	93.5	%	PWM_OSC = 0, TSx = 1.55 V
		8.0	10.3	12.4	%	PWM_OSC = 1, TSx = 2.45 V
		26.1	28.5	30.9	%	PWM_OSC = 1, TSx = 2.25 V
		89.7	92.0	94.2	%	PWM_OSC = 1, TSx = 1.55 V
Duty Cycle						
Minimum		0.67	1.3	2.05	%	TS1 = 3.0 V
Maximum		98.5	99	99.2	%	TS1 = 0 V
Overtemperature						
Detect Delay Time	t_{DOT}	0.9	1.00	1.14	ms	
Fault Delay Time	t_{DOT_FLT}	530	715	920	ns	
Detection Voltage						
Rising	$V_{OT_0_R}$	1.62	1.69	1.75	V	OT_FAULT_SEL = 0
	$V_{OT_1_R}$	1.67	1.73	1.79	V	OT_FAULT_SEL = 1
Falling	$V_{OT_0_F}$	1.59	1.64	1.70	V	OT_FAULT_SEL = 0
	$V_{OT_1_F}$	1.63	1.68	1.74	V	OT_FAULT_SEL = 1
Hysteresis	$V_{OT_HYST_0_R}$		50		mV	OT_FAULT_SEL = 0
	$V_{OT_HYST_1_R}$		50		mV	OT_FAULT_SEL = 1
Low Temperature Threshold						
Rising	$V_{LOW_T_R}$	2.33	2.40	2.46	V	TS1 pin voltage
Falling	$V_{LOW_T_F}$	2.32	2.36	2.40	V	TS1 pin voltage
Hysteresis	$V_{LOW_HYST_T_F}$		40		mV	
TEMP_OUT Resistance						
NMOS R_{DSON}	R_{TEMP_N}		12	25	Ω	TEMP_OUT current (I_{TEMP_OUT}) = 20 mA, V_{DD1} = 4.5 V
PMOS R_{DSON}	R_{TEMP_P}		14	26	Ω	I_{TEMP_OUT} = 20 mA, V_{DD1} = 4.5 V
Pull-Down	R_{TEMP_PD}	0.9	1	1.3	MΩ	
Miller Clamp Voltage Threshold	V_{MILLER}	1.88	2.0	2.14	V	Referenced to GND_2

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Fault Reporting						
Latch Assert Time A	t_{LA_A}	10	13	16	ms	
Latch Assert Time B	t_{LA_B}	18	20	23	ms	
Latch Assert Time C	t_{LA_C}	23	26	30	ms	
DRIVE SPECIFICATIONS						
Internal NFET						
On Resistance	R_{DSON_N}		0.51	0.95	Ω	V_{OUT_OFF} current (I_{VOUT_OFF}) = 0.5 A, V_{DD1} = 6 V, V_{DD2} = 12 V
On Resistance 2 Level	$R_{DSON_N_2LEV}$		1.78	3.45	Ω	I_{VOUT_OFF} = 0.1 A, V_{DD1} = 6 V, V_{DD2} = 12 V
Internal PFET						
On Resistance	R_{DSON_P}		0.64	1.18	Ω	V_{OUT_ON} current (I_{VOUT_ON}) = 0.5 A, V_{DD1} = 6 V, V_{DD2} = 12 V
On Resistance 2 Level	$R_{DSON_P_2LEV}$		2.04	3.90	Ω	I_{VOUT_ON} = 0.1 A, V_{DD1} = 6 V, V_{DD2} = 12 V
Miller Pull-Down NFET	R_{DSON_MILLER}		4	10	Ω	Miller current (I_{MILLER}) = 10 mA
V_{OFF_SOFT} R_{DSON}	$R_{DSON_SOFT_OFF}$		15	33	Ω	V_{OFF_SOFT} current (I_{OFF_SOFT}) = 10 mA
Peak Current	I_{PEAKIP}		6		A	V_{DD2} = 15 V, 2 Ω external resistance
Two-Level Plateau Voltage	V_{2LEV}	11.67	11.89	12.05	V	
SWITCHING SPECIFICATIONS						
Pulse Width[1]	PW	70			ns	V_{DD2} = 15 V, V_{OUT_ON} = V_{OUT_OFF}, no load
Propagation Delay						
Rising[2]	t_{DLH}	78	105	131	ns	V_{DD2} = 15 V, V_{OUT_ON} = V_{OUT_OFF}, no load
Falling[2]	t_{DHL}	83	107	137	ns	V_{DD2} = 15 V, V_{OUT_ON} = V_{OUT_OFF}, no load
Dead Time	t_{DEXT}	0.91	1.00	1.11	µs	

[1] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

[2] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 0% level of the V_{OUT_ON} or V_{OUT_OFF} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{OUT_ON} or V_{OUT_OFF} signal. See Figure 13 for waveforms of propagation delay parameters.

SPI TIMING SPECIFICATIONS

SPI timing specifications are guaranteed by design. All devices are production tested with 200 kHz SPI communication.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_S	Time to first clock edge	8			µs
t_{DS}	Set period	1			µs
t_{DH}	Hold period	1			µs
t_{CLK}	Clock period	5			µs
t_H	Release time	8			µs
t_{HIGH}	Clock time high	100			ns
t_{LOW}	Clock time low	100			ns
t_{OV}	Output valid time			240	ns

SPI Timing Diagram

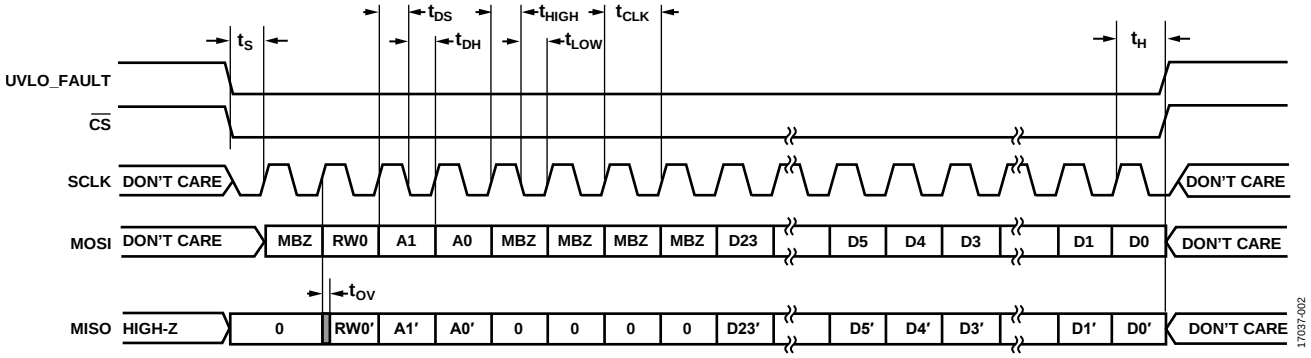


Figure 2. SPI Timing Diagram

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	

[1] The device is considered a 2-terminal device: Pin 1 through Pin 14 are shorted together, and Pin 15 through Pin 28 are shorted together.

REGULATORY INFORMATION

Table 4.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
UL 1577 Component Recognition Program Single Protection, 5000 V rms Isolation Voltage	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 830 V rms (1174 V_{PEAK}) Reinforced insulation at 415 V rms (587 V_{PEAK}) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (MOPP)), 519 V rms (734 V_{PEAK}) Reinforced insulation (2 MOPP), 261 V rms (369 V_{PEAK}) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation, 300 V rms mains, 830 V secondary (1174 V_{PEAK}) Reinforced insulation, 300 V rms mains, 415 V secondary (587 V_{PEAK})	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Reinforced insulation at 849 V_{PEAK}, V_{IOTM} = 8 kV_{PEAK}	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation, 830 V rms (1174 V_{PEAK}) Reinforced insulation, 415 V rms (587 V_{PEAK})
File E214100	File 205078	File 2471900-4880-0001	File (pending)

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.7	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V_{PEAK} working voltage.

Table 6. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per IEC 60664-1				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			1274	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1019	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8000	V_{PEAK}
Impulse	1.2 µs rise time, 50 µs, 50% fall time in air to the preferred sequence	$V_{IMPULSE}$	8000	V_{PEAK}
Surge Isolation Voltage Basic	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	9800	V_{PEAK}
Surge Isolation Voltage Reinforced	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at T_A = 25°C		P_S	2.0	W
Insulation Resistance at T_S	Voltage between the input and output (V_{IO}) = 500 V	R_S	$>10^9$	Ω

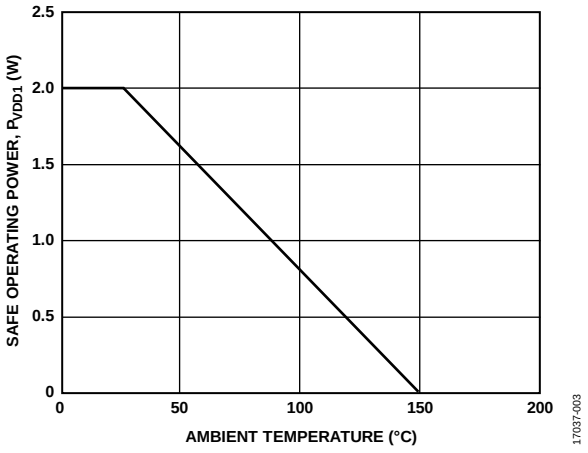


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values on Ambient Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Value
Operating Temperature Range (T_J)	−40°C to +150°C
Supply Voltages	
V_{DD1} [1]	4.5 V to 25 V
V_{DD2} [2]	12 V to 25 V

[1] Referenced to GND_1.
[2] Referenced to GND_2.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Junction Operating Temperature Range (T_J)	−40°C to +150°C
Supply Voltages	
V_{DD1}[1]	−0.2 V to +30 V
V_{DD2}[2]	−0.2 V to +30 V
Primary Side Pins[1]	
VI+, VI−, MOSI, $\overline{CS}$, SCLK	−0.2 V to +5.5 V
$\overline{FAULT}$, TEMP_OUT, MISO, DRIVER_$\overline{FAULT}$, UVLO_$\overline{FAULT}$	−0.2 V to V5_1 + 0.2 V
Secondary Side Pins[2]	
TS1, TS2	−0.2 V to V5_2 + 0.2 V
MILLER_OUT, V_{OFF_SOFT}, V_{OUT_OFF}	−0.2 V to +30 V
GATE_SENSE, OC1, OC2	−0.2 V to V_{DD2} + 0.2 V
V_{OUT_ON}, ASC	−0.2 V to V_{DD2} + 0.2 V
Common-Mode Transients (|CM|)	−150 kV/µs to +150 kV/µs

[1] Referenced to GND_1.
[2] Referenced to GND_2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top characterization parameter.

Table 9. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Unit
RN-28-1	62.4	2.97	°C/W

[1] 4-layer PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1, 2, 3]

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	707 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Unipolar Waveform		
Basic Insulation	1697 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	892 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
DC Voltage		
Basic Insulation	1092 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	546 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1

[1] See the Insulation Lifetime section for details.
[2] Other pollution degree and material group requirements yield a different limit.
[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

Table 11. Truth Table (Positive Logic)[1]

VI+ Input	VI− Input	ASC	$\overline{\text{FAULT}}$	DRIVER_$\overline{\text{FAULT}}$	UVLO_$\overline{\text{FAULT}}$	V_{DD1} State	V_{DD2} State	V_{OFF_SOFT}	V_{OUT_ON}	V_{OUT_OFF}
Low	High	<9 V	High	High	High	Powered	Powered	Low	Low	High
High	Low	<9 V	High	High	High	Powered	Powered	Low	High	Low
High	High	<9 V	High	High	High	Powered	Powered	Low	Low	High
Low	Low	<9 V	High	High	High	Powered	Powered	Low	Low	High
X	X	>9 V	High	Low	High	Powered	Powered	Low	High	Low
X	X	X	Low	X	X	Powered	Powered	High	X	Low[3]
X	X	X	X	Low	X	Powered	Powered	High[3, 4]	X	X
X	X	X	X	X	Low	Powered	Powered	High[3]	X	X
X	X	>9 V	X	X	X	Unpowered	Powered	Low	High	Low
X	X	<9 V	X	X	X	Unpowered	Powered	Low	Low	High
X	X	X	X	X	X	X	Unpowered	High-Z	High-Z	Low[2]

[1] X means don't care or unknown.
[2] With an unpowered V_{DD2}, the ADuM4137 tries to hold the IGBT gate voltage to a value of approximately 3 V to 5 V.
[3] The NMOS on V_{OUT_OFF} is off during soft shutdown until the GATE_SENSE pin reaches 2 V, then the V_{OUT_OFF} NMOS turns on along with the Miller clamp.
[4] The driver only goes into soft shutdown when an actual fault occurs, such as an overcurrent, gate low violation or an error correction code (ECC) error (see Table 12 for fault mapping).

Table 12. $\overline{\text{FAULT}}$ Pin Mapping

Fault Conditions	$\overline{\text{FAULT}}$ Pin	DRIVER_$\overline{\text{FAULT}}$ Pin	UVLO_$\overline{\text{FAULT}}$ Pin
TSD	Low, Latch Assert Time B = 20 ms (typical)	Don't care or unknown	Don't care or unknown
TSx_OT_FAULT	Low, Latch Assert Time B = 20 ms (typical)	Don't care or unknown	Don't care or unknown
Gate Low	Low, Latch Assert Time C = 26 ms (typical)	Low, Latch Assert Time C = 26 ms (typical)	Low, Latch Assert Time C = 26 ms (typical)
V_{DD2} UVLO	Low, Latch Assert Time B = 20 ms (typical)	Don't care or unknown	Low, Latch Assert Time A = 13 ms (typical)
OCx Overcurrent	Low, Latch Assert Time B = 20 ms (typical)	Low, Latch Assert Time C = 26 ms (typical)	Don't care or unknown
ECC Error	Low, Latch Assert Time B = 20 ms (typical)	Low, Latch Assert Time C = 26 ms (typical)	Don't care or unknown
ASC	Don't care or unknown	Low, Latch Assert Time C = 26 ms (typical)	Don't care or unknown
DT_FAULT	Don't care or unknown	Low, Latch Assert Time A = 13 ms (typical)	Don't care or unknown

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

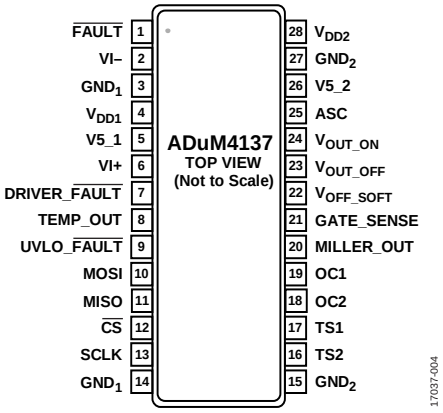


Figure 4. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{FAULT}}$	Fault Reporting Pin. When $\overline{\text{FAULT}}$ is low, the driver is disabled for as long as the $\overline{\text{FAULT}}$ pin persists or for the extent of the latch time, whichever is longer. See Table 11 for the $\overline{\text{FAULT}}$ reporting truth table.
2	VI–	Inverting Input with Dead Time Control.
3	GND_1	Ground Reference for the Primary Side.
4	V_{DD1}	Input Supply Voltage on the Primary Side, 4.5 V to 25 V Referenced to GND_1.
5	V5_1	5 V Regulated Output. Connect this pin to a 1 µF external capacitor referenced to GND_1. This pin controls logic levels for the input pins.
6	VI+	Noninverting Input.
7	DRIVER_$\overline{\text{FAULT}}$	Fault Reporting Pin. When an OCx fault, gate low fault, ECC fault, an ASC event, or DT_FAULT occurs, the DRIVER_$\overline{\text{FAULT}}$ pin is driven low on the primary side.
8	TEMP_OUT	10 kHz or 50 kHz, 1.3% to 99% (Typical) PWM Output for Diode Temperature Sensor.
9	UVLO_$\overline{\text{FAULT}}$	UVLO_$\overline{\text{FAULT}}$ Fault Reporting Pin. See Table 11 for the $\overline{\text{FAULT}}$ reporting truth table. When the UVLO_$\overline{\text{FAULT}}$ pin is pulled low externally, the SPI interface is activated.
10	MOSI	MOSI Connection for SPI Bus.
11	MISO	MISO Connection for SPI Bus.
12	$\overline{\text{CS}}$	Chip Select for SPI Bus.
13	SCLK	Clock for SPI Bus.
14	GND_1	Ground Reference for the Primary Side.
15	GND_2	Ground Reference for the Secondary Side.
16	TS2	Remote Temperature Sensor 2. Float or pull high to V5_2 if not used.
17	TS1	Remote Temperature Sensor 1. See the Applications Information section for more information if unused.
18	OC2	Split Emitter Overcurrent Detection 2. Connect this pin to GND_2 if not used.
19	OC1	Split Emitter Overcurrent Detection 1. Connect this pin to GND_2 if not used.
20	MILLER_OUT	Output Signal to Control External MOSFET for Miller Clamping.
21	GATE_SENSE	Miller Clamp Sense Pin. Connect this pin directly to the gate of the IGBT.
22	V_{OFF_SOFT}	Soft Shutdown Gate Connection. Connect this pin to the gate through the external series resistor. This pin pulls the gate down during fault conditions.
23	V_{OUT_OFF}	Turn Off Current Path Connection. Connect this pin to the gate through an external series resistor. This pin pulls the gate down during a low output command.
24	V_{OUT_ON}	Turn On Current Path Connection. Connect this pin to the gate through an external series resistor. This pin pulls the gate up during a high output command.
25	ASC	External Secondary Side Control for Enabling the Driver. The ASC pin has a comparator triggering at 8.93 V (typical) with 0.85 V (typical) of hysteresis. When the ASC signal is greater than 8.93 V (typical), the pin forces the driver on if no fault occurs.
26	V5_2	5 V Regulated Output on the Secondary Side. Connect this pin to a 1 µF external capacitor referenced to GND_2.
27	GND_2	Ground Reference for the Secondary Side.
28	V_{DD2}	Input Supply Voltage on the Secondary Side, Referenced to GND_2.

TYPICAL PERFORMANCE CHARACTERISTICS

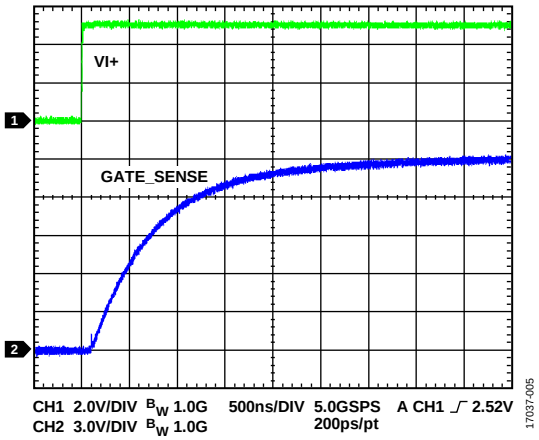


Figure 5. Example Turn On Edge, V_{DD1} = 5 V, V_{DD2} = 15 V, 3 Ω Turn On, 100 nF Load

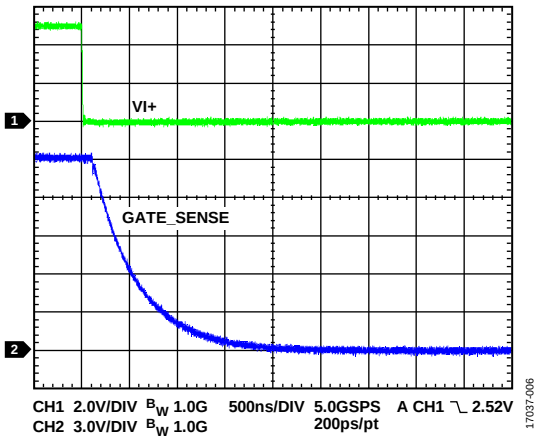


Figure 6. Example Turn Off Edge, V_{DD1} = 5 V, V_{DD2} = 15 V, 2 Ω Turn Off, 100 nF Load

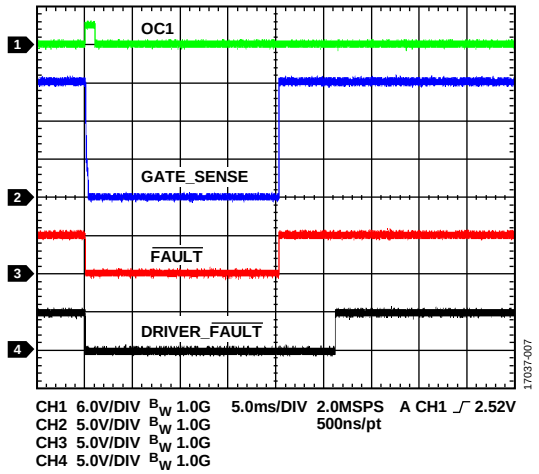


Figure 7. Example Overcurrent Fault, V_{DD1} = 5 V, V_{DD2} = 15 V, VI+ = 5 V, 1 ms Overcurrent Simulation, 100 nF Load

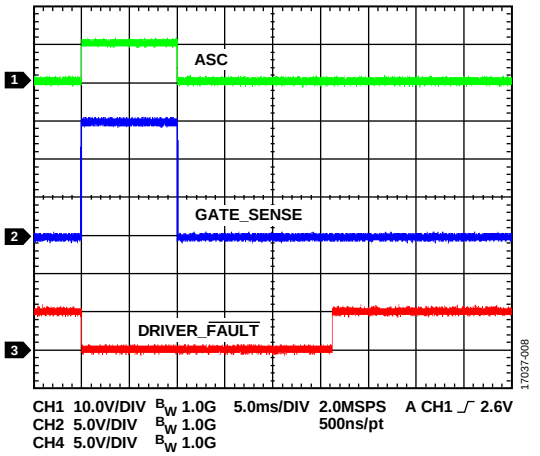


Figure 8. Example ASC Signal, V_{DD1} = 5 V, V_{DD2} = 15 V, VI+ = 5 V, 10 ms ASC, 100 nF Load

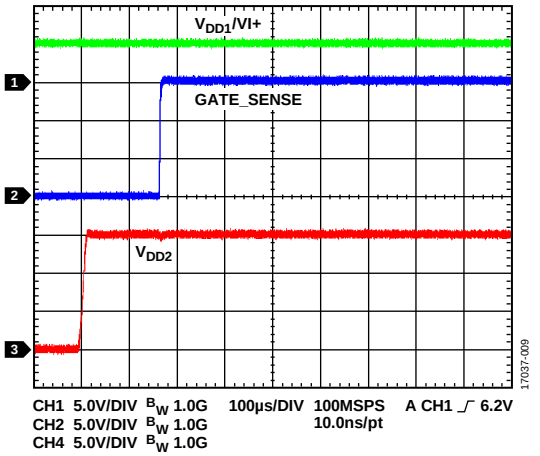


Figure 9. Typical V_{DD2} Startup Time, VI+ = V_{DD1}

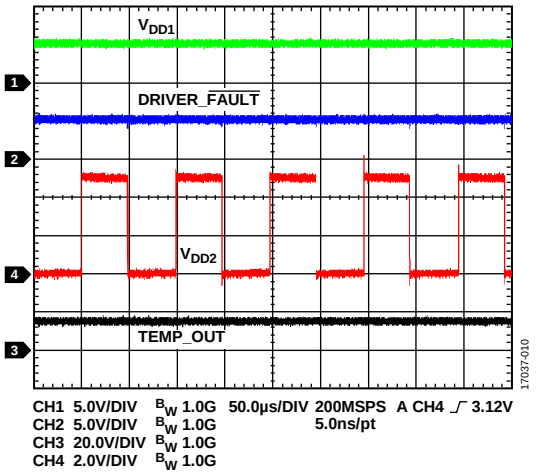


Figure 10. Example TEMP_OUT Reading, V_{DD1} = 5 V, V_{DD2} = 15 V, 2 kΩ Resistor on TS1

THEORY OF OPERATION

Gate drivers are required in situations where fast rise times of switching device gates are required. The gate signals for enhancement power devices are referenced to a source or emitter node. The gate driver must follow this source or emitter node. As such, isolation is necessary between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a complementary metal-oxide semiconductor (CMOS) output reduce the total delay time and increase the final drive strength of the driver.

The ADuM4137 achieves isolation between the control side and the output side of the gate driver using a high frequency carrier that transmits data across the isolation barrier with *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. The ADuM4137 uses positive logic on/off keying (OOK) encoding, in which a high signal is transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices and can drive in situations where shoot through conditions are present. The architecture of the ADuM4137 is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and differential coil layout. Figure 11 shows the OOK encoding used by the ADuM4137.

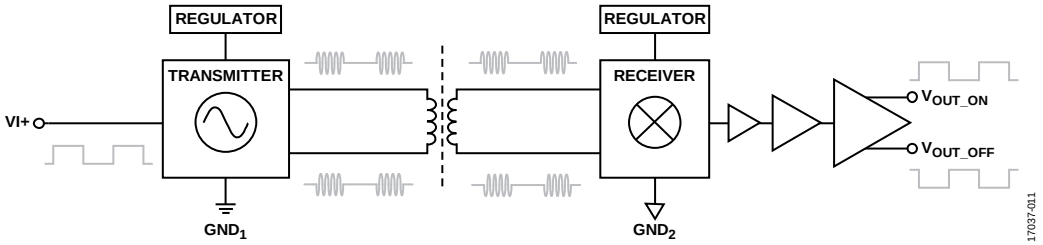


Figure 11. Operational Block Diagram of OOK Encoding

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4137 IGBT gate driver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the V_{DD1} and V_{DD2} supply pins. Use a ceramic capacitor >10 µF on V_{DD1} to GND_1. Add at least 30 µF to 60 µF of capacitance on the output power supply pin (V_{DD2}) to provide the charge required to drive the gate capacitance at the outputs. This capacitance can be provided by multiple parallel capacitors. Avoid using vias on the bypass capacitor or employ multiple vias to reduce the inductance in the bypassing because board vias can introduce parasitic inductance. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed approximately 5 mm. For the 5 V regulators, place 1 µF capacitors as close as possible to the ADuM4137.

The input pins (VI+, VI−, MOSI, $\overline{CS}$, and SCLK) require in series 100 Ω resistors to limit current.

SPI AND EEPROM OPERATION

SPI Programming

The ADuM4137 contains an SPI bus for setting remote temperature gains and offsets, PWM reporting frequency, high temperature faults, and low temperature operation mode.

SPI programming is enabled when $\overline{CS}$ is low and UVLO_$\overline{FAULT}$ is actively pulled low. The SPI bus allows programming of the secondary side EEPROM, allowing a permanent operation setting. The SPI interface can operate in a daisy-chain mode to allow efficient use of the microcontroller input and output pins. When used in a daisy-chain configuration, the ADuM4137 expects an integer multiple of 24 clock cycles for each chip select. All noninteger multiples of 24 clock cycles within a chip select period are ignored. If the ADuM4137 is in a daisy-chain link with devices other than ADuM4137 devices, ensure that the register space of the other devices adds up to an integer multiple of 24. When the chip select pin ($\overline{CS}$) is brought low while the UVLO_$\overline{FAULT}$ pin is pulled low, programming of the EEPROM is available. However, the gate drive output is disabled. The gate drive output is available again when $\overline{CS}$ is brought back to high.

Programming is performed using the standard SPI convention of clock polarity, CPOL = 0 and clock phase CPHA = 1. The timing diagram in Figure 2 demonstrates a typical read or write operation. Bit A1 and Bit A0 are the address bits. The must be zero (MBZ) bits must be set to 0. Bits[D23:D0] are the data bits, with MSB first. Bit RW0 sets whether the action is a read (0) or a write (1).

USER REGISTER MAP

Figure 12 shows the user trim register map and binary addresses.

ADDRESS	NAME	BIT																					
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	USER	OFFSET_2[5:0]						GAIN_2[5:0]						OFFSET_1[5:0]						GAIN_1[5:0]					
01	CONFIG	RESERVED							OT_FAULT_OP	OT_FAULT_SEL	OC_TIME_OP	OC_2LEV_OP	LOW_T_OP	OC_BLANK_OP	t_{BLANK}[3:0]				ECC_OFF_OP	RESERVED				T_RAMP_OP	PWM_OSC
10	CONTROL	RESERVED																		ECC2_DBL_ERR	ECC2_SNG_ERR	ECC1_DBL_ERR	ECC1_SNG_ERR	PROG_BUSY	SIM_TRIM

17037-012

Figure 12. User Trim Register Map

USER REGISTER BITS

Table 14 lists the user register (Address 00) bits and bit descriptions.

Table 14. User Register (Address 00) Bit Descriptions

Bit(s)	Bit Name	Description
[23:18]	OFFSET_2[5:0]	TS2 offset
[17:12]	GAIN_2[5:0]	TS2 gain
[11:6]	OFFSET_1[5:0]	TS1 offset
[5:0]	GAIN_1[5:0]	TS1 gain

OFFSET_2[5:0] Bits

Use the OFFSET_2 bits of the EEPROM to adjust the internal offset for the TS2 pin. See the Isolated Temperature Sensor section for more information.

GAIN_2[5:0] Bits

Use the GAIN_2 bits of the EEPROM to adjust the internal gain for the TS2 pin. See the Isolated Temperature Sensor section for more information.

OFFSET_1[5:0] Bits

Use the OFFSET_1 bits of the EEPROM to adjust the internal offset for the TS1 pin. See the Isolated Temperature Sensor section for more information.

GAIN_1[5:0] Bits

Use the GAIN_1 bits of the EEPROM to adjust the internal gain for the TS1 pin. See the Isolated Temperature Sensor section for more information.

CONFIGURATION REGISTER BITS

Table 15 lists the configuration (CONFIG) register (Address 01) bits and bit descriptions.

Table 15. CONFIG Register (Address 01) Bit Descriptions

Bit(s)	Bit Name	Description
[23:17]	Reserved	Reserved
16	OT_FAULT_OP	Overtemperature fault disable
15	OT_FAULT_SEL	Overtemperature fault select
14	OC_TIME_OP	Disable two-level drive and timer during overcurrent event
13	OC_2LEV_OP	Overcurrent two-level operation select
12	LOW_T_OP	Low temperature operation select
11	OC_BLANK_OP	Overcurrent blanking operation select
[10:7]	t_{BLANK}	Overcurrent blanking time
6	ECC_OFF_OP	Enable soft shutdown with ECC fault
[5:2]	Reserved	Reserved
1	T_RAMP_OP	Overcurrent temperature ramp enable
0	PWM_OSC	Temperature reading output oscillator select

OT_FAULT_OP Bit

Set the OT_FAULT_OP bit to 1 to disable a fault for over-temperature. If this bit is set to 0, the ADuM4137 issues a fault when the TS1 or TS2 pin detects an overtemperature event.

OT_FAULT_SEL Bit

The OT_FAULT_SEL bit selects between two overtemperature fault voltage thresholds. Set this bit to 0 to set the falling threshold to 1.64 V (typical) and the rising threshold is 1.69 V (typical). Set the OT_FAULT_SEL bit to 1 to set the falling threshold to 1.68 V (typical) and the rising threshold is 1.73 V (typical).

OC_TIME_OP Bit

Set the OC_TIME_OP bit to 1 to disable the two-level drive and timer during an overcurrent event. During an overcurrent event, the output immediately enters soft shutdown. If enabled, overcurrent blanking is still available.

OC_2LEV_OP Bit

Set the OC_2LEV_OP bit to 1 to disable the two-level drive during an overcurrent event before a fault registers. After the overcurrent detection time completes, a fault register and the output shuts down using soft shutdown. If this bit is set to 0 during an overcurrent event, but before t_{dOC}, the two-level drive level is output to the gate.

LOW_T_OP Bit

Bit 12 of the CONFIG register can disable a special low temperature operation. If the LOW_T_OP bit is set to 0 when the TS1 pin rises above 2.40 V (typical), the gate voltage goes to the two-level plateau voltage during an on command. Hysteresis allows operation down to 2.36 V (typical) on TS1 before the low temperature operation mode is exited. If the LOW_T_OP bit is set to 1, all nonfault gate signals are at the V_{DD2} output voltage on an on signal.

OC_BLANK_OP Bit

Set OC_BLANK_OP to 1 to enable two-level drive during current blanking time. When the OC_BLANK_OP bit is set to 1, it enters two-level drive in case of an overcurrent event during the blanking time, t_{BLANK}.

t_{BLANK}[3:0] Bits

During the initial turn on of a gate, a large amount of noise caused by switching actions can exist. By setting different t_{d_OC} values, the overcurrent detection can be masked by setting different t_{BLANK} values. During the masking time, overcurrent events are ignored.

Table 16. t_{BLANK} Blanking Times

t_{BLANK}[3:0], Bits[10:7]	Blanking Time (µs) Typical
0000	0
0001	0.36
0010	0.56
0011	0.77
0100	0.97
0101	1.17
0110	1.57
0111	1.97
1000	2.37
1001	2.78
1010	3.18
1011	3.58
1100	3.98
1101	4.39
1110	4.79
1111	5.19

ECC_OFF_OP Bit

If the ECC_OFF_OP bit is set to 1 when an ECC error is detected, the ADuM4137 enters soft shutdown and a fault registers. This fault registers whether a single or double ECC fault is detected. If this bit is set to 0, ECC faults are set in the control register (Address 10), but the ADuM4137 continues to operate without shutting down.

T_RAMP_OP Bit

Set the T_RAMP_OP bit to 0 to allow the overcurrent reference voltage to vary with temperature. The current reference varies from 2.7 V (typical) to 1.75 V (typical) across the TS1 voltages of 1.55 V to 2.45 V, as shown in Figure 14. Set the T_RAMP_OP bit to 1 to have the overcurrent reference voltage, V_{OCD_TH}, set to 2 V (typical) regardless of the sensed temperature.

PWM_OSC

The PWM_OSC bit controls whether the reported TEMP_OUT pin PWM frequency is 10 kHz or 50 kHz. When the PWM_OSC bit is set to 0, the output frequency is 10 kHz (typical). When the PWM_OSC bit is set to 1, the PWM output frequency is 50 kHz (typical).

CONTROL REGISTER BITS

Table 17 lists the control register (Address 10) bits and bit descriptions.

Table 17. Control Register (Address 10) Bit Descriptions

Bit(s)	Bit Name	Description
[23:6]	Reserved	Reserved.
5	ECC2_DBL_ERR	ECC Bank 2 double error detected
4	ECC2_SNG_ERR	ECC Bank 2 single error detected
3	ECC1_DBL_ERR	ECC Bank 1 double error detected
2	ECC1_SNG_ERR	ECC Bank 1 single error detected
1	PROG_BUSY	Program/busy bit
0	SIM_TRIM	Simulate trim

ECC2_DBL_ERR Bit

When two errors are detected in the EEPROM stored data, the ECC2_DBL_ERR bit sets to 1 when read. Two errors are detectable. However, these errors cannot be corrected using the error correcting code employed by the ADuM4137. The ECC2_DBL_ERR bit set to 1 indicates when a double error is detected in the memory banks, representing trim performed on the ADuM4137 outside of registers affected by user and CONFIG addresses. When this bit is set to 0, it indicates no error was detected for bits greater than 1.

ECC2_SNG_ERR Bit

When a single error is detected in the EEPROM stored data, the ECC2_SNG_ERR bit sets to 1 when read. The error correcting code employed by the ADuM4137 can detect and correct a single error. The ECC2_SNG_ERR bit set to 1 indicates when a single error is detected in the memory banks, representing trim performed on the ADuM4137 outside of the registers affected by the user and configuration addresses. When this bit is set to 0, it indicates no single bit error was detected.

ECC1_DBL_ERR Bit

When two errors are detected in the EEPROM stored data, the ECC1_DBL_ERR bit sets to 1 when read. Two errors are detectable. However, these errors cannot be corrected using the error correcting code employed by the ADuM4137. The ECC2_DBL_ERR bit set to 1 indicates that a double error is detected in the memory banks, representing trim performed on the ADuM4137 by the user and configuration addresses. A value of 0 indicates no error was detected for bits greater than 1.

ECC1_SNG_ERR Bit

When a single error is detected in the EEPROM stored data, the ECC1_SNG_ERR bit is set to 1 when read. The error correcting code employed by the ADuM4137 can detect and correct a single error. The ECC2_SNG_ERR bit set to 1 indicates that a single error is detected in the memory banks, representing trim performed on the ADuM4137 by the user and configuration addresses. A value of 0 indicates no single bit error was detected.

PROG_BUSY Bit

Set the PROG_BUSY bit high to program the EEPROM memory. When this bit is set to 1, the EEPROM begins to write to the memory. The hardware sets this bit back to 0 to indicate that programming has occurred. The write sequence takes 40 ms (maximum) to perform but can write faster than 40 ms (maximum). If a shorter wait time is required, read the PROG_BUSY bit back multiple times during the write time. If 0 is read back after the user sets the bit to 1, the write completes.

SIM_TRIM Bit

If the SIM_TRIM bit is set to 0, the user and configuration registers have no effect on the operation of the ADuM4137. Use this bit to simulate trim settings but not to write to the registers.

If SIM_TRIM is set high, address values can change the operation of the gate driver to simulate the effect of programming the values to the EEPROM across power-ups. When SIM_TRIM is set to 0, previous address values from the EEPROM are loaded, and operation returns to the power on state.

SPI SAFETY

To reduce single-point failure nodes, bring two signals low to activate the SPI communication. During SPI communication, the forward path channel deactivates. To activate SPI communication, drive both the UVLO_$\overline{\text{FAULT}}$ pin and $\overline{\text{CS}}$ pins low. Pull the UVLO_$\overline{\text{FAULT}}$ pin low using an external open-drain connection to not disrupt the normal UVLO_$\overline{\text{FAULT}}$ behavior. When the UVLO_$\overline{\text{FAULT}}$ pin is high, the SPI is not active. Refer to Table 12 for the $\overline{\text{FAULT}}$ pin mapping. For normal operation, a $\overline{\text{FAULT}}$ (TSD, TSx_OT_FAULT, OCx overcurrent, gate low, V_{DD2} UVLO, and ECC error) forces the driver off. During SPI communication, it is possible to mask faults shown on the fault pins. During SPI communication, any fault information on DRIVER_$\overline{\text{FAULT}}$ or UVLO_$\overline{\text{FAULT}}$ does not posted. When $\overline{\text{CS}}$ is brought low to initiate SPI communication, both DRIVER_$\overline{\text{FAULT}}$ and UVLO_$\overline{\text{FAULT}}$ are forced high.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay describes the time it takes a logic signal to propagate through a component. The propagation delay to a low output can differ from the propagation delay to a high output. The ADuM4137 specifies the rising propagation delay, t_{DLH} (see Figure 13), as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold. Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

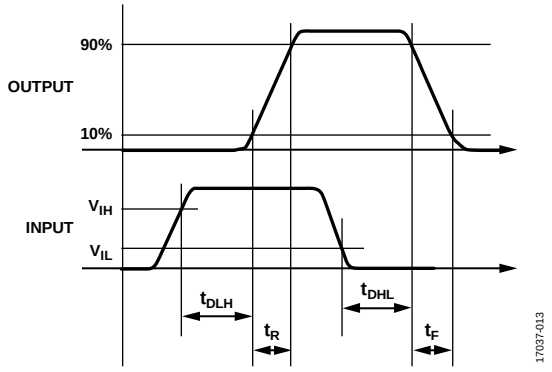


Figure 13. Propagation Delay Parameters

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4137 components operating under the same temperature, input voltage, and load conditions.

PROTECTION FEATURES

Primary Side UVLO

The ADuM4137 has UVLO on both the primary and secondary sides. If the primary side voltage supply, V_{DD1}, drops below 4.25 V (typical), the transmission to the secondary side is stopped, effectively bringing the output low.

Fault Reporting

The ADuM4137 provides protections for faults that may occur during the operation of an IGBT. The primary fault condition is overcurrent as detected by the overcurrent detection pins, OC1 and OC2. If detected, the ADuM4137 shuts the gate drive down and asserts the $\overline{\text{FAULT}}$ pin low. Faults initiate a soft shutdown through the V_{OFF_SOFT} pin. During a fault, the external Miller clamp does not activate. Secondary undervoltage lock out (UVLO2), secondary thermal shutdown (TSD2), ECC error, overcurrent, gate low voltage detect, and remote overtemperature can initiate faults.

Overcurrent Detection

The ADuM4137 operates with split emitter IGBTs or split source MOSFETs. Use the lower current section of the split leg switches for an accurate measurement of the current through the IGBT or MOSFET, resulting in a fast reaction to overcurrent events. When an overcurrent event is detected, a high speed, two-level turn off initiates. If the overcurrent condition remains beyond the two-level detect delay time (t_{dOC}), a fault reports to the primary side of the ADuM4137. If the overcurrent condition is removed before the turn off time, the V_{OUT_ON} pin returns to a high output state and the fault timer is reset.

The sense temperature on the TS1 pin can modify the overcurrent threshold. If the T_RAMP_OP bit is set to 1, the overcurrent threshold is set to 2 V (typical) across all operating conditions. When the T_RAMP_OP bit is set to 0, the overcurrent threshold, $V_{OCD_TH_EN}$, is 2.7 V typical at a TS1 = 1.55 V and 1.75 V typical at a TS1 = 2.45 V in a linear fashion (see Figure 14).

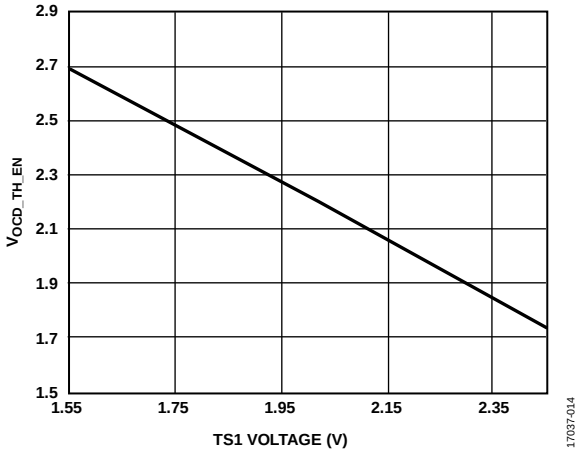


Figure 14. Overcurrent Threshold Variation Due to Sensed Temperature

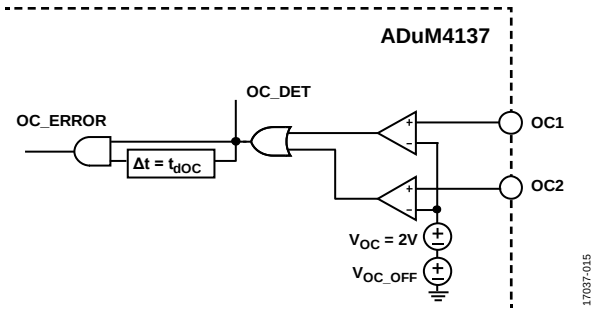


Figure 15. Split Emitter Overcurrent Detection Functional Block Diagram

High Speed, Two-Level Turn Off

If the OC1 or OC2 pin detects an overcurrent, the two-level turn off circuitry drives the gate low. The internal NMOS FET drives the device gate low until the GATE_SENSE pin reaches the 11.89 V (typical) voltage plateau. t_{dOCR} is the time the output takes from detecting an overcurrent to driving the overcurrent to the plateau voltage. After the detect time (t_{dOC}), a fault is registered and reported to the primary side (see Figure 16). If during t_{dOC} the overcurrent threshold, V_{OCD_TH}, is no longer violated, the internal PMOS returns the gate voltage back to the V_{DD2} voltage, and the two-level timer is reset (see Figure 17).

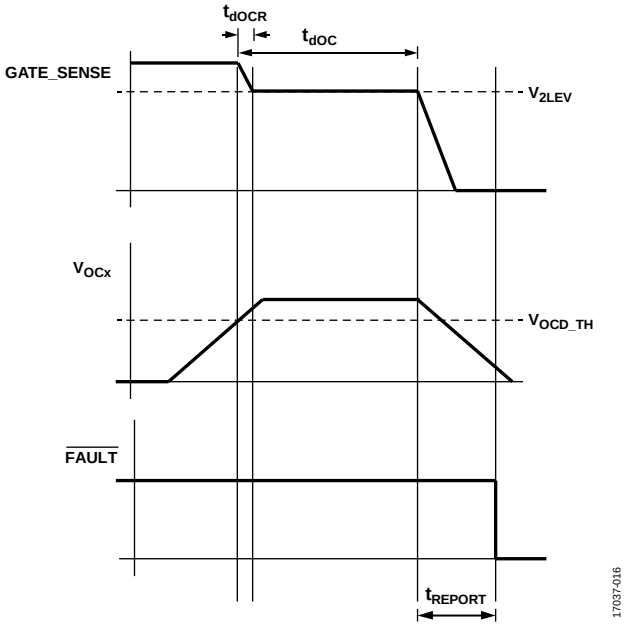


Figure 16. Two-Level Turn Off Fault Example (Not to Scale)

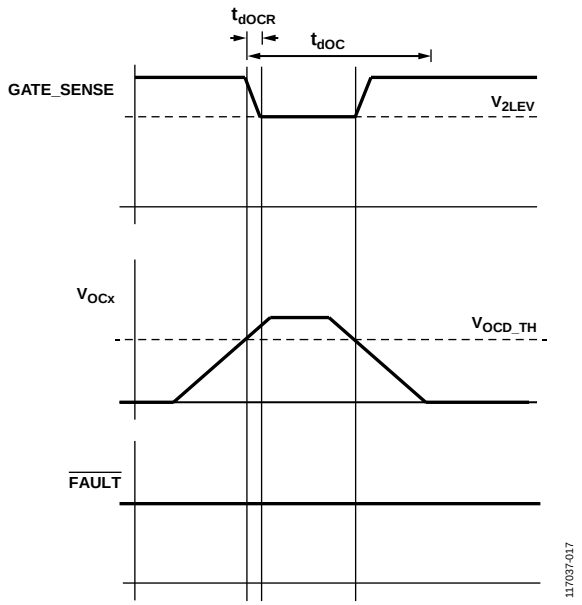


Figure 17. Two-Level Timer Recovery Example

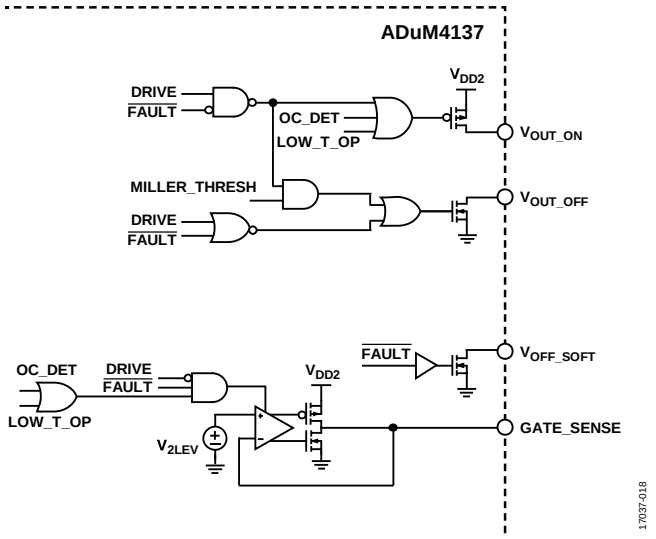


Figure 18. Gate Voltage Output Functional Block Diagram

Miller Clamp

The ADuM4137 has an integrated Miller clamp control signal to reduce voltage spikes on the IGBT gate due to the Miller capacitance during shutoff of the IGBT. When the input gate signal calls for the IGBT to turn off (drive low), the external Miller clamp MOSFET signal is initially off. When the voltage on the GATE_SENSE pin crosses the 2 V (typical) internal voltage reference as referenced to GND_2, the Miller clamp latches on for the remainder of the off time of the IGBT, creating a second low impedance current path for the gate current to follow. The Miller clamp switch remains on until the input drive signal changes from low to high. An example waveform of the timing is shown in Figure 19.

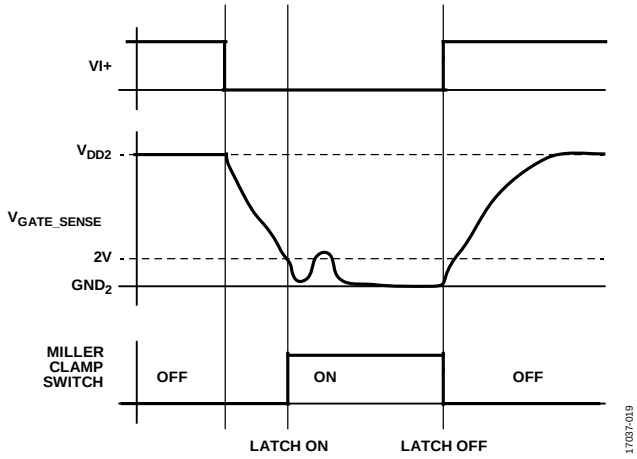


Figure 19. Miller Clamp Example

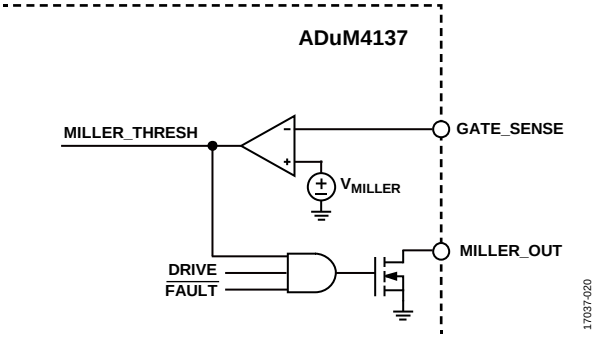


Figure 20. Miller Clamp Functional Block Diagram

Thermal Shutdown

The ADuM4137 contains two TSDs. If the internal temperature of the secondary side of the ADuM4137 exceeds 150°C (typical), the ADuM4137 enters a TSD fault, and the gate drive disables by means of a soft shutdown. When a TSD occurs, the ADuM4137 does not exit TSD until the internal temperature drops below 130°C (typical). After reaching this temperature, the ADuM4137 exits shutdown. A fault output is available on the primary side during a TSD event on the secondary side by means of the $\overline{\text{FAULT}}$ pin.

If the primary die temperature exceeds 154°C (typical), the primary side functions shut down, stopping the flyback switching and shutting down the secondary side. The primary side leaves TSD when the internal temperature drops below 135°C (typical).

The main cause of overtemperature is driving too large a load for a given ambient temperature. This type of temperature overload typically affects the secondary side die because the main power dissipation for load driving occurs on the secondary side.

ASC Pin Functionality

The ASC pin provides external secondary side control for enabling the driver. The ASC pin has a comparator triggering at 8.93 V (typical) with a 0.85 V (typical) hysteresis. When the ASC signal is greater than 8.93 V (typical), the signal forces the driver to output high if no fault occurs. The ASC pin signal is OR'ed with the forward path drive signal. Read and write capabilities via the SPI interface to the EEPROM on the secondary side are still available during an ASC event. Interfacing with the ASC pin can be performed directly or with an external open-drain NMOS MOSFET with a pull-up resistor to a value more than 8.93 V (typical). An internal pull-down current source is included on the ASC pin.

Isolated Temperature Sensor

The ADuM4137 allows simple isolated temperature detection. Using an internal current source to bias an external temperature sensing diode, the ADuM4137 encodes the forward-biased voltage of the diode into a PWM signal that is passed across the isolation barrier from the secondary side to the primary side. The PWM signal operates at 10 kHz or 50 kHz (programmed in the EEPROM). Voltages between the minimum and maximum are approximately linear and monotonically interpolated. The ADuM4137 contains support for two remote temperature sensing diode assemblies, which can both cause overheating faults on the secondary side. Additionally, one temperature sensor readback is available for reading on the primary side through the isolated temperature reporting channel. The lower voltage (higher temperature) of the two temperature sensor pins, TS1 and TS2, report on the TEMP_OUT pin. The gain and offset of the pulse-width modulated temperature sensor can be set in the EEPROM. A typical plot of the duty cycle vs. the lower temperature sense pin (TSx) voltage is shown in Figure 21.

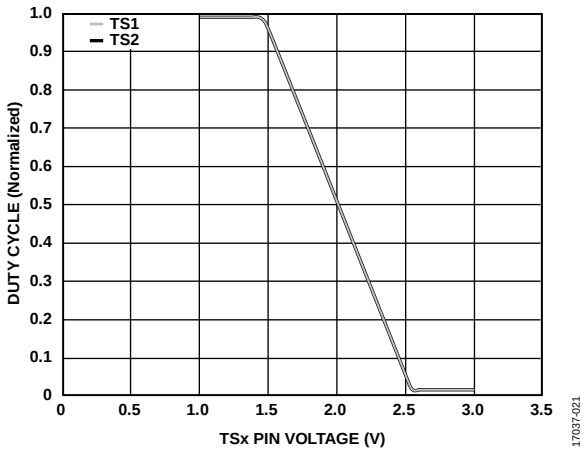


Figure 21. TEMP_OUT Duty Cycle vs. Lower TSx Pin Voltage

The voltage mapping for the PWM follows this typical equation:

$$PWM_DUTY = -0.9065 \times TS_VOLTAGE + 2.3264$$

where:
PWM_DUTY is the duty cycle on the TEMP_OUT pin where full scale is 1. *PWM_DUTY* is equivalent to the percent of duty cycle divided by 100.
TS_VOLTAGE is the lowest voltage on the TS1 or the TS2 pin.

Use the GAIN_1, GAIN_2, OFFSET_1, and OFFSET_2 bits to adjust the voltage to the PWM response of the TSx pins. The gain and offset registers are 6-bit, twos complement values. The MSB is Bit 5 in each gain and offset bit field.

The gain bits affect the slope of the response, centered on 2.22 V (typical). This pivot point was selected to be approximately where a temperature sense diode stack may sit at 25°C. The gain bit values affect the slope of the response with a LSB of −0.00558 (typical). When the gain register changes, the response pivots such that the 2.22 V (typical) point returns a PWM of 0.194 (typical), unless an offset bit setting of a value other than 000000 is set. The offset bits shift the voltage to the PWM response up and down. The LSB of the offset bits is 0.001336 (typical).

Rewriting the PWM_DUTY equation to allow gain and offset settings, and accounting for a 2.22 V typical pivot point in the gain setting results in the following:

$$PWM_DUTY = (-0.9065 + GAIN_x \times GAIN_LSB) \times (TS_VOLTAGE - 2.22) + (2.3264 + OFFSET_x \times OFFSET_LSB - 0.194)$$

where:
GAIN_x is a GAIN_1 or GAIN_2 twos complement decimal equivalent.
GAIN_LSB = −0.00558 typical.
TS_VOLTAGE is the voltage seen on TS1 or TS2.
OFFSET_x is the OFFSET_1 or OFFSET_2 twos complement decimal equivalent.
OFFSET_LSB = 0.001336 typical.

Low Temperature Operation Mode

A low temperature operation mode is available if the voltage sensed on the TS1 pin is greater than 2.4 V (typical), the maximum gate voltage is set to the two-level plateau voltage of 11.89 V (typical). Hysteresis allows continued low temperature operation until the TS1 pin voltage goes below 2.36 V (typical). Low temperature operation can be enabled or disabled in the EEPROM settings in the LOW_T_OP bit, Address 01, Bit 12. Basic operation is shown in Figure 22. During a two-level drive, the R_{DSON} resistances of the turn on and turn off drivers are increased to approximately 4 times the normal turn on and turn off resistances.

$\overline{\text{FAULT}}$ Pin

The $\overline{\text{FAULT}}$ pin can map to TSD, TSx_OT_FAULT, gate low, V_{DD2} UVLO, OCx overcurrent, and ECC error faults. The $\overline{\text{FAULT}}$ pin is a CMOS output that is connected between the GND_1 and V5_1 pins. When $\overline{\text{FAULT}}$ is brought low due to a fault detection on the ADuM4137, the output driver forward path is disabled, which brings the output low.

The latch time for the TSD, TSx_OT_FAULT, V_{DD2} UVLO, OCx overcurrent, and ECC error faults is 20 ms typical (Latch Assert Time B). The latch time for a gate low error is 26 ms typical (Latch Assert Time C). The $\overline{\text{FAULT}}$ pin is held low for the hold time (t_{PW}) or the length of time the error persists, whichever is longer.

DRIVER_$\overline{\text{FAULT}}$ Pin

The DRIVER_$\overline{\text{FAULT}}$ pin is an open-drain output with an internal pull-up current source ($I_{PU_D\overline{F}}$) of 78 µA (typical) to V5_1. The DRIVER_$\overline{\text{FAULT}}$ pin can map to the gate low, OCx overcurrent, ECC error, ASC, and DT_$\overline{\text{FAULT}}$ faults. If any of the faults mapped to the DRIVER_$\overline{\text{FAULT}}$ occur, the DRIVER_$\overline{\text{FAULT}}$ pin is driven low for the minimum latch time or as long as the fault persists, whichever is longer. The minimum fault latch time for the gate low, OCx overcurrent, ECC error, and ASC is 26 ms (typical). The minimum fault latch time for a DT_FAULT is 13 ms (typical) (Latch Assert Time A).

UVLO_$\overline{\text{FAULT}}$ Pin

The UVLO_$\overline{\text{FAULT}}$ pin can map to the gate low and VDD2 UVLO. The UVLO_$\overline{\text{FAULT}}$ pin is an open-drain output with an internal $I_{PU_D\overline{F}}$ of 78 µA (typical) to V5_1.

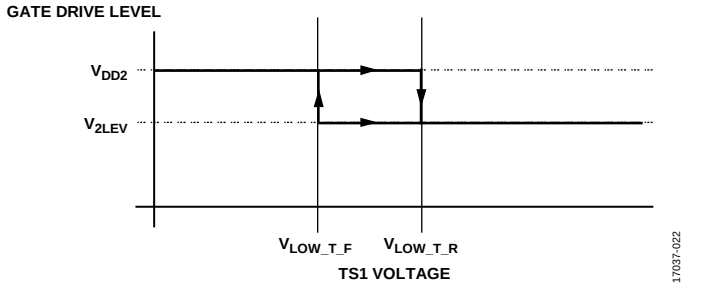


Figure 22. Low Temperature Operation

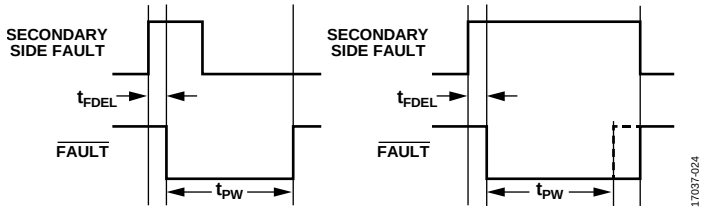


Figure 23. $\overline{\text{FAULT}}$ Pin Fault

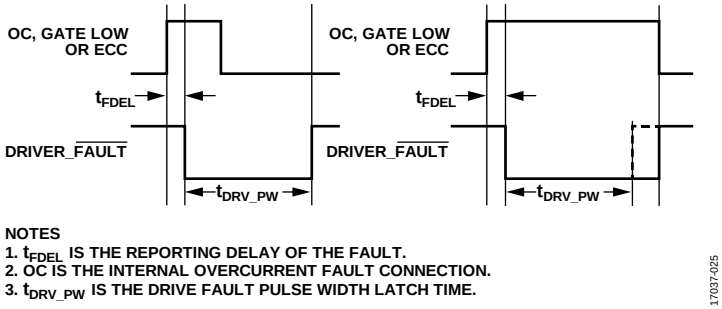
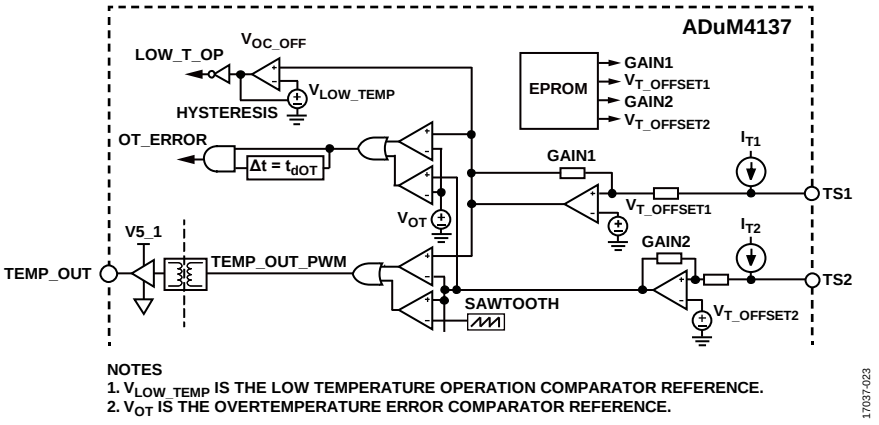
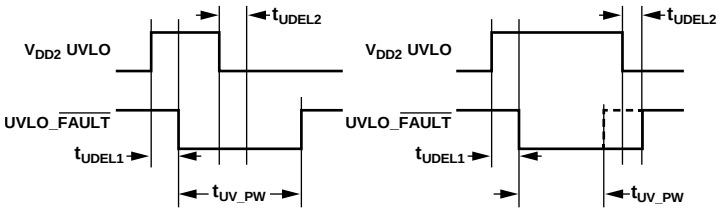


Figure 24. DRIVER_$\overline{\text{FAULT}}$ Fault



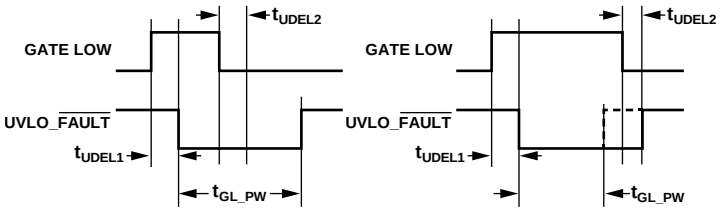
NOTES
1. V_{LOW_TEMP} IS THE LOW TEMPERATURE OPERATION COMPARATOR REFERENCE.
2. V_{OT} IS THE OVERTEMPERATURE ERROR COMPARATOR REFERENCE.

Figure 25. Remote Temperature Sensing Block Diagram



NOTES
1. t_{UV_PW} IS THE V_{DD2} UVLO FAULT LATCH TIME, ~13ms TYPICAL.

Figure 26. UVLO_$\overline{FAULT}$ Fault for V_{DD2} UVLO



NOTES
1. t_{GL_PW} IS THE GATE LOW FAULT LATCH TIME, ~26ms TYPICAL.

Figure 27. UVLO_$\overline{FAULT}$ Fault, Gate Low

V_{DD2} UVLO Fault

When a V_{DD2} UVLO fault occurs, the fault drives the UVLO_$\overline{FAULT}$ pin low within the fault propagation delay posting time, t_{UDEL1} (within 6.7 µs typical) and reports the fault on the primary side for 13 ms (typical) if the V_{DD2} UVLO fault exists for less than ~13 ms. When the V_{DD2} UVLO fault exists for longer than ~13 ms, the UVLO_$\overline{FAULT}$ releases within the fault propagation delay clearing time, t_{UDEL2} (within 6.7 µs typical), after the V_{DD2} UVLO is released on the secondary side.

UVLO_$\overline{FAULT}$ Fault, Gate Low

When a gate low fault occurs, the fault drives the UVLO_$\overline{FAULT}$ low within t_{UDEL1} and reports the fault on the primary side for ~26 ms if the V_{DD2} UVLO fault exists for less than ~26 ms. If the gate low fault exists for longer than ~26 ms, the UVLO_$\overline{FAULT}$ releases within t_{UDEL2} after the V_{DD2} UVLO releases on the secondary side. Separately, the pulse width can distinguish the gate low and V_{DD2} UVLO faults. However, if these faults occur simultaneously, only the longer pulse can be seen.

Dead Time Control

Dead time (t_{DEXT}) is set between VI+ and VI−. If t_{DEXT} > delay, the dead time is set by t_{DEXT}. Otherwise, if less than or equal to the delay, the dead time is set by delay. Delay is 1 µs typical.

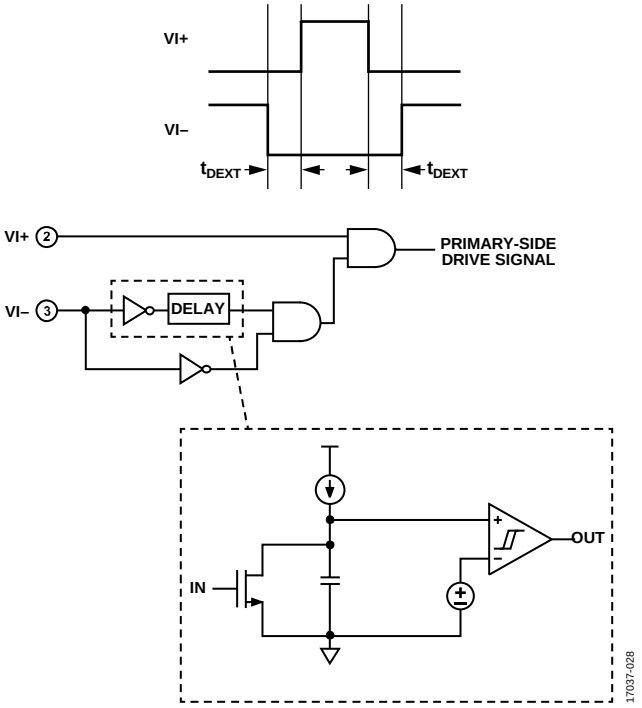


Figure 28. Dead Time Control

DRIVER_$\overline{FAULT}$ Fault, Dead Time Fault

The VI+ signal is monitored as well as the internal dead time at the start of each cycle. If the VI+ signal goes high before the rising edge of the 1 µs internal dead time complete signal, a dead time fault issues. This fault latches on the primary side for approximately 13 ms and does not turn off the driver. If VI− is always kept low, VI+ must be held low during startup.

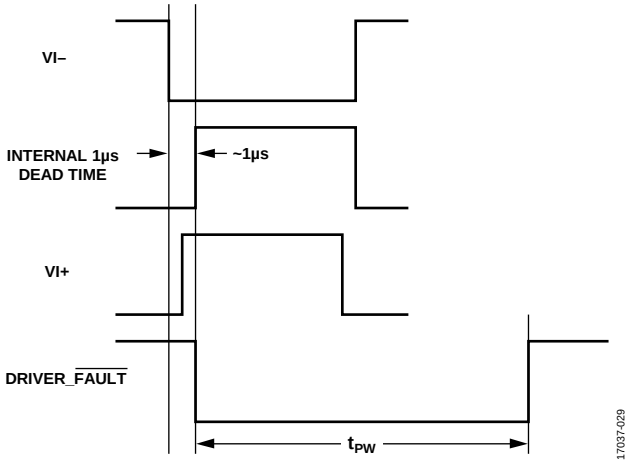


Figure 29. Dead Time Fault

Power Dissipation

When driving an IGBT gate, the driver must dissipate power. This power can lead to TSD if the following considerations are not made. The gate of an IGBT can be simulated roughly as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance (C_{ISS}) of a given IGBT and multiply it by a factor of 5 to arrive at a conservative estimate to approximate the load being driven. With this value, the estimated total power dissipation (P_{DISS}) in the system due to the switching action is given by the following equation:

$$P_{DISS} = C_{EST} \times (V_{DD2})^2 \times f_S$$

where:
$C_{EST} = C_{ISS} \times 5$ (conservative estimate).
V_{DD2} is the voltage on the V_{DD2} pin.
f_S is the switching frequency of the IGBT.

This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances (R_{GON} and R_{GOFF}). The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4137 chip.

Take the power dissipation found inside the chip due to switching, add the quiescent power losses, and multiply it by the θ_{JA} value to product the rise above ambient temperature that the ADuM4137 experiences.

$$P_{DISS_ADuM4137} = P_{DISS} \times 0.5(R_{DSON_P}/(R_{GON} + R_{DSON_P}) + (R_{DSON_N}/(R_{GOFF} + R_{DSON_N})) + P_{QUIESCENT}$$

where:
$P_{DISS_ADuM4137}$ is the power dissipation of the ADuM4137.
R_{GON} is the external series resistance in the on path.
R_{GOFF} is the external series resistance in the off path.
$P_{QUIESCENT}$ is the quiescent power.

$$T_{ADuM4137} = \theta_{JA} \times P_{DISS_ADuM4137} + T_{AMB}$$

where:
$T_{ADuM4137}$ is the junction temperature of the ADuM4137.
T_{AMB} is the ambient temperature.

For the ADuM4137 to remain within specification, $T_{ADuM4137}$ must not exceed 150°C (typical). If $T_{ADuM4137}$ exceeds 150°C (typical), the ADuM4137 enters TSD.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4137.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 10 summarize the peak voltage for 20 years of service life for a bipolar ac operating condition, and the maximum CSA and VDE approved working voltages. In many cases, the approved working voltage is higher than the 20 year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4137 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 30, Figure 31, and Figure 32 show these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 20 year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 20 year service life. Treat any cross insulation voltage waveform that does not conform to Figure 31 or Figure 32 as a bipolar ac waveform, and limit its peak voltage to the 20 year lifetime voltage value listed in Table 10.

The voltage presented in Figure 31 is shown as sinusoidal only for illustration purposes. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

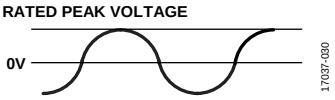


Figure 30. Bipolar AC Waveform

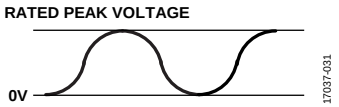


Figure 31. Unipolar AC Waveform

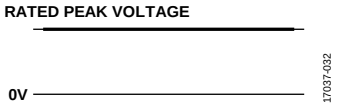


Figure 32. DC Waveform

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM4137 is resistant to external magnetic fields. The limitation on the ADuM4137 magnetic field immunity is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

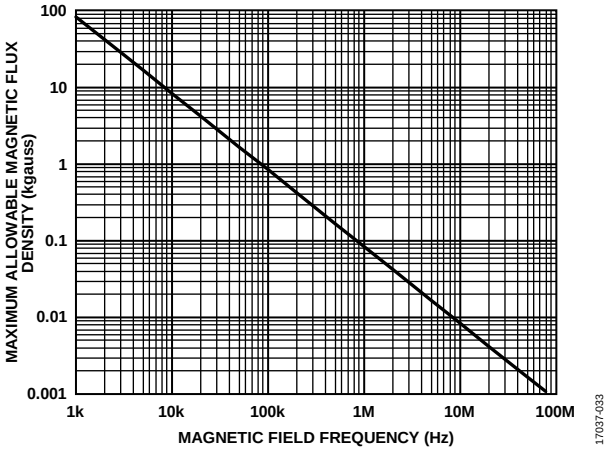


Figure 33. Maximum Allowable External Magnetic Flux Density

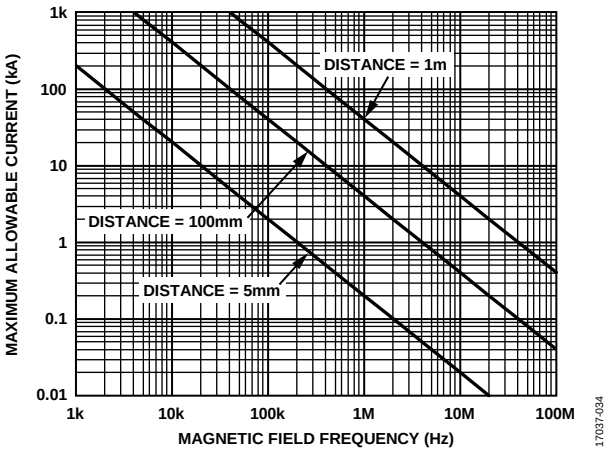
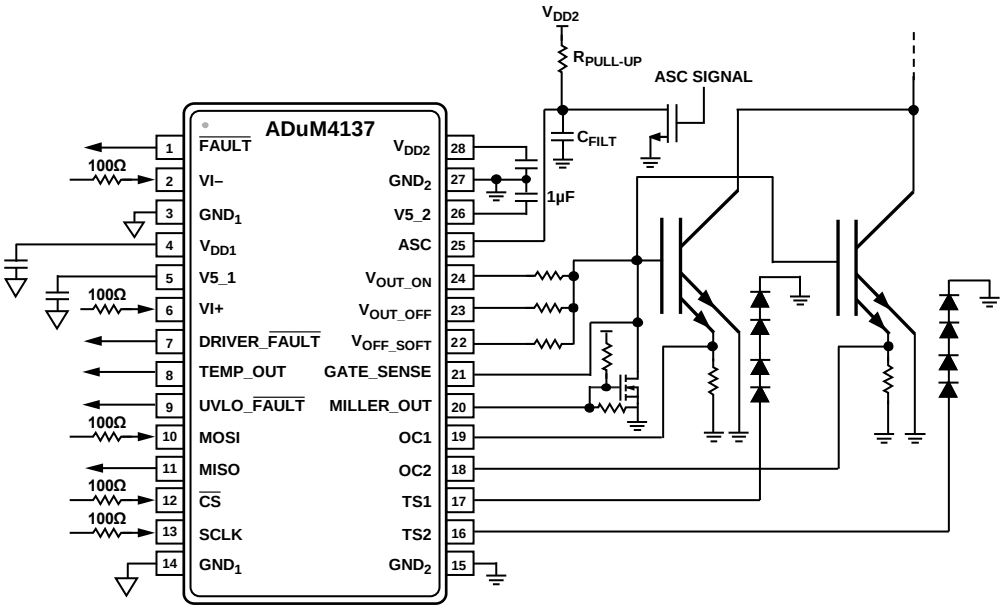


Figure 34. Maximum Allowable Current for Various Current to ADuM4137 Spacings

TYPICAL APPLICATION CIRCUIT



NOTES
1. C_{FILT} IS THE ASC PIN FILTER CAPACITOR.
2. $R_{PULL-UP}$ IS THE ASC PIN PULL-UP RESISTOR

Figure 35. IGBT Drive Example Application

OUTLINE DIMENSIONS

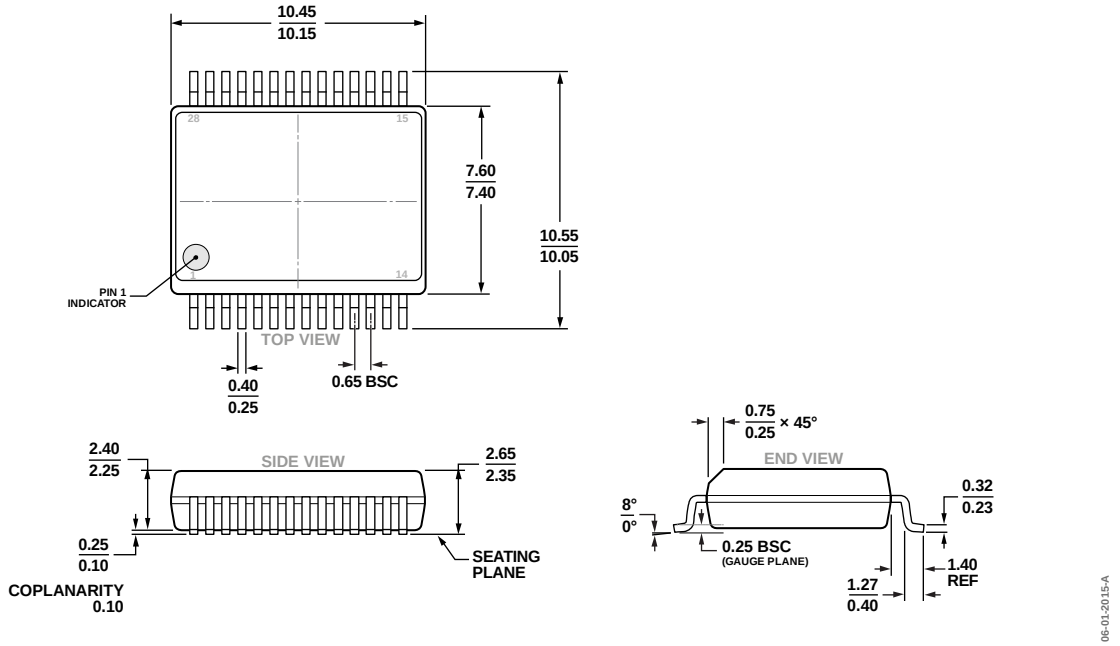


Figure 36. 28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADuM4137WBRNZ	−40°C to +150°C	28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP]	RN-28-1
ADuM4137WBRNZ-RL	−40°C to +150°C	28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP], 13″ Tape and Reel	RN-28-1
EVAL-ADuM4137EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADuM4137W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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