10 GHz to 20 GHz Tunable Band-Pass Filter

Preliminary Technical Data

ADMV8420

FEATURES

Fast tuning response (amplitude settling time): TBD ns
Excellent wideband rejection: ≤35 dB
Single-chip implementation
24-lead, 4 mm × 4 mm RoHS compliant LFCSP

APPLICATIONS

Test and measurement equipment
Military radar and electronic warfare systems
Very small aperture terminal (VSAT) communications

FUNCTIONAL BLOCK DIAGRAM

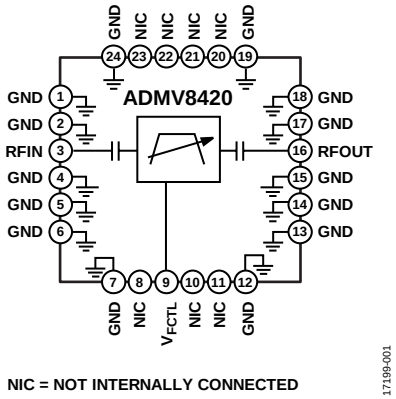

Figure 1.

GENERAL DESCRIPTION

The ADMV8420 is a monolithic microwave integrated circuit (MMIC) tunable band-pass filter that features a user-selectable pass-band frequency. The 3 dB filter bandwidth is approximately TBD% and the ≤35 dB filter bandwidth is approximately TBD%. Additionally, the center frequency can be varied between 10 GHz and 20 GHz by applying an analog control voltage between 0 V and 14 V. This tunable filter can be used as a much smaller alternative to physically large switched filter banks and cavity tuned filters. The ADMV8420 has excellent microphonics due to the monolithic design and provides a dynamically adjustable solution in advanced communications applications.

Rev. PrA Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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SPECIFICATIONS

T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
Center (f_{CENTER})	10		20	GHz	
Including 1 dB Bandwidth (BW)	TBD		TBD	GHz	
Including 3 dB BW	TBD		TBD	GHz	
BANDWIDTH					
1 dB		TBD		%	
3 dB		22		%	
REJECTION					
Low Side	TBD			dB	TBD BW away from 3 dB BW
High Side	TBD			dB	TBD BW away from 3 dB BW
Re-Entry		TBD × f_{CENTER}		GHz	≤35 dB wideband rejection
LOSS					
Insertion Loss		32		dB	
Return Loss		7		dB	
DYNAMIC PERFORMANCE					
Maximum Input Power for Linear Operation		TBD		dBm	
Input Third-Order Intercept (IP3)		TBD		dBm	Input power (P_{IN}) = 20 dBm
Input Power at TBD° Shift in Insertion Phase		TBD		dBm	
Group Delay Flatness		TBD		ns	
Phase Sensitivity		TBD		Rad/V	
Tuning Response (Amplitude Settling Time)		TBD		ns	TBD
Drift Rate		TBD		MHz/°C	
RESIDUAL PHASE NOISE					
1 MHz Offset		TBD		dBc/Hz	
TUNING					
Voltage (V_{FCTL})	0		14	V	
Current (I_{FCTL})			±1	µA	

ABSOLUTE MAXIMUM RATINGS

Table 2.

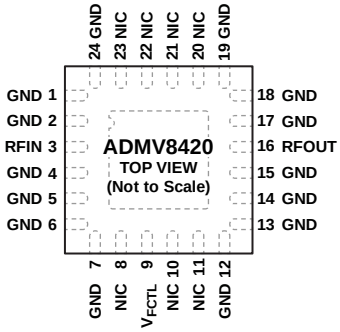
Parameter	Rating
Tuning	
Voltage (V_{FCTL})	−0.5 V to +15 V
Current (I_{FCTL})	±TBD mA
RF Input Power	TBD dBm
Temperature	
Operating	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Junction for 1 Million Mean Time to Failure (MTTF)	135°C
Nominal Junction (Exposed Pad Temperature (T_{PADDLE}) = 85°C, P_{IN} = 10 dBm)	TBD°C
Human Body Model (HBM) Electrostatic Discharge (ESD) Rating	TBD
Moisture Sensitivity Level (MSL) Rating	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, ALL DATA SHOWN HEREIN WAS MEASURED WITH THESE CONNECTED TO RF AND DC GROUND.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 12 to 15, 17 to 19, 24	GND	Ground. These pins must be connected to RF and dc ground.
3	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. An external voltage must not be applied.
8, 10, 11, 20 to 23	NIC	Not Internally Connected. These pins are not connected internally. However, all data shown herein was measured with these connected to RF and dc ground.
9	V_{FCTL}	Frequency Control.
16	RFOUT	RF Output. This pin is dc-coupled and matched to 50 Ω. An external voltage must not be applied.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. V_{FCTL} Interface Schematic

Figure 4. GND Interface Schematic

Figure 5. RFIN Interface Schematic

Figure 6. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

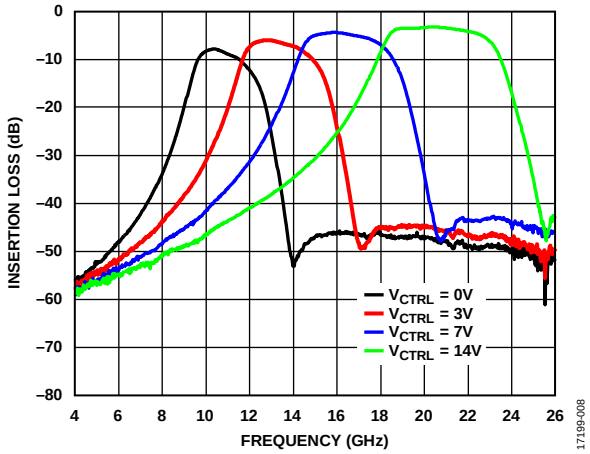


Figure 7. Insertion Loss vs. Frequency at Various Control Voltages (V_{FCTL}), Narrow Band

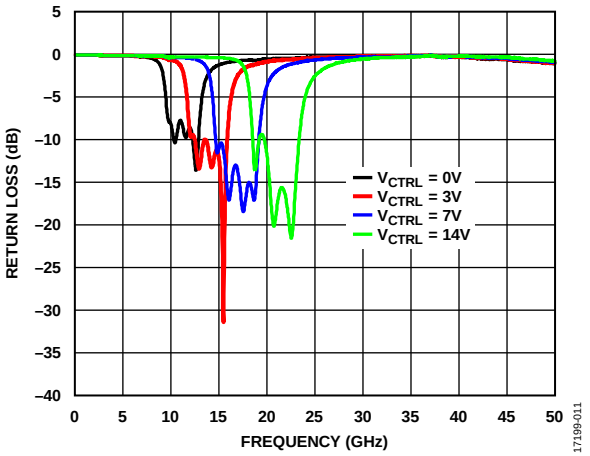


Figure 10. Return Loss vs. Frequency at Various Control Voltages (V_{FCTL}), Broadband

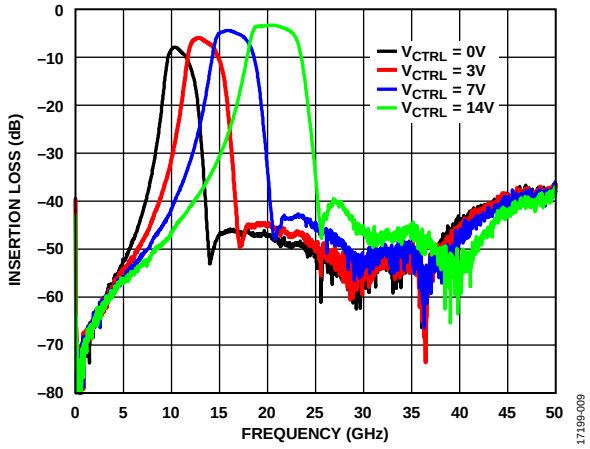


Figure 8. Insertion Loss vs. Frequency at Various Control Voltages (V_{FCTL}), Broadband

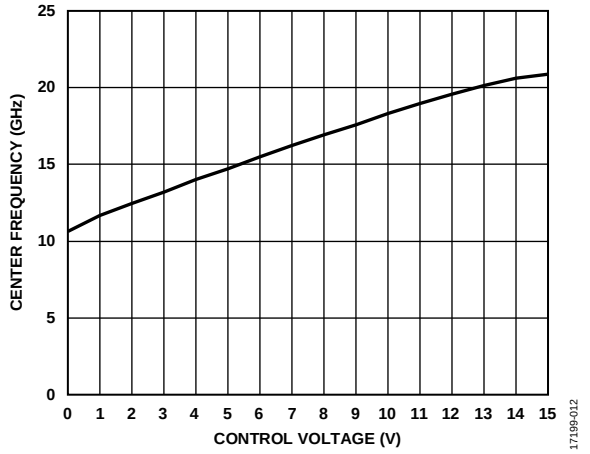


Figure 11. Center Frequency vs. Control Voltage (V_{FCTL})

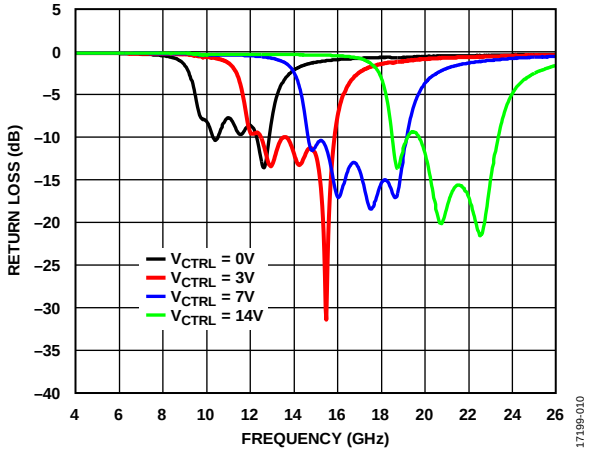


Figure 9. Return Loss vs. Frequency at Various Control Voltages (V_{FCTL}), Narrow Band

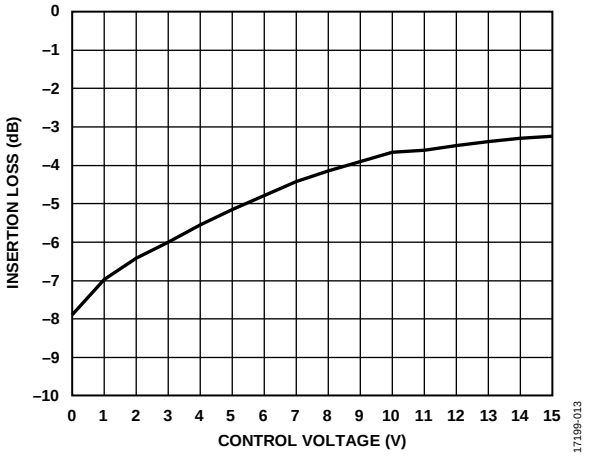


Figure 12. Insertion Loss vs. Control Voltage (V_{FCTL})

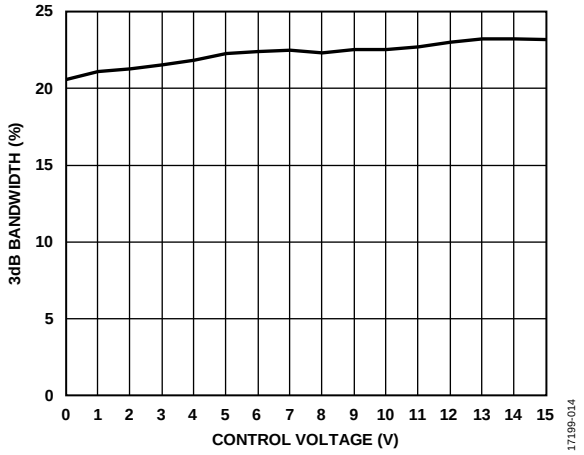


Figure 13. 3 dB Bandwidth vs. Control Voltage (V_{FCTL})

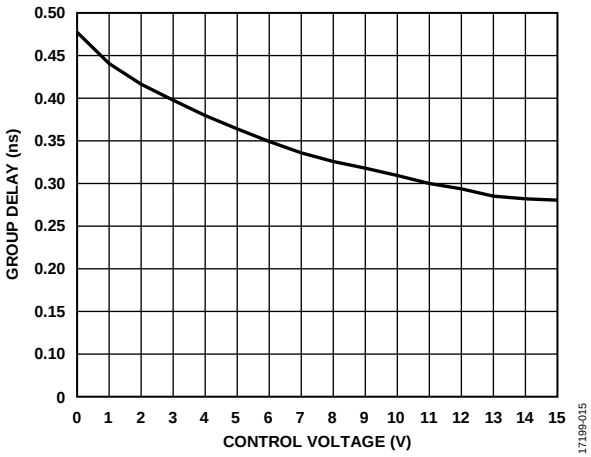


Figure 14. Group Delay vs. Control Voltage (V_{FCTL})

THEORY OF OPERATION

The ADMV8420 is a MMIC band-pass filter that features a user-selectable pass-band frequency. Varying the applied analog tune voltage between 0 V and 14 V at V_{FCTL} varies the center frequency between 10 GHz and 20 GHz.

APPLICATIONS INFORMATION

Figure 15 shows the typical application circuit for the ADMV8420. The RFIN pin and RFOUT pin are dc-coupled and require external 100 pF series capacitors (C1 and C2).

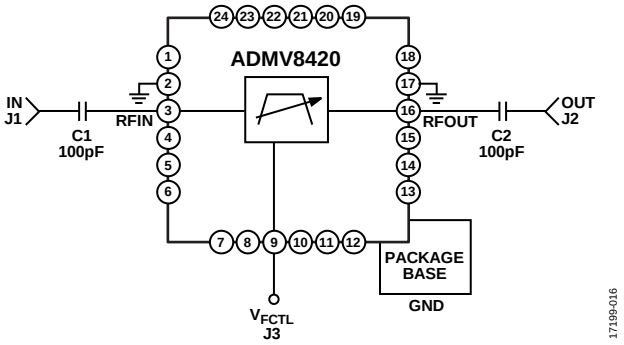
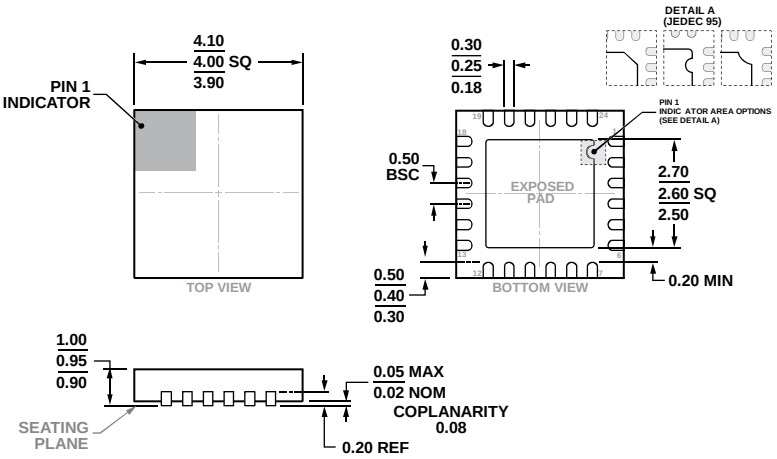


Figure 15. Typical Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 16. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.95 mm Package Height
CP-24-17
Dimensions shown in millimeters

PR17199-0-9/18(PrA)