High Speed, ±0.1 µV/°C Offset Drift, Fully Differential ADC Driver

Data Sheet

ADA4945-1

FEATURES

- Broad power supply range: 3 V to 10 V
- Wide input common-mode voltage range: $-V_S$ to $+V_S - 1.3$ V
- Rail-to-rail output
- Fully specified dual power mode operation
  - 4 mA full power mode (145 MHz)
  - 1.4 mA low power mode (80 MHz)
- Full power mode
  - Low harmonic distortion
  - −133 dBc HD2 and −140 dBc HD3 at 1 kHz
  - −133 dBc HD2 and −116 dBc HD3 at 100 kHz
  - Fast settling time
    - 18-bit: 100 ns
    - 16-bit: 50 ns
  - Input voltage noise: 1.8 nV/√Hz, f = 100 kHz
- ±115 µV maximum offset voltage from −40°C to +125°C
- Adjustable output clamps for ADC input protection

APPLICATIONS

- Low power Σ-Δ, PulSAR®, and SAR ADC drivers
- Single-ended to differential converters
- Differential buffers
- Medical imaging
- Process control
- Portable electronics

FUNCTIONAL BLOCK DIAGRAM

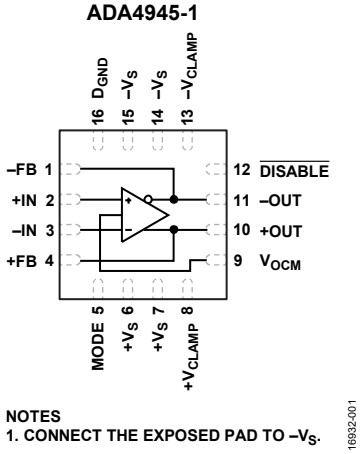


Figure 1.

GENERAL DESCRIPTION

The ADA4945-1 is a low noise, low distortion, fully differential amplifier with two selectable power modes. The device operates over a broad power supply range of 3 V to 10 V. The low dc offset, dc offset drift, and excellent dynamic performance of the ADA4945-1 makes it well suited for a variety of data acquisition and signal processing applications. The device is an ideal choice for driving high resolution, high performance successive approximation register (SAR) and Σ-Δ analog-to-digital converters (ADCs) on 4 mA of quiescent current (full power mode). The device can also be selected to operate on 1.4 mA of quiescent current (low power mode) to scale the power consumption to the desired performance necessary for an ADC drive application. The adjustable common-mode voltage allows the ADA4945-1 to match the input common-mode voltage of multiple ADCs. The internal common-mode feedback loop provides exceptional output balance, as well as suppression of even order harmonic distortion products.

With the ADA4945-1, differential gain configurations are achieved with a simple external feedback network of four resistors determining the closed-loop gain of the amplifier. The ADA4945-1 is fabricated using Analog Devices, Inc., proprietary, silicon germanium (SiGe), complementary bipolar process, enabling the device to achieve low levels of distortion with an input voltage noise of only 1.8 nV/√Hz (full power mode).

The ADA4945-1 is available in a RoHS-complaint, 3 mm × 3 mm, 16-lead LFCSP. The ADA4945-1 is specified to operate from −40°C to +125°C.

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REVISION HISTORY

4/2019—Revision 0: Initial Version

SPECIFICATIONS

SUPPLY VOLTAGE (V_S) = 10 V

Output common-mode voltage (V_{OCM}) = midsupply, Gain (G) = 1, feedback resistance (R_F) = gain resistance (R_G) = 499 Ω, differential load resistance ($R_{L, dm}$) = 1 kΩ, and T_A = 25°C, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 98 for circuit definitions.

Positive Input (+D_{IN}) or Negative Input (–D_{IN}) to Differential Output Voltage ($V_{OUT, dm}$) Performance

Table 1.

		Full Power Mode			Low Power Mode			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 20 mV p-p, G = 1		145			80		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 2		95			40		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 5		40			17		MHz
–3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2 V p-p, G = 1		60			18		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 2		54			40		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 5		52			16		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 20 mV p-p, G = 1		28			27		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 2		20			7		MHz
Slew Rate	$V_{OUT, dm}$ = 8 V step		600			100		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 8 V step		35			85		ns
Settling Time	16-bit		50			150		ns
	18-bit		100			300		ns
Input Overdrive Recovery	G = 1, differential input voltage ($V_{IN, dm}$) = 10 V p-p, triangular waveform		500			300		ns
Output Overdrive Recovery	G = 10, $V_{OUT, dm}$ = 22 V p-p, triangular waveform		200			120		ns
NOISE/HARMONIC PERFORMANCE	$V_{OUT, dm}$ = 8 V p-p							
Second Harmonic Distortion (HD2)	Center frequency (f_C) = 1 kHz		–133			–133		dBc
	f_C = 100 kHz		–133			–133		dBc
	f_C = 100 kHz, G = 2		–128			–128		dBc
	f_C = 1 MHz		–95			–68		dBc
Third Harmonic Distortion (HD3)	f_C = 1 kHz		–140			–138		dBc
	f_C = 100 kHz		–116			–116		dBc
	f_C = 100 kHz, G = 2		–123			–122		dBc
	f_C = 1 MHz		–88			–62		dBc
Input Voltage Noise								
Differential	Frequency under test							
	f = 10 Hz		5			7		nV/√Hz
	f = 100 kHz		1.8			3		nV/√Hz
	1/f corner frequency		100			40		Hz
Common Mode	f = 10 Hz		350			284		nV/√Hz
	f = 100 kHz		30			38		nV/√Hz
	1/f corner frequency		1000			1000		nV/√Hz

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
Integrated Voltage Noise	0.1 Hz to 10 Hz		35			25		nV rms
Input Current Noise	f = 10 Hz		11			4		pA/√Hz
	f = 100 kHz		1.0			0.6		pA/√Hz
	1/f corner frequency		2000			1000		Hz
INPUT CHARACTERISTICS								
Input Offset Voltage	25°C		±10	±50		±10	±50	μV
	T_A = 20°C to 85°C		±15	±80		±15	±80	μV
	T_A = −40°C to +125°C		±30	±115		±30	±115	μV
Input Offset Voltage Drift	T_A = 20°C to 85°C		±0.1	±0.5		±0.1	±0.5	μV/°C
	T_A = −40°C to +125°C		±0.2	±1.0		±0.2	±1.0	μV/°C
Input Bias Current	T_A = 25°C		−1.2	−2.5		−0.5	−0.8	μA
	T_A = 20°C to 85°C		−1.5	−3.0		−0.6	−1.0	μA
	T_A = −40°C to +125°C		−1.8	−3.4		−0.7	−1.2	μA
Input Bias Current Drift	T_A = 20°C to 85°C		−10	−50		−10	−50	nA/°C
	T_A = −40°C to +125°C		−10	−50		−10	−50	nA/°C
Input Offset Current	T_A = 25°C		±20	±200		±10	±130	nA
	T_A = 20°C to 85°C		±25	±250		±20	±150	nA
	T_A = −40°C to +125°C		±40	±300		±25	±200	nA
Input Offset Current Drift	T_A = 20°C to 85°C		±0.1	±0.6		±0.06	±0.38	nA/°C
	T_A = −40°C to +125°C		±0.12	±0.7		±0.07	±0.4	nA/°C
Input Common-Mode Voltage (V_{CM}) Range		$-V_S$		$+V_S - 1.3$	$-V_S$		$+V_S - 1.3$	V
Input Resistance	Differential		50			50		kΩ
	Common mode		50			50		MΩ
Input Capacitance			1			1		pF
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0.5 V to 9 V		−110			−110		dB
Open-Loop Gain	Output voltage (V_{OUT}) = ±4 V		120			115		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Load resistance (R_L) = 100 Ω for each single-ended output	$-V_S + 0.55$		$+V_S - 0.55$	$-V_S + 0.55$		$+V_S - 0.55$	V
	R_L = 1 kΩ	$-V_S + 0.1$		$+V_S - 0.1$	$-V_S + 0.1$		$+V_S - 0.1$	V
Short-Circuit Current			170			140		mA peak
Output Balance Error	f = 100 kHz, $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$		100			100		dB

V_{OCM} to Common-Mode Output Voltage ($V_{OUT, cm}$) Performance

Table 2.

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{OCM} DYNAMIC PERFORMANCE								
−3 dB Small Signal Bandwidth	$V_{OUT, cm}$ = 20 mV p-p		35			15		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, cm}$ = 2 V p-p		3.8			1.3		MHz
Slew Rate	$V_{OUT, cm}$ = 2 V p-p		26			9		V/µs
Input Voltage Noise	f = 100 kHz		35			45		nV/√Hz
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.99	1	1.01	0.99	1	1.01	V/V
V_{OCM} CHARACTERISTICS								
Input Common-Mode Voltage Range		$-V_S + 0.4$		$+V_S - 1.4$	$-V_S + 0.4$		$+V_S - 1.4$	V
Input Resistance			125			125		kΩ
Offset Voltage	Common mode offset ($V_{OS, cm}$) = $V_{OUT, cm} - V_{OCM}$, positive input (V_{IP}) = negative input (V_{IN}) = V_{OCM} = 0 V							
	25°C		±5	±60		±5	±60	mV
	T_A = 20°C to 85°C		±10			±10		mV
	T_A = −40°C to +125°C		±20			±20		mV
Input Offset Voltage Drift	T_A = 20°C to 85°C		±5			±5		µV/°C
	T_A = −40°C to +125°C		±10			±10		µV/°C
Input Bias Current	T_A = 25°C		−220			−160		µA
	T_A = 20°C to 85°C		−300			−205		µA
	T_A = −40°C to +125°C		−350			−230		µA
Input Bias Current Drift	T_A = 20°C to 85°C		−1.3			−0.75		µA/°C
	T_A = −40°C to +125°C		−1.5			−1.0		µA/°C
CMRR	$\Delta V_{OS, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−130			−130		dB

General Performance

Table 3.

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
CLAMP								
Clamp Output Voltage	Differential	$-V_S - 0.5$		$+V_S + 0.5$	$-V_S - 0.5$		$+V_S + 0.5$	V
	Common mode	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Recovery Time			100			100		ns
Input Resistance	Resistance between $+V_{CLAMP}$ and $-V_{CLAMP}$		480			480		kΩ
DISABLE ($\overline{\text{DISABLE}}$ PIN) MODE								
Input Voltage	Disabled	$-V_S - 0.3$		$D_{GND} + 1$	$-V_S - 0.3$		$D_{GND} + 1$	V
	Enabled	$D_{GND} + 1.4$		$V_S + 0.3$	$D_{GND} + 1.4$		$V_S + 0.3$	V
Turn Off Time	Quiescent current <10% of enabled quiescent current		6			6		µs
Turn On Time	Turn on time (t_O) >90% of final V_{OUT}		1.2			2		µs
$\overline{\text{DISABLE}}$ Pin Bias Current								
Enabled	$\overline{\text{DISABLE}}$ = 10 V		50			50		nA
Disabled	$\overline{\text{DISABLE}}$ = 0 V		50			50		nA
D_{GND} PIN VOLTAGE RANGE		$-V_S$		$+V_S - 2.5$	$-V_S$		$+V_S - 2.5$	V
POWER SUPPLY								
Operating Range		3		10	3		10	V
Quiescent Current								
Enabled	Full power mode, MODE = $+V_S$		4	4.2				mA
	Low power mode, MODE = $-V_S$					1.4	1.6	mA
Disabled	Full power mode, MODE = $+V_S$		60	70				µA
	Low power mode, MODE = $-V_S$					60	70	µA
Positive Power Supply Rejection Ratio (+PSRR)	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−120			−120		dB
Negative Power Supply Rejection Ratio (−PSRR)	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−120			−120		dB
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

V_S = 5 V

V_{OCM} = midsupply, G = 1, R_F = R_G = 499 Ω, $R_{L, dm}$ = 1 kΩ, T_A = 25°C, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 98 for circuits definitions.

+D_{IN} or –D_{IN} to $V_{OUT, dm}$ Performance

Table 4.

Parameter	Test Conditions/Comments	Full Power Mode Min	Full Power Mode Typ	Full Power Mode Max	Low Power Mode Min	Low Power Mode Typ	Low Power Mode Max	Unit
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 20 mV p-p, G = 1		145			80		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 2		95			40		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 5		40			17		MHz
–3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2 V p-p, G = 1		60			18		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 2		54			40		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 5		52			16		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 20 mV p-p, G = 1		28			27		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 2		20			7		MHz
Slew Rate	$V_{OUT, dm}$ = 8 V step		600			100		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 8 V step		35			85		ns
Settling Time	16-bit		50			150		ns
	18-bit		100			300		ns
Input Overdrive Recovery	G = 1, $V_{IN, dm}$ = 10 V p-p, triangular waveform		300			500		ns
Output Overdrive Recovery	G = 2, $V_{OUT, dm}$ = 12 V p-p, triangular waveform		145			80		ns
NOISE/HARMONIC PERFORMANCE	$V_{OUT, dm}$ = 8 V p-p							
HD2	Center frequency (f_C) = 1 kHz		–133			–133		dBc
	f_C = 100 kHz		–133			–133		dBc
	f_C = 100 kHz, G = 2		–128			–128		dBc
	f_C = 1 MHz		–95			–68		dBc
HD3	f_C = 1 kHz		–140			–138		dBc
	f_C = 100 kHz		–116			–116		dBc
	f_C = 100 kHz, G = 2		–123			–122		dBc
	f_C = 1 MHz		–88			–62		dBc
Input Voltage Noise								
Differential	f = 10 Hz		5			7		nV/√Hz
	f = 100 kHz		1.8			3		nV/√Hz
	1/f corner frequency		100			40		Hz
Common Mode	f = 10 Hz		350			284		nV/√Hz
	f = 100 kHz		30			38		nV/√Hz
	1/f corner frequency		1000			1000		nV/√Hz
Integrated Voltage Noise	0.1 Hz to 10 Hz		35			25		nV rms
Input Current Noise	f = 10 Hz		11			4		pA/√Hz
	f = 100 kHz		1.0			0.6		pA/√Hz
	1/f corner frequency		2000			1000		Hz

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input Offset Voltage	25°C		±10	±50		±10	±50	μV
	T_A = 20°C to 85°C		±15	±80		±15	±80	μV
	T_A = −40°C to +125°C		±30	±115		±30	±115	μV
Input Offset Voltage Drift	T_A = 20°C to 85°C		±0.1	±0.5		±0.1	±0.5	μV/°C
	T_A = −40°C to +125°C		±0.2	±1.0		±0.2	±1.0	μV/°C
Input Bias Current	T_A = 25°C		−1.2	−2.5		−0.5	−0.8	μA
	T_A = 20°C to 85°C		−1.5	−3.0		−0.6	−1.0	μA
	T_A = −40°C to +125°C		−1.8	−3.4		−0.7	−1.2	μA
Input Bias Current Drift	T_A = 20°C to 85°C		−10	−50		−10	−50	nA/°C
	T_A = −40°C to +125°C		−10	−50		−10	−50	nA/°C
Input Offset Current	T_A = 25°C		±20	±200		±10	±130	nA
	T_A = 20°C to 85°C		±25	±250		±20	±150	nA
	T_A = −40°C to +125°C		±40	±300		±25	±200	nA
Input Offset Current Drift	T_A = 20°C to 85°C		±0.1	±0.6		±0.06	±0.38	nA/°C
	T_A = −40°C to +125°C		±0.12	±0.7		±0.07	±0.4	nA/°C
V_{CM} Range		$-V_S$		$+V_S - 1.3$	$-V_S$		$+V_S - 1.3$	V
Input Resistance	Differential		50			50		kΩ
	Common mode		50			50		MΩ
Input Capacitance			1			1		pF
CMRR	V_{CM} = 0.5 V to 9 V		−110			−110		dB
Open-Loop Gain	V_{OUT} = ±4 V		120			115		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 100 Ω	$-V_S$ + 0.55		$+V_S - 0.55$	$-V_S + 0.55$		$+V_S - 0.55$	V
	R_L = 1 kΩ	$-V_S + 0.1$		$+V_S - 0.1$	$-V_S + 0.1$		$+V_S - 0.1$	V
Short-Circuit Current			170			140		mA peak
Output Balance Error	f = 100 kHz, $\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$		100			100		dB

V_{OCM} to $V_{OUT, cm}$ Performance

Table 5.

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{OCM} DYNAMIC PERFORMANCE								
−3 dB Small Signal Bandwidth	$V_{OUT, cm}$ = 20 mV p-p		35			15		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, cm}$ = 2 V p-p		3.8			1.3		MHz
Slew Rate	$V_{OUT, cm}$ = 2 V p-p		26			9		V/µs
Input Voltage Noise	f = 100 kHz		35			45		nV/√Hz
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.99	1	1.01	0.99	1	1.01	V/V
V_{OCM} CHARACTERISTICS								
Input Common-Mode Voltage Range		$-V_S + 0.4$		$+V_S - 1.4$	$-V_S + 0.4$		$+V_S - 1.4$	V
Input Resistance			125			125		kΩ
Offset Voltage	$V_{OS, cm} = V_{OUT, cm} - V_{OCM}$, $V_{IP} = V_{IN} = V_{OCM}$ = 0 V							
	25°C		±10	±60		±10	±60	mV
	T_A = 20°C to 85°C		±10			±10		mV
	T_A = −40°C to +125°C		±20			±20		mV
Input Offset Voltage Drift	T_A = 20°C to 85°C		±5			±5		µV/°C
	T_A = −40°C to +125°C		±10			±10		µV/°C
Input Bias Current	T_A = 25°C		−220			−160		µA
	T_A = 20°C to 85°C		−300			−205		µA
	T_A = −40°C to +125°C		−350			−230		µA
Input Bias Current Drift	T_A = 20°C to 85°C		−1.3			−0.75		µA/°C
	T_A = −40°C to +125°C		−1.5			−1.0		µA/°C
CMRR	$\Delta V_{OS, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−130			−130		dB

General Performance

Table 6.

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
CLAMP								
Clamp Output Voltage	Differential	$-V_S - 0.5$		$+V_S + 0.5$	$-V_S - 0.5$		$+V_S + 0.5$	V
	Common mode	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Recovery Time			100			100		ns
Input Resistance	Resistance between $+V_{CLAMP}$ and $-V_{CLAMP}$		480			480		kΩ
DISABLE ($\overline{\text{DISABLE}}$ PIN) MODE								
Input Voltage	Disabled	$-V_S - 0.3$		$D_{GND} + 1$	$-V_S - 0.3$		$D_{GND} + 1$	V
	Enabled	$D_{GND} + 1.4$		$+V_S + 0.3$	$D_{GND} + 1.4$		$+V_S + 0.3$	V
Turn Off Time	Quiescent current <10% of enabled quiescent current		6			6		µs
Turn On Time	t_O >90% of final V_{OUT}		1.2			2		µs
$\overline{\text{DISABLE}}$ Pin Bias Current								
Enabled	$\overline{\text{DISABLE}}$ = 5 V		50			50		nA
Disabled	$\overline{\text{DISABLE}}$ = 0 V		50			50		nA
D_{GND} PIN VOLTAGE RANGE		$-V_S$		$+V_S - 2.5$	$-V_S$		$+V_S - 2.5$	V
POWER SUPPLY								
Operating Range		3		10	3		10	V
Quiescent Current								
Enabled	Full power mode, MODE = $+V_S$		4	4.2				mA
	Low power mode, MODE = $-V_S$					1.4	1.6	mA
Disabled	Full power mode, MODE = $+V_S$		60	70				µA
	Low power mode, MODE = $-V_S$					60	70	µA
+PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−120			−120		dB
−PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−120			−120		dB
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

V_S = 3 V

V_{OCM} = midsupply, G = 1, R_F = R_G = 499 Ω, $R_{L, dm}$ = 1 kΩ, T_A = 25°C, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 98 for circuit definitions.

+D_{IN} or –D_{IN} to $V_{OUT, dm}$ Performance

Table 7.

		Full Power Mode			Low Power Mode			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 20 mV p-p, G = 1		145			80		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 2		95			40		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 5		40			17		MHz
–3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2 V p-p, G = 1		22			11		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 20 mV p-p, G = 1		28			27		MHz
	$V_{OUT, dm}$ = 20 mV p-p, G = 2		20			7		MHz
Slew Rate	$V_{OUT, dm}$ = 4 V step		600			100		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 4 V step		35			85		ns
Settling Time	16-bit		50			150		ns
	18-bit		100			300		ns
Input Overdrive Recovery	G = –1, $V_{IN, dm}$ = 3 V p-p, triangular waveform		500			300		ns
Output Overdrive Recovery	G = 2, $V_{OUT, dm}$ = 6 V p-p, triangular waveform		200			120		ns
NOISE/HARMONIC PERFORMANCE	$V_{OUT, dm}$ = 4 V p-p							
HD2	f_C = 1 kHz		–133			–133		dBc
	f_C = 100 kHz		–133			–133		dBc
	f_C = 100 kHz, G = 2		–128			–128		dBc
	f_C = 1 MHz		–95			–68		dBc
HD3	f_C = 1 kHz		–140			–138		dBc
	f_C = 100 kHz		–116			–116		dBc
	f_C = 100 kHz, G = 2		–123			–122		dBc
	f_C = 1 MHz		–88			–62		dBc
Input Voltage Noise								
Differential	f = 10 Hz		5			7		nV/√Hz
	f = 100 kHz		1.8			3		nV/√Hz
	1/f corner frequency		100			40		Hz
Common Mode	f = 10 Hz		350			284		nV/√Hz
	f = 100 kHz		30			38		nV/√Hz
	1/f corner frequency		1000			1000		nV/√Hz
Integrated Voltage Noise	0.1 Hz to 10 Hz		35			25		nV rms
Input Current Noise	f = 10 Hz		11			4		pA/√Hz
	f = 100 kHz		1.0			0.6		pA/√Hz
	1/f corner frequency		2000			1000		Hz

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input Offset Voltage	25°C		±10	±50		±10	±50	μV
	T_A = 20°C to 85°C		±15	±80		±15	±80	μV
	T_A = −40°C to +125°C		±30	±115		±30	±115	μV
Input Offset Voltage Drift	T_A = 20°C to 85°C		±0.1	±0.5		±0.1	±0.5	μV/°C
	T_A = −40°C to +125°C		±0.2	±1.0		±0.2	±1.0	μV/°C
Input Bias Current	T_A = 25°C		−1.2	−2.5		−0.5	−0.8	μA
	T_A = 20°C to 85°C		−1.5	−3.0		−0.6	−1.0	μA
	T_A = −40°C to +125°C		−1.8	−3.4		-0.7	−1.2	μA
Input Bias Current Drift	T_A = 20°C to 85°C		−10	−50		−10	−50	nA/°C
	T_A = −40°C to +125°C		−10	−50		−10	−50	nA/°C
Input Offset Current	T_A = 25°C		±20	±200		±10	±130	nA
	T_A = 20°C to 85°C		±25	±250		±20	±150	nA
	T_A = −40°C to +125°C		±40	±300		±25	±200	nA
Input Offset Current Drift	T_A = 20°C to 85°C		±0.1	±0.6		±0.06	±0.38	nA/°C
	T_A = −40°C to +125°C		±0.12	±0.7		±0.07	±0.4	nA/°C
V_{CM} Range		$-V_S$		$+V_S - 1.3$	$-V_S$		$+V_S - 1.3$	V
Input Resistance	Differential		50			50		kΩ
	Common mode		50			50		MΩ
Input Capacitance			1			1		pF
CMRR	V_{CM} = 0.5 V to 9 V		−110			−110		dB
Open-Loop Gain	V_{OUT} = ±4 V		120			115		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 100 Ω	$-V_S + 0.55$		$+V_S - 0.55$	$-V_S + 0.55$		$+V_S - 0.55$	V
	R_L = 1 kΩ	$-V_S + 0.1$		$+V_S - 0.1$	$-V_S + 0.1$		$+V_S - 0.1$	V
Short-Circuit Current			170			140		mA peak
Output Balance Error	f = 100 kHz, $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$		100			100		dB

V_{OCM} to $V_{OUT, cm}$ Performance

Table 8.

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{OCM} DYNAMIC PERFORMANCE								
−3 dB Small Signal Bandwidth	$V_{OUT, cm}$ = 20 mV p-p		35			15		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, cm}$ = 2 V p-p		3.8			1.3		MHz
Slew Rate	$V_{OUT, cm}$ = 2 V p-p		26			9		V/µs
Input Voltage Noise	f = 100 kHz		35			45		nV/√Hz
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.99	1	1.01	0.99	1	1.01	V/V
V_{OCM} CHARACTERISTICS								
Input Common-Mode Voltage Range		$-V_S + 0.4$		$+V_S - 1.4$	$-V_S + 0.4$		$+V_S - 1.4$	V
Input Resistance			125			125		kΩ
Offset Voltage	$V_{OS, cm} = V_{OUT, cm} - V_{OCM}$, $V_{IP} = V_{IN} = V_{OCM}$ = 0 V							
	25°C		±10	±60		±10	±60	mV
	T_A = 20°C to 85°C		±10			±10		mV
	T_A = −40°C to +125°C		±20			±20		mV
Input Offset Voltage Drift	T_A = 20°C to 85°C		±5			±5		µV/°C
	T_A = −40°C to +125°C		±10			±10		µV/°C
Input Bias Current	T_A = 25°C		−220			−160		µA
	T_A = 20°C to 85°C		−300			−205		µA
	T_A = −40°C to +125°C		−350			−230		µA
Input Bias Current Drift	T_A = 20°C to 85°C		−1.3			−0.75		µA/°C
	T_A = −40°C to +125°C		−1.5			−1.0		µA/°C
CMRR	$\Delta V_{OS, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−130			−130		dB

General Performance

Table 9.

Parameter	Test Conditions/Comments	Full Power Mode			Low Power Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
CLAMP								
Clamp Output Voltage	Differential	$-V_S - 0.5$		$+V_S + 0.5$	$-V_S - 0.5$		$+V_S + 0.5$	V
	Common mode	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Recovery Time			100			100		ns
Input Resistance	Resistance between $+V_{CLAMP}$ and $-V_{CLAMP}$		480			480		kΩ
DISABLE ($\overline{\text{DISABLE}}$ PIN) MODE								
Input Voltage	Disabled	$-V_S - 0.3$		$D_{GND} + 1$	$-V_S - 0.3$		$D_{GND} + 1$	V
	Enabled	$D_{GND} + 1.4$		$+V_S + 0.3$	$D_{GND} + 1.4$		$+V_S + 0.3$	V
Turn Off Time	Quiescent current <10% of enabled quiescent current		6			6		µs
Turn On Time	t_O >90% of final V_{OUT}		1.2			2		µs
$\overline{\text{DISABLE}}$ Pin Bias Current								
Enabled	$\overline{\text{DISABLE}}$ = 3 V		50			50		nA
Disabled	$\overline{\text{DISABLE}}$ = 0 V		50			50		nA
D_{GND} PIN VOLTAGE RANGE		$-V_S$		$+V_S - 2.5$	$-V_S$		$+V_S - 2.5$	V
POWER SUPPLY								
Operating Range		3		10	3		10	V
Quiescent Current								
Enabled	Full power mode, MODE = $+V_S$		4	4.2				mA
	Low power mode, MODE = $-V_S$					1.4	1.6	mA
Disabled	Full power mode, MODE = $+V_S$		60	70				µA
	Low power mode, MODE = $-V_S$					60	70	µA
+PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−120			−120		dB
−PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−120			−120		dB
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
Supply Voltage	11 V
V_{OCM}	$\pm V_S$
Differential Input Voltage	±1 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C
Electrostatic Discharge (ESD)	
Field Induced Charged Device Model (FICDM)	1250 V
Human Body Model (HBM)	4000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient, thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 11.

Package Type	θ_{JA}	θ_{JC}	Unit
CP-16-22	70	15	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4945-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of ADA4945-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) times the quiescent current (I_S). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. Consider RMS voltages and currents when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP (θ_{JA} = 70°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

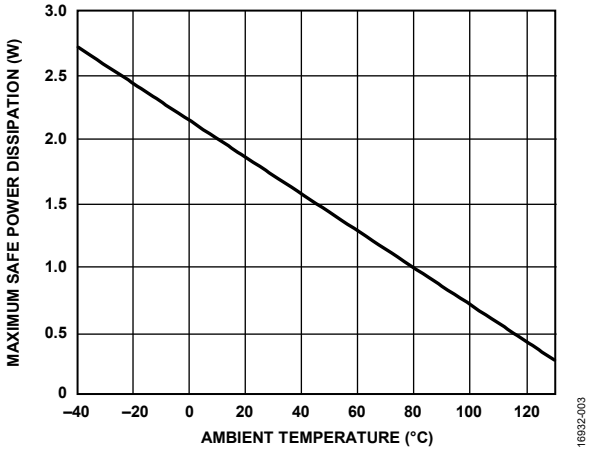


Figure 2. Maximum Safe Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

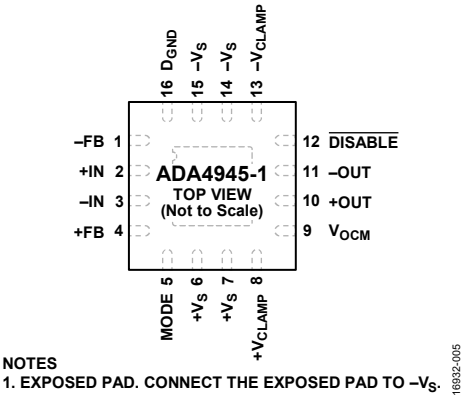


Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–FB	Negative Output for Feedback Component Connection.
2	+IN	Positive Input Summing Node.
3	–IN	Negative Input Summing Node.
4	+FB	Positive Output for Feedback Component Connection.
5	MODE	Selects Between Full Power Mode and Low Power Mode.
6	$+V_S$	Positive Supply Voltage.
7	$+V_S$	Positive Supply Voltage.
8	$+V_{CLAMP}$	Positive Clamp Level.
9	V_{OCM}	Output Common-Mode Voltage.
10	+OUT	Positive Output for Load Connection.
11	–OUT	Negative Output for Load Connection.
12	$\overline{\text{DISABLE}}$	Disable Pin.
13	$-V_{CLAMP}$	Negative Clamp Level.
14	$-V_S$	Negative Supply Voltage.
15	$-V_S$	Negative Supply Voltage.
16	D_{GND}	Digital Ground Level.
	Exposed pad (EPAD)	Exposed Pad. Connect the exposed pad to $-V_S$.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, V_S = ±5 V, G = 1, R_F = R_G = 499 Ω, R_T = 53.6 Ω (when used), and R_L = 1 kΩ, unless otherwise noted. See Figure 94, Figure 95, Figure 96, and Figure 97 for the test circuits.

FULL POWER MODE

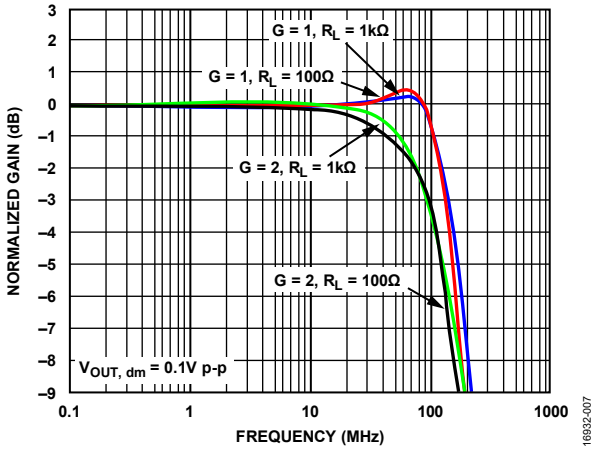


Figure 4. Small Signal Frequency Response for Various Gains and Loads

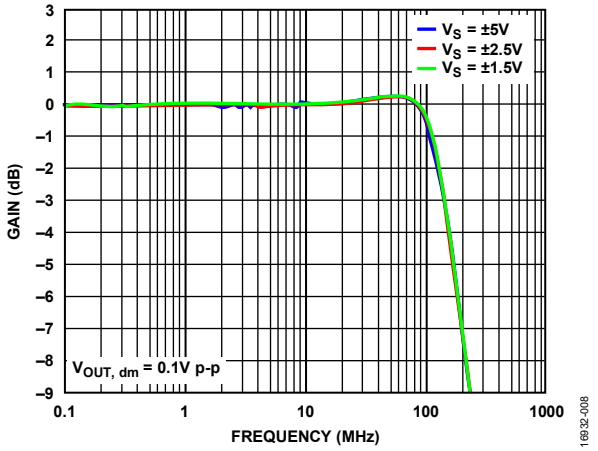


Figure 5. Small Signal Frequency Response for Various Supplies

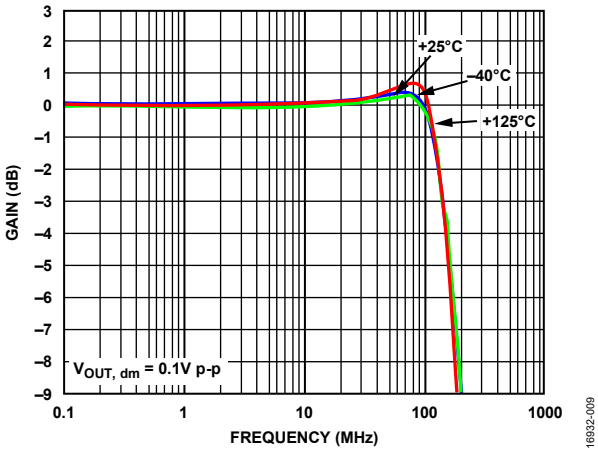


Figure 6. Small Signal Frequency Response for Various Temperatures

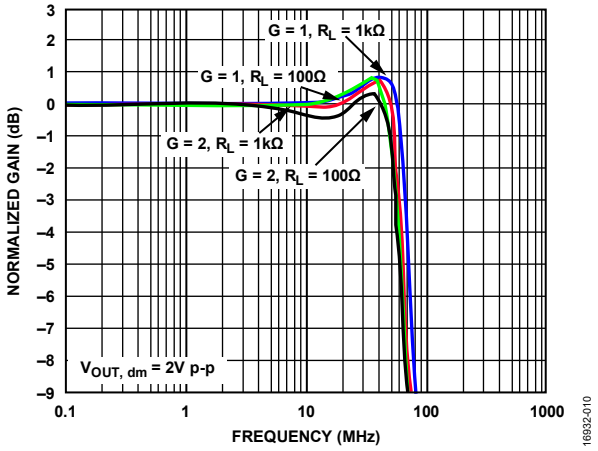


Figure 7. Large Signal Frequency Response for Various Gains and Loads

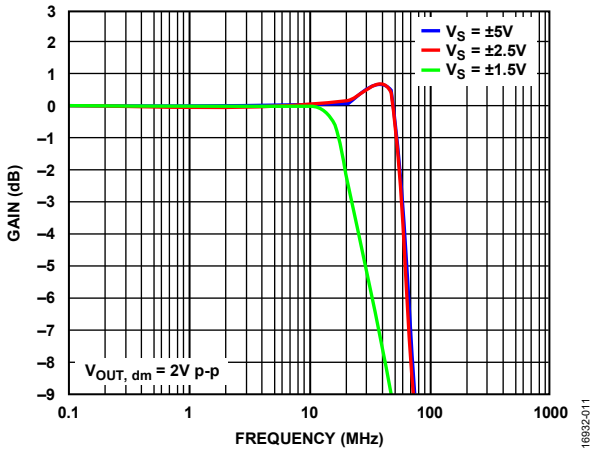


Figure 8. Large Signal Frequency Response for Various Supplies

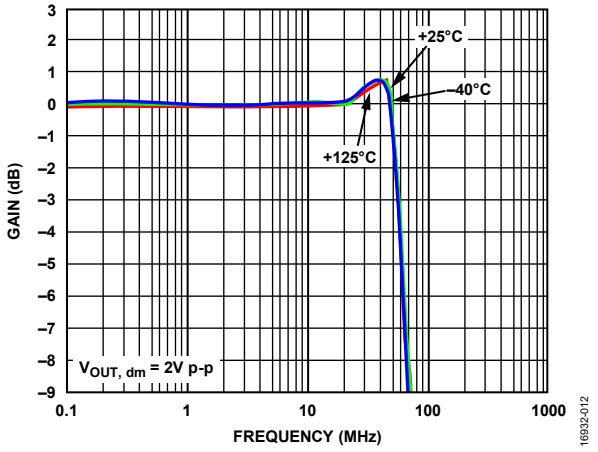


Figure 9. Large Signal Frequency Response for Various Temperatures

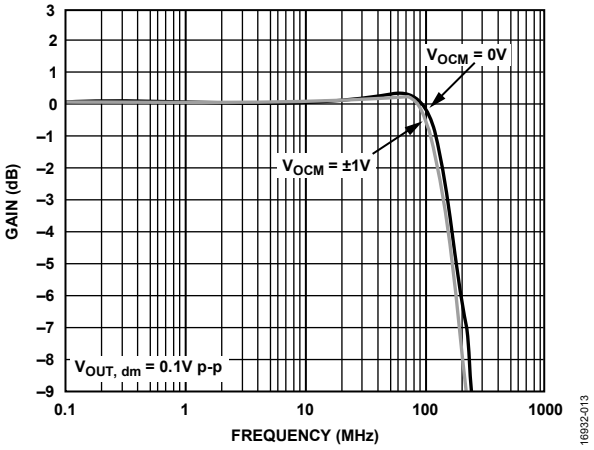


Figure 10. Small Signal Frequency Response at Various V_{OCM} Levels

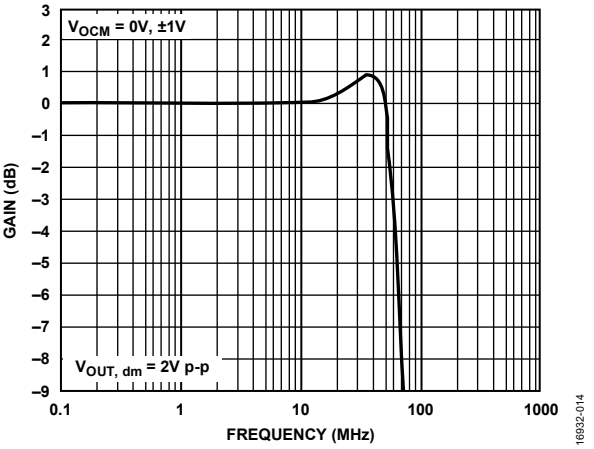


Figure 11. Large Signal Frequency Response at Various V_{OCM} Levels

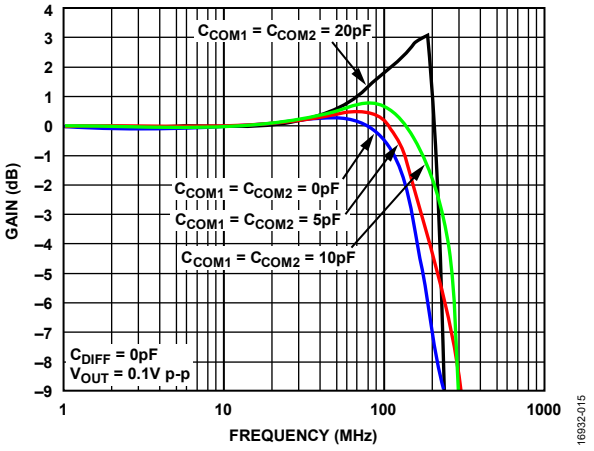


Figure 12. Small Signal Frequency Response for Various Capacitive Loads

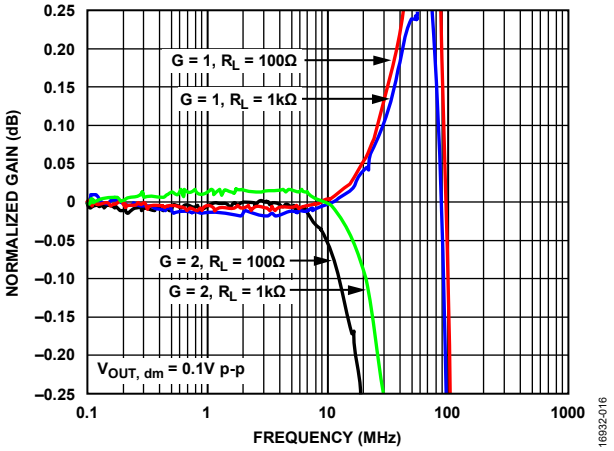


Figure 13. 0.1 dB Flatness Small Signal Frequency Response for Various Gains and Loads

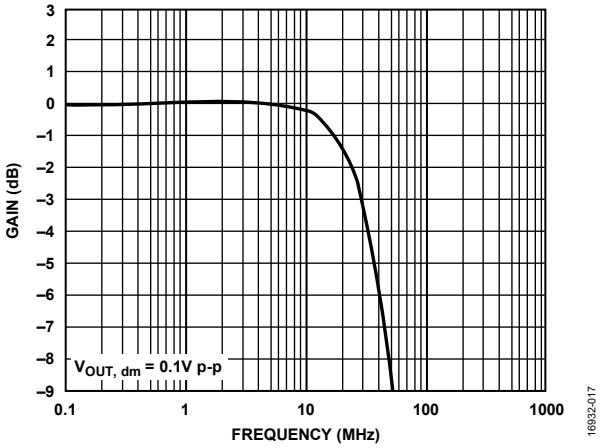


Figure 14. V_{OCM} Small Signal Frequency Response

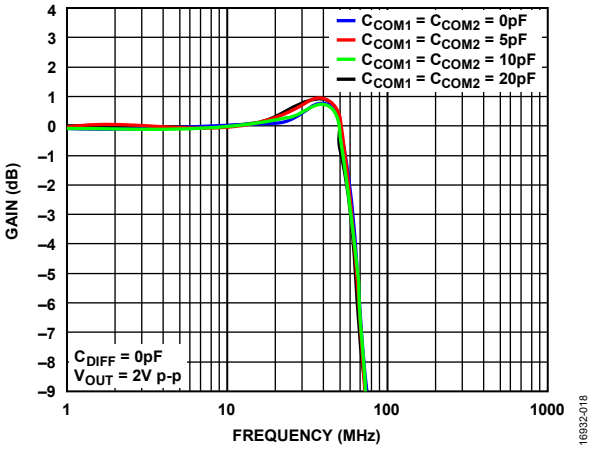


Figure 15. Large Signal Frequency Response for Various Capacitive Loads

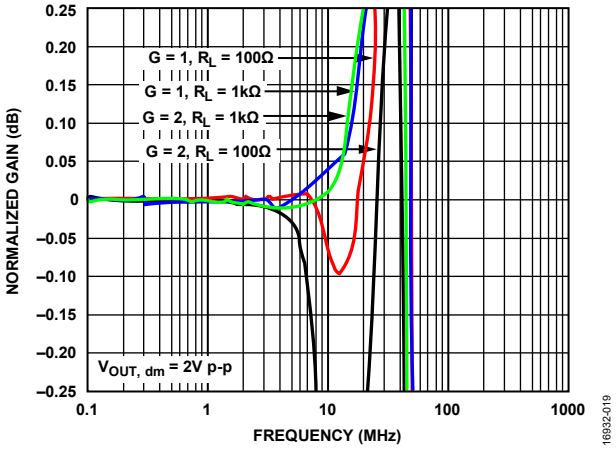


Figure 16. 0.1 dB Flatness Large Signal Frequency Response for Various Gains and Loads

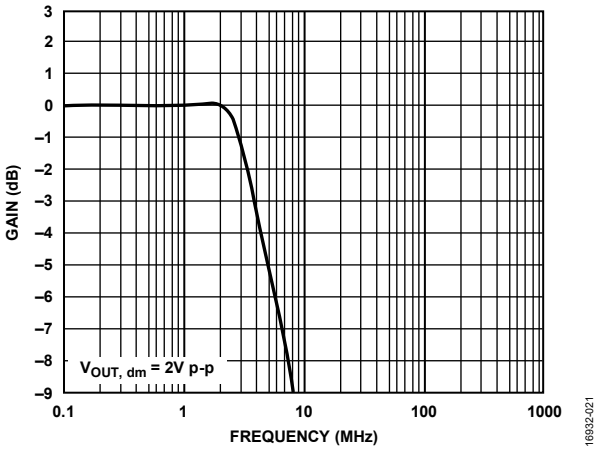


Figure 17. V_{OCM} Large Signal Frequency Response

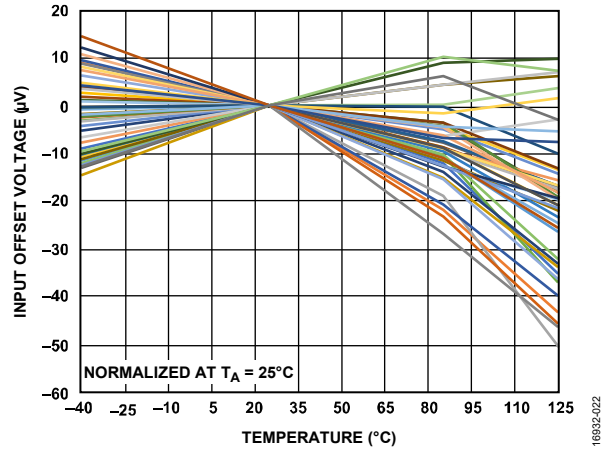


Figure 18. Input Offset Voltage vs. Temperature for 50 Devices

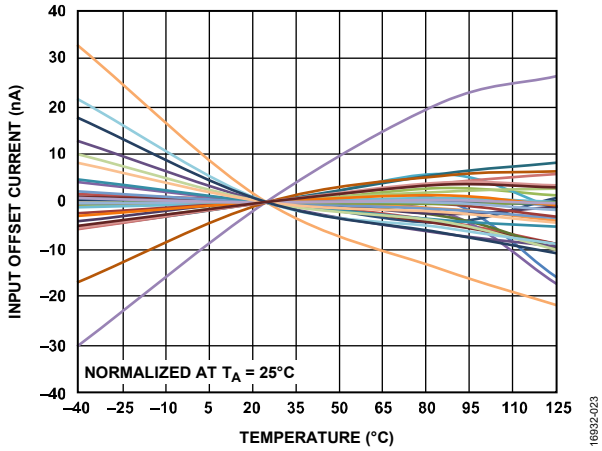


Figure 19. Input Offset Current vs. Temperature for 30 Devices

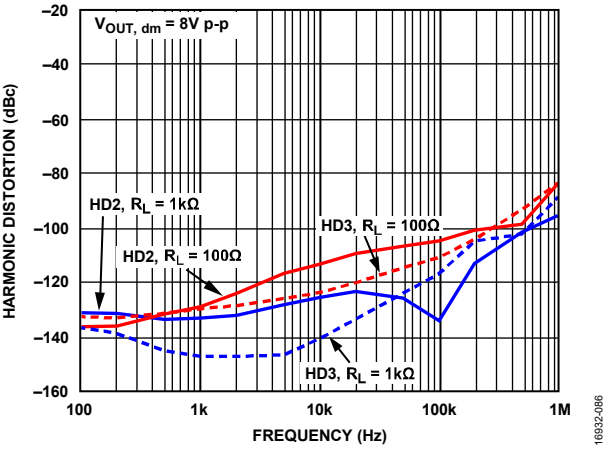


Figure 20. Harmonic Distortion vs. Frequency for Various Loads

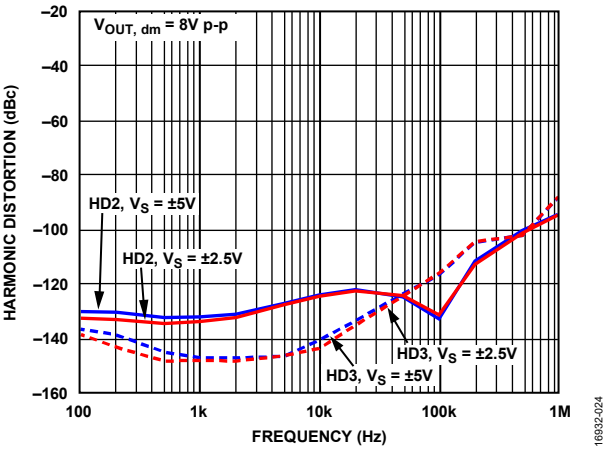


Figure 21. Harmonic Distortion vs. Frequency for Various Supplies

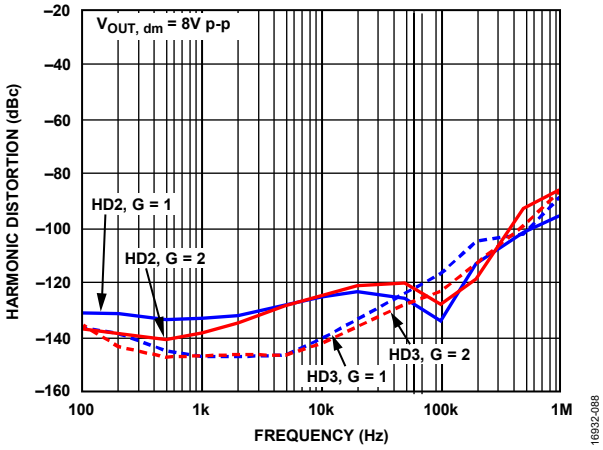


Figure 22. Harmonic Distortion vs. Frequency for Various Gains

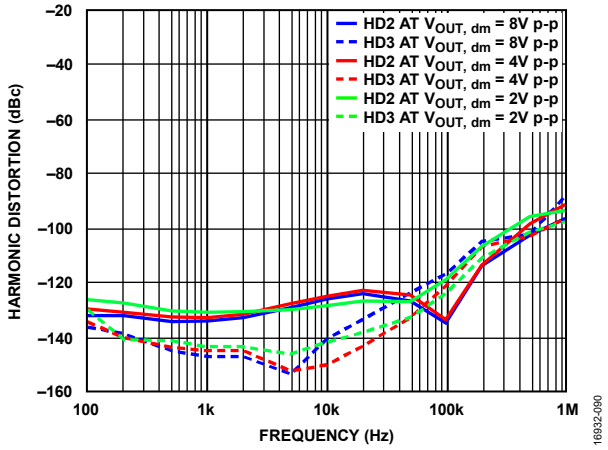


Figure 25. Harmonic Distortion vs. Frequency for Various $V_{OUT, dm}$

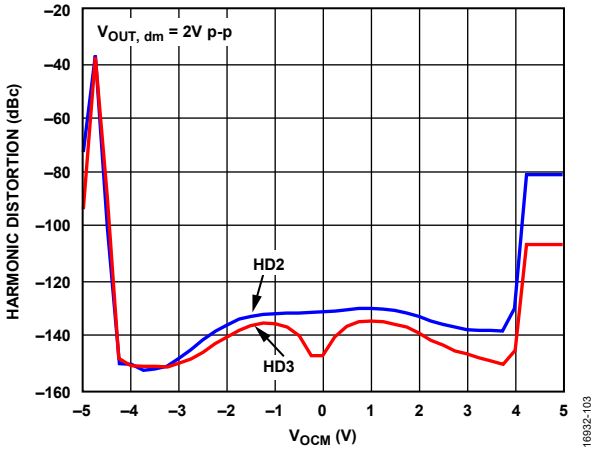


Figure 23. Harmonic Distortion vs. V_{OCM}, f = 1 kHz, ±5 V Supplies

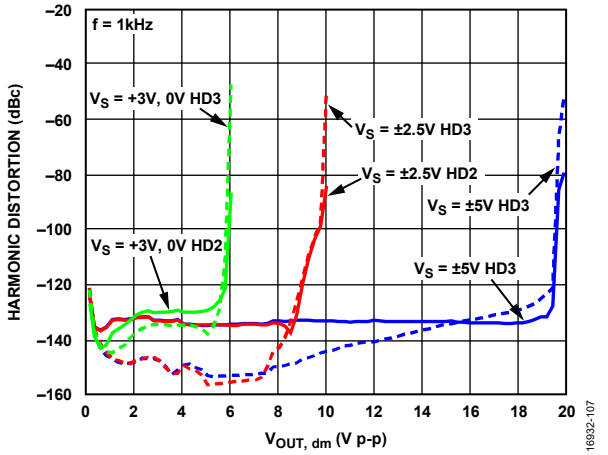


Figure 26. Harmonic Distortion vs. $V_{OUT, dm}$ for Various Supplies, f = 1 kHz

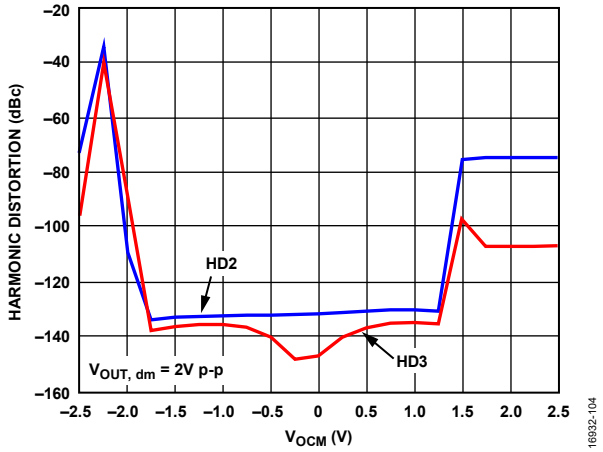


Figure 24. Harmonic Distortion vs. V_{OCM}, f = 1 kHz, ±2.5 V Supplies

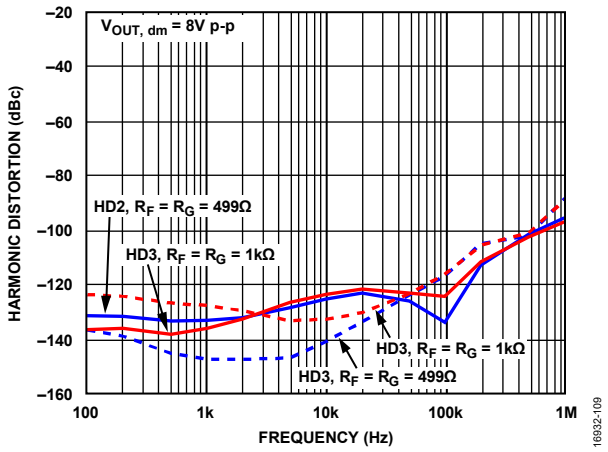


Figure 27. Harmonic Distortion vs. Frequency for Various R_F and R_G Values

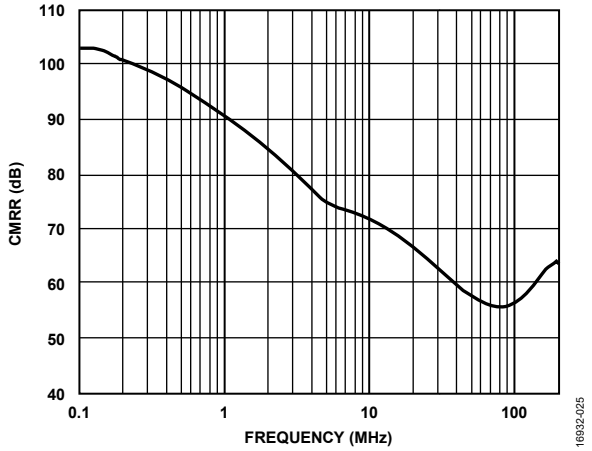


Figure 28. CMRR vs. Frequency

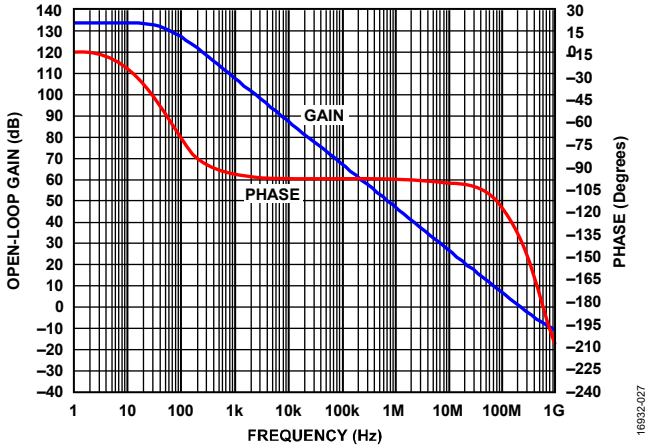


Figure 31. Open-Loop Gain and Phase vs. Frequency

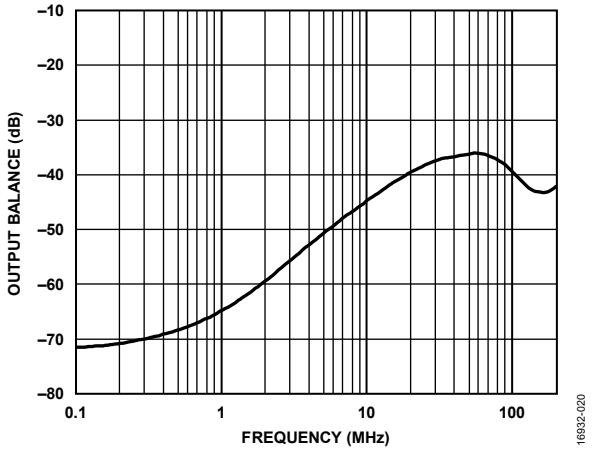


Figure 29. Output Balance vs. Frequency

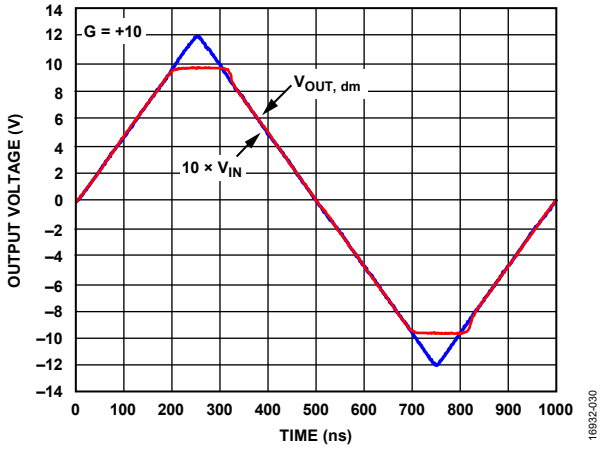


Figure 32. Output Overdrive Recovery, G = 2

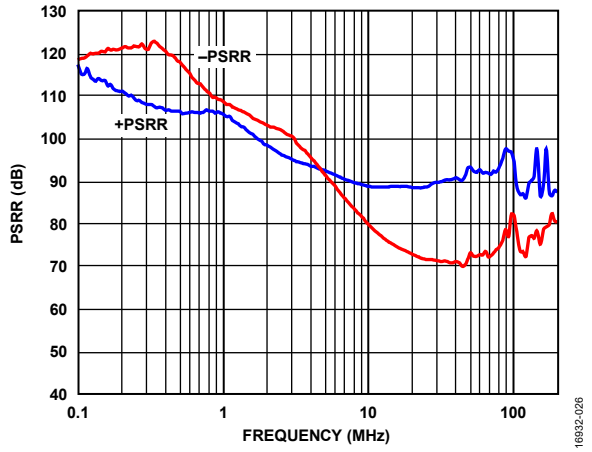


Figure 30. PSRR vs. Frequency

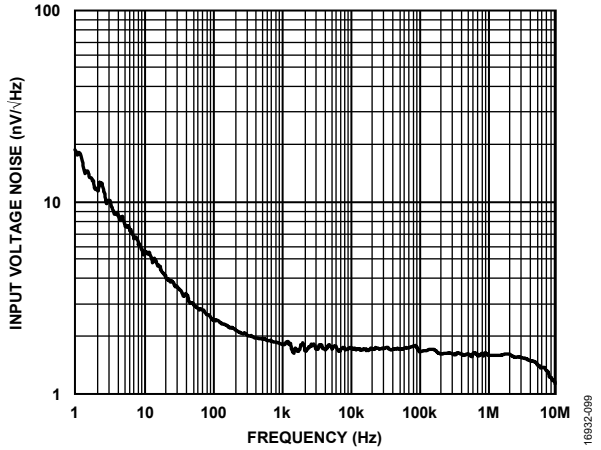


Figure 33. Voltage Noise Spectral Density, Referred to Input

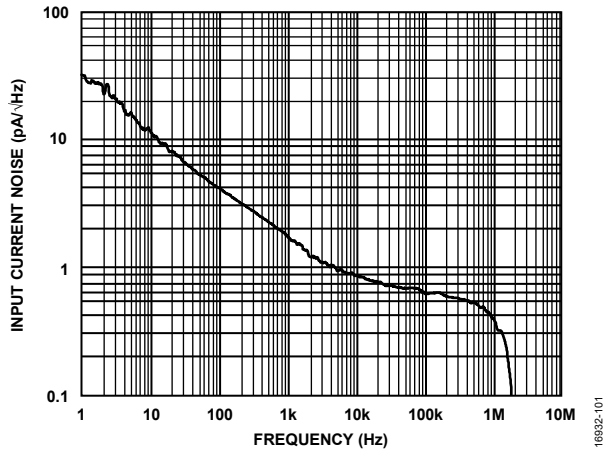


Figure 34. Input Current Noise Spectral Density

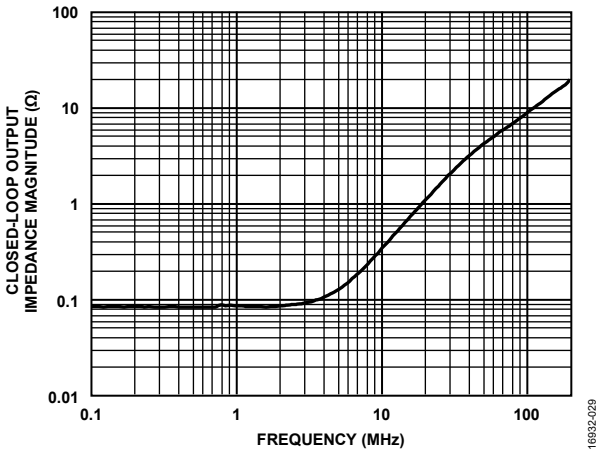


Figure 37. Closed-Loop Output Impedance Magnitude vs. Frequency, G = 1

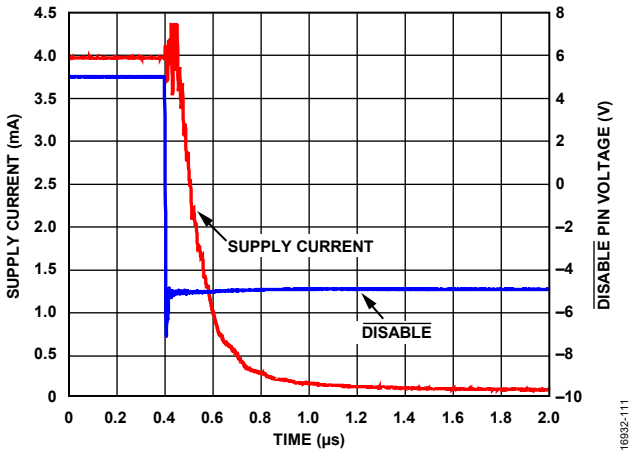


Figure 35. $\overline{DISABLE}$ Pin Turn-Off Time

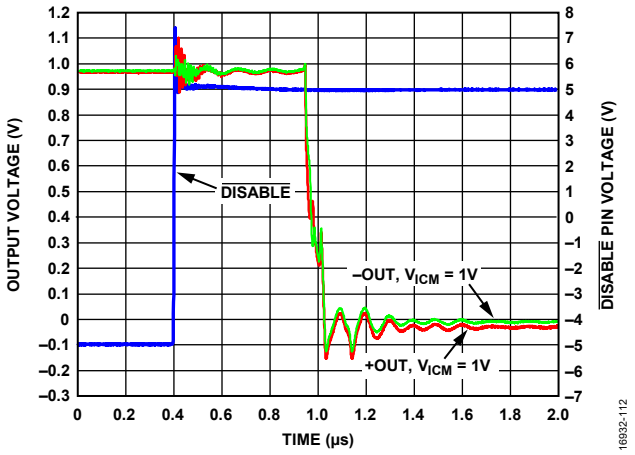


Figure 38. $\overline{DISABLE}$ Pin Turn-On Time

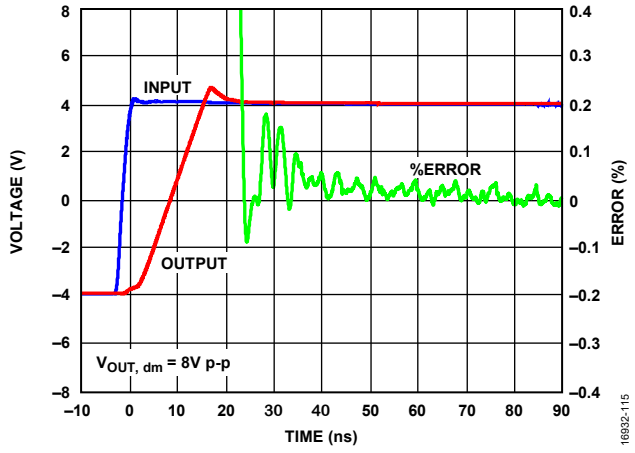


Figure 36. 0.1% Settling Time

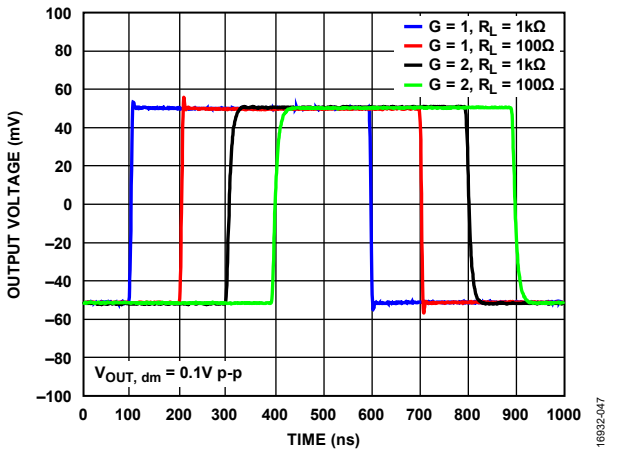


Figure 39. Small Signal Transient Response for Various Gains and Loads

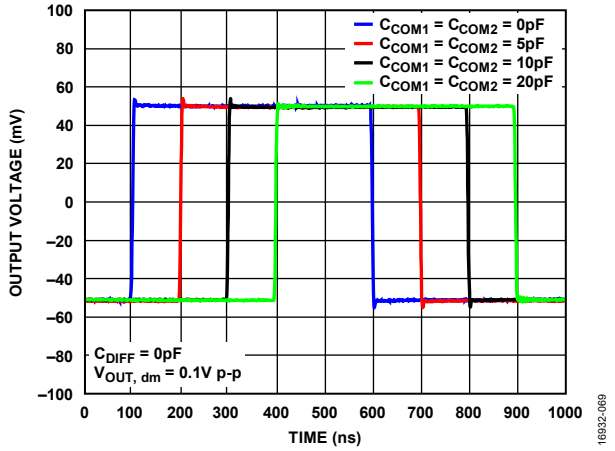


Figure 40. Small Signal Transient Response for Various Capacitive Loads, V_S = 10 V

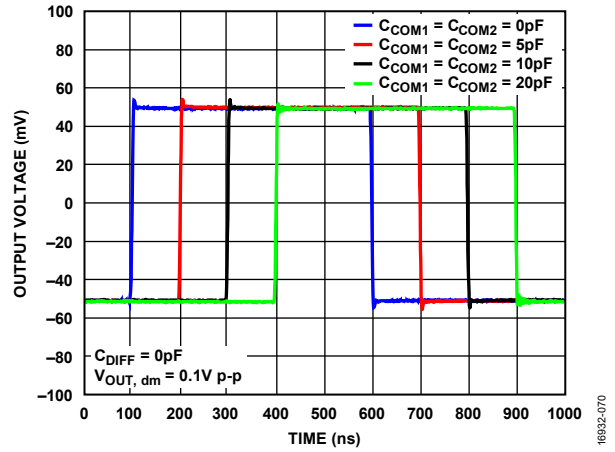


Figure 41. Small Signal Transient Response for Various Capacitive Loads, V_S = 5 V

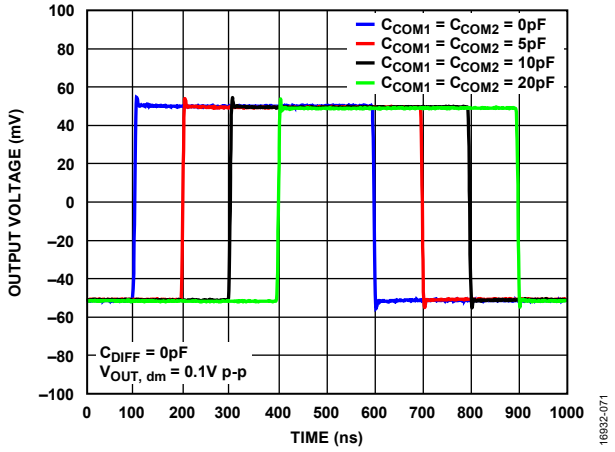


Figure 42. Small Signal Transient Response for Various Capacitive Loads, V_S = 3 V

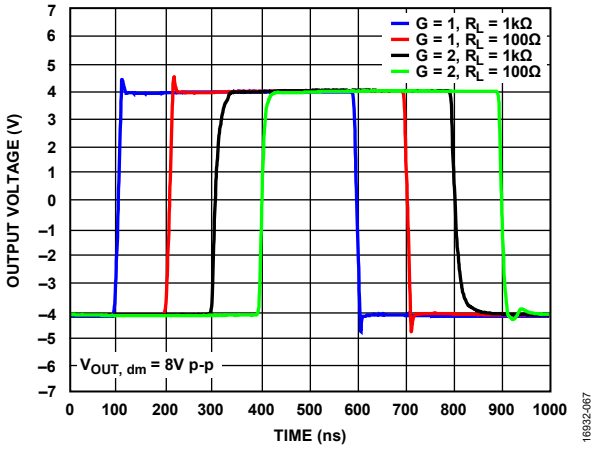


Figure 43. Large Signal Transient Response for Various Gains and Loads

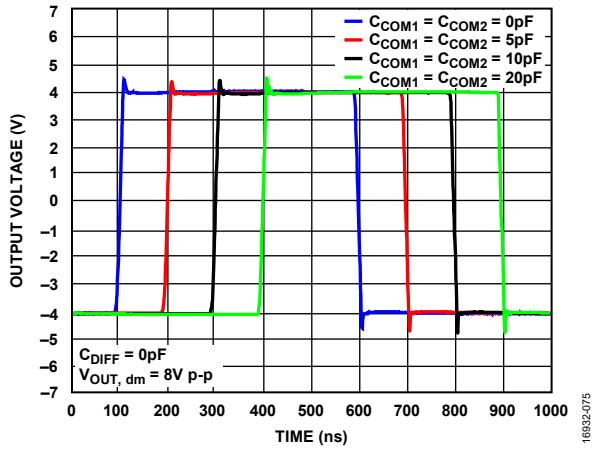


Figure 44. Large Signal Transient Response for Various Capacitive Loads, V_S = 10 V

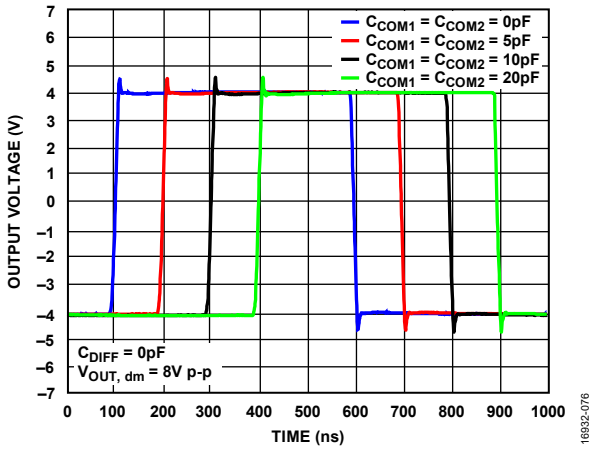


Figure 45. Large Signal Transient Response for Various Capacitive Loads, V_S = 5 V

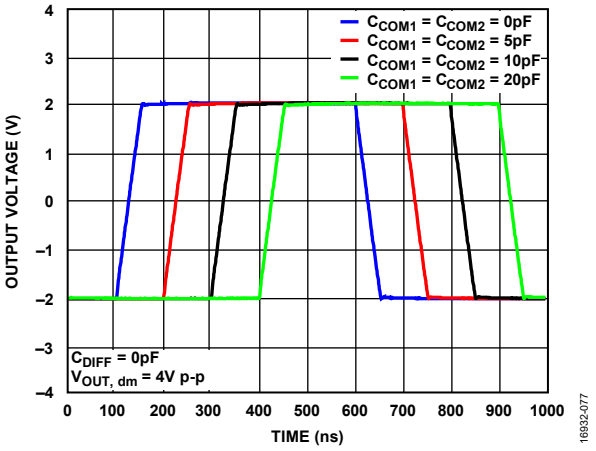


Figure 46. Large Signal Transient Response for Various Capacitive Loads, V_S = 3 V

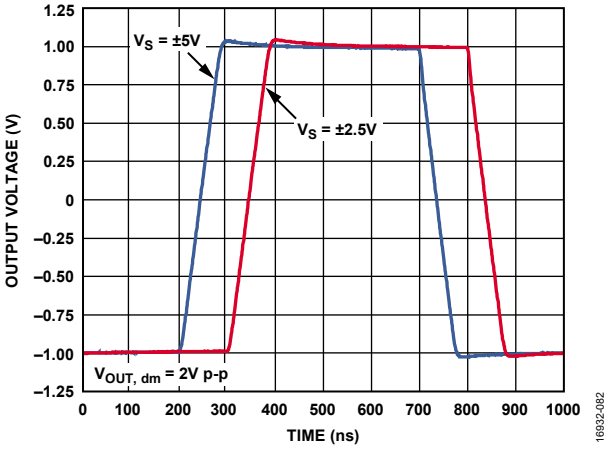


Figure 48. V_{OCM} Large Signal Transient Response

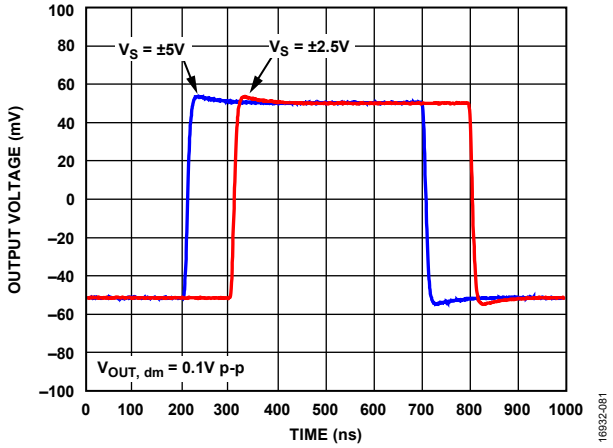


Figure 47. V_{OCM} Small Signal Transient Response

LOW POWER MODE

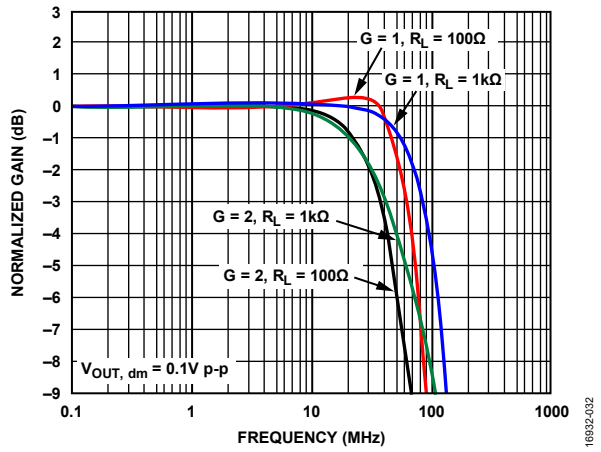


Figure 49. Small Signal Frequency Response for Various Gains and Loads

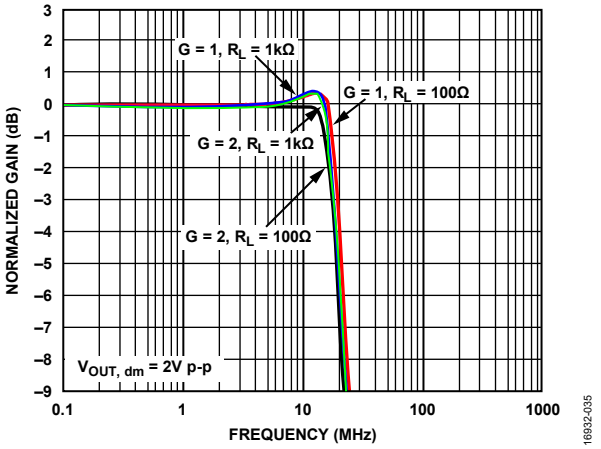


Figure 52. Large Signal Frequency Response for Various Gains and Loads

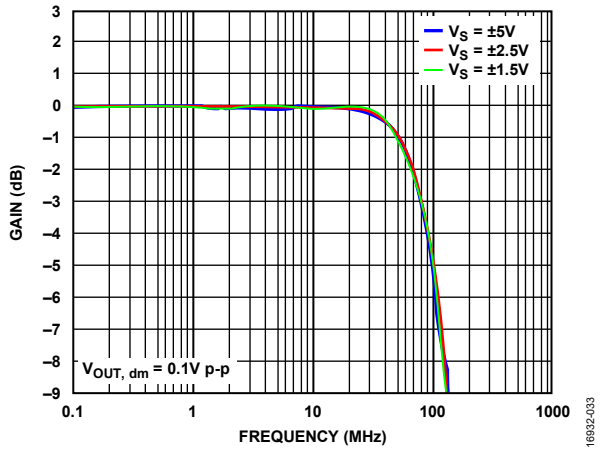


Figure 50. Small Signal Frequency Response for Various Supplies

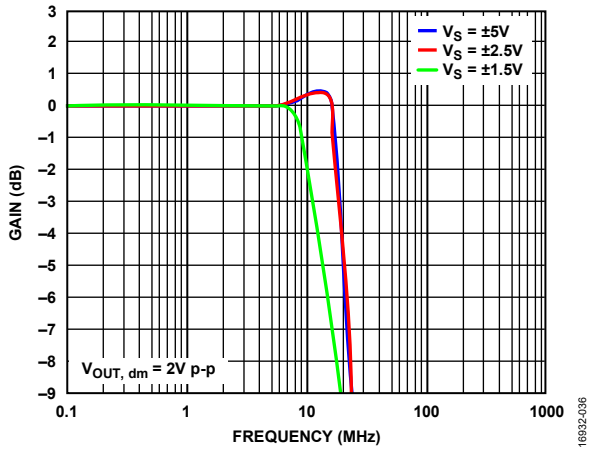


Figure 53. Large Signal Frequency Response for Various Supplies

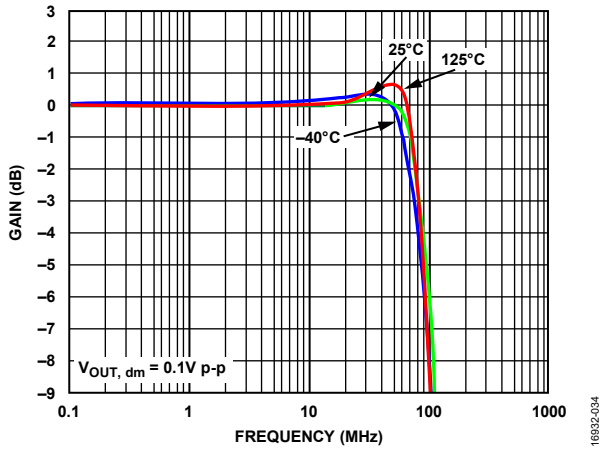


Figure 51. Small Signal Frequency Response for Various Temperatures

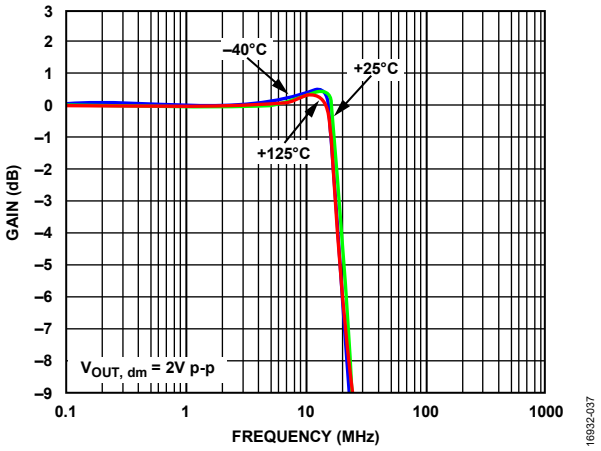


Figure 54. Large Signal Frequency Response for Various Temperatures

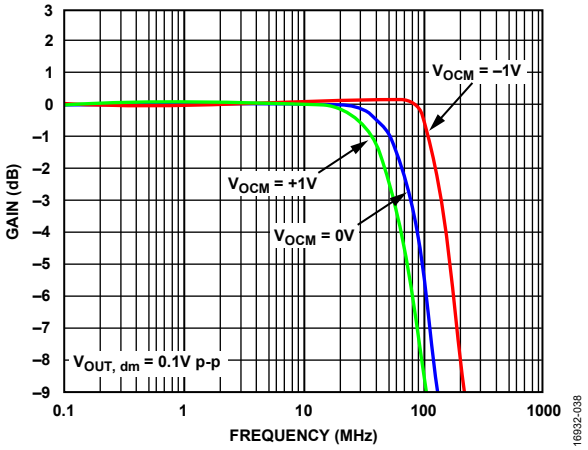


Figure 55. Small Signal Frequency Response at Various V_{OCM} Levels

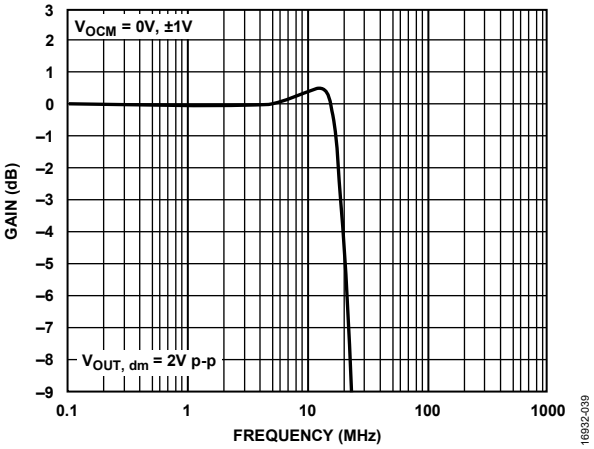


Figure 56. Large Signal Frequency Response at Various V_{OCM} Levels

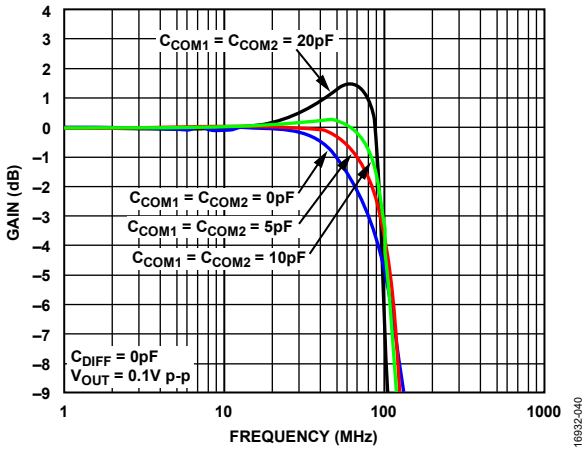


Figure 57. Small Signal Frequency Response for Various Capacitive Loads

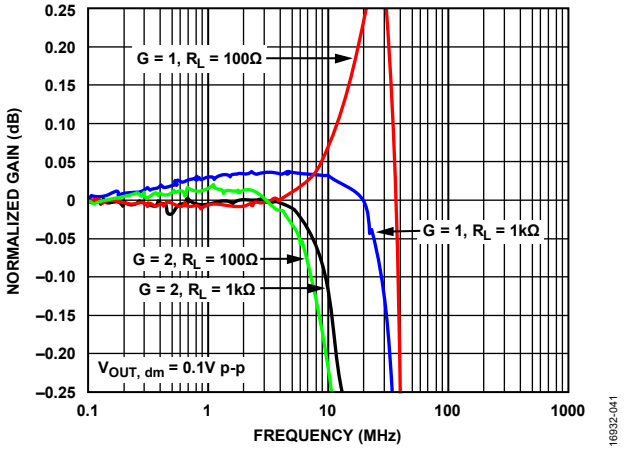


Figure 58. 0.1 dB Flatness Small Signal Frequency Response for Various Gains and Loads

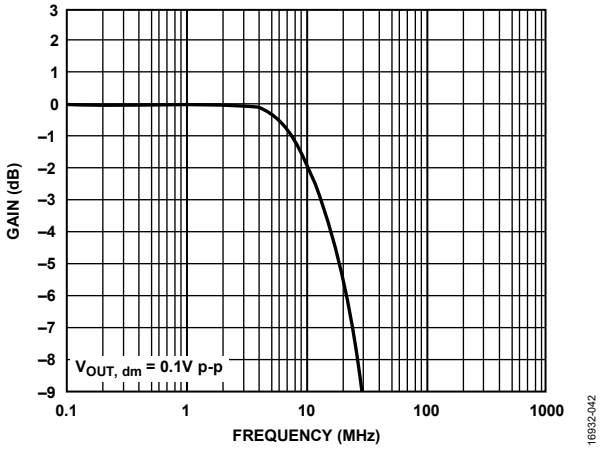


Figure 59. V_{OCM} Small Signal Frequency

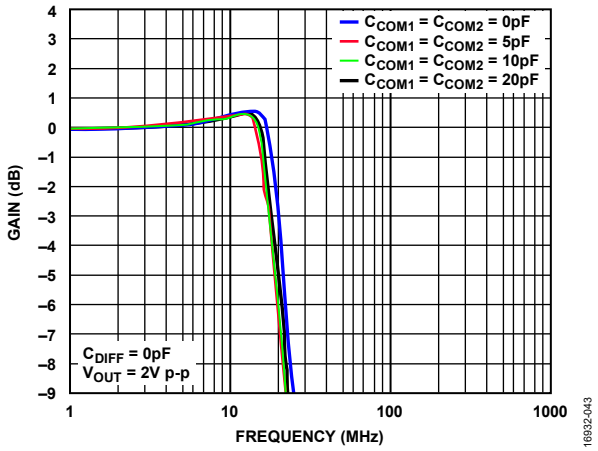


Figure 60. Large Signal Frequency Response for Various Capacitive Loads

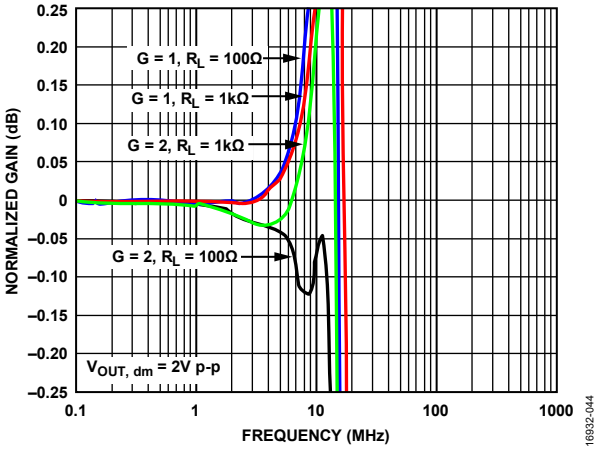


Figure 61. 0.1 dB Flatness Large Signal Frequency Response for Various Gains and Loads

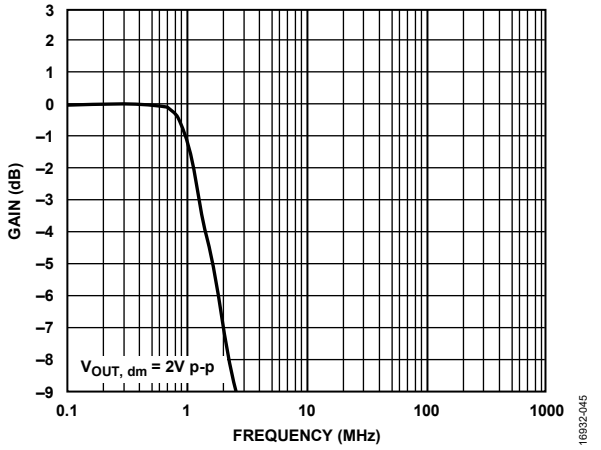


Figure 62. V_{OCM} Large Signal Frequency

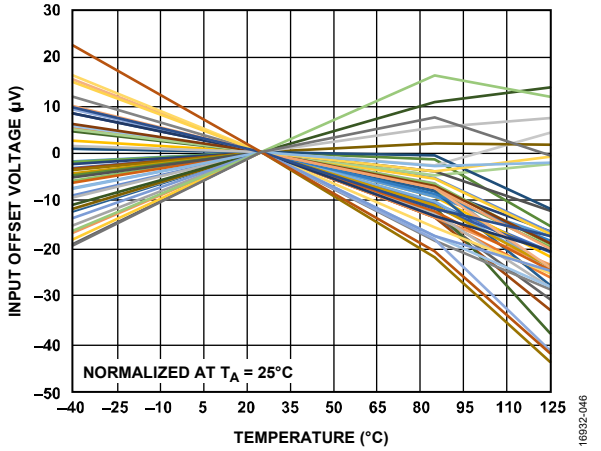


Figure 63. Input Offset Voltage vs. Temperature for 50 Devices

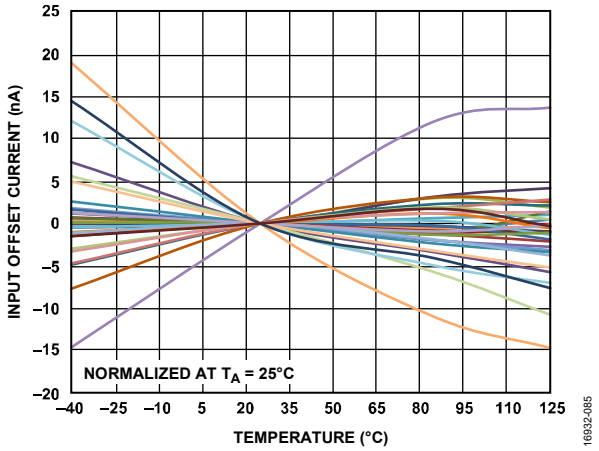


Figure 64. Input Offset Current vs. Temperature for 30 Devices

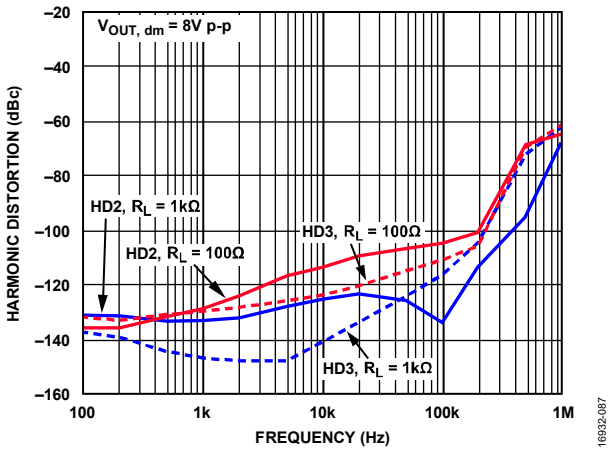


Figure 65. Harmonic Distortion vs. Frequency for Various Loads

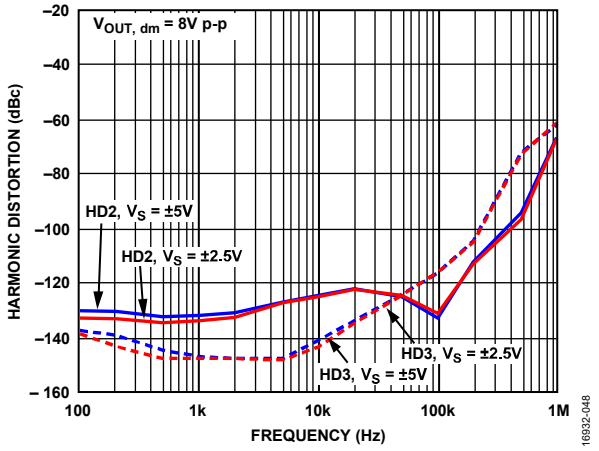


Figure 66. Harmonic Distortion vs. Frequency for Various Supplies

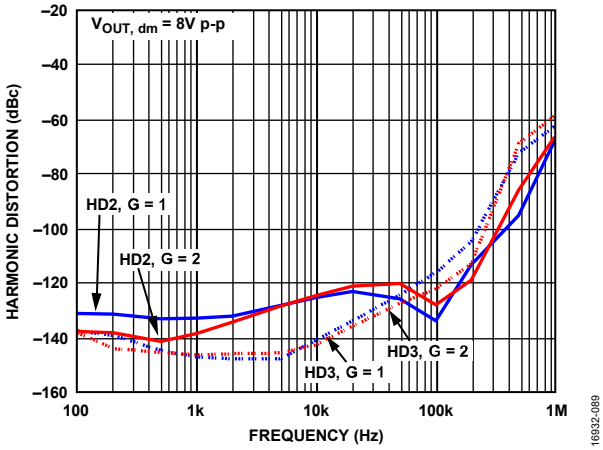


Figure 67. Harmonic Distortion vs. Frequency for Various Gains

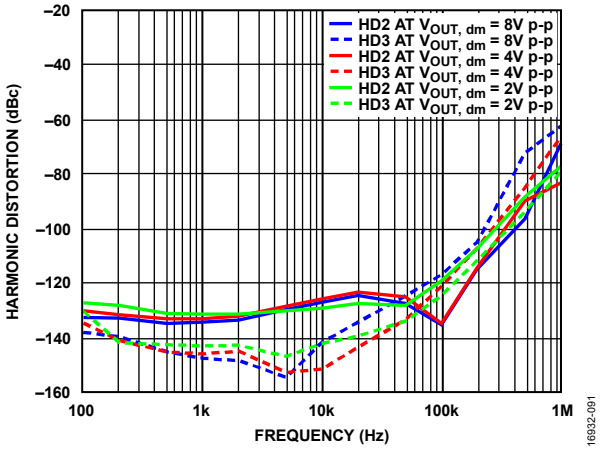


Figure 70. Harmonic Distortion vs. Frequency for Various $V_{OUT, dm}$

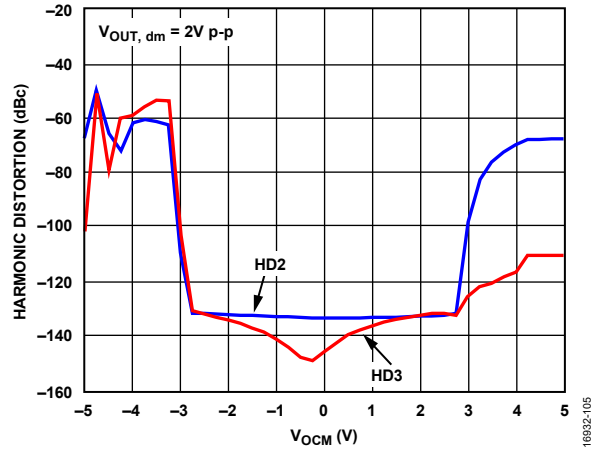


Figure 68. Harmonic Distortion vs. V_{OCM}, f = 1 kHz, ±5 V Supplies

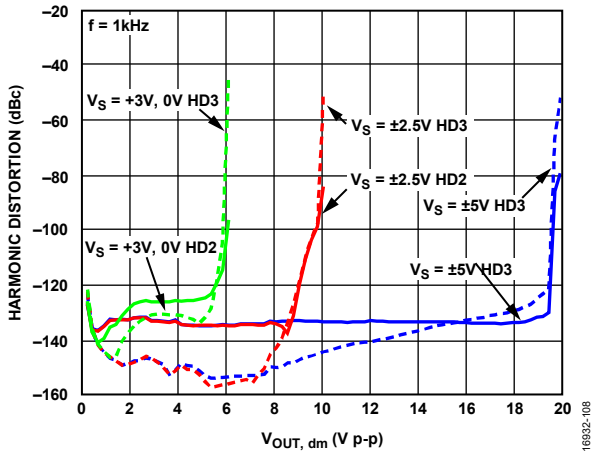


Figure 71. Harmonic Distortion vs. $V_{OUT, dm}$ for Various Supplies, f = 1 kHz

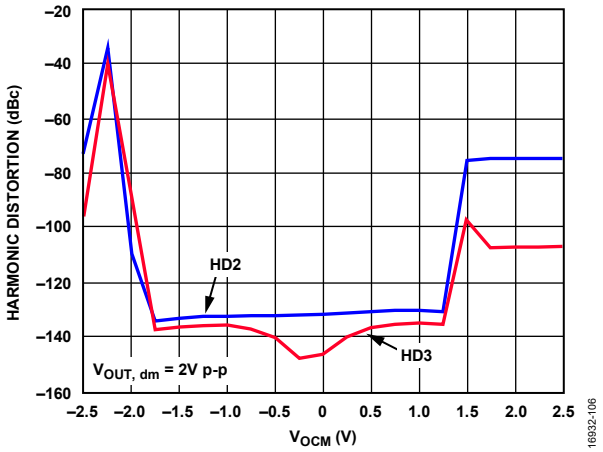


Figure 69. Harmonic Distortion vs. V_{OCM}, f = 1 kHz, ±2.5 V Supplies

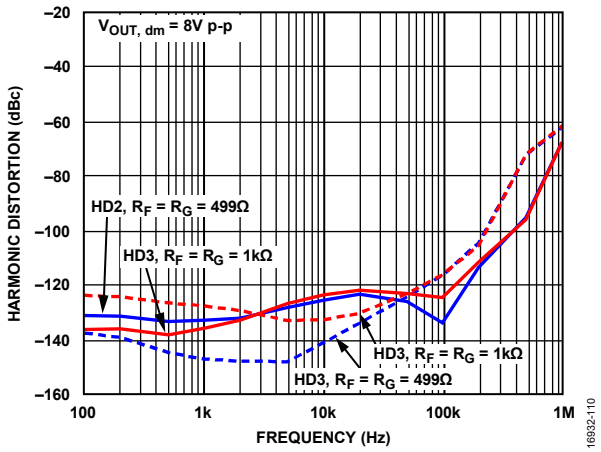


Figure 72. Harmonic Distortion vs. Frequency for Various R_F and R_G Values

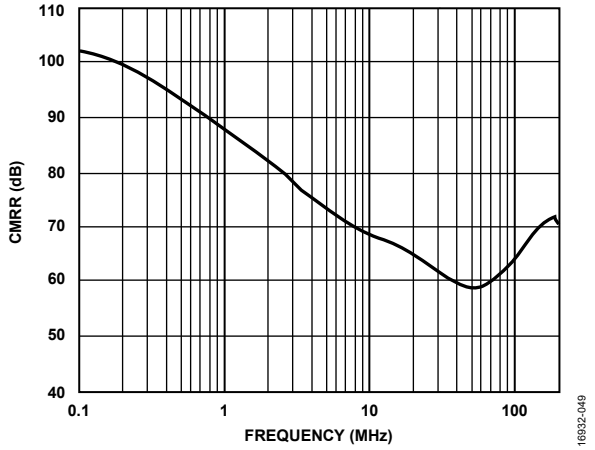


Figure 73. CMRR vs. Frequency

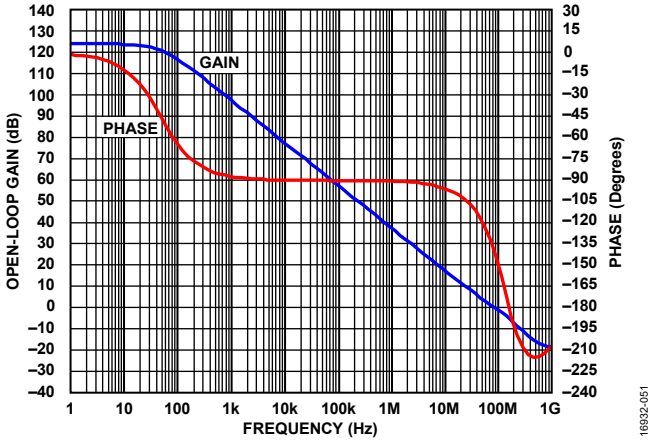


Figure 76. Open-Loop Gain and Phase vs. Frequency

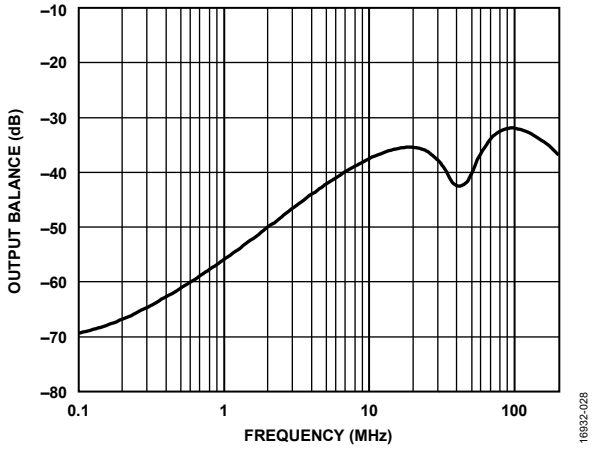


Figure 74. Output Balance vs. Frequency

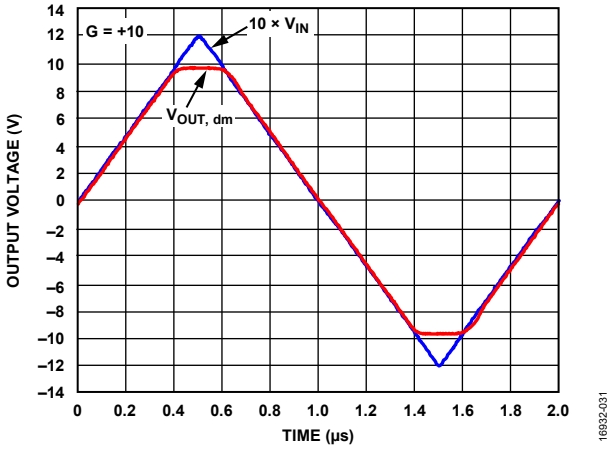


Figure 77. Output Overdrive Recovery, G = 2

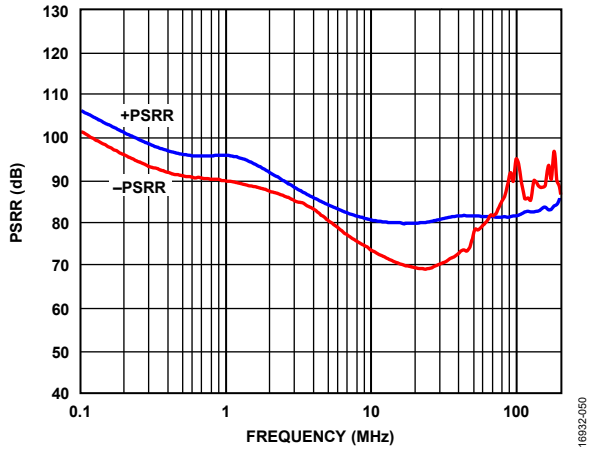


Figure 75. PSRR vs. Frequency

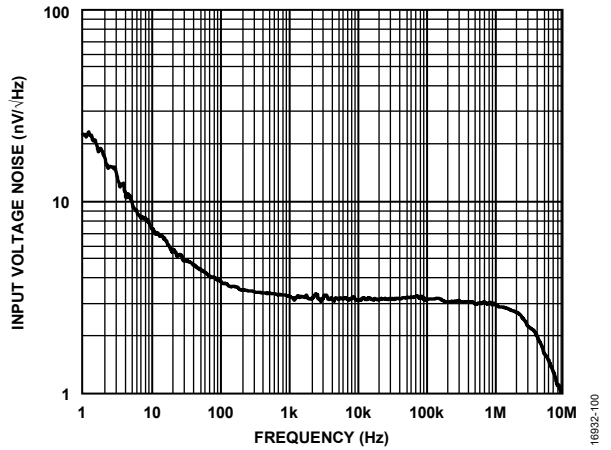


Figure 78. Voltage Noise Spectral Density, Referred to Input

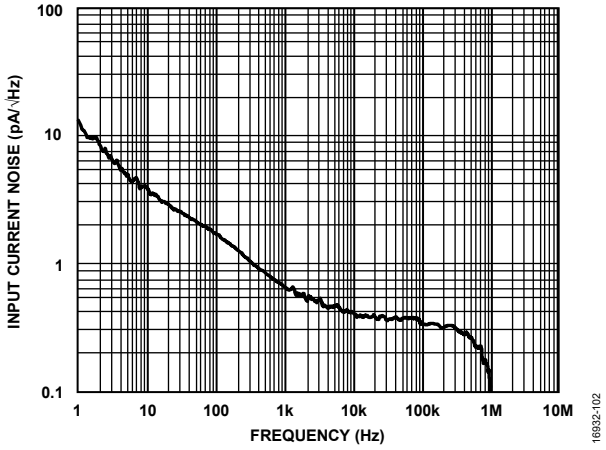


Figure 79. Current Noise Spectral Density

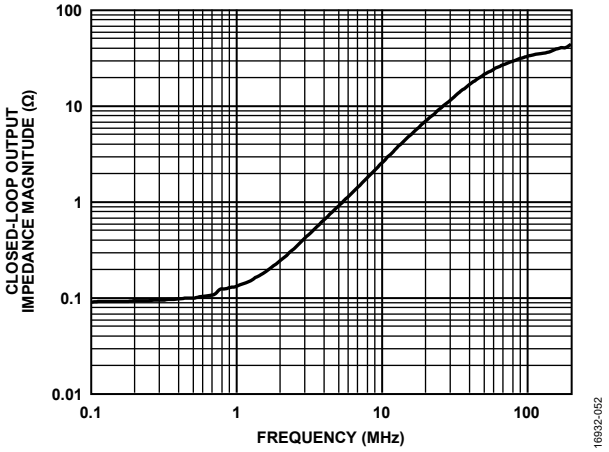


Figure 82. Closed-Loop Output Impedance Magnitude vs. Frequency, G = 1

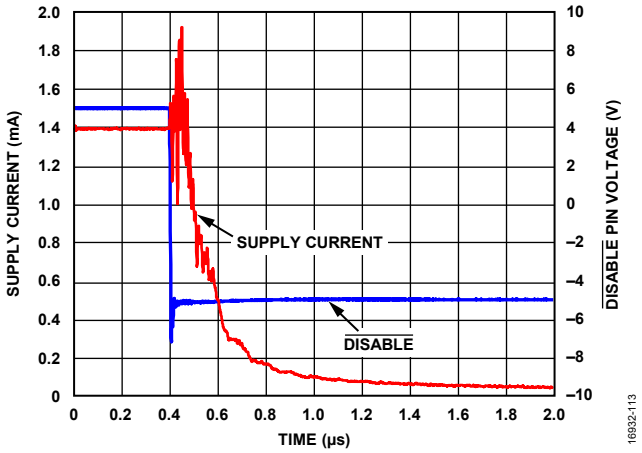


Figure 80. $\overline{DISABLE}$ Pin Turn-Off Time

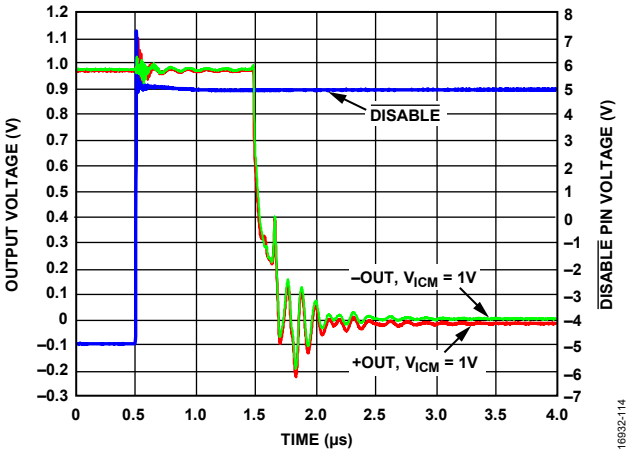


Figure 83. $\overline{DISABLE}$ Pin Turn-On Time

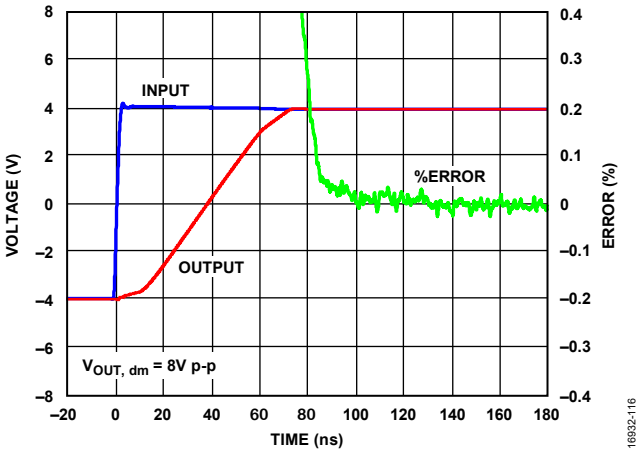


Figure 81. 0.1% Settling Time

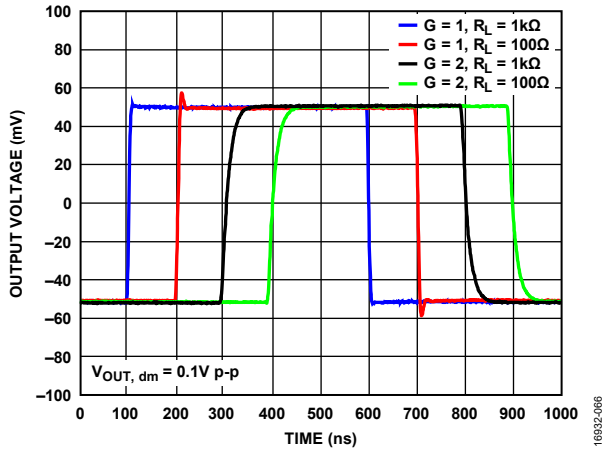


Figure 84. Small Signal Transient Response for Various Gains and Loads

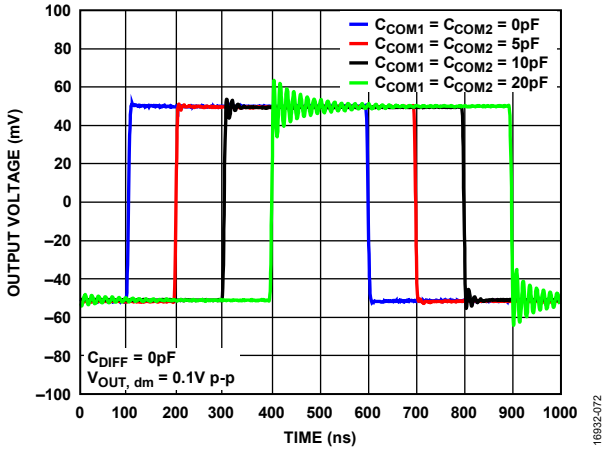


Figure 85. Small Signal Transient Response for Various Capacitive Loads, V_S = 10 V

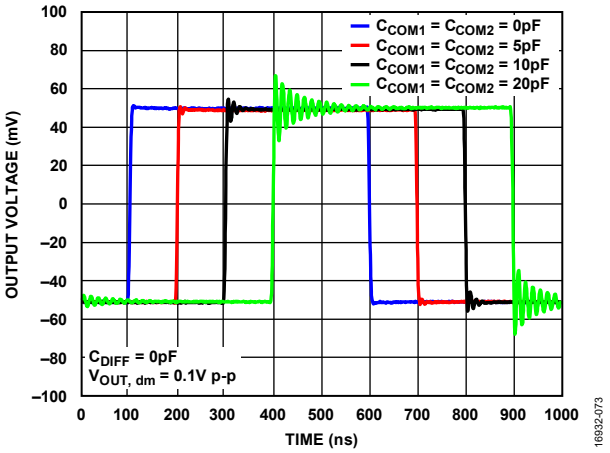


Figure 86. Small Signal Transient Response for Various Capacitive Loads, V_S = 5 V

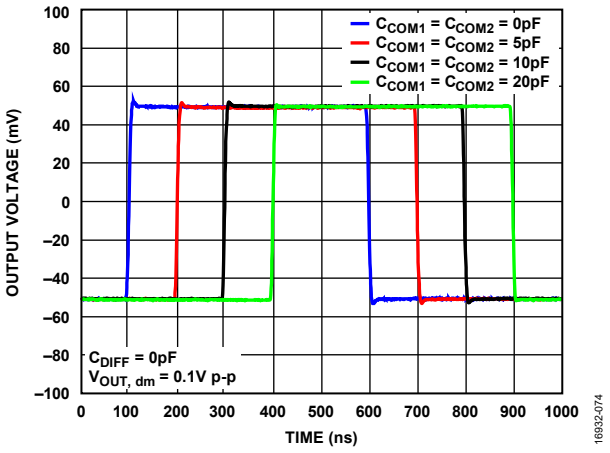


Figure 87. Small Signal Transient Response for Various Capacitive Loads, V_S = 3 V

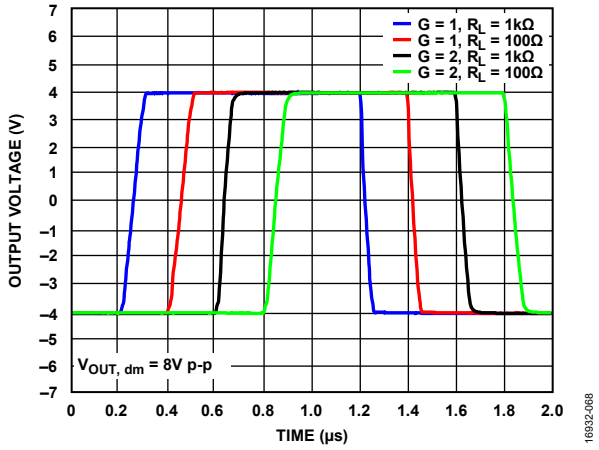


Figure 88. Large Signal Transient Response for Various Gains and Loads

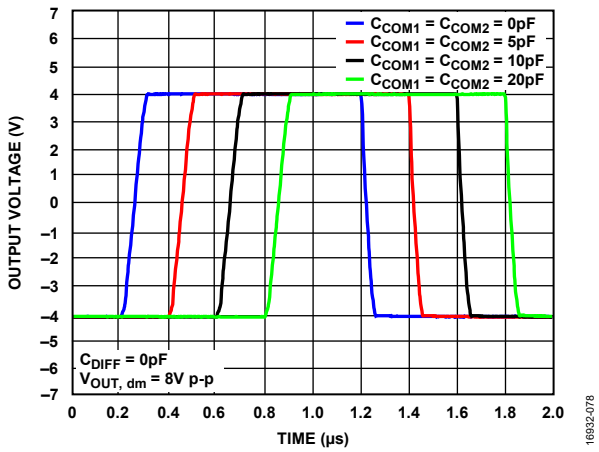


Figure 89. Large Signal Transient Response for Various Capacitive Loads, V_S = 10 V

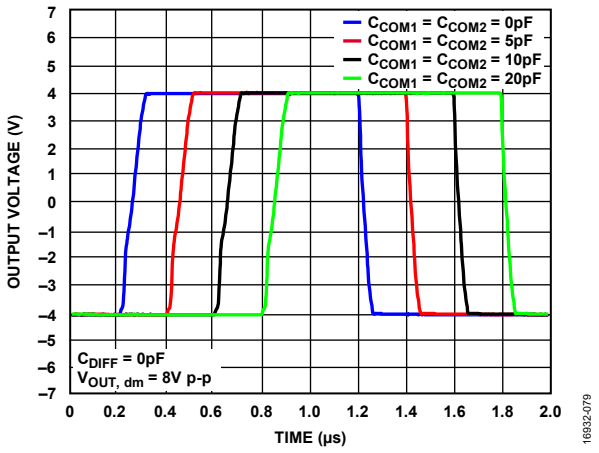


Figure 90. Large Signal Transient Response for Various Capacitive Loads, V_S = 5 V

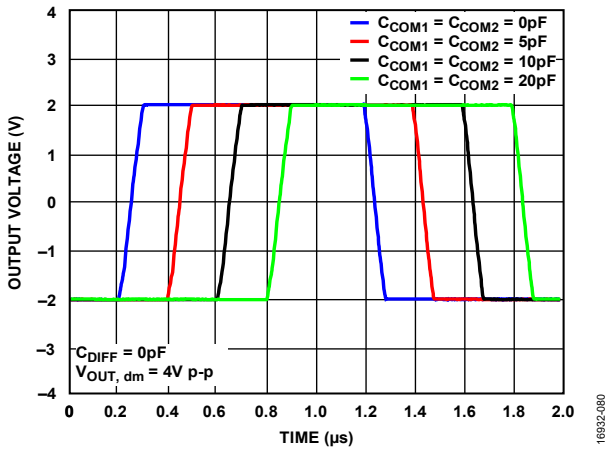


Figure 91. Large Signal Transient Response for Various Capacitive Loads, V_S = 3 V

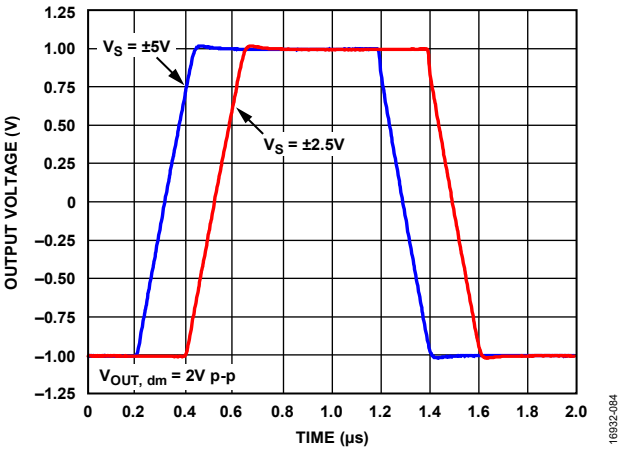


Figure 93. V_{OCM} Large Signal Transient Response

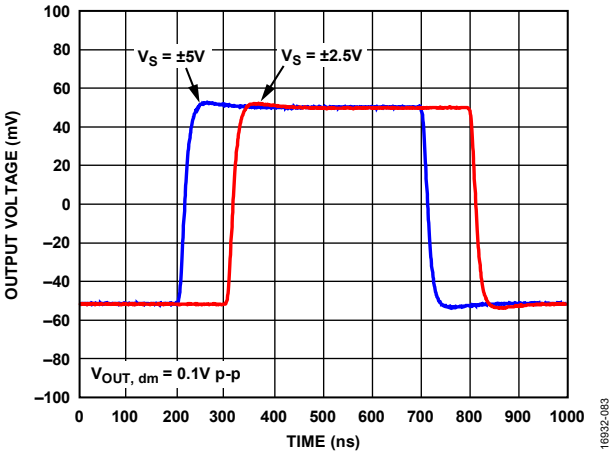


Figure 92. V_{OCM} Small Signal Transient Response

TEST CIRCUITS

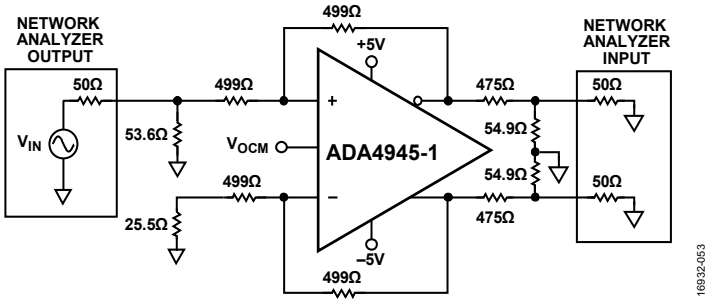


Figure 94. Equivalent Basic Test Circuit

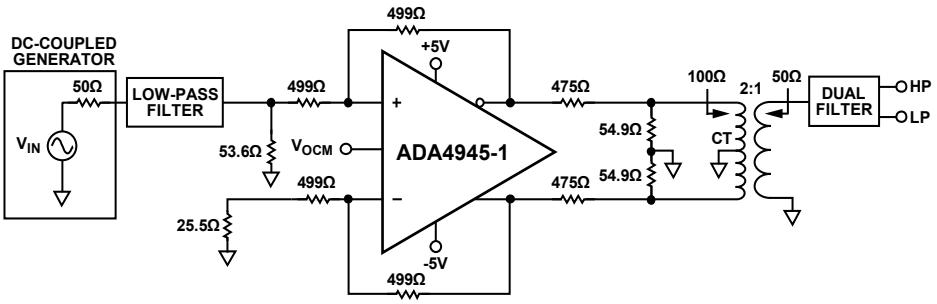


Figure 95. Test Circuit for Distortion Measurements

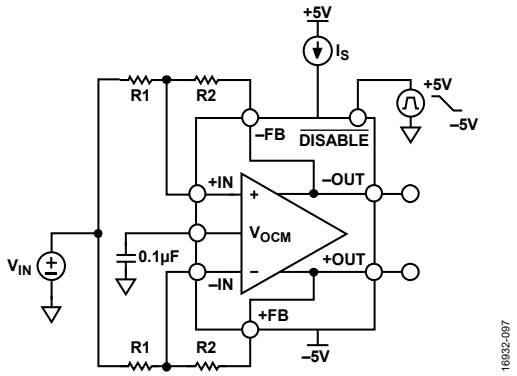


Figure 96. Test Circuit for $\overline{DISABLE}$ Pin Turn Off Time Measurement

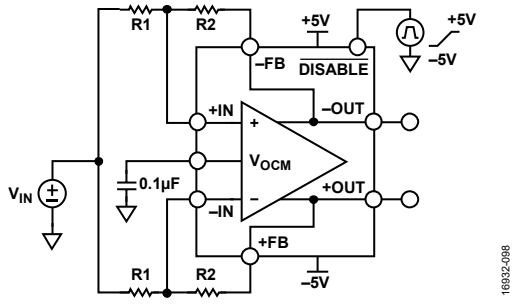


Figure 97. Test Circuit for $\overline{DISABLE}$ Pin Turn On Time Measurement

TERMINOLOGY

Differential Voltage

Differential voltage is the difference between two node voltages. For example, the differential output voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Similarly, the differential input voltage is defined as

$$V_{IN,\,dm} = (+D_{IN} - (-D_{IN}))$$

Common-Mode Voltage (CMV)

CMV is the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Similarly, the input common-mode voltage is defined as

$$V_{IN,\,cm} = (+D_{IN} + (-D_{IN}))/2$$

Common-Mode Offset Voltage

Common-mode offset voltage is the difference between the voltage applied to the V_{OCM} terminal and the common mode of the output voltage.

$$V_{OS,\,cm} = V_{OUT,\,cm} - V_{OCM}$$

Differential V_{OS}, Differential CMRR, and V_{OCM} CMRR

The differential mode and common-mode voltages each have their own error sources. The differential offset ($V_{OS,\,dm}$) is the voltage error between the +IN and −IN terminals of the amplifier. Differential CMRR reflects the change of $V_{OS,\,dm}$ in response to changes to the common-mode voltage at $+D_{IN}$ and $-D_{IN}$ (see Figure 98).

$$CMRR_{DIFF} = \frac{\Delta V_{IN,\,cm}}{\Delta V_{OS,\,dm}}$$

V_{OCM} CMRR reflects the change of $V_{OS,\,dm}$ in response to changes to the common-mode voltage at the output terminals.

$$CMRR_{V_{OCM}} = \frac{\Delta V_{OCM}}{\Delta V_{OS,\,dm}}$$

Balance

Balance is a measure of how well the differential signals are matched in amplitude. The differential signals are exactly 180° apart in phase. By this definition, the output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

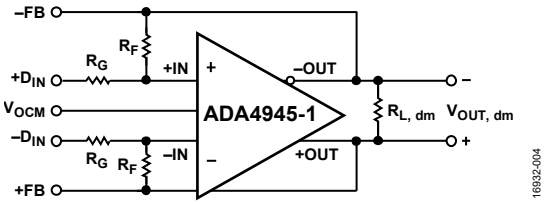


Figure 98. Circuit Definitions

THEORY OF OPERATION

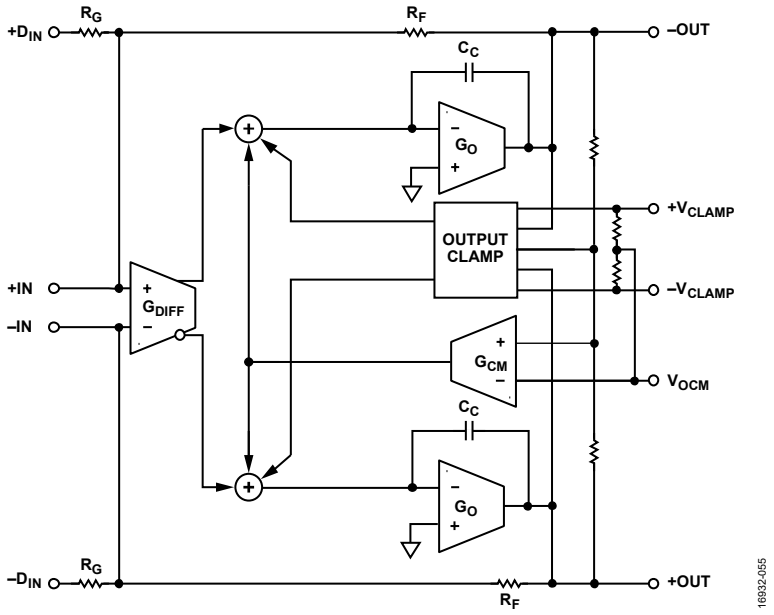


Figure 99. ADA4945-1 Architectural Block Diagram

The ADA4945-1 is a high speed, low power differential amplifier fabricated on Analog Devices advanced dielectrically isolated SiGe bipolar process. The device provides two closely balanced differential outputs in response to either differential or single-ended input signals. An external feedback network that is similar to a voltage feedback operational amplifier sets the differential gain. The output common-mode voltage is independent of the input common-mode voltage and is set by an external voltage at the V_{OCM} terminal. The PNP input stage allows input common-mode voltages between the negative supply and 1.3 V less than the positive supply. A rail-to-rail output stage supplies a wide output voltage range. The $\overline{\text{DISABLE}}$ pin can reduce the supply current (I_S) of the amplifier to 50 µA.

FULLY DIFFERENTIAL AND COMMON-MODE SIGNAL PATHS

Figure 99 shows a simplified diagram of the ADA4945-1 architecture. The differential feedback loop consists of the differential transconductance (G_{DIFF}) working through the G_O output buffers and the R_F/R_G feedback networks. The common-mode feedback loop is set up with a voltage divider across the two differential outputs to create an output voltage midpoint ($V_{OUT(CM)}$) and a common-mode transconductance (G_{CM}).

The differential feedback loop forces the voltages at +IN and −IN to equal each other. This voltage equalization sets the following relationships:

$$\frac{+D_{IN}}{R_G} = -\frac{V_{-OUT}}{R_F}$$

$$\frac{-D_{IN}}{R_G} = -\frac{V_{+OUT}}{R_F}$$

Subtracting the previous equations gives the relationship that shows R_F and R_G setting the differential gain.

$$(V_{+OUT} - V_{-OUT}) = (+D_{IN} - (-D_{IN})) \times \frac{R_F}{R_G}$$

The common-mode feedback loop drives the output common-mode voltage that is sampled at the midpoint of the output voltage divider to equal the voltage at V_{OCM}. This voltage equalization results in the following relationships:

$$V_{+OUT} = V_{OCM} + \frac{V_{OUT,dm}}{2}$$

$$V_{-OUT} = V_{OCM} - \frac{V_{OUT,dm}}{2}$$

Note that the summing junction input voltages of the differential amplifier (+IN and −IN in Figure 99) are set by both the output voltages and the input voltages.

$$V_{+IN} = +D_{IN}\left(\frac{R_F}{R_F + R_G}\right) + V_{-OUT}\left(\frac{R_G}{R_F + R_G}\right)$$

$$V_{-IN} = -D_{IN}\left(\frac{R_F}{R_F + R_G}\right) + V_{+OUT}\left(\frac{R_G}{R_F + R_G}\right)$$

OUTPUT VOLTAGE CLAMP

In addition to the differential and common-mode signal paths, the ADA4945-1 implements clamping circuits to protect the input devices of circuits being driven by the ADA4945-1, hereafter assumed to be an ADC, from being overdriven and potentially damaged. These clamping circuits use both differential and common-mode feedback to limit the output voltages to a range defined by the voltage applied to two reference pins, $+V_{CLAMP}$ and $-V_{CLAMP}$. These high impedance pins are typically connected to potentials that define the allowable input range of the ADC, which are the ADC reference voltages ($+V_{REF}$ and $-V_{REF}$) for most ADCs.

As shown in Figure 100, the common-mode clamping circuit senses the output voltage midpoint and applies a common-mode feedback signal to prevent $V_{OUT, cm}$ from exceeding $+V_{CLAMP}$ or going below $-V_{CLAMP}$.

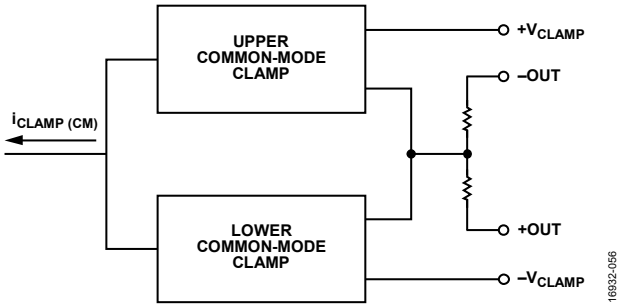


Figure 100. Common-Mode Clamp Block Diagram

The differential clamping circuit, shown in Figure 101, senses each output (+OUT and −OUT) and applies a differential feedback signal to prevent either output from exceeding ($+V_{CLAMP}$ + 0.5 V) or going below ($-V_{CLAMP}$ − 0.5 V). The approximately 500 mV offset voltage is designed to allow the outputs to fully use the input range of the ADC without any clamp engagement, while providing input protection prior to the turn on of the ADC input protection diodes. This feature allows the ADA4945-1 to provide a full-scale signal to the ADC without incurring any clamp induced distortion, thus maximizing signal-to-noise ratio (SNR) and linearity while protecting the ADC inputs.

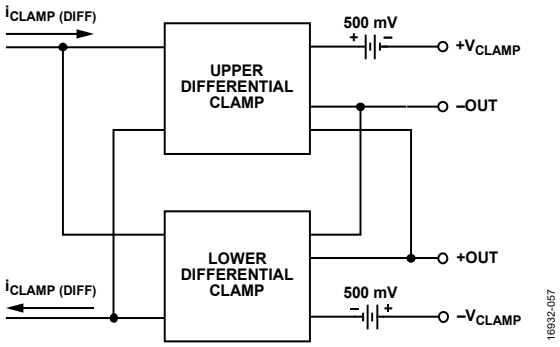


Figure 101. Differential Clamp Block Diagram

By applying a differential feedback signal in response to one or both outputs exceeding the clamp reference voltages, both outputs are limited equally, even if only one output exceeds one of the clamp reference voltages. This feature allows the ADA4945-1 to maintain a constant output common-mode voltage even while clamping the differential outputs, which enables a faster system recovery from a clamped condition.

In systems where output clamping is not desired, the upper output clamp can be disabled by connecting $+V_{CLAMP}$ to $+V_S$, and the lower output clamp can be disabled by connecting $-V_{CLAMP}$ to $-V_S$. If one clamp is disabled (for example, $-V_S = -V_{CLAMP} = 0$ V), the other can be remain active, and the output is limited when either or both outputs reaches the active clamp reference.

An additional feature of the ADA4945-1 is the use of a resistor divider between the $+V_{CLAMP}$ and $-V_{CLAMP}$ pins, as shown in Figure 99, to set the default potential on the V_{OCM} pin when the pin is not externally driven. Because the $+V_{CLAMP}$ and $-V_{CLAMP}$ pins are typically set to the maximum and minimum desired input voltage of the ADC (for example, $+V_{REF}$ and $-V_{REF}$), respectively, this resistor divider sets the output common-mode voltage of the ADA4945-1 at the midpoint of the ADC input range by default. By contrast, most fully-differential amplifiers use a resistor divider between the amplifier supply voltages to set the default output common-mode voltage, which may not be optimal for maximizing ADC input range usage.

POWER MODES

The ADA4945-1 implements two fully characterized active power modes (full power, low power) and a disable mode to optimize system power and performance trade-offs. The transition time from disable mode to either of the active power modes is fast (<2 µs), allowing additional power savings by dynamically placing the ADA4945-1 in disable mode when the output voltage is not needed (for example, between ADC samples in low data rate systems).

APPLICATIONS INFORMATION

ANALYZING AN APPLICATION CIRCUIT

The ADA4945-1 uses open-loop gain and negative feedback to force the differential and common-mode output voltages to minimize the differential and common-mode error voltages. The differential error voltage is the voltage between the differential inputs labeled +IN and −IN (see Figure 98). For most purposes, this voltage is 0 V. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} is also 0 V. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

Determine the differential mode gain of the circuit in Figure 98 by using the following equation:

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This calculation assumes that the input resistors (R_G) and feedback resistors (R_F) on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4945-1 can be estimated by using the noise model in Figure 102. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The noise currents are assumed equal and produce a voltage across the parallel combination of the gain and feedback resistances. v_{nCM} is the noise voltage density at the V_{OCM} pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 13 summarizes the input noise sources, the multiplication factors, and the output referred noise density terms. For more noise calculation information, go to the Analog Devices Differential Amplifier Calculator (DiffAmpCalc™), click ADIDiffAmpCalculator.zip, and follow the on-screen prompts.

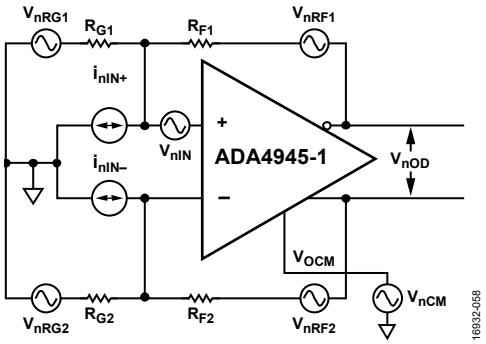


Figure 102. ADA4945-1 Noise Model

As with conventional op amps, the output noise voltage densities can be estimated by multiplying the input referred terms at +IN and −IN by the appropriate output factor, where:

$$G_N = \frac{2}{(\beta_1 + \beta_2)}$$ is the circuit noise gain.

$$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}} \text{ and } \beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

Table 13. Output Noise Voltage Density Calculations

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Output-Referred Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N (v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{G2} \| \| R_{F2})$	G_N	$v_{nO2} = G_N [i_{nIN-} \times (R_{G2} \| \| R_{F2})]$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{G1} \| \| R_{F1})$	G_N	$v_{nO3} = G_N [i_{nIN+} \times (R_{G1} \| \| R_{F1})]$
V_{OCM} Input	v_{nCM}	v_{nCM}	$G_N (\beta_1 - \beta_2)$	$v_{nO4} = G_N (\beta_1 - \beta_2)(v_{nCM})$
Gain Resistor, R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	$G_N (1 - \beta_2)$	$v_{nO5} = G_N (1 - \beta_2)(4kTR_{G1})^{1/2}$
Gain Resistor, R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	$G_N (1 - \beta_1)$	$v_{nO6} = G_N (1 - \beta_1)(4kTR_{G2})^{1/2}$
Feedback Resistor, R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor, R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

Even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from V_{OCM}, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, similar to a four resistors difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential mode, output offset voltage. When G = 1, with a ground referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst case input CMRR of about 40 dB, a worst case differential mode output offset of 25 mV due to the 2.5 V level shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance depends on whether the signal source is single-ended or differential. For a balanced differential input signal, as shown in Figure 103, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is $R_{IN, dm} = 2 \times R_G$.

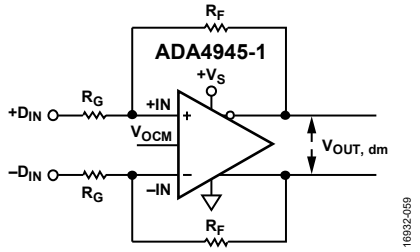


Figure 103. ADA4945-1 Configured for Balanced (Differential) Inputs

For an unbalanced single-ended input signal, as shown in Figure 104, the input impedance is

$$R_{IN,SE} = R_{G1}\,\frac{\beta 1+\beta 2}{\beta 1(\beta 2+1)}$$

where:

$$\beta 1 = \frac{R_{G1}}{R_{G1}+R_{F1}}$$

$$\beta 2 = \frac{R_{G2}}{R_{G2}+R_{F2}}$$

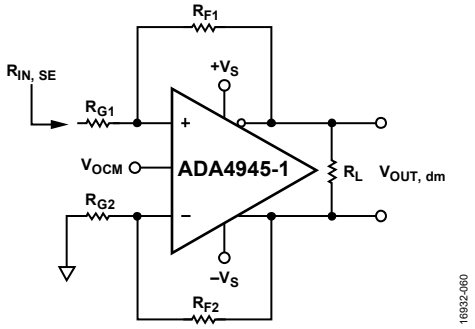


Figure 104. ADA4945-1 with Unbalanced (Single-Ended) Input

For a balanced system where $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$, the equations simplify to

$$\beta 1 = \beta 2 = \frac{R_G}{R_G + R_F} \text{ and } R_{IN,SE} = \left(\frac{R_G}{1-\dfrac{R_F}{2(R_G+R_F)}}\right)$$

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the R_{G1} input resistor.

Terminating a Single-Ended Input

This section describes how to properly terminate a single-ended input to the ADA4945-1. Assume a system gain of 1 where R_{F1} = R_{F2} = R_{G1} = R_{G2} = 499 Ω, an input source with an open-circuit output voltage of 2 V p-p, and a source resistance of 50 Ω. Figure 105 shows the circuit.

1. Calculate the input impedance.

   $\beta 1 = \beta 2$ = 499/998 = 0.5 and R_{IN} = 665.33 Ω

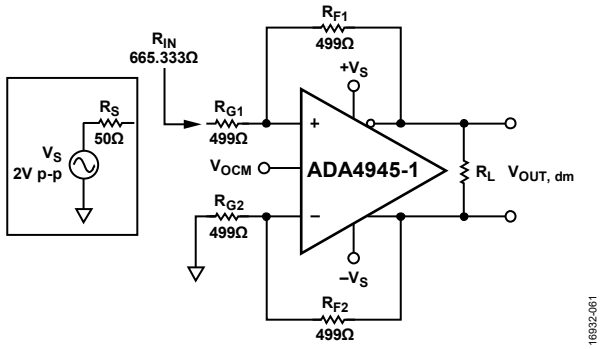


Figure 105. Single-Ended Input Impedance R_{IN}

2. Add a termination resistor (R_T) to match the 50 Ω source resistance. Because $R_T||665.33\ \Omega = 50\ \Omega$, R_T = 54.06 Ω.

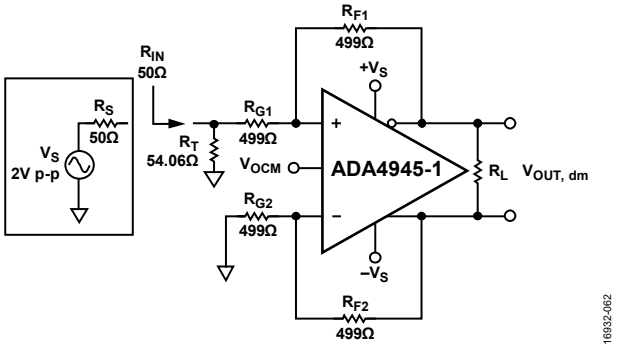


Figure 106. Adding Termination Resistor, R_T

3. Replace the source termination resistor combination with the Thevenin equivalent. The Thevenin equivalent of the source resistance, R_S, and the termination resistance, R_T, is $R_{TH} = R_S||R_T$ = 25.976 Ω. The Thevenin equivalent of the source voltage is

$$V_{TH} = V_S \frac{R_T}{R_S + R_T} = 1.039\ \text{V p-p}$$

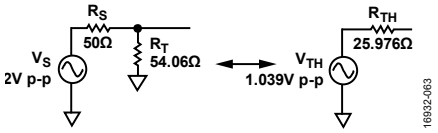


Figure 107. Thevenin Equivalent Circuit

4. Set R_{F1} = R_{F2} = R_F to maintain a balanced system. Compensate the imbalance caused by R_{TH}. There are two methods available to compensate, as follows:

   - Add R_{TH} to R_{G2} to maintain balanced gain resistances and increase R_{F1} and R_{F2} to $R_F = \frac{V_S}{V_{TH}}\text{Gain}(R_G + R_{TH})$ to maintain the system gain.
   - Decrease R_{G2} to $R_{G2} = \frac{R_F \times V_{TH}}{V_S \times \text{Gain}}$ to maintain system gain and decrease R_{G1} to ($R_{G2} - R_{TH}$) to maintain balanced gain resistances.

   The first compensation method is used in the Analog Devices DiffAmpCalc™ tool. Using the second compensation method, R_{G2} =259.241 Ω and R_{G1} = 259.241 – 25.976 = 233.265 Ω. The modified circuit is shown in Figure 108.

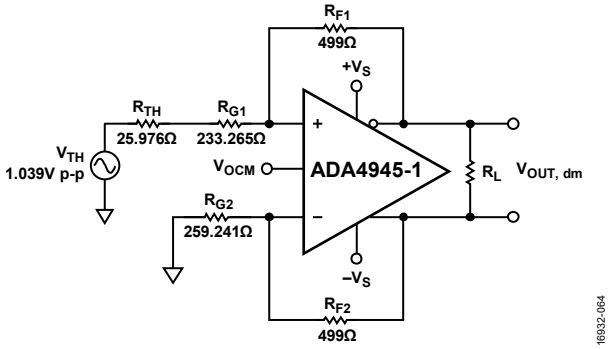


Figure 108. Thevenin Equivalent with Matched Gain Resistors

Figure 108 shows an easily manageable circuit with matched feedback loops that can be easily evaluated.

5. The modified gain resistor, R_{G1}, changes the input impedance. Repeat Step 1 through Step 4 several times using the modified value of R_{G1} from the previous iteration until the value of R_T does not change from the previous iteration. After three additional iterations, the change in R_{G1} is less than 0.1%. The final circuit is shown in Figure 109 with the closest 1% resistor values.

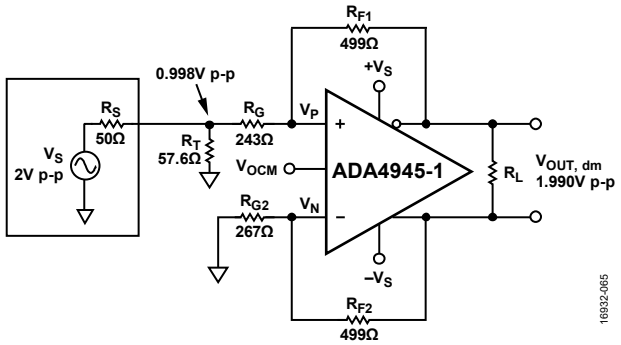


Figure 109. Terminated Single-Ended-to-Differential System with G = 1

INPUT COMMON-MODE VOLTAGE RANGE

The input common-mode range at the summing nodes of the ADA4945-1 is specified as $-V_S$ to $+V_S - 1.3$ V. By extending the input common-mode range down to $-V_S$, the ADA4945-1 is especially well suited to dc-coupled, single-ended-to-differential, and single-supply applications, such as ADC driving.

INPUT AND OUTPUT CAPACITIVE AC COUPLING

Although the ADA4945-1 is best suited to dc-coupled applications, it is possible to use the device in ac-coupled circuits. Input ac coupling capacitors can be inserted between the source and R_G. This ac coupling blocks the flow of the dc common-mode feedback current and causes the ADA4945-1 dc input common-mode voltage to equal the dc output common-mode voltage. These ac coupling capacitors must be placed in both loops to keep the feedback factors matched. Output ac coupling capacitors can be placed in series between each output and the respective load of each output.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4945-1 is internally biased at a voltage approximately equal to the midway between the output voltage clamps, $((+V_{CLAMP}) + (-V_{CLAMP}))/2$. Relying on this internal bias results in an output common-mode voltage that is within approximately 100 mV of the expected value.

When more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used. The output common-mode offset listed in Table 2, Table 5, and Table 8 assumes that the V_{OCM} input is driven by a low impedance voltage source.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC. However, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 125 kΩ.

DISABLE PIN

The ADA4945-1 features a $\overline{\text{DISABLE}}$ pin that can be used to minimize the quiescent current consumed when the device is not being used. $\overline{\text{DISABLE}}$ is asserted by applying a low logic level to the $\overline{\text{DISABLE}}$ pin. The logic level for the $\overline{\text{DISABLE}}$ pin is referenced to D_{GND}. See Table 3, Table 6, and Table 9 for the threshold limits.

The $\overline{\text{DISABLE}}$ pin features an internal pull-up network that enables the amplifier for normal operation. The ADA4945-1 $\overline{\text{DISABLE}}$ pin can be left floating (that is, no external connection is required) and does not require an external pull-up resistor to ensure normal on operation (see Figure 110). When the ADA4945-1 is disabled, the output is high impedance. Note that the outputs are tied to the inputs through the feedback resistors and to the source using the gain resistors. In addition, there are back to back diodes on the input pins that limit the differential voltage to 1.2 V.

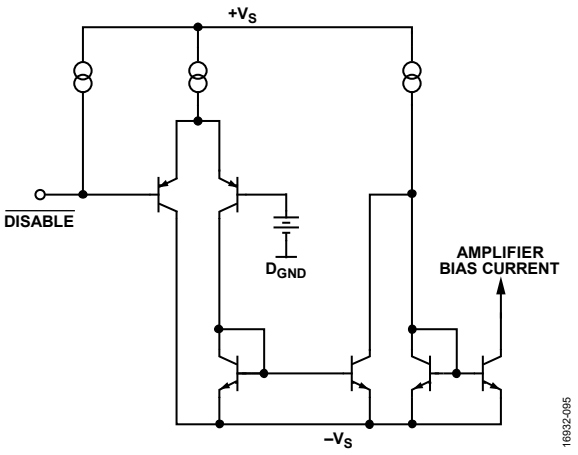


Figure 110. $\overline{\text{DISABLE}}$ Pin Circuit

DRIVING A CAPACITIVE LOAD

A purely capacitive load reacts with the bond wire and pin inductance of the ADA4945-1, resulting in high frequency ringing in the transient response and loss of phase margin. One way to minimize this effect is to place a resistor in series with each output to buffer the load capacitance. The resistor and load capacitance form a first-order, low-pass filter. Therefore, the resistor value must be as small as possible. In some cases, the ADCs require small series resistors to be added on their inputs.

Figure 111 shows the capacitive load vs. the series resistance required to maintain a minimum 45° of phase margin. The test circuit is shown in Figure 112.

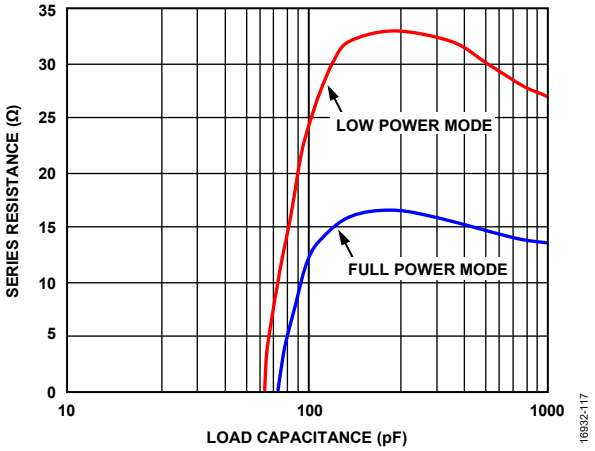


Figure 111. Series Resistance vs. Load Capacitance

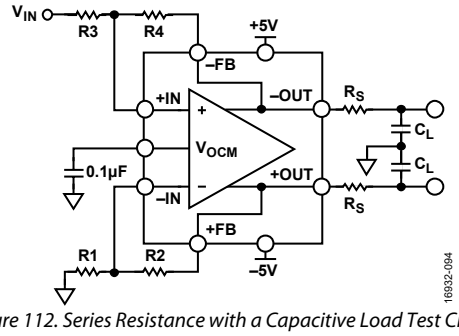


Figure 112. Series Resistance with a Capacitive Load Test Circuit

OUTPUT CLAMPS

The ADA4945-1 implements output voltage clamps to effectively limit the differential and common-mode signal levels, thereby protecting circuitry following the ADA4945-1 from being overdriven. The operation of these clamps is discussed in the Theory of Operation section. Figure 113 shows an example where the output voltage clamp may be used while driving an ADC. In this example, the ADA4945-1 is operating from +7 V and −2 V supplies, and the ADC is using +5 V reference. In such a scenario, the ADC input can potentially be overdriven if no clamping were present. By connecting the clamps to the positive and negative references of the ADC, the differential and common-mode signal levels are limited as shown in Figure 114 and Figure 115. Note that the differential signals are clamped ~500 mV beyond the clamp set voltage to allow full swing to the references. The common-mode signal is clamped right at the clamp set voltages.

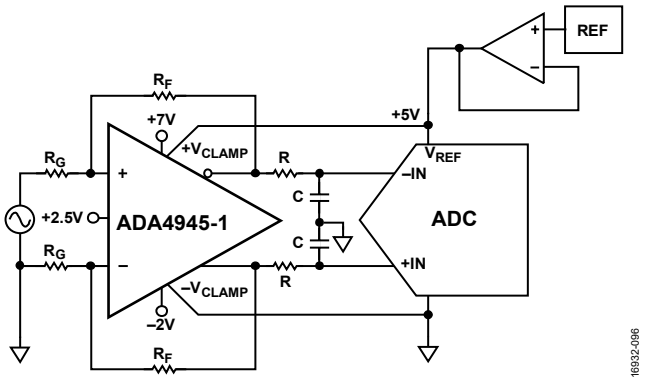


Figure 113. ADA4945-1 Output Voltage Clamp Usage

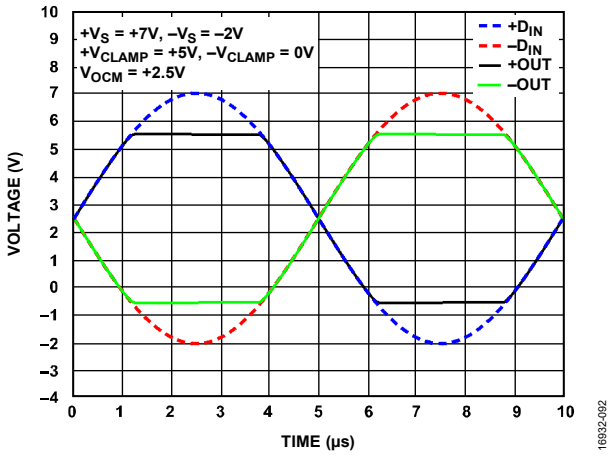


Figure 114. Clamped Differential Signal Levels

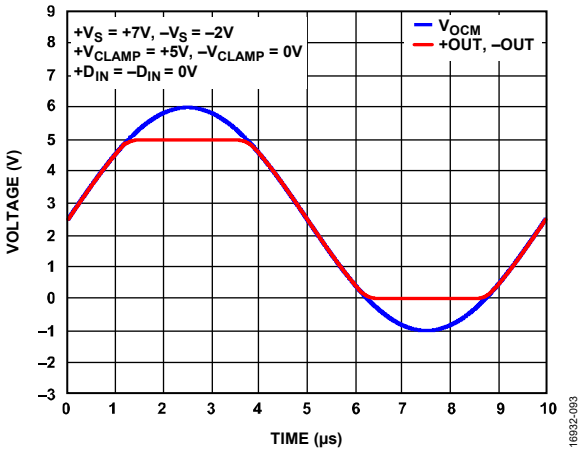


Figure 115. Clamped Common-Mode Signal Levels

DRIVING A HIGH PRECISION ADC

The ADA4945-1 is ideally suited for broadband dc-coupled applications. The recommended list of precision converters is shown in Table 15. The circuit in Figure 116 shows an example of the ADA4945-1 driving a precision ADC such as the AD4003 (an 18-bit, 2 MSPS, successive approximation ADC), or the AD7768 (a 24-bit, 256 kSPS, sigma-delta ADC). The ADA4945-1 is dc-coupled on the input and the output, which eliminates the need for a transformer to drive the ADC. In this example, the ADA4945-1 is applied in a differential input to differential output configuration, with a gain of 1, and with dual supplies of +7 V and −2 V. The output of the ADA4945-1 is level shifted to match the input common mode of the ADC. The gain is set by the ratio of the feedback resistor to the gain resistor. In addition, the circuit can be used in a single-ended input to differential output configuration. If needed, a termination resistor in parallel with the source input can be used. When a single-ended input is used, the input impedance of the amplifier can be calculated as shown in the Terminating a Single-Ended Input section. If the feedback and gain resistors are all 1 kΩ, as in Figure 116, the single-ended input impedance is approximately 1.33 kΩ, which, in parallel with a 52.3 Ω termination resistor, provides a 50 Ω termination for the source. An additional 25.5 Ω (1025.5 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input. However, if a differential source input is used, the differential input impedance is 2 kΩ. In this case, two 52.3 Ω termination resistors are used to terminate the inputs.

When driving the AD7768 in this example, the ADA4945-1 is driven by a signal generator having an 8 V p-p symmetric, bipolar output. The V_{OCM} input of the ADA4945-1 is bypassed for noise reduction and is driven via the common-mode source of the AD7768 to 2.5 V. With an output common-mode voltage of 2.5 V, each ADA4945-1 output swings between 0 V and 4 V, opposite in phase, providing a gain of 1 and a 8 V p-p differential signal to the ADC input. The differential RC section between the ADA4945-1 output and the ADC input provides a single-pole, low-pass filter to help reduce current spikes due to ADC input switching.

Table 14 shows the SNR and total harmonic distortion (THD) of the ADA4945-1 driving the AD7768 and AD4003 for various input frequencies at a near full-scale signal. The RC filter values in Figure 116 are also shown, as well as the reference voltage (REF) level.

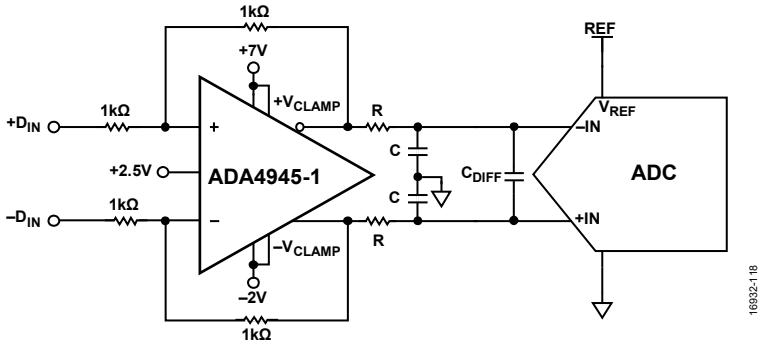


Figure 116. ADA4945-1 Driving Precision ADC

Table 14. SNR and THD for ADA4945-1 Driving AD7768 and AD4003

ADC	Frequency (kHz)	Signal Level (V p-p)	REF (V)	R (Ω)	C (nF)	C_{DIFF} (nF)	SNR (dB)	THD (dB)
AD7768	1	8.0	4.096	10	0.27	0.68	106.7	−115.9
	2	8.0	4.096	10	0.27	0.68	106.5	−115.5
	10	8.0	4.096	10	0.27	0.68	105.8	−116.9
	20	7.98	4.096	10	0.27	0.68	104.7	−116.2
AD4003	1	9.5	5.0	200	180.0	Not applicable	98.5	−123.5
	10	9.5	5.0	200	180.0	Not applicable	98.3	−117.0
	100	9.1	5.0	200	180.0	Not applicable	96.3	−100.3

Table 15. Recommended Converters

Product	Power (mW)	Throughput (MSPS)	Resolution (Bits)	SNR (dB)
AD4001	16	2	16	96
AD4003	16	2	18	100
AD4005	8	1	16	96
AD4007	8	1	18	100
AD4011	4	0.5	18	100
AD4020	20	2	20	100

LAYOUT, GROUNDING, AND BYPASSING

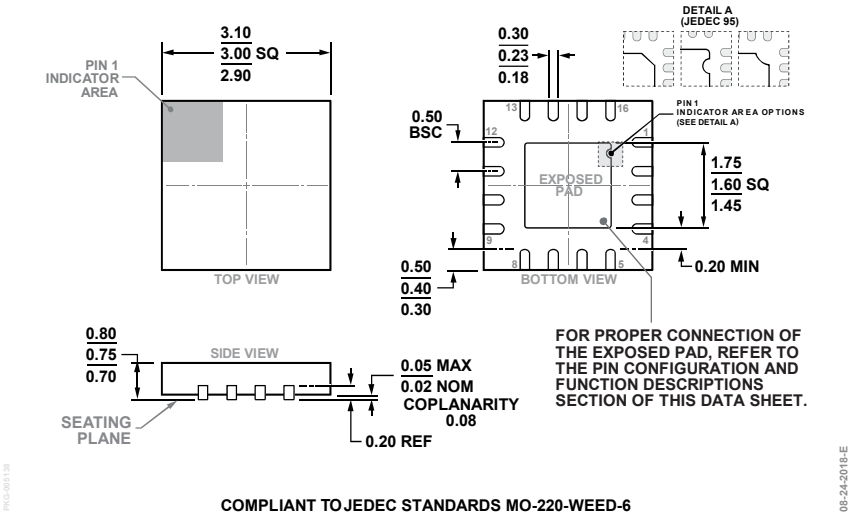
As a high speed device, the ADA4945-1 is sensitive to the PCB environment in which it operates. Using the superior performance of the ADA4945-1 requires attention to the details of high speed PCB design.

Ensure that signal routing is short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, ensure that PCB traces are close together, and twist any differential wiring such that loop area is minimized. This configuration reduces radiated energy and makes the circuit less susceptible to interference.

Bypass the power supply pins as near to the device as possible and directly to a nearby ground plane. Use high frequency ceramic chip capacitors. Use two parallel bypass capacitors (0.1 μF and 10 μF) for each supply. Place the 0.1 μF capacitor as near to the device as possible. Further away, provide low frequency bypassing using 10 μF tantalum capacitors from each supply to ground.

The ground plane must be as continuous and unbroken as possible to provide a low impedance path for return currents to the supply. As such, the ground plane should be kept free of any signal traces or other interruptions.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6

Figure 117. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Marking Code
ADA4945-1ACPZ-R2	−40°C to +125°C	16-Lead LFCSP	CP-16-22	250	C9D
ADA4945-1ACPZ-RL	−40°C to +125°C	16-Lead LFCSP	CP-16-22	5,000	C9D
ADA4945-1ACPZ-R7	−40°C to +125°C	16-Lead LFCSP	CP-16-22	1,500	C9D
ADA4945-1CP-EBZ		Evaluation Board			
AMC-ADA4945-1EBZ		ADC Mezzanine Card			

[1] Z = RoHS Compliant Part.

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