Dual-Channel, 3.7 GHz to 5.3 GHz, Receiver Front End

Preliminary Technical Data

ADRF5547

FEATURES

- Integrated dual-channel RF front end
  - 2-stage LNA and high power SPDT switch
  - On-chip bias and matching
  - Single supply operation
- Gain
  - High gain mode: 33 dB typical at 4.6 GHz
  - Low gain mode: 18 dB typical at 4.6 GHz
- Low noise figure
  - High gain mode: 1.6 dB typical at 4.6 GHz
  - Low gain mode: 1.6 dB typical at 4.6 GHz
- High isolation
  - RxOut-ChA and RxOut-ChB: 45 dB typical
  - TERM-ChA and TERM-ChB: 53 dB typical
- Low insertion loss: 0.5 dB typical at 4.6 GHz
- High power handling at T_{CASE} = 105°C
  - Full lifetime
    - LTE average power (9 dB PAR): 40 dBm
  - Single event (<10 sec operation)
    - LTE average power (9 dB PAR): 43 dBm
- High OIP3: 31 dBm typical
- Power-down mode and low gain mode for LNA
- Low supply current
  - High gain mode: 86 mA typical at 5 V
  - Low gain mode: 36 mA typical at 5 V
  - Power-down mode: 12 mA typical at 5 V
- Positive logic control
- 6 mm × 6 mm, 40-lead LFCSP (36mm²)

APPLICATIONS

- Wireless infrastructure
- TDD Massive Multiple input and Multiple Output (Massive MIMO) and Active Antenna Systems
- TDD-based Communication Systems

FUNCTIONAL BLOCK DIAGRAM

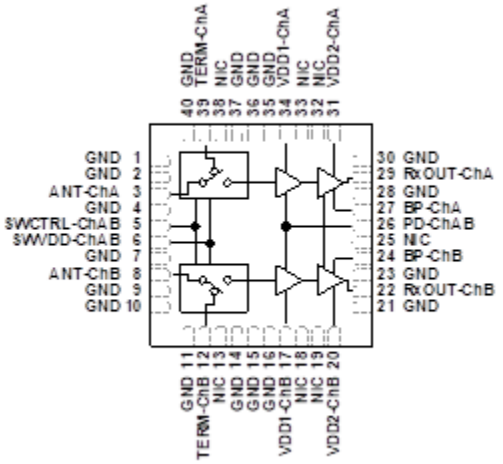

Figure 1.

GENERAL DESCRIPTION

The ADRF5547 is a dual-channel, integrated radio frequency (RF), front end multichip module designed for time division duplexing (TDD) applications and that operates from 3.7 GHz to 5.3 GHz. The ADRF5547 is configured in dual channels with a cascading two-stage low noise amplifier (LNA) and a high power silicon single-pole, double-throw (SPDT) switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure (NF) of 1.6 dB and high gain of 33 dB at 4.6 GHz with an output third order intercept point (OIP3) of 31 dBm (typical). In low gain mode, one stage of the two-stage LNAs is in bypass, providing 18 dB gain at lower current of 36 mA. In power-down mode, the LNAs are turned off and the device draws 12 mA.

In transmit operation, when RF inputs are connected to termination pin (TERM-ChA or TERM-ChB), the switch provides a low insertion loss of 0.5 dB and handles long term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 40 dBm for full lifetime operation and 43 dBm for single event (<10 sec) LNA protection operation.

The device comes in an RoHS-compliant, compact, 40-lead, 6 mm × 6 mm LFCSP package.

Rev. PrC Document Feedback

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, and SWVDD-ChAB = 5 V; SWCTRL-ChAB = 0 V or SWVDD-ChAB; BP-ChA = VDD1-ChA or 0 V; BP-ChB = VDD1-ChB or 0 V; PD-ChAB = 0 V or VDD1-ChA; case temperature (T_{CASE}) = 25°C, 50 Ω system, unless otherwise noted.

Table 1

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		3.7		5.3	GHz
GAIN[1]	Receive operation at 4.6 GHz				
High Gain Mode			33		dB
Low Gain Mode			18		dB
GAIN FLATNESS[1]	Receive operation in any 100 MHz bandwidth				
High Gain Mode			0.6		dB
Low Gain Mode			0.2		dB
NOISE FIGURE (NF)[1]	Receive operation at 4.6 GHz				
High Gain Mode			1.6		dB
Low Gain Mode			1.6		dB
OUTPUT THIRD ORDER INTERCEPT POINT (OIP3)[1]	Receive operation, two-tone output power = 8dBm per tone at 1 MHz tone spacing				
High Gain Mode			31		dBm
Low Gain Mode			22		dBm
OUTPUT 1 dB COMPRESSION (OP1dB)					
High Gain Mode			18		dBm
Low Gain Mode			6		dBm
INSERTION LOSS[1]	Transmit operation at 4.6 GHz		0.50		dB
CHANNEL TO CHANNEL ISOLATION	At 4.6 GHz				
Between RxOut-ChA and RxOut-ChB[1]	Receive operation		45		dB
Between TERM-ChA and TERM-ChB[1]	Transmit operation		53		dB
SWITCH ISOLATION					
ANT-ChA to TERM-ChA and ANT-ChB to TERM-ChB[1]	Transmit operation, PD-ChAB = 0 V		20		dB
SWITCHING CHARACTERISTICS (T_{ON}, T_{OFF})					
	50% control voltage to 90%, 10% of RxOut-ChA or RxOut-ChB in receive operation		860		ns
	50% control voltage to 90%, 10% of TERM-ChA or TERM-ChB in transmit operation		800		ns
RF INPUT POWER AT ANT-CHA, ANT-CHB[1]	Receive operation, LTE average (9 dB PAR)			15	dBm
RECOMMENDED OPERATING CONDITIONS					
Bias Voltage Range	VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, SWVDD-ChAB	4.75	5	5.25	V
Control Voltage Range	SWCTRL-ChAB, BP-ChA, BP-ChB, PD-ChAB	0		VDD[3]	V
RF Input Power at ANT-ChA, ANT-ChB	SWCTRL-ChAB = 5 V, BP-ChA = BP-ChB = 0 V, PD-ChAB = 5V, T_{CASE} = 105°C[2]				
	Continuous wave			40	dBm
	9 dB PAR LTE full lifetime average			40	dBm
	9 dB PAR LTE single event (<10 sec) average			43	dBm
Case Temperature Range (T_{CASE})[2]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}[2]					
	Receive operation[1]			132	°C
	Transmit operation[1]			134	°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
SWCTRL-ChAB, PD-ChAB					
Low (V_{IL})		0		0.7	V
High (V_{IH})		1.4		VDD[3]	V
BP-ChA, BP-ChB					
Low (V_{IL})		0		0.3	V
High (V_{IH})		1.0		VDD[3]	V
SUPPLY CURRENT (I_{DD})	VDD1-Chx and VDD2-Chx = 5 V per channel				
High Gain			86		mA
Low Gain			36		mA
Power-Down Mode			12		mA
TX current (Switch)	SWVDD-ChAB = 5 V		4.3		mA
DIGITAL INPUT CURRENTS	SWCTRL-ChAB, PD-ChAB, BP-ChA, BP-ChB =5 V per channel				
SWCTRL-ChAB			0.0004		mA
PD-ChAB			0.2		mA
BP-ChA, BP-ChB			0.4		mA

[1] See Table and Table .
[2] Measured at EPAD.
[3] V_{DD} is the voltage of the SWVDD-CHAB, VDD1-CHA, VDD1-CHB, VDD2-CHA, and VDD2-CHB pins.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
POSITIVE SUPPLY VOLTAGE	
VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB	7 V
SWVDD-ChAB	5.4 V
DIGITAL CONTROL INPUT VOLTAGE	
SWCTRL-ChAB	−0.3 V to V_{DD}[1] + 0.3 V
BP-ChA, BP-ChB, PD-ChAB	−0.3 V to V_{DD}[1] + 0.3 V
RF INPUT POWER	
Transmit Input Power (LTE Peak)	53 dBm
Receive Input Power (LTE Peak)	25 dBm
TEMPERATURE	
Storage	−65°C to +150°C
Reflow (MSL3 Rating)	260°C
ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY	
Human Body Model (HBM)	500 V, Class 1B
Charge Device Model (CDM)	1.25 KV

[1] V_{DD} is the voltage of the VDD1-CHA, VDD1-CHB, VDD2-CHA, and VDD2-CHB pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-40-15		
High Gain and Low Gain Mode	30	°C/W
Power-Down Mode	8.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

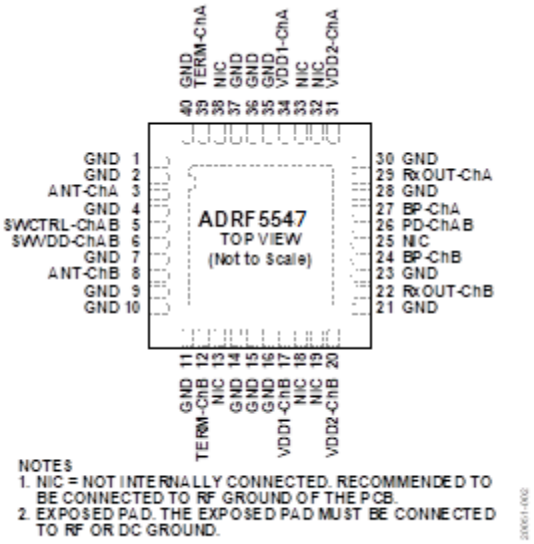


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 7, 9 to 11, 14 to 16, 21, 23, 28, 30, 35 to 37, 40	GND	Ground.
3	ANT-CHA	RF Input to Channel A.
5	SWCTRL-CHAB	Control Voltage for Switches on Channel A and Channel B.
6	SWVDD-CHAB	Supply Voltage for Switches on Channel A and Channel B.
8	ANT-CHB	RF Input to Channel B.
12	TERM-CHB	Termination Output. This pin is the transmitter path for Channel B.
13, 18, 19, 25, 32, 33, 38	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-CHB	Supply Voltage for Stage 1 LNA on Channel B.
20	VDD2-CHB	Supply Voltage for Stage 2 LNA on Channel B.
22	RXOUT-CHB	RF Output. This pin is the receiver path for Channel B.
24	BP-CHB	Bypass Second Stage LNA of Channel B.
26	PD-CHAB	Power-Down All Stages of LNA for Channel A and Channel B.
27	BP-CHA	Bypass Second Stage LNA of Channel A.
29	RXOUT-CHA	RF Output. This pin is the receiver path for Channel A.
31	VDD2-CHA	Supply Voltage for Stage 2 LNA on Channel A.
34	VDD1-CHA	Supply Voltage for Stage 1 LNA on Channel A.
39	TERM-CHA	Termination Output. This pin is the transmitter path for Channel A.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface

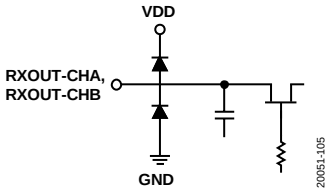


Figure 4. RXOUT-CHx Interface

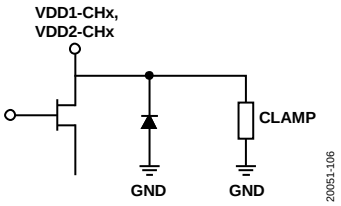


Figure 5. VDD1-CHx, VDD2-CHx Interface

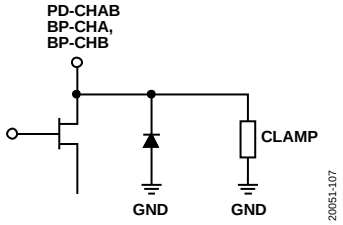


Figure 6. PD-CHAB, BP-CHx Interface

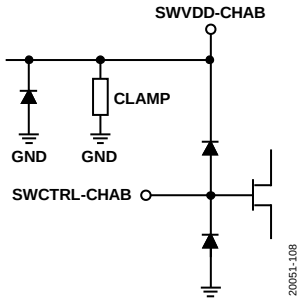


Figure 7. SWCTRL-CHAB, SWVDD-CHAB Interface

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION, HIGH GAIN MODE

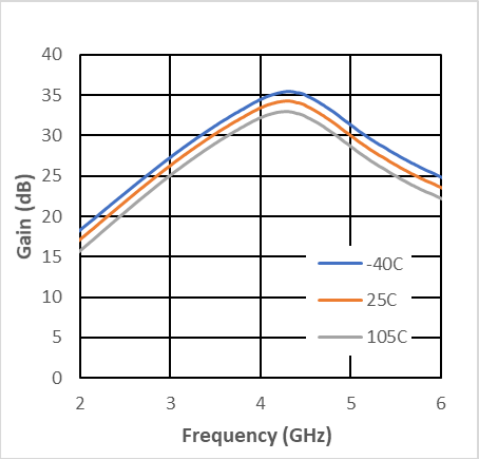


Figure 8. Gain vs. Frequency at Various Temperatures

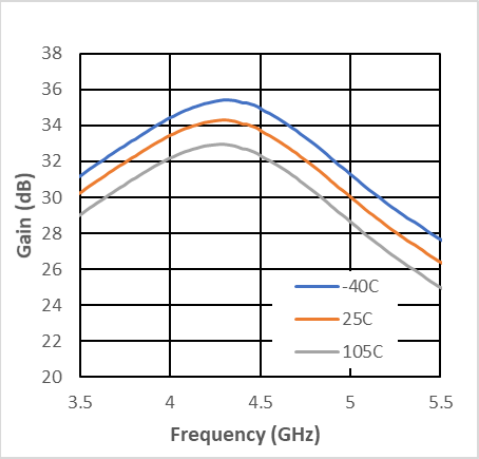


Figure 11. Gain vs. Frequency at Various Temperatures, 3.5 GHz to 5.5 GHz

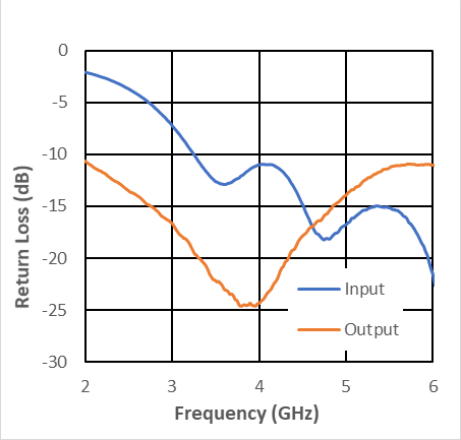


Figure 9. Return Loss vs. Frequency

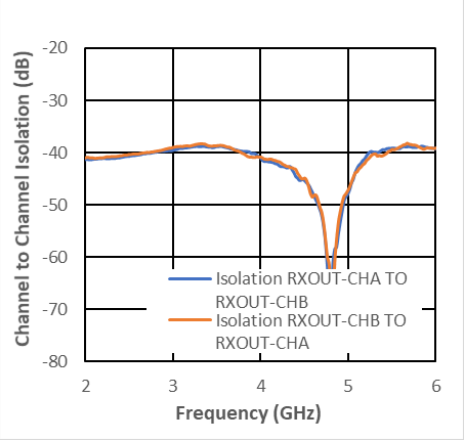


Figure 12. Channel to Channel Isolation vs. Frequency

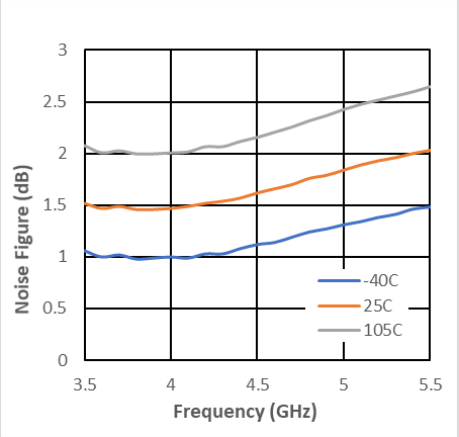


Figure 10. Noise Figure vs. Frequency

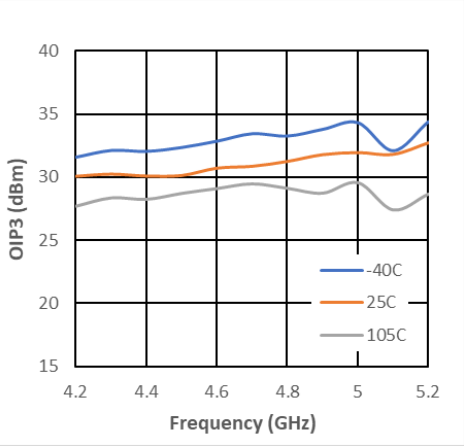


Figure 13. OIP3 vs. Frequency, 8 dBm Output Tone Power

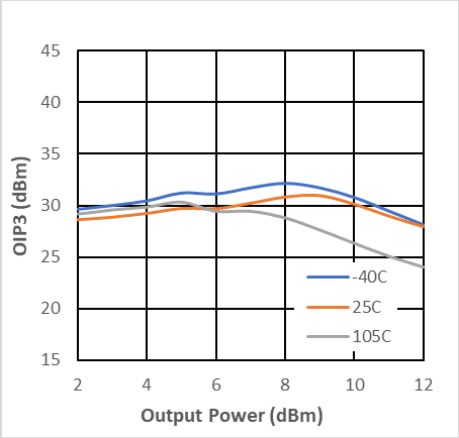


Figure 14. OIP3 vs. Output Power, 4.6 GHz

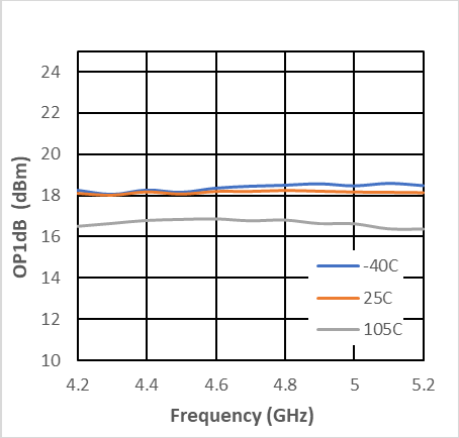


Figure 15. OP1dB vs. Frequency at Various Temperatures

RECEIVE OPERATION, LOW GAIN MODE

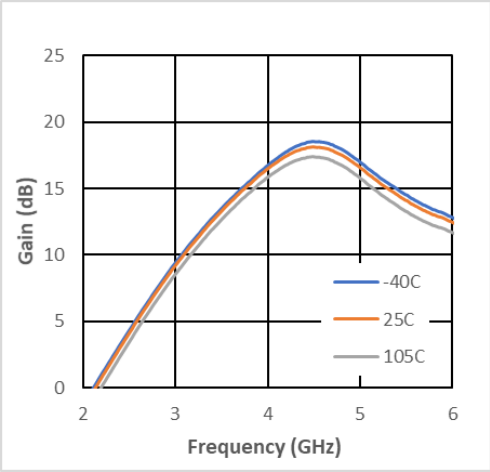


Figure 16. Gain vs. Frequency at Various Temperatures

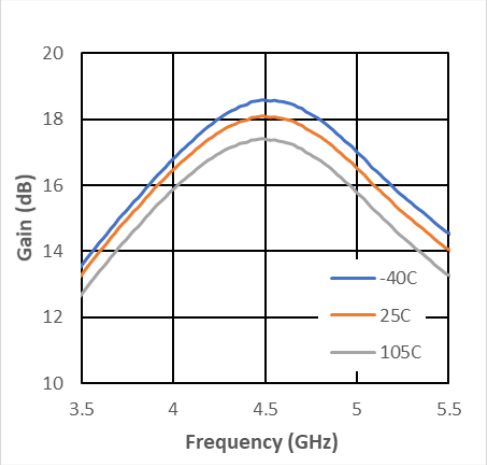


Figure 19. Gain vs. Frequency at Various Temperatures 3.5 GHz to 5.5 GHz

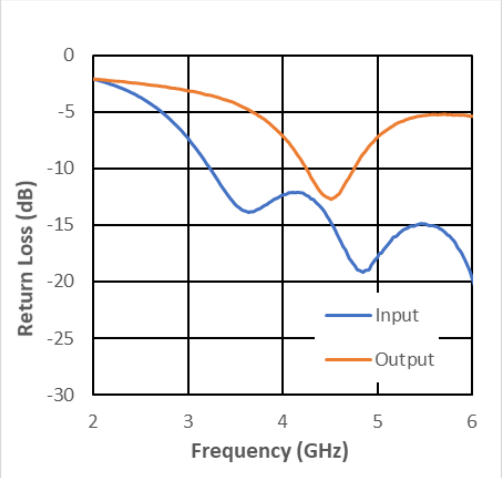


Figure 17. Return Loss vs. Frequency

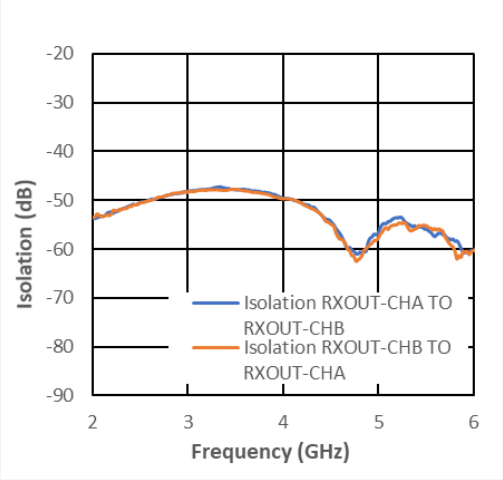


Figure 20. Channel to Channel Isolation vs. Frequency

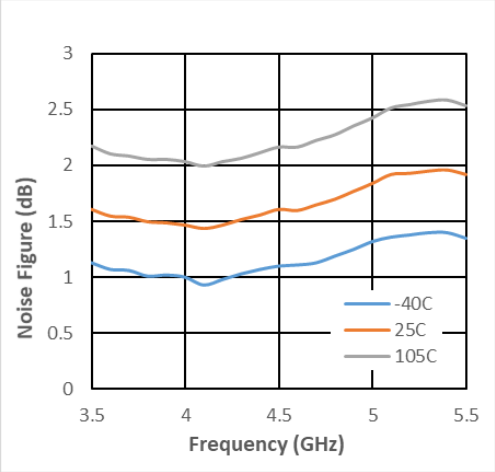


Figure 18. Noise Figure vs. Frequency at Various Temperatures

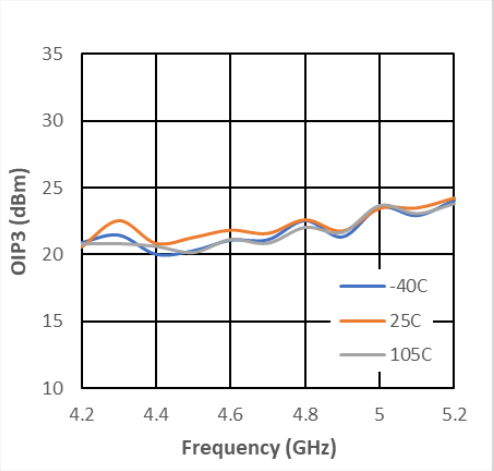


Figure 21. OIP3 Vs Frequency, -8dBm Output Tone Power

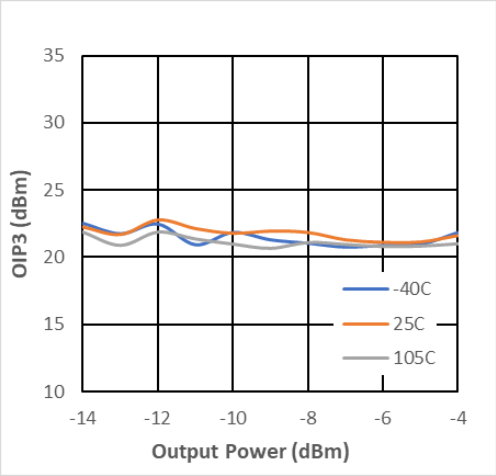


Figure 22. OIP3 vs. Output Power, 4.6 GHz

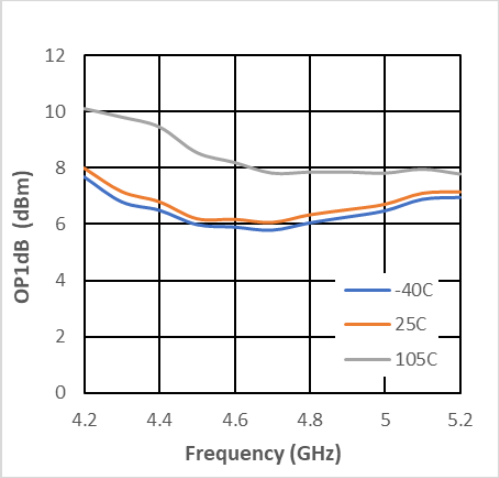


Figure 24. OP1dB Vs Frequency at Various Temperatures

TRANSMIT OPERATION

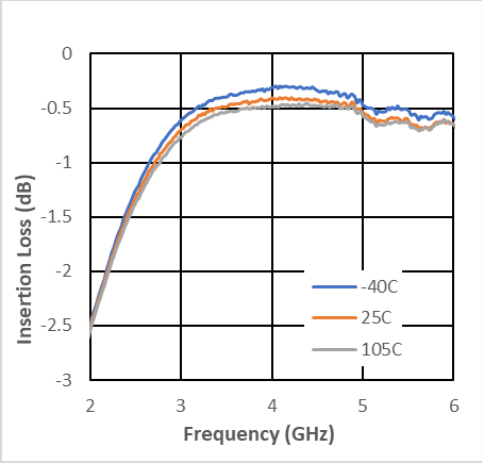


Figure 23. Insertion Loss vs. Frequency at Various Temperatures

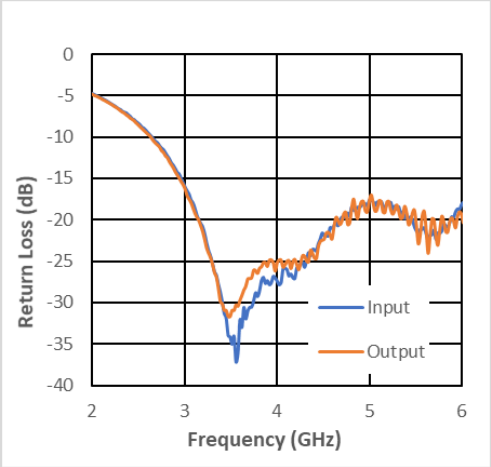


Figure 25. Return Loss vs. Frequency

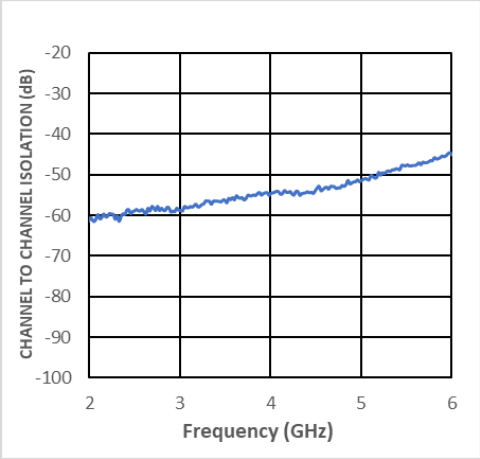


Figure 26. Channel to Channel Isolation vs. Frequency

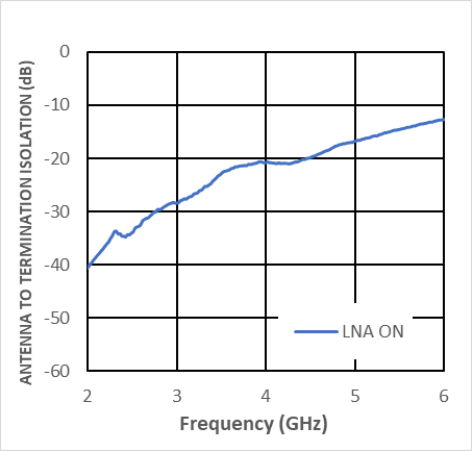


Figure 27. Antenna to Termination Isolation vs. Frequency

THEORY OF OPERATION

The ADRF5547 requires a positive supply voltage applied to VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB. Use bypassing capacitors on the supply lines to filter noise.

SIGNAL PATH SELECT

The ADRF5547 supports transmit operations when 5 V is applied to SWCTRL-ChAB. In transmit operation, when an RF input is applied to ANT-ChA and ANT-ChB, the signal paths are connected from ANT-ChA to TERM-ChA and from ANT-ChB to TERM-ChB.

The ADRF5547 supports receive operations when 0 V is applied to SWCTRL-ChAB. In receive operation, an RF input applied at ANT-ChA and ANT-ChB connects ANT-ChA to RxOUT-ChA and ANT-ChB to RxOUT-ChB.

Transmit Operation

The ADRF5547 supports insertion loss mode and isolation mode when in transmit operation, that is, when SWCTRLCHAB = 5 V. As detailed in Table 6, with PD-CHAB set to 5 V and BP-CHA or BP-CHB set to 0 V, insertion loss mode is selected. Under the same circumstances, isolation mode is selected by applying 0 V to PD-CHAB

Receive Operation

The ADRF5547 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table .

When 0 V is applied to PD-ChAB, the LNA is powered up and the user can select high gain mode or low gain mode. To select high gain mode, apply 0 V to BP-ChA or BP-ChB. To select low gain mode, apply 5 V to BP-ChA or BP-ChB.

When 5 V is applied to PD-ChAB, the ADRF5547 enters power-down mode. To select power-down high isolation mode, apply 0 V to BP-ChA or BP-ChB. To select power-down low isolation mode, apply 5 V to BP-ChA or BP-ChB.

BIASING SEQUENCE

To bias up the ADRF5547, perform the following steps:

1. Connect GND to ground.
2. Bias up VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB.
3. Bias up SWCTRL-ChAB.
4. Bias up PD-ChAB.
5. Bias up BP-ChA and BP-ChB.
6. Apply an RF input signal.

To bias down, perform these steps in the reverse order.

Table 5. Truth Table: Signal Path

	Signal Path Select	
SWCTRL-ChAB	**Transmit Operation[1]**	**Receive Operation**
Low	Off	On
High	On	Off

[1] See the signal path descriptions in Table 6.

Table 6. Truth Table: Operation

Operation	PD-ChAB	BP-ChA, BP-ChB	Signal Path
Receive Operation			ANT-ChA to RxOUT-ChA, ANT-ChB to RxOUT-ChB
High Gain Mode	Low	Low	
Low Gain Mode	Low	High	
Power-Down High Isolation Mode	High	Low	
Power-Down Low Isolation Mode	High	High	
Transmit Operation			ANT-CHA to TERM-CHA, ANT-CHB to TERM-CHB
Insertion Loss Mode	High	Low	
Isolation Mode	Low	Low	

APPLICATIONS INFORMATION

To generate the evaluation PCB used in the application circuit shown in **Error! Reference source not found.**, use proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and the backside ground slug must connect directly to the ground plane. The evaluation board shown in Figure is available from Analog Devices, Inc., upon request.

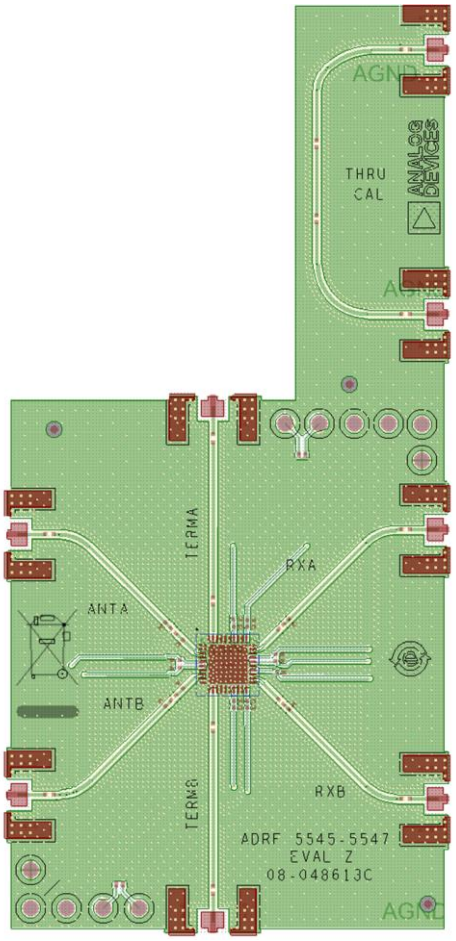


Figure 28. ADRF5547-EVALZ Evaluation Board

The ADRF5547-EVALZ consists of eight metal layers, with dielectrics between each layer, as shown in Figure . The top and the bottom metal layers have a copper thickness of 2 oz (2.7 mil), and the six metal layers in between have a copper thickness of 1oz (1.3 mil). The top dielectric material is 10 mil Rogers RO4350, which exhibits a very low thermal coefficient, offering control over thermal rise of the board. The dielectrics between other metal layers are FR4. The overall board thickness is 62 mil.

The top copper layer has all RF and dc traces. The other seven layers are ground layers that also help to manage thermal rise on the evaluation board during high power operations. In addition, several via holes are provided around the transmission lines and under the exposed pad of the package for proper thermal grounding.

To ensure maximum heat dissipation and reduce thermal rise on the board, several application considerations are essential. The bottom of the evaluation board must be attached to a copper support plate. The ADRF5547-EVALZ comes with this support plate attachment. Attach the evaluation board and support plate to a heat sink. Use thermal grease during all high power operations.

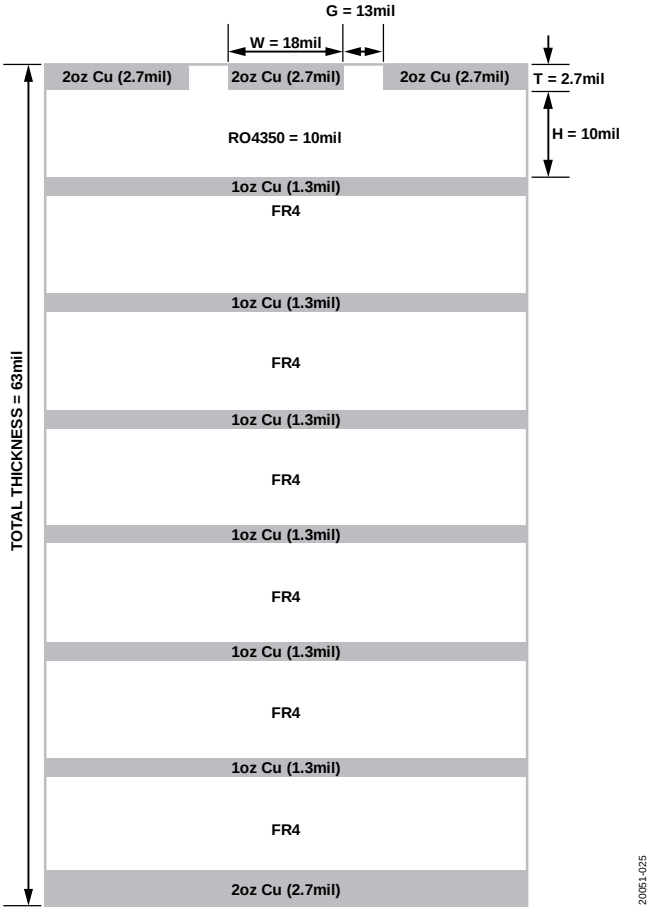


Figure 29. ADRF5547-EVALZ Layers

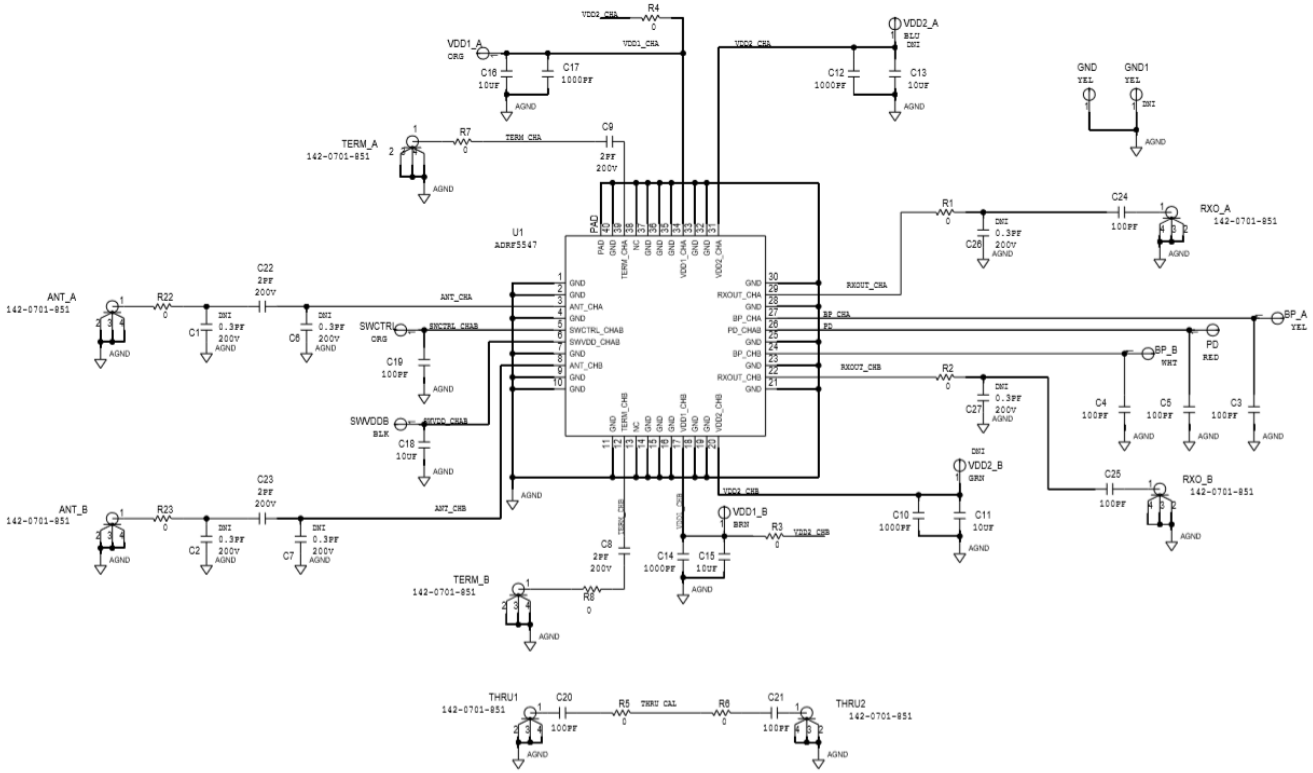


Figure 30. Application Circuit

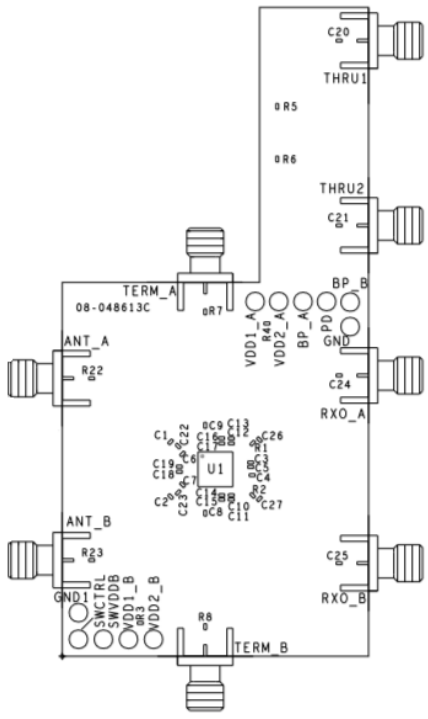
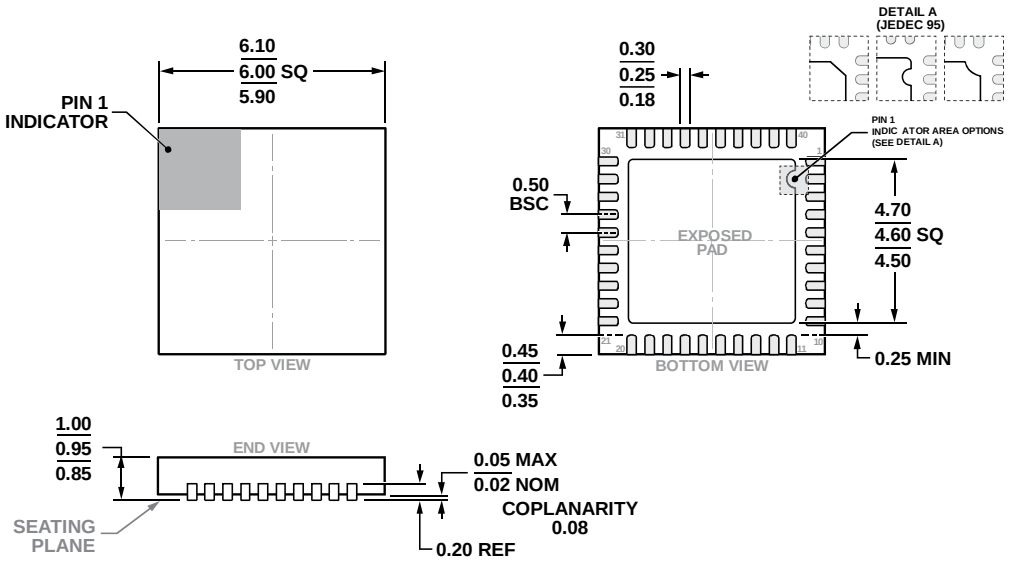


Figure 31. ADRF5547-EVALZ Evaluation Board Top View

Table 7. Bill of Materials for ADRF5547-EVALZ Evaluation Board

Reference Designator	Description
J1 to J8	PCB mount Subminiature Version A (SMA) connector
C10,C12,C14,C17	1000 pF, 25 V capacitor, 0402 package
C11,C13,C15,C16,C18	10 µF, 10 V capacitor, 0402 package
C19,C20,C21,C24,C25	100 pF capacitor, 200 V, 0402 package
C8,C9,C22,C23	2pF capacitor, 200 V, 0402 package
C3,C4,C5	100 pF, 50 V capacitor, 0402 package
R1,R2,R3,R4,R5,R6,R7,R8,R22,R23	0 Ω resistor, 0402 package
U1	ADRF5547 integrated circuit (IC)
PCB[1]	ADRF5547-EVALZ evaluation PCB

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 32. 40-Terminal Lead Frame Chip Scale Package [LFSCP]
6 mm × 6 mm Body and 0.95mm Package Height
(CP-40-15)
Dimensions shown in millimeters

[1] Circuit board material: Rogers RO4350 or Arlon 25FR.

PR20790-0-5/19(PrC)