

## 7 GHz INTEGER N SYNTHESIZER (N = 12 - 259)



### Typical Applications

The HMC698LP5(E) is ideal for:

- Satellite Communication Systems
- Point-to-Point Radios
- Military Applications
- Sonet Clock Generation

### Features

Ultra Low SSB Phase Noise Floor:

-153 dBc/Hz @ 10 kHz offset @ 100 MHz  
Reference Frequency.

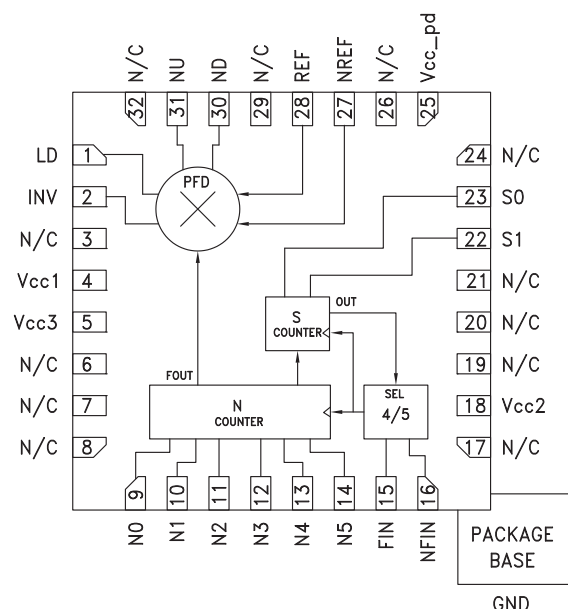
Programmable Divider (N= 12 - 259) Operating  
up to 7 GHz

Open Collector Output Buffer Amplifiers for  
Interfacing w/ Op-Amp Based Loop Filter

Reversible Polarity PFD w/ Lock Detect Output

32 Lead 5x5mm SMT Package: 25mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC698LP5(E) is a frequency synthesizer with a wideband reversible polarity digital PFD and lock detect output. The divider operates unconditionally from 80 - 7000 MHz with a continuous integer division ratio of 12 to 259. The HMC698LP5(E) high frequency operation along with ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast settling and very low phase noise. When used in conjunction with a differential loop filter, the HMC698LP5(E) can be used to phase lock a VCO to a reference oscillator.

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{cc} = V_{cc1} = V_{cc2} = V_{cc3} = V_{cc\_pd} = 5\text{V}$

| Parameter                    | Conditions                                                     | Min. | Typ. | Max. | Units       |
|------------------------------|----------------------------------------------------------------|------|------|------|-------------|
| Maximum Ref. Input Frequency | Sine or Square Wave Input [1]                                  | 1300 |      |      | MHz         |
| Minimum Ref. Input Frequency | Square Wave Input [2]                                          |      |      | 10   | MHz         |
| Reference Input Power Range  | 100 MHz Frequency                                              | -5   |      | +5   | dBm         |
| Maximum VCO Input Frequency  |                                                                | 7000 |      |      | MHz         |
| Minimum VCO Input Frequency  |                                                                |      |      | 80   | MHz         |
| VCO Input Power Range        | 100 MHz Input Frequency                                        | -10  |      | +5   | dBm         |
| PFD Output Voltage           |                                                                |      | 2000 |      | mV, Pk - Pk |
| PFD Gain                     | Gain = $V_{pp} / 2\pi$ Rad.                                    |      | 0.32 |      | V/Rad.      |
| SSB Phase Noise              | @ 10 kHz Offset @ 100 MHz Square Wave Ref. Input<br>Pin= 0 dBm |      | -153 |      | dBc/Hz      |
| Total Supply Current         |                                                                |      | 310  |      | mA          |

[1] Maximum frequencies may be limited by available counter division ratio.

[2] Square wave input achieves best phase noise at lower ref. frequency (see sine & square wave comparison plots)

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

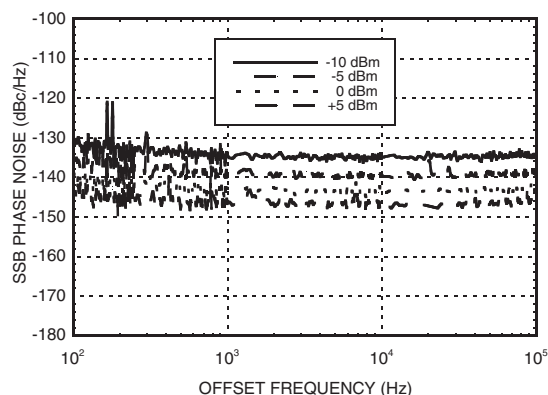
For price, delivery, and to place orders: Analog Devices, Inc.,  
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106  
Phone: 781-329-4700 • Order online at [www.analog.com](http://www.analog.com)  
Application Support: Phone: 1-800-ANALOG-D



## 7 GHz INTEGER N SYNTHESIZER (N = 12 - 259)

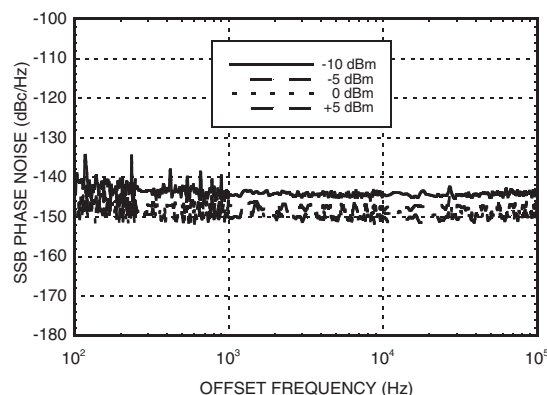
### Phase Noise Floor <sup>[1][2][3]</sup>

Ref = Sine Wave, Vcc = 4.75V



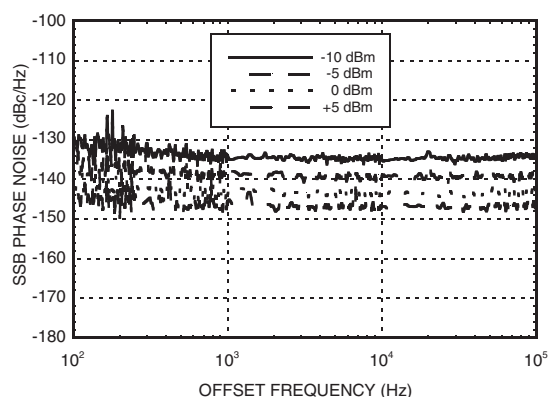
### Phase Noise Floor <sup>[1][2][3]</sup>

Ref = Square Wave, Vcc = 4.75V



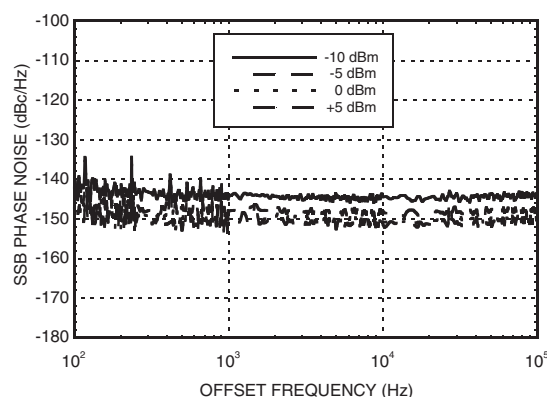
### Phase Noise Floor <sup>[1][2][3]</sup>

Ref = Sine Wave, Vcc = 5V



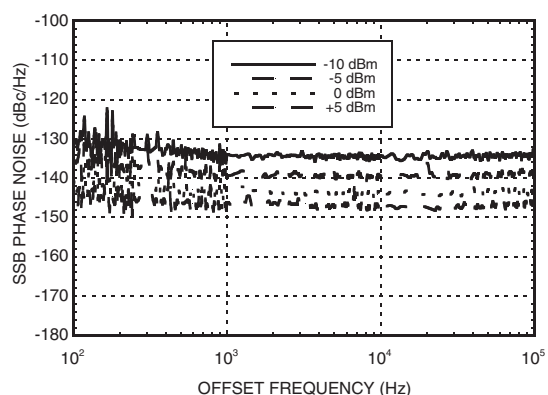
### Phase Noise Floor <sup>[1][2][3]</sup>

Ref = Square Wave, Vcc = 5V



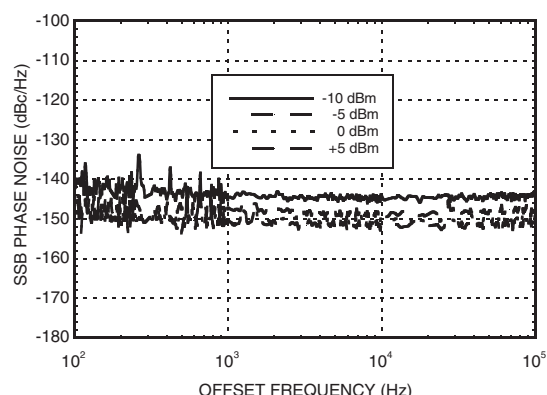
### Phase Noise Floor <sup>[1][2][3]</sup>

Ref = Sine Wave, Vcc = 5.25V

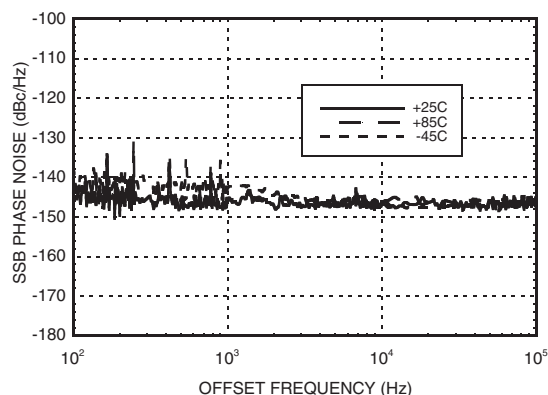
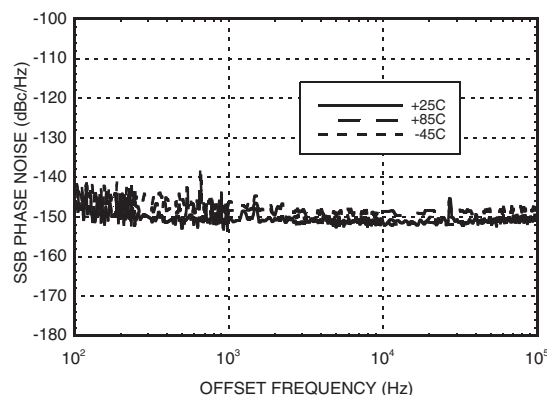
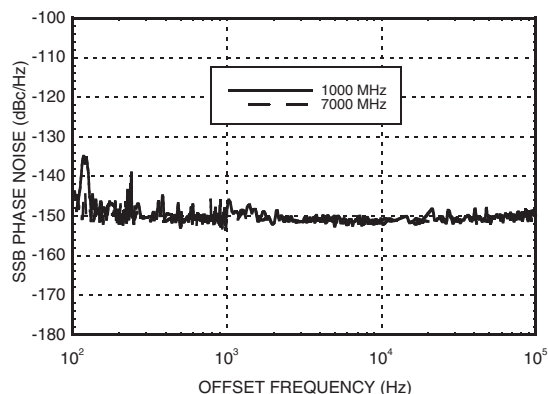


### Phase Noise Floor <sup>[1][2][3]</sup>

Ref = Square Wave, Vcc = 5.25V



- [1] Phase Noise Floor vs Offset Frequency with varying Ref Power Level  
 [2] Fin= 7000 MHz @ 0 dBm, Ref Frequency = 100 MHz, N = 70  
 [3] Phase Noise Floor remains constant beyond 100 kHz offset frequency


**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**
**Phase Noise Floor <sup>[1][2][3]</sup>**
**Ref = Sine Wave @ 5 dBm, Vcc = 5V**

**Phase Noise Floor <sup>[1][2][3]</sup>**
**Ref = Square Wave @ 5 dBm, Vcc = 5V**

**Phase Noise Floor vs Offset Frequency  
with varying Fin @ 0 dbm, Ref = 100 MHz  
Square Wave @ 5 dBm, Vcc = 5V <sup>[3]</sup>**


[1] Phase Noise Floor vs Offset Frequency over temperature

[2] Fin= 7000 MHz @ 0 dBm, Ref Frequency = 100 MHz, N = 70

[3] Phase Noise Floor remains constant beyond 100 kHz offset frequency



# HMC698LP5 / 698LP5E

## 7 GHz INTEGER N SYNTHESIZER (N = 12 - 259)

### Absolute Maximum Ratings

|                                                                            |                       |
|----------------------------------------------------------------------------|-----------------------|
| RF Input (Vcc= +5V)                                                        | +10 dBm               |
| Supply Voltage (Vcc)                                                       | +5.5V                 |
| Logic Inputs                                                               | -0.5V to (0.5V + Vcc) |
| Junction Temperature (Tc)                                                  | 135 °C                |
| Continuous P <sub>diss</sub> (T = 85 °C)<br>(derate 78 mW/° C above 85 °C) | 3.9 W                 |
| Thermal Resistance<br>(Junction to ground paddle)                          | 12.90 °C/W            |
| Storage Temperature                                                        | -65 to +150 °C        |
| Operating Temperature                                                      | -40 to +85 °C         |

### Typical Supply Current vs. Vcc

| Vcc (Vdc) | Icc (mA) |
|-----------|----------|
| 4.75      | 294      |
| 5.00      | 310      |
| 5.25      | 342      |

Note: HMC698LP5 will work over full voltage range above.



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

**6**

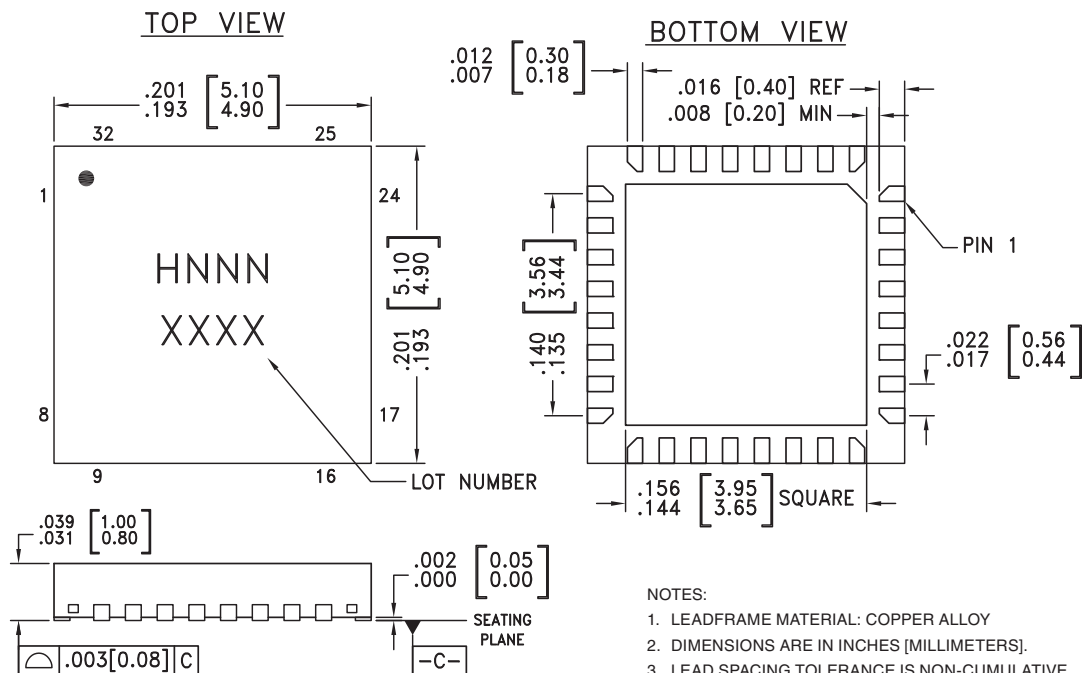
### Typical DC Characteristics @ Vcc = +5V

| Symbol | Characteristics               | +25C |      |      | Units |
|--------|-------------------------------|------|------|------|-------|
|        |                               | Min. | Typ. | Max. |       |
| Icc    | Power Supply Current          | 280  | 310  | 340  | mA    |
| Voh    | Output High Voltage, (NU, ND) | 5    | 5    | 5    | V     |
| Vol    | Output Low Voltage, (NU, ND)  | 2.9  | 3.0  | 3.1  | V     |



## 7 GHz INTEGER N SYNTHESIZER (N = 12 - 259)

### Outline Drawing



#### NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.  
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

### Package Information

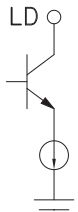
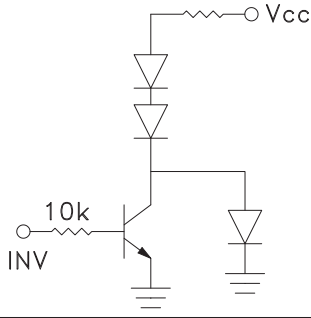
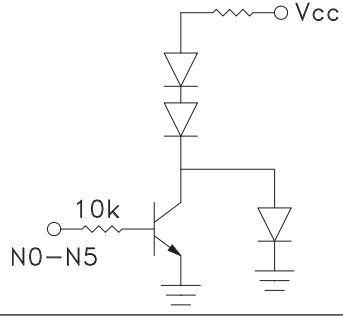
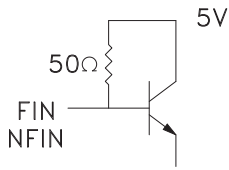
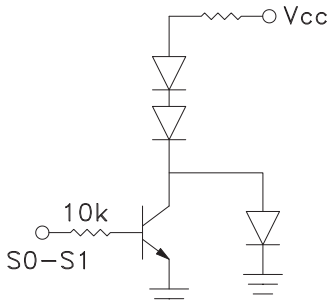
| Part Number  | Package Body Material                              | Lead Finish   | MSL Rating          | Package Marking <sup>[3]</sup> |
|--------------|----------------------------------------------------|---------------|---------------------|--------------------------------|
| HMC698LP5    | Low Stress Injection Molded Plastic                | Sn/Pb Solder  | MSL1 <sup>[1]</sup> | H698<br>XXXX                   |
| HMC698LP5(E) | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 <sup>[2]</sup> | H698<br>XXXX                   |

[1] Max peak reflow temperature of 235 °C

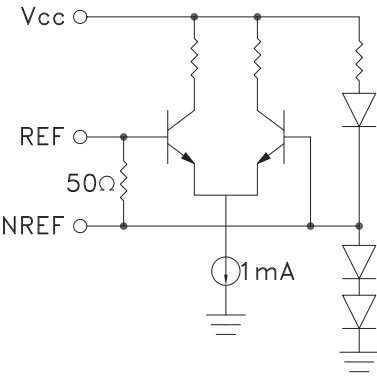
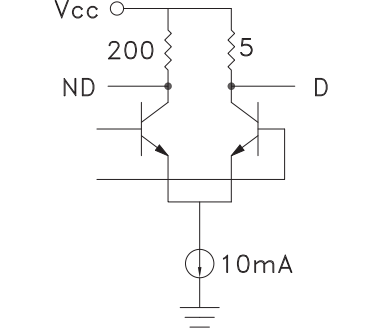
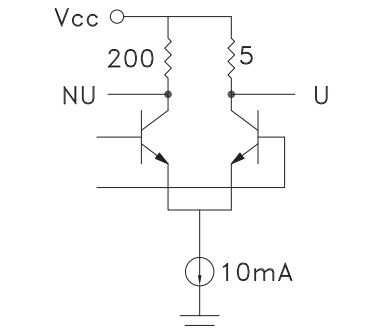
[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX


**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**
**Pin Description**

| Pin Number   | Function                    | Description                                                                                               | Interface Schematic                                                                   |
|--------------|-----------------------------|-----------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 1            | LD                          | Pulsed output.<br>Average "LOW" = UNLOCKED.<br>Average "HIGH" = LOCKED                                    |    |
| 2            | INV                         | PFD INVERT function<br>CMOS compatible input control bit<br>Logic "LOW" = NORMAL<br>Logic "HIGH" = INVERT |    |
| 4, 5, 18, 25 | Vcc1, Vcc3,<br>Vcc2, Vcc_pd | Supply Voltage 5V ±0.25V                                                                                  |                                                                                       |
| 9 - 14       | N0 - N5                     | CMOS compatible control input bit 0 (LSB) - 5                                                             |  |
| 15           | FIN                         | (These pins are AC coupled and must be DC Blocked externally.)<br>Frequency Input                         |  |
| 16           | NFIN                        |                                                                                                           |                                                                                       |
| 22, 23       | S1, S0                      | CMOS compatible<br>Control Input<br>bit 0 (LSB) -1                                                        |  |


**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**
**Pin Description** (Continued)

| Pin Number                                  | Function | Description                                                                                      | Interface Schematic                                                                   |
|---------------------------------------------|----------|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 28                                          | REF      | Reference Input                                                                                  |    |
| 27                                          | NREF     | Reference Input Complement<br>(These pins are AC coupled and must be DC Blocked externally.)     |                                                                                       |
| 30                                          | ND       | Down Output                                                                                      |   |
| 31                                          | NU       | Up Output                                                                                        |  |
| 3, 6 - 8, 17,<br>19 - 21, 24,<br>26, 29, 32 | N/C      | No Connection. These pins may be connected to RF/DC ground.<br>Performance will not be affected. |                                                                                       |
| Ground Paddle                               | GND      | Package bottom has an exposed ground paddle that must be connected to RF/DC ground               |  |


**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**
**HMC698LP5(E) Programming Truth Table**

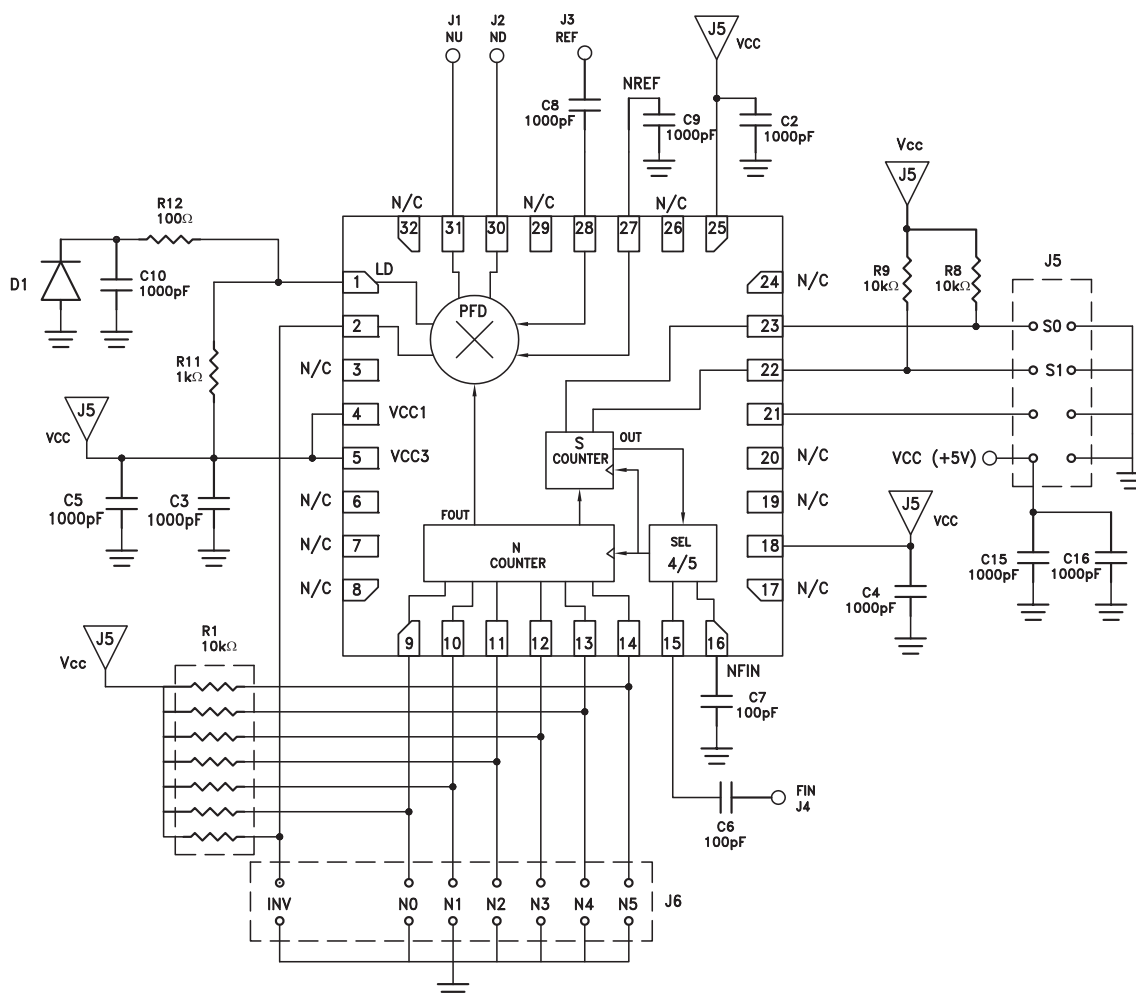
| Division Ratio n | N Counter | N Counter Decimal Set | Swallow S Counter | Swallow S Decimal Set | (LSB) N0 | N1 | N2 | N3 | N4 | N5 | (LSB) S0 | S1 |
|------------------|-----------|-----------------------|-------------------|-----------------------|----------|----|----|----|----|----|----------|----|
| 12               | 3         | 2                     | 0                 | 0                     | 0        | 1  | 0  | 0  | 0  | 0  | 0        | 0  |
| 13               | 3         | 2                     | 1                 | 1                     | 0        | 1  | 0  | 0  | 0  | 0  | 1        | 0  |
| 14               | 3         | 2                     | 2                 | 2                     | 0        | 1  | 0  | 0  | 0  | 0  | 0        | 1  |
| 15               | 3         | 2                     | 3                 | 3                     | 0        | 1  | 0  | 0  | 0  | 0  | 1        | 1  |
| 16               | 4         | 3                     | 0                 | 0                     | 1        | 1  | 0  | 0  | 0  | 0  | 0        | 0  |
| 17               | 4         | 3                     | 1                 | 1                     | 1        | 1  | 0  | 0  | 0  | 0  | 1        | 0  |
| 18               | 4         | 3                     | 2                 | 2                     | 1        | 1  | 0  | 0  | 0  | 0  | 0        | 1  |
| 19               | 4         | 3                     | 3                 | 3                     | 1        | 1  | 0  | 0  | 0  | 0  | 1        | 1  |
| 20               | 5         | 4                     | 0                 | 0                     | 0        | 0  | 1  | 0  | 0  | 0  | 0        | 0  |
| 21               | 5         | 4                     | 1                 | 1                     | 0        | 0  | 1  | 0  | 0  | 0  | 1        | 0  |
| 22               | 5         | 4                     | 2                 | 2                     | 0        | 0  | 1  | 0  | 0  | 0  | 0        | 1  |
| 23               | 5         | 4                     | 3                 | 3                     | 0        | 0  | 1  | 0  | 0  | 0  | 1        | 1  |
| ⋮                | ⋮         | ⋮                     | ⋮                 | ⋮                     | ⋮        | ⋮  | ⋮  | ⋮  | ⋮  | ⋮  | ⋮        | ⋮  |
| 252              | 63        | 62                    | 0                 | 0                     | 0        | 1  | 1  | 1  | 1  | 1  | 0        | 0  |
| 253              | 63        | 62                    | 1                 | 1                     | 0        | 1  | 1  | 1  | 1  | 1  | 1        | 0  |
| 254              | 63        | 62                    | 2                 | 2                     | 0        | 1  | 1  | 1  | 1  | 1  | 0        | 1  |
| 255              | 63        | 62                    | 3                 | 3                     | 0        | 1  | 1  | 1  | 1  | 1  | 1        | 1  |
| 256              | 64        | 63                    | 0                 | 0                     | 1        | 1  | 1  | 1  | 1  | 1  | 0        | 0  |
| 257              | 64        | 63                    | 1                 | 1                     | 1        | 1  | 1  | 1  | 1  | 1  | 1        | 0  |
| 258              | 64        | 63                    | 2                 | 2                     | 1        | 1  | 1  | 1  | 1  | 1  | 0        | 1  |
| 259              | 64        | 63                    | 3                 | 3                     | 1        | 1  | 1  | 1  | 1  | 1  | 1        | 1  |

N = INT (n/P)  
S = MOD (n/P)  
Where: n = Desired division ratio  
P = Prescaler value = 4  
N = Counter N value (counter decimal set is N - 1)

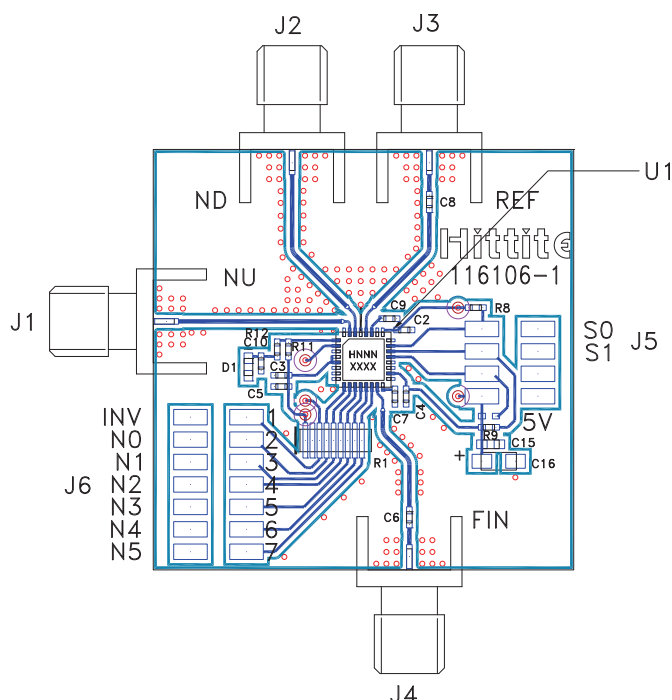
**HMC698LP5(E) Programming Truth Table, Non-Continuous Division Ratios**

| Division Ratio n | N Counter | N Counter Decimal Set | Swallow S Counter | Swallow S Decimal Set | (LSB) N0 | N1 | N2 | N3 | N4 | N5 | (LSB) S0 | S1 |
|------------------|-----------|-----------------------|-------------------|-----------------------|----------|----|----|----|----|----|----------|----|
| 8                | 2         | 1                     | 0                 | 0                     | 1        | 0  | 0  | 0  | 0  | 0  | 0        | 0  |
| 9                | 2         | 1                     | 1                 | 1                     | 1        | 0  | 0  | 0  | 0  | 0  | 1        | 0  |
| 10               | 2         | 1                     | 2                 | 2                     | 1        | 0  | 0  | 0  | 0  | 0  | 0        | 1  |

N = INT (n/P)  
S = MOD (n/P)  
Where: n = Desired division ratio  
P = Prescaler value = 4  
N = Counter N value (counter decimal set is N - 1)


**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**
**Evaluation PCB Circuit**


**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**

**Evaluation PCB**


The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

**List of Materials for  
Evaluation PCB 122625 <sup>[1]</sup>**

| Item               | Description                           |
|--------------------|---------------------------------------|
| J1 - J4            | PC Mount SMA RF Connector             |
| J5 - J6            | 2mm DC Header                         |
| C1 - C5, C8 - C10  | 1000 pF Capacitor, 0402 Pkg           |
| C6 - C7            | 100 pF Capacitor, 0402 Pkg            |
| C15                | 1000 pF Capacitor, 0603 Pkg           |
| C16                | 4.7 $\mu$ F Tantalum Capacitor Case A |
| D                  | LED Green, 0603 Pkg                   |
| R1                 | 10k Ohm, Resistor, Array              |
| R8, R9             | 10k Ohm, Resistor, 0402 Pkg.          |
| R11                | 1k Ohm, Resistor, 0402 Pkg.           |
| R12                | 100 Ohm, Resistor, 0402 Pkg.          |
| U1                 | HMC698LP5(E) Synthesizer              |
| PCB <sup>[2]</sup> | 116106 Eval Board                     |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

**Evaluation PCB Truth Table  
(see Programming Truth Table)**

Note: 0 = Jumper Installed.  
1 = Jumper Not Installed.

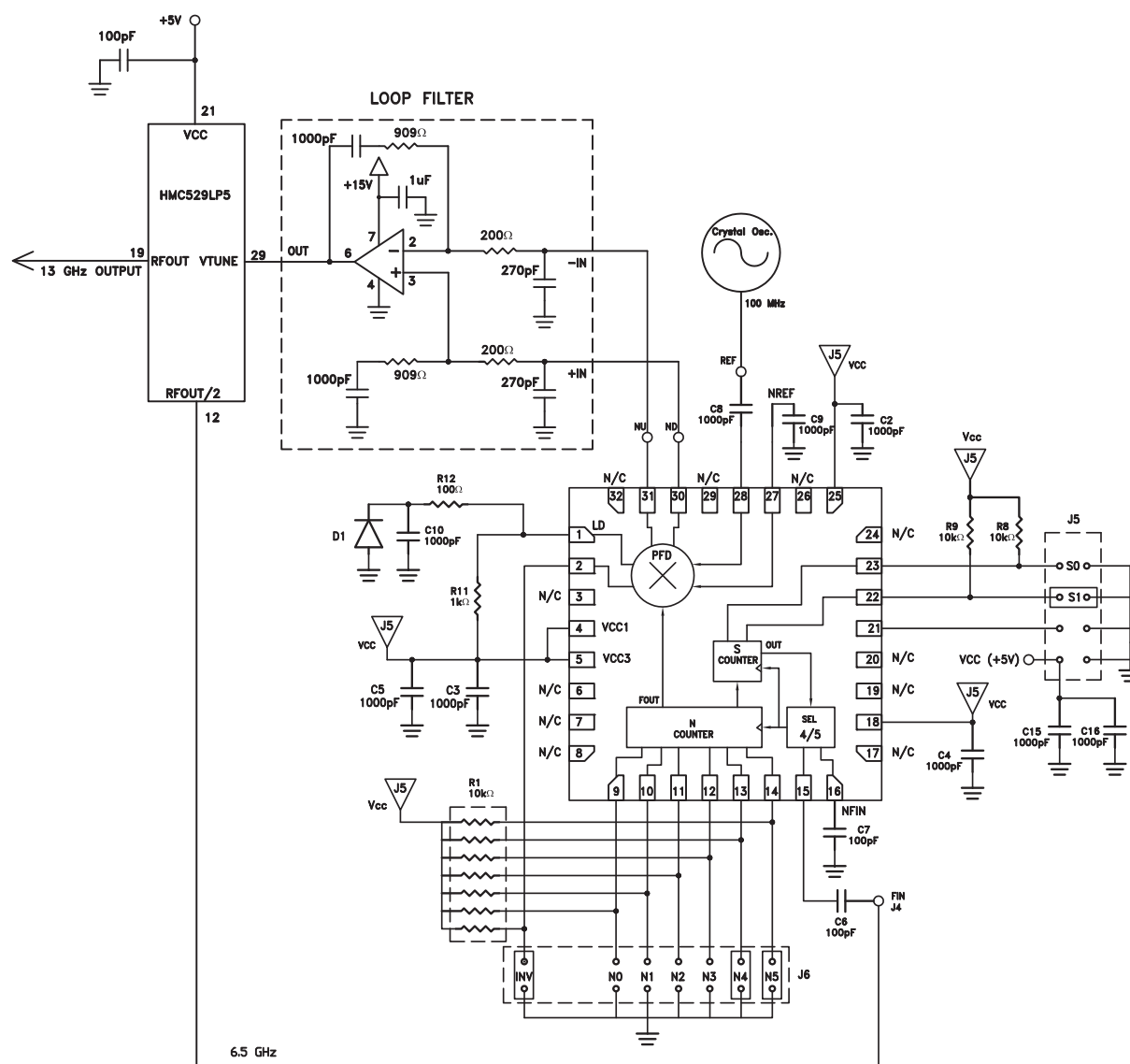
Note: The evaluation PCB for the HMC698LP5 contains 10K Ohm pull up resistors for each of the 9 control inputs. Programming the 251 distinct division ratios consists of installing or removing jumpers N0 through N5 and S0, S1.

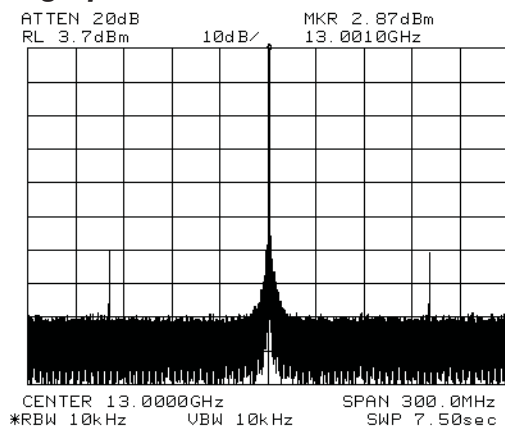
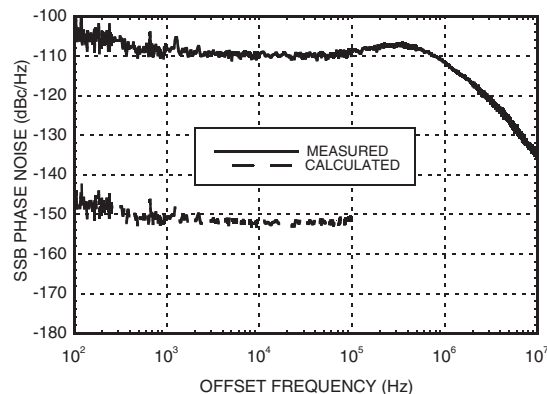


## 7 GHz INTEGER N SYNTHESIZER (N = 12 - 259)

### Typical PLL Application Circuit using HMC698LP5

PLL application shown for a 13.0 GHz Fout. Contact HMC to discuss your specific application.




**7 GHz INTEGER N SYNTHESIZER  
(N = 12 - 259)**
**Typical Application  
Showing Spurious Performance**

**Typical Application  
13 GHz Measured Phase Noise <sup>[1]</sup>**


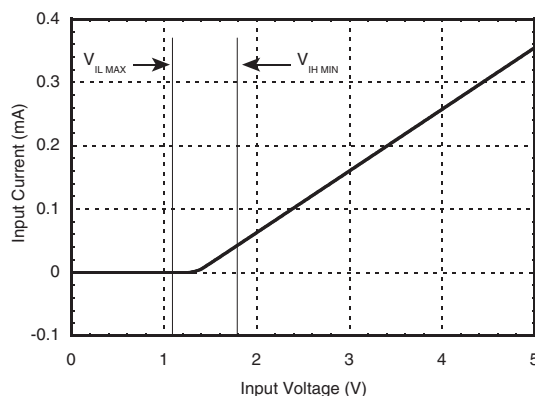
[1] Phase Noise Floor remains constant beyond 100 kHz offset frequency. Measured phase noise using Agilent 5500 with 2 unit measurement technique and corresponding calculated phase noise floor.

**CMOS/TTL Input Characteristics**

Maximum Input Logic "0" Voltage ( $V_{IL\ MAXIMUM}$ ) = 1.1V @ 1  $\mu$ A.

Minimum Input Logic "1" Voltage ( $V_{IH\ MINIMUM}$ ) = 1.8V @ 50  $\mu$ A.

Input IV characteristics for the logic inputs (N0 - N5, S0 - S1) are shown below:



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[HMC698LP5E](#) [122625-HMC698LP5](#) [HMC698LP5](#) [HMC698LP5ETR](#) [HMC698LP5TR](#)