Low Noise Amplifier, 0.01 GHz to 10 GHz

Data Sheet

HMC8411LP2FE

FEATURES

Low noise figure: 1.7 dB typical
Single positive supply (self biased)
High gain: 15.5 dB typical
High OIP3: 34 dBm typical
6-lead, 2 mm × 2 mm LFCSP

APPLICATIONS

Test instrumentation
Military communications

FUNCTIONAL BLOCK DIAGRAM

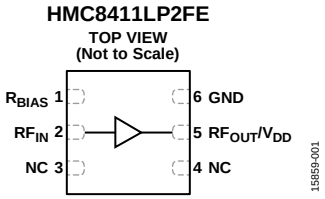

Figure 1.

GENERAL DESCRIPTION

The HMC8411LP2FE is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 0.01 GHz to 10 GHz.

The HMC8411LP2FE provides a typical gain of 15.5 dB, a 1.7 dB typical noise figure, and a typical output third-order intercept (OIP3) of 34 dBm, requiring only 55 mA from a 5 V supply voltage. The saturated output power (P_{SAT}) of 19.5 dBm typical enables the low noise amplifier (LNA) to function as a local oscillator (LO) driver for many of Analog Devices, Inc., balanced, in-phase/quadrature (I/Q), or image rejection mixers.

The HMC8411LP2FE also features inputs and outputs that are internally matched to 50 Ω, making the device ideal for surface-mounted technology (SMT)-based, high capacity microwave radio applications.

The HMC8411LP2FE is housed in a RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP.

Multifunction pin names may be referenced by their relevant function only.

Rev. A **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

5/2019—Rev. 0 to Rev. A

Changes to Table 3 4
Changes to Theory of Operation Section 18

3/2019—Revision 0: Initial Version

SPECIFICATIONS

0.01 GHz TO 1 GHz FREQUENCY RANGE

V_{DD} = 5 V, supply current (I_{DQ}) = 55 mA, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		1	GHz	
GAIN		12.5	15.5		dB	
Gain Variation over Temperature			0.005		dB/°C	
NOISE FIGURE			1.8		dB	
RETURN LOSS						
Input			22		dB	
Output			17		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	17	20		dBm	
Saturated Output Power	P_{SAT}		20.5		dBm	
Output Third-Order Intercept	OIP3		33.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 6 dBm
Output Second-Order Intercept	OIP2		43		dBm	Measurement taken at P_{OUT} per tone one = 6 dBm
POWER ADDED EFFICIENCY	PAE		30		%	Measured at P_{SAT}
SUPPLY CURRENT	I_{DQ}		55		mA	
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

1 GHz TO 6 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 55 mA, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		1		6	GHz	
GAIN		12	15		dB	
Gain Variation over Temperature			0.01		dB/°C	
NOISE FIGURE			1.7		dB	
RETURN LOSS						
Input			25		dB	
Output			18		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	17	20		dBm	
Saturated Output Power	P_{SAT}		21		dBm	
Output Third-Order Intercept	OIP3		34		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
Output Second-Order Intercept	OIP2		39		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
POWER ADDED EFFICIENCY	PAE		34		%	Measured at P_{SAT}
SUPPLY CURRENT	I_{DQ}		55		mA	
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

6 GHz TO 10 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 55 mA, and T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		6		10	GHz	
GAIN		11	14		dB	
Gain Variation over Temperature			0.018		dB/°C	
NOISE FIGURE			2		dB	
RETURN LOSS						
Input			15		dB	
Output			17		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	13	16		dBm	
Saturated Output Power	P_{SAT}		19.5		dBm	
Output Third-Order Intercept	OIP3		33		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
Output Second-Order Intercept	OIP2		40		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
POWER ADDED EFFICIENCY	PAE		23		%	Measured at P_{SAT}
SUPPLY CURRENT	I_{DQ}		55		mA	
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
Drain Bias Voltage (V_{DD})	7 V
Radio Frequency Input (RF_{IN}) Power	20 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 12.2 mW/°C Above 85°C)	1.098 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Peak Reflow Temperature Moisture Sensitivity Level 1 (MSL1)[2]	260°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	500 V, Class 1B passed

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] See the Ordering Guide section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-6-12	82	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

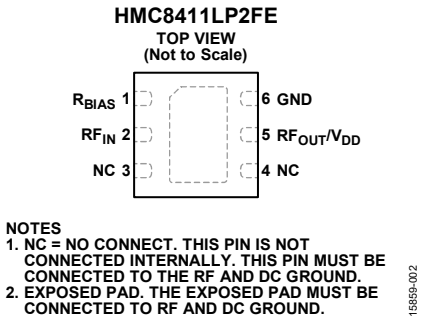

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{BIAS}	Current Mirror Bias Resistor Pin. Use this pin to set the current to the internal resistor by the external resistor. See Figure 3 for the interface schematic.
2	RF_{IN}	RF Input (RF_{IN}). This pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
3, 4	NC	No Connect. This pin is not connected internally. This pin must be connected to the RF and dc ground.
5	RF_{OUT}/V_{DD}	RF Output (RF_{OUT}). This pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic. Drain Bias for the Amplifier (V_{DD}). This pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
6	GND	Ground. This pin must be connected to the RF and dc ground. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

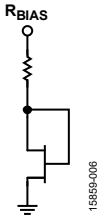

Figure 3. R_{BIAS} Interface Schematic

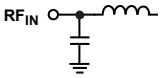

Figure 4. RF_{IN} Interface Schematic

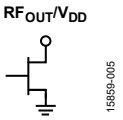

Figure 5. RF_{OUT}/V_{DD} Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

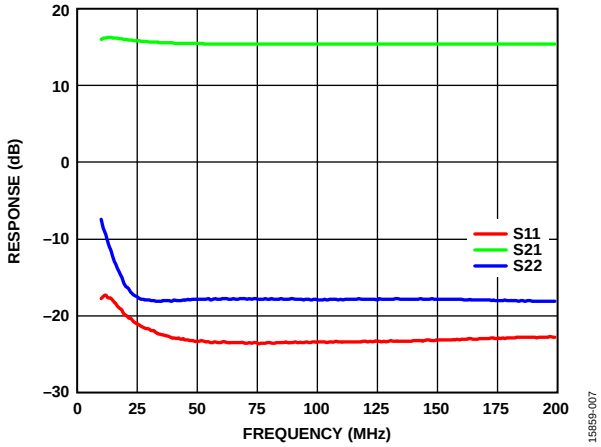

Figure 7. Gain and Return Loss (Response) vs. Frequency, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 55 mA

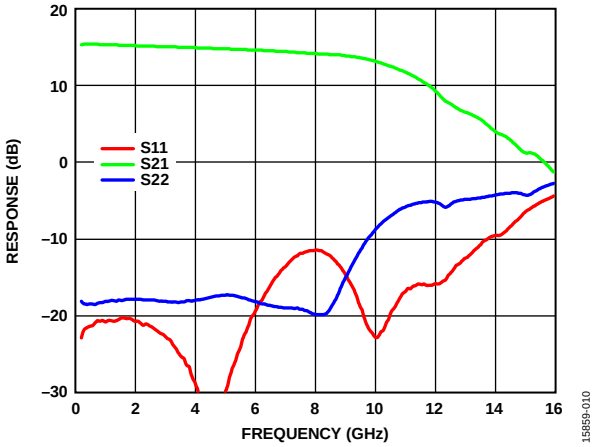

Figure 10. Broadband Gain and Return Loss (Response) vs. Frequency, 200 MHz to 16 GHz, V_{DD} = 5 V, I_{DQ} = 55 mA

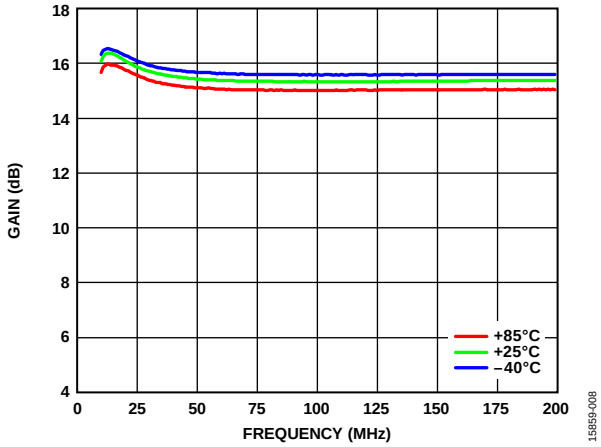

Figure 8. Gain vs. Frequency, 10 MHz to 200 MHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

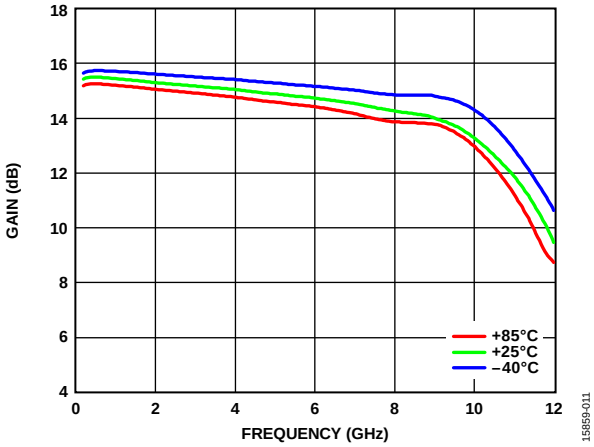

Figure 11. Gain vs. Frequency, 200 MHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

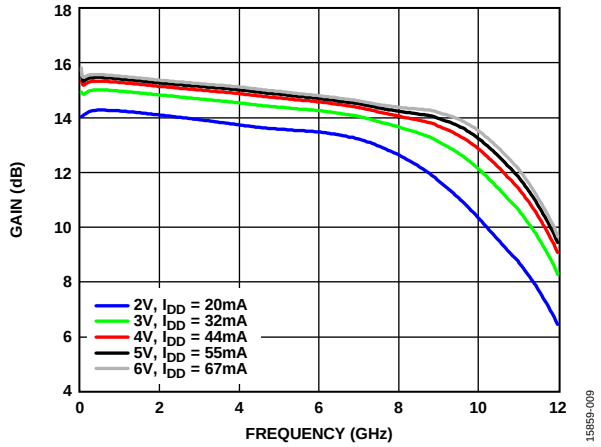

Figure 9. Gain vs. Frequency for Various Supply Voltages and Currents (I_{DD}), R_{BIAS} = 1.1 kΩ

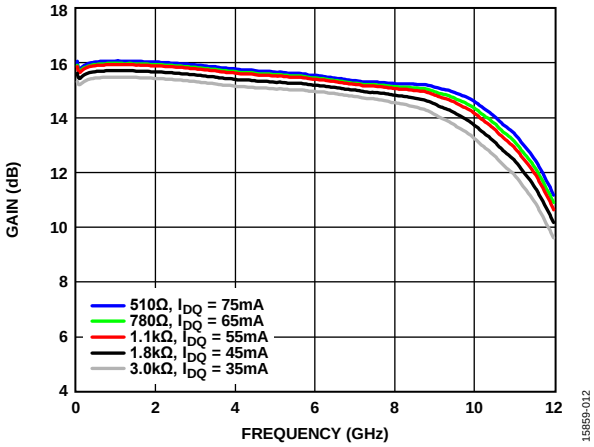

Figure 12. Gain vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

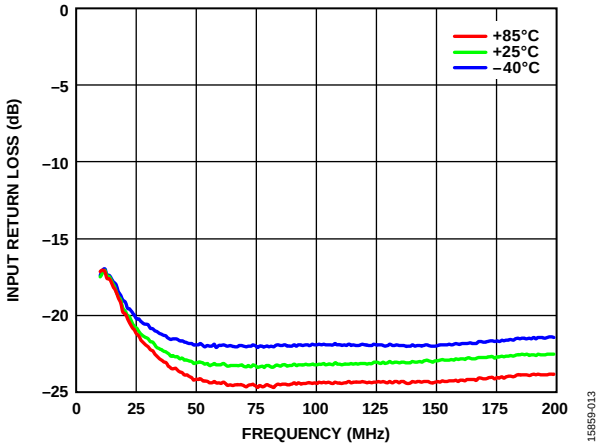

Figure 13. Input Return Loss vs. Frequency, 10 MHz to 200 MHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

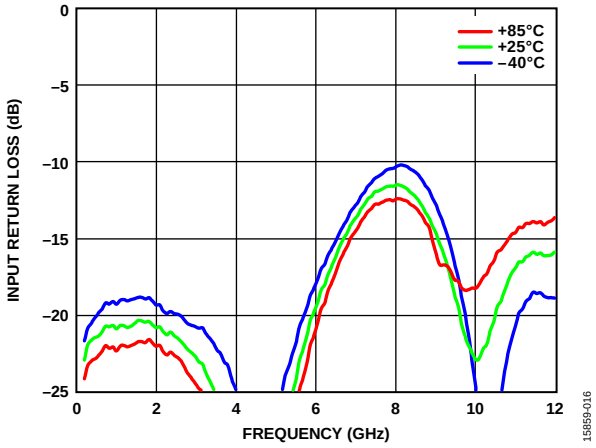

Figure 16. Input Return Loss vs. Frequency, 200 MHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

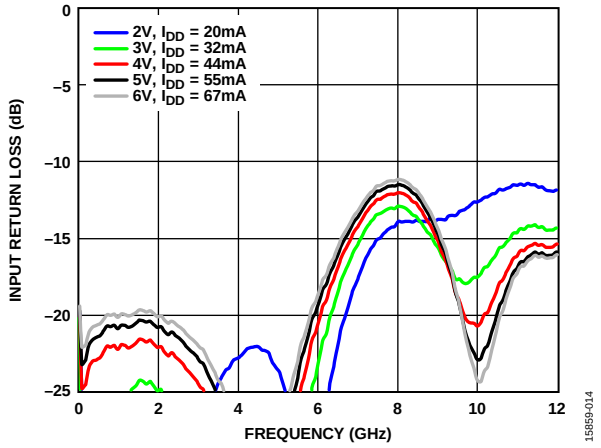

Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

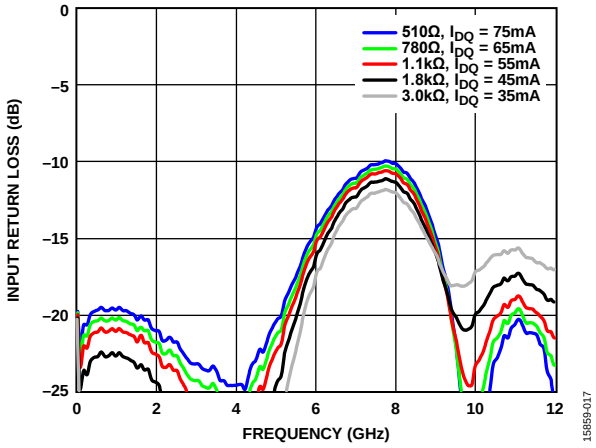

Figure 17. Input Return Loss vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

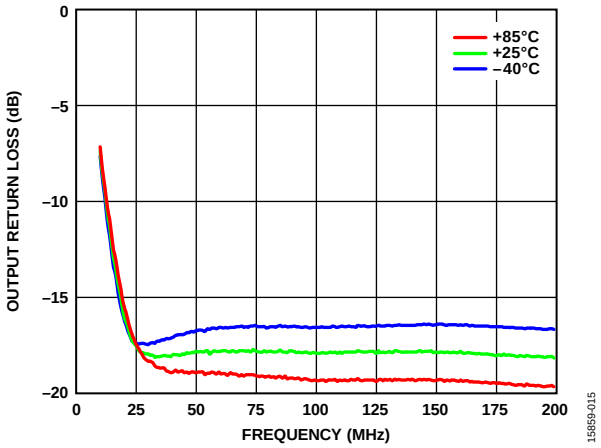

Figure 15. Output Return Loss vs. Frequency, 10 MHz to 200 MHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

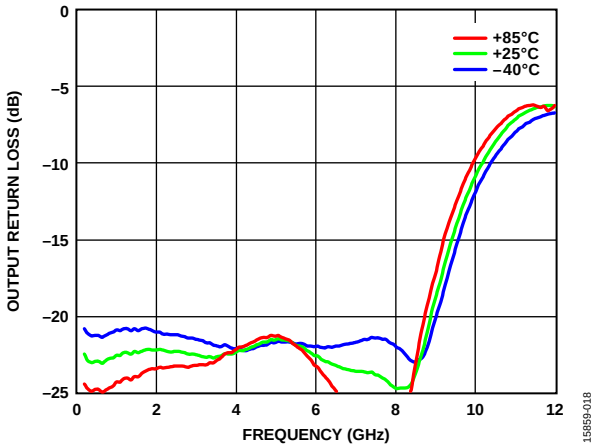

Figure 18. Output Return Loss vs. Frequency, 200 MHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

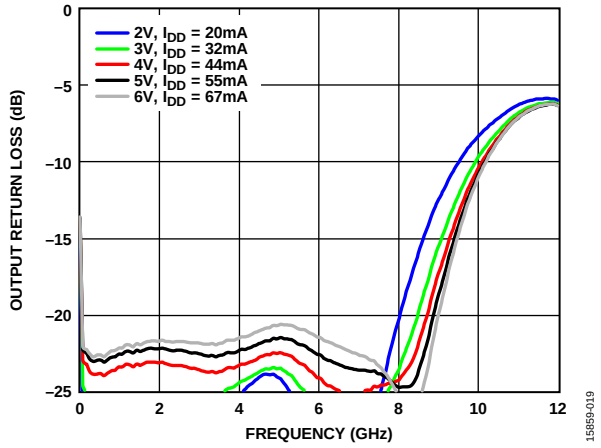

Figure 19. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

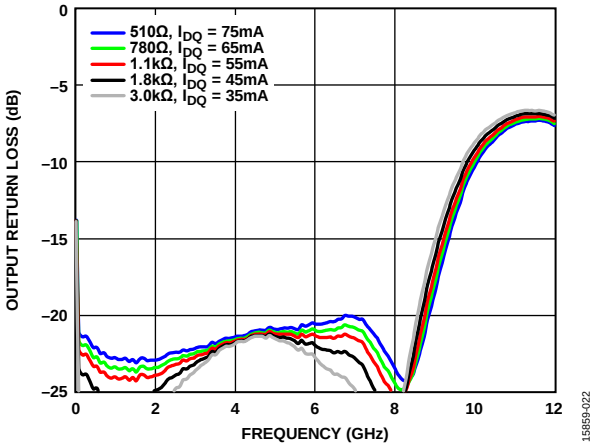

Figure 22. Output Return Loss vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

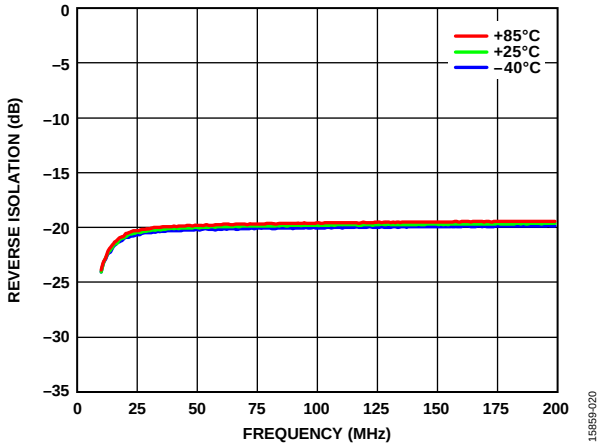

Figure 20. Reverse Isolation vs. Frequency, 10 MHz to 200 MHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

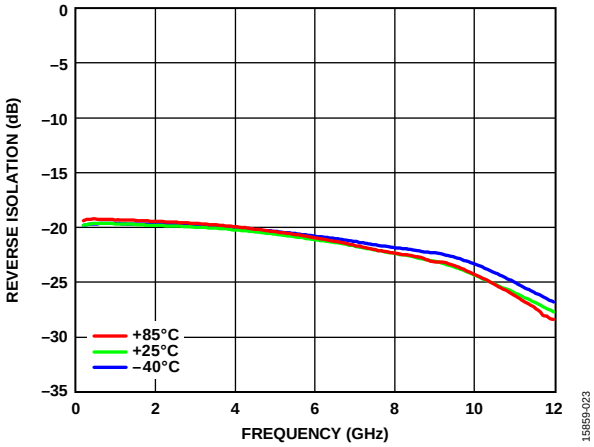

Figure 23. Reverse Isolation vs. Frequency, 200 MHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

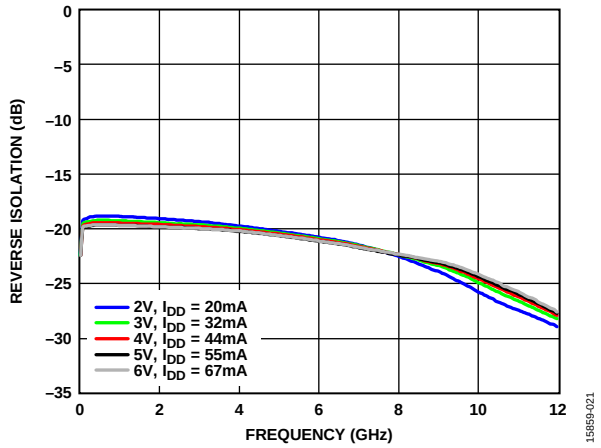

Figure 21. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

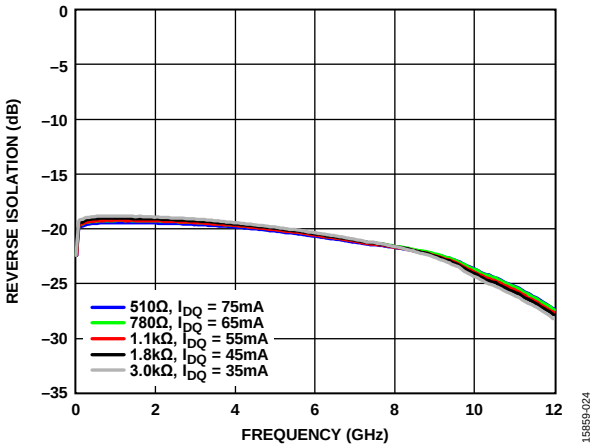

Figure 24. Reverse Isolation vs. Frequency for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

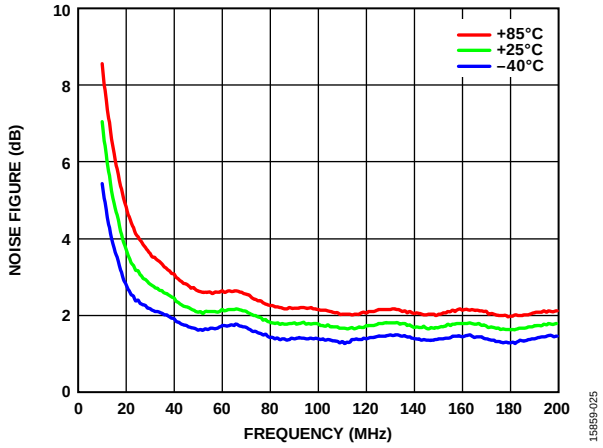

Figure 25. Noise Figure vs. Frequency, 10 MHz to 200 MHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

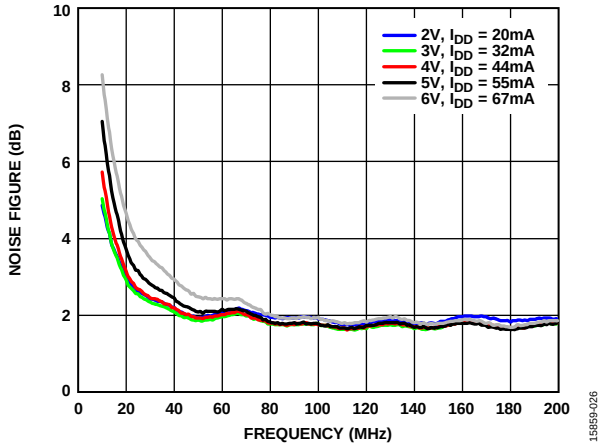

Figure 26. Noise Figure vs. Frequency, 10 MHz to 200 MHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

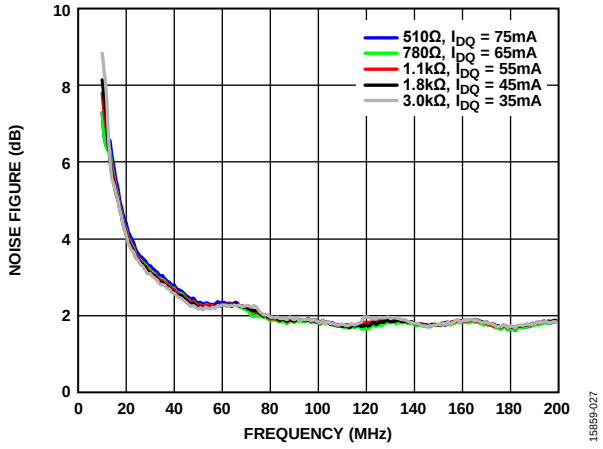

Figure 27. Noise Figure vs. Frequency, 10 MHz to 200 MHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

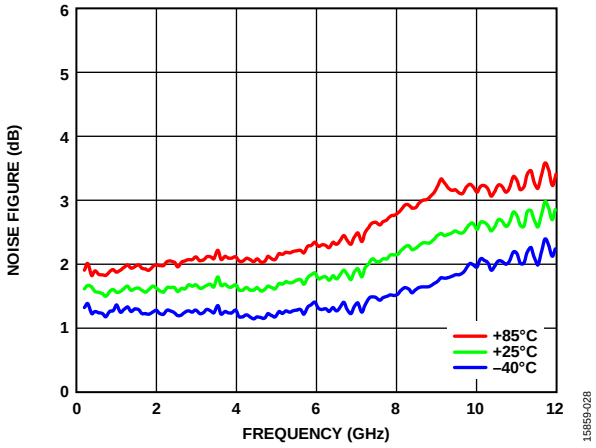

Figure 28. Noise Figure vs. Frequency, 200 MHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

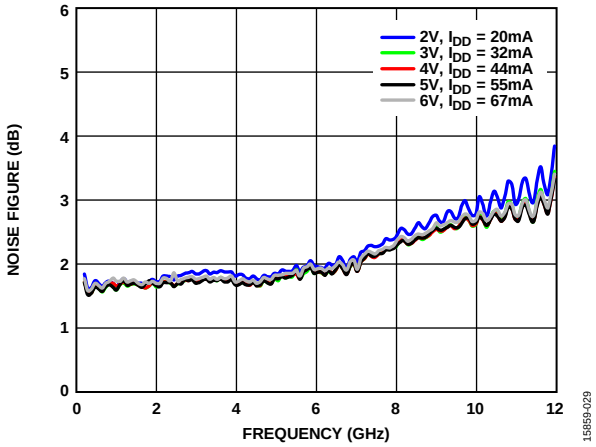

Figure 29. Noise Figure vs. Frequency, 200 MHz to 12 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

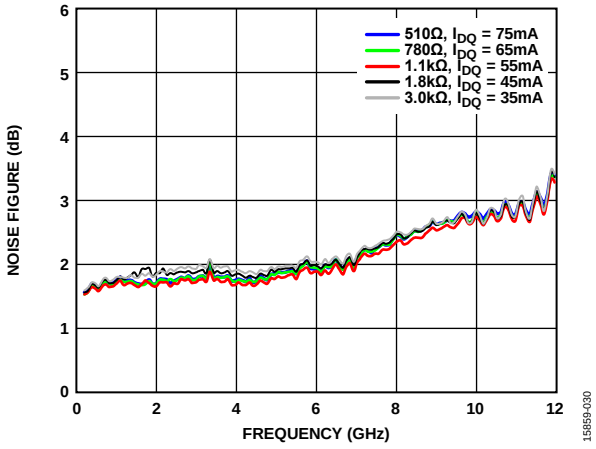

Figure 30. Noise Figure vs. Frequency, 200 MHz to 12 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

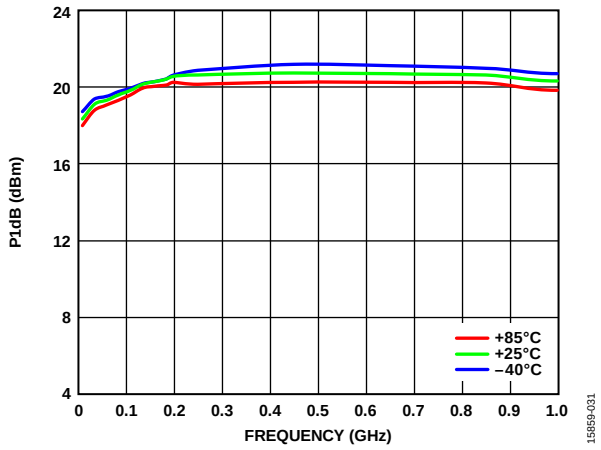

Figure 31. P1dB vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

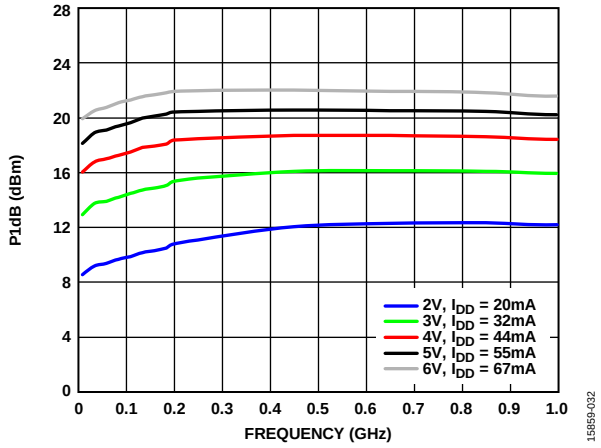

Figure 32. P1dB vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

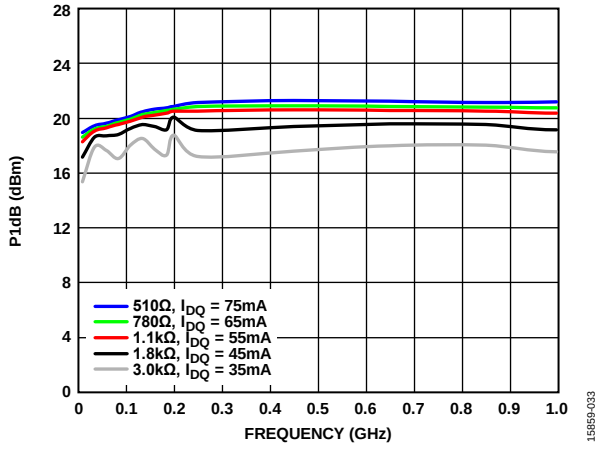

Figure 33. P1dB vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

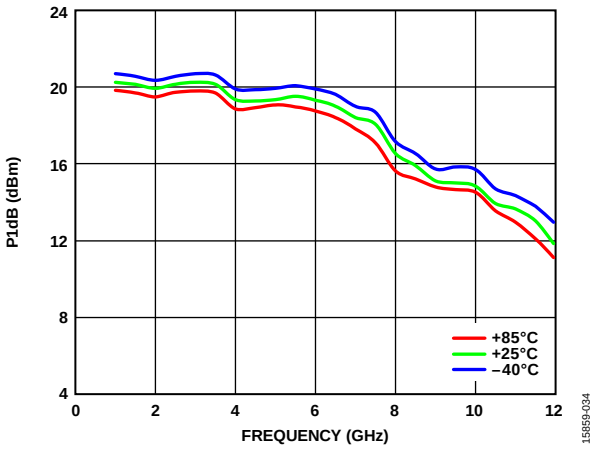

Figure 34. P1dB vs. Frequency, 1 GHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

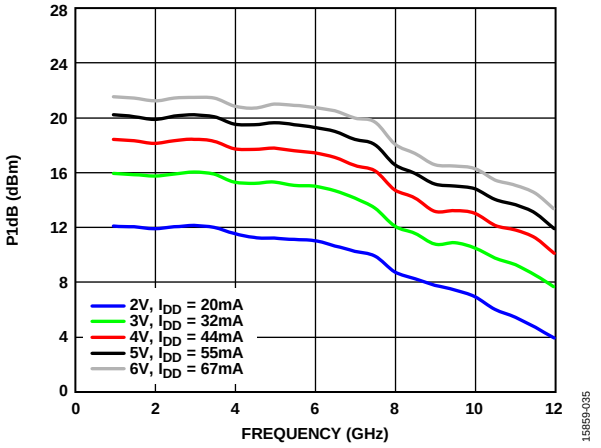

Figure 35. P1dB vs. Frequency, 1 GHz to 12 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

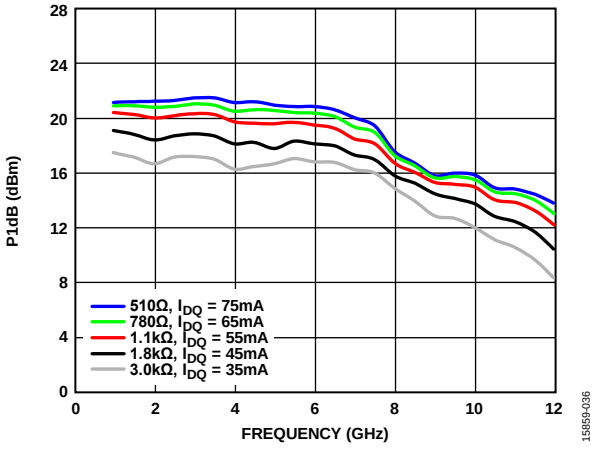

Figure 36. P1dB vs. Frequency, 1 GHz to 12 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

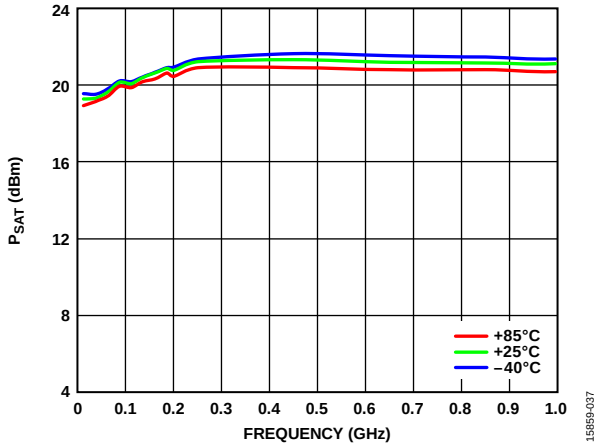

Figure 37. P_{SAT} vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

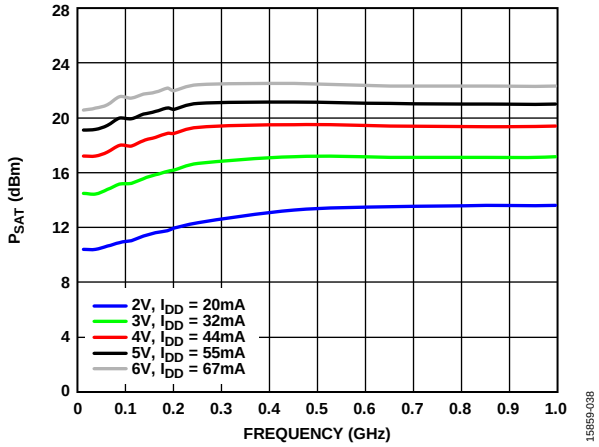

Figure 38. P_{SAT} vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

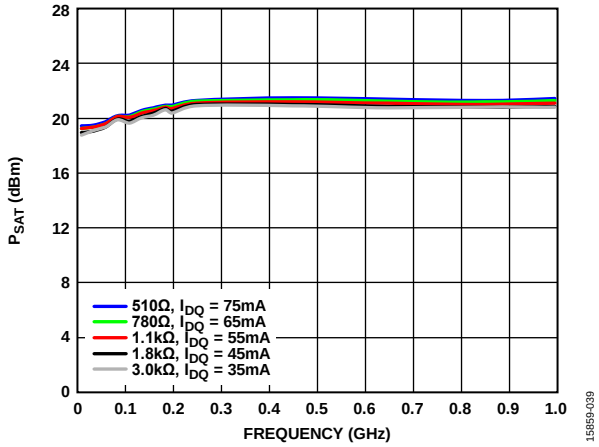

Figure 39. P_{SAT} vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

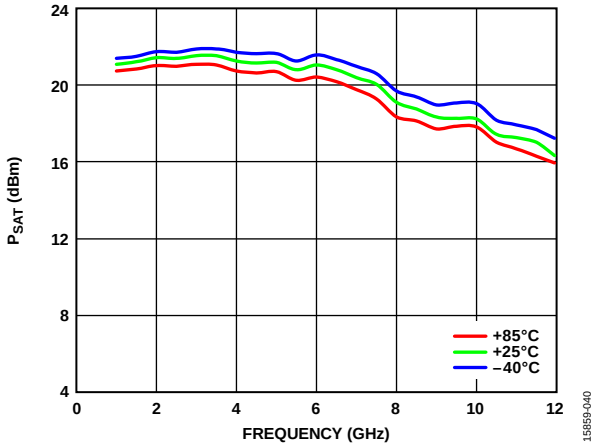

Figure 40. P_{SAT} vs. Frequency, 1 GHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

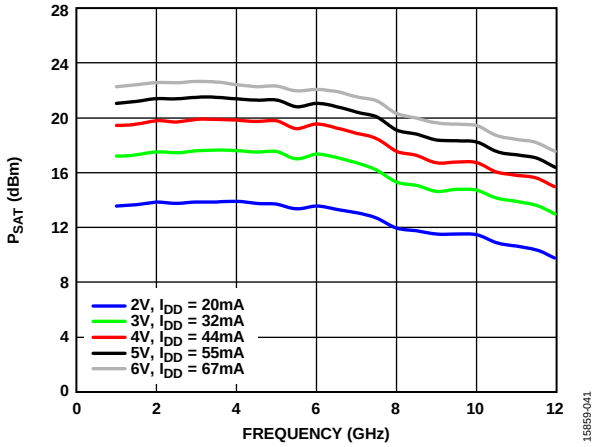

Figure 41. P_{SAT} vs. Frequency, 1 GHz to 12 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

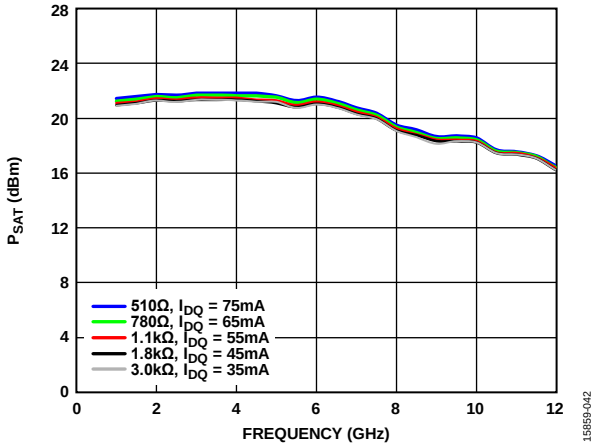

Figure 42. P_{SAT} vs. Frequency, 1 GHz to 12 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

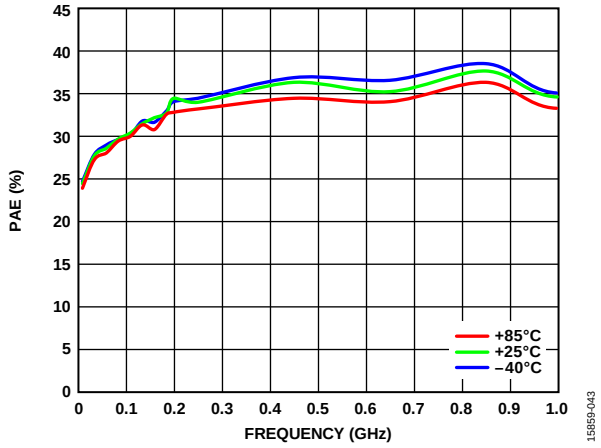

Figure 43. PAE vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

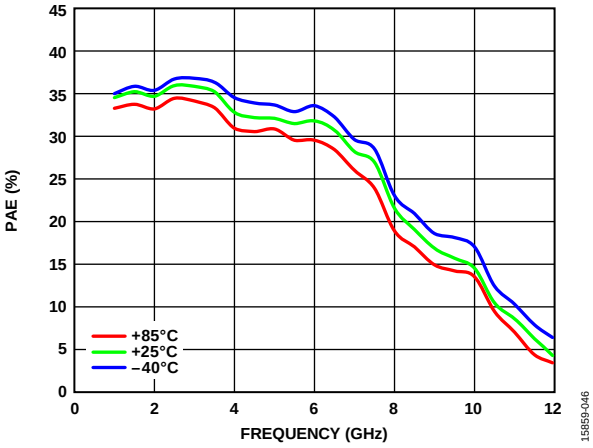

Figure 46. PAE vs. Frequency, 1 GHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

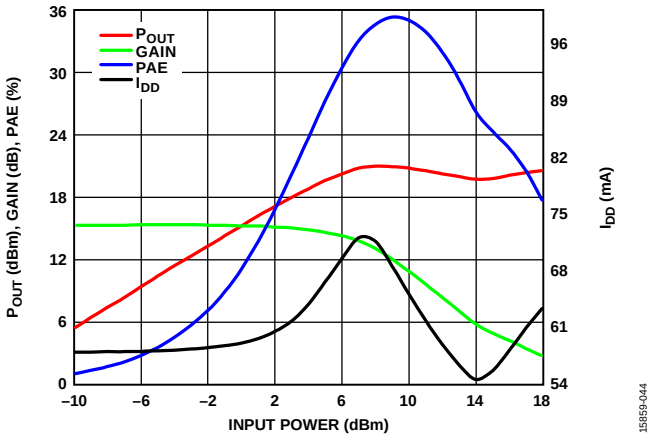

Figure 44. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 1 GHz, V_{DD} = 5 V, I_{DQ} = 55 mA

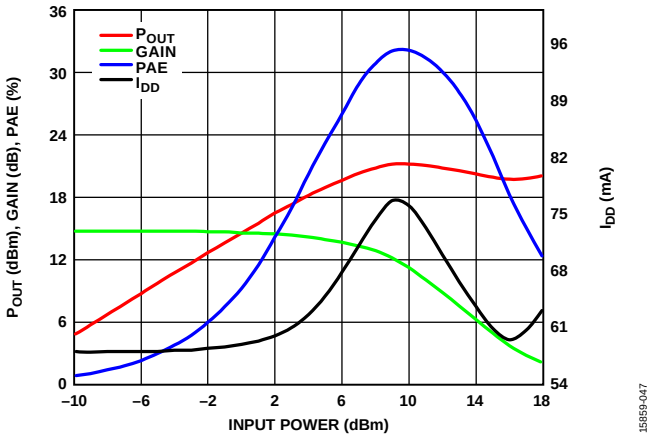

Figure 47. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 5 GHz, V_{DD} = 5 V, I_{DQ} = 55 mA

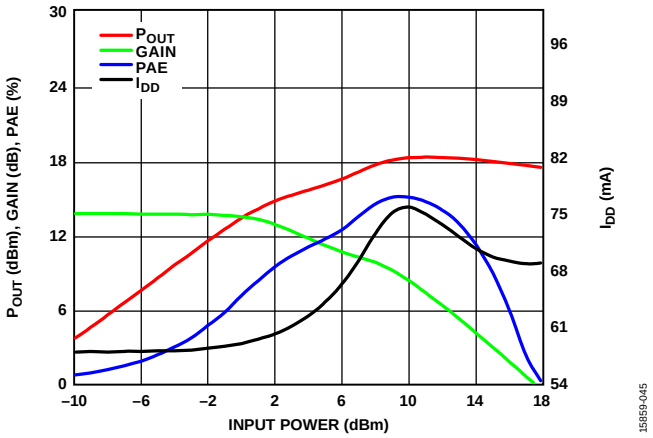

Figure 45. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 10 GHz, V_{DD} = 5 V, I_{DQ} = 55 mA

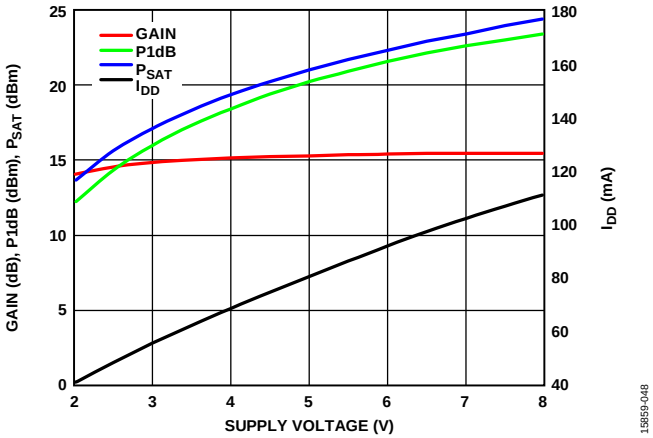

Figure 48. P_{OUT}, Gain, PAE, and I_{DD} vs. Supply Voltage, Power Compression at 1 GHz, R_{BIAS} = 1.1 kΩ

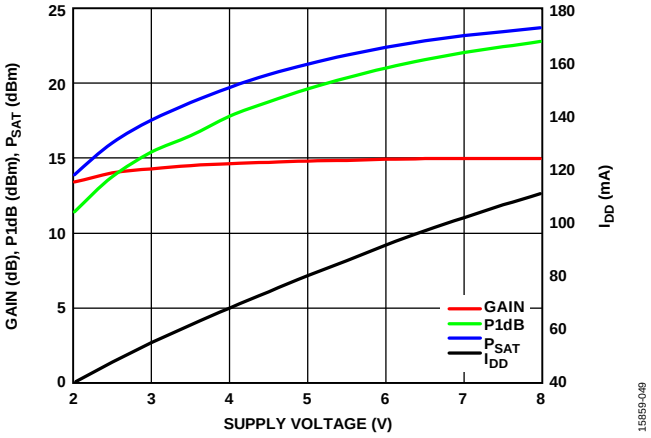

Figure 49. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 5 GHz, R_{BIAS} = 1.1 kΩ

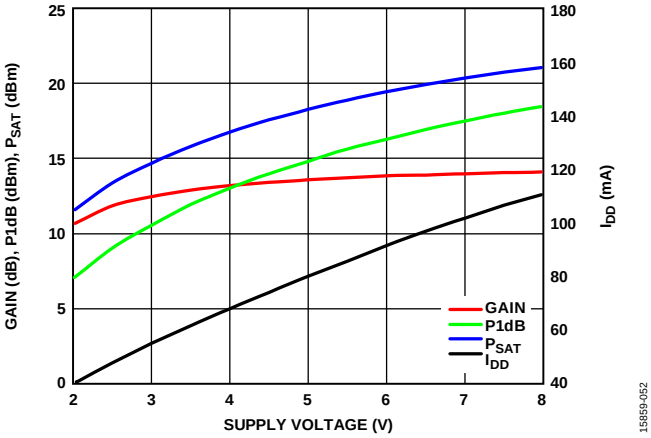

Figure 52. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Power Compression at 10 GHz, R_{BIAS} = 1.1 kΩ

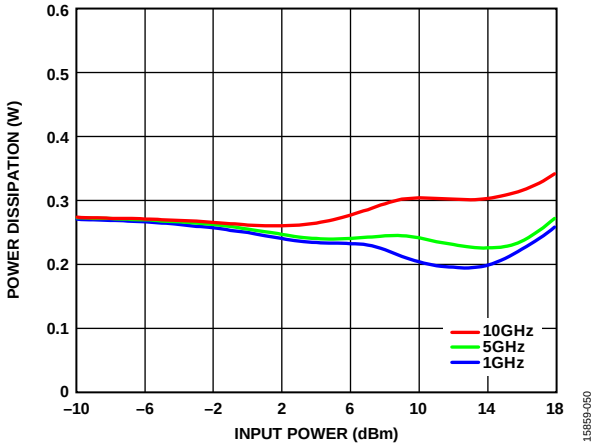

Figure 50. Power Dissipation vs. Input Power at T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 55 mA

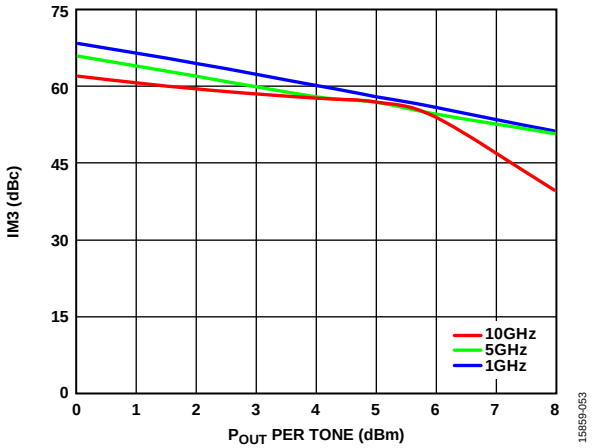

Figure 53. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 55 mA

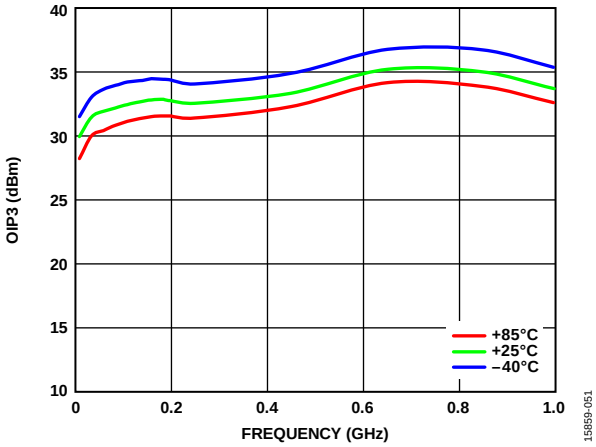

Figure 51. OIP3 vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

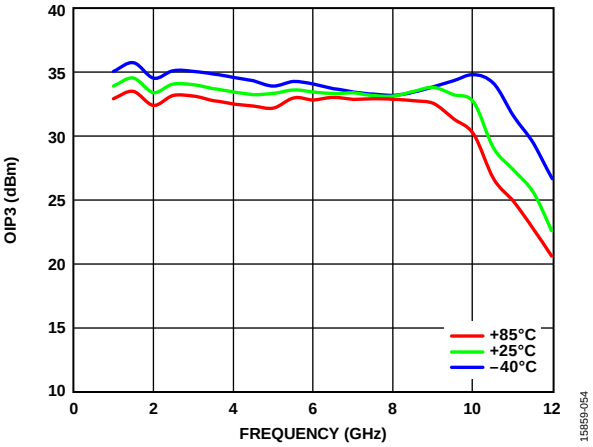

Figure 54. OIP3 vs. Frequency, 1 GHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

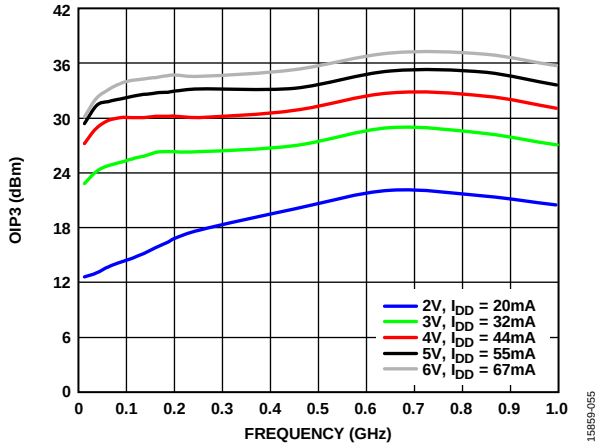

Figure 55. OIP3 vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

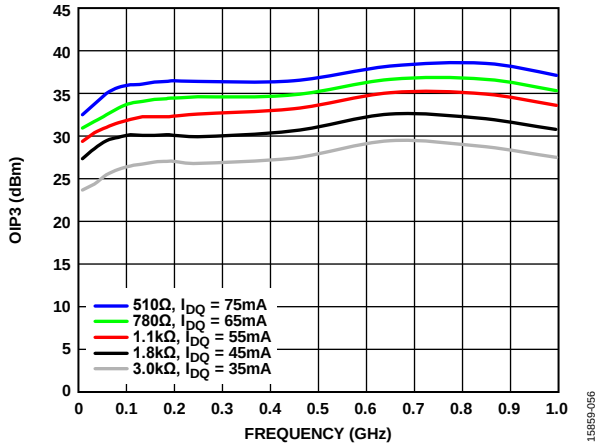

Figure 56. OIP3 vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

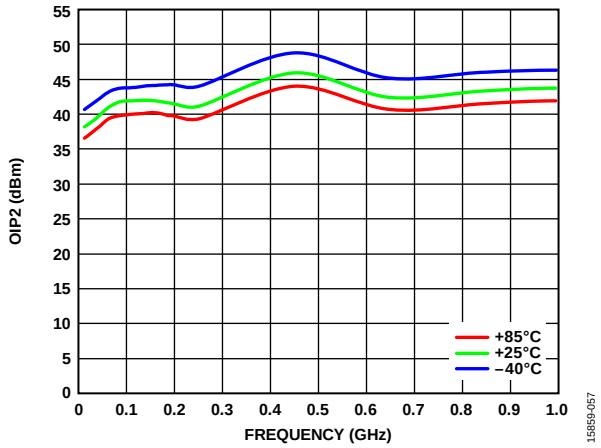

Figure 57. OIP2 vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

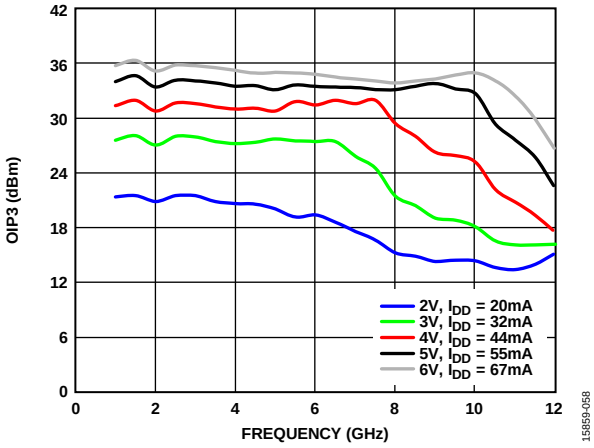

Figure 58. OIP3 vs. Frequency, 1 GHz to 12 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

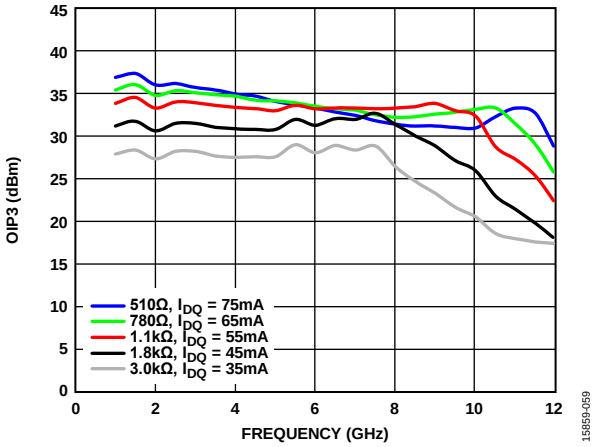

Figure 59. OIP3 vs. Frequency, 1 GHz to 12 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

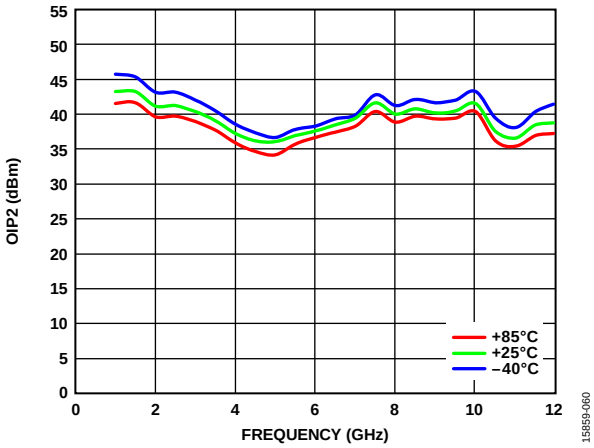

Figure 60. OIP2 vs. Frequency, 1 GHz to 12 GHz, for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 55 mA

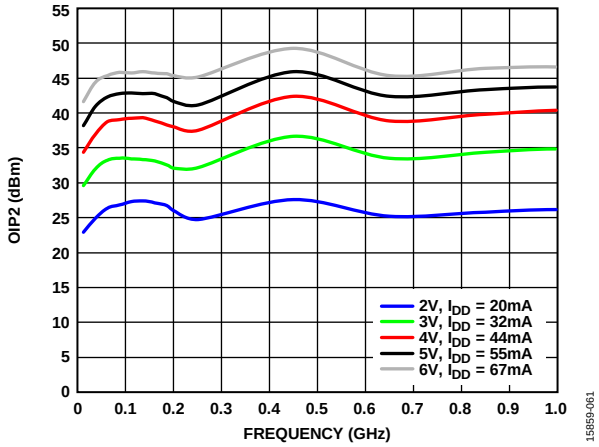

Figure 61. OIP2 vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

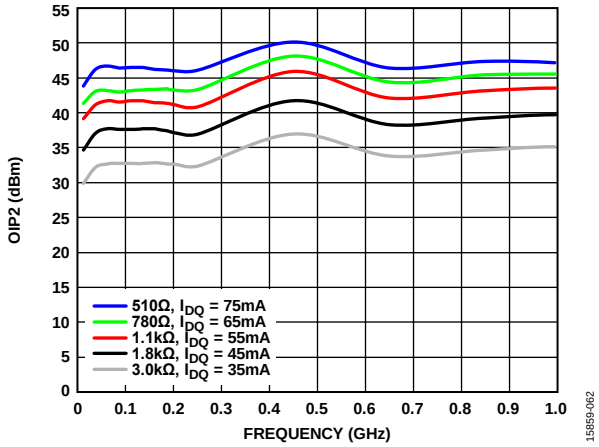

Figure 62. OIP2 vs. Frequency, 0.01 GHz to 1.0 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

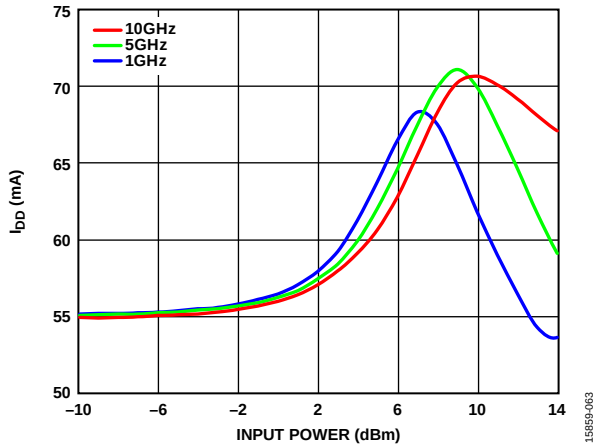

Figure 63. I_{DD} vs. Input Power for Various Frequencies, V_{DD} = 5 V

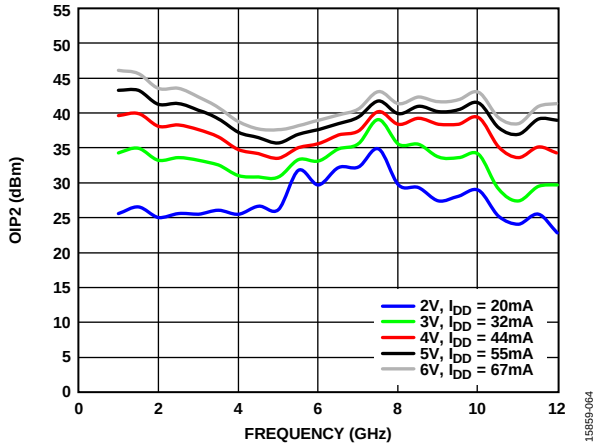

Figure 64. OIP2 vs. Frequency, 1 GHz to 12 GHz, for Various Supply Voltages and I_{DD}, R_{BIAS} = 1.1 kΩ

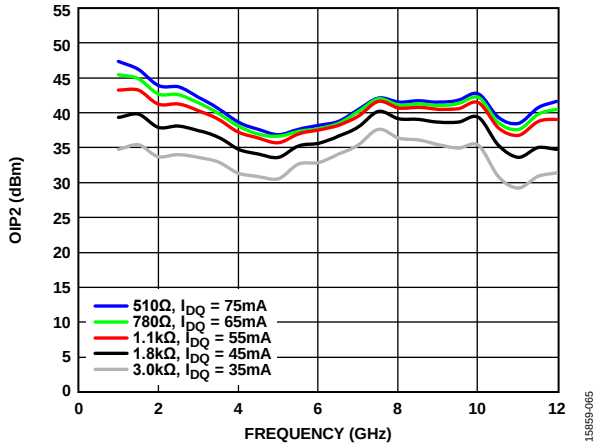

Figure 65. OIP2 vs. Frequency, 1 GHz to 12 GHz, for Various Bias Resistor Values and I_{DQ}, V_{DD} = 5 V

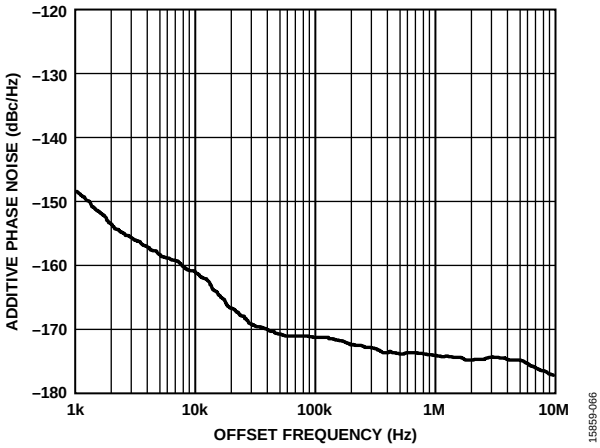

Figure 66. Additive Phase Noise vs. Offset Frequency, RF Frequency = 6 GHz, RF Input Power = 0 dBm

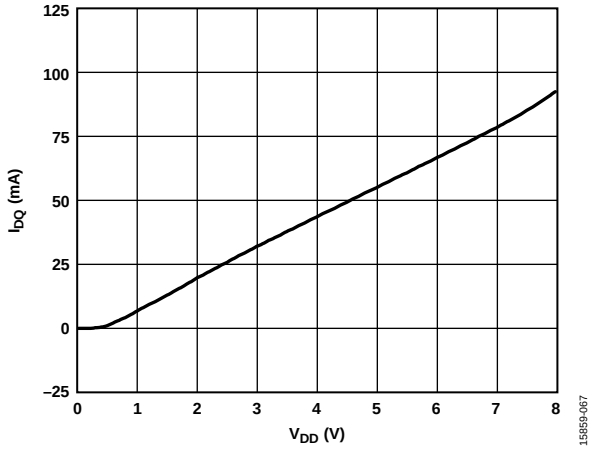

Figure 67. I_{DQ} vs. V_{DD}, Representative of a Typical Device, R_{BIAS} = 1.1 kΩ

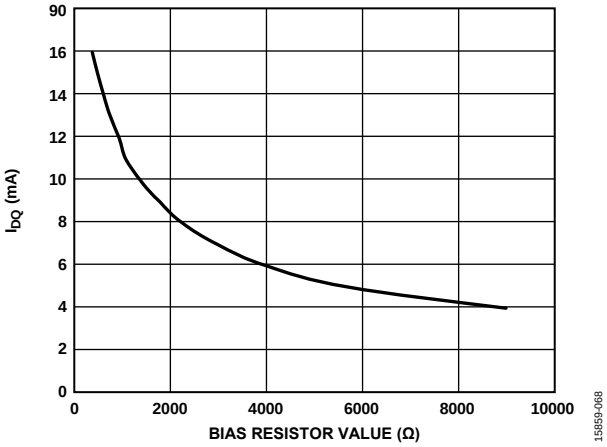

Figure 68. I_{DQ} vs. Bias Resistor Value, V_{DD} = 5 V

THEORY OF OPERATION

The HMC8411LP2FE is a GaAs, MMIC, pHEMT, low noise wideband amplifier.

The HMC8411LP2FE is a cascode amplifier that uses a fundamental cell of two field effect transistors (FETs) in series, source to drain. The basic schematic for the cascode cell is shown in Figure 69, which forms a low noise amplifier operating from 0.01 GHz to 10 GHz with excellent noise figure performance.

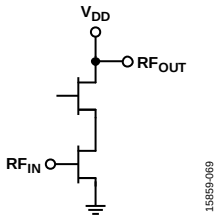

Figure 69. GaAs, MMIC, pHEMT, Low Noise Wideband Amplifier Schematic

The HMC8411LP2FE has single-ended input and output ports with impedances that nominally equal 50 Ω over the 0.01 GHz to 10 GHz frequency range. As a result, the device can be directly inserted into a 50 Ω system with external components on the RF input and output, as shown in Figure 70, without narrow-banded matching solutions. There is a need for an external bias choke for V_{DD} on the RF_{OUT} pin followed by a dc blocking capacitor, as well as a dc blocking capacitor on the RF_{IN} port. On the RF input, there is an additional resistor, inductor, and capacitor (RLC) shunt network that aids unconditional stability below 100 MHz.

The HMC8411LP2FE is a single-supply bias amplifier using an external resistor on the R_{BIAS} pin to set the I_{DQ} current. To adjust the I_{DQ} current, change the R_{BIAS} resistor value.

APPLICATIONS INFORMATION

The basic connections for operating the HMC8411LP2FE are shown in Figure 70. AC couple the input and output of the HMC8411LP2FE with appropriately sized capacitors. DC block capacitors are supplied on the RF_{IN} and RF_{OUT} pin of the evaluation board. A 5 V dc bias is supplied to the amplifier through the choke inductor connected to the RF_{OUT} pin.

The HMC8411LP2FE operates in self-bias mode when the R_{BIAS} pin is connected to a 1.1 kΩ external resistor to achieve a 55 mA supply current.

Refer to Table 7 for the recommended resistor values to achieve different supply currents.

RECOMMENDED BIAS SEQUENCING

During Power-Up

The recommended bias sequence during power-up follows:

1. Set V_{DD} to 5 V.
2. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down follows:

1. Turn off the RF signal.
2. Set V_{DD} to 0 V.

The bias conditions, V_{DD} = 5 V and I_{DQ} = 55 mA, are the recommended operating point to achieve optimum performance. The data used in this data sheet was taken with the recommended bias conditions. Using the HMC8411LP2FE with different bias conditions can provide different performance than what is shown in the Typical Performance Characteristics section.

Table 7. Recommended Bias Resistor Values

R_{BIAS} (Ω)	I_{DQ} (mA)	Amplifier Current, I_{DQ_AMP} (mA)	R_{BIAS} Current, I_{DQ_BIAS} (mA)
400	80	75.97	4.03
510	75	71.32	3.68
635	70	66.64	3.36
780	65	61.95	3.05
960	60	57.27	2.73
1100	55	52.47	2.53
1400	50	47.82	2.18
1800	45	43.16	1.84
2270	40	38.45	1.55
3000	35	33.75	1.25
4000	30	29.15	0.85
5700	25	24.93	0.07
9000	20	19.95	0.05

TYPICAL APPLICATION CIRCUIT

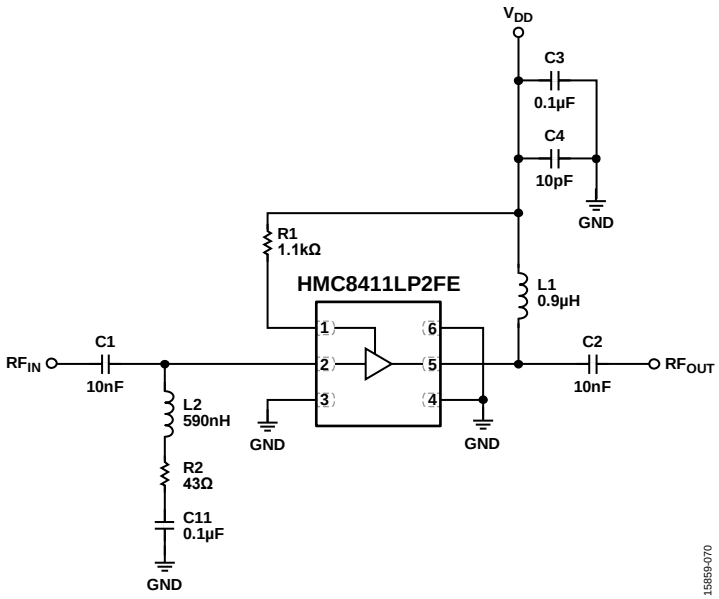

Figure 70. Typical Application Circuit

EVALUATION BOARD

The EV1HMC8411LP2F evaluation board is a 4-layer board fabricated using Rogers 4350 and using best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance.

The evaluation board and populated components operate over the −40°C to +85°C ambient temperature range. For proper bias sequence, see the Applications Information section.

The evaluation board schematic is shown in Figure 72. A fully populated and tested evaluation board (see Figure 71) is available from Analog Devices upon request.

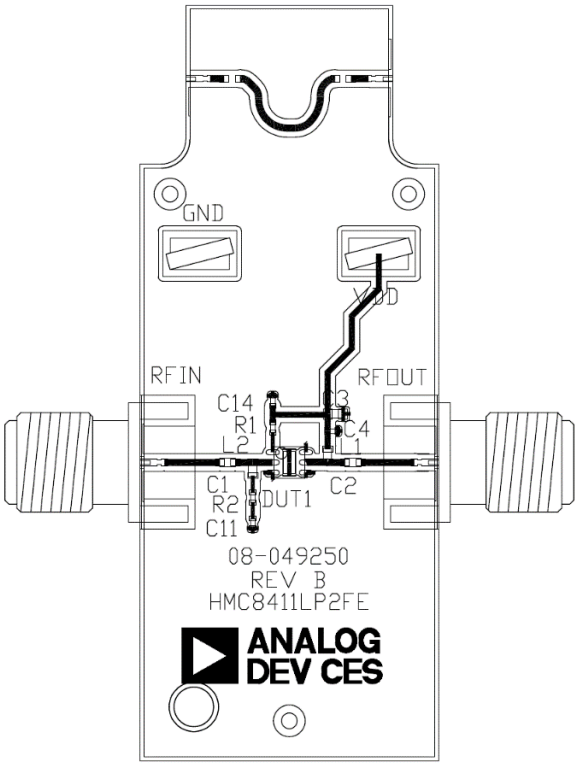

Figure 71. EV1HMC8411LP2F Printed Circuit Board (PCB)

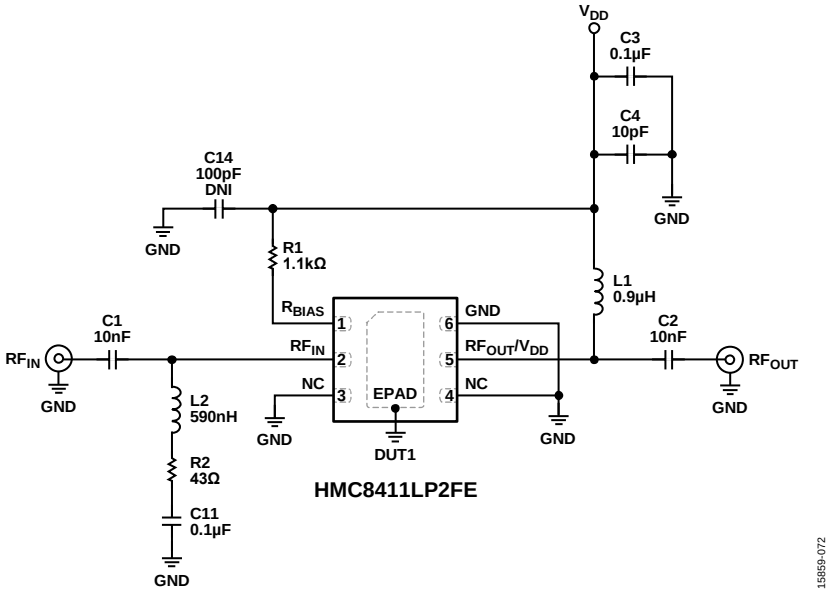

Figure 72. EV1HMC8411LP2F Evaluation Board Schematic

Table 8. Bill of Materials for Evaluation PCB EV1HMC8411LP2F

Item	Description
RF_{IN}, RF_{OUT}	PCB mount SMA RF connectors, SRI 21-146-1000-01
V_{DD}, GND	DC bias test points
C1, C2	10 nF broadband dc blocking capacitors, Presidio LBB0201X103MET5C8L
C3	Capacitor, 0.1 µF, 0402 package
C4	Capacitor, 10 pF, 0201 package
C11	Capacitor, 0.1 µF, 0201 package
L1	Inductor, 0.9 µH, 0402, 5% ferrite, Coilcraft 0402DF-901XJRW
L2	Inductor, 590 nH, 0402, 5% ferrite, Coilcraft 0402DF-591XJRU
R1	1.1 kΩ resistor, 0201 package
R2	43 Ω resistor, 0201 package
DUT1	IC, HMC8411LP2FE
Heat sink	Heat sink

OUTLINE DIMENSIONS

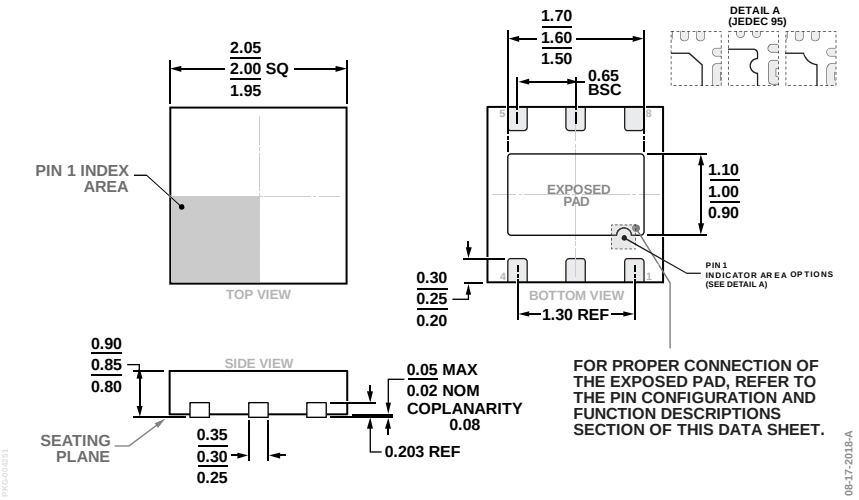

Figure 73. 6-Lead Lead Frame Chip Scale Package [LFCSP],
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-6-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	MSL Rating[3]	Package Description[4]	Package Option
HMC8411LP2FE	−40°C to +85°C	MSL1	6-Lead Lead Frame Chip Scale Package [LFCSP]	CP-6-12
HMC8411LP2FETR	−40°C to +85°C	MSL1	6-Lead Lead Frame Chip Scale Package [LFCSP]	CP-6-12
EV1HMC8411LP2F			Evaluation Board	

[1] The HMC8411LP2FE and HMC8411LP2FETR are RoHS compliant parts.
[2] When ordering the evaluation board only, reference the model number, EV1HMC8411LP2F.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC8411LP2FE and HMC8411LP2FETR is nickel palladium gold (NiPdAu).