450 MHz to 2800 MHz, DPD RFIC with Integrated Fractional-N PLL and VCO

Data Sheet **ADRF6821**

FEATURES

DPD receiver with integrated fractional-N PLL
RF input frequency range: 450 MHz to 2800 MHz
Internal LO input frequency range: 450 MHz to 2800 MHz
Dual RF inputs with SPDT absorptive RF switches
Integrated RF balun for single-ended 50 Ω input
Integrated VCO to cover complete RF input range
Digital programmable LO phase offset and dc nulling
Programmable via 4-wire SPI
56-lead, 8 mm × 8 mm LFCSP

APPLICATIONS

Cellular W-CDMA/GSM/LTE
DPD receivers
Microwave, point to point radios

GENERAL DESCRIPTION

The ADRF6821 is a highly integrated, dual radio frequency (RF) input, zero intermediate frequency (IF)/low IF RFIC receiver with a quadrature demodulator, digital step attenuator (DSA), IF linear amplifiers, an integrated, fractional-N phase-locked loop (PLL), and a low phase noise, multicore, voltage controlled oscillator (VCO). The RFIC is ideally suited for communication digital predistortion (DPD) systems.

The high isolation 2:1 RF switch and on-chip wideband RF balun enable the ADRF6821 to support two single-ended, 50 Ω terminated RF inputs. A programmable attenuator ensures an optimal differential RF input level to the high linearity demodulator core. The integrated attenuator offers an attenuation range of 15 dB with a step size of 1 dB. High linearity IF amplifiers follow the demodulator and provide an interface to the next component in the chain, typically an analog-to-digital converter (ADC).

The ADRF6821 offers two alternatives for generating the differential local oscillator (LO) input signal: internally via the on-chip fractional-N synthesizer with low phase noise VCOs or externally via a low phase noise LO signal. The integrated synthesizer enables continuous LO coverage from 450 MHz to 2800 MHz. The PLL reference input supports a wide frequency range and includes integrated reference dividers before the phase frequency detector (PFD).

When selected, the output of the internal fractional-N synthesizer is applied to a divide by 2, quadrature phase splitter. From the external LO path, a 2× LO signal can be used with the divide by 2, quadrature phase splitter to generate the quadrature LO inputs to the mixers.

The ADRF6821 is fabricated using an advanced silicon germanium (SiGe), bipolar complementary metal oxide semiconductor (BiCMOS) process. It is available in a 56-lead, RoHS compliant, 8 mm × 8 mm LFCSP package with an exposed pad. Performance is specified over the −40°C to +105°C case temperature range.

FUNCTIONAL BLOCK DIAGRAM

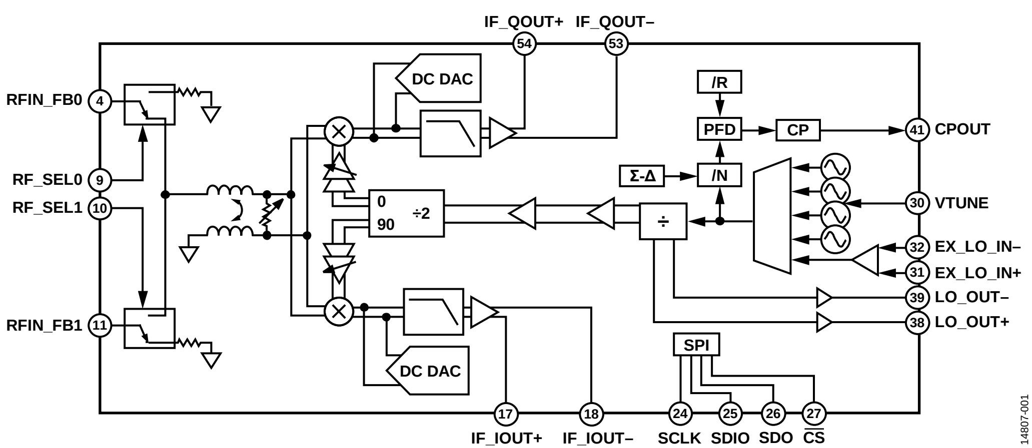

Figure 1.

Rev. A Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

8/2018—Rev. 0 to Rev. A

Changed VCC_AMP_I Pin and VCC_MIX_I Pin to VCC_IFMIX_I Pin ... Throughout
Changed VCC_MIX_Q Pin and VCC_AMP_Q Pin to VCC_IFMIX_Q Pin ... Throughout
Changes to Figure 3 ... 10
Changes to Figure 62 ... 32
Updated Outline Dimensions ... 62

5/2017—Revision 0: Initial Version

SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, low-side LO injection, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, common-mode voltage (V_{CM}) = 1.6 V, 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Input Impedance			50		Ω
RF Frequency Range		450		2800	MHz
I/Q OUTPUT INTERFACE					
Return Loss	IF_IOUT± and IF_QOUT± terminated with 100 Ω differential loads (25 Ω external resistors are required on each differential output pin)		−10		dB
Output Impedance			10		Ω
Output DC Offset	No correction		40		mV
	Correction applied		2		mV
DC Offset Correction Range			55		mV
Output V_{CM}		1.2	1.6	1.8	V
V_{CM} Ripple		−5		+5	mV
LO INPUT	External LO operation, differential				
Required Power		−6		+6	dBm
Input Impedance			100		Ω
Return Loss			−10		dB
Frequency Range	Low-side or high-side LO	450		2800	MHz
LO OUTPUT	2× LO output, differential, observation purposes only				
Power[1, 2]	TRM_XLODRV_DRV_POUT = 1				
2× f_{LO} = 1800 MHz			0		dBm
2× f_{LO} = 3600 MHz			−1		dBm
2× f_{LO} = 5400 MHz			0		dBm
Output Impedance	Differential		50		Ω
Return Loss			−10		dB
Frequency Range	2× f_{LO}	900		5600	MHz
POWER SUPPLY					
PLL/VCO Supplies[3]		3.2	3.3	3.4	V
RF/IF Supplies		3.1	3.3	3.5	V
POWER CONSUMPTION					
RF/IF Supplies			0.9		W
PLL/VCO Supplies					
f_{LO} = 1000 MHz	Internal LO		1.0		W
f_{LO} = 2000 MHz	Internal LO		0.9		W
f_{LO} = 2800 MHz	Internal LO		0.8		W

[1] For LO output power setting, see the LO Generation Block section.
[2] f_{LO} means LO frequency.
[3] See the Applications Information section for the supply circuit design.

SYSTEM SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, V_{CM} = 1.6 V, 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DEMODULATION BANDWIDTH			500		MHz
GROUP DELAY RIPPLE	Fixed LO frequency, any 75 MHz bandwidth (BW)		0.1		ns
	Fixed LO frequency, any 280 MHz BW		0.2		ns
DYNAMIC PERFORMANCE AT f_{LO} = 1000 MHz	High-side LO, IF frequency (f_{IF}) = 100 MHz, RF frequency (f_{RF}) = 900 MHz, low-pass filter (LPF) set to lowest BW				
Power Gain			12		dB
Gain Flatness	Over any 75 MHz bandwidth, LPF set to maximum BW		0.12		dB
	Over any 280 MHz bandwidth, LPF set to maximum BW		0.35		dB
Output 1 dB Power Compression (OP1dB)	Over all DSA settings, V_{CM} = 1.6 V		12		dBm
Output Third-Order Intercept (OIP3)	Over all DSA settings, output power (P_{OUT}) = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		33		dBm
	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 175 MHz to 200 MHz separation		35		dBm
Output Second-Order Intercept (OIP2)	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		75		dBm
Second-Order Harmonic Distortion (HD2)	P_{OUT} = −7 dBm continuous wave (CW) signal		−85		dBc
Third-Order Harmonic Distortion (HD3)	P_{OUT} = −7 dBm CW signal		−85		dBc
Noise Figure	Double-side band (DSB)		14		dB
Image Rejection			−41		dB
LO to IF Leakage	See Figure 26		−40		dBm
LO to RF Leakage	See Figure 27		−62		dBm
RF to IF Leakage	See Figure 25		−47		dBc
Isolation	Channel to channel		−58		dBc
DYNAMIC PERFORMANCE AT f_{LO} = 2000 MHz	Low-side LO, f_{IF} = 100 MHz, f_{RF} = 2100 MHz				
Power Gain			11		dB
Gain Flatness	Over any 75 MHz bandwidth		0.16		dB
	Over any 280 MHz bandwidth		0.55		dB
OP1dB	Over all DSA settings, V_{CM} = 1.6 V		12		dBm
OIP3	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} =1 MHz to 75 MHz separation		32		dBm
	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 175 MHz to 200 MHz separation		33		dBm
OIP2	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		74		dBm
HD2	P_{OUT} = −7 dBm CW signal		−81		dBc
HD3	P_{OUT} = −7 dBm CW signal		−86		dBc
Noise Figure	DSB		15		dB
Image Rejection			−41		dB
LO to IF Leakage	See Figure 26		−48		dBm
LO to RF Leakage	See Figure 27		−61		dBm
RF to IF Leakage	See Figure 25		−52		dBc
Isolation	Channel to channel		−43		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE AT f_{LO} = 2800 MHz	High-side LO, f_{IF} = 100 MHz, f_{RF} = 2700 MHz				
Power Gain			10		dB
Gain Flatness	Over any 75 MHz bandwidth		0.08		dB
	Over any 280 MHz bandwidth		0.25		dB
OP1dB	Over all DSA settings, V_{CM} = 1.6 V		12		dBm
OIP3	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} =1 MHz to 75 MHz separation		33		dBm
	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 175 MHz to 200 MHz separation		34		dBm
OIP2	Over all DSA settings, P_{OUT} = −10 dBm/tone, f_{IF} = 1 MHz to 75 MHz separation		70		dBm
HD2	P_{OUT} = −7 dBm CW signal		−80		dBc
HD3	P_{OUT} = −7 dBm CW signal		−82		dBc
Noise Figure	DSB		17		dB
Image Rejection			−32		dB
LO to IF Leakage	See Figure 26		−54		dBm
LO to RF Leakage	See Figure 27		−59		dBm
RF to IF Leakage	See Figure 25		−61		dBc
Isolation	Channel to channel		−46		dBc

DSA AND RF INPUT SWITCH SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, V_{CM} = 1.6 V, 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL STEP ATTENUATOR					
Attenuation Range			15		dB
Step Size			1		dB
Step Error			±(0.3 + attenuation × 5%)		dB
Settling Time	Between any two different attenuation settings		100		ns
DSA Phase Shift	Between any two different attenuation settings		5		Degrees
RF INPUT SWITCH					
Switch Settling Time	50% control signal to 99% or1% RF signal final value		2		µs

PLL/VCO SPECIFICATIONS

All supply pins = 3.3 V, T_A = 25°C, reference frequency (f_{REF}) = 122.88 MHz, f_{REF} power = 10 dBm, PFD frequency (f_{PFD}) = 30.72 MHz, and loop filter BW = 20 kHz, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL REFERENCE					
Frequency		10	30.72	250	MHz
Level	For PLL lock condition, 50 Ω to ground required close to REF_IN pin	0.7		3.3	V p-p
Step Size			240		kHz
Lock Time	For PLL lock condition		0.4		ms
PFD FREQUENCY, f_{PFD}			30.72	61.44	MHz
INTERNAL VCO RANGE		4000		8000	MHz
OPEN-LOOP VCO PHASE NOISE					
VCO Frequency (f_{VCO}) = 5440 MHz					
	10 kHz offset		−83		dBc/Hz
	100 kHz offset		−110		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	10 MHz offset		−152		dBc/Hz
f_{VCO} = 7060 MHz					
	10 kHz offset		−80		dBc/Hz
	100 kHz offset		−106		dBc/Hz
	1 MHz offset		−127		dBc/Hz
	10 MHz offset		−147		dBc/Hz
SYNTHESIZER SPECIFICATIONS					
Fractional Figure of Merit (FOM)			−227		dBc/Hz
Flicker FOM			−262		dBc/Hz
f_{PFD} Spurs[1]	Output to internal mixer and daisy-chain of another ADRF6821				
$f_{PFD} \times 1$			−90		dBc
$f_{PFD} \times 2$			−95		dBc
$f_{PFD} \times 3$ and Higher			−95		dBc
Unwanted Spurs (Other Than PFD and Harmonics)[1]	Output to internal mixer and daisy-chain of another ADRF6821		−70		dBc
f_{LO} = 1765 MHz, f_{VCO} = 7060 MHz					
Closed-Loop Phase Noise	1 kHz offset		−102		dBc/Hz
	10 kHz offset		−97		dBc/Hz
	100 kHz offset		−117		dBc/Hz
	950 kHz offset		−138		dBc/Hz
	2.1 MHz offset		−145		dBc/Hz
	3.5 MHz offset		−149		dBc/Hz
	7.5 MHz offset		−153		dBc/Hz
	10 MHz offset		−156		dBc/Hz
	85 MHz offset		−158		dBc/Hz
Integrated Phase Noise	100 Hz to 10 MHz integration BW		0.2		°rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{LO} = 2720 MHz, f_{VCO} = 5440 MHz					
Closed-Loop Phase Noise	1 kHz offset		−102		dBc/Hz
	10 kHz offset		−99		dBc/Hz
	100 kHz offset		−114		dBc/Hz
	950 kHz offset		−137		dBc/Hz
	2.1 MHz offset		−144		dBc/Hz
	3.5 MHz offset		−148		dBc/Hz
	7.5 MHz offset		−153		dBc/Hz
	10 MHz offset		−155		dBc/Hz
	85 MHz offset		−156		dBc/Hz
Integrated Phase Noise	100 Hz to 10 MHz integration BW		0.2		°rms

[1] Auxiliary LO output measurements are performed under a daisy-chain configuration with another ADRF6821 device. Measurements are taken from the auxiliary LO output of the daisy chained ADRF6821.

DIGITAL LOGIC SPECIFICATIONS

The following specifications are for all digital inputs.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUT VOLTAGE						
Low	V_{IL}		0		0.5	V
High	V_{IH}		1.2		3.6	V
LOGIC INPUT CURRENT						
High	I_{IH}		−100		+100	µA
Low	I_{IL}		−100		+100	µA
LOGIC OUTPUT VOLTAGE						
Low	V_{OL}		0		0.4	V
High	V_{OH}	When driving loads with complementary metal oxide semiconductor (CMOS) 1.8 V interface	1.4		1.8	V
		When driving loads with CMOS 3.3 V interface	2.4		3.3	V
LOGIC OUTPUT CURRENT						
High Driving	I_{OH}			1	2	mA
Low Driving	I_{OL}			1	2	mA

SERIAL PERIPHERAL INTERFACE (SPI) TIMING SPECIFICATIONS

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit
TIMING REQUIREMENTS					
SDI to SCLK Rising Edge Setup	t_{DS}	8			ns
SCLK Rising Edge to SDI Hold	t_{DH}	8			ns
Period of SCLK	t_{CLK}	50			ns
$\overline{CS}$ Falling Edge to SCLK Rising Edge, Setup Time	t_S	10			ns
SCLK Rising Edge to $\overline{CS}$ Rising Edge, Hold Time	t_C	30			ns
SCLK Falling Edge to Valid Readback Data, SDIO or SDO (Not Shown in Figure 2)	t_{DV}	18			ns
SCLK					
Period of SCLK for a Logic High State	t_{HIGH}	25			ns
Period of SCLK for a Logic Low State	t_{LOW}	25			ns

SPI Timing Diagram

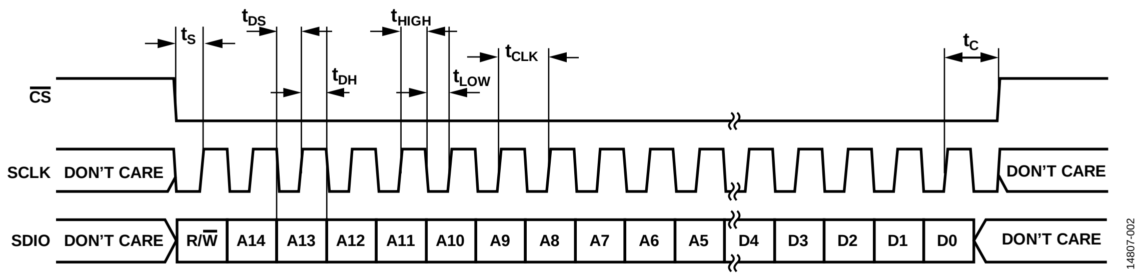

Figure 2. SPI Write (MSB First), 16-Bit Instruction, Timing Measurements

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VCC_LO1, VCC_LO2, VCC_3V3_I, VCC_3V3_Q, VCC_IFMIX_I, VCC_IFMIX_Q, VCCVCO_3V3, VCCDIV_3V3, VCCFBDIV_3V3, VCCLO_MIX_3V3, VCCLO_AUX_3V3, VCCCP_3V3, VCCPFD_3V3, VCCREF_3V3, VBAT_DIG_3V3	−0.3 V to +3.6 V
VCM_I, VCM_Q	−0.3 V to +3.3 V
$\overline{\text{CS}}$, SCLK, SDIO, SDO	−0.3 V to +3.6 V
RF_SEL0, RF_SEL1, RFBT_FB	−0.3 V to +3.6 V
RFIN_FB0, RFIN_FB1	2.5 V peak, ac-coupled
$\overline{\text{RST}}$, SLEEP	−0.3 V to +3.6 V
VTUNE, CPOUT, REF_IN, DCL_BIAS	−0.3 V to +3.6 V
RF Input Power RFIN	20 dBm
EXT_LO_IN−, EXT_LO_IN+	10 dBm, differential
Maximum Junction Temperature	125°C
Operating Temperature Range (Measured at Paddle)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Typical θ_{JA} and θ_{JC} are specified vs. the number of PCB layers. The use of appropriate thermal management techniques is recommended to ensure the maximum junction temperature does not exceed the limits shown in Table 8.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-56-16[1]			
JEDEC 1s0p Board[2]	Not applicable	3.3	°C/W
Cold Plate Only, No PCB[3]	Not applicable	2.8	°C/W
JEDEC 2s2p Board[2]	29.3	Not applicable	°C/W

[1] The maximum junction temperature of 125°C cannot be exceeded.
[2] Per JEDEC JESD51-12.
[3] For nonstandardized testing where the paddle of the device is directly connected to a cold plate. This approach can be useful to estimate junction temperature when the exact paddle temperature is known in the application.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

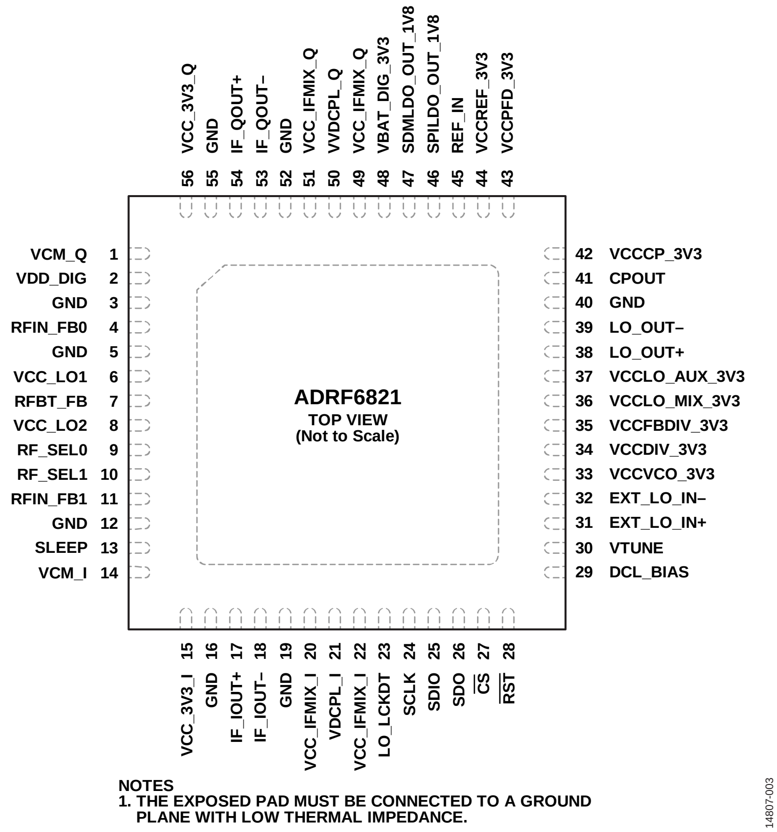

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCM_Q	Q Channel VCM Input.
2	VDD_DIG	Digital VDD (1.8 V) Pin from On-Chip LDO.
3, 5, 12, 16, 19, 52, 55	GND	Ground.
4	RFIN_FB0	RF Input 0 Single-Pole, Double-Throw (SPDT), 50 Ω Single-Ended.
6	VCC_LO1	LO Path VCC.
7	RFBT_FB	RF Input Low Frequency Balun Connection. This pin requires a dc block to an external inductor.
8	VCC_LO2	LO Path VCC.
9	RF_SEL0	RF Input 0 Select.
10	RF_SEL1	RF Input 1 Select.
11	RFIN_FB1	RF Input 1 SPDT, 50 Ω Single-Ended.
13	SLEEP	Pin Controllable Fast Turn On/Off (1.8 V and 3.3 V Compatible).
14	VCM_I	I Channel VCM Input.
15	VCC_3V3_I	I Channel 3.3 V Supply.
17	IF_IOUT+	I Channel IF Positive Output.
18	IF_IOUT–	I Channel IF Negative Output.
20	VCC_IFMIX_I	I Channel IF Amplifier VCC Supply.
21	VDCPL_I	I Channel Mixer Decoupling.
22	VCC_IFMIX_I	I Channel Mixer VCC Supply.
23	LO_LCKDT	LO Lock Detect.
24	SCLK	SPI Clock.
25	SDIO	SPI Data Input/Output in 3-Wire Mode. SPI data input in 4-wire mode.
26	SDO	SPI Data Output. SDO used in 4-wire mode only.

Pin No.	Mnemonic	Description
27	$\overline{\text{CS}}$	SPI Chip Select (N).
28	$\overline{\text{RST}}$	Reset (Active Low).
29	DCL_BIAS	VCO Core Bias Decouple.
30	VTUNE	V_{TUNE} Input.
31	EXT_LO_IN+	Positive External LO Input.
32	EXT_LO_IN−	Negative External LO Input.
33	VCCVCO_3V3	VCC 3.3 V Supply.
34	VCCDIV_3V3	LO Chain and Divider 3.3 V Supply.
35	VCCFBDIV_3V3	PLL Feedback Divider 3.3 V Supply.
36	VCCLO_MIX_3V3	LO Mixer Output Buffer 3.3 V Supply.
37	VCCLO_AUX_3V3	LO External Output Buffer 3.3 V Supply.
38	LO_OUT+	Positive External LO Output.
39	LO_OUT−	Negative External LO Output.
40	GND	Charge Pump Ground.
41	CPOUT	Charge Pump Output.
42	VCCCP_3V3	Charge Pump 3.3 V Supply.
43	VCCPFD_3V3	PFD 3.3 V Supply.
44	VCCREF_3V3	Reference Input Buffer 3.3 V Supply.
45	REF_IN	Reference Input Buffer.
46	SPILDO_OUT_1V8	SPI 1.8 V LDO External Decouple Output.
47	SDMLDO_OUT_1V8	Sigma-Delta Modulator (SDM) 1.8 V LDO External Decouple Output.
48	VBAT_DIG_3V3	SPI and SDM LDO 3.3 V Input.
49	VCC_IFMIX_Q	Q Channel Mixer VCC Supply.
50	VDCPL_Q	Q Channel Mixer Decoupling.
51	VCC_IFMIX_Q	Q Channel IF Amplifier VCC Supply.
53	IF_QOUT−	Q Channel IF Negative Output.
54	IF_QOUT+	Q Channel IF Positive Output.
56	VCC_3V3_Q	Q Channel 3.3 V Supply.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

All supply pins = 3.3 V, TA = 25°C, high-side LO injection for LO frequencies less than or equal to 1 GHz and equal to 2.8 GHz, low-side LO injection for frequencies between 1 GHz and 2.8 GHz, internal LO, minimum attenuation setting (DSA setting of 0 dB), MIXER_GAIN_PEAK = 0, V_{CM} = 1.6 V, and 25 Ω matching resistors on I/Q differential outputs, unless otherwise noted. For linearity measurements, a tone spacing of 75 MHz is used, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

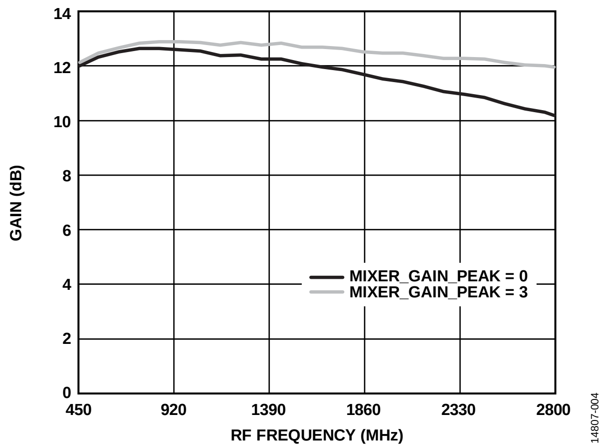

Figure 4. Gain vs. RF Frequency for Various MIXER_GAIN_PEAK (Register 0x003A, Bits[1:0]) Settings

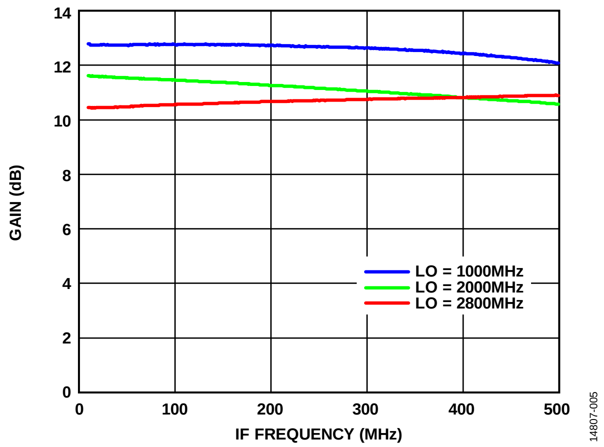

Figure 5. Gain vs. IF Frequency, RF Sweep with Fixed LO, RF to IF Roll-Off

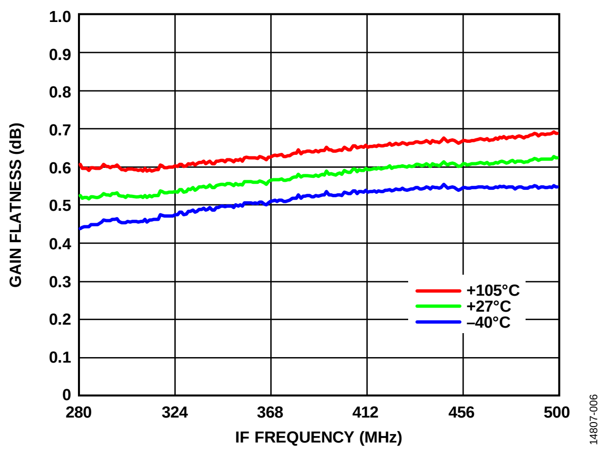

Figure 6. Gain Flatness vs. IF Frequency, Fixed LO Frequency of 2000 MHz, 280 MHz IF Frequency Window

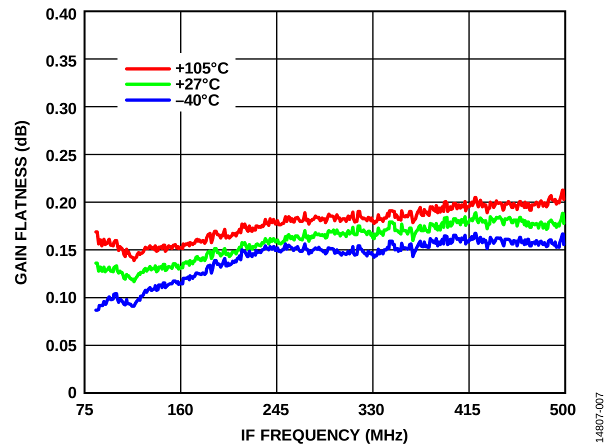

Figure 7. Gain Flatness vs. IF Frequency, Fixed LO Frequency of 2000 MHz, 75 MHz IF Frequency Window

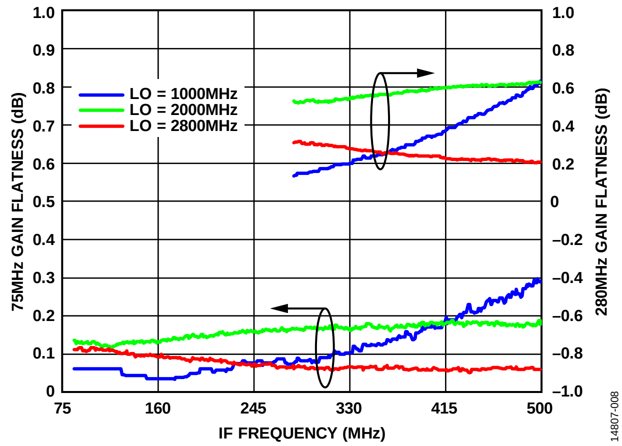

Figure 8. Gain Flatness vs. IF Frequency for Various LOs, 75 MHz (Left Axis) and 280 MHz (Right Axis) IF Frequency Window

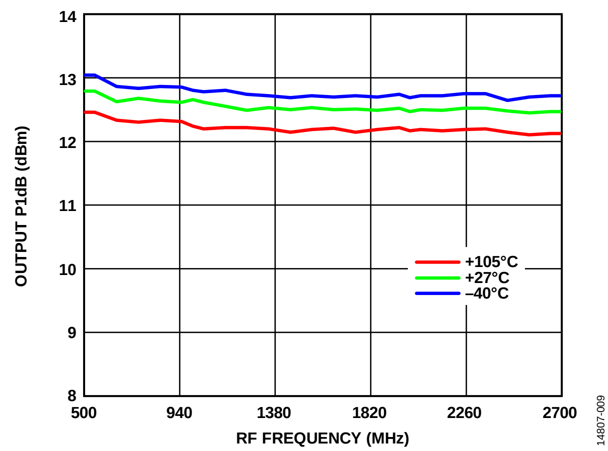

Figure 9. Output P1dB vs. RF Frequency

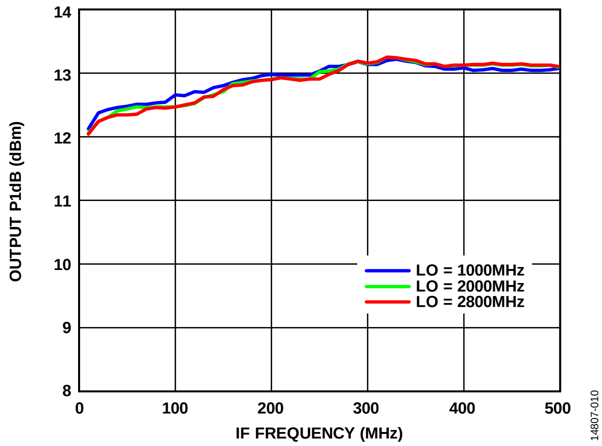

Figure 10. Output P1dB vs. IF Frequency, RF Sweep with Fixed LO, Various LO Frequency

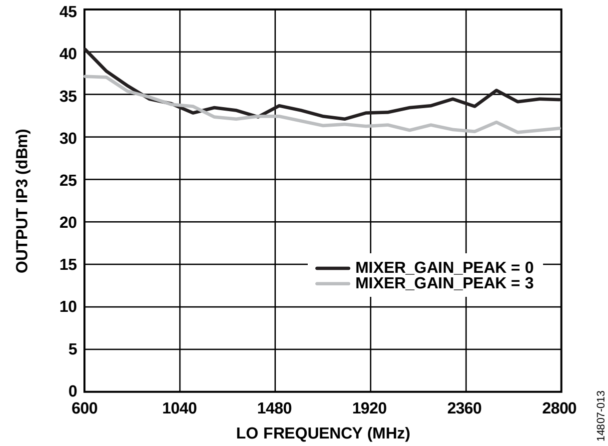

Figure 13. Output IP3 vs. LO Frequency, Measured on −10 dBm for Each Tone at the IF Output for Various MIXER_GAIN_PEAK (Register 0x003A, Bits[1:0]) Settings

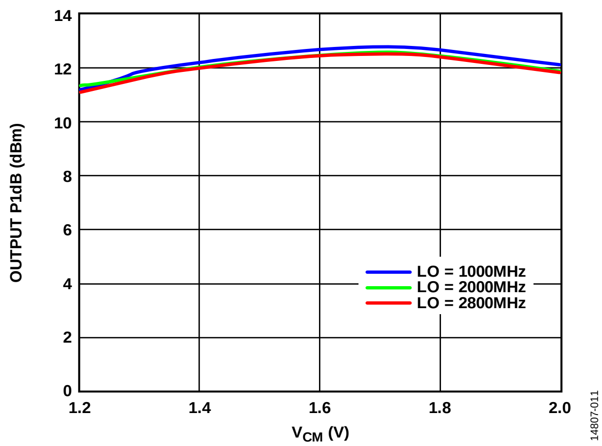

Figure 11. Output P1dB vs. Common-Mode Voltage (V_{CM}), IF = 100 MHz

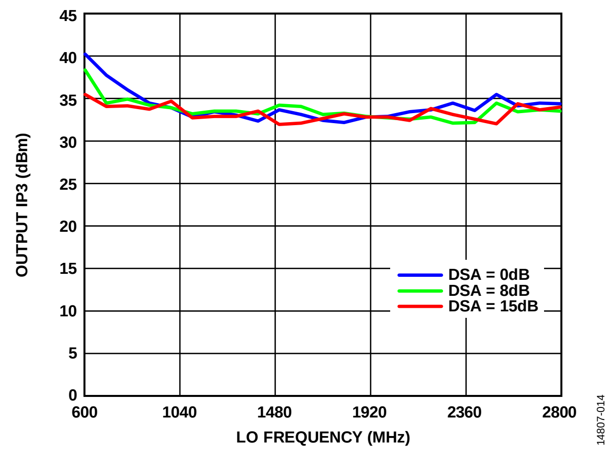

Figure 14. Output IP3 vs. LO Frequency for Various DSA Settings, Measured on −10 dBm for Each Tone at the IF Output

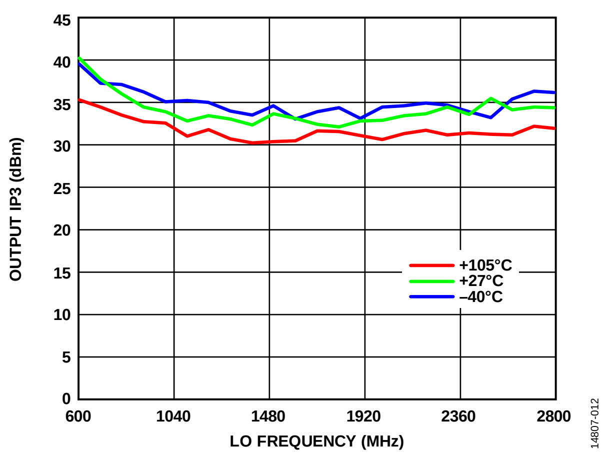

Figure 12. Output IP3 vs. LO Frequency, Measured on −10 dBm for Each Tone at the IF Output for Various Temperature

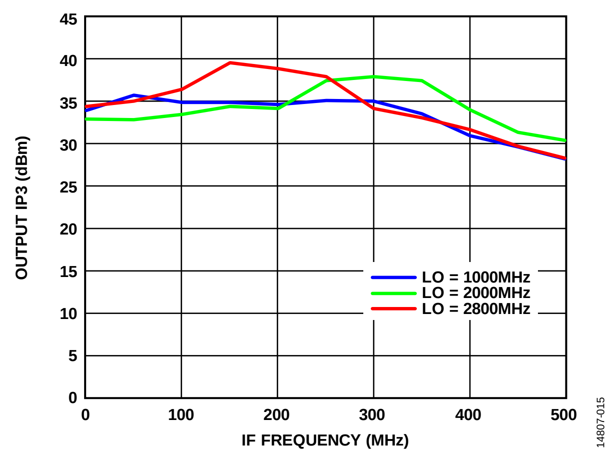

Figure 15. Output IP3 vs. IF Frequency for Various LO Frequencies, Measured on −10 dBm for Each Tone at the IF Output, Low Side LO for 1 GHz

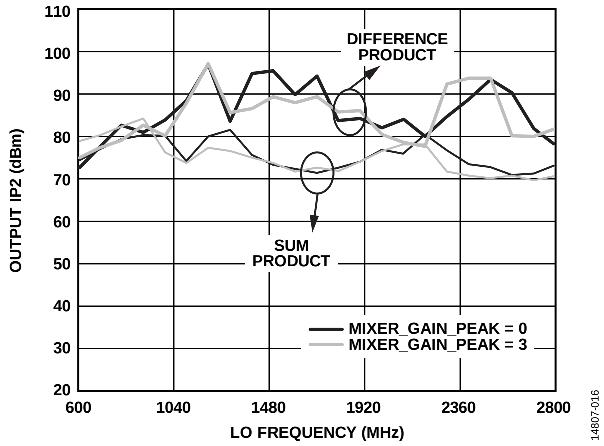

Figure 16. Output IP2 vs. LO Frequency for Various MIXER_GAIN_PEAK (Register 0x003A, Bits[1:0]) Settings

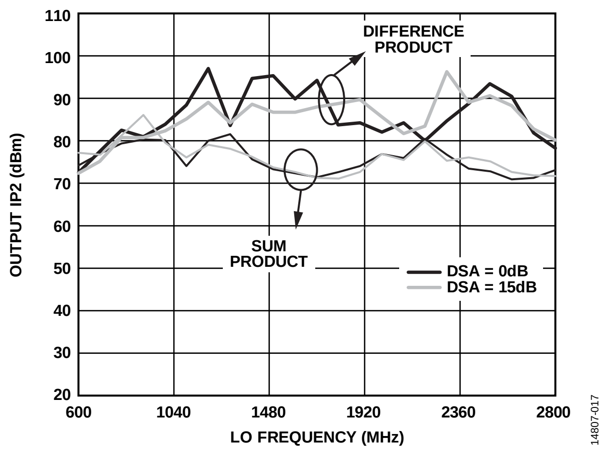

Figure 17. Output IP2 vs. LO Frequency, Measured on −10 dBm for Each Tone at the IF Output for Various DSA Settings

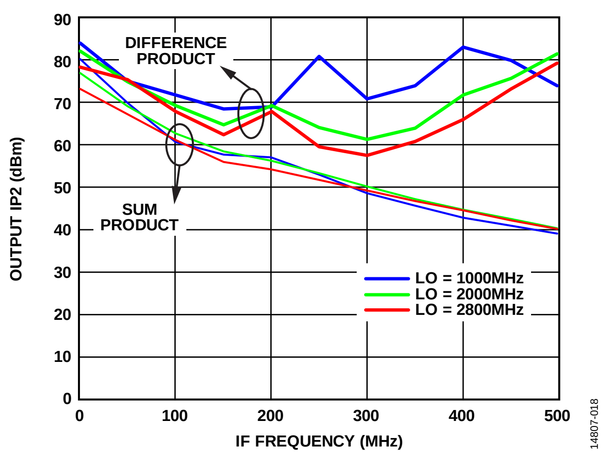

Figure 18. Output IP2 vs. IF Frequency, RF Sweep with Fixed LO, Measured on −10 dBm for Each Tone at the IF Output

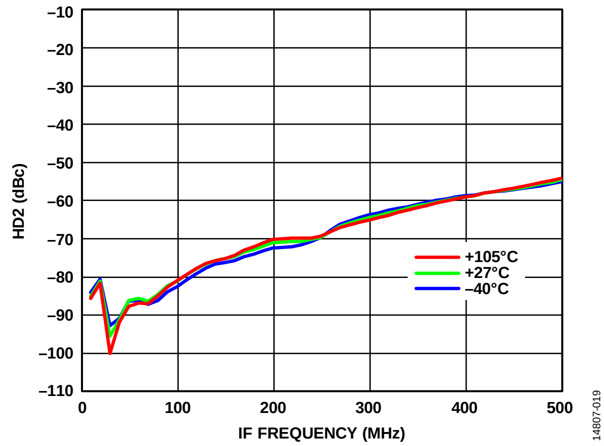

Figure 19. HD2 vs IF Frequency, LO at 2000 MHz and P_{OUT} = −7 dBm

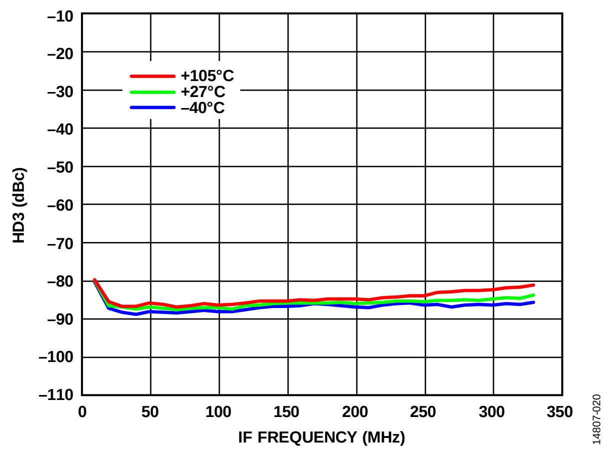

Figure 20. HD3 vs. IF Frequency, LO at 2000 MHz and P_{OUT} = −7 dBm

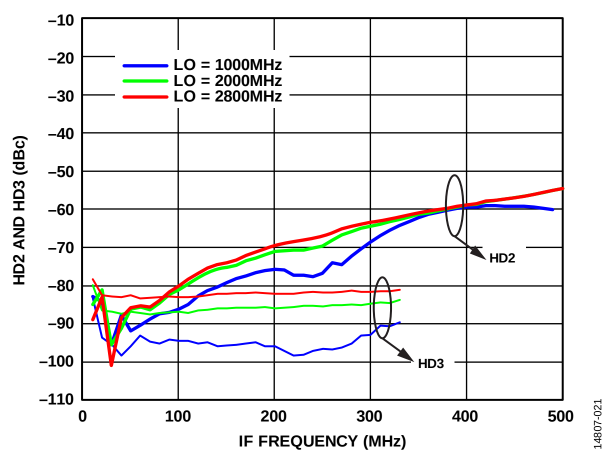

Figure 21. HD2 and HD3 vs. IF Frequency for Various LO Frequencies

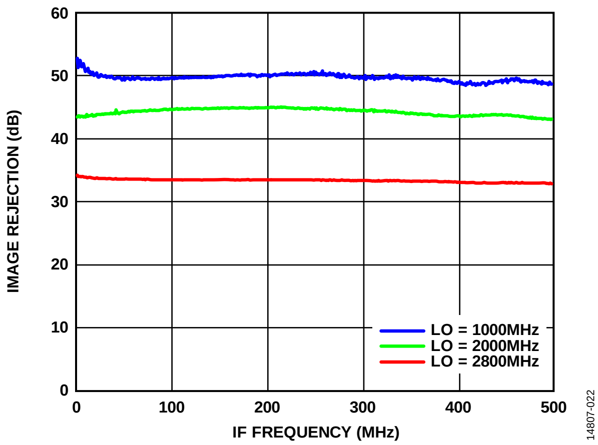

Figure 22. Image Rejection vs. IF Frequency for Various LO Frequencies

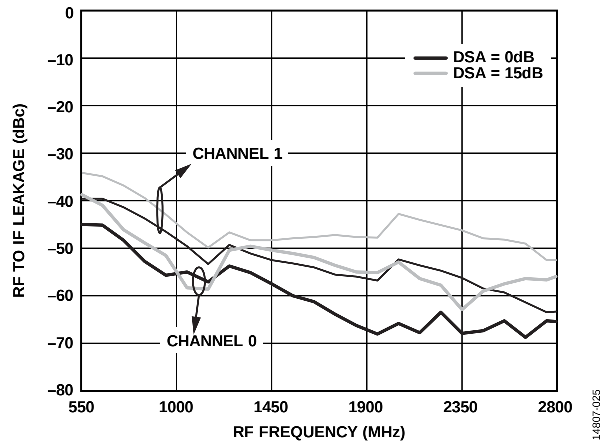

Figure 25. RF to IF Leakage at IF Output

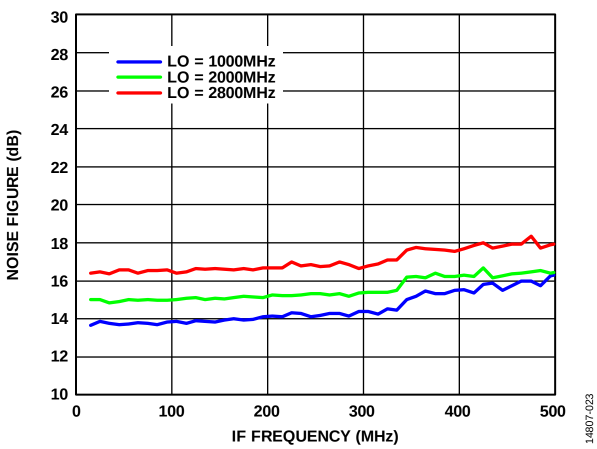

Figure 23. Noise Figure vs. IF Frequency for Various LO Frequencies, Double Side Band

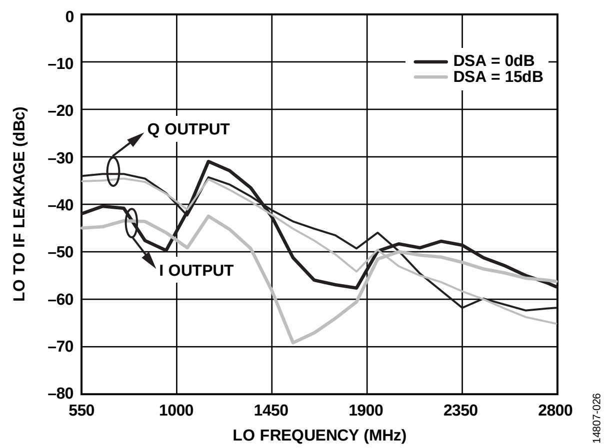

Figure 26. LO to IF Leakage at IF Output

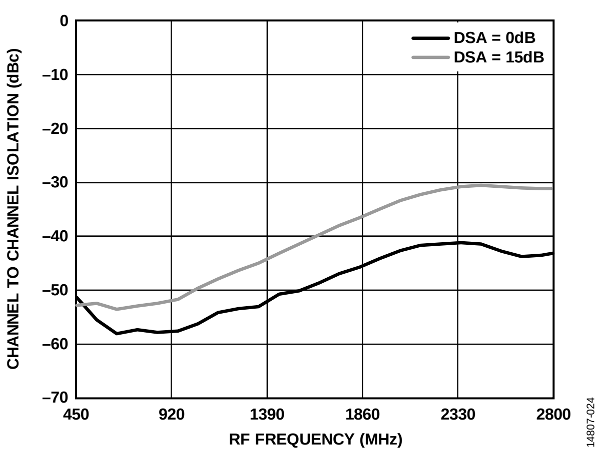

Figure 24. Channel to Channel Isolation vs. RF Frequency

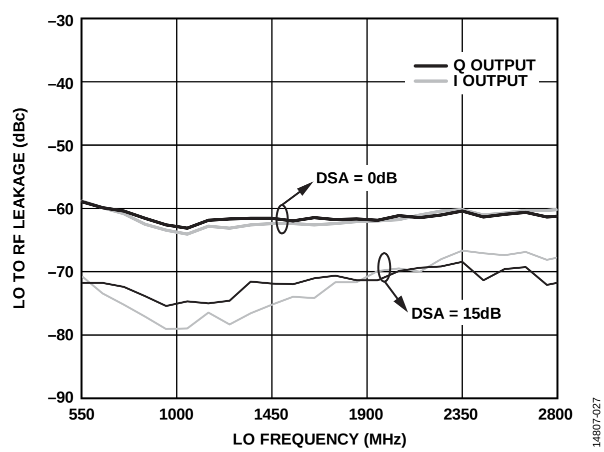

Figure 27. LO to RF Leakage vs. LO Frequency

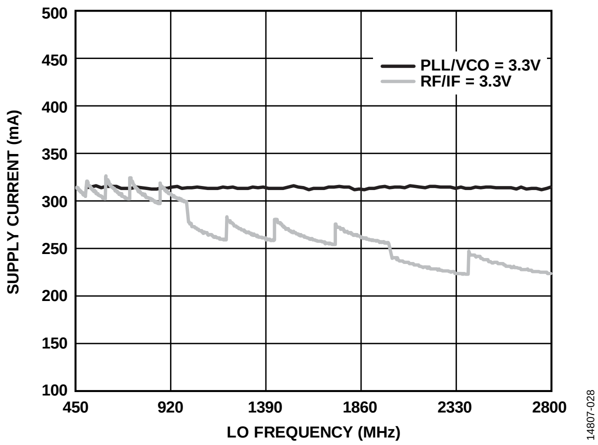

Figure 28. Supply Current vs. LO Frequency

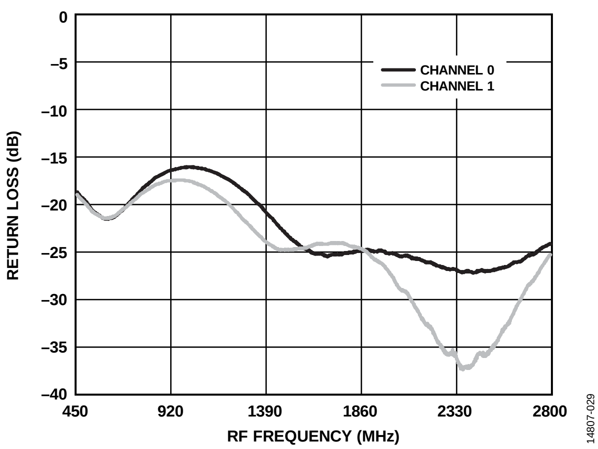

Figure 29. Return Loss vs. RF Frequency for Channel 0 and Channel 1

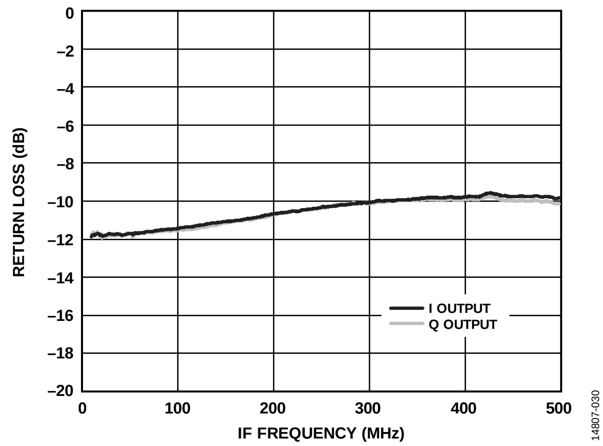

Figure 30. Return Loss vs. IF Frequency, Differential with 25 Ω Series Resistor on Each Leg, Measured with 100 Ω Differential

PHASE-LOCKED LOOP (PLL) PERFORMANCE

All supply pins = 3.3 V, T_A = 25°C, f_{PFD} = 30.72 MHz, f_{REF} = 122.88 MHz, 20 kHz loop filter, measured at LO output, unless otherwise noted.

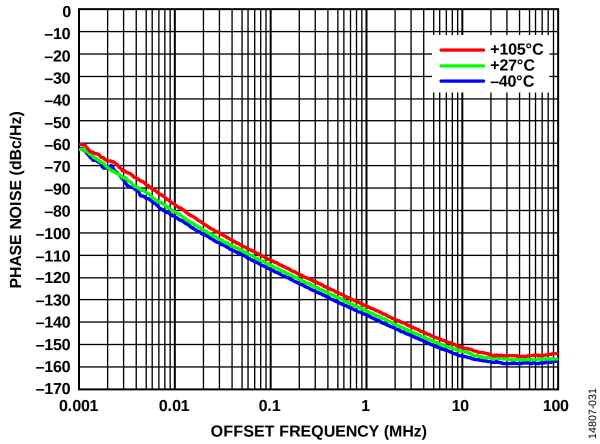

Figure 31. Open-Loop VCO Phase Noise vs. Offset Frequency for Various Temperatures

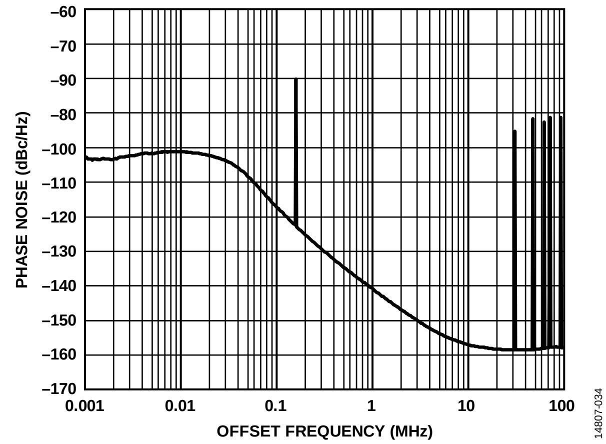

Figure 34. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 2350 MHz

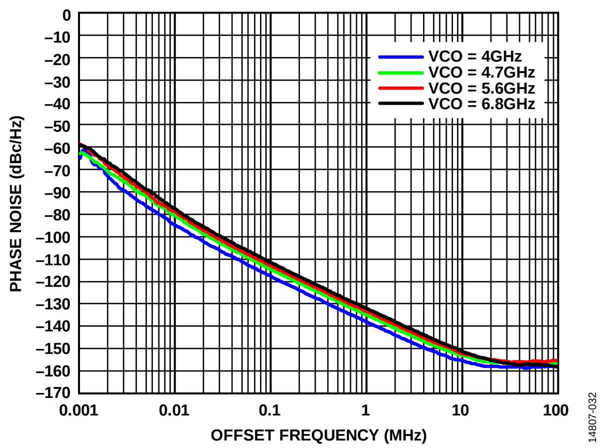

Figure 32. Open-Loop VCO Phase Noise vs. Offset Frequency for Various VCO Frequencies

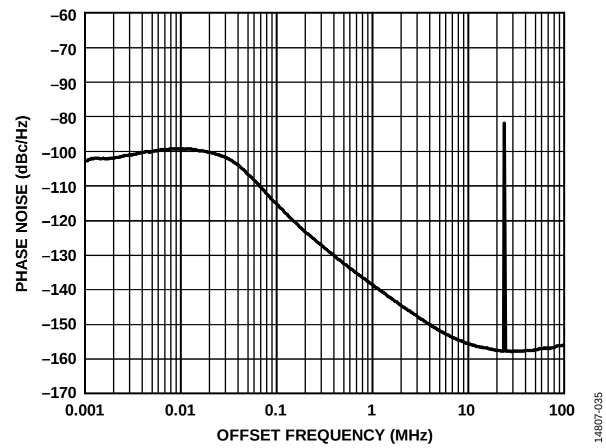

Figure 35. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 2720 MHz

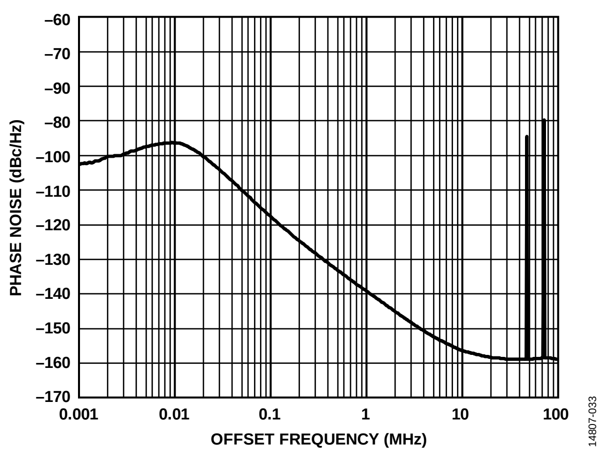

Figure 33. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 1765 MHz

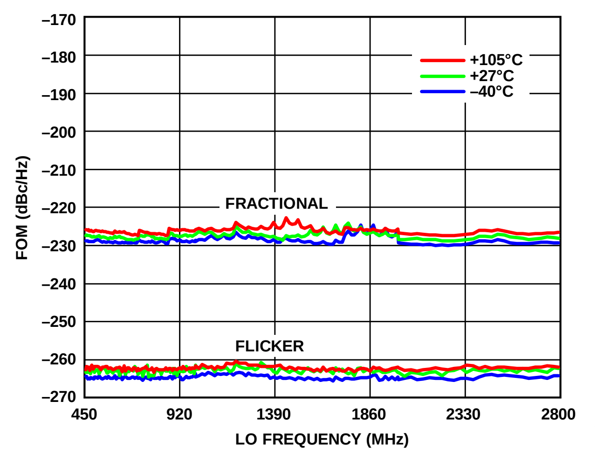

Figure 36. PLL Figure of Merit (FOM) vs. LO Frequency

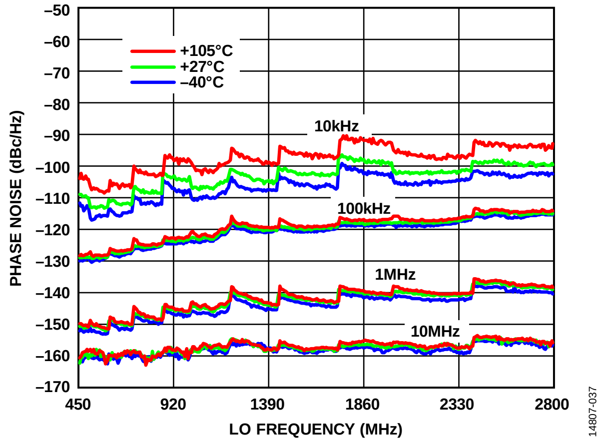

Figure 37. Closed-Loop LO Phase Noise vs. LO Frequency for Various Offset Frequencies and for Various Temperatures

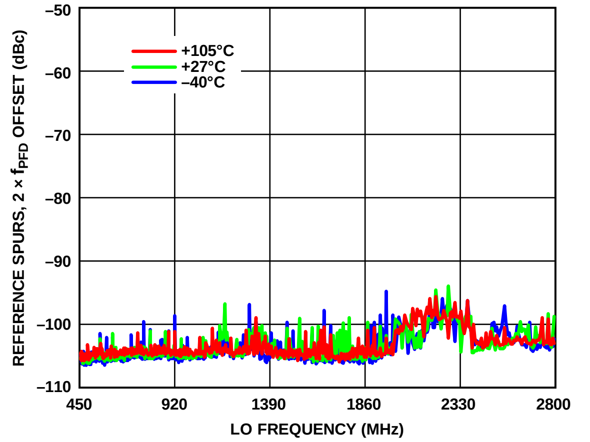

Figure 40. Reference Spurs, 2 × f_{PFD} Offset vs. LO Frequency

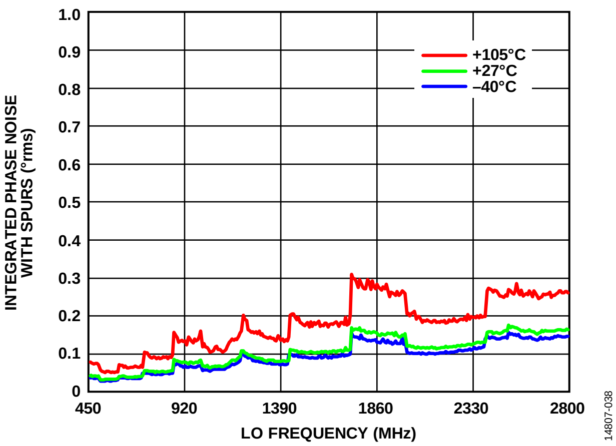

Figure 38. 100 Hz to 10 MHz Integrated Phase Noise with Spurs vs. LO Frequency

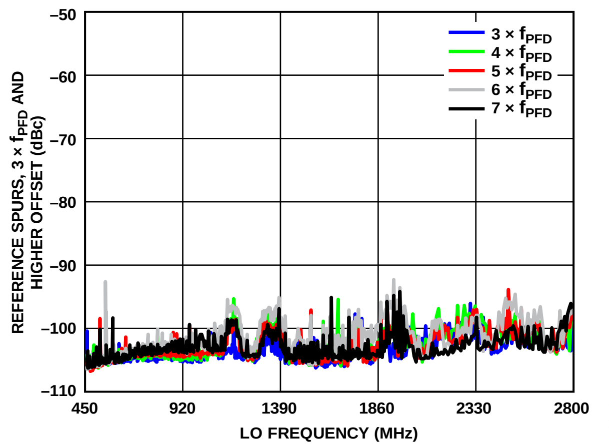

Figure 41. Reference Spurs, 3 × f_{PFD} and Higher Offset vs. LO Frequency

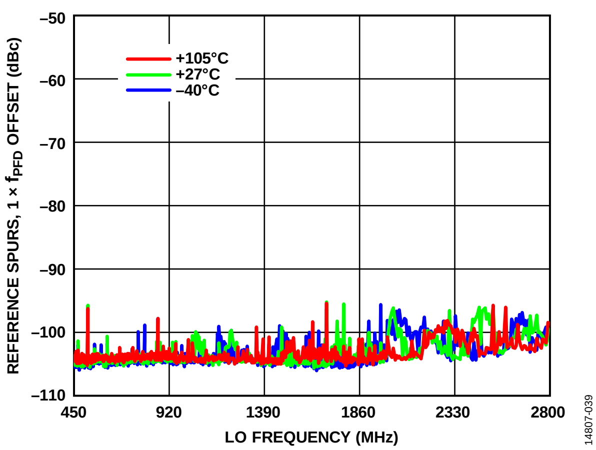

Figure 39. Reference Spurs, 1 × f_{PFD} Offset vs. LO Frequency

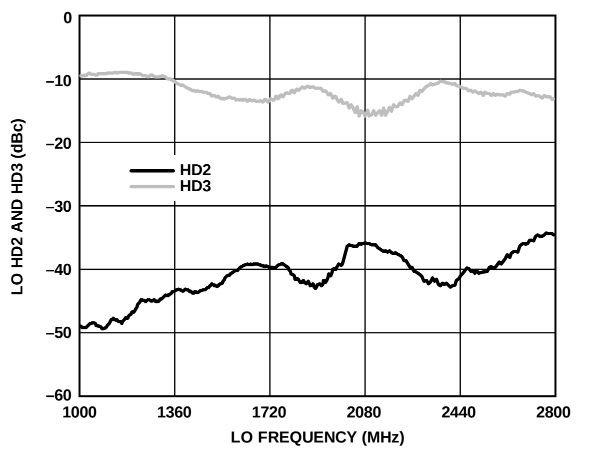

Figure 42. LO HD2 and HD3 vs. LO Frequency

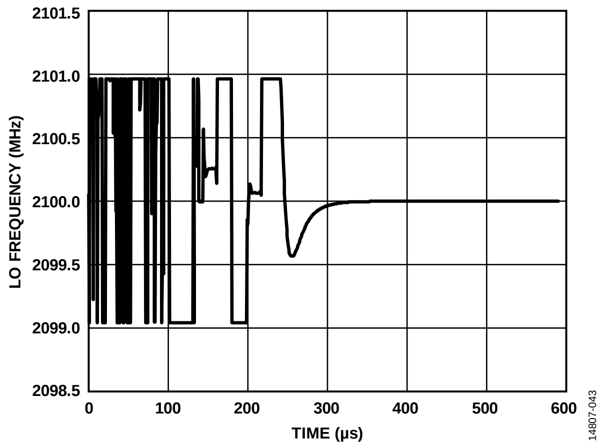

Figure 43. LO Frequency Settling Time, LO = 2.1 GHz

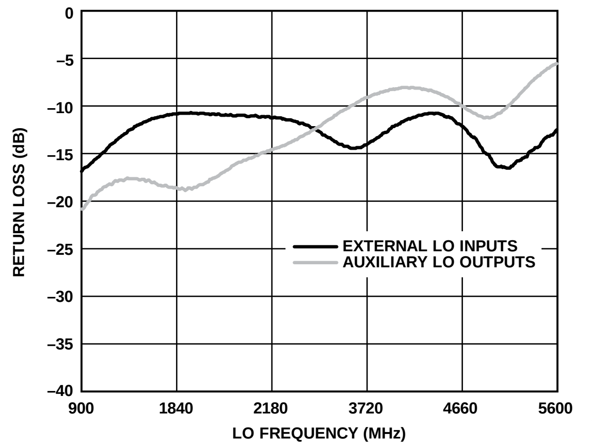

Figure 44. Return Loss vs. LO Frequency for Auxiliary LO Outputs and External LO Inputs

THEORY OF OPERATION

The ADRF6821 integrates many of the essential building blocks for a high bandwidth quadrature demodulator and receiver, especially for the feedback downconverter path for the digital predistortion in cellular base stations. The main features include two single-pole, double-throw (SPDT) RF input switches, a balun, a variable RF attenuator, a pair of active mixers, and two baseband buffers. Additionally, the local oscillator (LO) signals for the mixers are generated by a fractional-N synthesizer and a multicore voltage controlled oscillator (VCO), covering an octave frequency range with low phase noise. A pair of flip-flops then divides the LO frequency by two and generates the in phase and quadrature phase LO signals to drive the mixers. The synthesizer uses a fractional-N phase-locked loop (PLL) with additional frequency dividers to enable continuous LO coverage from 450 MHz to 2800 MHz.

The signal path through the device begins at one of two RF inputs, RFIN_FB0 and RFIN_FB1, selected by the RF switches. The selected single-ended input converts to a differential signal via the integrated balun. The differential RF signal attenuates to an optimal input level via the digital step attenuator with 15 dB of attenuation range in 1 dB steps. The RF signal then mixes with the LO signal in the Gilbert cell mixers down to an intermediate frequency (IF) or baseband. From the mixer, the signal passes through a wideband low-pass filter to remove the higher order mixing terms, followed by a fixed gain linear IF amplifier.

The different sections of the ADRF6821 are controlled through registers programmable via a serial peripheral interface (SPI).

The EN_ANALOG_MASTER bit (Register 0x0020, Bit 1) is the master enable for all enables related to the RF switch, attenuator, mixer, IF amplifiers, divider, and LO drivers. This bit does not control any of the enables related to LO generation blocks.

RF INPUT SWITCH

The ADRF6821 incorporates two SPDT switches, which allow one RF input to be selected while the other RF input can be correctly terminated to 50 Ω. Selection of the desired RF input is achieved externally via two control pins or serially via register writes to the SPI. When compared to the serial write approach, pin control allows faster switching between the RF inputs. Using the RF_SEL0 and RF_SEL1 pins (Pin 9 and Pin 10, respectively), the RF input can be switched from one channel to the other quickly and settle the IF output within 2 µs. When the input is controlled via the SPI serial port, the time for the serial data transfer must also be considered and is dependent on the serial interface clock rate.

The SEL_RFSW_SPI_CONTROL bit (Register 0x0030, Bit 6) selects whether the RF input switch is controlled via the external pins or via the SPI (see Table 10). By default at power-up, the device is configured for pin control. In serial mode control, writing to the RFSW_SEL0 bit (Register 0x0030, Bit 4) allows selection of RF Input 0 and writing to the RFSW_SEL1 bit (Register 0x0030, Bit 5) allows selection of RF Input 1. If only one RFINx port is used, the unused RF input must be properly terminated to improve isolation. It is recommended to use a dc blocking capacitor to GND as termination. Figure 45 shows the recommended configuration when only RFIN_FB0 is employed.

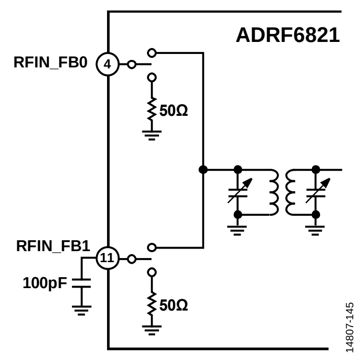

Figure 45. Terminating the Unused Port of the ADRF6821

Table 10. RF Input Selection[1]

SEL_RFSW_SPI_CONTROL Bit, (Register 0x0030, Bit 6)	RFSW_SEL0 Bit, (Register 0x0030, Bit 4)	RFSW_SEL1 Bit, (Register 0x0030, Bit 5)	RF_SEL0 and RF_SEL1 Pins	RF Input Pin
0	X	X	RF_SEL0	RFIN_FB0
0	X	X	RF_SEL1	RFIN_FB1
1	1	0	X	RFIN_FB0
1	0	1	X	RFIN_FB1

[1] X means don't care.

BALUN

The ADRF6821 integrates a balun operating over a 450 MHz to 2800 MHz frequency range. The wideband balun offers the benefit of ease of drivability with single-ended, 50 Ω RF inputs, and the single-ended to differential conversion of the integrated balun provides additional common-mode noise rejection.

RF ATTENUATOR

The RF digital step attenuator follows the balun, and the attenuation range is 0 dB to 15 dB with a step size of 1 dB. The ATTEN_DSA bits (Register 0x0031, Bits[5:2]) in the DSA_CONTROL register determine the setting of the RF digital step attenuator. The EN_DSA (Register 0x0031, Bit [0]) bit enables the RF attenuator.

ACTIVE MIXER

After the RF digital step attenuator, the RF signal is split and provided to a pair of double balanced, Gilbert cell active mixers. The RF signal is then downconverted by the on-chip LO at the mixer, resulting in a baseband output. Enable the mixer and the common-mode controls as listed in Table 11.

Table 11. Demodulator Enable Registers

Register Address	Value	Description
0x0032	0x3E	Demodulator enables
0x0040	0x0F	Common-mode control enables
0x0033	0x2D	Mixer LO common-mode control
0x0034	0x2D	Mixer output stage common-mode control

The ADRF6821 provides a gain peaking circuit to increase the gain for high RF. The amount of gain peaking is controlled by the MIXER_GAIN_PEAK bits (Register 0x003A, Bits[1:0]). Note that increased gain leads to slight degradation of the linearity performance.

The ADRF6821 uses dc compensation digital-to-analog converters (DACs) for both I and Q outputs. DC compensation covers a range of ±40 mV. Control the dc compensation value via the CODE_DC_IDAC_RF0 bits (Register 0x0051) for the I output and the CODE_DC_QDAC_RF0 bits (Register 0x0052) via the Q output for Channel 0. For Channel 1, use the CODE_DC_IDAC_RF1 bits (Register 0x0053) for the I output and the CODE_DC_QDAC_RF1 bits (Register 0x0054) for the Q output. The control words are in signed magnitude format and eight bits wide. The effective least significant bit (LSB) is approximately 0.5 mV.

I AND Q POLARITY

The ADRF6821 offers the flexibility of specifying the polarity of the I and Q outputs, where I can lead Q or vice versa. By addressing SEL_LODRV_PREDRVI_POL (Register 0x0080, Bit 1) or SEL_LODRV_PREDRVQ_POL (Register 0x0080, Bit 2), both the I and Q outputs can be inverted from their default configuration. The flexibility of specifying the polarity becomes important when the I and Q outputs are processed simultaneously in the complex domain, I + jQ.

At power-up, depending on the whether high-side or low-side injection of the LO frequency is applied, the I channel can either lead or lag the Q channel by 90°. When the RF frequency is greater than the LO frequency (low-side LO injection), the Q channel leads the I channel. On the contrary, if the RF frequency is less than the LO frequency (high-side LO injection), the I channel leads the Q channel by 90°.

LOW-PASS FILTERS (LPF) AND IF AMPLIFIERS

From the mixer, the IF or baseband outputs pass through an integrated adjustable LPF to remove the unwanted mixing product. The LPF bandwidth is adjustable over four steps, as listed in Table 12.

Table 12. LPF Bandwidth Selection

EN_LPF_LB_I (Register 0x0060, Bit 0)	EN_LPF_LB_Q (Register 0x0060, Bit 1)	LPF Bandwidth
0	0	1 GHz
0	1	750 MHz
1	0	500 MHz
1	1	250 MHz

From the LPF, the IF or baseband signal passes to a linear output amplifier to drive the baseband output pins (IF_IOUT+, IF_IOUT−, IF_QOUT−, and IF_QOUT+). The IF amplifier provides the overall gain for the ADRF6821 and, with the required 25 Ω series resistors, allows the ADRF6821 to drive a 100 Ω load directly. The ADRF6821 can be interfaced to a variety of analog-to-digital converters (ADCs), and the common-mode output can be adjusted with the external VCM pin. The IF amplifiers are enabled through the EN_IFAMP_I bit (Register 0x0070, Bit 0) and the EN_IFAMP_Q bit (Register 0x0070, Bit 1).

LO GENERATION BLOCK

The ADRF6821 supports the use of both internal and external LO signals for the mixers. The internally generated or externally supplied 2× LO signal is fed to the quadrature divider. The quadrature divider block divides the 2× LO frequency by 2 and then generates two LO signals with a 90° phase difference.

The internal 2× LO is generated by an on-chip VCO, which is tunable over a frequency range of 4000 MHz to 8000 MHz. The output of the VCO is phase locked to an external reference clock through a fractional-N PLL that is programmable through the SPI control registers. To produce 2× LO signals over the 900 MHz to 5600 MHz frequency range to drive the LO divider, steer the VCO outputs through an output divider. Alternatively, an external signal can be used with the dividers to generate the 2× LO signals to the quadrature divider and the demodulators.

Internal LO Mode

For internal LO mode, the ADRF6821 uses the on-chip PLL and VCO to synthesize the frequency of the LO signal. The PLL, shown in Figure 46, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and it is divided down by a value calculated with a reference (R) divider together with a doubler bit and a prescaler bit. Then the divided down reference signal passes to the PFD. The PFD compares this signal to the divided down signal from the VCO. The PFD sends an up or down signal to the charge pump if the VCO signal is slow or fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (V_{TUNE}).

The ADRF6821 integrates multiple VCO cores covering an octave range of 4 GHz to 8 GHz. The suitable VCO is selected with the autotune functionality built into the chip. After the user determines the necessary register values, a write to the INT_L register (Address 0x1200) initiates the autotune process.

LO Frequency and Dividers

The signal coming from the VCO or the external LO inputs passes through a series of dividers before it is buffered to drive the demodulator. The programmable, divide by 2 stages divide the frequency of the incoming signal by 1, 2, 4, and 8 before reaching the quadrature divider that further divides the signal frequency by 2 to generate the in phase and quadrature phase LO signals for the mixers. The LO control bits (OUT_DIVRATIO, Register 0x1414, Bits[4:0]) needed to select the different LO frequency ranges are listed in Table 13.

Table 13. Output Divide Ratio for Frequency Ranges

2× LO Frequency (MHz)	OUT_DIVRATIO (Register 0x1414, Bits[4:0])	VCO Frequency
900 to 1000	01000	(2× LO) × 8
1000 to 2000	00100	(2× LO) × 4
2000 to 4000	00010	(2× LO) × 2
4000 to 5600	00001	(2× LO) × 1

PLL Frequency Programming

The INT, FRAC1, FRAC2, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). Calculate the VCO frequency (VCOOUT) by

$$VCOOUT = f_{PFD} \times N \tag{1}$$

where:
VCOOUT is the output frequency of the VCO (without using the output divider).
f_{PFD} is the frequency of the phase frequency detector. Calculate f_{PFD} by

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \tag{2}$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit (Register 0x120E, Bit 3).
R is the preset divide ratio of the binary 7-bit programmable reference counter, 1 to 255, (Register 0x120C, Bits[6:0]).
T is the REF_{IN} divide by 2 bit, set to 0 or 1, (Register 0x120E, Bit 0).
N is the desired value of the feedback counter. N compromises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD}}{16{,}777{,}216} \tag{3}$$

where:
INT is the 16-bit integer value (23 to 32,767 for the prescaler in 4/5 mode, 75 to 65,535 for the prescaler in 8/9 mode) referenced with Register 0x1201 and Register 0x1200. The recommended setting for the prescaler is 8/9 mode, and it is set by enabling PRE_SEL (Register 0x120B, Bit 1).
FRAC1 is the 24-bit numerator of the primary modulus (0 to 16,777,215) referenced with Register 0x1204, Register 0x1203, and Register 0x1202.
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383) referenced with Register 0x1234, Bits[5:0] and Register 0x1233.
MOD is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383), referenced with Register 0x1209, Bits[5:0] and Register 0x1208.

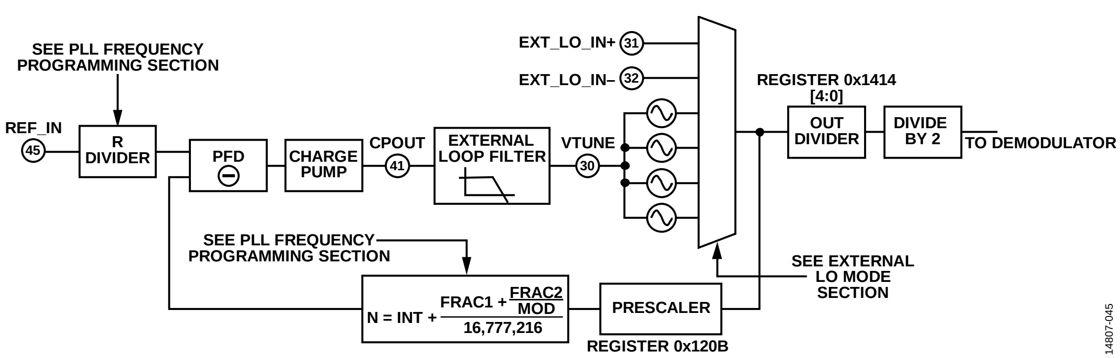

Figure 46. PLL/VCO Block Diagram

Equation 3 results in a very fine frequency resolution with no residual frequency error. To apply this formula, take the following steps:

1. Calculate N by VCOOUT/f_{PFD}.
2. The integer value of this number forms INT.
3. Subtract the INT value from the full N value.
4. Multiply the remainder by 2^{24}.
5. The integer value of this number forms FRAC1.
6. Calculate MOD based on the channel spacing (f_{CHSP}) by

   $$MOD = f_{PFD}/GCD(f_{PFD}, f_{CHSP}) \quad (4)$$

   where:
   $GCD(f_{PFD}, f_{CHSP})$ is the greatest common divider of the PFD frequency and the desired channel spacing frequency.

7. Calculate FRAC2 by the following equation:

   $$FRAC2 = ((N - INT) \times 224 - FRAC1)) \times MOD \quad (5)$$

The FRAC2 and MOD fraction result in outputs with zero frequency error for channel spacings when

$$f_{PFD}/GCD(f_{PFD}/f_{CHSP}) < 16{,}383 \quad (6)$$

where:
f_{PFD} is the frequency of the phase frequency detector.
GCD is a greatest common denominator function.
f_{CHSP} is the desired channel spacing frequency.

After determining the necessary register values for PLL, set the SD_EN_FRAC0 bit (Register 0x122A, Bit 5) to 1. In the integer mode (when FRAC = 0), set the SD_EN_OUT_OFF bit (Register 0x122A, Bit 4) to 1. In the same manner, set the SD_EN_OUT_OFF bit to 0 for fractional mode (that is, when FRAC ≠ 0).

It is recommended to set the charge pump current to be 2.4 mA, by setting the CP_CURRENT bit (Register 0x122E, Bits[3:0]) to 8. With a 20 kHz loop filter, the charge pump current setting results in an optimized performance.

Bleed Setting

The PFD circuitry compares the PFD and divided down VCO signals. The ADRF6821 employs a bleed circuit to put the PFD circuit in the linear operation region. The bleed circuit introduces a delay to the incoming PFD signal, indicated as PFD_OFFSET in Equation 7. Calculate the bleed current, BICP, (Register 0x122F, Bits[7:0]), from the desired PFD_OFFSET, as shown in Equation 7.

$$BICP = Integer(round(float(I_{CP} \times PFD\_OFFSET \times f_{PFD})/960)/255)) \quad (7)$$

where:
I_{CP} is the charge pump current.

The recommended PFD_OFFSET for the 20 kHz loop filter is 2 ns.

PLL Lock Time

The time it takes to lock the PLL after the last register is written into two parts: VCO band calibration and loop settling.

After writing to the last register, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration requires approximately 200 µs. After calibration completes, the feedback action of the PLL causes the VCO to eventually lock to the correct frequency. The speed with which this lock occurs depends on the small signal settling of the loop. Settling time, after calibration, depends on the PLL loop filter bandwidth. With a 20 kHz loop filter bandwidth, settling time is approximately 200 µs.

Lock Detect Control

The ADRF6821 provides two ways of observing lock detection. Lock detection can be monitored from a dedicated register, LOCK_DETECT (Register 0x124D, Bit 0). Lock detection can also be monitored through the dedicated LO_LCKDT pin (Pin 23).

Required PLL/VCO Settings and Register Write Sequence

Configure the PLL registers as described in the PLL Frequency Programming section to achieve the desired frequency, and the last write must be to Register 0x1200 (INT_L). When Register 0x1200 is programmed, an internal VCO calibration initiates, which is the last step to locking the PLL.

External LO Mode

The external LO frequency range is 900 MHz to 5600 MHz and 2× LO signal is used with the internal quadrature divider. To configure for external LO mode, write the following register sequence and apply the differential LO signals to Pin 31 (EXT_LO_IN+) and Pin 32 (EXT_LO_IN−).

Table 14. Register Settings for External LO Mode

Register	Required Value	Description
0x120B	0x00	Disable feedback divider
0x122D	0x00	Disable PFD and charge pump (CP)
0x1240	0x03	Disable VCO adjust
0x1217	0x00	Set VCO select to a low value
0x121F	0x40	Disable calibration
0x1021	0xD8	Disable PLL blocks
0x1414	0xA1	Use external LO

The EXT_LO_IN+ and EXT_LO_IN− input pins must be ac-coupled. When not in use, leave the EXT_LO_IN+ and EXT_LO_IN− pins unconnected.

Quadrature Divider

The quadrature divider block divides the 2× LO frequency generated by either the internal PLL and VCO or the external input by 2. Next, the quadrature divide block generates two LO signals with a 90° phase difference. To enable the divider, disable the bits, EN_IBIASGEN (Register 0x0090, Bit 0), EN_DIVPATH_BUF (Register 0x0090, Bit 1), and EN_DIVPATH_QUADDIV (Register 0x0090, Bit 2). Two separate LO drivers take these LO signals and feed them to the mixers. LO driver paths are enabled via the following registers:

- EN_LODRV_DRVI (Register 0x0090, Bit 3)
- EN_LODRV_DRVQ (Register 0x0090, Bit 4)
- EN_LODRV_PREDRVI (Register 0x0090, Bit 5)
- EN_LODRV_PREDRVQ (Register 0x0090, Bit 6)

REGISTER WRITE SEQUENCE

The proper register write sequence starts with locking the LO frequency or enabling the external LO inputs. After ensuring that the local oscillator is locked in either the internal PLL/VCO or the external LO source, enable the LO_OE bit (Register 0x1414, Bit 6). After enabling the LO_OE bit, the RF and IF blocks can be enabled as defined in the Theory of Operation section.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI of the ADRF6821 allows the user to configure the device for specific functions or operations through a structured register space provided inside the chip. This interface provides users with added flexibility and customization. Addresses are accessed via the SPI and can be written to or read from the SPI.

The serial peripheral interface consists of four control lines: SCLK, SDIO, SDO, and $\overline{CS}$. The serial clock (SCLK) is the serial shift clock, and it synchronizes the serial interface reads and writes. SDIO is the serial data input or the serial data output depending on the instruction sent and the relative position in the timing frame. Chip select bar ($\overline{CS}$) is an active low control that gates the read and write cycles. The falling edge of $\overline{CS}$ in conjunction with the rising edge of SCLK determines the start of the frame. When $\overline{CS}$ is high, all SCLK and SDIO activity is ignored. See Table 6 for the serial timing and its definitions.

The ADRF6821 protocol consists of a read/write followed by 16 register address bits and 8 data bits. Both the address and data fields are organized with the most significant bit (MSB) first and end with the least significant bit (LSB).

The SPI and general-purpose input/output (GPIO) interfaces of the ADRF6821 provides two options for the logic voltage levels, 1.8 V and 3.3 V. The interfaces use 1.8 V logic levels as the default. Enable SPI_18_33_SEL (Register 0x0020, Bit 0) and SPI_1P8_3P3_CTRL (Register 0x1401, Bit 4) for 3.3 V compatible logic levels. See Table 6 for the SPI specifications.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

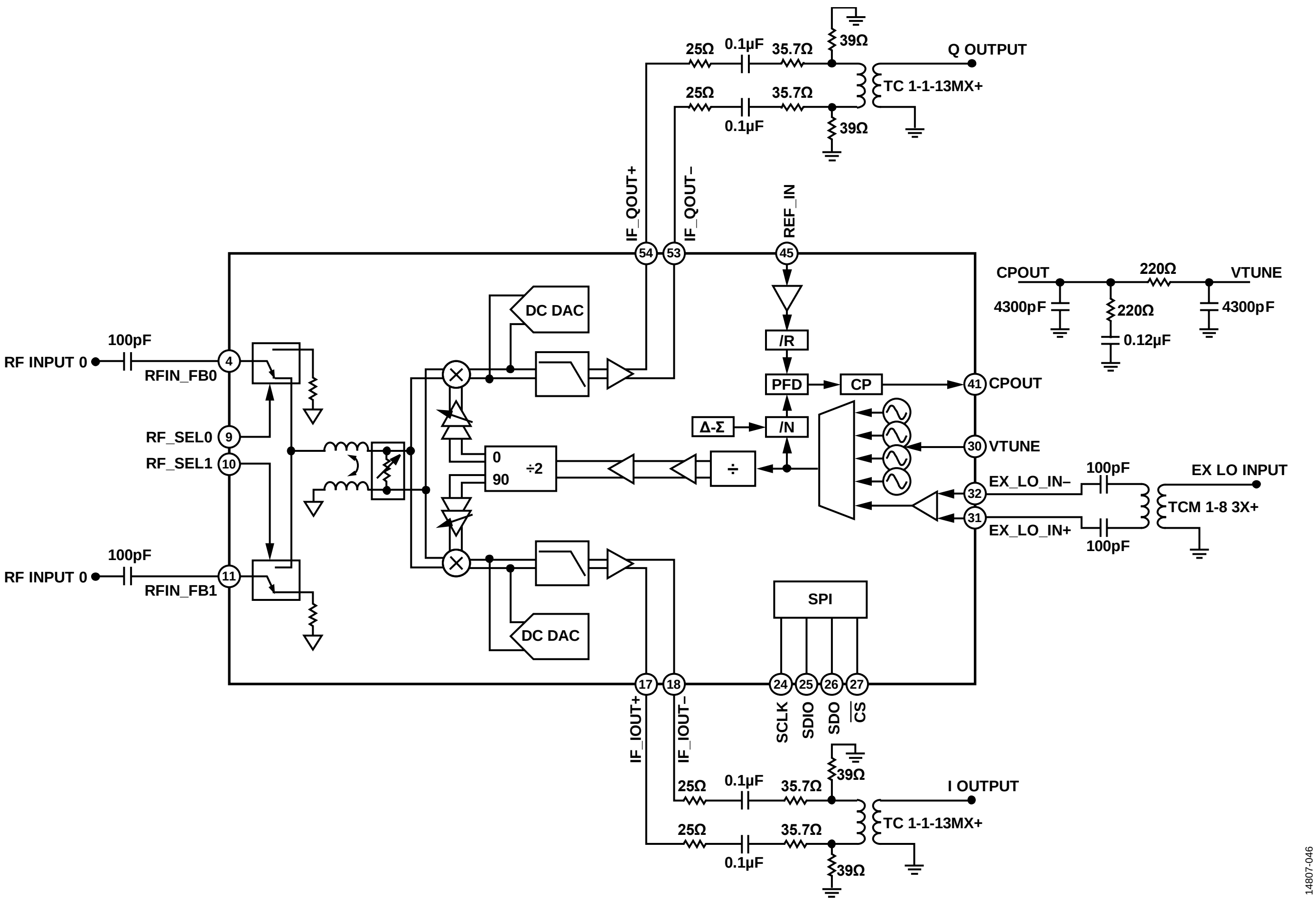

Figure 47. Typical Application Circuit

Table 15. Typical Connections

Pin No.	Mnemonic	Description	Basic Connection
RF Inputs			
4, 11	RFIN_FB0, RFIN_FB1	RF inputs	The single-ended RF inputs have a 50 Ω impedance. These pins must be ac-coupled. Terminate unused RF inputs with a dc blocking capacitor to ground to improve isolation. Refer to the Layout section for the recommended PCB layout.
RF Balun Optimization			
7	RFBT_FB	RF balun tuning inductor	Connect the balun tuning inductor (L_{TUNE}) to ground.
GPIOs			
9, 10	RF_SEL0, RF_SEL1	RF select control pins	Active high. 1.8 V and 3.3 V logic level compatible. See the Theory of Operation section for RF select pin use.
13	SLEEP	Sleep mode enable pin	Active high. 1.8 V and 3.3 V logic level compatible.

Pin No.	Mnemonic	Description	Basic Connection
3.3 V RF/IF Power			
15, 56	VCC_3V3_I, VCC_3V3_Q	Supply for DSA and RF switches	Decouple these power supply pins to ground using 100 pF, 0.1 μF, and 10 μF capacitors. Place the decoupling capacitors close to these pins.
6, 8	VCC_LO1, VCC_LO2	LO path to mixer supply	Decouple these power supply pins to ground using 100 pF and 0.1 μF capacitors. Place the decoupling capacitors close to these pins.
22, 49	VCC_IFMIX_I, VCC_IFMIX_Q	Mixer supply	
20, 51	VCC_IFMIX_I, VCC_IFMIX_Q	IF amplifier supply	
VCM Input			
1, 14	VCM_Q, VCM_I	VCM adjust pins	Decouple the VCM input pins to ground using 100 pF and 0.1 μF capacitors and connect these pins to the same supply domain as the VCC_IFMIX_Q and VCC_IFMIX_I pins. Place the decoupling capacitors close to the pins. Place a resistive divider to divide the supply voltage into two. Use 5.1 kΩ (or similar) for resistive divider component values.
Decoupling			
2	VDD_DIG	Decoupling pin for the internal LDO to supply the internal digital circuits	Decouple these pins to ground using 100 pF and 0.1 μF capacitors. Place the decoupling capacitors close to these pins.
21, 50	VDCPL_I, VDCPL_Q	Decoupling pins for I and Q channels	
IF Outputs			
17, 18, 53, 54	IF_IOUT+, IF_IOUT−, IF_QOUT−, IF_QOUT+	I and Q outputs	Place 25 Ω resistors in series for each differential leg. The differential I/Q output impedance together with the series 25 Ω resistors becomes 60 Ω. For optimized performance, the 60 Ω output impedance must be terminated with a 100 Ω load.
3.3 V PLL/VCO Power			
33	VCCVCO_3V3	VCO 3.3 V supply	Decouple these power supply pins to ground using 100 pF and 0.1 μF capacitors. Place the decoupling capacitors close to the pins. Employ ferrite beads to provide isolation between the PLL/VCO supply pins. Beware of the series resistance of the ferrite beads and try to minimize the voltage drop.
34	VCCDIV_3V3	LO chain and divider 3.3 V supply	
35	VCCFBDIV_3V3	PLL feedback divider 3.3 V supply	
36	VCCLO_MIX_3V3	LO mixer output buffer 3.3 V supply	
37	VCCLO_AUX_3V3	LO external output buffer 3.3 V supply	
42	VCCCP_3V3	Charge pump 3.3 V supply	
43	VCCPFD_3V3	PFD 3.3 V supply	
44	VCCREF_3V3	Reference input buffer 3.3 V supply	
48	VBAT_DIG_3V3	SPI and SDM LDO 3.3 V supply	
PLL/VCO			
23	LO_LCKDT	LO lock detect	
29	DCL_BIAS	VCO core bias decouple	Decouple this pin to ground using a 0.1 μF capacitor.
30	VTUNE	V_{TUNE} input	This pin is driven by the output of the loop filter; its nominal input voltage range is 1.5 V to 2.5 V.
41	CPOUT	Charge pump output	Connect this pin to the VTUNE pin through the loop filter.
45	REF_IN	Reference input buffer	The nominal input level of this pin is 1 V p-p. The input range is 10 MHz to 250 MHz. This pin is internally biased and must be ac-coupled and terminated externally with a 50 Ω resistor. Place the ac coupling capacitor between the pin and

Pin No.	Mnemonic	Description	Basic Connection
			the resistor.
46	SPILDO_OUT_1V8	SPI 1.8 V LDO external decouple output	Decouple these pins to ground using 100 pF and 0.1 μF capacitors. Place the decoupling capacitors close to the pins.
47	SDMLDO_OUT_1V8	SDM 1.8 V LDO external decouple output	
Auxiliary LO Output			
38, 39	LO_OUT+, LO_OUT−	LO outputs	The differential output impedance of the buffer of the LO outputs is 50 Ω.
External LO Inputs			
31, 32	EXT_LO_IN+, EXT_LO_IN−	External LO inputs	The differential input impedance of the buffer of the external LO inputs is 100 Ω.
Serial Peripheral Interface			
24	SCLK	SPI clock	1.8 V and 3.3 V compatible logic levels.
25	SDIO	SPI data input/output in 3-wire mode and SPI data input in for 4-wire mode	1.8 V and 3.3 V compatible logic levels.
26	SDO	SPI data output for 4-wire mode and this pin is not used for 3-wire mode	1.8 V and 3.3 V compatible logic levels.
27	$\overline{\text{CS}}$	SPI chip select	Active low; 1.8 V and 3.3 V compatible logic levels
Reset			
28	$\overline{\text{RST}}$	Reset	Active low; 1.8 V and 3.3 V compatible logic levels
Ground			
3, 5, 12, 16, 19, 52, 55	GND	Ground	Connect these pins to the ground of the PCB.
40	GND	Charge pump ground	Do not connect this pin to the paddle ground, connect this pin to the PCB ground.
Exposed Pad	EPAD	Exposed Pad	The exposed pad is on the bottom of the package. The exposed pad must be soldered to ground.

LOW-PASS FILTER BANDWIDTH SELECTION

The ADRF6821 incorporates an on-chip, third-order, low-pass filter (LPF) between the demodulator and the output buffer. The filter has four different bandwidth settings. The EN_LPF_LB_I (Register 0x0060, Bit 0) and the EN_LPF_LB_Q (Register 0x0060, Bit 1) bits enable various LPF bandwidth modes, as detailed in Table 12.

The ADRF6821 incorporates a wideband buffer at the I and Q outputs that poses a challenge for the linearity of the overall RFIC. For RF and LO frequencies lower than 1000 MHz, the mixing product, RF + LO, is amplified by the wideband buffer and, in turn, deteriorates the overall linearity. The on-chip LPF can improve the leakage rejection of the high frequency mixing product. Depending on the I/Q bandwidth requirement of the system, the LPF can be set to lower bandwidths to provide rejection at RF and LO frequencies. Table 16 can determine the LPF bandwidth according to RF and LO frequency of operation.

Table 16. LPF Bandwidth Selection for Various RF and LO Frequencies

LO Frequency (MHz)	LPF Bandwidth Setting (MHz)	EN_LPF_LB_I, EN_LPF_LB_Q
450 to 1000	250	1, 1
1000 to 1200	500	1, 0
1200 to 2000	750	0, 1
2000 to 2800	1000	0, 0

Moreover, the on-chip LPF can improve the RF to IF and LO to IF leakage performance for RF and LO frequencies higher than 1 GHz. However, note the gain flatness degradation with the use of various LPF settings (see Figure 48).

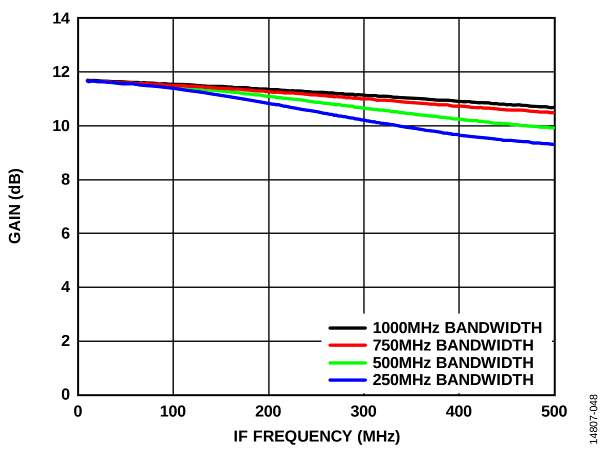

Figure 48. Gain vs. IF Frequency for Various Low-Pass Filter Settings, LO = 2000 MHz

Figure 49 and Figure 50 illustrate the effect of the LPF on the RF to IF leakage and LO to IF leakage.

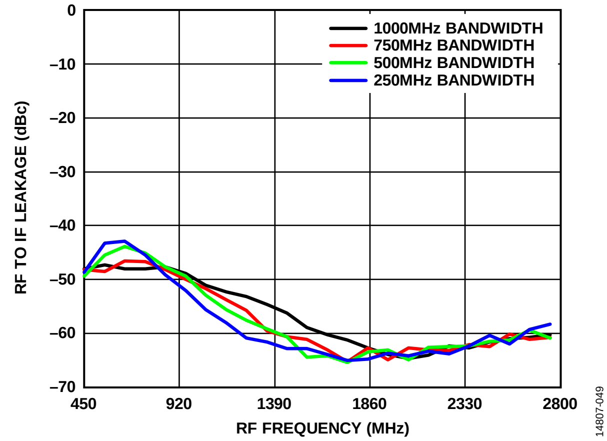

Figure 49. RF to IF Rejection for RF Frequency at 100 MHz and a Low-Pass Filter Setting of 250 MHz

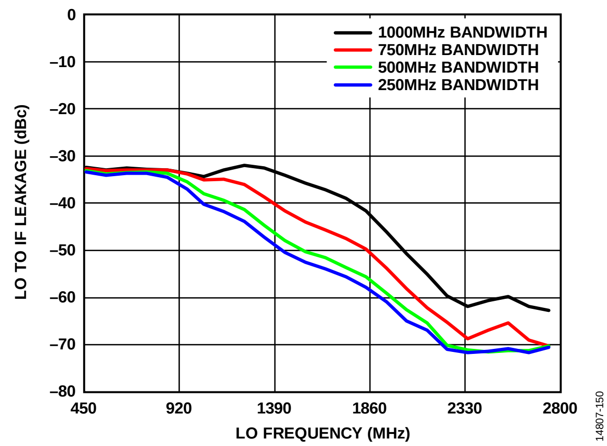

Figure 50. LO to IF Rejection for LO Frequency at 100 MHz and a Low-Pass Filter Setting of 250 MHz

I/Q OUTPUT LOADING

By design, the ADRF6821 has an I/Q output impedance of 10 Ω and it is optimized to perform with an external 25 Ω in each differential leg. External resistors increase the output impedance and with the external 25 Ω, the total differential output impedance equals 60 Ω. When terminated with a 100 Ω differential load, the return loss is less than −10 dB for a wide range of IF frequencies.

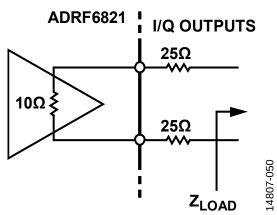

Figure 51. IF Output Schematic

Different application circuits can require various loading conditions for the I and Q outputs. Therefore, it is important to understand the effect of I and Q output loading on the performance characteristics, such as output IF gain, output IP3, output IP2, HD2 and HD3. Figure 53 to Figure 55 illustrates the effect of output loading on these characteristics.

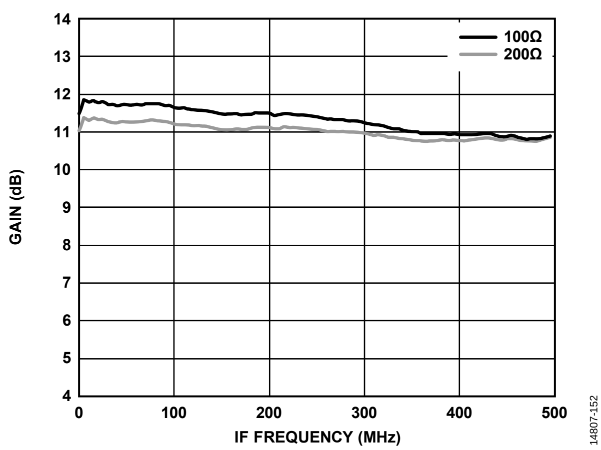

Figure 52. Gain vs. IF Frequency for Different Loads

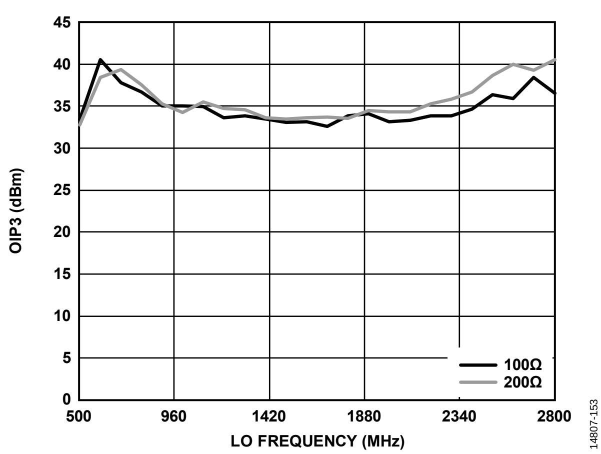

Figure 53. Output IP3 (OIP3) vs. LO Frequency for Different Loads

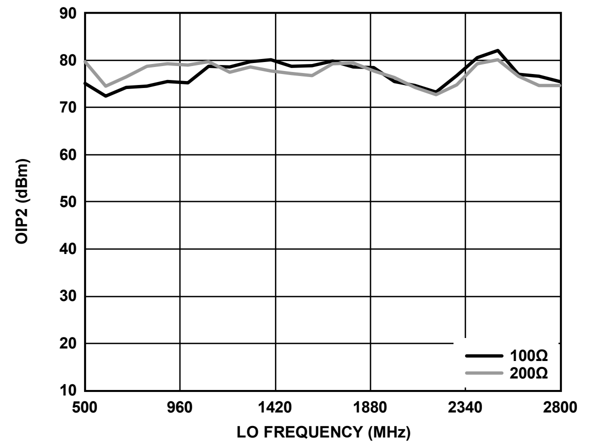

Figure 54. Output IP2 (OIP2) vs. LO Frequency for Different Loads

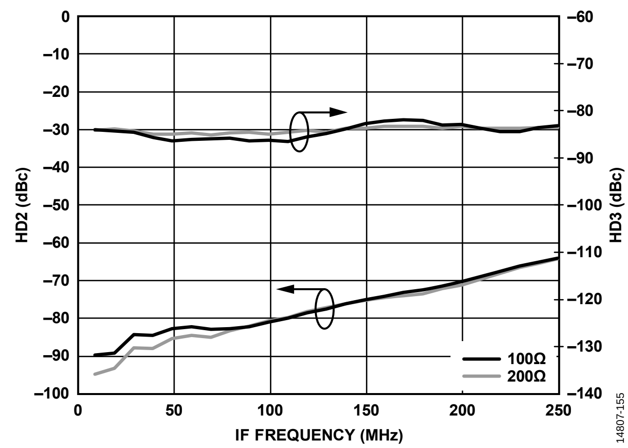

Figure 55. HD2 and HD3 vs. IF Frequency for Different Loads

ANALOG-TO-DIGITAL CONVERTER (ADC) INTERFACING

The ADRF6821 perfectly suits in a zero IF receiver chain. The integrated IF amplifier of the ADRF6821 provides variable and sufficient drive capabilities for both buffered and unbuffered ADCs. It also provides isolation between the sampling edges of the ADC and the mixer core. As a result, an antialiasing low-pass filter is sufficient when interfacing with an ADC.

The filter resides between the ADRF6821 and the ADC. The low-pass filter eliminates all out of band signals that may alias onto the actual band and degrade the performance of the ADRF6821 and the ADC pair. Selection of the low-pass filter center and bandwidth is application specific. Take into account the trade-off between the amount of rejection required and the insertion loss to choose the order of the filter. A higher order filter also requires more layout space, which is another design criterion.

For the purposes of ADC interfacing, consider a DPD receiver chain, correcting for a 70 MHz bandwidth signal. Assuming a fifth-order correction, 350 MHz from the output of the power amplifier must be sampled. With the use of a zero-IF receiver, I and Q bandwidths are half of the 350 MHz, that is, 175 MHz. Next, determine the sampling rate of the ADC. To relax the antialiasing filter requirements, use a slightly oversampled system. Considering the bandwidth of interest for I and Q (that is, 175 MHz), 500 MSPS is a sufficiently large sampling rate. With a 500 MSPS sampling rate, the second Nyquist zone lies between 250 MHz and 500 MHz. Because there are no interferers present in a DPD chain, only the replica of the signal of interest in the second Nyquist zone (between 325 MHz and 500 MHz) is of concern. As a result, the antialiasing filter provides sufficient attenuation starting from 325 MHz.

The required attenuation from the filter is determined with the dynamic range requirement. As previously mentioned, in a DPD receiver chain, ideally only the signal of interest is present. Therefore, the filter requirements can be relaxed further. Because of this, consider a 40 dB rejection at the aliased portion.

Considering the pass band, the stop band, and the attenuation at stop band, a seventh-order Chebyshev low-pass filter is suitable with a 0.1 dB ripple in-band. Keep in mind that the ADRF6821 is optimized with a 100 Ω load at the output. Therefore, design the filter for an input and output impedance of differential 100 Ω. The Chebyshev filter design is discussed extensively and is straightforward with the use of a filter wizard, such as ADS built-in filter design tool from Keysight. Filter design tools provide component values that are not necessarily commercially available. It is recommended that designers use commercially available component models and take into account the layout effects. Figure 56 displays the component values for the antialiasing LPF. Table 17 provides commercially available component values for the low-pass filter design.

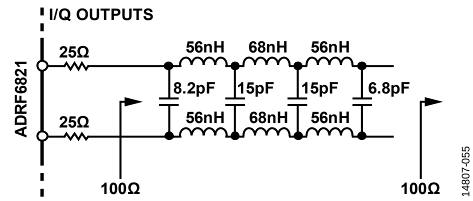

Figure 56. Low-Pass Filter Schematic

Table 17. Component Values for the Low-Pass Filter Design (1 dB Corner Frequency of 150 MHz)

Parameter	Value	Type	Manufacturer
Inductors	56 nH	0402 CS	Coilcraft
	68 nH	0402 CS	Coilcraft
Capacitors	8.2 pF	0402 C0G	Murata
	6.8 pF	0402 C0G	Murata
	15 pF	0402 C0G	Murata

Figure 57 compares the measured low-pass filter response and the normalized gain of the ADRF6821 LPF pair. Refer to the highest gain of the ADRF6821 (without the low-pass filter) to acheive normalization. The in band roll-off is associated to the finite Q and trace and pad losses.

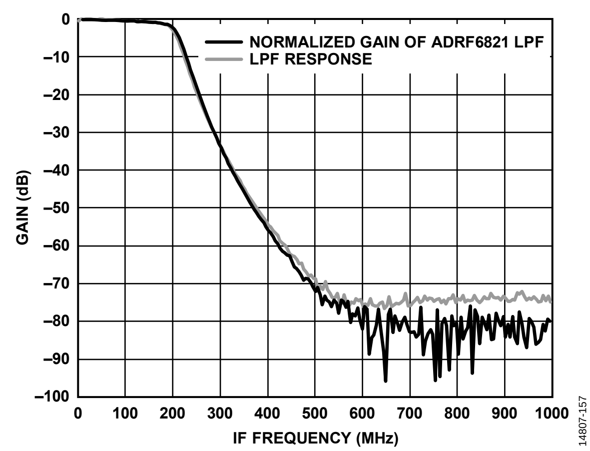

Figure 57. Frequency Response for the 150 MHz Low-Pass Filter and Frequency Response for ADRF6821 LPF Pair

IMAGE REJECTION

For direct conversion systems, maximizing image rejection is key to achieving performance and optimizing bandwidth. The amplitude and phase mismatch of the baseband I and Q paths directly translates to degradation in image rejection, as is shown in the following equation. The equation translates the gain and quadrature phase mismatch to the image rejection ratio (IRR) performance.

$$IRR\,(\text{dB}) = 10\log\frac{\left|1 + A_e^2 + 2A_e\cos(\varphi_e)\right|}{1 + A_e^2 + 2A_e\cos(\varphi_e)}$$

where:
A_e is the amplitude error and is shown in Figure 58 for various LO frequencies.
φ_e is the phase error and is shown in Figure 59 for various LO frequencies.

The image rejection calculated with the given phase and gain mismatches is shown in Figure 60.

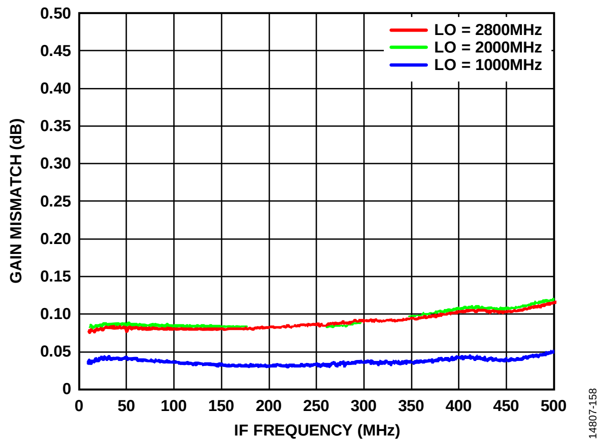

Figure 58. Gain Mismatch (Error) Between I and Q Outputs vs. IF Frequency

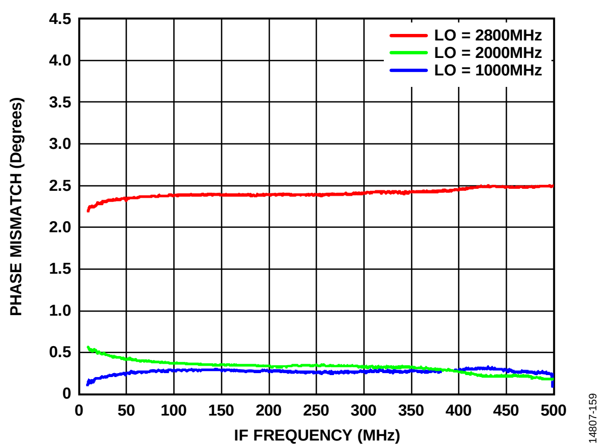

Figure 59. Phase Mismatch (Error) Between I and Q Outputs vs. IF Frequency

One of the dominant sources of phase error in a system originates from the demodulator where the quadrature phase split of the LO signal occurs. The ADRF6821 offers phase and gain adjustment of the I and Q paths independently to allow quadrature correction. Adjusting the phase with the TRM_LODRV_CAPI bits (Register 0x0092, Bits[3:0]) for the I path correction and the TRM_LODRV_CAPQ bits (Register 0x0092, Bits[7:4]) for the Q path correction accesses the quadrature correction. Adjust the I_MIXER_GAIN_ADJ bits (Register 0x003A, Bits[3:2]) and the Q_MIXER_GAIN_ADJ bits (Register 0x003A, Bits[5:4]) for the I and Q outputs, respectively, to achieve gain correction. Figure 60 shows uncalibrated and calibrated image rejection for an LO frequency of 2800 MHz and across temperature.

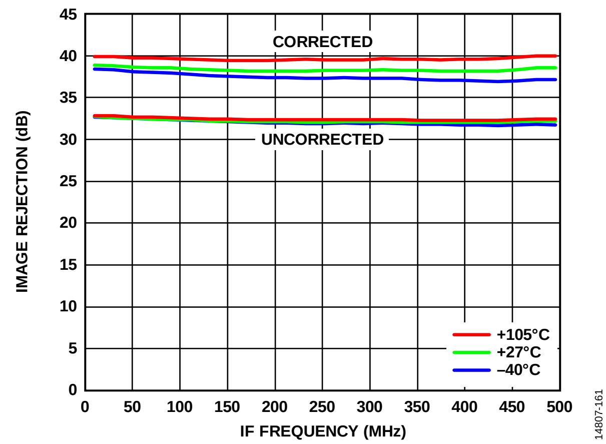

Figure 60. Corrected and Uncorrected Image Rejection vs. IF Frequency for Various Temperatures, f_{LO} = 2800 MHz

For any correction circuit, it is important to observe the effect of temperature on the correction level and settings. Figure 61 shows how the correction with a given phase and gain setting holds across temperature.

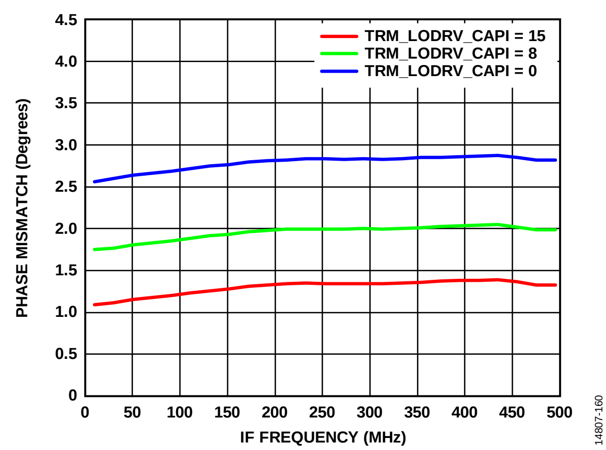

Figure 61. Phase Mismatch vs. IF Frequency (f_{LO} = 2800 MHz) for Various Phase Setting Values

POWER SUPPLY CONFIGURATION

The ADRF6821 incorporates two main supply domains, namely RF/IF and PLL/VCO. The RF/IF supply domain includes the supplies related to the RF switch, the DSA, the mixer, the mixer LO drivers, and the IF amplifier. The PLL/VCO supply domain includes the PFD/CP, the VCO, the dividers, and the output drivers.

RF/IF Supply Domain

Connect the RF/IF supply domain pins together with beads in between and decoupling capacitors specific to each pin as shown in Figure 62. The RF/IF supply pins draw a combined 350 mA approximately. For the RF/IF supply domain, the ADRF6821 evaluation board employs the ADM7170, a low noise and high power supply rejection ratio (PSRR) linear regulator that is capable of delivering 500 mA.

The power supply rejection (PSR) of the RF/IF supply pins allow the use of a switching supply to reduce the power consumption on the linear regulators. The ADRF6821 evaluation board includes the ADP2370 switching regulator and allows the observation of the operation with a switching supply. The ADP2370 is a low quiescent current buck regulator capable of delivering an output current of 800 mA with a selectable switching frequencies of 600 kHz and 1.2 MHz. See the ADRF6821-EVALZ user guide on how to configure the switching supply for RF/IF domain.

PLL/VCO Supply Domain

The PLL/VCO supply domain requires specific attention; otherwise, performance degradation can result. The ADRF6821 incorporates an ultralow noise PLL and VCO that are sensitive to any noise and/or frequency component at the supply pins. These unwanted noise and frequency components degrade the performance of the overall system. To avoid performance degradation, the ADRF6821 evaluation board employs the PLL/VCO supply domain circuit shown in Figure 63. The supply circuit in Figure 63 uses the HMC1060, an ultralow noise, LDO with four isolated outputs. Noise performance and isolated outputs make the HMC1060 an ideal solution for the PLL/VCO supply domain. For additional configuration options, refer to the ADRF6821-EVALZ user guide.

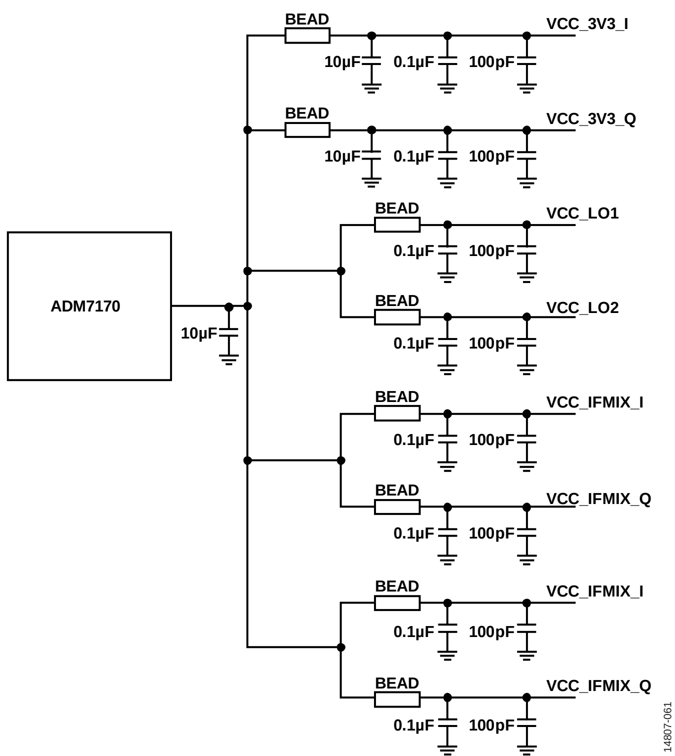

Figure 62. RF/IF Domain Power Supply Circuit

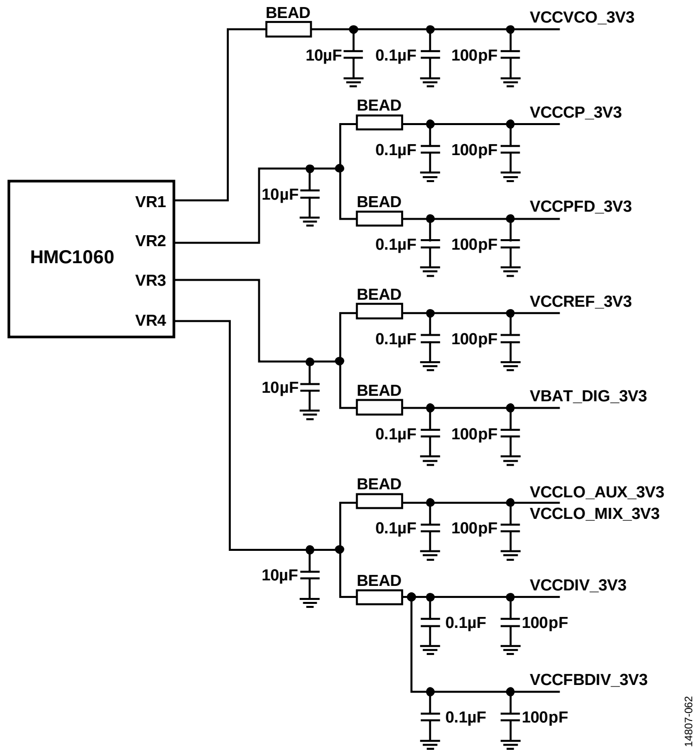

Figure 63. PLL/VCO Domain Power Supply Circuit

LAYOUT

Careful layout of the ADRF6821 is necessary for optimizing performance and minimizing stray parasitics. Because the ADRF6821 supports two channels, the layout of the RF section is critical in achieving isolation between channels. Figure 64 shows the recommended layout for the RF inputs. The best layout approach is to keep the traces short and direct. In addition, for improved isolation, do not route the RF input traces in parallel to each other and spread the traces immediately after each one leaves the pins. Keep the traces as far away from each other as possible (and at an angle, if possible) to prevent cross coupling.

The input impedance of the RF inputs is 50 Ω, and the traces leading to the pin must have a 50 Ω characteristic impedance. Terminate the unused RF inputs with a dc blocking capacitor to ground.

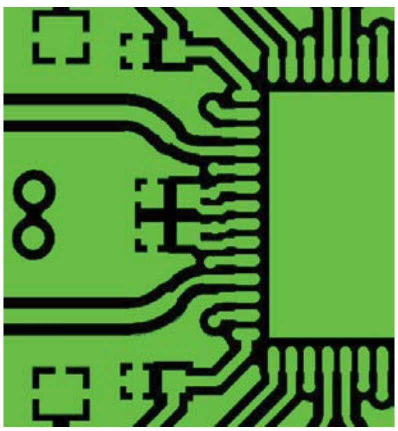
14807-063

Figure 64. RF/IF Domain Layout

The ADRF6821 incorporates a very low noise PLL/VCO and care must be taken when designing the PCB routing around the PLL/VCO pins. It is required to put the decoupling capacitors for the supply pins as close as possible. If 0402 capacitors are used, putting all of the decoupling capacitors close to the pin becomes problematic. In such a case, place the smaller value decoupling capacitor as close as possible to the pin. It is a good practice to keep the first capacitor of the loop filter close to the CPOUT pin, and the last capacitor close to the VTUNE pin, as can be seen in Figure 65.

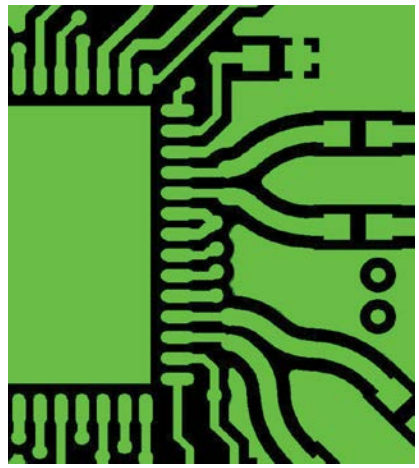
14807-064

Figure 65. PLL/VCO Domain Layout

REGISTER MAP AND REGISTER DESCRIPTIONS

Register addresses not listed in Table 18 are reserved, unused, or open registers.

Table 18.

Reg Addr (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0000	ADI_SPI_CONFIG	[7:0]	SOFTRESET_	LSB_FIRST_	ENDIAN_	SDOACTIVE_	SDOACTIVE	ENDIAN	LSB_FIRST	SOFTRESET	0x00	R/W
0001	SPI_CONFIG_B	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	MASTER_SLAVE_RB	RESERVED		SOFT_RESET		MASTER_SLAVE_TRANSFER	0x00	R/W
0003	CHIPTYPE	[7:0]	CHIPTYPE								0x01	R
0004	PRODUCT_ID_L	[7:0]	PRODUCT_ID, Bits[7:0]								0x13	R
0005	PRODUCT_ID_H	[7:0]	PRODUCT_ID, Bits[15:8]								0x00	R
000A	SCRATCHPAD	[7:0]	SCRATCHPAD								0x00	R/W
000B	SPI_REV	[7:0]	SPI_REV								0x00	R
000C	VENDOR_ID_L	[7:0]	VENDOR_ID, Bits[7:0]								0x56	R
000D	VENDOR_ID_H	[7:0]	VENDOR_ID, Bits[15:8]								0x04	R
0020	MASTER_CONFIG	[7:0]	RESERVED						EN_ANALOG_MASTER	SPI_18_33_SEL	0x00	R/W
0030	RF_SWITCH	[7:0]	RESERVED	SEL_RFSW_SPI_CONTROL	RFSW_SEL1	RFSW_SEL0	RFSW_SEL1_IN	RFSW_SEL0_IN	ENB_SW_1P8_GEN	EN_SW	0x00	R/W
0031	DSA_CONTROL	[7:0]	RESERVED		ATTEN_DSA				ENB_DSA_1P8_GEN	EN_DSA	0x00	R/W
0032	DEMOD_ENABLES	[7:0]	RESERVED		EN_IMXBIAS_Q	EN_IMXBIAS_I	EN_MIXIBIASGEN	EN_MIX_Q	EN_MIX_I	ENB_MIX_1P8_GEN	0x00	R/W
0033	DEMOD_LO_COM_CTRL	[7:0]	CODE_MIXER_DRVR								0x00	R/W
0034	DEMOD_OUT_COM_CTRL	[7:0]	CODE_MIXER_OCM								0x00	R/W
003A	DEMOD_SPARES	[7:0]	RESERVED		Q_MIXER_GAIN_ADJ		I_MIXER_GAIN_ADJ		MIXER_GAIN_PEAK		0x00	R/W
0040	DEMOD_DRIVER_COM_CTRL	[7:0]					EN_ICMLOBIAS_Q	EN_ICMLOBIAS_I	EN_ICMOBIAS_Q	EN_ICMOBIAS_I	0x00	R/W
0050	DC_CTRL	[7:0]	RESERVED					EN_DC_DAC_Q	EN_DC_DAC_I	ENB_DCCOMP_1P8_GEN	0x00	R/W
0051	DC_COMP_I_CHAN_RF0	[7:0]	CODE_DC_IDAC_RF0								0x00	R/W
0052	DC_COMP_Q_CHAN_RF0	[7:0]	CODE_DC_QDAC_RF0								0x00	R/W
0053	DC_COMP_I_CHAN_RF1	[7:0]	CODE_DC_IDAC_RF1								0x00	R/W
0054	DC_COMP_Q_CHAN_RF1	[7:0]	CODE_DC_QDAC_RF1								0x00	R/W
0060	LPF_BW_SEL	[7:0]	RESERVED						SEL_LPF_BW_LSB	SEL_LPF_BW_MSB	0x00	R/W
0070	IF_AMP_CTRL	[7:0]	RESERVED						EN_IFAMP_Q	EN_IFAMP_I	0x00	R/W
0080	LO_CTRL	[7:0]	RESERVED					SEL_LODRV_PREDRVQ_POL	SEL_LODRV_PREDRVI_POL	RESERVED	0x00	R/W
0090	EN_LO_DIVIDER_CTRL	[7:0]	RESERVED	EN_LODRV_PREDRVQ	EN_LODRV_PREDRVI	EN_LODRV_DRVQ	EN_LODRV_DRVI	EN_DIVPATH_QUADDIV	EN_DIVPATH_BUF	EN_IBIASGEN	0x00	R/W
0092	LO_PHASE_ADJ	[7:0]	TRM_LODRV_CAPQ				TRM_LODRV_CAPI				0x00	R/W
1021	BLOCK_RESETS	[7:0]	RESERVED	ARSTB_BLOCK_LKD	ARSTB_BLOCK_AUTOCAL	ARSTB_BLOCK_NDIV	ARSTB_BLOCK_RDIV	ARSTB_BLOCK_DSMOSTG	ARSTB_BLOCK_DSMCORE	ARSTB_BLOCK_DSMALL	0xFF	R/W
1109	SIG_PATH_9_NORMAL	[7:0]	RESERVED			TRM_MIXLODRV_DRV_POUT		TRM_XLODRV_DRV_POUT		RESERVED	0x0A	R/W

Reg Addr (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
1200	INT_L	[7:0]	INT_DIV, Bits[7:0]								0x89	R/W
1201	INT_H	[7:0]	INT_DIV, Bits[15:8]								0x01	R/W
1202	FRAC1_L	[7:0]	FRAC, Bits[7:0]								0x00	R/W
1203	FRAC1_M	[7:0]	FRAC, Bits[15:8]								0x00	R/W
1204	FRAC1_H	[7:0]	FRAC, Bits[23:16]								0x00	R/W
1205	SD_PHASE_L_0	[7:0]	PHASE, Bits[7:0]								0x00	R/W
1206	SD_PHASE_M_0	[7:0]	PHASE, Bits[15:8]								0x00	R/W
1207	SD_PHASE_H_0	[7:0]	PHASE, Bits[23:16]								0x00	R/W
1208	MOD_L	[7:0]	MOD2, Bits[7:0]								0x00	R/W
1209	MOD_H	[7:0]	RESERVED		MOD2, Bits[13:8]						0x00	R/W
120B	SYNTH	[7:0]	RESERVED						PRE_SEL	EN_FBDIV	0x01	R/W
120C	R_DIV	[7:0]	RESERVED	R_DIV							0x03	R/W
120E	SYNTH_0	[7:0]	RESERVED				DOUBLER_EN	RESERVED		RDIV2_SEL	0x04	R/W
1214	MULTI_FUNC_SYNTH_CTRL_0214	[7:0]	LD_BIAS		LDP			RESERVED			0x48	R/W
1215	SI_BAND_0	[7:0]	SI_BAND_SEL								0x00	R/W
1217	SI_VCO_SEL	[7:0]	RESERVED				SI_VCO_SEL				0x00	R/W
121C	VCO_TIMEOUT_L	[7:0]	VCO_TIMOUT[7:0]								0x20	R/W
121D	VCO_TIMEOUT_H	[7:0]	RESERVED						VCO_TIMEOUT[9:8]		0x00	R/W
121E	VCO_BAND_DIV	[7:0]	VCO_BAND_DIV								0x14	R/W
121F	VCO_FSM	[7:0]	RESERVED	DISABLE_CAL	RESERVED						0x00	R/W
122A	SD_CTRL	[7:0]	RESERVED		SD_EN_FRAC0	SD_EN_OUT_OFF	RESERVED		SD_SM_2	RESERVED	0x02	R/W
122C	MULTI_FUNC_SYNTH_CTRL_022C	[7:0]	RESERVED						CP_HIZ		0x03	R/W
122D	MULTI_FUNC_SYNTH_CTRL_022D	[7:0]	EN_PFD_CP	BLEED_POL	RESERVED			INT_ABP	RESERVED	BLEED_EN	0x81	R/W
122E	CP_CURR	[7:0]	RESERVED				CP_CURRENT				0x0F	R/W
122F	BICP	[7:0]	BICP								0x08	R/W
1233	FRAC2_L	[7:0]	FRAC2, Bits[7:0]								0x00	R/W
1234	FRAC2_H	[7:0]	RESERVED		FRAC2, Bits[13:8]						0x00	R/W
1235	MULTI_FUNC_SYNTH_CTRL_0235	[7:0]	RESERVED						PHASE_ADJ_EN	RESERVED	0x00	R/W
1240	VCO_LUT_CTRL	[7:0]	RESERVED			SI_VCO_FORCE_CAPSVCOI	RESERVED		SI_VCO_FORCE_VCO	SI_VCO_FORCE_CAPS	0x00	R/W
124D	LOCK_DETECT	[7:0]	RESERVED							LOCK_DETECT	0x00	R
1401	MULTI_FUNC_CTRL	[7:0]	RESERVED			SPI_1P8_3P3_CTRL	RESERVED				0x00	R/W
140E	LO_CNTRL2	[7:0]	EN_BIAS_R	RESERVED	REFBUF_EN	RESERVED					0xB3	R/W
1414	LO_CNTRL8	[7:0]	MIX_OE	LO_OE	USEEXT_LOI	OUT_DIVRATIO					0x02	R/W
1541	FRAC2_L_SLAVE	[7:0]	FRAC2_SLV, Bits[7:0]								0x00	R
1542	FRAC2_H_SLAVE	[7:0]	RESERVED		FRAC2_SLV, Bits[13:8]						0x00	R
1543	FRAC_L_SLAVE	[7:0]	FRAC_SLV, Bits[7:0]								0x00	R
1544	FRAC_M_SLAVE	[7:0]	FRAC_SLV, Bits[15:8]								0x00	R
1545	FRAC_H_SLAVE2	[7:0]	FRAC_SLV, Bits[23:16]								0x00	R

Reg Addr (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
1546	PHASE_L_ SLAVE	[7:0]	PHASE_SLV, Bits[7:0]								0x00	R
1547	PHASE_ M_SLAVE2	[7:0]	PHASE_SLV, Bits[15:8]								0x00	R
1548	PHASE_ H_SLAVE3	[7:0]	PHASE_SLV, Bits[23:16]								0x00	R
1549	INT_DIV_ L_SLAVE	[7:0]	INT_DIV_SLV, Bits[7:0]								0x89	R
154A	INT_DIV_ H_SLAVE	[7:0]	INT_DIV_SLV, Bits[15:8]								0x01	R
154B	R_DIV_ SLAVE	[7:0]	RESERVED	R_DIV_SLV							0x03	R
154C	RDIV2_ SEL_SLAVE	[7:0]	RESERVED							RDIV2_SEL_SLV	0x00	R
1583	DISABLE_ CFG	[7:0]	RESERVED			DSM_LAUNCH_DLY		DISABLE_ FREQHOP	DISABLE_ DBLBUFFERING	DISABLE_ PHASEADJ	0x00	R/W

REGISTER DESCRIPTIONS

Address: 0x0000, Reset: 0x00, Name: ADI_SPI_CONFIG

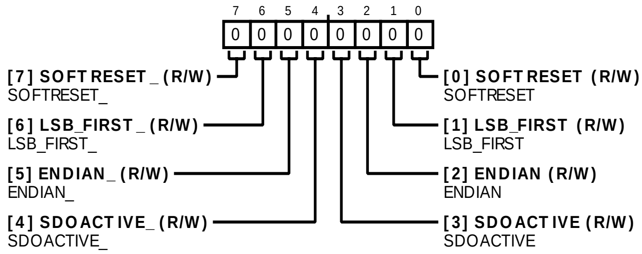

Table 19. Bit Descriptions for ADI_SPI_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
7	SOFTRESET_		SOFTRESET_	0x0	R/W
6	LSB_FIRST_		LSB_FIRST_	0x0	R/W
5	ENDIAN_		ENDIAN_	0x0	R/W
4	SDOACTIVE_		SDOACTIVE_	0x0	R/W
3	SDOACTIVE		SDOACTIVE	0x0	R/W
2	ENDIAN		ENDIAN	0x0	R/W
1	LSB_FIRST		LSB_FIRST	0x0	R/W
0	SOFTRESET		SOFTRESET	0x0	R/W

Address: 0x0001, Reset: 0x00, Name: SPI_CONFIG_B

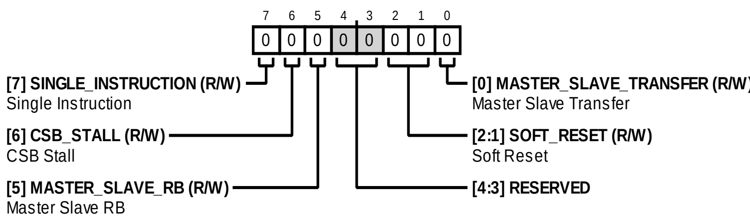

Table 20. Bit Descriptions for SPI_CONFIG_B

Bits	Bit Name	Settings	Description	Reset	Access
7	SINGLE_INSTRUCTION		Single Instruction	0x0	R/W
6	CSB_STALL		CSB Stall	0x0	R/W
5	MASTER_SLAVE_RB		Master Slave Readback (RB)	0x0	R/W
[4:3]	RESERVED		Reserved	0x0	R/W
[2:1]	SOFT_RESET		Soft Reset	0x0	R/W
0	MASTER_SLAVE_TRANSFER		Master Slave Transfer	0x0	R/W

Address: 0x0003, Reset: 0x01, Name: CHIPTYPE

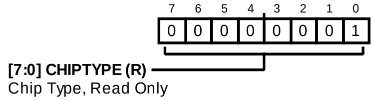

Table 21. Bit Descriptions for CHIPTYPE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHIPTYPE		Chip Type, Read Only	0x1	R

Address: 0x0004, Reset: 0x13, Name: PRODUCT_ID_L

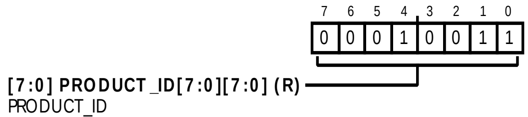

Table 22. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID, Bits[7:0]		PRODUCT_ID	0x13	R

Address: 0x0005, Reset: 0x00, Name: PRODUCT_ID_H

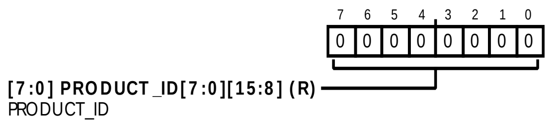

Table 23. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID, Bits[15:8]		PRODUCT_ID	0x13	R

Address: 0x000A, Reset: 0x00, Name: SCRATCHPAD

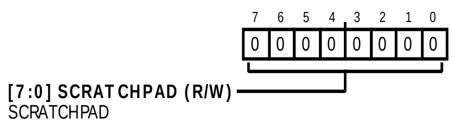

Table 24. Bit Descriptions for SCRATCHPAD

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SCRATCHPAD		SCRATCHPAD	0x0	R/W

Address: 0x000B, Reset: 0x00, Name: SPI_REV

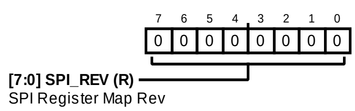

Table 25. Bit Descriptions for SPI_REV

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPI_REV		SPI Register Map Rev	0x0	R

Address: 0x000C, Reset: 0x56, Name: VENDOR_ID_L

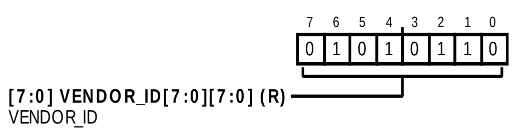

Table 26. Bit Descriptions for VENDOR_ID_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID, Bits[7:0]		VENDOR_ID	0x456	R

Address: 0x000D, Reset: 0x04, Name: VENDOR_ID_H

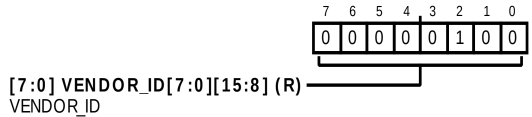

Table 27. Bit Descriptions for VENDOR_ID_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID, Bits[15:8]		VENDOR_ID	0x456	R

Address: 0x0020, Reset: 0x00, Name: MASTER_CONFIG

Controls master enable, SPI mode, sleep mode, and the input word for the dc DAC.

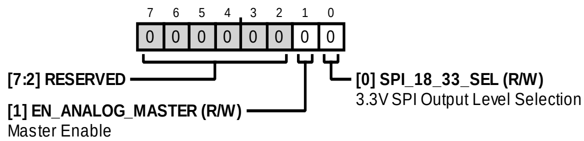

Table 28. Bit Descriptions for MASTER_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	EN_ANALOG_MASTER		Master Enable. Master enable for the DPD analog blocks. Active high.	0x0	R/W
0	SPI_18_33_SEL		3.3 V SPI Output Level Selection. The high level is 3.3 V, and the low level is 1.8 V.	0x0	R/W

Address: 0x0030, Reset: 0x00, Name: RF_SWITCH

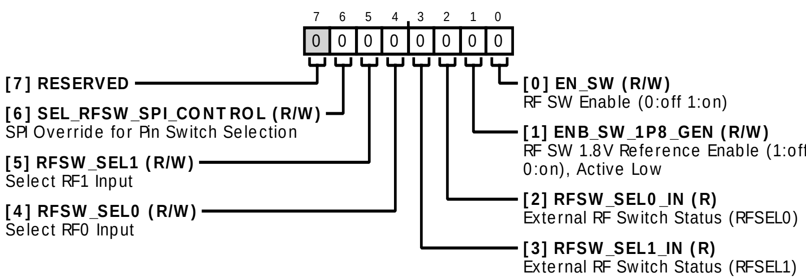

Table 29. Bit Descriptions for RF_SWITCH

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	SEL_RFSW_SPI_CONTROL		SPI Override for Pin Switch Selection.	0x0	R/W
5	RFSW_SEL1		Select RF1 Input. Software control for the RF channel selection (requires that SEL_RFSW_SPI_CONTROL is set to 1).	0x0	R/W
		0	Not selected (internal 50 Ω termination).		
		1	RF channel selected (signal connected to signal path).		
4	RFSW_SEL0		Select RF0 Input. Software control for the RF channel selection (requires that SEL_RFSW_SPI_CONTROL is set to 1).	0x0	R/W
		0	Not selected (internal 50 Ω termination).		
		1	RF channel selected (signal connected to signal path).		
3	RFSW_SEL1_IN		External RF Switch Status (RFSEL1). Readback status of the external RF channel selection pin (RF_SEL1).	0x0	R
		0	Not selected (internal 50 Ω termination).		
		1	RF channel selected (signal connected to signal path).		

Bits	Bit Name	Settings	Description	Reset	Access
2	RFSW_SEL0_IN		External RF Switch Status (RFSEL0). Readback status of the external RF channel selection pin (RF_SEL0).	0x0	R
		0	Not selected (internal 50 Ω termination).		
		1	RF channel selected (signal connected to signal path).		
1	ENB_SW_1P8_GEN		RF SW 1.8 V Reference Enable (0: off and 1: on). Active low. Note that the input is active low; therefore, the default value of 0 enables this circuit.	0x0	R/W
		0	On.		
		1	Off.		
0	EN_SW		RF SW Enable (0: off and 1: on). Enable for the RF channel switch. This must be enabled whenever RF Channel 1 or RF Channel 2 is used (either closed or set to open (that is, termination).	0x0	R/W
		0	Off.		
		1	On.		

Address: 0x0031, Reset: 0x00, Name: DSA_CONTROL

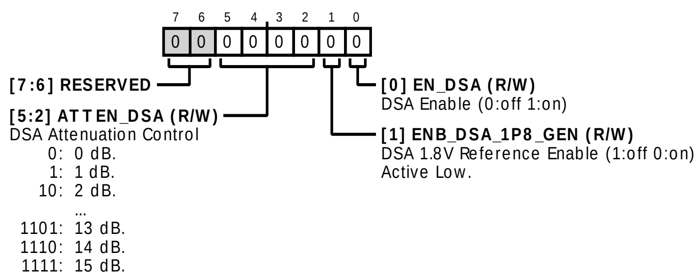

Table 30. Bit Descriptions for DSA_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:2]	ATTEN_DSA		DSA Attenuation Control. Controls the digital step attenuation in 1 dB steps.	0x0	R/W
		0	0 dB.		
		1	1 dB.		
		10	2 dB.		
		…	…		
		1101	13 dB.		
		1110	14 dB.		
		1111	15 dB.		
1	ENB_DSA_1P8_GEN		DSA 1.8 V Reference Enable (1: off and 0: on). Active low.	0x0	R/W
0	EN_DSA		DSA Enable (0: off and 1: on). This bit must be set to enable the RF digital step attenuator.	0x0	R/W

Address: 0x0032, Reset: 0x00, Name: DEMOD_ENABLES

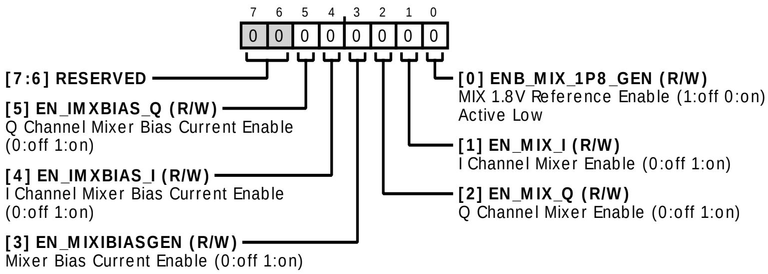

Table 31. Bit Descriptions for DEMOD_ENABLES

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
5	EN_IMXBIAS_Q		Q Channel Mixer Bias Current Enable (0: off and 1: on). Mixer bias current enable. This must be enabled whenever the mixer is enabled. The master mixer bias, EN_MIXBIASGEN, must also be enabled as well.	0x0	R/W
4	EN_IMXBIAS_I		I Channel Mixer Bias Current Enable (0: off and 1: on). Mixer bias current enable. This must be enabled whenever the mixer is enabled. The master mixer bias, EN_MIXBIASGEN, must also be enabled as well.	0x0	R/W
3	EN_MIXIBIASGEN		Mixer Bias Current Enable (0: off and 1: on). Master mixer bias current is enabled and must be enabled whenever the mixer is enabled.	0x0	R/W
2	EN_MIX_Q		Q Channel Mixer Enable (0: off and 1: on). Enable for the mixer. For the mixer to correctly function, the following bits must also be enabled or set to 45: EN_MIXBIAS_x, EN_MIXBIASGEN, EN_ICMOBIAS_x, and CODE_MIXER_OCM.	0x0	R/W
1	EN_MIX_I		I Channel Mixer Enable (0: off and 1: on). Enable for the mixer. For the mixer to correctly function the following bits must also be enabled or set to 45: EN_MIXBIAS_x, EN_MIXBIASGEN, EN_ICMOBIAS_x, and CODE_MIXER_OCM.	0x0	R/W
0	ENB_MIX_1P8_GEN		Mixer 1.8 V Reference Enable (0: off and 1: on). Active low.	0x0	R/W

Address: 0x0033, Reset: 0x00, Name: DEMOD_LO_COM_CTRL

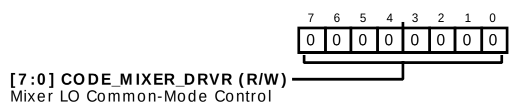

Table 32. Bit Descriptions for DEMOD_LO_COM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CODE_MIXER_DRVR		Mixer LO Common-Mode Control. Determines the dc level applied to the mixer LO driver LDO.	0x0	R/W

Address: 0x0034, Reset: 0x00, Name: DEMOD_OUT_COM_CTRL

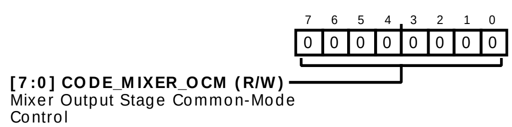

Table 33. Bit Descriptions for DEMOD_OUT_COM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CODE_MIXER_OCM		Mixer Output Stage Common-Mode Control. Determines the dc level applied to the mixer output LDO.	0x0	R/W

Address: 0x003A, Reset: 0x20, Name: DEMOD_SPARES

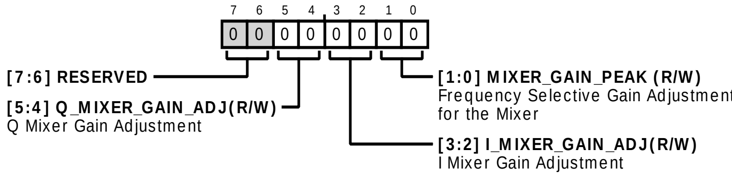

Table 34. Bit Descriptions for DEMOD_SPARES

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	Q_MIXER_GAIN_ADJ		Q Mixer Gain Adjustment. Allows the individual mixer gains to be adjusted in 0.2 dB steps (gains are adjusted relative to each other) to improve I/Q balance.	0x0	R/W
[3:2]	I_MIXER_GAIN_ADJ		I Mixer Gain Adjustment. Allows the individual mixer gains to be adjusted in 0.2 dB steps (gains are adjusted relative to each other) to improve I/Q balance.	0x0	R/W
[1:0]	MIXER_GAIN_PEAK		Frequency Selective Gain Adjustment for the Mixer. It compensates for the frequency dependent loss in RF front end. 0 for no compensation, and 3 (decimal) for maximum compensation.	0x0	R/W

Address: 0x0040, Reset: 0x00, Name: DEMOD_DRIVER_COM_CTRL

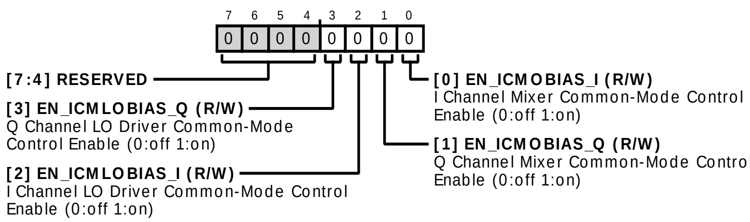

Table 35. Bit Descriptions for DEMOD_DRIVER_COM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
3	EN_ICMLOBIAS_Q		Q Channel LO Driver Common-Mode Control Enable (0: off and 1: on). LO path driver LDO bias current. This must be enabled to turn on the LDO for the LO driver block which interfaces to the mixer.	0x0	R/W
2	EN_ICMLOBIAS_I		I Channel LO Driver Common-Mode Control Enable (0: off and 1: on). LO path driver LDO bias current. This must be enabled to turn on the LDO for the LO driver block which interfaces to the mixer.	0x0	R/W
1	EN_ICMOBIAS_Q		Q Channel Mixer Common-Mode Control Enable (0: off and 1: on). Mixer LDO bias current. This must be enabled to turn on the LDO for the mixer. This is required whenever the mixer is enabled.	0x0	R/W
0	EN_ICMOBIAS_I		I Channel Mixer Common-Mode Control Enable (0: off and 1: on). Mixer LDO bias current. This must be enabled to turn on the LDO for the mixer. This is required whenever the mixer is enabled.	0x0	R/W

Address: 0x0050, Reset: 0x00, Name: DC_CTRL

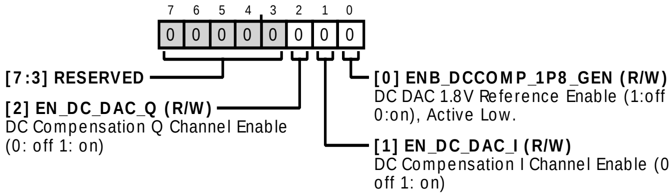

Table 36. Bit Descriptions for DC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x0	R
2	EN_DC_DAC_Q		DC Compensation Q Channel Enable (0: off and 1: on). Enables the dc compensation DAC.	0x0	R/W
1	EN_DC_DAC_I		DC Compensation I Channel Enable (0: off and 1: on). Enables the dc compensation DAC.	0x0	R/W
0	ENB_DCCOMP_1P8_GEN		DC DAC 1.8 V Reference Enable (1: off and 0: on). Active Low.	0x0	R/W

Address: 0x0051, Reset: 0x00, Name: DC_COMP_I_CHAN_RF0

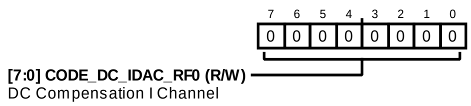

Table 37. Bit Descriptions for DC_COMP_I_CHAN_RF0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CODE_DC_IDAC_RF0		DC Compensation I Channel. Controls the dc correction applied to the IF path. LSB is approximately ½ mV referred to the output. Value is signed magnitude notation. 0xFF is the most negative, and 0x7F is the most positive.	0x0	R/W

Address: 0x0052, Reset: 0x00, Name: DC_COMP_Q_CHAN_RF0

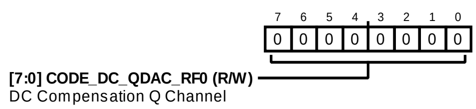

Table 38. Bit Descriptions for DC_COMP_Q_CHAN_RF0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CODE_DC_QDAC_RF0		DC Compensation Q Channel. Controls the dc correction applied to the IF path. LSB is approximately ½ mV referred to the output. Value is signed magnitude notation. 0xFF is the most negative, and 0x7F is the most positive.	0x0	R/W

Address: 0x0053, Reset: 0x00, Name: DC_COMP_I_CHAN_RF1

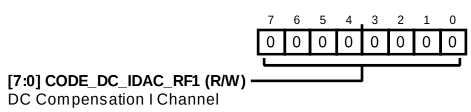

Table 39. Bit Descriptions for DC_COMP_I_CHAN_RF1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CODE_DC_IDAC_RF1		DC Compensation I Channel. Controls the dc correction applied to the IF path. LSB is approximately ½ mV referred to the output. Value is signed magnitude notation. 0xFF is the most negative, and 0x7F is the most positive.	0x0	R/W

Address: 0x0054, Reset: 0x00, Name: DC_COMP_Q_CHAN_RF1

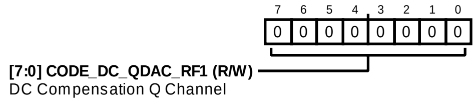

Table 40. Bit Descriptions for DC_COMP_Q_CHAN_RF1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CODE_DC_QDAC_RF1		DC Compensation Q Channel. Controls the dc correction applied to the IF path. LSB is approximately ½ mV referred to the output. Value is signed magnitude notation. 0xFF is the most negative, and 0x7F is the most positive.	0x0	R/W

Address: 0x0060, Reset: 0x00, Name: LPF_BW_SEL

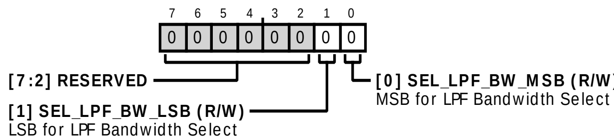

Table 41. Bit Descriptions for LPF_BW_SEL

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	SEL_LPF_BW_LSB		LSB for LPF Bandwidth Select. See the Theory of Operation section.	0x0	R/W
0	SEL_LPF_BW_MSB		MSB for LPF Bandwidth Select. See the Theory of Operation section.	0x0	R/W

Address: 0x0070, Reset: 0x00, Name: IF_AMP_CTRL

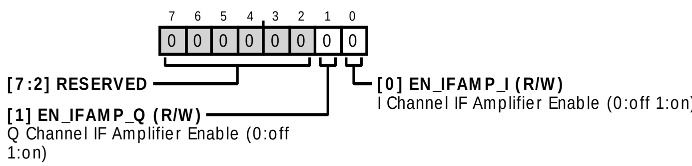

Table 42. Bit Descriptions for IF_AMP_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	EN_IFAMP_Q		Q Channel IF Amplifier Enable (0: off and 1: on). IF output amplifier enable.	0x0	R/W
0	EN_IFAMP_I		I Channel IF Amplifier Enable (0: off and 1: on). IF output amplifier enable.	0x0	R/W

Address: 0x0080, Reset: 0x00, Name: LO_CTRL

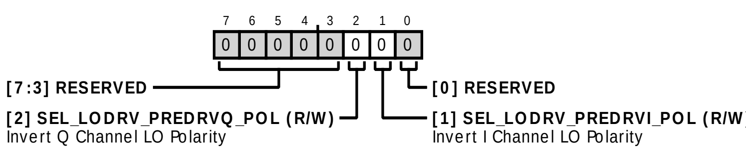

Table 43. Bit Descriptions for LO_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved.	0x0	R
2	SEL_LODRV_PREDRVQ_POL		Invert Q Channel LO Polarity. Selects the polarity for the Q channel LO path. 0: normal polarity. 1: inverted polarity.	0x0	R/W
1	SEL_LODRV_PREDRVI_POL		Invert I Channel LO Polarity. Selects the polarity for the I channel LO path. 0: normal polarity. 1: inverted polarity.	0x0	R/W
0	RESERVED		Reserved.	0x0	R/W

Address: 0x0090, Reset: 0x00, Name: EN_LO_DIVIDER_CTRL

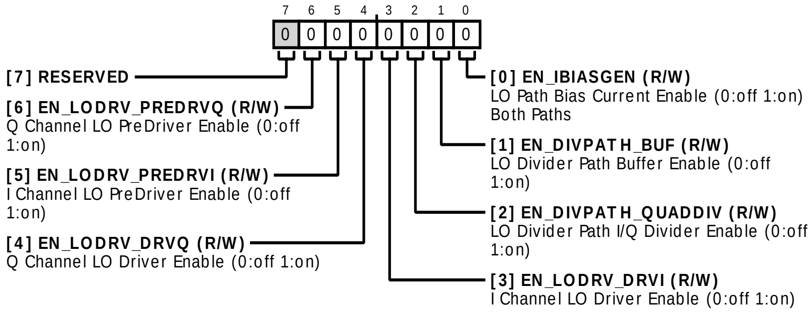

Table 44. Bit Descriptions for EN_LO_DIVIDER_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	EN_LODRV_PREDRVQ		Q Channel LO Predriver Enable (0: off and 1: on). LO path mixer predriver enable. This must be enabled whenever LO path is enabled.	0x0	R/W
5	EN_LODRV_PREDRVI		I Channel LO Predriver Enable (0: off and 1: on). LO path mixer predriver enable. This must be enabled whenever LO path is enabled.	0x0	R/W
4	EN_LODRV_DRVQ		Q Channel LO Driver Enable (0: off and 1: on). LO path mixer driver enable. This must be enabled whenever LO path is enabled.	0x0	R/W
3	EN_LODRV_DRVI		I Channel LO Driver Enable (0: off and 1: on). LO path mixer driver enable. This must be enabled whenever LO path is enabled.	0x0	R/W
2	EN_DIVPATH_QUADDIV		LO Divider Path I/Q Divider Enable (0: off and 1: on). Blocks required to be enabled in this path are: EN_DIVPATH_BUF, EN_LODRVR_DRVx, EN_LODRVR_PREDRVRx, EN_IBIASGEN, EN_ICMLOBIAS_x, CODE_MIXER_DRVR.	0x0	R/W
1	EN_DIVPATH_BUF		LO Divider Path Buffer Enable (0: off and 1: on). Blocks required to be enabled in this path are: EN_DIVPATH_QUADDIV, EN_LODRVR_DRVx, EN_LODRVR_PREDRVRx, EN_IBIASGEN, EN_ICMLOBIAS_x, CODE_MIXER_DRVR.	0x0	R/W
0	EN_IBIASGEN		LO Path Bias Current Enable (0: off and 1) Both Paths.	0x0	R/W

Address: 0x0092, Reset: 0x00, Name: LO_PHASE_ADJ

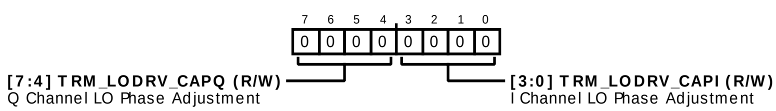

Table 45. Bit Descriptions for LO_PHASE_ADJ

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	TRM_LODRV_CAPQ		Q Channel LO Phase Adjustment. LO Quadrature Phase Adjust. Valid range is from 0x0 to 0xF. For no compensation or adjustment, both TRM_LODRV_CAPI and TRM_LODRV_CAPQ must be set to the same value.	0x0	R/W
[3:0]	TRM_LODRV_CAPI		I Channel LO Phase Adjustment. LO Quadrature Phase Adjust. Valid range is from 0x0 to 0xF. For no compensation or adjustment, both TRM_LODRV_CAPI and TRM_LODRV_CAPQ must be set to the same value.	0x0	R/W

Address: 0x1021, Reset: 0xFF, Name: BLOCK_RESETS

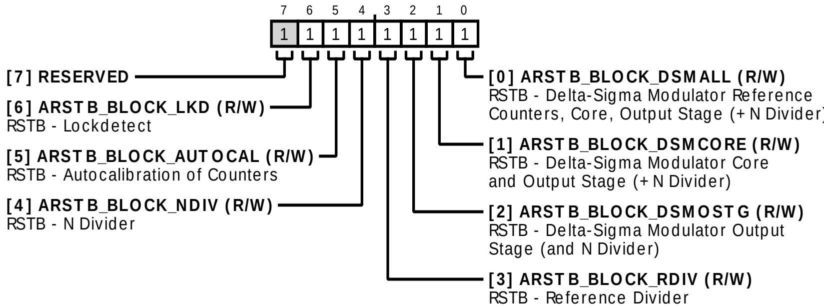

Table 46. Bit Descriptions for BLOCK_RESETS

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x1	R/W
6	ARSTB_BLOCK_LKD		RSTB – Lockdetect	0x1	R/W
5	ARSTB_BLOCK_AUTOCAL		RSTB – Autocalibration of Counters	0x1	R/W
4	ARSTB_BLOCK_NDIV		RSTB – N Divider (integer divider)	0x1	R/W
3	ARSTB_BLOCK_RDIV		RSTB – Reference Divider	0x1	R/W
2	ARSTB_BLOCK_DSMOSTG		RSTB – Delta-Sigma Modulator Output Stage (and N Divider)	0x1	R/W
1	ARSTB_BLOCK_DSMCORE		RSTB – Delta-Sigma Modulator Core and Output Stage (+N Divider)	0x1	R/W
0	ARSTB_BLOCK_DSMALL		RSTB – Delta-Sigma Modulator Reference Counters, Core, Output Stage (+N Divider)	0x1	R/W

Address: 0x1109, Reset: 0x0A, Name: SIG_PATH_9_NORMAL

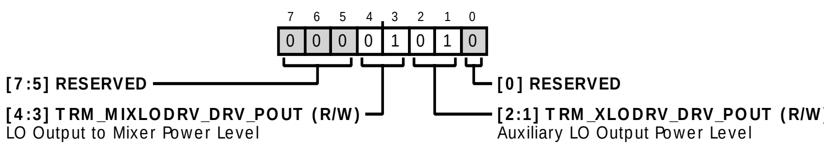

Table 47. Bit Descriptions for SIG_PATH_9_NORMAL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
[4:3]	TRM_MIXLODRV_DRV_POUT		LO Output to Mixer Power Level	0x1	R/W
[2:1]	TRM_XLODRV_DRV_POUT		Auxiliary LO Output Power Level	0x1	R/W
0	RESERVED		Reserved	0x0	R

Address: 0x1200, Reset: 0x89, Name: INT_L

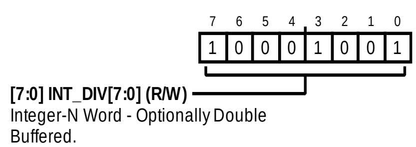

Table 48. Bit Descriptions for INT_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV, Bits[7:0]		Integer-N Word—Optionally Double Buffered. Writing the LSB of the integer word normally causes an autotune event.	0x189	R/W

Address: 0x1201, Reset: 0x01, Name: INT_H

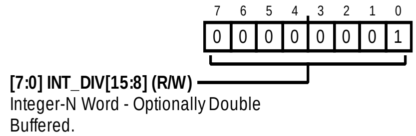

Table 49. Bit Descriptions for INT_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV, Bits[15:8]		Integer-N Word—Optionally Double Buffered. Writing the LSB of the integer word normally causes an autotune event.	0x189	R/W

Address: 0x1202, Reset: 0x00, Name: FRAC1_L

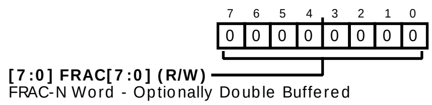

Table 50. Bit Descriptions for FRAC1_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC, Bits[7:0]		FRAC-N Word – Optionally Double Buffered. Lower 8 bits of 24-bit FRAC value.	0x0	R/W

Address: 0x1203, Reset: 0x00, Name: FRAC1_M

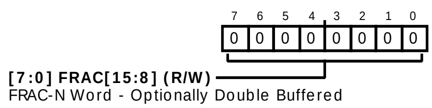

Table 51. Bit Descriptions for FRAC1_M

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC, Bits[15:8]		FRAC-N Word – Optionally Double Buffered. Lower 8 bits of 24-bit FRAC value.	0x0	R/W

Address: 0x1204, Reset: 0x00, Name: FRAC1_H

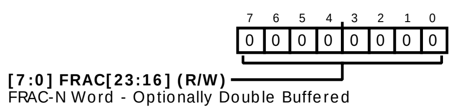

Table 52. Bit Descriptions for FRAC1_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC, Bits[23:16]		FRAC-N Word – Optionally Double Buffered. Lower 8 bits of 24-Bit FRAC value.	0x0	R/W

Address: 0x1205, Reset: 0x00, Name: SD_PHASE_L_0

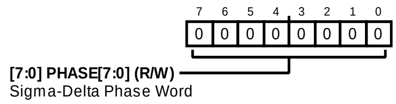

Table 53. Bit Descriptions for SD_PHASE_L_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE, Bits[7:0]		Sigma-Delta Phase Word. If phase adjust mode is enabled (PHASE_ADJ_EN = 1), the phase in the DSM is incremented by this amount on each phase adjustment trigger. The phase adjustment trigger can be caused by the SPI via a write to the LSB of this register (provided DISABLE_PHASEADJ = 0) or from the GPI port. The value is represented as an unsigned 24-bit fractional number, in units of VCO cycles. It, therefore, has a resolution of 21 μ°. For example, to adjust the phase by 5° of the fundamental VCO, program this word to (5°/360°) × 2^{24} = 233,017. This process can be done repetitively to effectively recede by multiple VCO cycles or to embed the PLL itself inside the phase or frequency control loops under some other supervisory control. The phase adjust feature cannot be done any faster than once every five PFD cycles and by no more than 180° on any individual adjustment.	0x0	R/W

Address: 0x1206, Reset: 0x00, Name: SD_PHASE_M_0

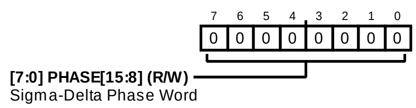

Table 54. Bit Descriptions for SD_PHASE_M_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE, Bits[15:8]		Sigma-Delta Phase Word. If phase adjust mode is enabled (PHASE_ADJ_EN = 1), the phase in the DSM is incremented by this amount on each phase adjustment trigger. The phase adjustment trigger can be caused by the SPI via a write to the LSB of this register (provided DISABLE_PHASEADJ = 0) or from the GPI port. The value is represented as an unsigned 24-bit fractional number, in units of VCO cycles. It, therefore, has a resolution of 21 μ°. For example, to adjust the phase by 5° of the fundamental VCO, program this word to (5°/360°) × 2^{24} = 233,017. This process can be done repetitively to effectively recede by multiple VCO cycles or to embed the PLL itself inside the phase or frequency control loops under some other supervisory control. The phase adjust feature cannot be done any faster than once every five PFD cycles and by no more than 180° on any individual adjustment.	0x0	R/W

Address: 0x1207, Reset: 0x00, Name: SD_PHASE_H_0

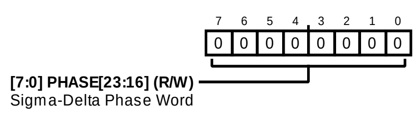

Table 55. Bit Descriptions for SD_PHASE_H_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE, Bits[23:16]		Sigma-Delta Phase Word. If phase adjust mode is enabled (PHASE_ADJ_EN = 1), the phase in the DSM is incremented by this amount on each phase adjustment trigger. The phase adjustment trigger can be caused by the SPI via a write to the LSB of this register (provided DISABLE_PHASEADJ = 0) or from the GPI port. The value is represented as an unsigned 24-bit fractional number, in units of VCO cycles. It, therefore, has a resolution of 21 μ°. For example, to adjust the phase by 5° of the fundamental VCO, program this word to (5°/360°) × 2^{24} = 233,017. This process can be done repetitively to effectively recede by multiple VCO cycles or to embed the PLL itself inside the phase or frequency control loops under some other supervisory control. The phase adjust feature cannot be done any faster than once every five PFD cycles, and by no more than 180° on any individual adjustment.	0x0	R/W

Address: 0x1208, Reset: 0x00, Name: MOD_L

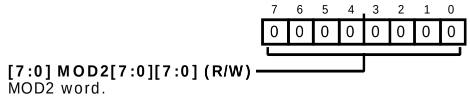

Table 56. Bit Descriptions for MOD_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	MOD2, Bits[7:0]		MOD2 word; lower bits	0x0	R/W

Address: 0x1209, Reset: 0x00, Name: MOD_H

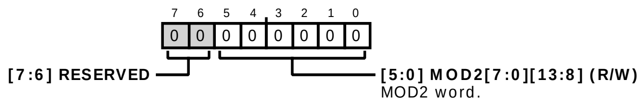

Table 57. Bit Descriptions for MOD_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:0]	MOD2, Bits[13:8]		MOD2 word; upper bits	0x0	R/W

Address: 0x120B, Reset: 0x01, Name: SYNTH

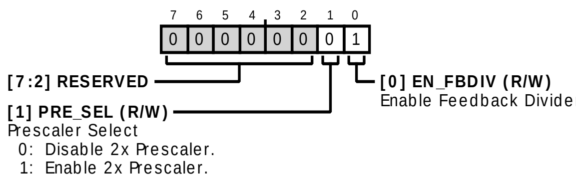

Table 58. Bit Descriptions for SYNTH

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	PRE_SEL		Prescaler Select	0x0	R/W
		0	Disable 2× Prescaler		
		1	Enable 2× Prescaler		
0	EN_FBDIV		Enable Feedback Divider	0x1	R/W

Address: 0x120C, Reset: 0x03, Name: R_DIV

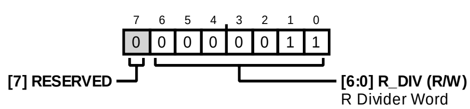

Table 59. Bit Descriptions for R_DIV

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:0]	R_DIV		R Divider Word. Lower 8 bits of 10-bit reference R divider word.	0x3	R/W

Address: 0x120E, Reset: 0x04, Name: SYNTH_0

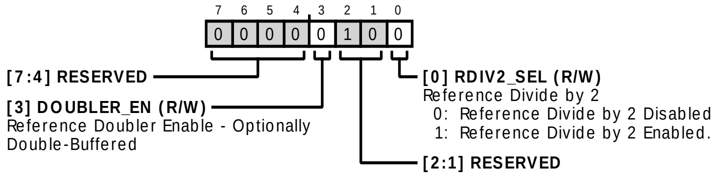

Table 60. Bit Descriptions for SYNTH_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
3	DOUBLER_EN		Reference Doubler Enable—Optionally Double Buffered	0x0	R/W
[2:1]	RESERVED		Reserved	0x2	R/W
0	RDIV2_SEL		Reference Divide by 2	0x0	R/W
		0	Reference Divide by 2 Disabled		
		1	Reference Divide by 2 Enabled		

Address: 0x1214, Reset: 0x48, Name: MULTI_FUNC_SYNTH_CTRL_0214

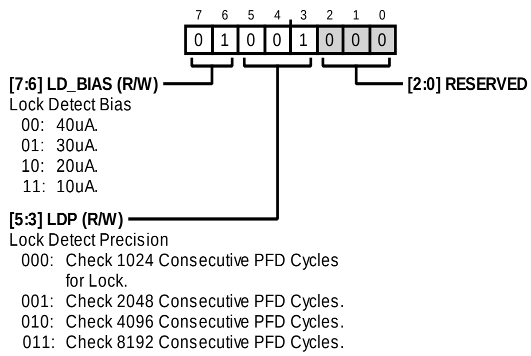

Table 61. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_0214

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LD_BIAS		Lock Detect Bias	0x1	R/W
		00	40 µA.		
		01	30 µA.		
		10	20 µA.		
		11	10 µA.		
[5:3]	LDP		Lock Detect Precision	0x1	R/W
		000	Check 1024 Consecutive PFD Cycles for Lock.		
		001	Check 2048 Consecutive PFD Cycles.		
		010	Check 4096 Consecutive PFD Cycles.		
		011	Check 8192 Consecutive PFD Cycles.		
[2:0]	RESERVED		Reserved.	0x0	R/W

Address: 0x1215, Reset: 0x00, Name: SI_BAND_0

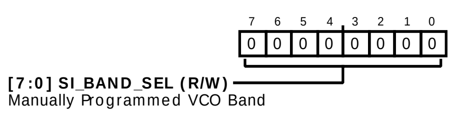

Table 62. Bit Descriptions for SI_BAND_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SI_BAND_SEL		Manually Programmed VCO Band.	0x0	R/W

Address: 0x1217, Reset: 0x00, Name: SI_VCO_SEL

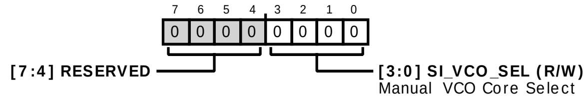

Table 63. Bit Descriptions for SI_VCO_SEL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
[3:0]	SI_VCO_SEL		Manual VCO Core Select	0x0	R/W

Address: 0x121C, Reset: 0x20, Name: VCO_TIMEOUT_L

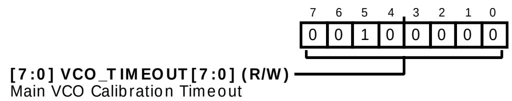

Table 64. Bit Descriptions for VCO_TIMEOUT_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VCO_TIMEOUT[7:0]		Main VCO Calibration Timeout. This value sets what a timing unit is in the VCO calibration. It is represented in a number of phase frequency detector (PFD) periods. For example, 32 is 32 PFD cycles. At a 30.72 MHz PFD rate, this timer represents an approximately 1 μs period. It is recommended that the user program this value, depending on their PFD rate, to represent approximately 1 μs to 2 μs. A longer value than necessary leads to longer autocalibration times, and shorter values may risk autotune accuracy due to insufficient settling times.	0x20	R/W

Address: 0x121D, Reset: 0x00, Name: VCO_TIMEOUT_H

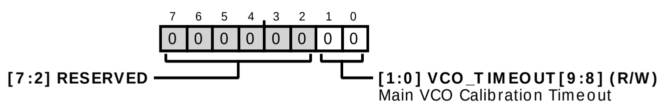

Table 65. Bit Descriptions for VCO_TIMEOUT_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
[1:0]	VCO_TIMEOUT[9:8]		Main VCO Calibration Timeout. This value sets what a timing unit is in the VCO calibration. It is represented in a number of PFD periods. For example, 32 is 32 PFD cycles. At a 30.72 MHz PFD rate, this timer represents an approximately 1 μs period. It is recommended that the user program this value, depending on their PFD rate, to represent approximately 1 μs to 2 μs. A longer value than necessary leads to longer autocalibration times, and shorter values may risk autotune accuracy due to insufficient settling times.	0x0	R/W

Address: 0x121E, Reset: 0x14, Name: VCO_BAND_DIV

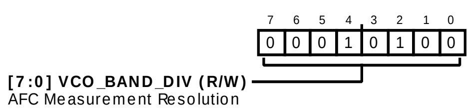

Table 66. Bit Descriptions for VCO_BAND_DIV

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VCO_BAND_DIV		AFC Measurement Resolution. This value sets how long a single automatic frequency calibration (AFC) measurement cycle lasts. The AFC measurement lasts 16 × VCO_BAND_DIV. It is required that the user program this value, depending on their PFD rate, to represent approximately 10 μs. A longer value than necessary leads to longer autocalibration times, and shorter values may risk autotune accuracy due to insufficient frequency measurement resolution.	0x14	R/W

Address: 0x121F, Reset: 0x00, Name: VCO_FSM

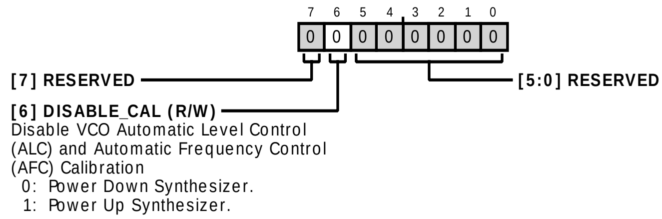

Table 67. Bit Descriptions for VCO_FSM

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	DISABLE_CAL		Disable VCO Automatic Level Control (ALC) and Automatic Frequency Control (AFC) Calibration. The PLL does not reset the calibration machine or trigger a new calibration if set to 1 on a frequency hop to maintain ALC and capacitor positions.	0x0	R/W
		0	Power-Down Synthesizer.		
		1	Power-Up Synthesizer.		
[5:0]	RESERVED		Reserved.	0x0	R/W

Address: 0x122A, Reset: 0x02, Name: SD_CTRL

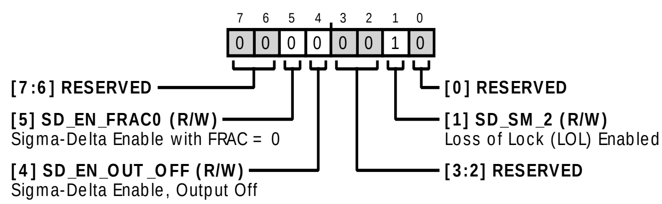

Table 68. Bit Descriptions for SD_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R/W
5	SD_EN_FRAC0		Sigma-Delta Enable with FRAC = 0. The DSM normally recognizes a FRAC value of all 0, and disables itself. Setting this mode can keep the DSM running even when a zero FRAC is presented.	0x0	R/W
4	SD_EN_OUT_OFF		Sigma-Delta Enable, Output Off. Keeps the DSM core enabled and clocking but ignores the output of the DSM and instead multiplexes the N divider setpoint from the double buffer data directly.	0x0	R/W
[3:2]	RESERVED		Reserved.	0x0	R
1	SD_SM_2		Loss of Lock (LOL) Enabled. Enables the CSP/LOL circuit. Recommend Reserved 1.	0x1	R/W
0	RESERVED		Reserved.	0x0	R/W

Address: 0x122C, Reset: 0x03, Name: MULTI_FUNC_SYNTH_CTRL_022C

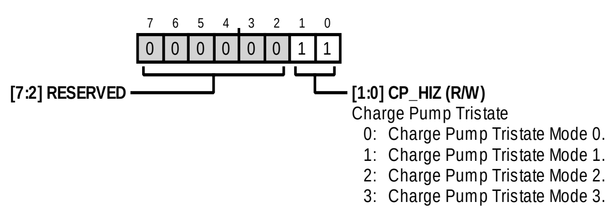

Table 69. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022C

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved	0x0	R
[1:0]	CP_HIZ		Charge Pump Tristate	0x3	R/W
		0	Charge Pump Tristate Mode 0		
		1	Charge Pump Tristate Mode 1		
		2	Charge Pump Tristate Mode 2		
		3	Charge Pump Tristate Mode 3		

Address: 0x122D, Reset: 0x81, Name: MULTI_FUNC_SYNTH_CTRL_022D

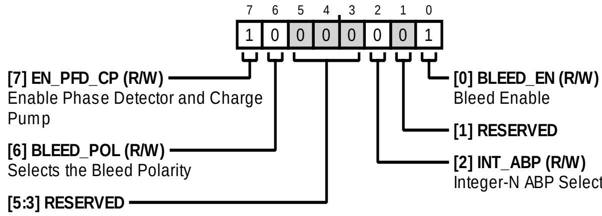

Table 70. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022D

Bits	Bit Name	Settings	Description	Reset	Access
7	EN_PFD_CP		Enable Phase Detector and Charge Pump.	0x1	R/W
6	BLEED_POL		Selects the Bleed Polarity.	0x0	R/W
[5:3]	RESERVED		Reserved.	0x0	R
2	INT_ABP		Integer-N ABP Select. Shortens the reset delay of the PFD by four inverters.	0x0	R/W
1	RESERVED		Reserved.	0x0	R
0	BLEED_EN		Bleed Enable.	0x1	R/W

Address: 0x122E, Reset: 0x0F, Name: CP_CURR

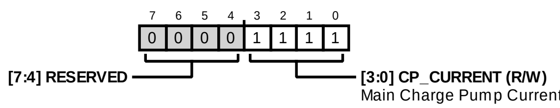

Table 71. Bit Descriptions for CP_CURR

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
[3:0]	CP_CURRENT		Main Charge Pump Current	0xF	R/W

Address: 0x122F, Reset: 0x08, Name: BICP

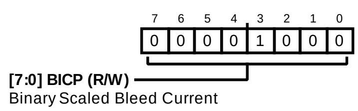

Table 72. Bit Descriptions for BICP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	BICP		Binary Scaled Bleed Current	0x8	R/W

Address: 0x1233, Reset: 0x00, Name: FRAC2_L

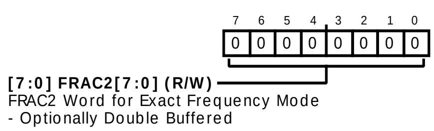

Table 73. Bit Descriptions for FRAC2_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC2, Bits[7:0]		FRAC2 Word for Exact Frequency Mode—Optionally Double Buffered	0x0	R/W

Address: 0x1234, Reset: 0x00, Name: FRAC2_H

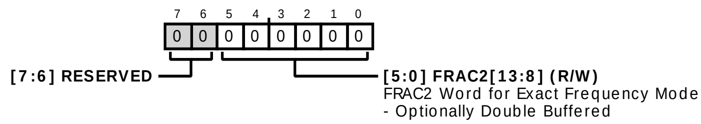

Table 74. Bit Descriptions for FRAC2_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:0]	FRAC2, Bits[13:8]		FRAC2 Word for Exact Frequency Mode—Optionally Double Buffered	0x0	R/W

Address: 0x1235, Reset: 0x00, Name: MULTI_FUNC_SYNTH_CTRL_0235

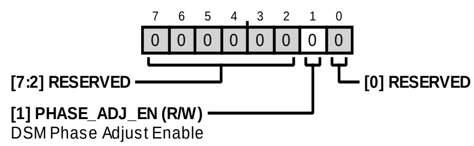

Table 75. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_0235

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	PHASE_ADJ_EN		DSM Phase Adjust Enable. If 1, a phase-adjust trigger causes a phase shift in the Δ-Σ by the amount programmed in the phase word. The phase trigger is either caused by a write to the LSB of the phase word or through a general-purpose input (GPI) trigger. See GPI1_FUNC_SEL for more information.	0x0	R/W
0	RESERVED		Reserved.	0x0	R

Address: 0x1240, Reset: 0x00, Name: VCO_LUT_CTRL

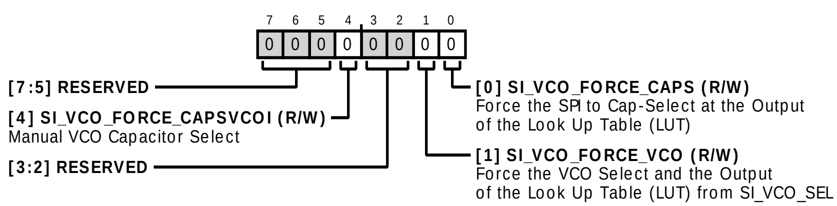

Table 76. Bit Descriptions for VCO_LUT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
4	SI_VCO_FORCE_CAPSVCOI		Manual VCO Capacitor Select	0x0	R/W
[3:2]	RESERVED		Reserved	0x0	R/W
1	SI_VCO_FORCE_VCO		Force the VCO Select and the Output of the Look Up Table (LUT) from SI_VCO_SEL	0x0	R/W
0	SI_VCO_FORCE_CAPS		Force the SPI to Capacitor Select at the Output of the Look Up Table (LUT)	0x0	R/W

Address: 0x124D, Reset: 0x00, Name: LOCK_DETECT

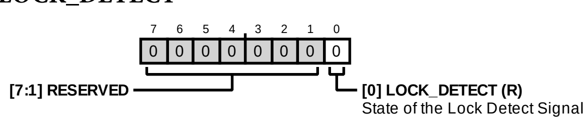

Table 77. Bit Descriptions for LOCK_DETECT

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved	0x0	R
0	LOCK_DETECT		State of the Lock Detect Signal	0x0	R

Address: 0x1401, Reset: 0x00, Name: MULTI_FUNC_CTRL

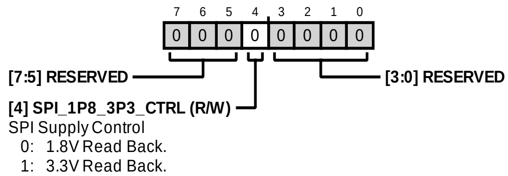

Table 78. Bit Descriptions for MULTI_FUNC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
4	SPI_1P8_3P3_CTRL		SPI Supply Control	0x0	R/W
		0	1.8 V Read Back		
		1	3.3 V Read Back		
[3:0]	RESERVED		Reserved	0x0	R

Address: 0x140E, Reset: 0xB3, Name: LO_CNTRL2

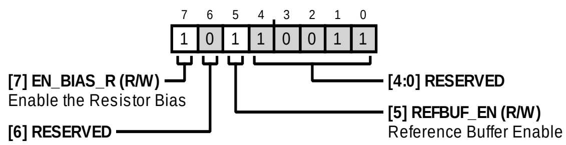

Table 79. Bit Descriptions for LO_CNTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	EN_BIAS_R		Enable the Resistor Bias. Selects the resistor bias instead of the band gap based bias for the LO path.	0x1	R/W
6	RESERVED		Reserved.	0x0	R/W
5	REFBUF_EN		Reference Buffer Enable.	0x1	R/W
[4:0]	RESERVED		Reserved.	0x13	R/W

Address: 0x1414, Reset: 0x02, Name: LO_CNTRL8

Recommended register for use to control the LO path from a single spot. By programming this register, the individual blocks enable and configuration bits are set appropriately.

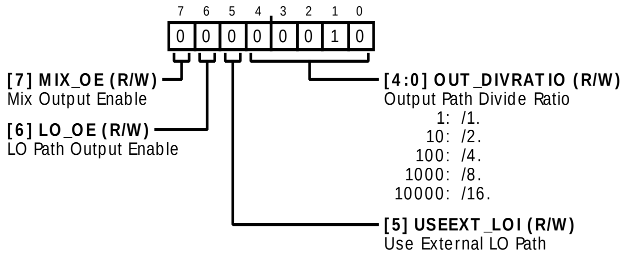

Table 80. Bit Descriptions for LO_CNTRL8

Bits	Bit Name	Settings	Description	Reset	Access
7	MIX_OE		Mix Output Enable. When disabled (OE = 0), mute = 1, or DIVRATIO = 0, the mute depth is selected via GEN_MUTE_DEPTH. Note that the mute depth can be artificially restricted if the other output path is still enabled and relies on a shared branch of the LO chain.	0x0	R/W
6	LO_OE		LO Path Output Enable. When disabled (OE = 0), MUTE = 1, or DIVRATIO = 0, the mute depth is selected via GEN_MUTE_DEPTH. Note that the mute depth can be artificially restricted if the other output path is still enabled and relies on a shared branch of the LO chain.	0x0	R/W
5	USEEXT_LOI		Use External LO Path.	0x0	R/W
[4:0]	OUT_DIVRATIO		Output Path Divide Ratio. Sets the divide ratio from the fundamental VCOs or the external input path to the output paths. Nominally, the internal VCO range is 4 GHz to 8 GHz.	0x2	R/W
		0	Mute		
		1	/1.		
		10	/2.		
		100	/4.		
		1000	/8.		
		10000	/16.		

Address: 0x1541, Reset: 0x00, Name: FRAC2_L_SLAVE

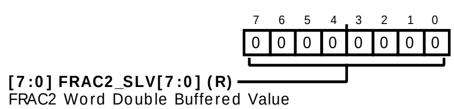

Table 81. Bit Descriptions for FRAC2_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC2_SLV, Bits[7:0]		FRAC2 Word Double Buffered Value	0x0	R

Address: 0x1542, Reset: 0x00, Name: FRAC2_H_SLAVE

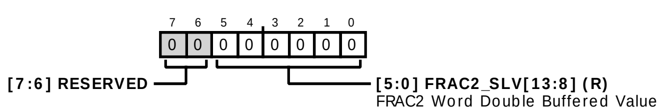

Table 82. Bit Descriptions for FRAC2_H_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:0]	FRAC2_SLV, Bits[13:8]		FRAC2 Word Double Buffered Value	0x0	R

Address: 0x1543, Reset: 0x00, Name: FRAC_L_SLAVE

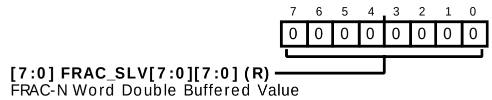

Table 83. Bit Descriptions for FRAC_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC_SLV, Bits[7:0]		FRAC-N Word Double Buffered Value. Lower 8 bits of 24-Bit FRAC value.	0x0	R

Address: 0x1544, Reset: 0x00, Name: FRAC_M_SLAVE

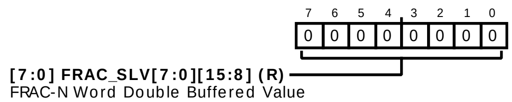

Table 84. Bit Descriptions for FRAC_M_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC_SLV, Bits[15:8]		FRAC-N Word Double Buffered Value. Lower 8 bits of 24-Bit FRAC value.	0x0	R

Address: 0x1545, Reset: 0x00, Name: FRAC_H_SLAVE2

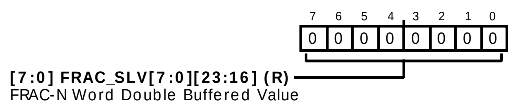

Table 85. Bit Descriptions for FRAC_H_SLAVE2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC_SLV, Bits[23:16]		FRAC-N Word Double Buffered Value. Lower 8 bits of 24-Bit FRAC value.	0x0	R

Address: 0x1546, Reset: 0x00, Name: PHASE_L_SLAVE

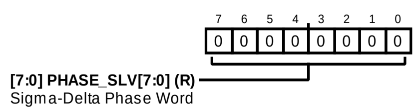

Table 86. Bit Descriptions for PHASE_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE_SLV, Bits[7:0]		Sigma-Delta Phase Word. Lower 8 bits of 24-bit SD phase word.	0x0	R

Address: 0x1547, Reset: 0x00, Name: PHASE_M_SLAVE2

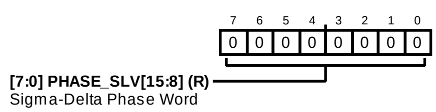

Table 87. Bit Descriptions for PHASE_M_SLAVE2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE_SLV, Bits[15:8]		Sigma-Delta Phase Word. Lower 8 bits of 24-bit SD phase word.	0x0	R

Address: 0x1548, Reset: 0x00, Name: PHASE_H_SLAVE3

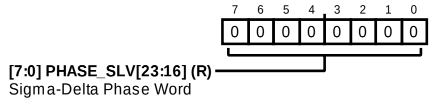

Table 88. Bit Descriptions for PHASE_H_SLAVE3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE_SLV, Bits[23:16]		Sigma-Delta Phase Word. Lower 8 bits of 24-bit SD phase word.	0x0	R

Address: 0x1549, Reset: 0x89, Name: INT_DIV_L_SLAVE

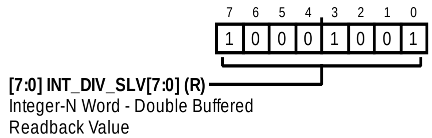

Table 89. Bit Descriptions for INT_DIV_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV_SLV, Bits[7:0]		Integer-N Word – Double Buffered Readback Value. Readback Data from the N divider setpoint ($N_{SETPOINT}$) double buffer output.	0x189	R

Address: 0x154A, Reset: 0x01, Name: INT_DIV_H_SLAVE

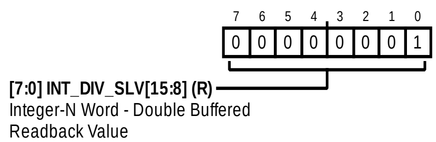

Table 90. Bit Descriptions for INT_DIV_H_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV_SLV, Bits[15:8]		Integer-N Word – Double Buffered Readback Value. Readback Data from the $N_{SETPOINT}$ double buffer output.	0x189	R

Address: 0x154B, Reset: 0x03, Name: R_DIV_SLAVE

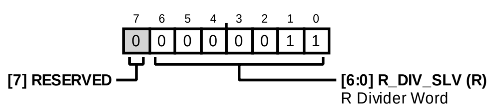

Table 91. Bit Descriptions for R_DIV_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:0]	R_DIV_SLV		R Divider Word. Lower 8 bits of 10-bit reference R divider word.	0x3	R

Address: 0x154C, Reset: 0x00, Name: RDIV2_SEL_SLAVE

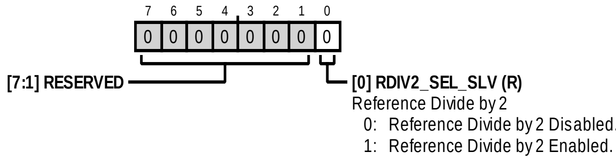

Table 92. Bit Descriptions for RDIV2_SEL_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	RDIV2_SEL_SLV		Reference Divide by 2	0x0	R
		0	Reference Divide by 2 Disabled		
		1	Reference Divide by 2 Enabled		

Address: 0x1583, Reset: 0x00, Name: DISABLE_CFG

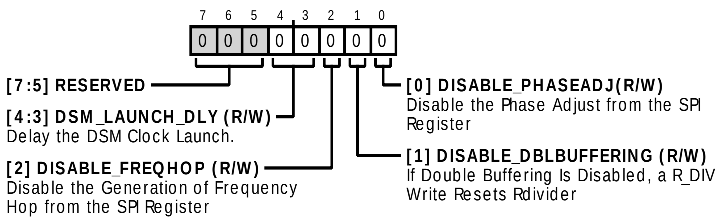

Table 93. Bit Descriptions for DISABLE_CFG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:3]	DSM_LAUNCH_DLY		Delay the DSM Clock Launch.	0x0	R/W
2	DISABLE_FREQHOP		Disable the Generation of the Frequency Hop from the SPI Register.	0x0	R/W
1	DISABLE_DBLBUFFERING		If Double Buffering Is Disabled, a R_DIV Write Resets $R_{DIVIDER}$.	0x0	R/W
0	DISABLE_PHASEADJ		Disable the Phase Adjust from the SPI Register.	0x0	R/W

OUTLINE DIMENSIONS

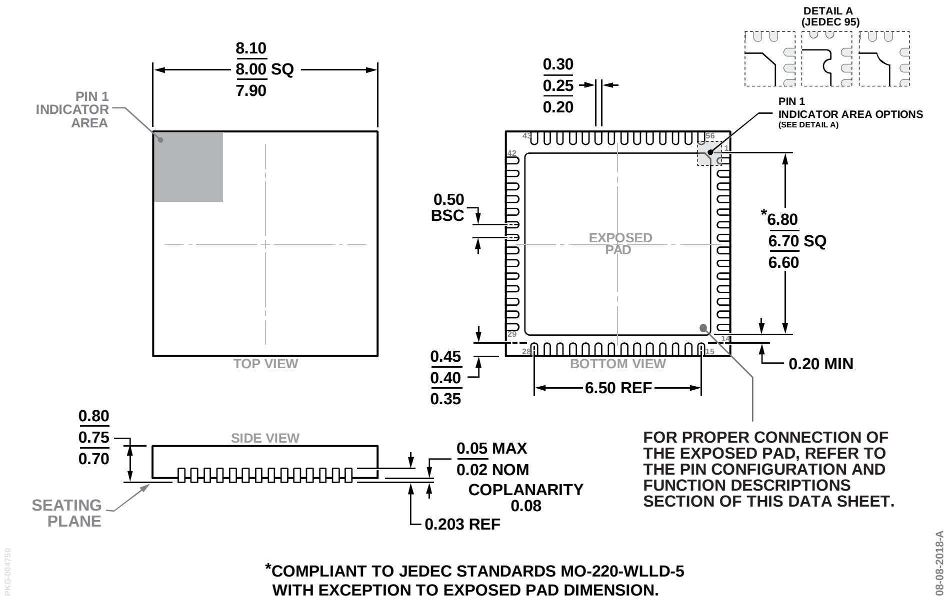

Figure 66. 56-Lead Lead Frame Chip Scale Package [LFCSP]
8 mm × 8 mm Body and 0.75 mm Package Height
(CP-56-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6821ACPZ	−40°C to +105°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-16
ADRF6821ACPZ-RL7	−40°C to +105°C	56-Lead Lead Frame Chip Scale Package [LFCSP], Reel	CP-56-16
ADRF6821-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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