Microwave Wideband Synthesizer with Integrated VCO

Data Sheet

ADF5610

FEATURES

RF output frequency range: 57 MHz to 14,600 MHz
RFOUT: 7300 MHz to 14,600 MHz
PDIV/NDIV: 57 MHz to 14,600 MHz
Fractional-N synthesizer and Integer N synthesizer modes
24-bit fractional modulus
Exact frequency mode for 0 Hz frequency error
Typical PFD spurious: <−105 dBc
Integrated rms jitter: <40 fs
Normalized inband phase noise floor FOM
- **High current mode: −232 dBc/Hz (integer) and −229 dBc/Hz (fractional)**
- **Normal mode: −229 dBc/Hz (integer) and −226 dBc/Hz (fractional)**

Maintains frequency lock over −40°C to +85°C (lock and leave)
Low phase noise VCO
- **−115 dBc/Hz typical at 100 kHz (7.3 GHz)**
- **−114 dBc/Hz typical at 100 kHz (10 GHz)**
- **−109 dBc/Hz typical at 100 kHz (14.6 GHz)**

RFOUT power: 5 dBm
Programmable divide by 1, 2, 4, 8, 16, 32, 64, or 128 output
Programmable output power level
Typical power dissipation: 815 mW
Programmable low current and power dissipation: <700 mW
Fast frequency hopping (autocalibration enabled): <40 µs
48-terminal, 7 mm × 7 mm LGA package: 49 mm²

APPLICATIONS

Military and defense
Test equipment
Clock generation
Wireless infrastructure
Satellite and very small aperture terminal (VSAT)
Microwave radio

GENERAL DESCRIPTION

The ADF5610 allows implementation of fractional-N or Integer N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference source. The wideband microwave voltage controlled oscillator (VCO) design permits frequency operation from 7300 MHz to 14600 MHz at a single radio frequency (RF) output. A series of frequency dividers with a differential frequency output allows operation from 57 MHz to 14600 MHz. Analog and digital power supplies for the PLL circuitry range from 3.1 V to 3.5 V, and the VCO supplies are between 4.75 V and 5.25 V. The charge pump supply voltage can be extended up to 3.6 V for improved frequency band overlap and extended upper frequency range.

The ADF5610 has an integrated VCO with a fundamental frequency of 3650 MHz to 7300 MHz. These frequencies are internally doubled and routed to the RFOUT pin. An additional differential output allows the doubled VCO frequency to be divided by 1, 2, 4, 8, 16, 32, 64, or 128, allowing the user to generate RF output frequencies as low as 57 MHz. A simple 3-wire serial port interface (SPI) provides control of all on-chip registers. To conserve power, this divider block can be disabled when not needed through the SPI interface. Likewise, the output power for both the single-ended output and the differential output are programmable via the VCO register settings. The ADF5610 also contains various power-down modes for the VCO circuitry and PLL circuitry.

The integrated phase detector (PD) and delta-sigma (Δ-Σ) modulator, capable of operating at up to 100 MHz, permit wide loop bandwidths and fast frequency tuning with a typical spurious level of −100 dBc.

With phase noise levels from −115 dBc/Hz at 7.3 GHz to −109 dBc/Hz at 14.6 GHz, the ADF5610 is equipped to minimize blocker effects, and to improve receiver sensitivity and transmitter spectral purity. The low phase noise floor eliminates any contribution to modulator and mixer noise floor in transmitter applications.

The ADF5610 is a PLL with integrated VCO. The device features an innovative programmable performance technology that enables the ADF5610 to tailor current consumption and corresponding noise performance to individual applications by selecting either a low current consumption mode or a high performance mode for improved phase noise performance.

Additional features of the ADF5610 include approximately 3 dB of RFOUT gain control in 1.5 dB steps and 5 dB of control on the differential port in approximately 2.5 dB steps. Finally, the Δ-Σ modulator with exact frequency mode enables users to generate output frequencies with 0 Hz frequency error.

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REVISION HISTORY

2/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

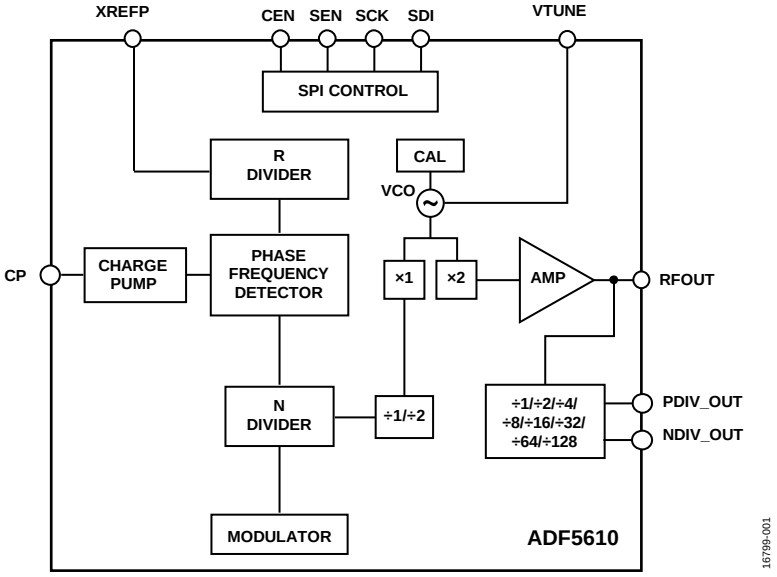


Figure 1.

SPECIFICATIONS

Analog supply (AVDD) = digital power supply (DVDD) = 3.3 V ± 5%, power supply for charge pump digital section (VDDLS), power supply for charge pump (VPPCP), reference path supply (RVDD), phase detector supply (VCCPD), prescaler supply (VCCPS), power supply for PLL RF section (VCCHF) = 3.3 V ± 5%, bias for VCO digital logic, SPI buffer, and input buffer to PLL (VDD1), reference voltage supply (VDD2), differential output divider supply (VDD3) = 3.3 V ± 5%, VCO supply (VCOVCC) = 5.0 V ± 5%, ground (GND) = 0 V, minimum and maximum specifications across the temperature range of −40°C to +85°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT CHARACTERISTICS						
RFOUT Frequency			7300		14,600	MHz
VCO Frequency at PLL Input			3650		7300	MHz
Frequency Range for PDIV_OUT and NDIV_OUT			57		14,600	MHz
OUTPUT POWER						
RFOUT Power		Across all frequencies, high performance mode (VCO Register 0x01, Bits[4:2] = 0x3), maximum gain setting (VCO Register 0x01, Bits[1:0] = 0x3)	0	5	10	dBm
RFOUT Power Control Range		1 dB steps		4		dB
RFOUT Power Variation vs. Temperature				±1		dBm
RFOUT Power Variation vs. Frequency				±2		dBm
PDIV_OUT and NDIV_OUT Power		Maximum gain setting (VCO Register 0x01, Bits[6:5] = 0x3), single-ended	−6	0	6	dBm
		Divide by 2 to divide by 128		2		dBm
PDIV_OUT and NDIV_OUT Control Range		Three settings, bypass mode (divide by 1)		6		dB
HARMONICS (RFOUT)						
½ Harmonic		3650 MHz to 7300 MHz		−20		dBc
1.5 Harmonic				−30		dBc
Second Harmonic				−30		dBc
2.5 Harmonic				−35		dBc
Third Harmonic				−30		dBc
HARMONICS (PDIV_OUT and NDIV_OUT)						
Single-Ended						
½ Harmonic		Fundamental feedthrough				
		N = divide by 1		−20		dBc
		N = divide by 2		−60		dBc
Second Harmonic		Push/push feedthrough				
		N = divide by 1		−26		dBc
		N = divide by 2		−24		dBc
Third Harmonic		N = divide by 1		−24		dBc
		N = divide by 2		−17		dBc
Differential						
½ Harmonic		Fundamental feedthrough (N = 1)		−20		dBc
		Push/push feedthrough (N = 2)		−52		dBc
Second Harmonic		N = divide by 1		−31		dBc
		N = divide by 2		−27		dBc

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Third Harmonic		N = divide by 1		−30		dBc
		N = divide by 2		−16		dBc
VCO Supply Pushing (VDD1)[1]		RFOUT (VT = 1.65 V)		67		MHz/V
VCO Supply Pushing (VCOVCC)[1]		RFOUT (VT = 1.65 V)		1.0		MHz/V
VCO Load Pulling (2.0:1)[2]		RFOUT (VT = 1.65 V)		1.0		MHz p-p
VCO Frequency Drift		RFOUT (VT = 1.65 V)				
		Operating at 7.3 GHz		0.5		MHz/°C
		Operating at 14.6 GHz		1.02		MHz/°C
PLL RF INPUT PRESCALER						
Input Frequency Range		Approximate drive level = −10 dBm	57		4000	MHz
PLL RF DIVIDER CHARACTERISTICS						
19-Bit N Divider Range (Integer N)		Maximum = $2^{19} - 1$	16		524,287	
19-Bit N Divider Range (Fractional-N)		Fractional nominal divide ratio varies (±4) dynamically maximum	20		524,283	
REFERENCE INPUT CHARACTERISTICS						
Maximum XREFP Input Frequency			DC	50	350	MHz
XREFP Input Level		AC-coupled[3]	−6		+12	dBm
XREFP Input Capacitance					5	pF
14-Bit R Divider Range			1		16,383	
PHASE DETECTOR (PD)[4]						
PD Frequency Fractional Mode[5]		Fractional Mode B	DC		100	MHz
PD Frequency Integer Mode			DC		100	MHz
CHARGE PUMP						
Output Current			0.02		2.54	mA
Charge Pump Gain Step Size				20		µA
LOGIC INPUTS						
Logic Switching Threshold (V_{SW})		Input high voltage (V_{IH}) and input low voltage (V_{IL}) within 50 mV of V_{SW}	40	50	60	% of DVDD
SDO LOGIC OUTPUT						
Output High Voltage						
		Complementary metal-oxide semiconductor (CMOS) 3.3 V mode (Register 0x0F, Bits[9:8] = 00b)	−0.2			V
		Open-drain mode (Register 0x0F, Bits[9:8] = 01b)[6]			3.3	V
Output Low Voltage (V_{OL})		CMOS mode (Register 0x0F, Bits[9:8] = 00b)			0.1	V
		Open-drain mode (Register 0x0F, Bits[9:8] = 01b)[7]		0.4		
Serial Clock (SCK) Frequency Rate		CMOS mode (Register 0x0F, Bits[9:8] = 00b)[8]		6	50	MHz
		Open-drain mode (Register 0x0F[9:8] = 01b)[9]		5	10	MHz
Capacitive Load		CMOS mode (Register 0x0F, Bits[9:8] = 00b)		10	20	pF
		Open-drain mode (Register 0x0F, Bits[9:8] = 01b)[10]			10	pF
Load Current		CMOS mode (Register 0x0F, Bits[9:8] = 00b)[11]			3.6	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		Open-drain mode (Register 0x0F, Bits[9:8] = 01b)[12]			7.2	mA
Output Resistance When Driver Is Low (R_{ON})		Open-drain mode (Register 0x0F, Bits[9:8] = 01b)		100	200	Ω
Pull-Up Resistor (R_{UP})		Open-drain mode (Register 0x0F, Bits[9:8] = 01b)	500	1000		Ω
Rise Time		CMOS mode (Register 0x0F, Bits[9:8] = 00b)[13]		$0.5 + 0.3 \times C_{LOAD}$	7	ns
Fall Time		CMOS mode (Register 0x0F, Bits[9:8] = 00b)[13]		$1.5 + 0.2 \times C_{LOAD}$	10	ns
SCK to SDO Turnaround Time		CMOS mode (Register 0x0F, Bits[9:8] = 00b)[13]		$0.9 + 0.1 \times C_{LOAD}$	12	ns
RF Divider Input Below 4 GHz, Integer Mode		19-bit, all values[14]	16		524,287	
RF Divider Input Above 4 GHz, Integer Mode		19-bit, even values only	32		1,048,574	
RF Divider Input Below 4 GHz, Fractional Mode		19-bit, all values	20		524,283	
RF Divider Input Above 4 GHz, Fractional Mode		19-bit, even values only	40		1,048,566	
POWER SUPPLY VOLTAGES						
3.3 V Supplies		AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD, VPPCP, VDDLS, VDD1, VDD2, VDD3	3.1	3.3	3.5	V
5.0 V Supplies		VCOVCC	4.75	5.0	5.25	V
POWER DISSIPATION						
Typical Power Dissipation				815		mW
Programmable Low Current and Power Dissipation				<700		mW
POWER SUPPLY CURRENTS						
AVDD		3.3 V		1.6		mA
RVDD		3.3 V		6		mA
VCCHF		3.3 V		4		mA
VCCPS		3.3 V		29.7		mA
VCCPD		3.3 V		1.0		mA
DVDD		3.3 V		11.9		mA
VPPCP[15]		3.3 V		5.6		mA
VDDLS[15]		3.3 V		0.6		mA
VDD1		3.3 V		3		mA
VDD2		3.3 V		1		mA
VDD3		Divide by 1		62		mA
		Divide by 2		73.7		mA
		Divide by 4		78.8		mA
		Divide by 8		82.4		mA
		Divide by 16		85.9		mA
		Divide by 32		88.1		mA
		Divide by 64		90		mA
		Divide by 128		92		mA
VCOVCC		5.0 V		110		mA
Power-Down						
PLL[16]		Power down via SPI Register 0x01, Bit 0 = 0 and Register 0x01, Bit 1 = 0		100		µA
VCOVCC[17]		Power down using VCO Register 0x02, Bit 3 = 1		13		mA
Divider[17]		Power down using VCO Register 0x01, Bit 8 = 0		1.5		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-ON RESET						
Typical Reset Voltage on DVDD				700		mV
Minimum DVDD Voltage for No Reset			1.5			V
Power-On Reset Delay				250		µs
VCO OPEN-LOOP PHASE NOISE						
RFOUT at 7.3 GHz						
10 kHz Offset				−92		dBc/Hz
100 kHz Offset				−115		dBc/Hz
1 MHz Offset				−135		dBc/Hz
10 MHz Offset				−155		dBc/Hz
100 MHz Offset				−168		dBc/Hz
RFOUT at 10 GHz						
10 kHz Offset				−92		dBc/Hz
100 kHz Offset				−114		dBc/Hz
1 MHz Offset				−135		dBc/Hz
10 MHz Offset				−155		dBc/Hz
100 MHz Offset				−164		dBc/Hz
RFOUT at 11 GHz						
10 kHz Offset				−89		dBc/Hz
100 kHz Offset				−112		dBc/Hz
1 MHz Offset				−132		dBc/Hz
10 MHz Offset				−152		dBc/Hz
100 MHz Offset				−161		dBc/Hz
RFOUT at 14.6 GHz						
10 kHz Offset				−87		
100 kHz Offset				−109		dBc/Hz
1 MHz Offset				−130		dBc/Hz
10 MHz Offset				−150		dBc/Hz
100 MHz Offset				−163		dBc/Hz
PLL						
Phase Noise at 20 kHz Offset, 50 MHz Phase Frequency Detector (PFD) Rate		Over process with 3.3 V power supply at 25°C, measured with >200 kHz loop bandwidth				
Fast Frequency Hopping (Autocalibration Enabled)				<40		µs
Lock Time		Depends on loop filter bandwidth, PFD rate, definition of lock (to within ±Hz or ±degrees of settling), and Register 0x0A configuration		100		µs
Frequency Resolution		Depends on PFD rate and VCO output divider setting		$f_{PD}/2^{24}$		Hz
Fundamental Mode		3.5 GHz to 7.5 GHz output, at typical phase detector frequency (f_{PD}) of 50 MHz, typical resolution = 3 Hz				
Divider Mode		<3.5 GHz output, resolution depends on VCO output divider setting		$f_{PD}/(2^{24} \times$ output divider)		Hz
Integer Boundary Spurs				−45		dBc
Phase Detector Spurs				−105		dBc
Reference Spurs				−100		dBc
Normalized Inband Phase Noise Floor Figure of Merit (FOM)		Normalized to 1 Hz				

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Floor Integer Mode				−229		dBc/Hz
Floor High Current Mode[18] Integer Mode				−232		dBc/Hz
Floor Fractional Mode				−226		dBc/Hz
Floor High Current Mode Fractional Mode				−229		dBc/Hz
Flicker Noise (Integer Mode and Fractional Mode)				−268		dBc/Hz
Integrated RMS Jitter				<40		fs
VCO CHARACTERISTICS						
VCO Tuning Sensitivity at RFOUT		Measured on RFOUT (VT = 1.65 V)				
7300 MHz				101		MHz/V
9000 MHz				80		MHz/V
11000 MHz				128		MHz/V
13000 MHz				109		MHz/V
14600 MHz				96		MHz/V
Tune Port Capacitance		VT = 0.5 V dc		175		pF
		VT = 1.65 V dc		154		pF
		VT = 2.8 V dc		135		pF
Autocalibration Delay (Enable or Disable)		VCO Register 0x00, Bit 0 switch time (VT to VPRST)		10		ns
VCO OUTPUT DIVIDER						
VCO RF Divider Range		1, 2, 4, 6, 8, … 128	1		128	
VCO Supply Pushing (VCOVCC)[1]		PDIV_OUT and NDIV_OUT, divide by 1, VT = 1.65 V		0.7		MHz/V
VCO Supply Pushing (VDD1)[17]		PDIV_OUT and NDIV_OUT, divide by 1, VT = 1.65 V		67		MHz/V
RETURN LOSS						
RFOUT				5		dB
PDIV_OUT (N > 1)				14		dB
NDIV_OUT (N > 1)				14		dB

[1] Pushing refers to a change in VCO frequency due to a change in the power supply voltage. To derive pushing at other divide ratios, divide the nominal pushing value by the divide ratio.
[2] Pulling refers to a change in VCO frequency due to a change in the load impedance.
[3] Measured with 100 Ω external termination. See the Reference Input Stage section for more details.
[4] Slew rate of ≥0.5 ns/V is recommended. See the Reference Input Stage section for more details. Frequency is guaranteed across process voltage and temperature from −40°C to +85°C.
[5] This maximum PD frequency can only be achieved if the minimum N value is respected. For example, in the case of fractional mode, the maximum PD frequency = f_{VCO}/20 or 100 MHz, whichever is less.
[6] External 1 kΩ pull-up resistor to 1.8 V.
[7] Limited by the 1 kΩ pull-up resistor and NMOS R_{ON}.
[8] 10 pF load capacitor.
[9] 10 pF load capacitor, 1 kΩ pull-up resistor. In general, open-drain mode can support higher frequencies at the expense of maximum V_{OL}. The maximum frequency for a given pull-up resistor and load capacitor is approximately $1/(10 \times R_{PULL\text{-}UP} \times C_{LOAD})$. For example, a 10 pF load capacitor and 1 kΩ pull-up resistor can support up to 10 MHz, where V_{OL} maximum = $V_{DD} \times R_{ON}/(1\ k\Omega + R_{ON}) \approx 164$ mV. With a 500 Ω pull-up resistance and a 10 pF load, a 20 MHz maximum frequency is possible, and the maximum V_{OL} increases to 300 mV.
[10] 1 kΩ pull-up resistor.
[11] The minimum resistive load to ground in CMOS mode is 1 kΩ.
[12] The SDO pin does not have short-circuit protection. Do not exceed the maximum current of 7.2 mA under any condition.
[13] C_{LOAD} is the capacitive load in pF. C_{LOAD} maximum = 20 pF. For example, with a 5 pF capacitive load, the rise time is 0.5 + 0.3 × 5 = 2 ns.
[14] Values shown are the product of the prescaler divide ratio × N counter value.
[15] VCCPD and VDDLS can be operated at 3.6 V maximum to increase band and VCO core overlap and extend the upper end of the frequency range. The typical current is expected to be less than 1.5 mA. Both must be equal. Therefore, if one changes, so must the other. Exceeding 3.6 V results in ESD diodes drawing current.
[16] Reference disconnected.
[17] Some circuits remain on.
[18] High current mode is a register setting that is enabled and works in conjunction with the functional mode in which the device is operating (integer mode or fractional mode).

TIMING SPECIFICATIONS

SPI Open Mode: Write Timing Characteristics

AVDD = DVDD = 3.3 V, exposed pad (EPAD) = 0 V. See Figure 30.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	Serial data input (SDI) setup time to SCK rising edge	3			ns
t_2	Serial clock (SCK) rising edge to SDI hold time	3			ns
t_3	Serial enable (SEN) low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCK 32nd rising edge to SEN rising edge	10			ns
t_6	Recovery time (not shown in Figure 30)	20			ns
f_{SCK}	Maximum SPI clock speed		50		MHz

SPI Open Mode: Read Timing Characteristics

AVDD = DVDD = 3.3 V, EPAD = 0 V. See Figure 31 and Figure 32.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI setup time to SCK rising edge.	3			ns
t_2	SCK rising edge to SDI hold time.	3			ns
t_3	SEN low duration.	10			ns
t_4	SEN high duration.	10			ns
t_5[1]	SCK rising edge to SDO time. Add 0.2 ns for each pF of C_{LOAD}.			8.2	ns
t_6	Recovery time.	10			ns
t_7	SCK 32nd rising edge to SEN rising edge.	10			ns

[1] An extra 0.2 ns delay is required for every 1 pF load on SDO.

SPI Legacy Mode: Write Timing Characteristics

AVDD = DVDD = 3.3 V ± 10%, analog ground (AGND) = digital ground (DGND) = 0 V. See Figure 28.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
t_1	SEN to SCK setup time	8			ns
t_2	SDI to SCK setup time	3			ns
t_3	SCK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
Maximum SPI Clock Frequency				50	MHz

SPI Legacy Mode: Read Timing Characteristics

AVDD = DVDD = 3.3 V, ±10%, AGND = DGND = 0 V. See Figure 29.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
t_1	SEN to SCK setup time	8			ns
t_2	SDI to SCK setup time	3			ns
t_3	SCK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCK to SDO delay. Add 0.2 ns for each pF of C_{LOAD}			8.2	ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to GND, DVDD to GND	−0.3 V to +3.6 V
AVDD to DVDD	−0.5 V to +0.5 V
VDDLS, VPPCP to GND	−0.3 V to +3.8 V
VDDLS to VPPCP[1]	−0.5 V to +0.5 V
RVDD, VCCPD, VCCPS, VCCHF to GND	−0.3 V to +3.6 V
XREFP	18 dBm, 5.6 V peak
Minimum Digital Load	1.0 kΩ
Digital Input 1.4 V to 1.7 V Minimum Rise Time	20 ns
Digital Input Voltage Range	−0.25 V to DVDD + 0.5 V
VDD1, VDD2, VDD3	−0.3 V to +3.6 V
VCOVCC	−0.3 V to +5.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +120°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Electrostatic Discharge (ESD)	
Charged Device Model	500 V
Human Body Model	1000 V

[1] VDDLS must be equal to VPPCP.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CC-48-1	31.2	6.9	°C/W

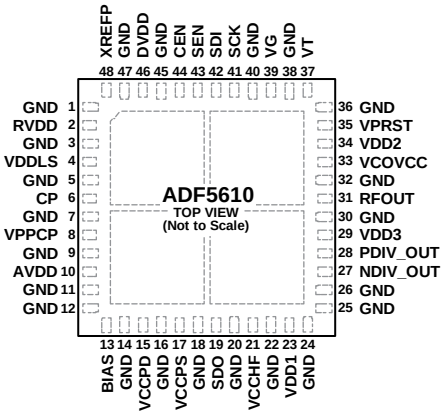
[1] Thermal impedance measured values are based on use of a 2S2P board with the thermal impedance pad (EPAD) soldered to GND (GND = 0 V). A cold plate is set to 20°C and attached to the bottom side of the PCB using 100 µm thermal interface material (3.56 W/mK).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD OR GROUND PADDLE ON THE BACKSIDE OF THE PACKAGE MUST BE TIED TO DC GROUND FOR ELECTRICAL, MECHANICAL, AND THERMAL REASONS. NOTE THAT RF GROUND AND DC GROUND ARE THE SAME IN THIS CASE.

16799-007

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 24 to 26, 30, 32, 36, 38, 40, 45, 47	GND	Ground.
2	RVDD	Reference Path Supply. 3.3 V ± 5%.
4	VDDLS	Power Supply for Charge Pump Digital Section. 3.3 V ± 5% typical, 3.6 V maximum. VDDLS must be equal to VPPCP.
6	CP	Charge Pump Output. Place first pole of low-pass loop filter close to this pin if loop filter path is electrically long.
8	VPPCP	Power Supply for Charge Pump. 3.3 V ± 5% typical, 3.6 V maximum. VPPCP must be equal to VDDLS.
10	AVDD	Analog Supply. 3.3 V ± 5%. AVDD must be equal to DVDD.
13	BIAS	External Bypass Decoupling for Precision Bias Circuits. Note that the 1.920 V ± 20 mV reference voltage is generated internally and cannot drive an external load. The reference voltage must be measured with a 10 GΩ meter, such as the Agilent 34410A. A normal 10 MΩ digital voltmeter reads erroneously.
15	VCCPD	Phase Detector Supply. 3.3 V ± 5%.
17	VCCPS	Prescaler Supply. 3.3 V ± 5%.
19	SDO	Serial Data Output. Lock detect and various other functions are available via an internal mux.
21	VCCHF	Power Supply for PLL RF Section. 3.3 V ± 5%. Place a decoupling capacitor as close as possible to this pin.
23	VDD1	Bias for VCO Digital Logic, VG Pin, SPI Buffer, and Input Buffer to PLL. Nominally 3.3 V ± 5%. Retain bias to hold the VCO register contents when the VCO is powered down.
27	NDIV_OUT	Complementary Output of Differential Frequency Divider. N = 1, 2, 4, 8, 16, 32, 64, or 128. DC block required. A broadband 100 nF capacitor is recommended.
28	PDIV_OUT	Primary Output of Differential Frequency Divider. N = 1, 2, 4, 8, 16, 32, 64, or 128. DC block required. A broadband 100 nF capacitor is recommended.
29	VDD3	Differential Output Divider Supply. 3.3 V ± 5%.
31	RFOUT	RF Output (7300 MHz to 14,600 MHz). Internal dc block. DC block using a broadband 100 nF capacitor.
33	VCOVCC	VCO Power Supply. 5.0 V ± 5%.
34	VDD2	Reference Voltage Supply. 3.3 V ± 5%.
35	VPRST	Temperature Dependent, Calibration Preset. Decouple with a 470 nF capacitor.
37	VT	VCO Tuning Port. 0 V to 3.6 V, ± 5%. Place last pole of low-pass filtered charge pump output close to this pin if loop filter path is electrically long.

Pin No.	Mnemonic	Description
39	VG	Gate Voltage Bypassing. Decouple to GND with a low effective series resistance (ESR), 10 µF capacitor.
41	SCK	Serial Port Interface Clock Input.
42	SDI	Serial Port Data Input.
43	SEN	Serial Port Interface Enable Input. Active high.
44	CEN	Hardware Chip Enable Input. Active high. Logic low powers down the PLL section.
46	DVDD	Digital Power Supply. 3.3 V ± 5%. Retain bias to hold the PLL register contents when powering down the PLL.
48	XREFP	External Reference Input. For 50 Ω match, ac couple to the XREFP pin using a low reactance capacitor value and add a 100 Ω resistor to ground.
	EPAD	Exposed Pad. The exposed pad or ground paddle on the backside of the package must be tied to dc ground for electrical, mechanical, and thermal reasons. Note that RF ground and dc ground are the same in this case.

TYPICAL PERFORMANCE CHARACTERISTICS

For Figure 3 through Figure 7, Agilent E5052B is the test equipment used to measure the phase noise.

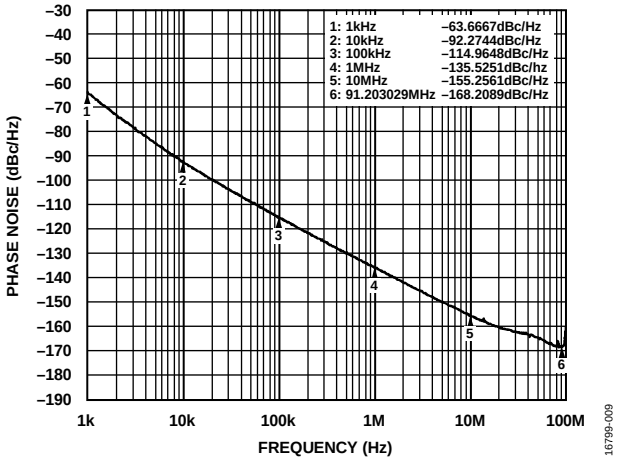


Figure 3. Open-Loop VCO Phase Noise at 7300 MHz, RFOUT, High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal)

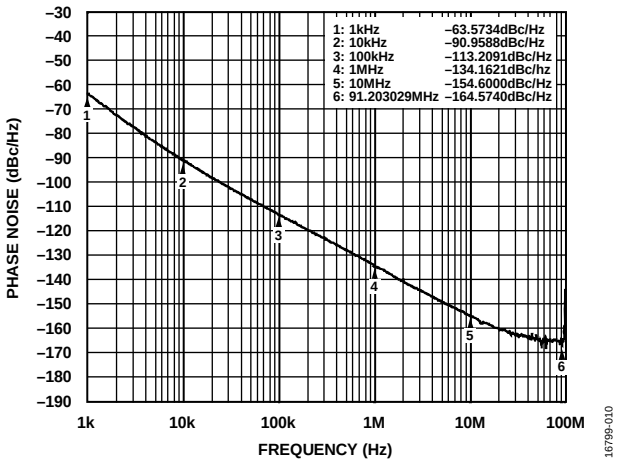


Figure 4. Open-Loop VCO Phase Noise at 10000 MHz, RFOUT, High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

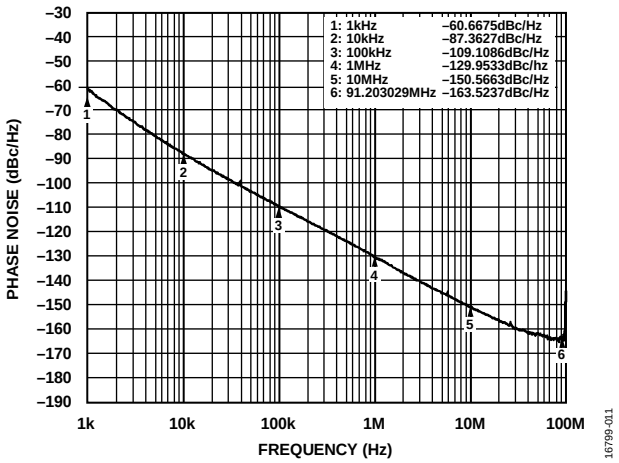


Figure 5. Open-Loop VCO Phase Noise 14.6 GHz, RFOUT, High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

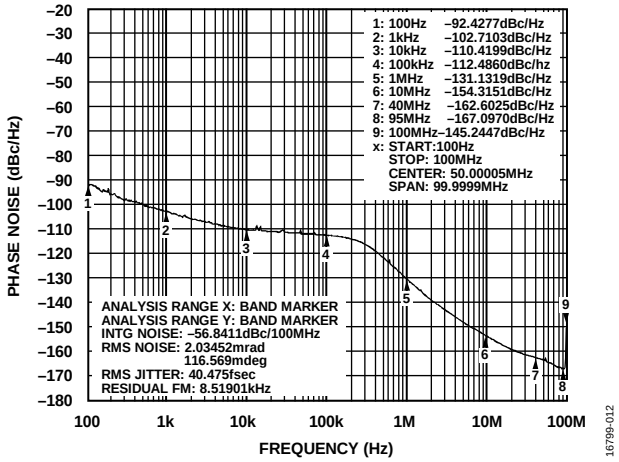


Figure 6. Closed-Loop Phase Noise Illustrating Low Jitter Capability at 8.0 GHz, Wenzel 100 MHz Reference, 100 MHz PFD, RFOUT, High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal)), 25°C

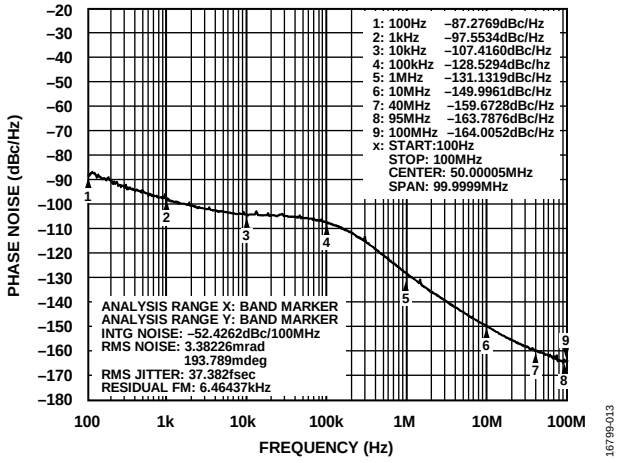


Figure 7. Closed-Loop Phase Noise Illustrating Low Jitter Capability at 14.4 GHz, Wenzel 100 MHz Reference, 100 MHz PFD, RFOUT, High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal)), 25°C

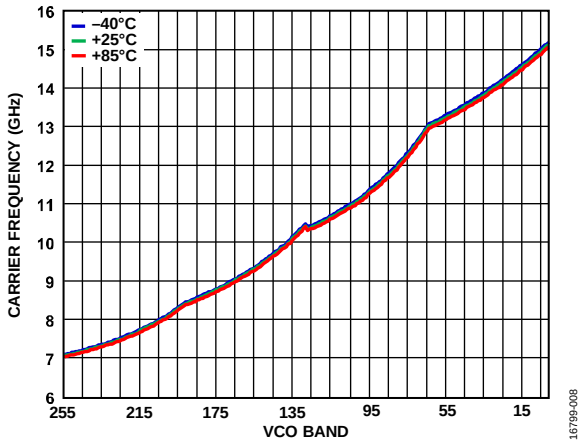


Figure 8. Carrier Frequency vs. VCO Band, Autocalibration Enabled, VDDLS = 3.3 V, VPPCP = 3.3 V

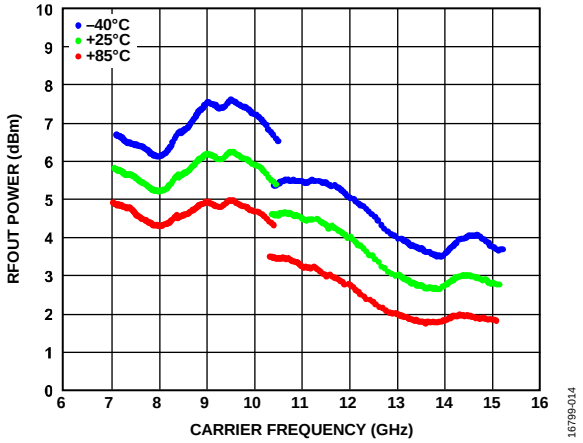


Figure 9. RFOUT Power vs. Carrier Frequency, Maximum Output Gain = (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

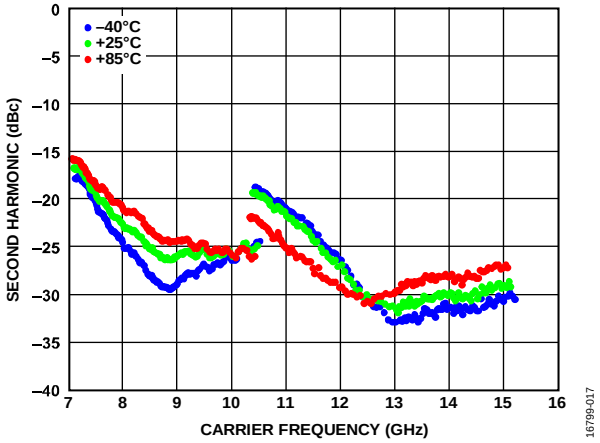


Figure 12. Second Harmonic vs. Carrier Frequency at RFOUT, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

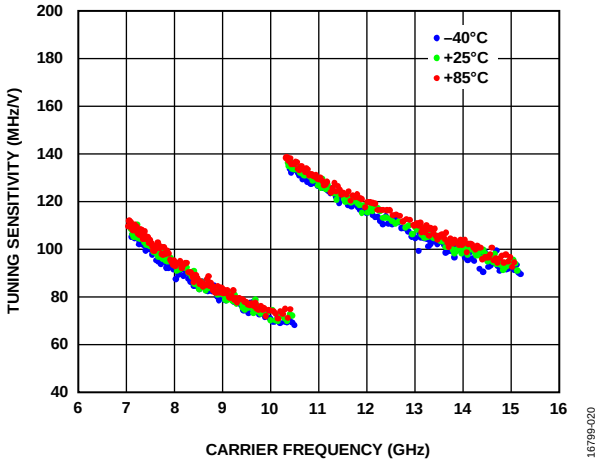


Figure 10. Tuning Sensitivity vs. Carrier Frequency, VT = 1.65 V, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

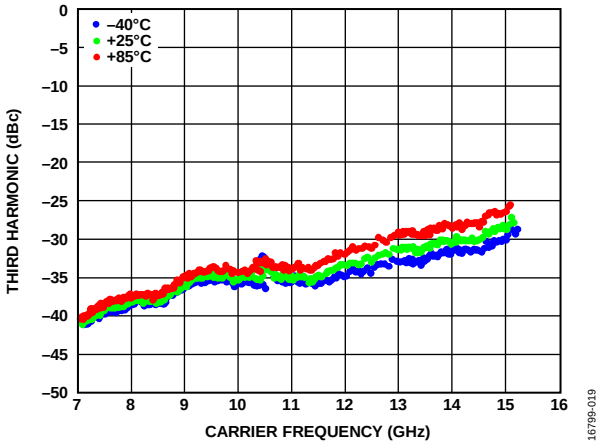


Figure 13. Third Harmonic vs. Carrier Frequency, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

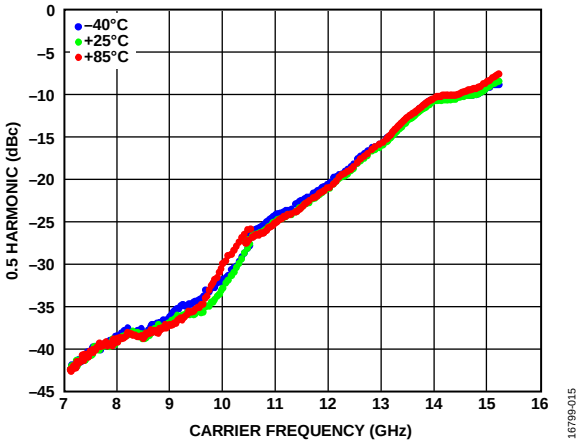


Figure 11. 0.5 Harmonic vs. Carrier Frequency (Fundamental Feedthrough at RFOUT), Maximum Output Gain = (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

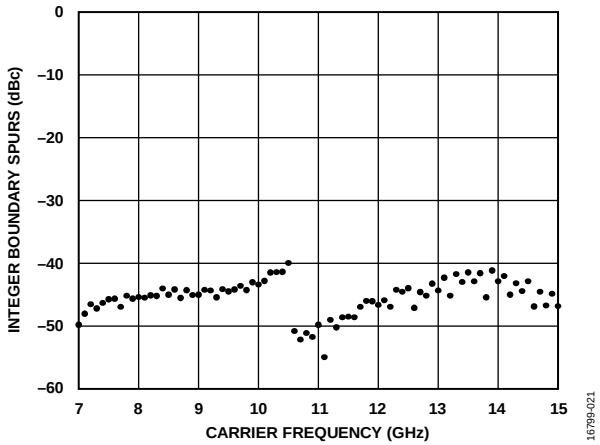


Figure 14. Integer Boundary Spurs (IBS) vs. Carrier Frequency, 10 kHz Spur, 100 kHz Loop, 50 MHz PFD, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal)), Low Current Mode (VCO Register 0x01, Bits[4:2] = 0 (Decimal))

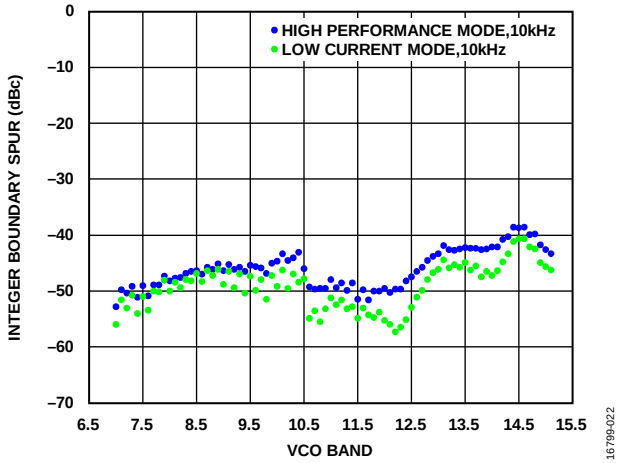


Figure 15. Integer Boundary Spur vs. VCO Band, 20 kHz Spur, 100 kHz Loop, 50 MHz PFD, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal)), Low Current Mode (VCO Register 0x01, Bits[4:2] = 0 (Decimal)

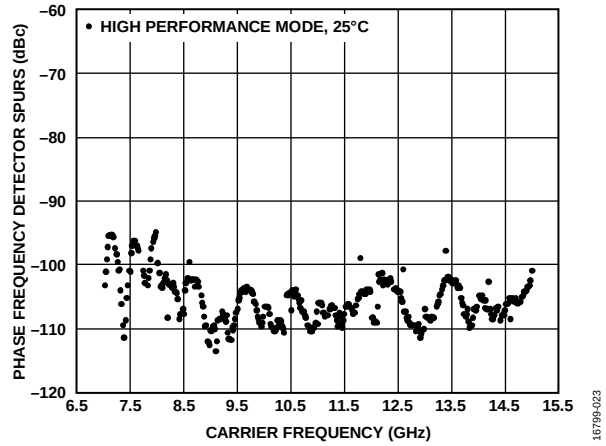


Figure 16. Phase Frequency Detector Spurs vs. Carrier Frequency, 100 MHz PFD Frequency, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

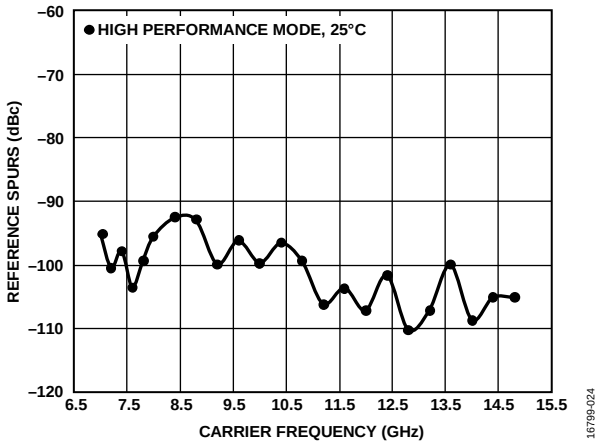


Figure 17. Reference Spurs vs. Carrier Frequency, 100 MHz PFD Frequency, Maximum Output Gain (VCO Register 0x01, Bits[1:0] = 3 (Decimal)), High Performance Mode (VCO Register 0x01, Bits[4:2] = 7 (Decimal))

THEORY OF OPERATION

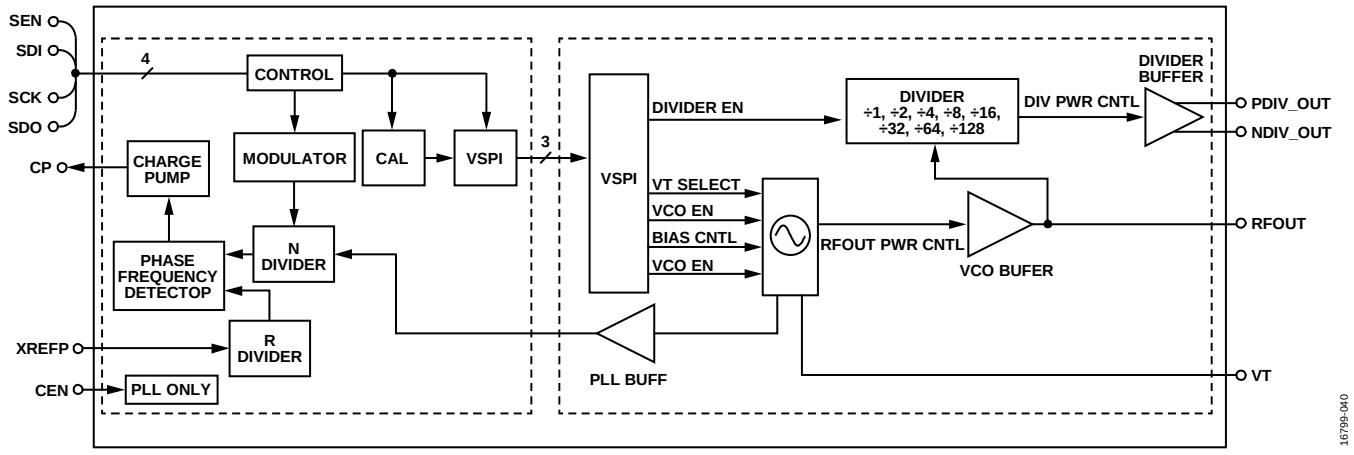


Figure 18. PLL and VCO Subsystems

The ADF5610 PLL with integrated VCO is composed of two subsystems, a PLL subsystem and a VCO subsystem, as shown in Figure 18.

PLL SUBSYSTEM OVERVIEW

The PLL subsystem divides down the VCO output to the desired comparison frequency via the N divider (integer value set in Register 0x03, fractional value set in Register 0x04), compares the divided VCO signal to the divided reference signal (reference divider set in Register 0x02) in the phase detector (PD), and drives the VCO tuning voltage via the charge pump (CP) (configured in Register 0x09) to the VCO subsystem. Some of the additional PLL subsystem functions include

- Δ-Σ configuration (Register 0x06).
- Exact frequency mode (configured in Register 0x0C, Register 0x03, and Register 0x04).
- LD configuration (use Register 0x07 to configure LD and Register 0x0F to configure the SDO output pin).
- External CEN pin used for the hardware PLL enable pin. The CEN pin does not affect the VCO subsystem.

Only writes to the divider registers of the PLL subsystem are required for ADF5610 output frequency changes.

The divider registers of the PLL subsystem (Register 0x03 and Register 0x04) set the fundamental frequency (3650 MHz to 7300 MHz) of the VCO subsystem. Output frequencies ranging from 57 MHz to 14,600 MHz are generated by tuning to the appropriate fundamental VCO frequency (3650 MHz to 7300 MHz), by programming the N divider (Register 0x03 and Register 0x04), and programming the output divider (divide by 1 to 128, in VCO Register 0x02) in the VCO subsystem. Depending on the step size, high performance applications may require one or more additional register writes to optimize spurs, loop bandwidth and settling time, or to set the lock detect window at the new frequency.

For detailed frequency tuning information and an example, see the Frequency Tuning section.

VCO SUBSYSTEM OVERVIEW

The VCO subsystem consists of a switched capacitor, step tuned VCO, and an output stage. The topology of the VCO allows both fundamental and doubled frequency outputs. This arrangement allows the lower, fundamental frequency of the oscillator to be routed to the input of the PLL, which reduces the N counter of the PLL by a factor of 2. This reduction of the N counter results in not only a 3 dB improvement in the close in-phase noise, but also prevents residual phase noise degradation at offsets beyond 10 MHz.

The VCO tuning is a two-step process consisting of a coarse then fine tune. During normal operation, autocalibration is enabled (Register 0x0A, Bit 11), which allows the PLL finite state machine (FSM) to perform a binary search of the VCO bands (coarse tune). After the proper band is located, the charge pump output from the PLL takes control of the tuning port (VT) on the VCO and adjusts to the proper fundamental frequency (3650 MHz to 7300 MHz), and is phase locked by the PLL.

The VCO subsystem controls the output stages of the ADF5610, enabling configuration of the following:

- User defined performance settings (see the Programmable Performance Technology section) that are configured via VCO Register 0x01, Bits[4:2].
- VCO output divider settings that are configured in VCO Register 0x02, Bits[2:0] (divide by 2 to 128 to generate frequencies from 3650 MHz to 57 MHz, respectively) or divide by 1 to generate frequencies between 7300 MHz and 14,600 MHz.
- RFOUT gain settings (VCO Register 0x01, Bits[1:0]).
- PDIV_OUT and NDIV_OUT gain settings (VCO Register 0x01, Bits[6:5]).
- Power down VCO (VCO Register 0x02, Bit 3).
- Power down divider (VCO Register 0x01, Bit 8).

SPI CONFIGURATION OF PLL AND VCO SUBSYSTEMS

The two subsystems (PLL and VCO) each have their own register maps, as shown in the Serial Port Interface section and the VCO Subsystem Register Map section. Typically, writes to both register maps are required for initialization and frequency tuning operations.

As shown in Figure 18, the PLL subsystem is connected directly to the SPI interface of the ADF5610, whereas VCO SPI commands are passed through the PLL subsystem to the ADF5610 VCO. As a result, writes to the PLL register map are written directly and immediately, whereas the writes to the VCO subsystem register map are written to PLL Register 0x05 and forwarded via the internal VCO SPI (VSPI) to the VCO subsystem, which is a form of indirect addressing.

The VCO registers are write only and cannot be read. However, the VCO tuning band that is currently enabled can be read back via PLL Register 0x0A. For more information, see the VCO Serial Port Interface (VSPI) section.

VCO Serial Port Interface (VSPI)

The ADF5610 communicates with the internal VCO subsystem via an internal 16-bit VSPI. The internal serial port controls the step tuned VCO and other VCO subsystem functions.

The internal VSPI runs at the rate of the autocalibration FSM clock (t_{FSM}) (see the VCO Autocalibration section), where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by PLL Register 0x0A, Bits[14:13].

Writes to the control registers of the VCO are handled indirectly via writes to Register 0x05 of the ADF5610. A write to Register 0x05 causes the internal PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where the packet is interpreted.

VSPI Use of Register 0x05

The packet data written into Register 0x05 is subparsed by logic at the VCO subsystem into the following three fields:

- Field 1, Bits[2:0]: 3-bit VCO_ID, target subsystem address = 000b.
- Field 2, Bits[6:3]: 4-bit VCO_REGADDR, the internal register address inside the VCO subsystem.
- Field 3, Bits[15:7]: 9-bit VCO_DATA, the data field to write to the VCO register.

For example, to write 0 0000 0110 into VCO Register 0x02 of the VCO subsystem (VCO_ID = 000b) and set the VCO output divider to divide by 2, the following must be written to Register 0x05.

- 0b (VCO_DATA, Bit 15)
- 0000b (VCO_DATA, Bits[14:11])
- 0110b (VCO_DATA, Bits[10:7])
- 0010b (VCO_REGADDR)
- 000b (VCO_ID)

When concatenated, the result is Register 0x05 = 0x0310.

During autocalibration, the autocalibration controller writes into the VCO register address specified by the VCO_ID and VCO_REGADDR, as stored in Register 0x05, Bits[2:0] and Register 0x05, Bits[6:3], respectively. Autocalibration requires that the values for VCO_ID be zero (Register 0x05, Bits[2:0] = 0). When the VCO_ID values are not zero (Register 0x05, Bits[2:0] ≠ 0), autocalibration does not function. Because VCO Register 0x00 is the register that manages the VCO bands and frequencies, Register 0x05, Bits[6:0] = 0.

To ensure that frequency changes can occur after configuring the VCO subsystem settings in Register 0x05, it is critical to write Register 0x05, Bits[6:0] = 0 after the last VCO subsystem write, but prior to the output frequency change. The frequency change is triggered by the final PLL register write, which is Register 0x03 for integer values or Register 0x04 for fractional frequencies. Register 0x03 must be the last write in integer mode because it triggers autocalibration to implement a frequency change. When operating in fractional mode, Register 0x04 is written last to trigger autocalibration to make a frequency change. If the last write to Register 0x05, Bits[6:0] ≠ 0), autocalibration does not function.

Note that it is impossible to write only Register 0x05, Bits[6:0] = 0 (VCO_ID and VCO_REGADDR) without also writing to VCO_DATA (Register 0x05, Bits[15:7]). Therefore, if it is desired to remain in the existing VCO band and only change the divide ratio (see previous example), the user must ensure that VCO_DATA (Register 0x05, Bits[15:7]) is not changed. To accomplish this, it is required to read the band settings provided in Register 0x10, Bits[7:0], and then rewrite them to Register 0x05, Bits[15:7] as follows:

1. Read Register 0x10.
2. Write the following to Register 0x05:
    a. Register 0x05, Bits[15:14] = Register 0x10, Bits[7:6].
    b. Register 0x05, Bit 13 = 1 (reserved bit).
    c. Register 0x05, Bits[12:8] = Register 0x10, Bits[4:0].
    d. Register 0x05, Bits[7:0] = 0.

Changing the VCO subsystem configuration (see the VCO Subsystem Register Map section) without following the preceding procedure results in a failure to lock to the desired frequency.

For applications not using the read functionality of the ADF5610 SPI, in which Register 0x10 cannot be read, it is possible to write Register 0x05 = 0 to set Register 0x05, Bits[6:0] = 0, which also sets the VCO subband setting equal to zero (Register 0x05, Bits[15:7] = 0), effectively programming an incorrect VCO subband settings and causing the ADF5610 to lose lock. This procedure is then immediately followed by a write to the following:

- Register 0x03, if in integer mode
- Register 0x04, if in fractional mode

This write effectively retriggers the FSM, forcing the ADF5610 to relock whether in integer mode or fractional mode.

Lock times within 10° of phase settling as low as 30 µs can be achieved, but are dependent on both the loop filter design (loop filter bandwidth and loop filter phase margin) and the configuration of the autocalibration register (Register 0x0A).

For applications where lock time is critical, it is recommended that lock time be verified at the operating temperature extremes.

VCO SUBSYSTEM

See Figure 19 and Figure 20.

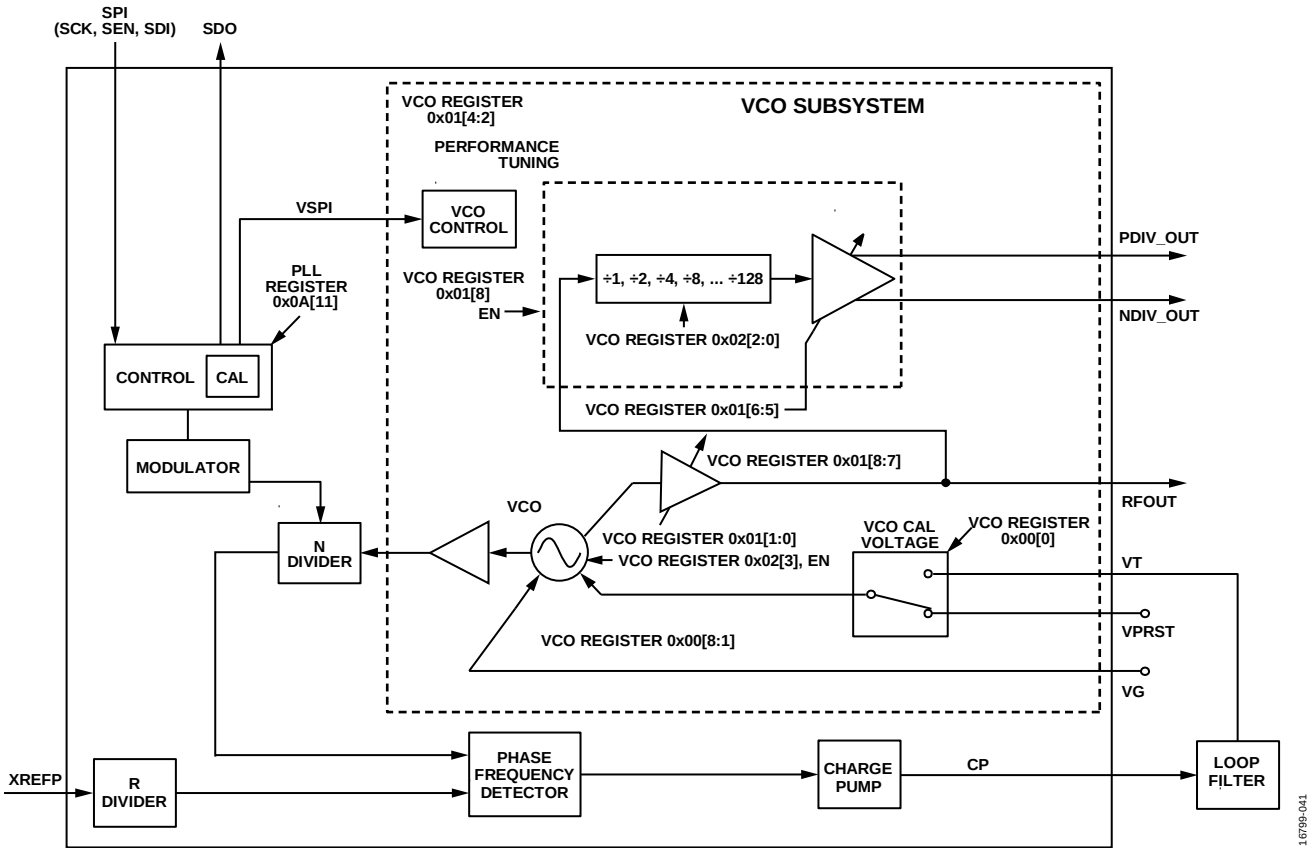


Figure 19. Detail of PLL and VCO Subsystems

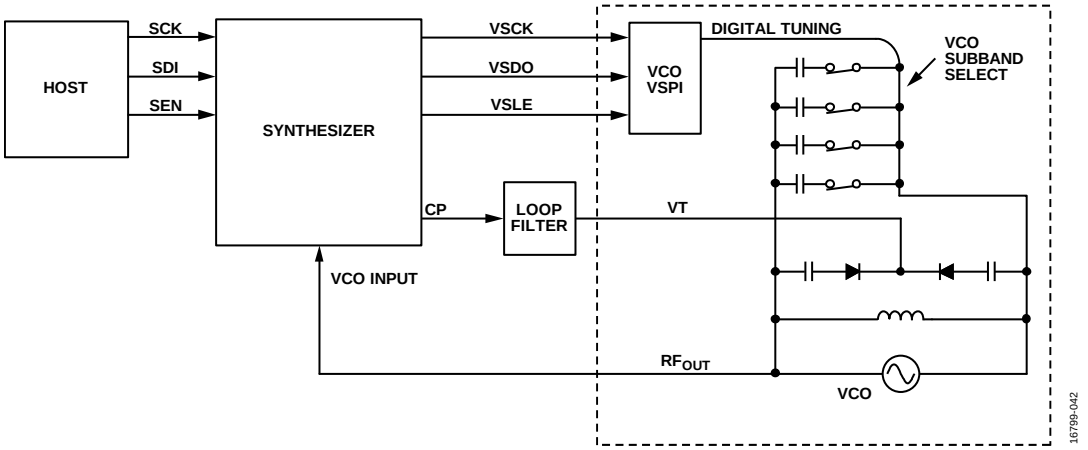


Figure 20. Simplified Step Tuned VCO

The ADF5610 contains a VCO subsystem that can be configured to provide the following output frequencies:

- Fundamental frequency (f_O) mode (3650 MHz to 7300 MHz) is available at the differential outputs by setting the output frequency divider to N = 2.
- The push/push (doubled) frequency is always available at RFOUT. The push/push frequency is also available at the differential outputs by setting N = 1 to bypass the divider.
- Divide by N mode, where N = 1, 2, 4, 6, 8 … 32, 64, 128 (57 MHz to 1750 MHz).
- All modes are VCO register programmable, as shown in Figure 19. One loop filter design can be used for the entire frequency of operation of the ADF5610.

VCO Calibration

VCO Autocalibration

The ADF5610 incorporates a step tuned VCO. A simplified step tuned VCO is shown in Figure 20. Step tuned VCOs are unique because they incorporate not only varactor diodes for frequency tuning, but also a digitally selectable, binary bank of capacitors. This bank of capacitors, along with the varactor diodes, defines the frequency range of each subband within a given VCO core. The ADF5610 contains two VCO cores, each with their own bank of capacitors. Multiple VCO cores allow not only broader frequency coverage, but also more consistent tuning sensitivity across the band.

As capacitors are selected or deselected within the bank, the nominal center frequency of the VCO tank circuit is stepped up or stepped down. Multiple capacitors can be changed at once or one at a time if required. Essentially, the capacitor banks provide coarse frequency tuning in the form of 128 subbands within each VCO core while the varactor diodes manage fine tuning within each of these subbands. To guarantee continuous frequency coverage over process, voltage, and temperature (PVT), the ends of each frequency subband and each VCO core overlap.

The frequency overlap implies that certain frequencies exist in more than one subband. It is known that the frequency of a VCO varies (drifts) with temperature. Selection of a subband where the desired frequency is too close to the edge may lead to loss of lock if the operating temperature change is large enough and in a direction that allows the frequency to drift beyond the edge of the subband. During normal operation, the ADF5610 is designed to remain locked and in the same band as long as the temperature remains within the specified operating range. During manual calibration (autocalibration disabled, refer to the Manual VCO Calibration for Fast Frequency Hopping section), it is possible to select a band where the desired frequency exists, but is too close to the transition point where multiple bands overlap. Having the frequency too close to the transition point may result in the selection of a different band as the operating temperature changes. If automatic relock is enabled (Register 0x07, Bit 13 = 1), the autocalibration routine runs one additional time in an attempt to relock the synthesizer. This temporary loss of lock results in a phase hit during this transition period. Phase hits are unacceptable for many applications. If a different band is selected upon relock, the tuning sensitivity changes slightly, resulting in a minor shift to the 3 dB corner for the loop filter. A different band results in a minor change to phase settling time and spurious suppression. If the loss of lock was initially due to selection of a band where the frequency is near the band edge, the accompanying tuning voltage may be close to the charge pump rail. As the charge pump approaches its limits of operation (rails), its performance becomes nonlinear, resulting in increased spurious and PLL FOM and consequently degrades phase noise performance at frequency offsets inside the loop filter bandwidth.

The ADF5610 simultaneously solves these potential issues by integrating a temperature compensation circuit within the autocalibration routine. This circuit produces a very low noise, temperature dependent voltage, and depending on the state of the autocalibration bit (VCO Register 0x00, Bit 7), routes the voltage to the tuning port of the VCO during the autocalibration process. When the operating temperature of the ADF5610 is low (−40°C), a band where the desired frequency occurs at a low tune voltage is required so that as the temperature increases, higher tune voltages are available. Likewise, when the ADF5610 is operating at high temperatures (85°C), a band where the desired frequency falls at a higher tune voltage is needed to maintain lock as the temperature drops. The reference voltage used for band selection ranges linearly from about 0.85 V dc at −40°C to 1.75 V dc at +85°C. The voltage range, which is centered around 1.3 V dc at room temperature, is offset with respect to the available tune voltage range of 0 V dc to 3.3 V dc. This offset allows additional voltage at the upper end of each VCO core to compensate for the reduction in tuning sensitivity. By limiting the voltage range from approximately 0.85 V dc to 1.70 V dc, bands are selected that allow operation away from the charge pump rails over the full operating temperature range. Band selection where tuning voltage falls from 0.85 V dc to 1.70 V dc allows phase lock using a single subband over temperature extremes (lock and leave) to be met as long as sufficient charge pump voltage exists to compensate for the frequency drift. Some applications may require increasing the charge pump supply (VPPCP) and the charge pump digital supply level shifter (VDDLS) to 3.6 V dc to meet lock and leave requirements. Note that the voltage for the VPPCP and VDDLS must be equal. Phase lock is maintained within a single VCO core and VCO subband over the full temperature range (−40°C to +85°C) regardless of the operating temperature when autocalibration initially selected the subband.

When the ADF5610 PLL receives a request to change the frequency such that a new VCO band must be selected, the process is as follows. Note that the PLL portion of the autocalibration circuitry, the FSM, is assumed to already be enabled (Register 0x0A, Bit 11 = 0).

1. The PLL registers that must be updated to facilitate lock at the new frequency as well as any changes to the VCO registers (gain settings, divide ratio) are sent to the ADF5610 via the SPI. There is no need for users to change the VCO autocalibration bit when changing frequencies. The VCO autocalibration bit state is handled automatically when PLL Register 0x0A, Bit 11 = 0.
2. The FSM takes control of the VCO autocalibration bit (VCO Register 0x00, Bit 7), changing the bit from 0 to 1, temporarily opening the loop filter path and switching the source of the VT pin from the charge pump to the VPRST pin.
3. With VT set to a value that provides optimal performance, the PLL FSM begins a binary search for the VCO core and subband with a frequency that is closest to the desired frequency. Note that the setting for the VT resolution (Register 0x0A, Bits[2:0]) can impact band selection as well as the ability to retain lock over the full operating temperature range. When in doubt, use the highest setting for the best resolution.
4. After the proper band has been determined, the VCO autocalibration bit (VCO Register 0x00, Bit 7) changes from 1 back to 0, closing the loop filter path and returning the source of the VT pin to the charge pump.
5. The new VCO frequency is then routed to the input of the PLL, divided down, and compared to the reference frequency. The charge pump adjusts the VCO tuning voltage as necessary to phase lock the divided down VCO frequency to the reference frequency.

The temperature compensated voltage that is used during autocalibration is transferred to the VPRST pin (Pin 35) of the ADF5610. This voltage correlates to the temperature of the silicon and can be used for a real-time estimate of the junction temperature of the die. The voltage at VPRST is a function of the ambient temperature as well as the PCB design and assembly quality. Take caution if it is desired to continuously monitor this voltage. The VPRST pin is tied to a low noise circuit, and although the internal switch has sufficient isolation, it may still allow external noise to be coupled onto the precision reference circuit, which results in unwanted spurs, sidebands, and degraded phase noise.

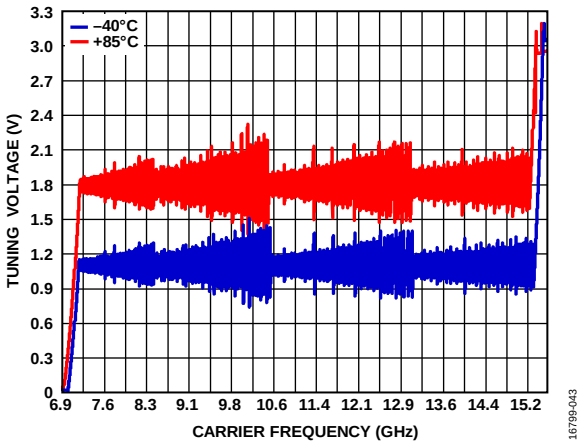


Figure 21. Tuning Voltage vs. Carrier Frequency After Calibration, Maximum Tuning Resolution, Register 0x0A, Bits[2:0] = 7

Although the digital VCO bands are automatically controlled by the ADF5610 using the autocalibration feature, the VCO bands can also be controlled directly via Register 0x05 for testing or for special purpose operations. Other control bits specific to the VCO are also sent via Register 0x05. Refer to the VCO Subsystem Register Map section for further details.

As mentioned in the VCO Subsystem Overview section, during autocalibration, coarse tuning is provided by the FSM as it selects the most appropriate band for operation over the full operating temperature range. Fine tuning is achieved by varactor diodes after the VCO autocalibration bit (VCO Register 0x00, Bit 7) is reset by the FSM. The reset gives control of the tuning voltage back to the phase detector and charge pump. When the band is selected, a narrow voltage range on the varactor is all that is needed for phase lock. Note that the tuning voltage stays in a narrow range over a wide range of output frequencies.

The calibration is normally run automatically, once for every change of frequency. Autocalibration ensures optimum selection of VCO band settings vs. time and temperature. The user does not need to be concerned about which band setting is used for a given frequency because this selection is handled by the autocalibration routine.

The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the step setting where the desired frequency falls within the frequency range (determined by the FSM resolution setting) that is centered around the temperature compensated VPRST value being used during the search. When located, the loop filter path is closed and the VCO is locked at the programmed frequency. If the proper resolution is used, the VCO remains locked and operates away from the charge pump rails over its full temperature range without additional calibration, regardless of the temperature at which the VCO was calibrated. Note that when autocalibration is enabled, preselection of the VCO core that autocalibration starts in is not possible.

Autocalibration can be disabled, thereby allowing manual band selection and even faster VCO tuning. Refer to the Manual VCO Calibration for Fast Frequency Hopping section for more information about manual tuning.

Autocalibration Using Register 0x05

Autocalibration transfers band control data to the VCO subsystem via Register 0x05. The address of the VCO subsystem in Register 0x05 is not altered by the autocalibration routine. The address and ID of the VCO subsystem in Register 0x05 must be set to the correct value before autocalibration is executed. For more information, see the VCO Serial Port Interface (VSPI) section.

Automatic Relock on Lock Detect Failure

It is possible, by setting Register 0x07, Bit 13, to have the VCO subsystem automatically rerun the calibration routine and relock itself if the lock detect bit indicates an unlocked condition for any reason. With this option, the system attempts to relock only once.

VCO Autocalibration on Frequency Change

Assuming Register 0x0A, Bit 11 = 0, the VCO calibration starts automatically whenever a frequency change is requested. To rerun the autocalibration routine for any reason at the same frequency, rewrite the frequency change with the same value, and the autocalibration routine executes again without changing the final frequency.

VCO Autocalibration Time and Accuracy

The VCO frequency is counted for the period of a single autocalibration measurement cycle (t_{MMT}).

$$t_{MMT} = t_{XTAL} \times R \times 2^n \quad (1)$$

where:
t_{XTAL} is the period of the external reference (crystal) oscillator.
R is the reference path division ratio currently in use, set in Register 0x02.
n is set by Register 0x0A, Bits[2:0] and results in measurement periods that are multiples of the PD period, $t_{XTAL} \times R$. The frequency resolution used by the FSM during autocalibration is dependent on the value of n and the PD frequency. Higher values of n result in reduced frequency error (higher frequency resolution) during autocalibration. The highest value is currently recommended.

The VCO autocalibration counter, on average, expects to register N counts, rounded down (floor) to the nearest integer, for every PD cycle.

N is the ratio of the target VCO frequency (f_{VCO}) to the frequency of the PD (f_{PD}) where N can be any rational number supported by the N divider.

N is set by the integer register and fractional register contents using Equation 2.

$$N = N_{INT} + N_{FRAC}/2^{24} \quad (2)$$

where:
N_{INT} is the integer set in Register 0x03.
N_{FRAC} is the fractional part set in Register 0x04.

The autocalibration FSM and the data transfers to the internal VCO VSPI run at the rate of the FSM clock (t_{FSM}) where the FSM clock frequency must not be greater than 50 MHz.

$$t_{FSM} = t_{XTAL} \times 2^m \quad (3)$$

where m is 0, 2, 4, or 5 as determined by Register 0x0A, Bits[14:13]. The VSPI and FSM clock rate are determined by the value of m. It is recommended to set Register 0x0A, Bits[14:13] = 2.

The expected number of VCO counts is given by

$$VCO\ Counts = \text{floor}(N \times 2^n) \quad (4)$$

The nominal VCO frequency measured (f_{VCOM}) is given by

$$f_{VCOM} = VCO\ Counts \times f_{XTAL}/(2^n \times R) \quad (5)$$

where the worst case measurement error (f_{ERR}) is

$$f_{ERR} \approx \pm f_{PD}/2^{n+1} \quad (6)$$

For example, the autocalibration time (t_{CAL}) for an 8-bit step tuned VCO (where the total number of bits includes those needed to switch VCO cores) is as follows. First, a 20 × (k + 1) bit wait state occurs. Register 0x0A, Bits[9:3] set the value of the wait state (k) for wideband devices to k = 1. Wideband VCOs like the ADF5610 require additional wait time or one additional PD cycle (k = 1), whereas narrowband VCOs operate with no additional wait time (k = 0). The wait period is followed by the t_{MMT} for calibration, then the VSPI data transfers of 20 clock cycles each. This process repeats eight times because there is one bit to select the VCO core and seven bits to select the VCO band for a total of eight bits. Total calibration time, worst case, is given by the following equation:

$$t_{CAL} = t_{XTAL}\ (8R \times 2^n + (160 + (128 \times (k + 1)) \times 2^m)) \quad (8)$$

For guaranteed lock retention across temperature extremes using a single subband (lock and leave), the frequency error must be less than 1/8 of the frequency step required to induce a VCO subband change.

VCO Autocalibration Example

The VCO subsystem must satisfy the maximum f_{PD} limited by the two following conditions:

$$N \geq 16\ (f_{INT}),\ N \geq 20.0\ (f_{FRAC})$$

where:
$N = f_{VCO}/f_{PD}$. $f_{PD} \leq 100$ MHz.
f_{INT} is integer mode.
f_{FRAC} is fractional-N mode. The minimum N values change depending on the operating mode.

For example, if the VCO subsystem output frequency is to operate at 7.01 GHz and the crystal frequency is f_{XTAL} = 50 MHz, R = 1, and m = 2 (see Figure 22), then t_{FSM} = 80 ns (12.5 MHz).

When using autocalibration, do not allow the autocalibration FSM clock to exceed 50 MHz (see Register 0x0A, Bits[14:13]). The FSM clock does not affect the accuracy of the measurement.

The FSM clock only affects the time to produce the result. This same time standard clocks the 16-bit VSPI.

If the time to change frequencies is not a concern, use the longest calibration time, because this provides the minimum frequency error during band selection. The longest calibration time results in the selection of bands where the desired frequency is as close as possible to the recommended tuning voltage value as determined by the temperature compensation circuit.

Using an input crystal of 50 MHz (R = 1 and f_{PD} = 50 MHz), the times and accuracies for calibration using Equation 6 and Equation 8 are listed in Table 9, where minimal tuning time is 1/8 of the VCO band spacing.

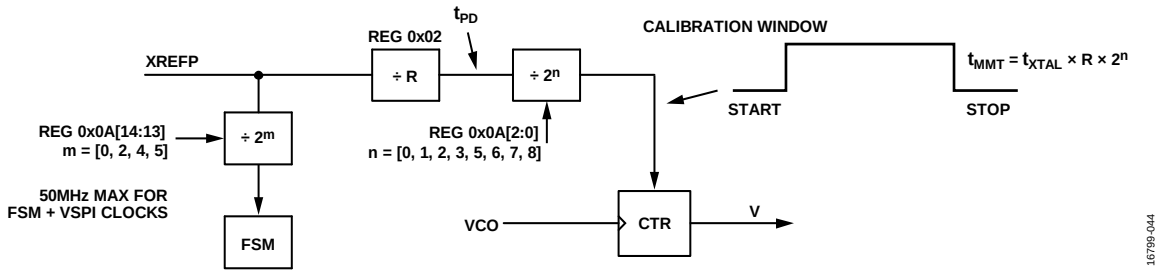


Figure 22. VCO Calibration

Table 9. Autocalibration Example with f_{XTAL} = 50 MHz, R = 1, m = 2

VCO Autocalibration Configuration Register 0x0A, Bits[2:0]	n	2^n	t_{MMT} (µs)	t_{CAL} (µs)	f_{ERR} Maximum
0	0	1	0.02	33.44	±25 MHz
1	1	2	0.04	33.60	±12.5 MHz
2	2	4	0.08	33.92	±6.25 MHz
3	3	8	0.16	34.56	±3.125 MHz
4	5	32	0.64	38.40	±781 kHz
5	6	64	1.28	43.52	±390 kHz
6	7	128	2.56	53.76	±95 kHz
7	8	256	5.12	74.24	±98 kHz

For example, it is determined that across all VCO subbands, a measurement resolution of at least 800 kHz results in the selection of the correct frequency band. Setting m = 2 and n = 5 provides 781 kHz of resolution and adds 38.4 µs of autocalibration time to a normal frequency hop. After autocalibration selects the band (38.4 µs after the frequency change command in the preceding example), the fractional register is loaded, and the loop locks with the normal transient predicted by the loop dynamics. This means that, as shown in this example, autocalibration adds 38.4 µs to the normal time to achieve frequency lock. Autocalibration is recommended for all but the most extreme frequency hopping requirements.

Manual VCO Calibration for Fast Frequency Hopping

When switching frequencies quickly is needed, it is possible to eliminate the autocalibration time by calibrating the VCO in advance and storing the step number vs. frequency information in the host, which is accomplished by initially locking the ADF5610 on each desired frequency using autocalibration, then reading and storing the selected VCO band settings. The VCO band settings are available in Register 0x10, Bits[7:0] after every autocalibration operation. The host must then program the VCO band settings directly when changing frequencies.

Manual writes to the VCO bands are executed immediately as are writes to the integer and fractional registers when autocalibration is disabled. Therefore, frequency changes with manual control and autocalibration disabled requires a minimum of two serial port transfers to the PLL, once to select the VCO band and once to set the PLL frequency.

When autocalibration is disabled (Register 0x0A, Bit 11 = 1), the VCO updates its registers immediately with the value written via Register 0x05. The VCO internal transfer requires 16 VCO SPI clock (VSCK) cycles after the completion of a write to Register 0x05. VSCK and the autocalibration controller clock are equal to the input reference divided by 0, 4, 16, or 32, as controlled by Register 0x0A, Bits[14:13].

For settling time requirements faster than 50 µs, contact Analog Devices, Inc., applications support. Settling times under 50 µs are possible, but certain limitations on performance may exist.

Registers Required for Frequency Changes in Fractional Mode

In fractional mode (Register 0x06, Bit 11 = 1), a large change of frequency may require main serial port writes to one of the three following registers:

- The integer register, Register 0x03. This write is required only if the integer part changes. For integer frequencies, write this register last because it triggers the frequency change.
- The fractional register, Register 0x04. The fractional register write triggers autocalibration when Register 0x0A, Bit 11 = 0, and the fractional frequency change is loaded into the modulator automatically after the autocalibration runs. If autocalibration is disabled (Register 0x0A, Bit 11 = 1), the fractional frequency change is loaded immediately into the modulator when the register is written with no adjustment to the VCO. Write this register last for fractional frequencies because it triggers the frequency change.
- The VCO SPI register, Register 0x05. This write is required only for manual control of VCO if Register 0x0A, Bit 11 = 1, autocalibration is disabled, or to enable or change the VCO output divider value, VCO bias, or the divider power level or RFOUT power level. See Figure 19 for more information.

Small steps in frequency in fractional mode, with autocalibration enabled (Register 0x0A, Bit 11 = 0), usually require only a single write to the fractional register. In a worst case scenario, three main serial port transfers to the ADF5610 may be required to change frequencies in fractional mode. If the frequency step is small such that the integer part of the frequency does not change, the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register, Register 0x04, for frequency changes.

Registers Required for Frequency Changes in Integer Mode

In integer mode (Register 0x06, Bit 11 = 0), a change of frequency requires main serial port writes to the following registers:

- VCO SPI register, Register 0x05. This write is required only for manual control of the VCO when Register 0x0A, Bit 11 = 1 (autocalibration disabled) or when the VCO configuration or the output frequency divider value must change (VCO Register 0x02).
- Integer register, Register 0x03. In integer mode, an integer register write triggers autocalibration when Register 0x0A, Bit 11 = 0 and the integer frequency change is loaded into the prescaler automatically after autocalibration runs. If autocalibration is disabled (Register 0x0A, Bit 11 = 1), the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally, changes to the integer register cause large steps in the VCO frequency. Therefore, the VCO band settings must be adjusted. Autocalibration enabled is the recommended method for integer mode frequency changes. If autocalibration is disabled (Register 0x0A, Bit 11 = 1), a prior knowledge of the correct VCO band setting and the corresponding adjustment to the VCO is required before executing the integer frequency change. Failure to select the proper band may result in loss of lock at temperature extremes or degraded phase noise performance.

VCO Built In Self Test (BIST) with Autocalibration

The frequency limits of the VCO can be measured using the BIST features of the autocalibration FSM by setting Register 0x0A, Bit 10 = 1, which freezes the VCO bands in one position. VCO bands can then be written manually with the varactor biased at the nominal midrail voltage used for autocalibration. For example, to measure the VCO maximum frequency, use Subband 0 (see

Table 35), written to the VCO subsystem via Register 0x05 = 000000001 0000 VCO_ID, where VCO_ID = 000b.

When autocalibration is enabled (Register 0x0A, Bit 11 = 0), and a new frequency is written, autocalibration runs. The VCO frequency error relative to the command frequency is measured and the results are written to Register 0x11, Bits[19:0], where Register 0x11, Bit 19 is the sign bit. The result is written in terms of VCO count error (see Equation 4 through Equation 6).

Using generic values as an example, if the expected frequency at the RFOUT pin is 7.0 GHz, the PFD frequency is 50 MHz, and Register 0x0A, Bits[2:0] = 8 (n = 8), expect to measure 3500/(50/28) = 17,920 counts. Frequencies less than 8.0 GHz route the fundamental frequency directly to the N counter. Therefore, in this case, 3500 MHz is routed to the N counter. For RFOUT frequencies greater than or equal to 8.0 GHz, the internal prescaler of the PLL (Register 0x08, Bit 19) must be enabled. If a difference of −5 counts is measured in Register 0x11, that means 17,915 counts were actually measured. With a 7 GHz VCO, 50 MHz reference, and n = 8, one count is 195.3125 kHz. Therefore, the actual frequency of the VCO is low in frequency by 5 × 195.3 kHz for a fundamental frequency of 3499.0234375 MHz or a push/push frequency of 6998.04687 MHz at RFOUT.

PLL SUBSYSTEM

Charge Pump (CP) and Phase Detector (PD)

The PD has two inputs, one from the reference path divider and one from the RF path divider. When in lock, these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. The frequency of operation of the phase detector is f_{PD}. Most formulas related to step size, Δ-Σ modulation, and timers, are functions of the operating frequency of the phase detector (f_{PD}). The f_{PD} is also referred to as the comparison frequency of the phase detector.

The phase detector compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

Charge Pump

A simplified diagram of the charge pump is shown in Figure 24. The charge pump consists of four programmable current sources. There are two sources controlling the charge pump gain (up gain, Register 0x09, Bits[13:7], and down gain, Register 0x09, Bits[6:0]) and two sources controlling the charge pump offset, where the magnitude of the offset is set by Register 0x09, Bits[20:14] and the direction is selected by Register 0x09, Bit 21 = 1 for up offset and Register 0x09, Bit 22 = 1 for down offset.

Charge pump gain is used at all times, whereas charge pump offset is recommended for fractional mode only. Typically, the charge pump up and charge pump down gain settings are set to the same value (Register 0x09, Bits[13:7] = Register 0x09, Bits[6:0]) to minimize spurs.

Charge Pump Gain

Charge pump up and charge pump down gains are set by Register 0x09, Bits[13:7] and Register 0x09, Bits[6:0], respectively. The current gain of the pump in amps per radian is equal to the gain setting of this register (Register 0x09) divided by 2π.

The typical CP gain setting is set from 2 mA to 2.5 mA. However, lower values can also be used. Note that values less than 1 mA may result in degraded phase noise performance.

For example, if both Register 0x09, Bits[13:7] and Register 0x09, Bits[6:0] are set to 50 decimal, the output current of each pump is 1 mA, and the phase frequency detector gain is k_P = 1 mA/2π radians, or 159 µA/rad. See the Charge Pump (CP) and Phase Detector (PD) section for more information. Setting both the charge pump up (Register 0x09, Bits[13:7] = 0) and charge pump down (Register 0x09, Bits[6:0] = 0) tristates the charge pump.

Tristating can also be achieved using Register 0x0B. Refer to the Phase Detector Functions section for more information.

Charge Pump Phase Offset

In integer mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. Integer mode does not require any CP offset current. When operating in integer mode, disable the CP offset in both directions (up and down) by writing Register 0x09, Bits[22:21] = 00b, and set the CP offset magnitude to zero by writing Register 0x09, Bits[20:14] = 0 decimal.

In fractional mode, CP linearity is of paramount importance. Any nonlinearity degrades phase noise and spurious performance. These nonlinearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always leads or arrives at the PD).

A programmable CP offset current source adds dc current to the loop filter and creates the desired phase offset. Positive current causes the VCO to lead, whereas negative current causes the reference to lead. Applications requiring an active loop filter use the up offset, or positive offset. The ADF5610 uses a passive loop filter. Therefore, a down offset, or negative offset, is recommended. Note that there can be conditions where the offset that is not typically recommended may provide improved spurious suppression, but these are often over very narrow bandwidths.

The CP offset is controlled via Register 0x09. Increasing the offset current causes the phase offset to scale from 0° to 360°.

The specific level of the charge pump offset current (Register 0x09, Bits[20:14]) is calculated using Equation 9 and shown in Figure 23.

$$\textit{Required CP Offset} = \min\left((4.3 \times 10^{-9} \times f_{PD} \times I_{CP}), 0.25 \times I_{CP}\right) \quad (9)$$

where:
f_{PD} is the comparison frequency of the phase detector (Hz).
I_{CP} is the full-scale current setting (A) of the switching charge pump (set in Register 0x09, Bits[6:0] and Register 0x09, Bits[13:7]).

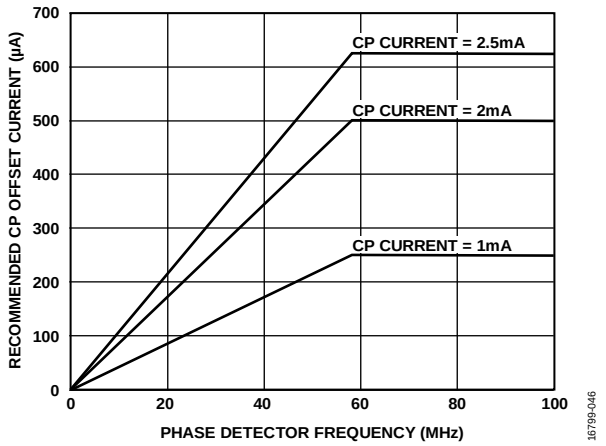


Figure 23. Recommended CP Offset Current vs. Phase Detector Frequency for Typical CP Gain Currents, Calculated Using Equation 9

Do not allow the required CP offset current to exceed 25% of the programmed CP current. It is recommended to enable the up offset and disable the down offset by writing Register 0x09, Bits[22:21] = 01b.

Operation with CP offset influences the required configuration of the lock detect function. See the description of the lock detect function in the Lock Detect section.

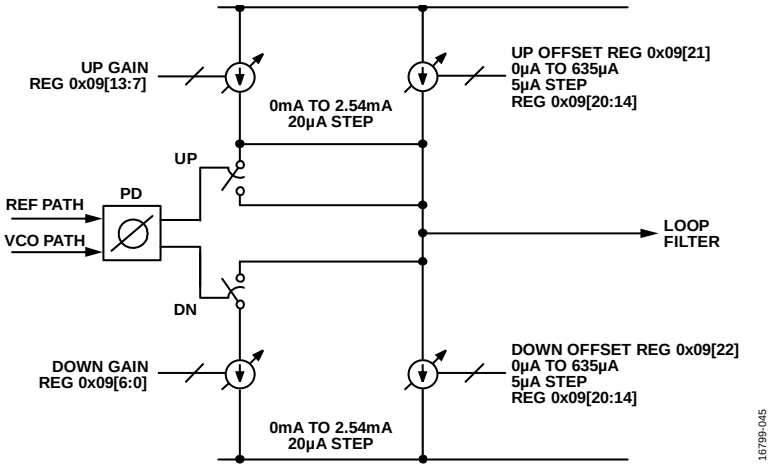


Figure 24. Charge Pump Gain and Offset Control

Phase Detector Functions

Register 0x0B, the phase detector register, provides access to special phase detector features.

Setting Register 0x0B, Bit 5 = 0 masks the PD up output, which prevents the charge pump from pumping up.

Setting Register 0x0B, Bit 6 = 0 masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Register 0x0B, Bit 5 and Register 0x0B, Bit 6 tristates the charge pump while leaving all other functions operating internally.

The CP_FORCE_UP (Register 0x0B, Bit 9 = 1) and CP_FORCE_DOWN (Register 0x0B, Bit 10 = 1) bits allow the charge pump to be forced up or down, respectively. These bits force the VCO to the ends of the tuning range, which is useful in testing the VCO or the continuity of the loop filter path.

Reference Input Stage

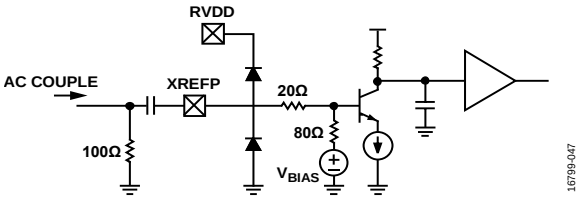


Figure 25. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider and eventually to the phase detector. The buffer has two modes of operation controlled by Register 0x08, Bit 21. High gain (Register 0x08, Bit 21 = 0) is recommended below 200 MHz, and high frequency (Register 0x08, Bit 21 = 1) for 200 MHz to 350 MHz operation. The buffer is internally dc biased with 100 Ω internal termination. For a 50 Ω match, add an external 100 Ω resistor to ground, followed by an ac coupling capacitor (impedance less than 1 Ω).

At low frequencies, a relatively square reference is recommended to maintain a high input slew rate. At higher frequencies, use a square or sinusoid. Table 10 shows the recommended operating regions for different reference frequencies. If operating outside these regions, the device usually still operates, but with degraded reference path phase noise performance.

When operating at 50 MHz, the input referred phase noise of the PLL is between −148 dBc/Hz and −150 dBc/Hz at a 10 kHz offset, depending on the mode of operation. To avoid degradation of the PLL noise contribution, the input reference signal must be 10 dB lower (−158 dBc/Hz to −160 dBc/Hz), or lower at a 10 kHz offset, than this floor. Such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

Reference Path R Divider

The reference path R divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled via Register 0x02.

RF Path, N Divider

The main RF path divider is capable of average divide ratios between $2^{19} - 5$ (524,283) and 20 in fractional mode, and between $2^{19} - 1$ (524,287) and 16 in integer mode. Normally, the VCO frequency range divided by the minimum N divider value can result in practical restrictions on the maximum usable PD frequency. For example, a VCO operating at 1.5 GHz in fractional mode with a minimum N divider value of 20 has a maximum PD frequency of 75 MHz, which is not the case with the ADF5610. Regardless of the mode of operation or the PD frequency, the minimum N value never occurs as long as the specified maximum phase detector frequency is respected. For RFOUT frequencies less than 8 GHz, the minimum frequency at the input to the PLL is 3650 MHz. Therefore, N is always greater than the minimum regardless of the mode. When RFOUT is set to 8.0 GHz, the input to the PLL is 4.0 GHz, and the internal prescaler must be enabled (Register 0x08, Bit 19 = 1). Enabling the internal prescaler results in the 4.0 GHz fundamental frequency being divided down so that 2.0 GHz are supplied to the PD input. Operating in integer mode allows PD rates up to 100 MHz. This results in an N value of 20, which is not a problem. Operation in fractional mode limits the PD rate to 100 MHz, which results in the minimum value for N when RFOUT equals 8.0 GHz, but no less than this minimum value.

Table 10. Reference Sensitivity[1]

Reference Input Frequency (MHz)	Square Input, Slew > 0.5 V/ns			Sinusoidal Input		
		Recommended Swing (V p-p)			Recommended Power Range (dBm)	
	Recommended	Minimum	Maximum	Recommended	Minimum	Maximum
<10	Yes	0.6	2.5	No	No	No
10	Yes	0.6	2.5	No	No	No
25	Yes	0.6	2.5	Okay	8	15
50	Yes	0.6	2.5	Yes	6	15
100	Yes	0.6	2.5	Yes	5	15
150	Okay	0.9	2.5	Yes	4	12
200	Okay	1.2	2.5	Yes	3	8
200 to 350	No	No	No	Yes	5	10

[1] Okay means the setting works. For example, a 150 MHz input square wave is sufficient but 100 MHz may provide improved performance.

Lock Detect

The lock detect (LD) function verifies that the ADF5610 is generating the desired frequency. LD is enabled by writing Register 0x07, Bit 3 = 1. The ADF5610 provides an LD indicator in the following two ways:

- As an output available on the SDO pin of the ADF5610 (configuration is required to use the SDO pin for LD purposes). For more information, see the Configuring the SDO Pin for LD Output section.
- Reading from Register 0x12, Bit 1, where Bit 1 = 1 indicates a locked condition and Bit 1 = 0 indicates an unlocked condition.

The LD circuit expects the divided VCO edge and the divided reference edge to appear at the PD within a user specified time period (window), repeatedly. Either signal may arrive first. Only the difference in arrival times is significant. The arrival of the two edges within the designated window increments an internal counter. When the count reaches and exceeds a user specified value (Register 0x07, Bits[2:0]), the ADF5610 declares lock.

Failure in registering the two edges in any one window resets the counter and immediately declares an unlocked condition. Lock is deemed to be reestablished when the counter reaches the user specified value (Register 0x07, Bits[2:0]) again.

The ADF5610 supports the following two lock detect modes:

- Analog LD supports a fixed window size of 10 ns. Analog LD mode is selected by writing Register 0x07, Bit 6 = 0.
- Digital LD supports a user configurable window size, programmed in Register 0x07, Bits[11:7]. Digital LD is selected by writing Register 0x07, Bit 6 = 1.

Lock Detect Configuration

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration, described in detail in the Charge Pump (CP) and Phase Detector (PD) section.

The PD frequency and settings in the CP (Register 0x09) impact the required LD window size in fractional mode of operation. To function properly, the required lock detect window size is provided by Equation 10 in fractional mode and Equation 11 in integer mode.

$$LD\ Window(\text{sec}) = \frac{\left(\frac{I_{CP_OFFSET}(\text{A})}{f_{PD}(\text{Hz}) \times I_{CP}\ (\text{A})} + 2.66 \times 10^{-9}(\text{sec}) + \frac{1}{f_{PD}(\text{Hz})}\right)}{2} \quad (10)$$

$$LD\ Window\ (\text{sec}) = \frac{1}{2 \times f_{PD}} \quad (11)$$

where:

f_{PD} is the comparison frequency of the phase detector.

I_{CP_OFFSET} is the charge pump offset current (Register 0x09, Bits[20:14]).

I_{CP} is the full-scale current setting of the switching charge pump (Register 0x09, Bits[6:0] or Register 0x09, Bits[13:7]).

If the result provided by Equation 10 is equal to 10 ns, analog LD can be used (Register 0x07, Bit 6 = 0). Otherwise, digital LD is necessary (Register 0x07, Bit 6 = 1). Table 11 lists the required Register 0x07 settings to appropriately program the digital LD window size. From Table 11, select the closest value in the digital LD window size columns to the ones calculated in Equation 10 and Equation 11, and program Register 0x07, Bits[11:10] and Register 0x07, Bits[9:7] accordingly.

Digital Window Configuration Example

For this example, assume the device is in fractional mode, with a 50 MHz PD and the following conditions:

- Charge pump gain of 2 mA (Register 0x09, Bits[13:7] = 0x64, Register 0x09, Bits[6:0] = 0x64)
- Up offset (Register 0x09, Bits[22:21] = 01b)
- Offset current magnitude of 400 µA (Register 0x09, Bits[20:14] = 0x50)

Apply Equation 10 to calculate the required LD window size.

$$LD\ Window\ (\text{sec}) = \frac{\left(\frac{0.4 \times 10^{-3}(\text{A})}{50 \times 10^{6}(\text{Hz}) \times 2 \times 10^{-3}(\text{A})} + 2.66 \times 10^{-9}(\text{sec}) + \frac{1}{50 \times 10^{6}(\text{Hz})}\right)}{2}$$

$$= 13.33\ \text{ns}$$

Locate the Table 11 value that is closest to this result, which is, in this case, 13.3 ≈ 13.33. To set the digital LD window size, program Register 0x07, Bits[11:10] = 10b and Register 0x07, Bits[9:7] = 010b, according to Table 11. For a given operating point, there is typically a correct solution for the lock detect window. However, one solution does not fit all operating points. As observed from Equation 10 and Equation 11, if the charge pump offset or PD frequency is changed significantly, the lock detect window may need to be adjusted.

Table 11. Typical Digital Lock Detect Window for Various LD Timer Divide Settings, Register 0x07, Bits[9:7]

	Digital Lock Detect Window Size Nominal Value (ns)							
LD Timer Speed, Register 0x07, Bits[11:10]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
00 (Fastest)	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
11 (Slowest)	7.6	10.2	15.4	26	47	88	172	338

Configuring the SDO Pin for LD Output

Setting Register 0x0F, Bit 7 = 1 and Register 0x0F, Bits[4:0] = 1 displays the lock detect flag on the SDO pin of the ADF5610. When locked, SDO is high. As the name suggests, the SDO pin is multiplexed between the LD and the serial data output (SDO) signals. Therefore, LD is available on the SDO pin at all times except when a serial port read is requested, in which case the pin reverts temporarily to the serial data output pin and returns to the lock detect flag after the read is completed.

LD can be made available on the SDO pin at all times by writing Register 0x0F, Bit 6 = 1. In that case, the ADF5610 does not provide any readback functionality because the SDO signal is not available.

Cycle Slip Prevention (CSP)

When changing the VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Because the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD cycles from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump cycles from maximum to minimum, even though the VCO has not yet reached its final frequency.

The charge on the loop filter small capacitor may actually discharge slightly during the low gain portion of the cycle. This discharge can make the VCO frequency reverse temporarily during locking. This phenomenon is known as cycle slipping. Cycle slipping causes the pull in rate during the locking phase to vary cyclically. Cycle slipping increases the time to lock to a value greater than predicted by normal small signal Laplace transform analysis.

The ADF5610 PD features an ability to reduce cycle slipping during acquisition. The CSP feature increases the PD gain during large phase errors. The specific phase error that triggers the momentary increase in PD gain is set via Register 0x0B, Bits[8:7].

Frequency Tuning

The ADF5610 VCO subsystem always operates in the doubled frequency range of operation (7300 MHz to 14600 MHz), which is always available at the RFOUT port or at the differential divider ports, PDIV_OUT and NDIV_OUT, when the divider is set to divide by 1 in VCO Register 0x02, Bits[2:0].

Frequencies at or below the VCO fundamental frequency of operation (57 MHz to 7300 MHz) are realized by tuning to the appropriate doubled frequency and selecting the appropriate output divider setting (divide by 2 to 128) in VCO Register 0x02, Bits[2:0].

The fundamental band of operation (3650 MHz to 7300 MHz) is input to the internal PLL and is not directly available to the user. For more information, see the VCO Autocalibration section.

Integer Mode

The ADF5610 is capable of operating in integer mode. For integer mode, set the following registers:

- Disable the fractional modulator, Register 0x06, Bit 11 = 0
- Bypass the modulator circuit, Register 0x06, Bit 7 = 1

In integer mode, the VCO step size is fixed to that of the PD frequency. Integer mode typically has a 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used. Therefore, lower phase noise can often be realized in fractional mode. Disable the charge pump offset when in integer mode.

Integer Frequency Tuning

In integer mode, the digital Σ-Δ modulator is shut off and the N divider (Register 0x03) can be programmed to any integer value in the range of 16 to 219 − 1. To run in integer mode, configure Register 0x06 (as described in the Configuring the SDO Pin for LD Output section), then program the integer portion of the frequency as explained by Equation 12, ignoring the fractional part.

The following sequence illustrates how to reconfigure the PLL registers to switch from fractional mode to integer mode and enable the output divider at the PDIV_OUT and NDIV_OUT pins.

1. Disable the fractional modulator, Register 0x06, Bit 11 = 0.
2. Bypass the Δ-Σ modulator, Register 0x06, Bit 7 = 1.
3. Because the fundamental frequency (3650 MHz to 7300 MHz) range is supplied to the PLL, the fundamental frequency is the basis for all programming. Determine the fundamental frequency being used during operation.
4. If the fundamental frequency is <4000 MHz (RFOUT < 8000 MHz), set the internal prescaler to divide by 1 (Register 0x08, Bit 19 = 0). Otherwise, set the internal prescaler to 1.
5. To tune to frequencies (<7300 MHz), select the appropriate output divider value (VCO Register 0x02, Bits[2:0]), then enable the differential output divider (VCO Register 0x01, Bit 8 = 1).

Writing to the VCO subsystem registers (VCO Register 0x02, Bits[2:0] and VCO Register 0x01, Bit 8 in this case) is accomplished indirectly through PLL Register 0x05. For more information on communicating with the VCO subsystem through PLL Register 0x05, see the VCO Serial Port Interface (VSPI) section.

Fractional Mode

Set the following registers to place the ADF5610 in fractional mode:

- Enable the fractional modulator, Register 0x06, Bit 11 = 1.
- Connect the Δ-Σ modulator in circuit, Register 0x06, Bit 7 = 0.

Fractional Frequency Tuning

This sections provides a generic example with the goal of explaining how to program the output frequency. Actual variables are dependent on the reference in use.

The ADF5610 in fractional mode achieves frequencies at fractional multiples of the reference. The frequency of the ADF5610 is given by the following equation:

$$f_{RF} = 2 \times f_{VCO}$$

where:

$$f_{VCO} = \frac{f_{XTAL}}{R}(N_{INT} + N_{FRAC}) = f_{INT} + f_{FRAC} \quad (12)$$

and

$$f_{DIV} = f_{RF}/k \quad (13)$$

where:
f_{RF} is the doubled frequency (RFOUT).
f_{VCO} is the fundamental frequency (input to PLL) after any necessary correction. The f_{VCO} value must always be less than or equal to 4000 MHz. When f_{VCO} is greater than or equal to 4000 MHz, the internal divide by 2 prescaler (Register 0x08, Bit 19) must be enabled.
f_{XTAL} is the frequency at the reference oscillator input.
R is the reference path division ratio (set in Register 0x02).
N_{INT} is the integer division ratio (set in Register 0x03), an integer number between 20 and 524,284.
N_{FRAC} is the fractional part, from 0.0 to 0.99999…, N_{FRAC} = Register 0x04/2^{24}.
f_{DIV} is the output frequency after any potential dividers.
k is 1 for fundamental, or k = 2 to 128 depending on the selected output divider value (Register 0x05, Bits[9:7] indirectly address VCO Register 0x02, Bits[2:0]).

For example, f_{DIV} = 1752.5 MHz, k = 4, f_{VCO} = 3505 MHz, f_{RF} = 7010 MHz, f_{XTAL} = 50 MHz, R = 1, f_{PD} = 50 MHz, N_{INT} = 70, and N_{FRAC} = 0.1. The f_{PD} value is the PD operating frequency, f_{XTAL}/R.

Register 0x04 = round(0.1 × 2^{24}) = round(1,677,721.6) = 1,677,722.

If $f_{VCO} \leq$ 4000 MHz, then Register 0x08, Bit 19 = 0 (divide by 1).

If f_{VCO} > 4000 MHz, then Register 0x08, Bit 19 = 1.

f_{VCO} (50 × 10^6/1) (70 + 1677722/2^{24}) = 3505 MHz + 1.192 Hz error (14)

$f_{RF} = 2 \times f_{VCO}$ = 7010 MHz + 2.384 Hz error (15)

$f_{DIV} = f_{RF}/k$ = (7010 MHz + 2.384 Hz error)/4 = 1752.5 MHz + 0.596 Hz error (16)

In this example, the differential divider output frequency of 1752.5 MHz is achieved by programming the 19-bit binary value of 70 decimal = 0x46 into the INTG_REG bit in Register 0x03, and the 24-bit binary value of 1677722 decimal = 0x19999A into the FRAC bit in Register 0x04. Eliminate the 0.596 Hz quantization error using the exact frequency mode, if required. In this example, the RFOUT value is divided by 4. Specific control of the output divider is required. See the VCO Subsystem Register Map section for details.

Exact Frequency Tuning

Due to quantization effects, the absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example, the frequency resolution of a 24-bit fractional modulator is set by the PD comparison rate divided by 2^{24}. The 2^{24} value in the denominator is sometimes referred to as the modulus. Analog Devices PLLs use a fixed modulus, which is a binary number. In some types of fractional PLLs, the modulus is variable, allowing exact frequency steps to be achieved with decimal step sizes. Unfortunately, small steps using small modulus values result in large spurious outputs at multiples of the modulus period (channel step size). For this reason, Analog Devices PLLs use a large fixed modulus. Normally, the step size is set by the size of the fixed modulus. In the case of a 50 MHz PD rate, a modulus of 2^{24} results in a 2.98 Hz step resolution, or 0.0596 ppm. In some applications, it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (for example, N = 50.0, 50.5, 50.25, 50.75). Some common frequencies cannot be exactly represented. For example, N_{FRAC} = 0.1 = 1/10 must be approximated as round((0.1 × 2^{24})/2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz, the N_{FRAC} value translates to a 1.2 Hz error. The exact frequency mode of the ADF5610 addresses this issue and can eliminate quantization error by programming the channel step size to f_{PD}/10 in Register 0x0C to 10 (in this example). More generally, this feature can be used whenever the desired frequency (f_{VCO}) can be exactly represented on a step plan where there is an integer number of steps (<2^{14}) across Integer N boundaries. Mathematically, this situation is satisfied if

$$f_{VCOk} \bmod (f_{GCD}) = 0 \quad (17)$$

where:
f_{VCOk} is the channel step frequency, $0 < k < 2^{24} - 1$, as shown in Figure 26.
GCD is the greatest common divisor.

$$f_{GCD} = GCD(f_{VCO1}, f_{PD}) \text{ and } f_{GCD} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

where f_{PD} is the frequency of the phase detector.

Some fractional PLLs are able to achieve these exact frequencies by shortening the length of the phase accumulator (the denominator or the modulus of the Δ-Σ modulator) so that the Δ-Σ modulator phase accumulator repeats at an exact period

related to the interval frequency ($f_{VCOk} - f_{VCO(k-1)}$) in Figure 26. Consequently, the shortened accumulator results in more frequent repeating patterns and, as a result, often leads to spurious emissions at multiples of the repeating pattern period, or at harmonic frequencies of $f_{VCOk} - f_{VCO(k-1)}$. For example, in some applications, these intervals may represent the spacing between radio channels, with the spurious occurring at multiples of the channel spacing.

In comparison, the Analog Devices method is able to generate exact frequencies between adjacent Integer N boundaries while still using the full 24-bit phase accumulator modulus. This method achieves exact frequency steps with a high phase detector comparison rate, which allows Analog Devices PLLs to maintain excellent phase noise and spurious performance in the exact frequency mode.

Using Exact Frequency Mode

If the constraint in Equation 17 is satisfied, the ADF5610 is able to generate signals with zero frequency error at the desired VCO frequency. Exact frequency mode can be reconfigured for each target frequency or be set up for a fixed f_{GCD} that applies to all channels.

Configuring Exact Frequency Mode for a Particular Frequency

The following sequence shows how to properly derive the various PLL register values for exact frequency mode operation. An example is provided as well.

1. Calculate and program the integer register setting.

   $$Register\ 0x03 = N_{INT} = \text{floor}(f_{VCO}/f_{PD})$$

   where the *floor* function is the rounding down to the nearest integer.
2. Then calculate the low side integer boundary frequency.

   $$f_N = N_{INT} \times f_{PD}$$

3. Calculate and program the exact frequency register value.

   $$Register\ 0x0C = f_{PD}/f_{GCD}$$

   where $f_{GCD} = GCD(f_{VCO}, f_{PD})$.
4. Calculate and program the fractional register setting.

   $$Register\ 0x04 = \text{ceil}\left(\frac{2^{24}(f_{VCOk} - f_N)}{f_{PD}}\right)$$

   where ceil is the ceiling function, meaning round up to the nearest integer.

For example, to configure the ADF5610 for exact frequency mode at f_{VCO} = 2800.2 MHz, where the PD rate (f_{PD}) = 61.44 MHz, proceed by checking Equation 17 to confirm that the exact frequency mode for this f_{VCO} is possible.

$$f_{GCD} = GCD(f_{VCO}, f_{PD}) \text{ and } f_{GCD} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

$$f_{GCD} = GCD(2800.2 \times 10^6, 61.44 \times 10^6) =$$

$$120 \times 10^3 > \frac{61.44 \times 10^6}{2^{14}} = 3750$$

Because Equation 17 is satisfied, the ADF5610 can be configured for exact frequency mode at f_{VCO} = 2800.2 MHz by continuing with the following steps:

1. Calculate N_{INT}.

   $$N_{INT} = Register\ 0x03 =$$

   $$\text{floor}\left(\frac{f_{VCO1}}{f_{PD}}\right) = \text{floor}\left(\frac{2800.2 \times 10^6}{61.44 \times 10^6}\right) =$$

   $$45\ decimal = 0x2D$$

2. Calculate the value for Register 0x0C.

   $$Register\ 0x0C =$$

   $$\frac{f_{PD}}{GCD((f_{VCOk+1} - f_{VCOk}), f_{PD})} =$$

   $$\frac{61.44 \times 10^6}{GCD(100 \times 10^3, 61.44 \times 10^6)} =$$

   $$\frac{61.44 \times 10^6}{20000} = 3072\ decimal = 0xC00$$

3. To program Register 0x04, the closest integer N boundary frequency (f_N) that is less than the desired VCO frequency (f_{VCO}) must be calculated by $f_N = f_{PD} \times N_{INT}$. Using the current example,

   $$f_N = f_{PD} \times N_{INT} = 45 \times 61.44 \times 10^6 = 2764.8 \text{ MHz}$$

   then,

   $$Register\ 0x04 =$$

   $$\text{ceil}\left(\frac{2^{24}(f_{VCO} - f_N)}{f_{PD}}\right) =$$

   $$\text{ceil}\left(\frac{2^{24}(2800.2 \times 10^6 - 2764.8 \times 10^6)}{61.44 \times 10^6}\right) =$$

   $$9666560\ decimal = 0x938000$$

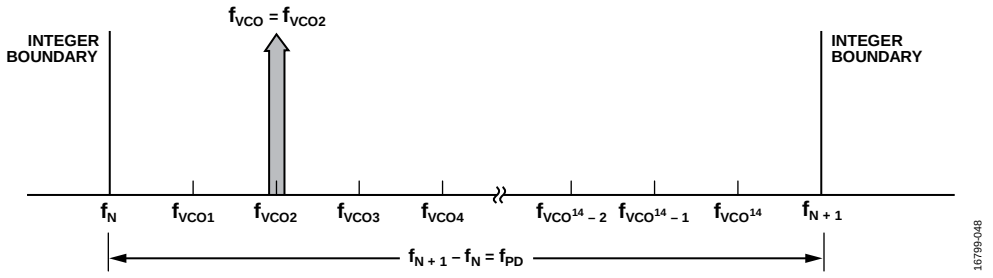


Figure 26. Exact Frequency Tuning

Exact Frequency Channel Mode

When multiple, equally spaced, exact frequency channels are needed that fall within the same interval (that is, $f_N \le f_{VCOk} < f_{N+1}$) where f_{VCOk} is shown in Figure 26 and $1 \le k \le 2^{14}$, it is possible to maintain the same Integer N register (Register 0x03) and exact frequency register (Register 0x0C) settings and only update the fractional register (Register 0x04) setting. The exact frequency channel mode is possible when Equation 17 is satisfied for at least two equally spaced adjacent frequency channels, that is, the channel step size.

To configure the ADF5610 for exact frequency channel mode, initially and only at the beginning, the Integer N register (Register 0x03) and exact frequency register (Register 0x0C) must be programmed for the smallest f_{VCO} frequency (f_{VCO1} in Figure 26). Calculate and program the integer register setting by

$$Register\ 0x03 = N_{INT} = \text{floor}(f_{VCO1}/f_{PD})$$

where f_{VCO1} is shown in Figure 26 and corresponds to the minimum channel VCO frequency. Then, the lower integer boundary frequency is given by $f_N = N_{INT} \times f_{PD}$.

Calculate and program the exact frequency register value by $Register\ 0x0C = f_{PD}/f_{GCD}$, where $f_{GCD} = GCD((f_{VCOk+1} - f_{VCOk}), f_{PD})$, greatest common divisor of the desired equidistant channel spacing and the PD frequency ($(f_{VCOk+1} - f_{VCOk})$ and f_{PD}). To switch between various equally spaced intervals (channels) only, the fractional register (Register 0x04) must be programmed to the desired VCO channel frequency (f_{VCOk}) in the following manner:

$$Register\ 0x04 = N_{FRAC} = \text{ceil}\left(\frac{2^{24}(f_{VCOk} - f_N)}{f_{PD}}\right)$$

where:
$f_N = \text{floor}(f_{VCO1}/f_{PD})$.
f_{VCO1}, as shown in Figure 26, represents the smallest channel VCO frequency that is greater than f_N.

For example, to configure the ADF5610 for the exact frequency mode for equally spaced intervals of 100 kHz, where the first channel (Channel 1) = f_{VCO1} = 2800.200 MHz and the PD rate (f_{PD}) = 61.44 MHz, proceed as follows:

1. Check that the exact frequency mode for f_{VCO1} = 2800.2 MHz (Channel 1) and f_{VCO2} = 2800.2 MHz + 100 kHz = 2800.3 MHz (Channel 2) is possible.

$$f_{GCD1} = GCD(f_{VCO1}, f_{PD}) \text{ and}$$
$$f_{GCD1} \ge \left(\frac{f_{PD}}{2^{14}}\right) \text{and } f_{GCD2} = GCD(f_{VCO2}, f_{PD}) \quad (18)$$
$$\text{and}$$
$$f_{GCD2} \ge \left(\frac{f_{PD}}{2^{14}}\right)$$

$$f_{GCD1} = GCD(2800.2 \times 10^6, 61.44 \times 10^6) =$$
$$120 \times 10^3 > \frac{61.44 \times 10^6}{2^{14}} = 3750$$

$$f_{GCD2} = GCD(2800.3 \times 10^6, 61.44 \times 10^6) =$$
$$20 \times 10^3 > \frac{61.44 \times 10^6}{2^{14}} = 3750$$

2. If Equation 17 is satisfied for at least two of the equally spaced interval (channel) frequencies (f_{VCO1}, f_{VCO2}, f_{VCO3}, ... f_{VCON}) as it is in Equation 18, the ADF5610 exact frequency channel mode is possible for all desired channel frequencies, and can be configured as follows:

$$Register\ 0x03 =$$
$$\text{floor}\left(\frac{f_{VCO1}}{f_{PD}}\right) = \text{floor}\left(\frac{2800.2 \times 10^6}{61.44 \times 10^6}\right) = 45\ decimal$$
$$= 0x2D$$
$$Register\ 0x0C =$$
$$\frac{f_{PD}}{GCD((f_{VCOk+1} - f_{VCOk}), f_{PD})} =$$
$$\frac{61.44 \times 10^6}{GCD(100 \times 10^3, 61.44 \times 10^6)} = \frac{61.44 \times 10^6}{20000}$$
$$= 3072\ decimal = 0xC00$$

where (f_{VCOk}+1 − f_{VCOk}) is the desired channel spacing (100 kHz in this example).

3. To program Register 0x04, the closest Integer N boundary frequency (f_N) that is less than the smallest channel VCO frequency (f_{VCO1}) must be calculated ($f_N = \text{floor}(f_{VCO1}/f_{PD})$) using the following example:

$$f_N = f_{PD} \times \text{floor}\left(\frac{2800.2 \times 10^6}{61.44 \times 10^6}\right) =$$
$$45 \times 61.44 \times 10^6 = 2764.8\ \text{MHz}$$

Then, for Channel 1,

$$Register\ 0x04 = \text{ceil}\left(\frac{2^{24}(f_{VCO1} - f_N)}{f_{PD}}\right)$$

where f_{VCO1} = 2800.2 MHz.

The following equation provides the value for Register 0x04 for operating in Channel 1 (f_{VCO1} = 2800.2 MHz).

$$= \text{ceil}\left(\frac{2^{24}(2800.2\times10^6 - 2764.8\times10^6)}{61.44\times10^6}\right) = 9666560\ decimal$$

$$= 0x938000$$

4. To change from Channel 1 (f_{VCO1} = 2800.2 MHz) to Channel 2 (f_{VCO2} = 2800.3 MHz), only Register 0x04 must be programmed, as long as all of the desired exact frequencies (f_{VCOk}, see Figure 26) fall between the same Integer N boundaries ($f_N < f_{VCOk} < f_{N+1}$). In that case,

$$Register\ 0x04 = \text{ceil}\left(\frac{2^{24}(2800.3\times10^6 - 2764.8\times10^6)}{61.44\times10^6}\right) =$$

$$9693867\ decimal = 0x93EAAB$$

Seed Register

The start phase of the fractional modulator digital phase accumulator (DPA) can be set to one of four possible default values via the SEED_SELECT bits, Register 0x06, Bits[1:0]. The ADF5610 automatically reloads the start phase (seed value) into the DPA every time a new fractional frequency is selected. Certain zero seed values or binary seed values may cause spurious energy correlation at specific frequencies. For most cases, a random (not zero and not binary) start seed is recommended (Register 0x06, Bits[1:0] = 2).

SOFT RESET AND POWER-ON RESET

The ADF5610 features a hardware power-on reset (POR). All chip registers are reset to default states approximately 250 µs after power-up.

The PLL subsystem SPI registers can also be soft reset by an SPI write to Register 0x00. Note that the soft reset does not clear the SPI mode of operation referred to in the SPI Modes of Operation section. The VCO subsystem is not affected by the PLL soft reset. The VCO subsystem registers can only be reset by removing the power supply.

If external power supplies or regulators have rise times slower than 250 µs, write to the SPI RST_SWRST bit (Register 0x00, Bit 5 = 1) immediately after power-up, before any other SPI activity. This write procedure ensures starting from a known state.

POWER-DOWN MODE

The VCO subsystem is not affected by the CEN pin or PLL soft reset. Therefore, device power-down consists of the following two-step process:

1. Power down the VCO by writing 1 to VCO Register 0x02, Bit 3 via PLL Register 0x05.
2. Power down the PLL by pulling the CEN pin (Pin 44) low (assuming there are no SPI overrides (Register 0x01, Bit 0 = 1)). Pulling the CEN pin low disables all analog functions and internal clocks. Current consumption typically drops to 100 µA in the power-down state if the reference input is disconnected. The serial port still responds to normal communication in power-down mode.

It is possible to ignore the CEN pin by setting Register 0x01, Bit 0 = 0. Control of the power-down mode then comes from the serial port register, Register 0x01, Bit 1.

It is also possible to leave various blocks turned on when in power-down (see Register 0x01), as listed in Table 12.

Table 12. Bit and Block Assignments for Register 0x01

Bit Assignment	Block Assignment
Bit 2	Internal bias reference sources
Bit 3	PD block
Bit 4	CP block
Bit 5	Reference path buffer
Bit 6	VCO path buffer
Bit 7	Digital I/O test pads (GPO driver)

GENERAL-PURPOSE OUTPUT (GPO)

The PLL shares the SDO (lock detect/serial data output) pin to perform various functions. Although the pin is most commonly used to read back registers from the chip via the SPI, the pin is also capable of exporting a variety of signals and real-time test waveforms (including lock detect). The SDO pin is driven by a tristate CMOS driver with ~200 Ω R_{OUT}. The SDO pin has logic associated with it to dynamically select whether the driver is enabled, and to determine which data to export from the chip.

In the default configuration of the output driver, after POR, the output driver is disabled, and drives only during appropriately addressed SPI reads. This configuration allows the ADF5610 to share its output with other devices on the same bus.

The pin driver is enabled if the chip is addressed. That is, the last three bits of the SPI cycle = 000b before the rising edge of SEN. If SEN rises before SCK has clocked in an invalid (nonzero) chip address, the ADF5610 starts to drive the bus.

To monitor any of the GPO signals, including lock detect, set Register 0x0F, Bit 7 = 1 to keep the SDO driver always on. This setting stops the LDO driver from tristating and means that the SDO line cannot be shared with other devices.

The ADF5610 naturally switches from the GPO data and exports the SDO signal during an SPI read. To prevent this automatic data selection and to always select the GPO signal, set Register 0x0F, Bit 6 = 1 to prevent automuxing of the SDO pin. The phase noise performance at this output is poor and uncharacterized. Also, do not toggle the GPO during normal operation because toggling may degrade the spectral performance.

Additional controls are available that may be helpful when sharing the bus with other devices, and are as follows:

- To disable the driver completely, set Register 0x08, Bit 5 = 0 (this bit takes precedence over all other SDO driver bit settings).
- To disable either the pull-up or pull-down sections of the driver, set Register 0x0F, Bit 8 = 1 or Register 0x0F, Bit 9 = 1, respectively.

Example scenarios are listed in Table 13. The signals that are available on the GPO are selected by changing the GPO_SELECT bits (Register 0x0F, Bits[4:0]).

The ADF5610 SPI supports both 1.8 V and 3.3 V input voltage levels. Input pins including SDI, SCK, and SEN support both voltage levels without the need for any configuration.

The SPI output (SDO pin) only supports 3.3 V levels when driven and 1.8 V and 3.3 V in open-drain mode. The CMOS or open-drain configuration is register programmable via Register 0x0F, Bits[9:8]. Open-drain mode requires an external pull-up resistor. See Table 1 for more information.

Table 13. Driver Scenarios

Scenario	Action
Drive SDO During Reads, Tristate Otherwise (Allows Bus Sharing)	No action required.
Drive SDO During Reads, Lock Detect Otherwise	Set GPO select, Register 0x0F, Bits[4:0] = 00001b (default) Set Register 0x0F, Bit 6 = 0, enable automux of SDO Set Register 0x0F, Bit 7 = 1, prevent GPO driver disable
Always Drive Lock Detect, 3.3 V Output	Set Register 0x0F, Bit 6 = 1, prevent automux of SDO Set the GPO select, Register 0x0F, Bits[4:0] = 00001 (default) Set Register 0x0F, Bit 7 = 1, prevent GPO driver disable

CHIP IDENTIFICATION

Identifies the PLL subsystem version information by reading the content of Register 0x00. It is not possible to read the VCO subsystem version.

POWER SUPPLY

The ADF5610 is a high performance, low noise device. Phase noise and spurious performance may be degraded by noisy power supplies. To achieve maximum performance and ensure that power supply noise does not degrade the performance of the ADF5610, it is recommended to use Analog Devices low noise, high power supply rejection ratio (PSRR) regulators. Preferred regulators include the LT3042, LT3045, ADM7150, and the ADM7151. Optimal spectral performance and supply isolation is also achievable with the HMC1060LP3E quad low noise regulator, which conserves board space.

PROGRAMMABLE PERFORMANCE TECHNOLOGY

For low power applications that do not require maximum noise floor performance, the ADF5610 features the ability to reduce current consumption by 18 mA (power consumption by 90 mW)

High performance is enabled by writing VCO Register 0x01, Bits[4:2] = 7 decimal, and high performance is disabled (low current consumption mode enabled) by writing VCO Register 0x01, Bits[4:2] = 0 decimal. High performance mode improves phase noise and output power at the cost of increased current consumption.

LOOP FILTER AND FREQUENCY CHANGES

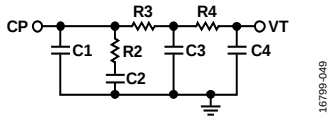


Figure 27. Loop Filter Design

All PLLs with integrated VCOs exhibit integer boundary spurs at harmonics of the reference frequency. Figure 15 shows the worst case spurious scenario where the harmonic of the reference frequency (50 MHz) is within the loop filter bandwidth of the fundamental frequency of the ADF5610.

A tunable reference can be used to vary the reference frequency and to distance the harmonic of the reference frequency (spurious emissions) from the fundamental output frequency of the ADF5610 so that the harmonic of the reference frequency is filtered by the loop filter. The internal ADF5610 setup and divide ratios can be changed in the opposite direction accordingly so that the ADF5610 generates an identical output frequency without the spurious emissions inside the loop bandwidth using these same procedures.

The ADF5610 features an internal autocalibration process that seamlessly calibrates the ADF5610 when a frequency change is executed. When the ADF5610 is calibrated at any temperature, the calibration setting is guaranteed to hold across the entire operating range of the ADF5610 (−40°C to +85°C). The tuning voltage is maintained within a narrow operating range for worst case scenarios where calibration is executed at one temperature extreme and the device is operating at the other temperature extreme. For optimum temperature and spurious performance, use EIA character code C0G capacitors of the NP0 or C0G type. The use of capacitors with a temperature coefficient worse than X7R is not recommended.

For applications that require fast frequency changes, the ADF5610 supports manual calibration that enables faster settling times. Manual calibration must be characterized once for each individual ADF5610 device, at any temperature, and is valid across all temperature operating ranges of the ADF5610. Manual calibration is achieved by using autocalibration to initially determine the proper band for each frequency. The frequency vs. band information is stored in a look up table

(LUT) for future access. For more information about manual calibration, see the Manual VCO Calibration for Fast Frequency Hopping section. Any size frequency hop has a similar settling time with autocalibration disabled (Register 0x0A, Bit 11 = 1).

MUTE MODE

The ADF5610 has some support for muting the outputs. The differential divider outputs, PDIV_OUT and NDIV_OUT, can be disabled be setting VCO Register 0x01, Bit 8 = 0 to power down the divider when not in use. The RFOUT port can only be muted by powering down the VCO from VCO Register 0x02, Bit 3. However, powering down the VCO also effectively mutes the differential divider outputs simultaneously because no signal is present at the input of the buffer to the divider.

SERIAL PORT INTERFACE

The ADF5610 SPI supports both 1.8 V and 3.3 V input voltage levels. Input pins including SDI, SCK, and SEN support both voltage levels without the need for any configuration.

The SPI output (SDO pin) only supports 3.3 V levels when driven and 1.8 V and 3.3 V in open-drain mode. See Table 1 and the General-Purpose Output (GPO) section for more information.

The SPI protocol has the following general features:

- 3-bit chip address. Can address up to eight devices connected to the serial bus.
- Wide compatibility with multiple protocols from multiple vendors.
- Simultaneous read/write during the SPI cycle.
- 5-bit address space.
- 3-wire for write only capability, 4-wire for read/write capability.
- Typical serial port interface operation can be run with SCK at speeds up to 50 MHz.

SPI MODES OF OPERATION

The PLL VCO serial port interface can operate in two different modes of operation, as follows:

- Legacy mode: single slave per SPI bus.
- Open mode: up to eight slaves per SPI bus.

Both protocols support five bits of register address space. Legacy mode can support up to six bits of register address, but is restricted to five bits when compatibility with open mode is offered.

REGISTER 0x00 MODES

Register 0x00 has a dedicated function in each mode. Open mode allows wider compatibility with SPI protocols of other manufacturers.

SERIAL PORT MODE DECISION AFTER POWER-ON RESET

On power-up, both legacy mode and open mode are active and listening. All digital inputs and outputs must be low at power-up.

Selection of the desired serial port mode (protocol) is determined on the first occurrence of SEN or SCK, after which the serial port mode is fixed and only changeable by a power-down. If a rising edge on SEN is detected first, legacy mode is selected. If a rising edge on SCK is detected first, open mode is selected.

SERIAL PORT LEGACY MODE

Typical serial port legacy mode operation can be run with SCK at speeds up to 50 MHz. This mode is used with the legacy evaluation software for Analog Devices PLL products with an HMC prefix. The ADF5610 incorporates the HMC704 PLL. The ADI HMC PLL VCO evaluation software can be used to communicate with the ADF5610.

SERIAL PORT LEGACY MODE: SINGLE PLL

Legacy mode SPI operation can only address and communicate with a single PLL. The legacy mode protocol for the SPI is designed for a 4-wire interface with a fixed protocol featuring

- Compatibility with the Analog Devices line of multichip, microwave, VCO PLL solutions, including the HMC764, HMC765, HMC783, and HMC807.
- Primarily utilized for the ADI HMC PLL VCO evaluation software and the HMC700, HMC701, and HMC702 microwave products.
- One read/write bit
- Six address bits
- 24 data bits

SERIAL PORT OPEN MODE

The serial port open mode features:

- Compatibility with general serial port protocols that use a shift and strobe approach to communication.
- Up to eight supported devices of various types can be addressed from a single serial port bus.

The open mode protocol has the following general features:

- 3-bit chip address. Can address up to eight devices connected to the serial bus.
- Wide compatibility with multiple protocols from multiple vendors.
- Simultaneous read/write during the SPI cycle.
- 5-bit register address space.
- 3-wire for write only capability, 4-wire for read/write capability.

The HMC767, HMC769, and HMC778 RF PLLs with integrated VCOs also support open mode. The HMC700, HMC701, HMC702, and some generations of microwave PLLs with integrated VCOs do not support open mode. Typical open mode serial port operation can be run with SCK at speeds up to 50 MHz.

Table 14. Register 0 Comparison: Legacy Mode vs. Open Mode

Type	Legacy Mode (Single User)	Open Mode (Single or Multiple User)
Read	Chip ID, 24 bits	Chip ID, 24 bits
Write	Soft reset, general strobes	Read address, Bits[4:0] Soft reset, Bit 5 General strobes, Bits[24:6]

LEGACY MODE: SERIAL PORT WRITE OPERATION

A typical legacy mode write cycle is shown in Figure 28.

The following list is the sequence of operations for a write cycle while communicating in legacy mode.

1. The master (host) both asserts serial port enable (SEN) and clears SDI to indicate a write cycle, followed by a rising edge of SCK.
2. The slave (PLL) reads SDI on the first rising edge of SCK after SEN. SDI low indicates a write cycle ($\overline{WR}$).
3. The host places the six address bits on the next six falling edges of SCK, with the MSB first.
4. The slave registers the address bits in the next six rising edges of SCK (two to seven clock cycles).
5. The host places the 24 data bits on the next 24 falling edges of SCK, with the MSB first.
6. The slave registers the data bits on the next 24 rising edges of SCK (8 to 31 clock cycles).
7. SEN is cleared on the 32nd falling edge of SCK.
8. The 32nd falling edge of SCK completes the cycle.

LEGACY MODE: SERIAL PORT READ OPERATION

A typical legacy mode read cycle is shown in Figure 29.

The following list is the sequence of operations for a read cycle while communicating in legacy mode:

1. The master (host) asserts both SEN and SDI to indicate a read cycle, followed by a rising edge on SCK. Note that the lock detect (LD) function is usually multiplexed onto the SDO pin. It is suggested that LD only be considered valid when SEN is low. In fact, LD does not toggle until the first active data bit toggles on SDO and is restored immediately after the trailing edge of the LSB of the serial data output, as shown in Figure 29.
2. The slave (PLL) reads SDI on the first rising edge of SCK after SEN. SDI high initiates the read cycle.
3. The host places the six address bits on the next six falling edges of SCK, with the MSB first.
4. The slave registers the address bits on the next six rising edges of SCK (two to seven clock cycles).
5. The slave switches from lock detect and places the requested 24 data bits on SDO on the next 24 rising edges of SCK (eight to 31 clock cycles) with the MSB first.
6. The host registers the data bits on the next 24 falling edges of SCK (8 to 31 clock cycles).
7. The slave restores lock detect on the 32nd rising edge of SCK.
8. SEN is deasserted on the 32nd falling edge of SCK.
9. The 32nd falling edge of SCK completes the read cycle.

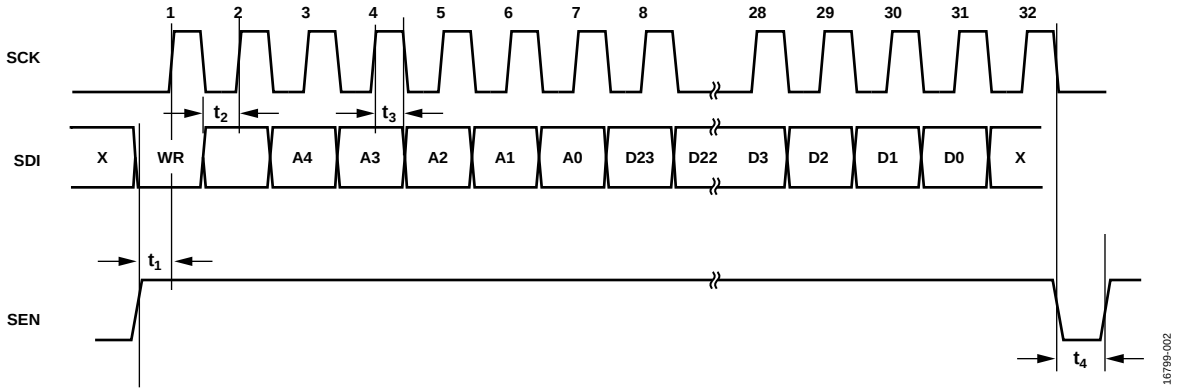


Figure 28. Legacy Mode: Serial Port Timing Diagram, Write Cycle

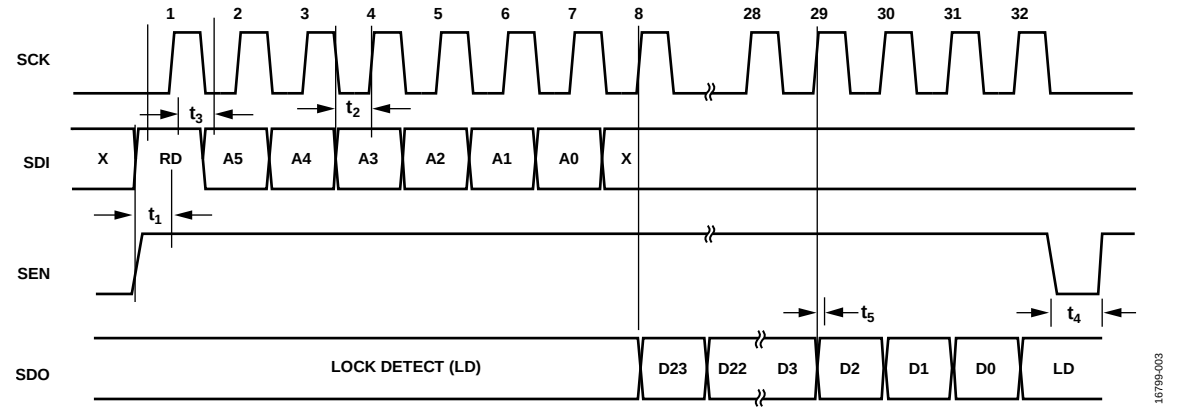


Figure 29. Legacy Mode: Serial Port Timing Diagram, Read Cycle

OPEN MODE: SERIAL PORT WRITE OPERATION

A typical write cycle is shown in Figure 30.

The following list is the sequence of operations for write cycle while communicating in open mode:

1. The master (host) places 24 bit data, Bits[D23:D0], with the MSB first, on SDI on the first 24 falling edges of SCK.
2. The slave (PLL) shifts in data on SDI on the first 24 rising edges of SCK.
3. The master places a 5-bit register address to be written to, Bits[R4:R0], with the MSB first, on the next five falling edges of SCK (25 to 29 clock cycles).
4. The slave shifts the register bits on the next five rising edges of SCK (25 to 29 clock cycles).
5. The master places a 3-bit chip address, Bits[A2:A0], with the MSB first, on the next three falling edges of SCK (30 to 32 clock cycles). Analog Devices reserves chip address Bits[A2:A0] = 000 for all RF PLL VCOs.
6. The slave shifts the chip address bits on the next three rising edges of SCK (30 to 32 clock cycles).
7. The master asserts SEN after the 32nd rising edge of SCK.
8. The slave registers the SDI data on the rising edge of SEN.
9. The master clears SEN to complete the write cycle.

OPEN MODE: SERIAL PORT READ OPERATION

A typical read cycle is shown in Figure 31 and Figure 32.

In general, in open mode, the SDO line is always active during the write cycle. During any open mode SPI cycle, SDO contains the data from the current address written in Register 0x00, Bits[4:0]. If Register 0x00, Bits[4:0] are not changed, the same data is always present on SDO when an open mode cycle is in progress. If it is desired to read from a specific address, it is necessary in the first SPI cycle to write the desired address to Register 0x00, Bits[4:0]. Then, in the next SPI cycle, the desired data is available on SDO.

An example of the open mode two-cycle procedure to read from any random address is as follows:

1. The master (host), on the first 24 falling edges of SCK places 24 bit data, Bits[D23:D0], with the MSB first, on SDI, as shown in Figure 31 and Figure 32. Set Bits[D23:D5] to zero. Bits[D4:D0] is the address of the register to be read on the next cycle.
2. The slave (PLL) shifts in data on SDI on the first 24 rising edges of SCK.
3. The master places a 5-bit register address, Bits[R4:R0] (the read address register), with the MSB first, on the next five falling edges of SCK (23 to 29 clock cycles). Bits[R4:R0] = 00000.
4. The slave shifts the register bits on the next five rising edges of SCK (23 to 29 clock cycles).
5. The master places a 3-bit chip address, Bits[A2:A0], with the MSB first, on the next three falling edges of SCK (30 to 32 clock cycles). Chip address is always 000 for RF PLL VCOs.
6. The slave shifts the chip address bits on the next three rising edges of SCK (30 to 32 clock cycles).
7. The master asserts SEN after the 32nd rising edge of SCK.
8. The slave registers the SDI data on the rising edge of SEN.
9. The master clears SEN to complete the address transfer of the two-part read cycle.
10. If the user does not wish to write data to the chip at the same time as the second cycle, it is recommended to simply rewrite the same contents on SDI to Register 0x00 on the readback part of the cycle.
11. The master places the same SDI data as the previous cycle on the next 32 falling edges of SCK.
12. The slave (PLL) shifts the SDI data on the next 32 rising edges of SCK.
13. The slave places the desired data (for example, data from the address in Register 0x00, Bits[4:0]) on SDO on the next 32 rising edges of SCK. Lock detect is disabled.
14. The master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to lock detect on SDO.

Note that if the chip address bits are unrecognized (Bits[A2:A0]), the slave tristates the SDO output to prevent a possible contention issue.

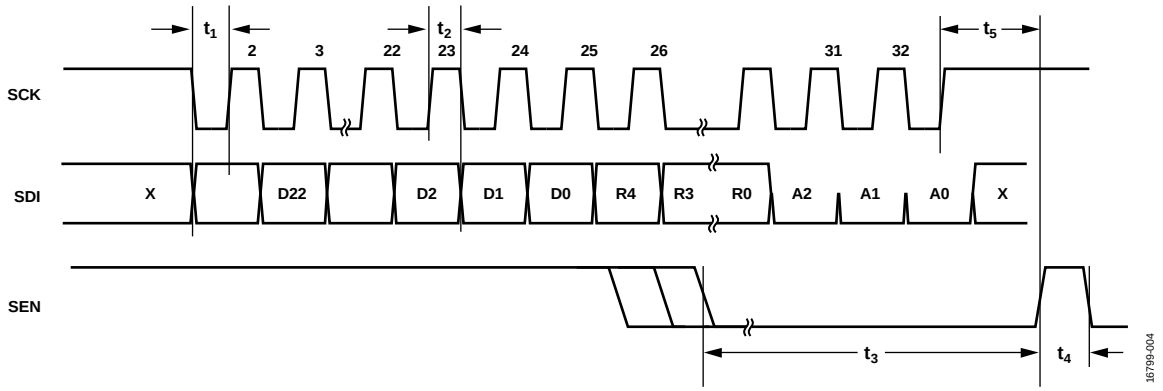


Figure 30. Open Mode: Serial Port Timing Diagram, Write Cycle

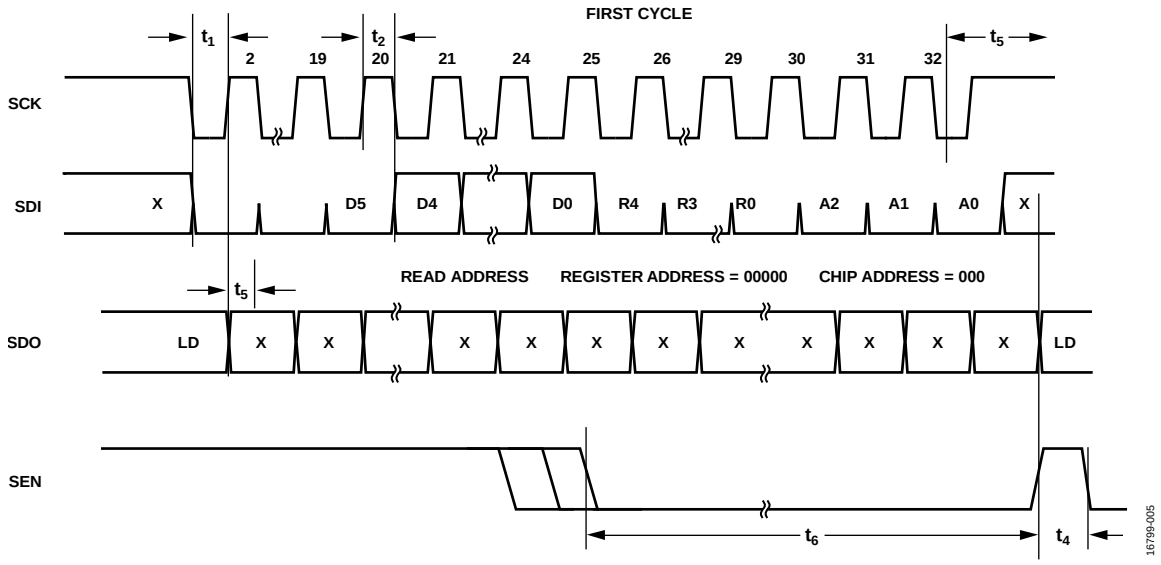
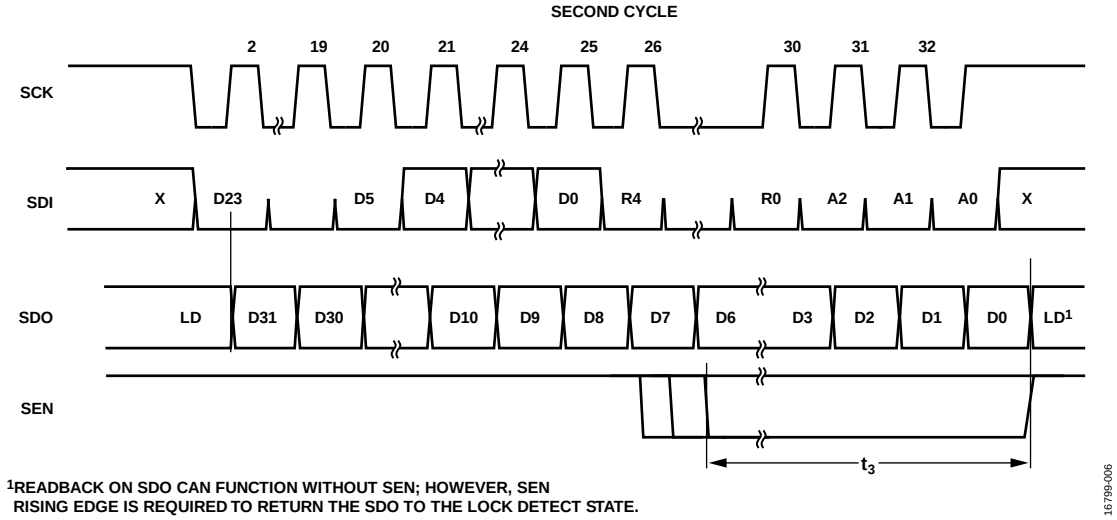


Figure 31. Open Mode: Serial Port Timing Diagram, Read Operation, First Cycle



[1]READBACK ON SDO CAN FUNCTION WITHOUT SEN; HOWEVER, SEN RISING EDGE IS REQUIRED TO RETURN THE SDO TO THE LOCK DETECT STATE.

Figure 32. Open Mode: Serial Port Timing Diagram, Read Operation, Second Cycle

PLL REGISTER MAP

ID REGISTER, RESET STROBE REGISTER, AND OPEN MODE READ REGISTER

The ID register is read only and returns the chip ID when read.

The reset strobe register only contains one functional bit field for resetting all digital content and registers to the default values. The reset strobe register is write only.

Table 15. Register 0x00, ID Register (Read Only)

Bits	Type	Name	Default	Description
23:0	Read	CHIP_ID	A7975	ADF5610 chip ID

Table 16. Register 0x00, Reset Strobe Register (Write Only)

Bits	Type	Name	Default	Description
4:0	Write	Reserved	Not Applicable	Reserved. Set all bits to 0 for proper operation.
5	Write	RST_SWRST	Not Applicable	Strobe generates soft reset. Resets all registers to the default state. Can be used in both legacy mode and open mode.
23:6	Write	Reserved	Not Applicable	Reserved. Set all bits to 0 for proper operation.

Table 17. Register 0x00, Open Mode Read Address Register (Write Only)

Bits	Type	Name	Default	Description
4:0	Write	OPEN_MODE_READ_ADDRESS	Not applicable	Read address for next cycle when in open mode, two-cycle read.
5	Write	RST_SWRST	Not Applicable	Strobe generates soft reset. Resets all registers to the default state.
23:6	Write	Reserved	Not applicable	Reserved. Set all bits to 0 for proper operation.

RST REGISTER

Table 18. Register 0x01, RST Register (Default 0x000002)

Bits	Type	Name	Default	Description
0	Read/Write	RST_CHIPEN_PIN_SELECT	0	1 = power down the PLL via the CEN pin (see the Power-Down Mode section). 0 = power down the PLL via the SPI (RST_CHIPEN_FROM_SPI), Register 0x01, Bit 1.
1	Read/Write	RST_CHIPEN_FROM_SPI	1	PLL enable bit of the SPI.
2	Read/Write	KEEP_BIAS_ON	0	Keeps internal bias generators on, ignores chip enable control.
3	Read/Write	KEEP_PFD_ON	0	Keeps PFD circuit on, ignores chip enable control.
4	Read/Write	KEEP_CP_ON	0	Keeps charge pump on, ignores chip enable control.
5	Read/Write	KEEP_REF_BUF_ON	0	Keeps reference buffer block on, ignores chip enable control.
6	Read/Write	KEEP_VCO_BUF_ON	0	Keeps VCO divider buffer block on, ignores chip enable control.
7	Read/Write	KEEP_GPO_DRIVER_ON	0	Keeps GPO output driver on, ignores chip enable control.
8	Read/Write	Reserved	0	Reserved. Program 0.
9	Read/Write	Reserved	0	Reserved. Program 0.

REFERENCE DIVIDER (RDIV) REGISTER

Table 19. Register 0x02, RDIV Register (Default 0x000001)

Bits	Type	Name	Default	Description
13:0	Read/Write	RDIV	1	Reference divider R value (see Equation 12). Using the divider requires the reference path buffer to be enabled (Register 0x08, Bit 3 = 1). 1 decimal ≤ RDIV ≤ 16,383 decimal.

FREQUENCY REGISTER, INTEGER PART

Table 20. Register 0x03, Frequency Register, Integer Part (Default 0x000019)

Bits	Type	Name	Default	Description
18:0	Read/Write	INTG_REG	25 decimal	Integer divider register. These bits are the VCO divider integer part, used in all modes (see Equation 12). Fractional mode: Minimum = 0x14 = 20 decimal. Maximum = $2^{19} - 4$ = 0x7FFFC = 524,284 decimal. Integer mode: Minimum = 0x10 = 16 decimal. Maximum = $2^{19} - 1$ = 0x7FFFF = 524,287 decimal.

FREQUENCY REGISTER, FRACTIONAL PART

Table 21. Register 0x04, Frequency Register, Fractional Part (Default 0x000000)

Bits	Type	Name	Default	Description
23:0	Read/Write	FRAC	0	VCO divider fractional part (24-bit unsigned). See the Fractional Frequency Tuning section. These bits are used in fractional mode only (N_{FRAC} = Register 0x04/2^{24}). Minimum = 0 decimal. Maximum = $2^{24} - 1$.

VCO SPI REGISTER

Register 0x05 is a special register used for indirect addressing of the VCO subsystem. Writes to Register 0x05 are automatically forwarded to the VCO subsystem by the VCO SPI FSM controller.

The auxiliary SPI outputs the contents of Register 0x05 upon receipt of a frequency change command. The auxiliary SPI data is output at the auxiliary SPI clock rate, which is based on the f_{PD} rate (Register 0x05, Bit 6). A single auxiliary SPI transfer requires 16 auxiliary SPI cycles plus four overhead cycles.

Register 0x05 is a read/write register. However, Register 0x05 holds only the contents of the last transfer to the VCO subsystem. Therefore, it is not possible to read the full contents of the VCO subsystem. Only the content of the last transfer to the VCO subsystem can be read. The ADF5610 VCO has three registers, each containing various functionality. All VCO register bits default to zero at power-up. As long as autocalibration is enabled, the FSM controls VCO Register 0x00, which is the tuning register. This register provides access to the VCO cores and frequency bands. When autocalibration is enabled, there is no need to write to VCO Register 0x00. Writes are only required when manually selecting a VCO core or frequency band. VCO Register 0x01 is the power control register. Unless the default settings are required, this register must be initialized to configure the VCO bias, output power levels, and to enable the frequency divider. Lastly, VCO Register 0x02 is the output divider register, which allows the divider ratio to be configured as well as powering down the VCO. Initialize the output divider register only if the functions are needed for the application.

For autocalibration, Register 0x05, Bits[6:0] must be set to 0. This write is required whenever autocalibration is used and is always the final register write. This write allows Register 0x03, when programming an integer frequency, or Register 0x04, for fractional frequencies, to trigger autocalibration. Setting Register 0x05, Bits[6:0] to zero is not required when manually selecting a VCO band.

VCO register writes are typically performed in descending order. However, other sequences may work as well. Depending on the application, there is a total of one to four Register 0x05 writes. For additional information, refer to the VCO Subsystem Register Map section.

Table 22. Register 0x05, VCO SPI Register (Default 0x000000)

Bits	Type	Name	Default	Description
2:0	Read/Write	VCO_ID	0	Internal VCO subsystem ID.
6:3	Read/Write	VCO_REGADDR	0	VCO subsystem register address. These bits are for interfacing with the VCO. See the VCO Serial Port Interface (VSPI) section.
15:7	Read/Write	VCO_DATA	0	VCO subsystem data. These bits are used to write the data to the VCO subsystem.

Δ-Σ CONFIGURATION REGISTER

Table 23. Register 0x06, Δ-Σ Configuration Register (Default 0x200B4A)

Bit	Type	Name	Default	Description
1:0	Read/Write	SEED_SELECT	2	Selects the seed in fractional mode. Writes to this register are stored in the ADF5610 and are loaded into the modulator only when a frequency change is executed and when Register 0x06, Bit 8 = 1. 0: 0 seed. 1: LSB seed. 2: 0xB29D08 seed. 3: 0x50F1CD seed.
6:2	Read/Write	Reserved	18 decimal (0x12)	Reserved.
7	Read/Write	FRAC_BYPASS	0	Bypass fractional mode. When bypassing the fractional modulator, the output is ignored, but the fractional modulator continues to be clocked when SD enable = 1. Use this bit to test the isolation of the digital fractional modulator from the VCO output in integer mode. 0: use modulator, required for fractional mode. 1: bypass modulator, required for integer mode.
10:8	Read/Write	Reserved	3 decimal	Program to 7 decimal. Default initialization
11	Read/Write	SD_ENABLE	1	This bit controls whether autocalibration starts on an integer write or a fractional write. 0: disables fractional core, use for integer mode or integer mode with CSP. 1: enables fractional core (required for fractional mode), or integer isolation testing.
20:12	Read/Write	Reserved	0	Reserved.
21	Read/Write	AUTO_CLK_CONFIGURATION	1	Program to 0.
22	Read/Write	Reserved	0	Reserved.

LOCK DETECT REGISTER

Table 24. Register 0x07, Lock Detect Register (Default 0x00014D)

Bit	Type	Name	Default	Description
2:0	Read/Write	LKD_WINCNT_MAX	5 decimal	The lock detect window sets the number of consecutive counts of the divided VCO that must be within the lock detect window to declare lock. 0: 5. 1: 32. 2: 96. 3: 256. 4: 512. 5: 2048. 6: 8192. 7: 65,535.
3	Read/Write	LKD_ENABLE	1	Enable internal lock detect. See the Serial Port Interface section.
5:4	Read/Write	Reserved	0	Reserved.

Bit	Type	Name	Default	Description
6	Read/Write	LKD_ONESHOT_SEL	1	Lock detection window timer selection. 1: digital programmable timer. 0: analog one shot, nominal 10 ns window.
9:7	Read/Write	LKD_ONESHOT_DURATION	2	Lock detection, digital window duration. 0: half cycle. 1: one cycle. 2: two cycles. 3: four cycles. 4: eight cycles. 5: 16 cycles. 6: 32 cycles. 7: 64 cycles.
11:10	Read/Write	LKD_CONFIG	0	Lock detect digital timer frequency control (see the Lock Detect section for more information). 00: fastest. 11: slowest.
12	Read/Write	Reserved	0	Reserved.
13	Read/Write	LKD_AUTOCAL_WHEN_UNLOCKED	0	1: autorelock attempts to relock one time, if lock detect fails for any reason.

ANALOG ENABLE (EN) REGISTER

Table 25. Register 0x08, Analog EN Register (Default 0xC1BEFF)

Bit	Type	Name	Default	Description
0	Read/Write	BIAS_EN	1	Enables main chip bias reference.
1	Read/Write	CP_EN	1	Charge pump enable.
2	Read/Write	PD_EN	1	PD enable.
3	Read/Write	REFBUF_EN	1	Reference path buffer enable.
4	Read/Write	VCOBUF_EN	1	VCO path RF buffer enable.
5	Read/Write	GPO_PAD_EN	1	0: disables the SDO pin. 1: enables the GPO port or allows a shared SPI. When Bit 5 = 1 and Register 0xF, Bit 7 = 1, the SDO pin is always driven, which is required for use of the GPO port. When Bit 5 = 1 and Register 0xF, Bit 7 = 0, SDO is off when an unmatched chip address is seen on the SPI. Allows shared SPI with other compatible devices.
9:6	Read/Write	Reserved	11 decimal (0x0B)	Reserved.
10	Read/Write	VCO_SIDE_BIAS	1	VCO buffer and prescaler bias enable.
18:11	Read/Write	Reserved	55 decimal (0x37)	Reserved. Program to 55 decimal (0x37).
19	Read/Write	DIV_SEL	0	8 GHz divide by 2 enable. Allows PLL operation up to 8 GHz. When input to PLL is less than 4000 MHz, set to 0 decimal to bypass internal divider. When input to PLL is greater than or equal to 4.0 GHz, set to 1 decimal to enable internal fixed divide by 2.
20	Read/Write	Reserved	0	Reserved. Program 0.
21	Read/Write	HI_FREQ_RF_SEL	0	High frequency reference select. Program to 1 for reference frequencies from 200 MHz to 350 MHz. Program to 0 for reference frequencies less than 200 MHz.
23:22	Read/Write	Reserved	3 decimal	Reserved.

CHARGE PUMP REGISTER

Table 26. Register 0x09, Charge Pump Register (Default 0x403264)

Bit	Type	Name	Default	Description
6:0	Read/Write	CP_DOWN_MAG	100 decimal, 0x64	Charge pump down gain control, 20 µA per step. Affects fractional phase noise and lock detect settings. 0 = 0 µA. 1 = 20 µA. 2 = 40 µA. … 127 = 2.54 mA.
13:7	Read/Write	CP_UP_MAG	100 decimal, 0x64	Charge pump up gain control, 20 µA per step. Affects fractional phase noise and lock detect settings. 0 = 0 µA. 1 = 20 µA. 2 = 40 µA. … 127 = 2.54 mA.
20:14	Read/Write	CP_LEAK_MAG	0	Charge pump offset control, 5 µA per step. Affects fractional phase noise and lock detect settings. 0 = 0 µA. 1 = 5 µA. 2 = 10 µA. … 127 = 635 µA.
21	Read/Write	CP_LEAK_UP_EN	0	Charge pump up offset. Recommended setting in fractional mode using a passive loop = 0 decimal. Set to 0 decimal in integer mode.
22	Read/Write	CP_LEAK_DN_EN	1	Charge pump down offset. Recommended setting in fractional mode using a passive loop equals 1 decimal. Set to 0 decimal in integer mode.
23	Read/Write	CP_HIK_EN	0	High current charge pump. Low noise, narrow compliance range. Requires an op amp.

AUTOCALIBRATION REGISTER

Table 27. Register 0x0A, VCO Autocalibration Configuration Register (Default 0x002205), Program to 0x002047

Bit	Type	Name	Default	Description
2:0	Read/Write	VTUN_RESOLUTION	5	R divider cycles. 0: 1 cycle. 1: 2 cycles. 2: 4 cycles. … 7: 256 cycles.
9:3	Read/Write	Reserved	64d	Reserved. Program 8 decimal.
10	Read/Write	VTUN_FORCE_CAPS	0	Force capacitors programmed in Register 0x05. Program 0 for normal operation.
11	Read/Write	VTUN_DISABLE	0	Disable autocalibration. Program 0 for normal operation using VCO autocalibration.
12	Read/Write	VCO_SPI_DISABLE	0	0: normal operation. 1: this bit disables the serial transfers to the VCO subsystem (via Register 0x05).
14:13	Read/Write	AUX_CLK_DIV_SEL	1	These bits set the autocalibration FSM and VSPI clock (100 MHz maximum). 0: input crystal reference. 1: input crystal reference divide by 4. 2: input crystal reference divide by 16. 3: input crystal reference divide by 32.
16:15	Read/Write	Reserved	0	Reserved.

PHASE DETECTOR (PD) REGISTER

Table 28. Register 0x0B, PD Register (Default 0x0F8061)

Bit	Type	Name	Default	Description
2:0	Read/Write	PFD_DEL_SEL	1	Sets the PFD reset path delay (recommended setting is 001).
4:3	Read/Write	Reserved	0	Reserved.
5	Read/Write	PFD_UP_EN	1	Enables the PFD up output.
6	Read/Write	PFD_DN_EN	1	Enables the PFD down output.
8:7	Read/Write	FIX_CP_MODE	0	Cycle slip prevention mode. This delay varies by ±10% with temperature and ±12% with process. Extra current (~8 mA) is driven into the loop filter when the phase error is larger than the following: 0: Disabled. 1: 5.4 ns. 2: 14.4 ns. 3: 24.1 ns. Only use CSP with comparison frequencies ≤ 50 MHz, otherwise disable. Always confirm loop stability when using CSP.
9	Read/Write	CP_FORCE_UP	0	Forces CP up output to turn on. Use for test only.
10	Read/Write	CP_FORCE_DN	0	Forces CP down output to turn on. Use for test only.
11	Read/Write	CP_FORCE_MID	0	Forces CP to midrail. Use for test only.
19:12	Read/Write	Reserved	248 decimal (0xF8)	Reserved.
[21:20]	Read/Write	DIV_PULSEWIDTH_SEL	0	Divider pulse width. 0: shortest. 3: longest.
[23:22]	Read/Write	Reserved	0	Reserved.

EXACT FREQUENCY MODE REGISTER

Table 29. Register 0x0C, Exact Frequency Mode Register (Default 0x000000)

Bit	Type	Name	Default	Description
13:0	Read/Write	CHANNELSPERBOUND	0	Number of channels per f_{PD}. The comparison frequency divided by the correction rate must be an integer. Frequencies at exactly the correction rate have zero frequency error. 0: disabled. 1: disabled. 2: 16383 decimal (0x3FFF).

GENERAL-PURPOSE, SPI, AND REFERENCE DIVIDER (GPO_SPI_RDIV) REGISTER

Table 30. Register 0x0F, GPO_SPI_RDIV Register (Default 0x000001)

Bit	Type	Name	Default	Description
4:0	Read/Write	GPO_SELECT	1d	The signal selected by this bit is an output to the SDO pin when the SDO pin is enabled via Register 0x08, Bit 5. 0: data from Register 0x0F, Bit 5. 1: lock detect output. 2: lock detect trigger. 3: lock detect window output. 4: ring oscillator test. 5: pull-up resistor is ~230 Ω from CSP. 6: pull-down resistor is ~230 Ω from CSP. 7: reserved. 8: reference buffer output. 9: reference divider output.

Bit	Type	Name	Default	Description
				10: VCO divider output. 11: modulator clock from VCO divider. 12: auxiliary clock. 13: auxiliary SPI clock. 14: auxiliary SPI enable. 15: auxiliary SPI data output. 16: PD down. 17: PD up. 18: internal clock path third-order, Δ-Σ modulator (DSM3) clock delay. 19: DSM3 core clock. 20: autostrobe integer write. 21: autostrobe fractional write 22: autostrobe auxiliary SPI. 23: SPI latch enable. 24: VCO divider sync reset. 25: seed load strobe. 26 to 29: do not use. 30: SPI output buffer enable. 31: soft reset.
5	Read/Write	GPO_STATIC_TEST	0	1: GPO test data.
6	Read/Write	GPO_ALWAYS	0	Prevent automux on SDO. 0: automuxes between SDO and GPO data. 1: outputs GPO data only.
7	Read/Write	GPO_OUTBUFF_HIGH	0	LDO driver always on. 0: SDO pin driver only on during SPI read cycle. 1: SDO pin driver always on. Prevents SPI from disabling SDO. Set to 1 if using SPI mode.
8	Read/Write	GPO_PULLUP_DISABLE	0	Disable P channel MOSFET transistor (PFET). 0: enable SDO pin high drive. 1: disable SDO pin high drive.
9	Read/Write	GPO_PULLDN_DISABLE	0	Disable N channel MOSFET transistor (NFET). 0: enable SDO pin low drive. 1: disable SDO pin low drive.

VCO TUNE REGISTER

The VCO tune register is a read only register.

Table 31. Register 0x10, VCO Tune Register (Default 0x000020)

Bit	Type	Name	Default	Description
7:0	Read	SAR_DATA_IN	32	Indicates the VCO band setting selected by the autocalibration FSM to yield the nearest free running VCO frequency to the desired operating frequency. Not valid when Register 0x10, Bit 8 = 1, autocalibration busy. When a manual change is made to the VCO band settings, this register does not indicate the current VCO band position. VCO subsystems may not use all the MSBs, in which case the unused bits are don't care bits. 0: highest frequency. 1: second highest frequency. … 255: lowest frequency.
8	Read	VTUNE_BUSY	0	Busy when the autocalibration FSM is searching for the nearest band setting to the requested frequency.

SUCCESSIVE APPROXIMATION REGISTER

The successive approximation register (SAR) is a read only register.

Table 32. Register 0x11, Successive Approximation Register (Default 0x07FFFF)

Bit	Type	Name	Default	Description
18:0	Read	SAR_ERR_ABS_MIN	2^{19} to 1	SAR error magnitude counts
19	Read	SAR_ERR_SIGN	0	SAR error sign 0: error is positive 1: error is negative

GENERAL-PURPOSE 2 REGISTER

The GPO2 register is a read only register.

Table 33. Register 0x12, GPO2 Register (Default 0x000000)

Bit	Type	Name	Default	Description
0	Read	GPO	0	GPO state
1	Read	LOCK_DETECT	0	Lock detect status 1: locked 0: unlocked

BUILT IN SELF TEST (BIST) REGISTER

The BIST register is a read only register.

Table 34. Register 0x13, BIST Register (Default 0x001259)

Bit	Type	Name	Default	Description
16:0	Read	Reserved	4697 decimal	Reserved

VCO SUBSYSTEM REGISTER MAP

The VCO subsystem uses indirect addressing via Register 0x05, unlike the PLL registers. Because the VCO contains three registers and all are accessed via PLL Register 0x05, it is necessary to add the VCO Chip ID (Register 0x000) and VCO Register Address (Register 0x00xx) prior to sending the VCO data bits shown in Table 35, Table 36, and Table 37. For more detailed information on how to write to the VCO subsystem, see the VCO Serial Port Interface (VSPI) section.

Note that VCO Register 0x00, Bit 0 controls the switch that selects either the internal, temperature compensated tuning voltage or VT.

The VCO tuning register is write only.

Table 35. VCO Register 0x00, Tuning Register

Bit	Type	Name	Default	Description
0	Write	VT_SEL	0	0: VCO tune voltage provided by an internal, temperature compensated calibration voltage 1: VCO tune voltage provided by VT pin
8:1	Write	CAPS	16	VCO subband selection 0000 0000 = Subband 0 (contains maximum frequency) 1111 1111 = Subband 255 (contains minimum frequency)

VCO POWER CONTROL REGISTER

The VCO power control register is a write only register.

Table 36. VCO Register 0x01, Power Control Register

Bit	Type	Name	Default	Description
1:0	Write	RFOUT_PWR_CNTL	0	RFOUT power control 0: 2 dBm 1: 3 dBm 2: 4 dBm 3: 5 dBm
4:2	Write	VCO_BIAS_CNTL	0	VCO bias control 0: low current mode 7: high performance mode
6:5	Write	DIV_PWR_CNTL	0	Divider output power 0: −4 dBm 1: 0 dBm 2: 0 dBm 3: 3 dBm (nominal single-ended power level of PDIV_OUT and NDIV_OUT)
7	Write		0	Reserved. Program to 0 decimal
8	Write	DIV_EN	0	Divider enable 0: power down differential output divider and buffer amplifier 1: enable differential output divider and buffer amplifier

Example: Optimizing Power and Phase Noise Performance at RFOUT Using the VCO Subsystem

For optimum phase noise on all ports and maximum power at the RFOUT port, configure VCO Register 0x01, Bits[4:0] data bits by accessing the VCO subsystem of the ADF5610. The VCO subsystem register is accessed via a write to the PLL subsystem using Register 0x05 = 0011111110001000b = 0x3F88.

The following settings illustrate how settings for VCO Register 0x01 translate to Register 0x05.

- Register 0x05, Bits[2:0] = 000b. 3-bit VCO_ID, target subsystem address = 000b.
- Register 0x05, Bits[6:3] = 0001b. VCO subsystem register address.

The remaining bits, Register 0x05, Bits[15:7], are data bits for VCO Register 0x01, Bits[8:0].

- Register 0x05, Bits[8:7] = 11b. RFOUT maximum output power, 5 dBm nominally.
- Register 0x05, Bits[11:9] = 111b. VCO bias, high performance mode.
- Register 0x05, Bits[13:12] = 11b. Differential divider output power set to maximum. Note that disabling the differential output divider, VCO Register 0x01, Bit 8, also disables the differential buffer amplifier.
- Register 0x05, Bit 14 = 0b. Reserved.
- Register 0x05, Bit 15 = 0b. Disable differential output divider (improves RFOUT power level by ~1 dBm).

VCO DIFFERENTIAL OUTPUT DIVIDER REGISTER

This is a write only register. To make use of the divider ratio settings, the divider must be enabled via VCO Register 0x01, Bit 8 = 1.

Table 37. VCO Register 0x02, Output Divider Register

Bit	Type	Name	Default	Description
2:0	Write	DIFF_DIV_RATIO	0	RF divider ratio. 0: f_O/128 1: f_O/64. 2: f_O/32. 3: f_O/16. 4: f_O/8. 5: f_O/4. 6: f_O/2. 7: f_O/1 (bypass).
3	Write	PD_VCO	0	0: enable VCO and buffer amplifier. 1: power down VCO and buffer amplifier.
8:4	Write	Reserved	0	Reserved. Program 0 decimal.

Example: Setting the Differential Output Divider to Divide by 64 via the VCO Subsystem

The VCO registers are written in reverse order (highest to lowest). First, set the divide ratio then enable the divider. Finally, select the band.

To write 0 0000 0001 into VCO Register 0x02 (VCO_ID = 000b) and set the VCO output divider to divide by 64, the following must be written to Register 0x05 = 0 0000 0001 0010 000 = 0x0090:

- Register 0x05, Bits[2:0] = 000. 3-bit VCO_ID, target subsystem address = 000b.
- Register 0x05, Bits[6:3] = 0010. VCO Register 0x02 address.
- Register 0x05, Bits[16:7] = 0 0000 0001. Divide by 64, maximum output RF gain.

Next, use the same settings for Bits[14:0] in the Example: Optimizing Power and Phase Noise Performance at RFOUT Using the VCO Subsystem section for VCO Register 0x01. To enable the differential output divider, simply change VCO Register 0x01, Bit 8 = 1. The full VCO subsystem write via PLL Register 0x05 = 0011111110001000 = 0xBF88. The following settings illustrate how settings for VCO Register 0x01 translate to Register 0x05.

- Register 0x05, Bits[2:0] = 000b. 3-bit VCO_ID, target subsystem address = 000b.
- Register 0x05, Bits[6:3] = 0001b. VCO subsystem register address.
- Register 0x05, Bits[8:7] = 11b. RFOUT maximum output power, 5 dBm nominally.
- Register 0x05, Bits[11:9] = 111b. VCO bias, high performance mode.
- Register 0x05, Bits[13:12] = 11b. Divider output power, 3 dBm.
- Register 0x05, Bit 14 = 0b. Reserved.
- Register 0x05, Bit 15 = 1b. Enable differential output divider (note that RFOUT power level drops by ~1 dBm).

If no VCO band change is required, register writes are complete.

Example: Changing Frequency after Configuring the VCO

If writing to the synthesizer for the first time or if the user is changing frequencies, a write to Register 0x05 = 0 to allow a subsequent frequency change via autocalibration is required. The last write in the PLL register sequence triggers the frequency update. If an integer value results at the phase detector input, the last write in the register sequence is PLL Register 0x03. If a fractional value results at the phase detector input, the last write in the register sequence is PLL Register 0x04.

If the band for the desired RFOUT frequency (prior to division) is already known, the VCO band can be written to directly via VCO Register 0x00 by disabling the temperature controlled VT calibration voltage and manually selecting the band via VCO Register 0x00.

For example, assume that the desired RFOUT frequency prior to division is 8 GHz and 8 GHz falls in Subband 205 (see Table 35) when autocalibration is used at room temperature. First, set VCO Register 0x02 = 0x0090 for divide by 64 and maximum output power at PDIV_OUT and NDIV_OUT. Next, set VCO Register 0x01 = 0xBF88 for maximum output power on the RFOUT port and the optimal phase noise performance on all ports. Lastly, configure the VCO Register 0x00 subsystem write via PLL Register 0x05 = 1100110100000000 = 0xCD00. The following are individual bit field settings used in Register 0x05 to achieve the write to VCO Register 0x00.

- Register 0x05, Bits[2:0] = 000b. 3-bit VCO_ID, target subsystem address = 000b.
- Register 0x05, Bits[6:3] = 0000b. VCO subsystem register address.
- Register 0x05, Bit 7 = 0b. Disable autocalibration.
- Register 0x05, Bits[15:8] = 1100101 (205 decimal). Subband 205 = Subband 77 of the lower VCO core (see Table 35).

APPLICATIONS INFORMATION

The ADF5610 contains two multiband VCOs that cover an octave frequency range. To ensure optimum performance, it is essential to provide biasing to all supply pins using low noise voltage regulators, such as the LT3042 and LT3045. The use of three regulators is ideal because it maximizes isolation by allowing one regulator for VCO biasing at 5.0 V, one regulator for the 3.3 V digital supply pins (VDDLS, VPPCP, VCCPD, and DVDD), and one regulator for the 3.3 V analog supply pins (VDD1, VDD2, VDD3, RVDD, BIAS, VCCPS, and VCCHF). Alternatively, a single LT3045 can be used to combine the 3.3 V analog and digital supply pins, but combining the pins may lead to some degradation in spurious performance due to the reduction in isolation between these circuits.

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The PCB used in the application uses RF circuit design techniques. Signal lines have 50 Ω impedance, whereas the package ground leads and exposed pad are connected directly to the ground plane. Use a sufficient number of thermal vias to connect the top and bottom ground planes. Use of double shielded cables with the proper adapters is strongly recommended for the dc connections. High quality RF cables that can support microwave frequencies are required for the RF outputs. The upper end of the frequency range for the RF cable must ideally include any harmonics that are important to consider at the highest frequency of operation. The evaluation board details are available on www.analog.com/EVAL-ADF5610.

EVALUATION KIT CONTENTS

The evaluation kit contains one EV-ADF5610SD1Z evaluation board, a CD ROM that contains the user manual, evaluation PCB schematic, evaluation software, and Analog Devices PLL design software.

OUTLINE DIMENSIONS

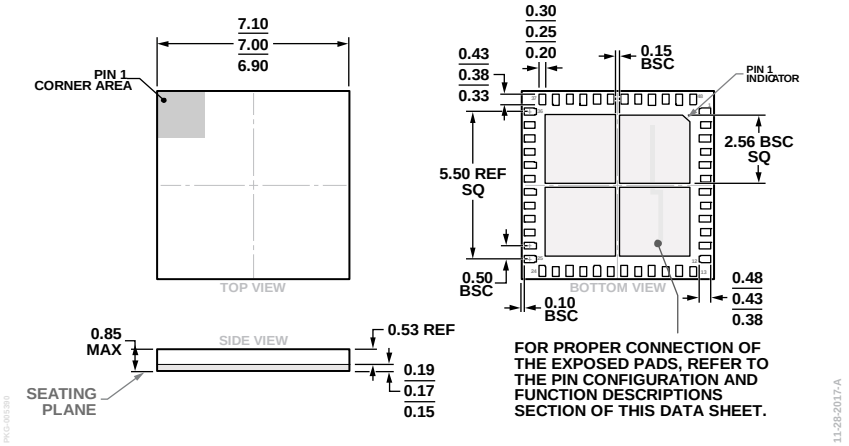


Figure 33. 48-Terminal Land Grid Array [LGA]
(CC-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Lead Finish[3]	Moisture Sensitivity Level (MSL) Rating[4]	Temperature Range	Package Description	Package Option
ADF5610BCCZ	ENEPIG	MSL3	−40°C to +85°C	48-Terminal Land Grid Array [LGA]	CC-48-1
ADF5610BCCZ-RL7	ENEPIG	MSL3	−40°C to +85°C	48-Terminal Land Grid Array [LGA]	CC-48-1
EV-ADF5610SD1Z				Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] USB interface board, EVAL-SDP-CS1Z, must be ordered separately.
[3] ENEPIG is electroless nickel electroless palladium immersion gold.
[4] See the Absolute Maximum Ratings section for more information.

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