0.1 GHz to 6.0 GHz,0.5 dB LSB, 6-Bit,GaAs Digital Attenuator

Enhanced Product

HMC624A-EP

FEATURES

- Attenuation range: 0.5 dB (LSB) steps to 31.5 dB
- Low insertion loss: 1.6 dB at 3 GHz
- Excellent attenuation accuracy
- High linearity
  - Input 0.1dB compression (P0.1dB): 33 dBm typical
  - Input third-order intercept (IP3): 55 dBm typical
- High RF input power handling: 28 dBm
- Low phase shift: 25° at 3 GHz
- Single-supply operation: 3 V to 5 V
- CMOS-/TTL-compatible control
- 24-lead, 4 mm × 4 mm LFCSP package

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available upon request

APPLICATIONS

- Cellular infrastructure
- Microwave radios and very small aperture terminals (VSATs)
- Test equipment and sensors
- Intermediate frequency (IF) and radio frequency (RF) designs

FUNCTIONAL BLOCK DIAGRAM

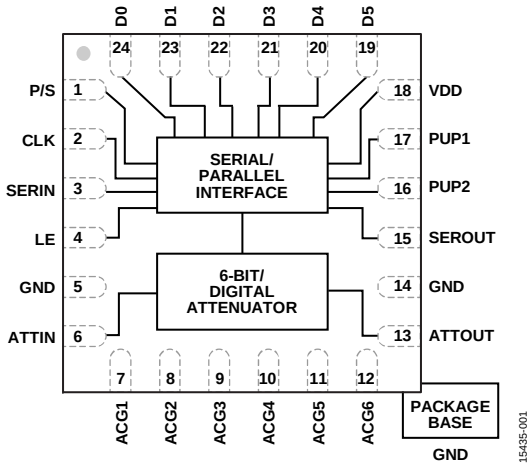

Figure 1.

GENERAL DESCRIPTION

The HMC624A-EP is a 6-bit digital attenuator with a 31.5 dB attenuation control range in 0.5 dB steps.

The HMC624A-EP offers excellent attenuation accuracy and high input linearity over the specified frequency range from 100 MHz to 6.0 GHz. However, this digital attenuator features external ac grounding capacitors to extend the operation below 100 MHz.

The HMC624A-EP is integrated with two dies: a CMOS driver and a gallium arsenide (GaAs) RF attenuator. The CMOS driver provides both serial and parallel control of the RF attenuator.

The device also features a user-selectable power-up state and a serial output port for cascading other serial controlled components.

The HMC624A-EP operates with a single positive supply voltage from 3 V to 5 V and provides a CMOS-/TTL-compatible control interface.

The HMC624A-EP comes in a RoHS compliant, compact, 4 mm × 4 mm LFCSP package.

Additional application and technical information can be found in the HMC624A data sheet.

Rev. A

Document Feedback

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Technical Support
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REVISION HISTORY

9/2017—Rev. 0 to Rev. A

Changed CP-24-2 to CP-24-22 ..... Throughout
Updated Outline Dimensions 10
Changes to Ordering Guide 10

7/2017—Revision 0: Initial Revision

SPECIFICATIONS

V_{DD} = 3 V to 5 V, control input voltage (V_{CTL}) = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		6.0	GHz
INSERTION LOSS		0.1 GHz to 3 GHz		1.6	2.4	dB
		3 GHz to 6.0 GHz		2.3	3.8	dB
ATTENUATION		0.1 GHz to 6.0 GHz				
Range		Between minimum and maximum attenuation states		31.5		dB
Step Size		Between any successive attenuation states		0.5		dB
Step Error		Between any successive attenuation states		<±0.2		dB
State Error		All attenuation states, referenced to insertion loss state				
		0.1 GHz to 0.8 GHz	−(0.1 + 5% of attenuation state)		+(0.1 + 5% of attenuation state)	dB
		0.8 GHz to 6.0 GHz	−(0.3 + 3% of attenuation state)		+(0.3 + 3% of attenuation state)	dB
RETURN LOSS (ATTIN and ATTOUT)		All attenuation states, 0.1 GHz to 6.0 GHz		15		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		100 MHz to 3 GHz		25		Degrees
		3 GHz to 6.0 GHz		50		Degrees
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		60		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		90		ns
INPUT LINEARITY[1]		All attenuation states, 250 MHz to 6.0 GHz				
0.1 dB Compression	P0.1dB	V_{DD} = 3 V		27		dBm
		V_{DD} = 5 V		33		dBm
Third-Order Intercept	IP3	V_{DD} = 3 V to 5 V, 10 dBm per tone, 1 MHz spacing		55		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 3 V to 5 V		3		mA
DIGITAL CONTROL INPUTS		P/S, CLK, SERIN, LE, D0 to D5, PUP1, and PUP2 pins				
Voltage						
Low	V_{INL}	V_{DD} = 3 V	0		0.5	V
		V_{DD} = 5 V	0		0.8	V
High	V_{INH}	V_{DD} = 3 V	2		3	V
		V_{DD} = 5 V	2		5	V
Current		V_{DD} = 3 V to 5 V				
Low	I_{INL}			15		µA
High	I_{INH}			65		µA
DIGITAL CONTROL OUTPUT		SEROUT				
Voltage						
Low	V_{OUTL}			0		V
High	V_{OUTH}			V_{DD}		V
Current						
Low	I_{OUTL}				1	mA
High	I_{OUTH}				1	mA

[1] Input linearity performance degrades at frequencies less than 250 MHz; see Figure 10 to Figure 17.

TIMING SPECIFICATIONS

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period	70			ns
t_{CS}	Control setup time	15			ns
t_{CH}	Control hold time		20		ns
t_{LN}	LE setup time	15			ns
t_{LEW}	Minimum LE pulse width		10		ns
t_{LES}	Minimum LE pulse spacing		630		ns
t_{CKN}	Serial clock hold time from LE		0		ns
t_{PH}	Data hold time from LE		10		ns
t_{PS}	Data setup time to LE		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	5.6 V
Digital Control Input Voltage	−1 V to V_{DD} + 1 V
RF Input Power[1] (All Attenuation States, f = 250 MHz to 6 GHz, T_{CASE} = 105°C)	
V_{DD} = 3 V	25 dBm
V_{DD} = 5 V	28 dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 105°C)	0.36 W
Temperature	
Junction, T_J	150°C
Operating	−55°C to +105°C
Storage	−65°C to +150°C
Reflow[2] ((Moisture Sensitivity Level 3 (MSL3) Rating)	260°C
ESD Sensitivity	
Human Body Model (HBM)	300 V

[1] For power derating at frequencies less than 250 MHz, see Figure 2.
[2] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

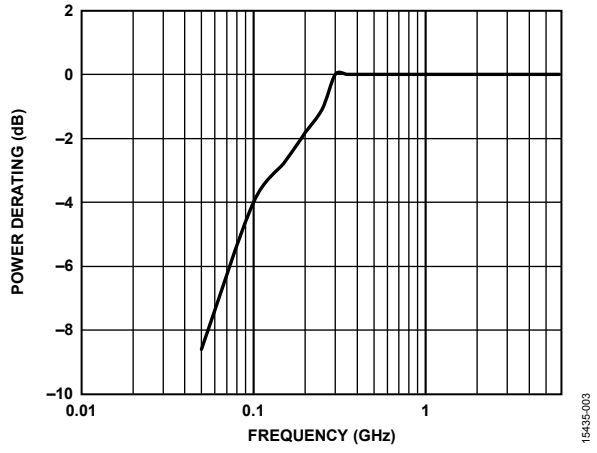


Figure 2. Power Derating at Frequencies < 250 MHz

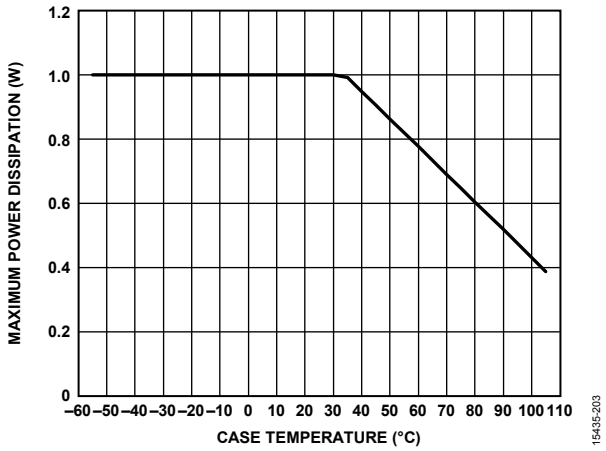


Figure 3. Power Derating vs. T_{CASE}

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-24-22[1]	116	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

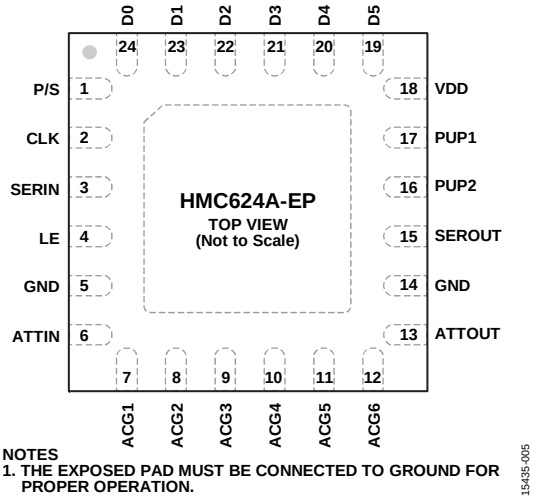


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to low. For serial mode operation, set this pin to high.
2	CLK	Serial Interface Clock Input.
3	SERIN	Serial Interface Data Input.
4	LE	Latch Enable Input.
5, 14	GND	Ground. These pins must be connected to ground.
6	ATTIN	Attenuator RF Input. This pin can also be used as an output because the design is bidirectional. ATTIN is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required.
7 to 12	ACG1 to ACG6	AC Grounding Capacitor Pins. These pins can be left unconnected when operating above 700 MHz. For frequencies less than 700 MHz, connect capacitors larger than 100 pF as close to the ACGx pins as possible. Select the capacitor value for the lowest frequency of operation.
13	ATTOUT	Attenuator RF Output. This pin can also be used as an input because the design is bidirectional. ATTOUT is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required.
15	SEROUT	Serial Interface Data Output. Serial input data is delayed by six clock cycles.
16, 17	PUP2, PUP1	Power-Up State Selection Pins. These pins set the attenuation value at power-up.
18	VDD	Power Supply.
19 to 24	D5 to D0	Parallel Control Voltage Inputs. These pins select the required attenuation. There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (V_{IH} or V_{IL}) and not be left floating.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

INTERFACE SCHEMATICS

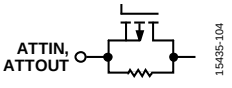


Figure 5. ATTIN, ATTOUT Interface Schematic

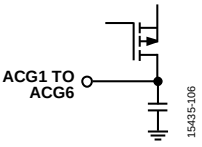


Figure 7. ACGx Pin Interface Schematic

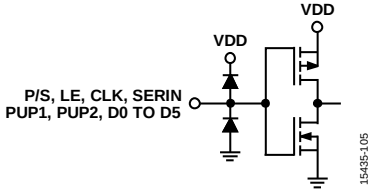


Figure 6. Digital Control Input Interface

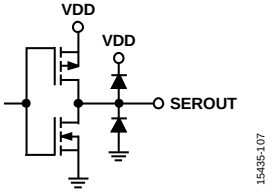


Figure 8. SEROUT Pin Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS

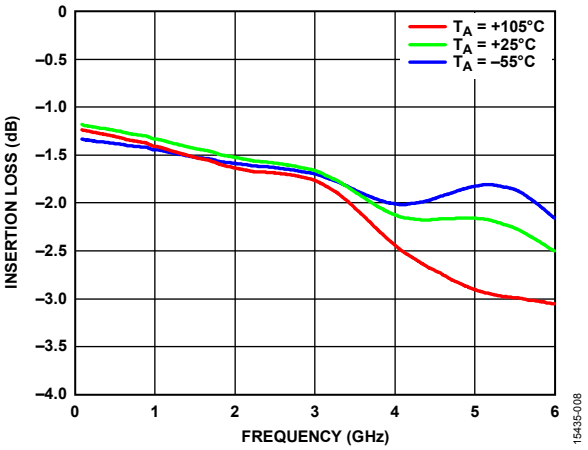


Figure 9. Insertion Loss vs. Frequency over Temperature

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

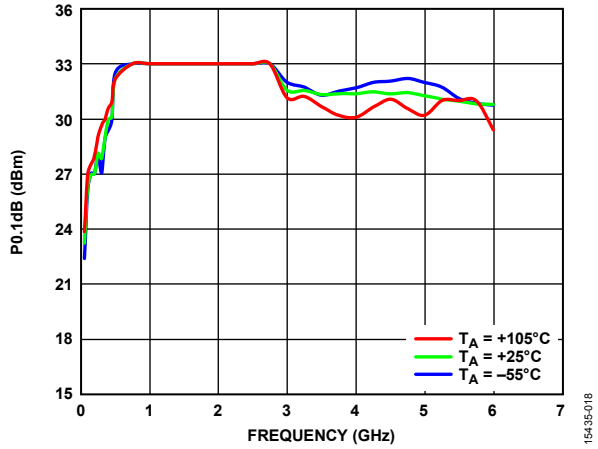


Figure 10. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V

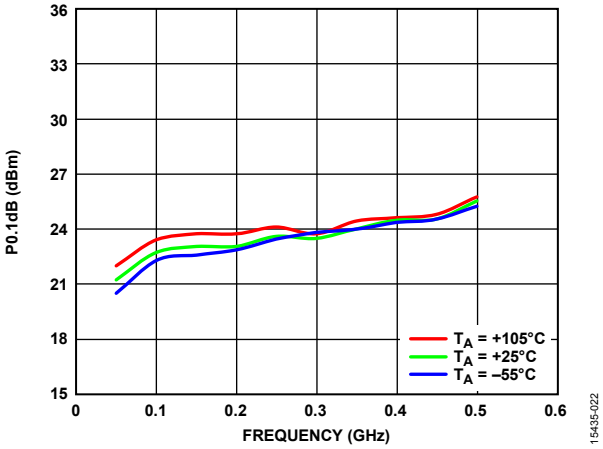


Figure 13. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V (Low Frequency Detail)

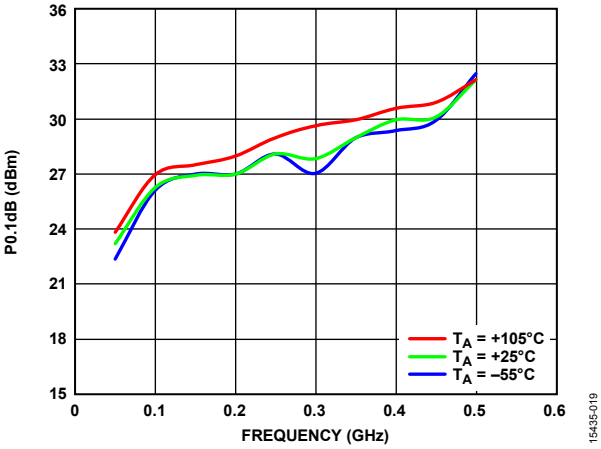


Figure 11. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V (Low Frequency Detail)

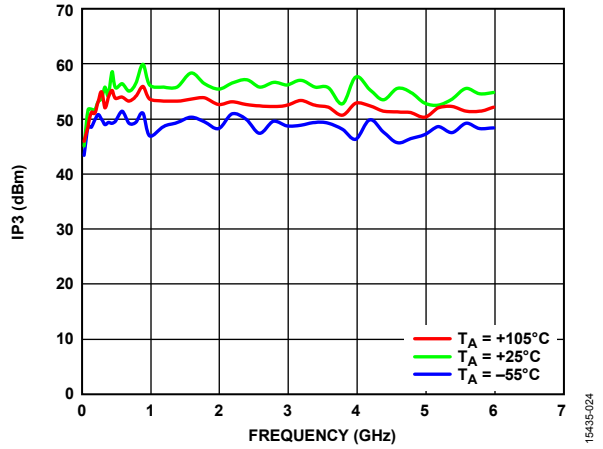


Figure 14. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V

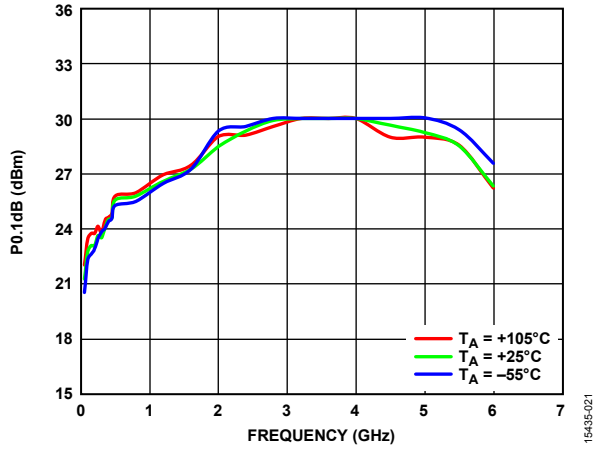


Figure 12. Input P0.1dB vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V

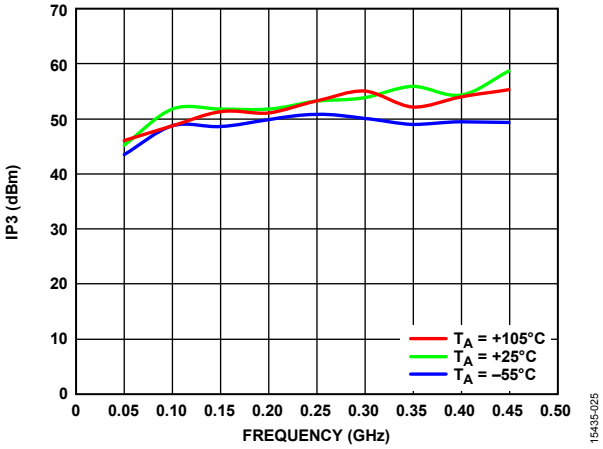


Figure 15. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 5 V (Low Frequency Detail)

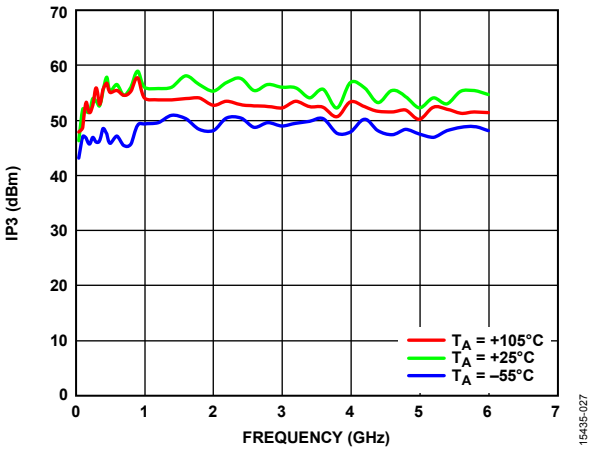


Figure 16. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V

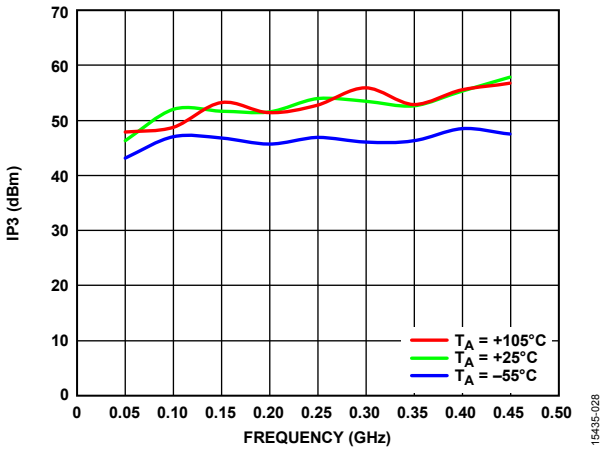
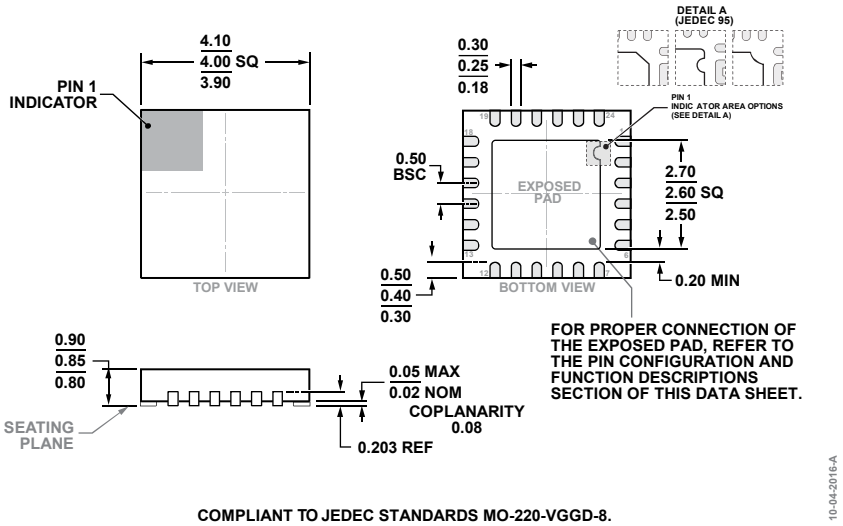


Figure 17. Input IP3 vs. Frequency at Minimum Attenuation State over Temperature, V_{DD} = 3 V (Low Frequency Detail)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 18. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(CP-24-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Branding[3]
HMC624ACPSZ-EP-PT	−55°C to +105°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-22	H624A XXXX
HMC624ACPSZ-EP-RL7	−55°C to +105°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-22	H624A XXXX

[1] The HMC624ACPSZ-EP-PT and HMC624ACPSZ-EP-RL7 are RoHS compliant parts.
[2] See the Absolute Maximum Ratings section.
[3] XXXX is the 4-digit lot number.

D15435-0-9/17(A)

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