RFMD + TriQuint = Qorvo

# TGA2975-SM

## *2.7 to 3.5GHz, 12W GaN Power Amplifier*

## Applications

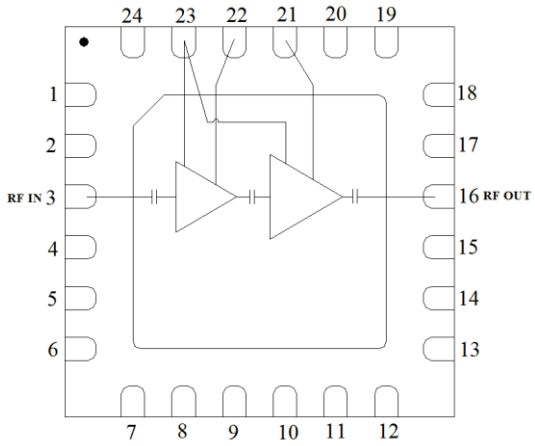
- Commercial and Military Radar


QFN 5x5 mm 24L

## Product Features

- Frequency Range: 2.7 - 3.5 GHz
- $P_{SAT}$: > 41 dBm at $P_{IN}$ = 16 dBm
- PAE: > 52 % at $P_{IN}$ = 16 dBm
- Small Signal Gain: 31 dB
- Return Loss: > 9 dB
- Bias: $V_D$ = 20 - 32 V, $I_{DQ}$ = 175 mA, $V_G$ = −2.7 V Typical
- Pulsed $V_D$: PW = 100 us, DC = 10 %
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

## Functional Block Diagram




## General Description

TriQuint's TGA2975-SM is a packaged MMIC power amplifier which operates from 2.7 to 3.5 GHz. The TGA2975-SM is designed using TriQuint's TQGaN25 0.25-µm GaN on SiC process.

The TGA2975-SM typically provides more than 41 dBm of saturated output power, 52% power-added efficiency, and 31 dB small signal gain. It can operate under both pulse and CW conditions.

The TGA2795-SM is available in a low-cost, surface mount 24 lead 5x5 Overmold QFN. It is ideally suited to support both commercial and defense related radar applications.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 ohms.

Lead-free and RoHS compliant

Evaluation Boards are available upon request.

## Pin Configuration

| Pad No. | Symbol |
|---|---|
| 1, 2, 4 – 15, 17 – 20, 24 | NC |
| 3 | RF IN |
| 16 | RF OUT |
| 21 | DRAIN 2 |
| 22 | DRAIN 1 |
| 23 | GATE |

## Ordering Information

| Part | ECCN | Description |
|---|---|---|
| TGA2975-SM | EAR99 | 2.7 - 3.5 GHz, 12 W GaN Power Amplifier |
| TGA2975-SM_EVB | EAR99 | TGA2975-SM Evaluation Board |

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain Voltage ($V_D$) | 40 V |
| Gate Voltage Range ($V_G$) | −8 to 0 V |
| Drain Current ($I_{D1}$) | 225 mA |
| Drain Current ($I_{D2}$) | 1250 mA |
| Gate Current ($I_G$) | See Graph (page 3) |
| Power Dissipation ($P_{DISS}$), 85°C | 27 W |
| Input Power ($P_{IN}$), CW, 50 Ω, 85°C | 30 dBm |
| Input Power ($P_{IN}$), CW, VSWR 10:1, $V_D$ = 28 V, 85°C | 23 dBm |
| Channel Temperature ($T_{CH}$) | 275°C |
| Mounting Temperature (30 Seconds) | 260°C |
| Storage Temperature | −55 to 150°C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

## Recommended Operating Conditions

| Parameter | Value |
|---|---|
| Drain Voltage ($V_D$) | 20 – 32 V |
| Drain Current ($I_{DQ}$) | 125 – 225 mA |
| Drain Current Under RF Drive ($I_{D\_DRIVE}$) | See plots p. 8 |
| Gate Voltage ($V_G$) | −2.7 V (Typ.) |
| Gate Current Under RF Drive ($I_{G\_DRIVE}$) | See plots p. 8 |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted: 25 °C, $V_D$ = 28 V, $I_{DQ}$ = 175 mA, $V_G$ = −2.7 V Typ, Pulsed $V_D$: PW = 100 us, DC = 10 %

| Parameter | Min | Typical | Max | Units |
|---|---|---|---|---|
| Operational Frequency Range | 2.7 | | 3.5 | GHz |
| Small Signal Gain | | 31 | | dB |
| Input Return Loss | | > 15 | | dB |
| Output Return Loss | | > 9 | | dB |
| Output Power at Saturation ($P_{IN}$ = 16 dBm) | | > 41 | | dBm |
| Power-Added Efficiency ($P_{IN}$ = 16 dBm) | | > 52 | | % |
| Gain Temperature Coefficient | | -0.05 | | dB/°C |
| Power Temperature Coefficient | | -0.007 | | dBm/°C |

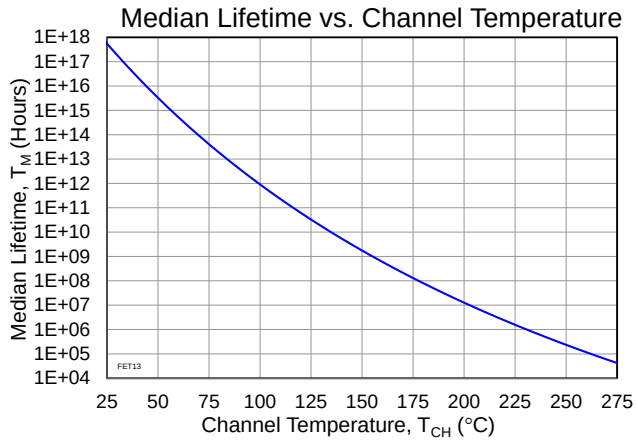
## Thermal and Reliability Information

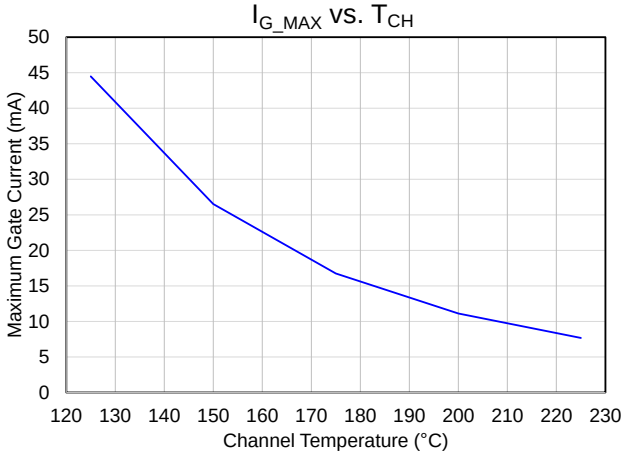
| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85°C, $V_D$ = 28 V, $I_{DQ}$ = 175 mA (Quiescent DC, CW) $P_{DISS}$ = 4.9 W | 3.9 | °C/W |
| Channel Temperature ($T_{CH}$) | | 104 | °C |
| Median Lifetime ($T_M$) | | 5.19E+11 | Hrs |
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85°C, $V_D$ = 28 V, $I_{D\ Drive}$ = 805 mA (PW = 100 µs, DC = 10%) Freq. = 3.3 GHz: $P_{IN}$ = 16 dBm, $P_{OUT}$ = 40.5 dBm, $P_{DISS}$ = 11 W | 3.14 | °C/W |
| Channel Temperature ($T_{CH}$) (Under RF drive) | | 120 | °C |
| Median Lifetime ($T_M$) | | 6.17E+11 | Hrs |

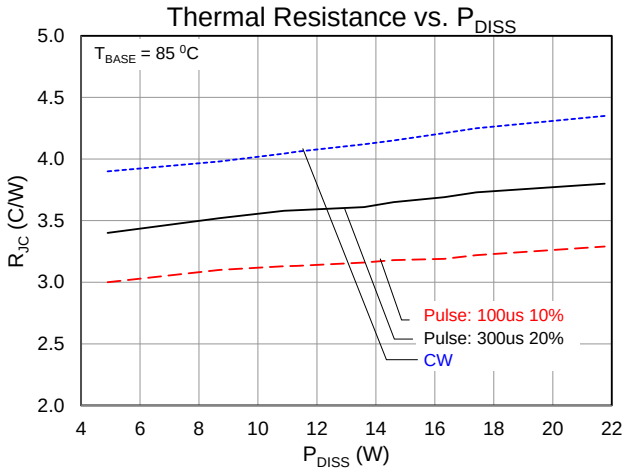
Notes:
1. Thermal resistance measured to back of package.

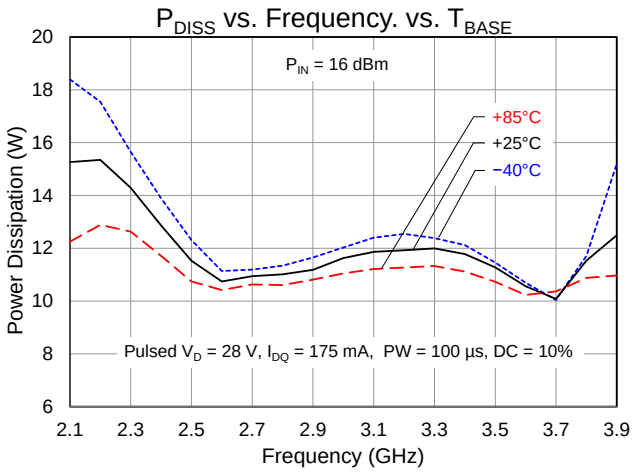
## Median Lifetime, Power Dissipation and Max. Gate Current

Test conditions: $V_D$ = 40V; Failure Criteria = 10% reduction in $I_{D\_MAX}$



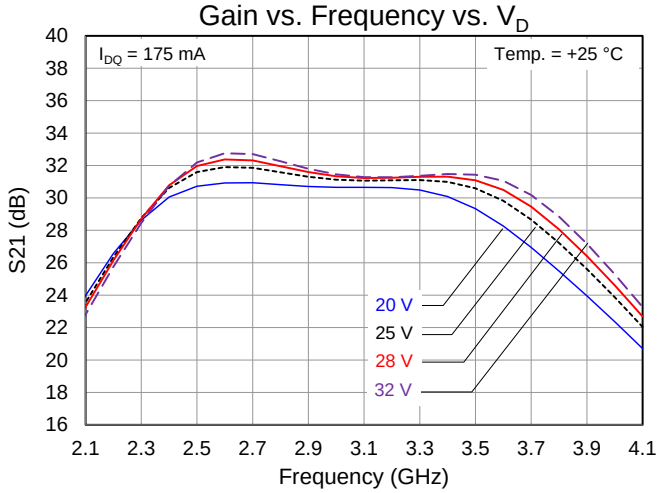



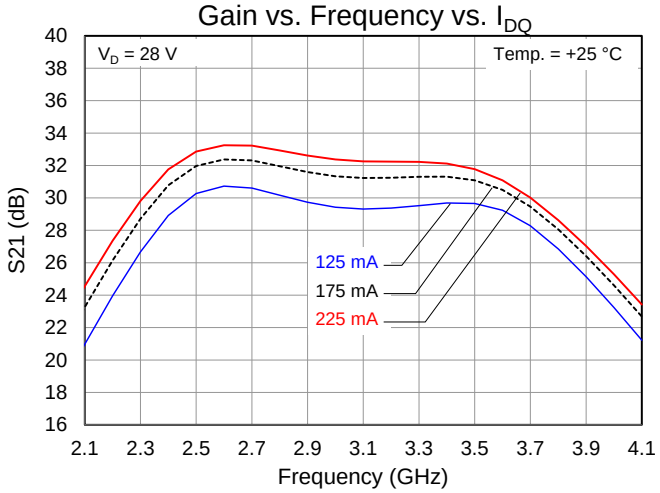
## Typical Performance: Small Signal

Condition: CW

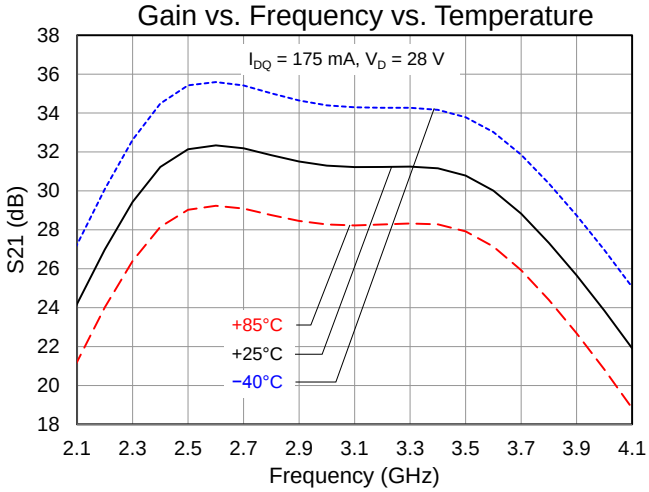
Gain vs. Frequency vs. $V_D$



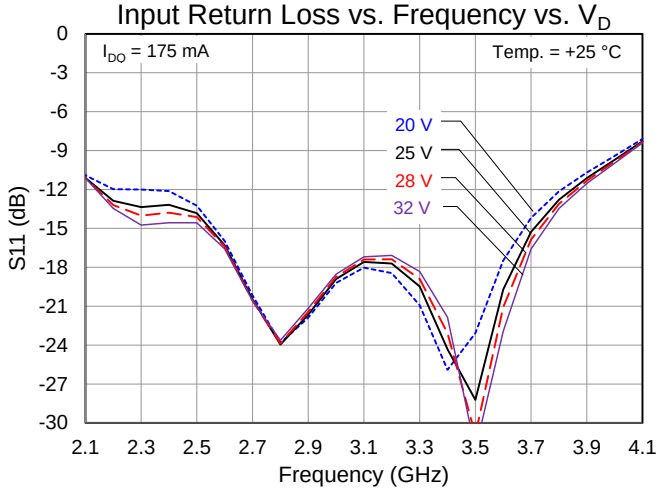

Gain vs. Frequency vs. $I_{DQ}$



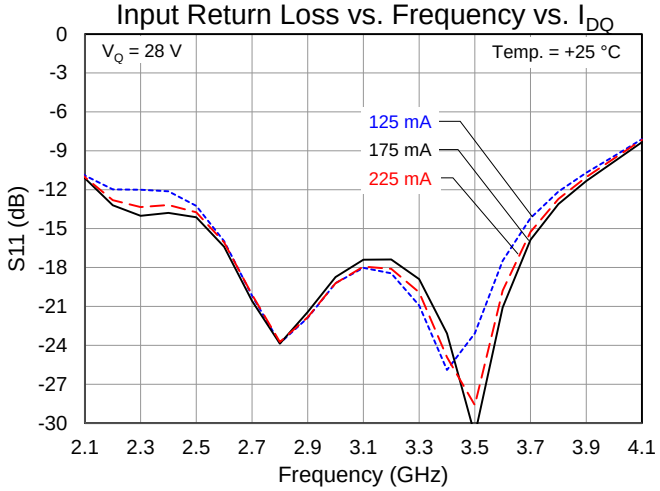

Gain vs. Frequency vs. Temperature




Input Return Loss vs. Frequency vs. $V_D$



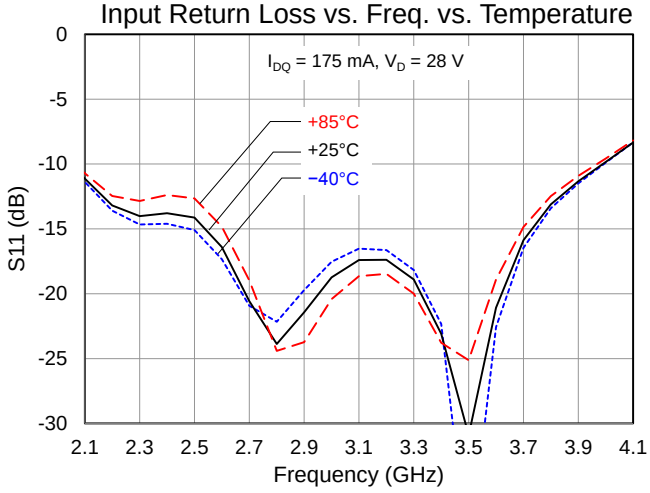

Input Return Loss vs. Frequency vs. $I_{DQ}$



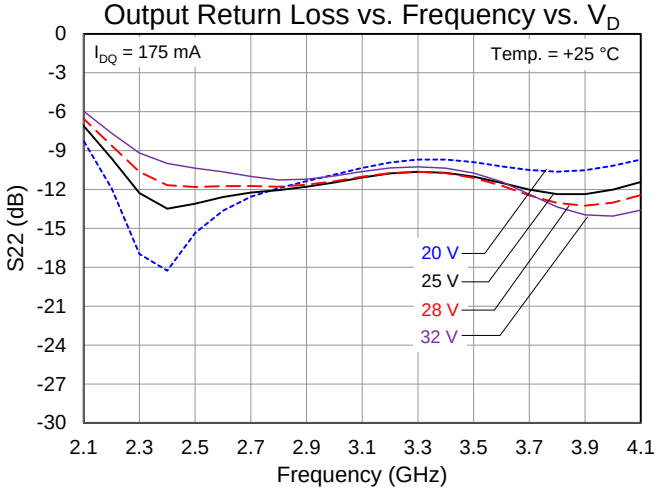
## Typical Performance: Small Signal

Condition: CW

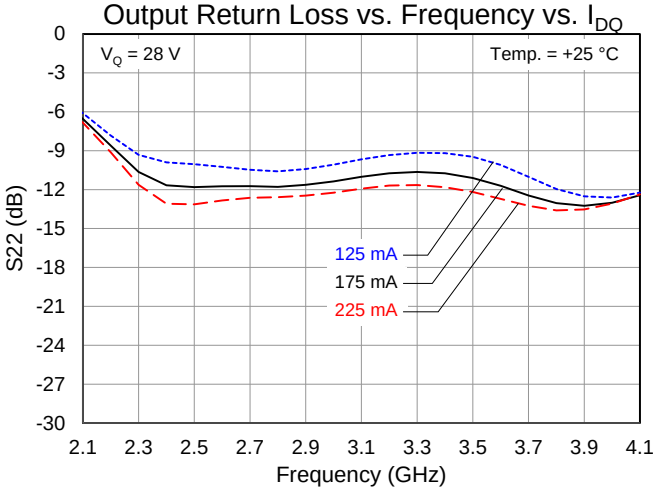
Input Return Loss vs. Freq. vs. Temperature



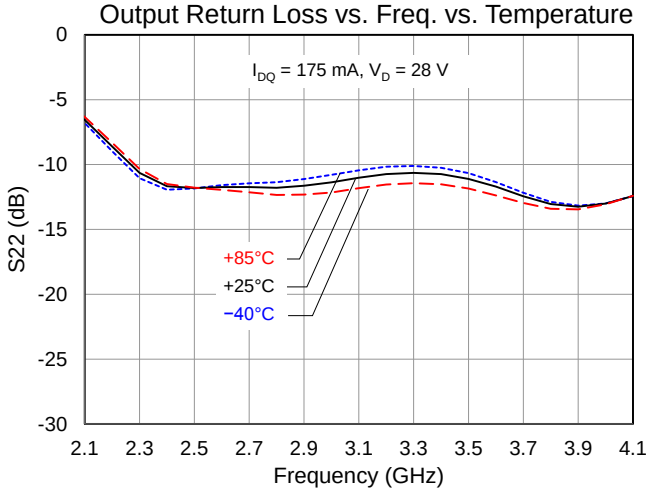

Output Return Loss vs. Frequency vs. $V_D$




Output Return Loss vs. Frequency vs. $I_{DQ}$



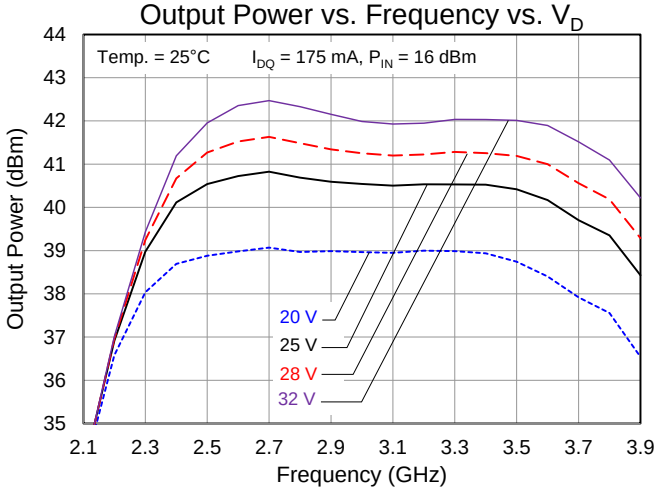

Output Return Loss vs. Freq. vs. Temperature



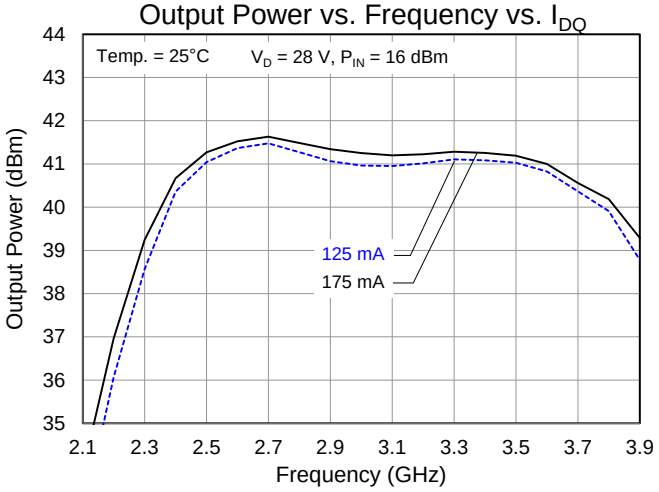
## Typical Performance: Large Signal

Condition: Pulsed $V_D$, Pulse Width = 100 us, Duty Cycle = 10%

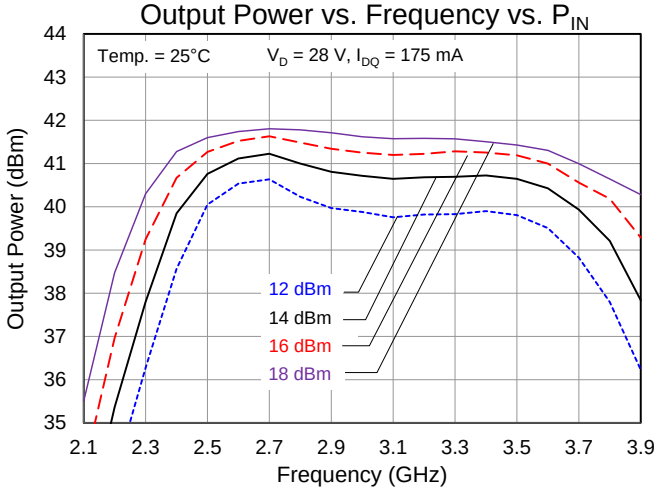
Output Power vs. Frequency vs. $V_D$



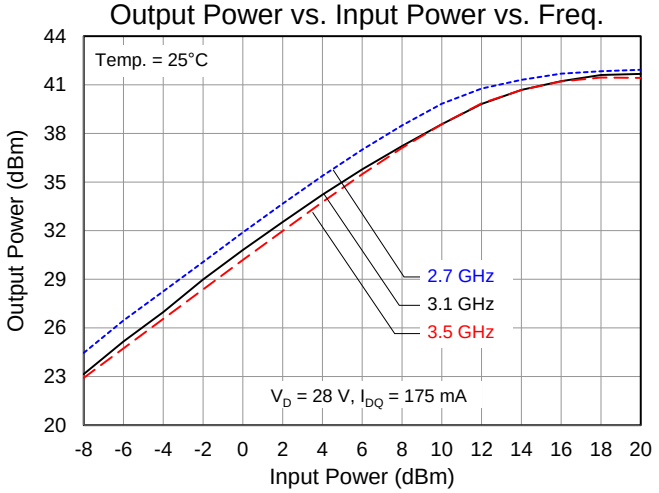

Output Power vs. Frequency vs. $I_{DQ}$



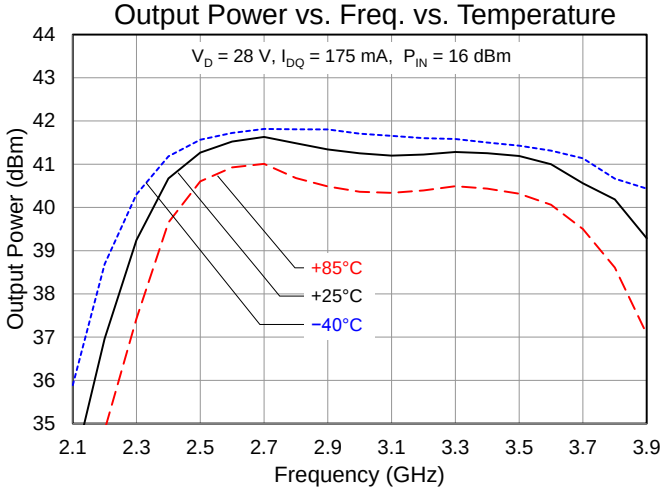

Output Power vs. Frequency vs. $P_{IN}$



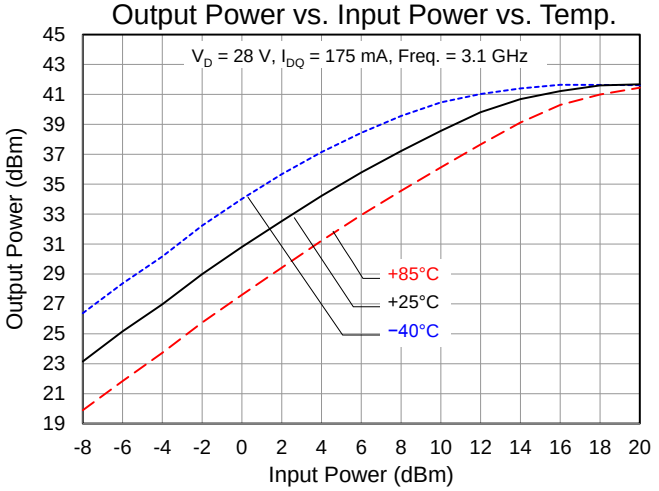

Output Power vs. Input Power vs. Freq.




Output Power vs. Freq. vs. Temperature



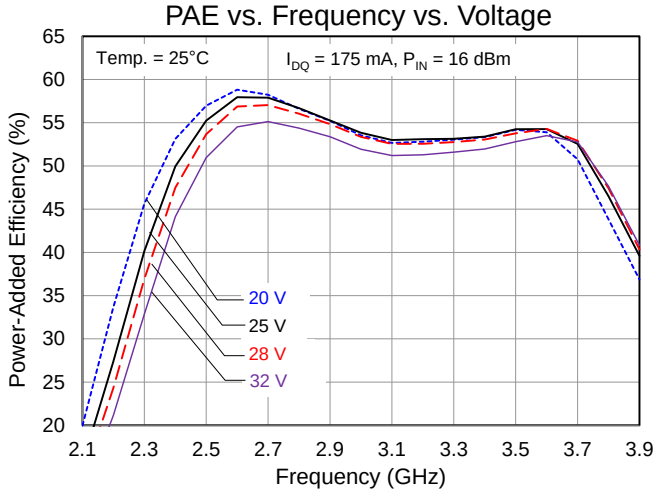

Output Power vs. Input Power vs. Temp.



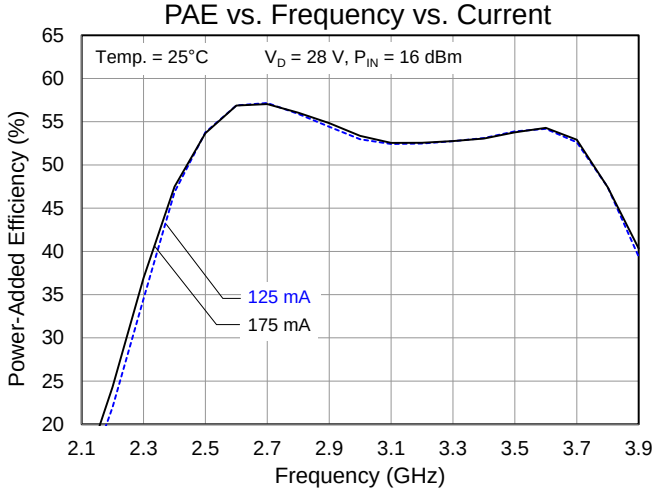
## Typical Performance: Large Signal

Condition: Pulsed $V_D$, Pulse Width = 100 us, Duty Cycle = 10%

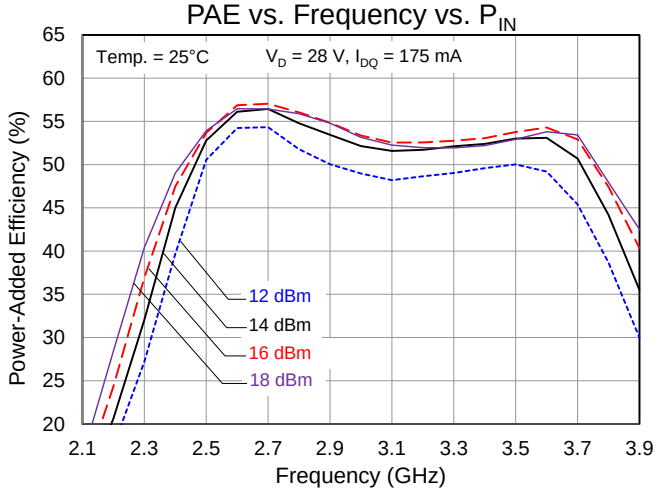
PAE vs. Frequency vs. Voltage



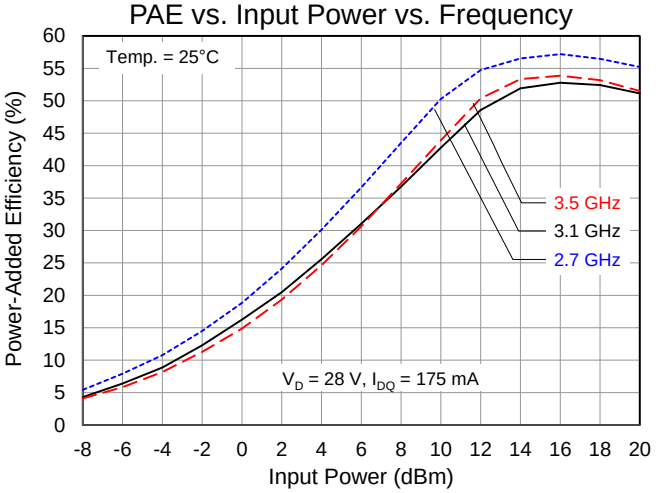

PAE vs. Frequency vs. Current



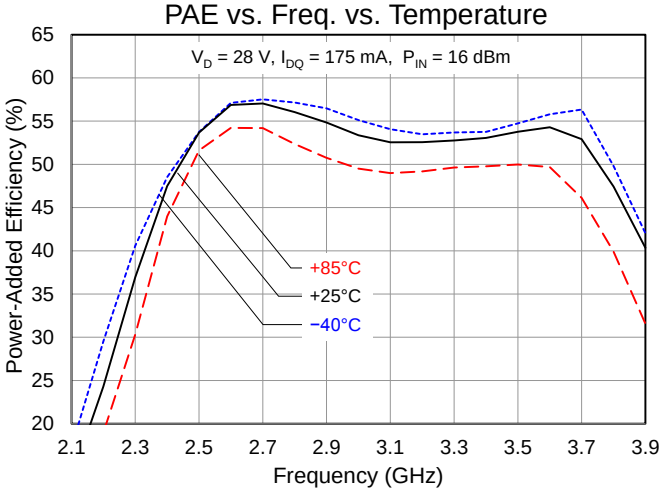

PAE vs. Frequency vs. $P_{IN}$



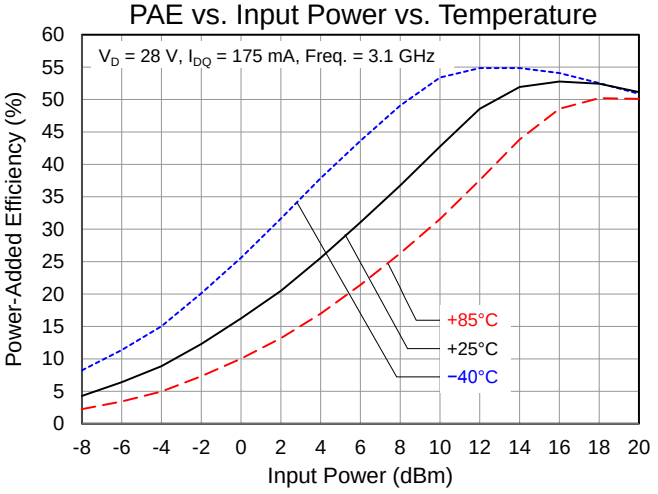

PAE vs. Input Power vs. Frequency




PAE vs. Freq. vs. Temperature



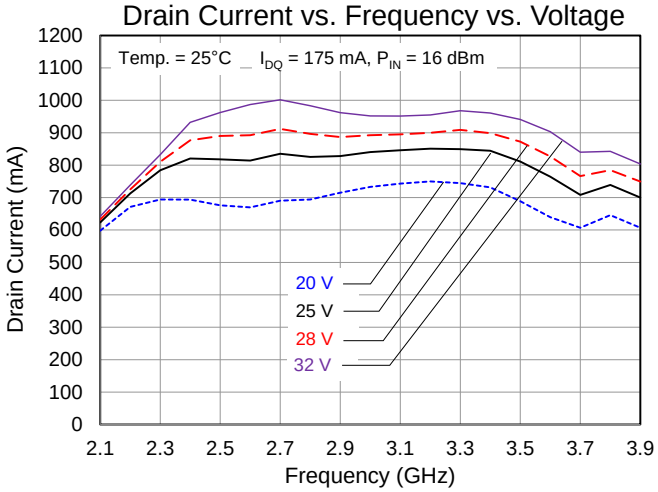

PAE vs. Input Power vs. Temperature



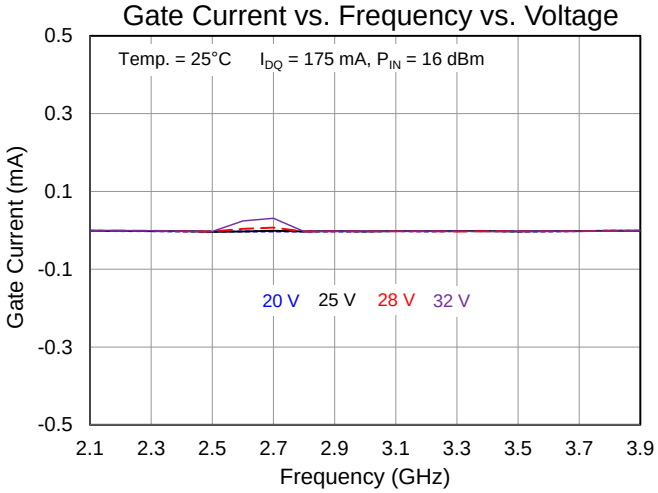
## Typical Performance: Large Signal

Condition: Pulsed $V_D$, Pulse Width = 100 us, Duty Cycle = 10%

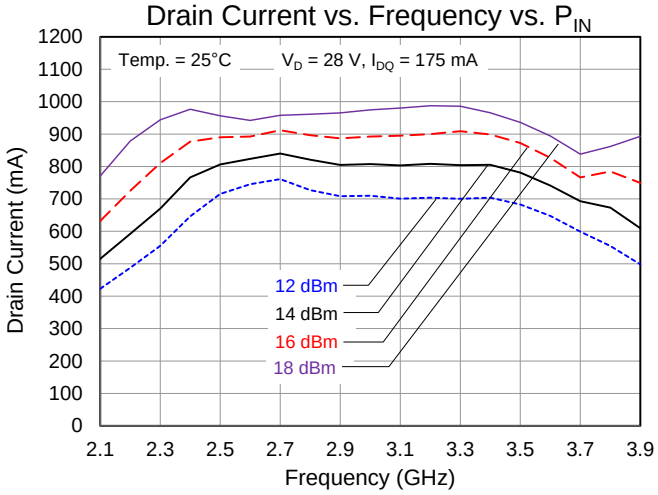
Drain Current vs. Frequency vs. Voltage



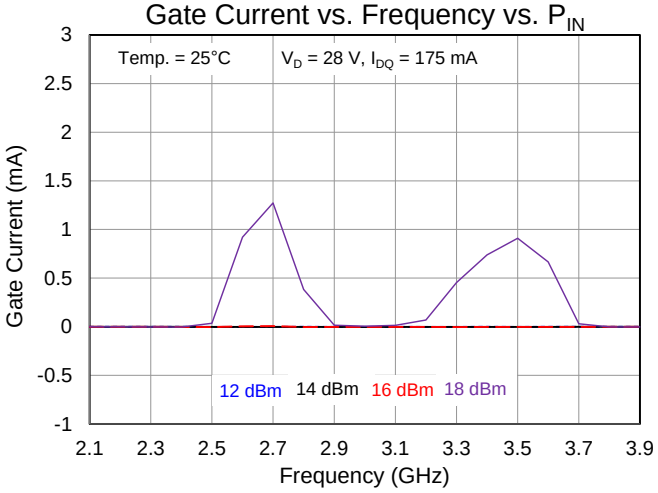

Gate Current vs. Frequency vs. Voltage



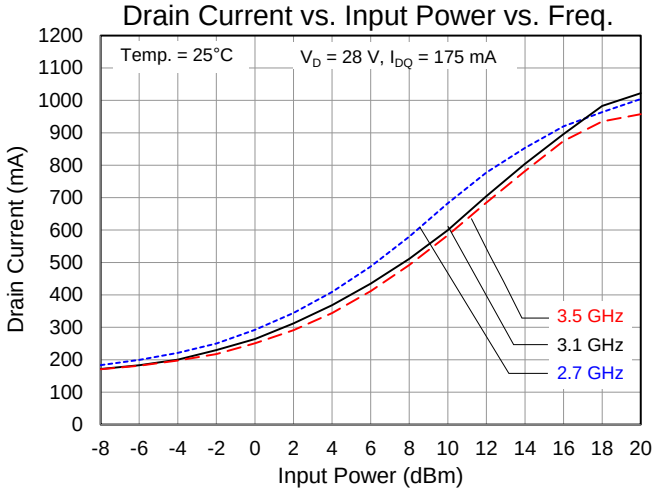

Drain Current vs. Frequency vs. $P_{IN}$



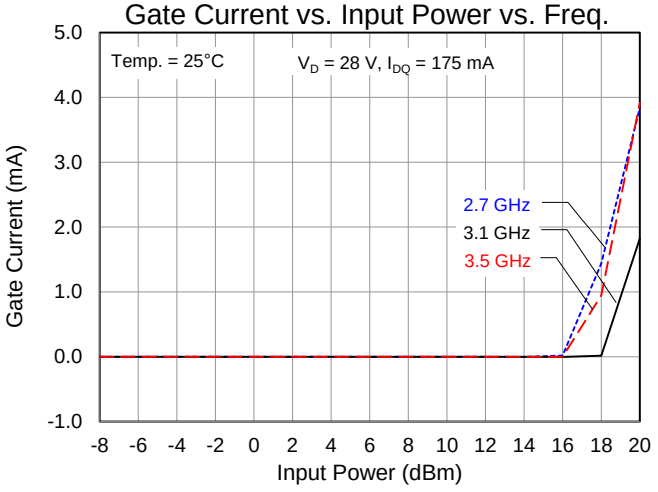

Gate Current vs. Frequency vs. $P_{IN}$




Drain Current vs. Input Power vs. Freq.



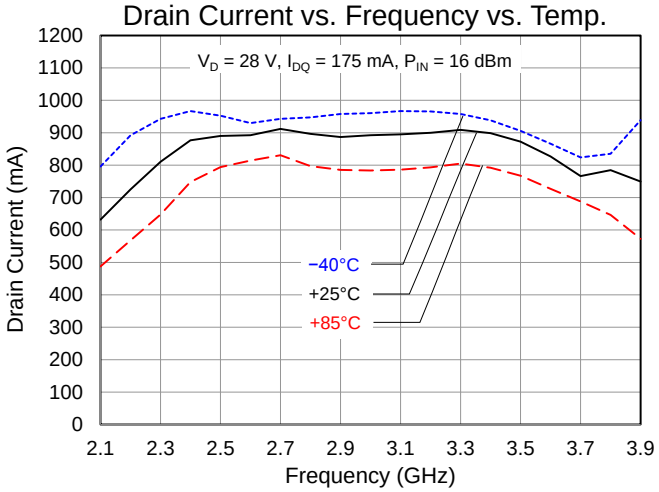

Gate Current vs. Input Power vs. Freq.



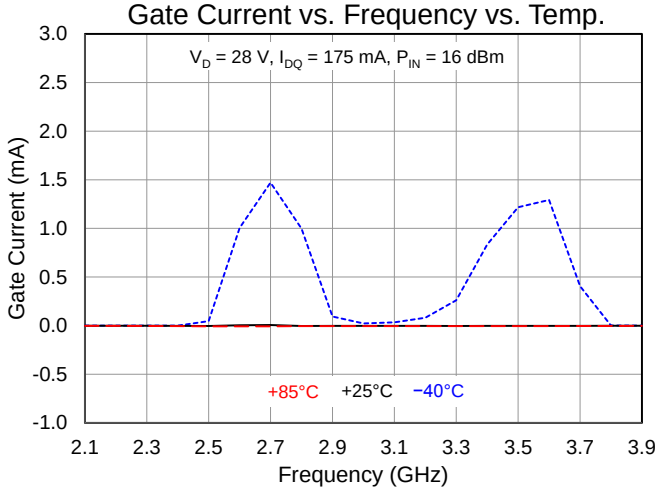
## Typical Performance: Large Signal

Condition: Pulsed $V_D$, Pulse Width = 100 us, Duty Cycle = 10%

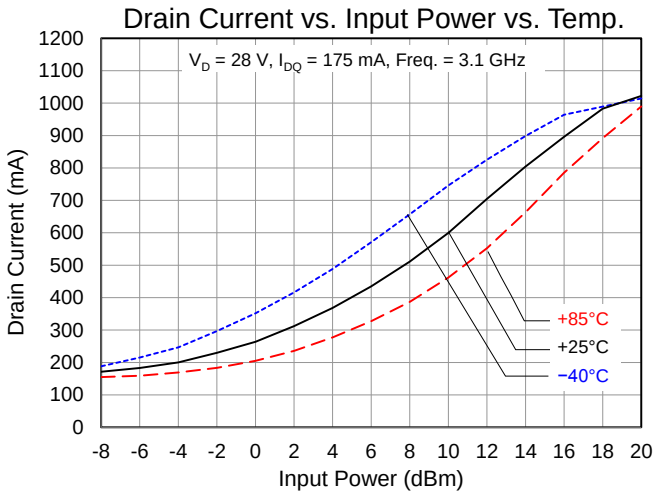
Drain Current vs. Frequency vs. Temp.



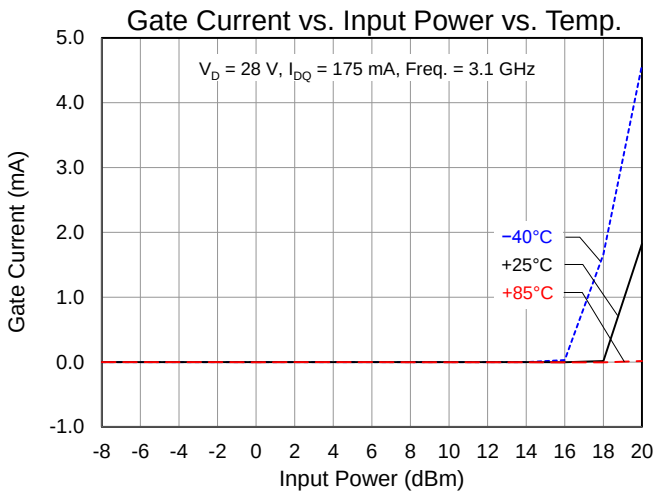

Gate Current vs. Frequency vs. Temp.



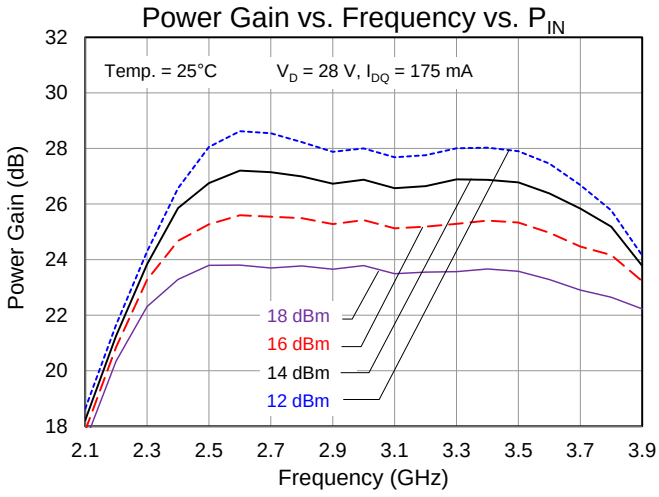

Drain Current vs. Input Power vs. Temp.



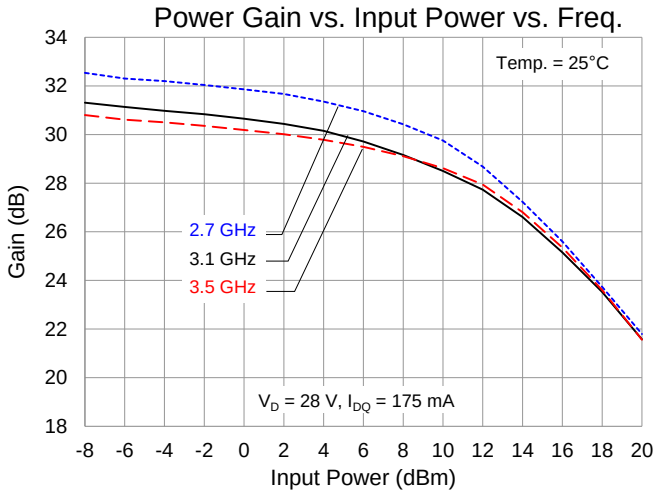

Gate Current vs. Input Power vs. Temp.




Power Gain vs. Frequency vs. $P_{IN}$



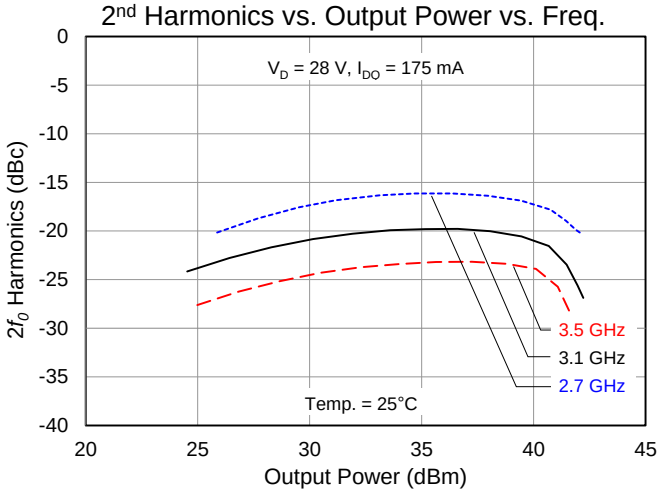

Power Gain vs. Input Power vs. Freq.



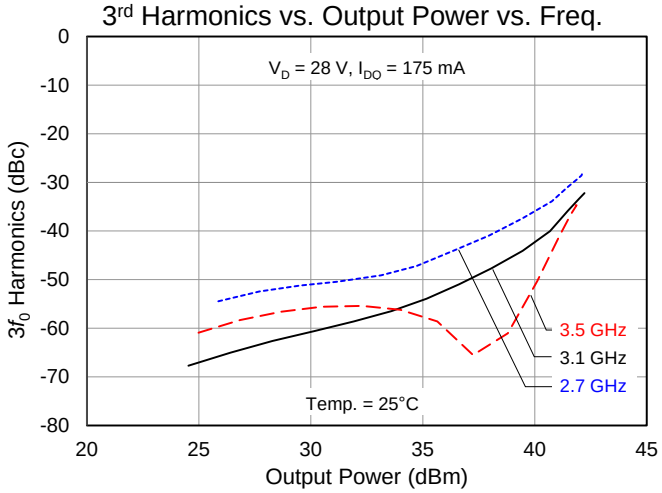
## Typical Performance: Large Signal and Linearity

Condition: CW

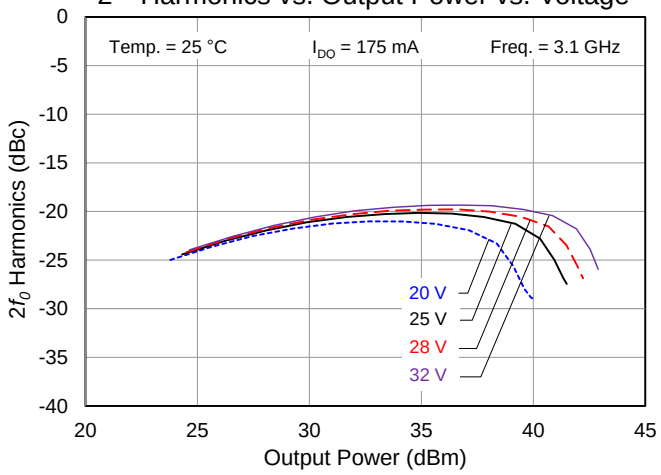
2nd Harmonics vs. Output Power vs. Freq.



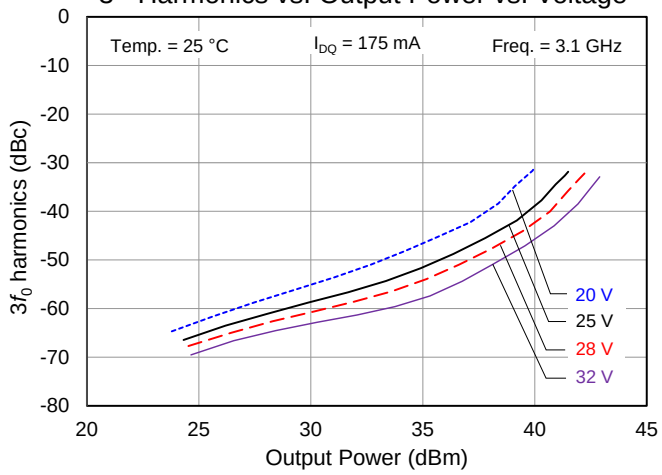

3rd Harmonics vs. Output Power vs. Freq.



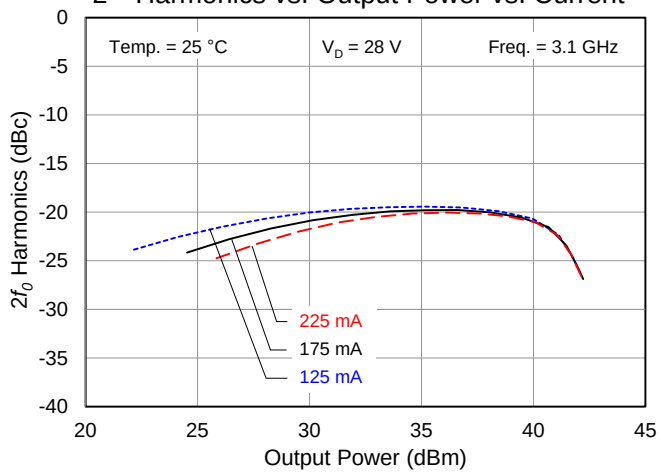

2nd Harmonics vs. Output Power vs. Voltage



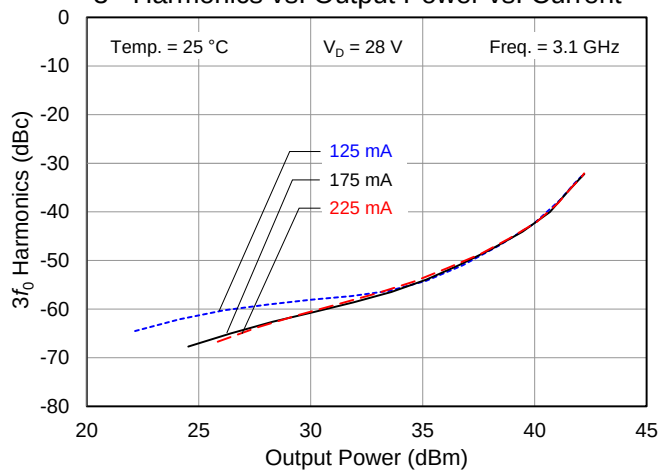

3rd Harmonics vs. Output Power vs. Voltage




2nd Harmonics vs. Output Power vs. Current



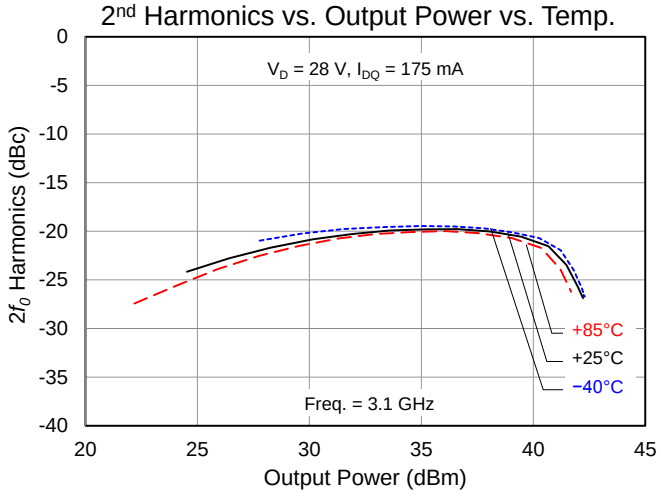

3rd Harmonics vs. Output Power vs. Current



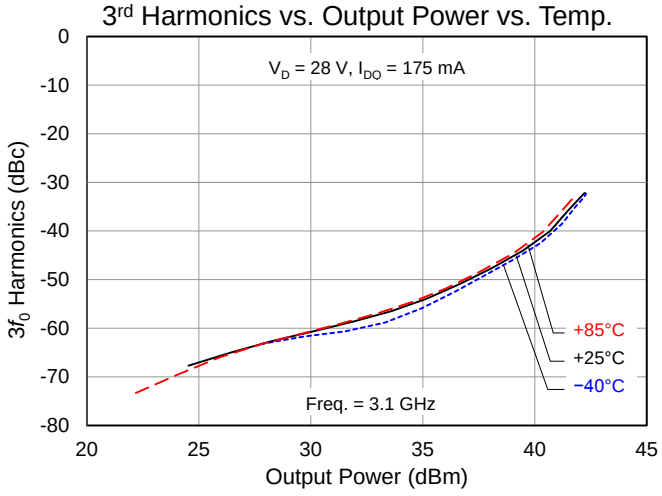
## Typical Performance: Large Signal & Linearity

Condition: CW

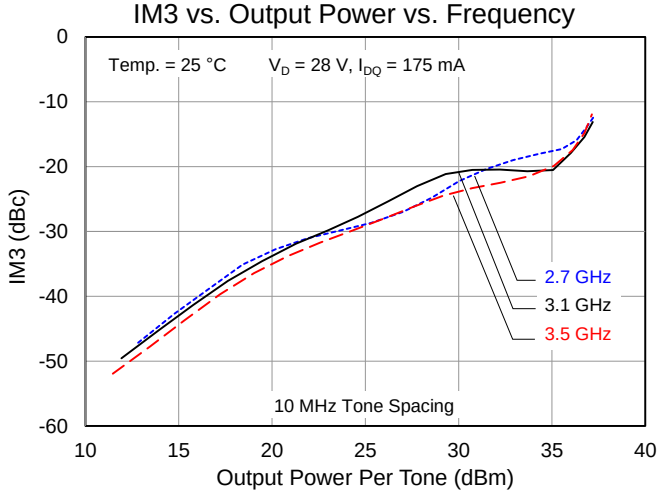
2nd Harmonics vs. Output Power vs. Temp.



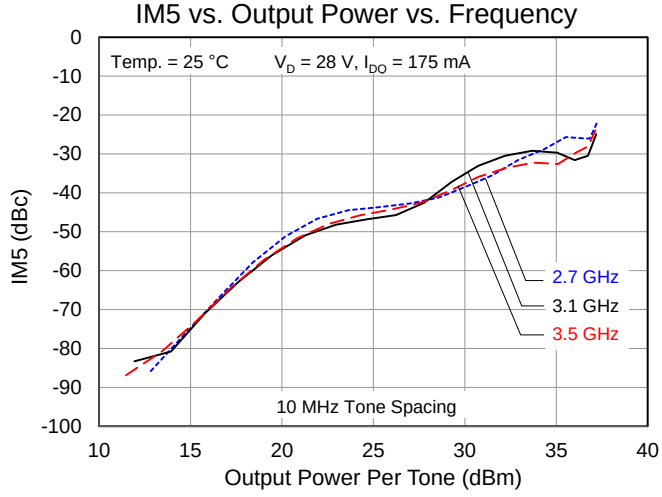

3rd Harmonics vs. Output Power vs. Temp.



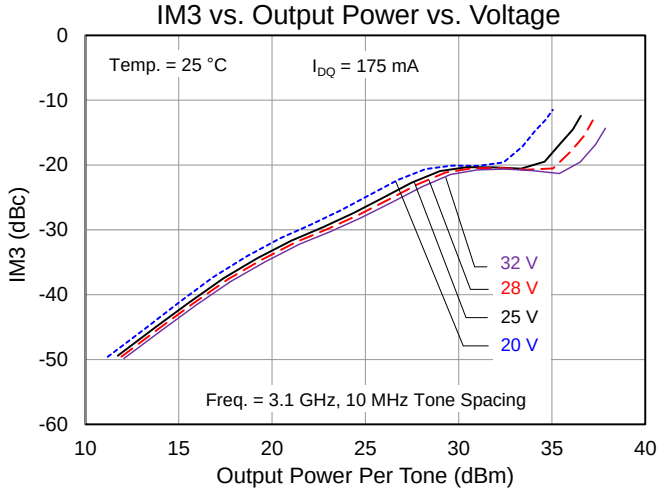

IM3 vs. Output Power vs. Frequency



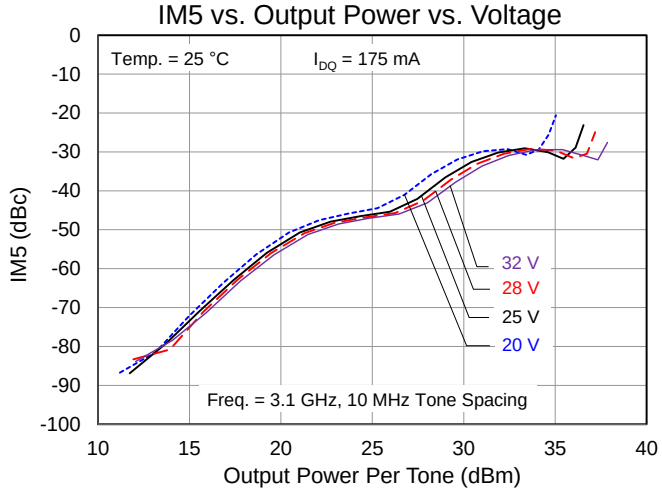

IM5 vs. Output Power vs. Frequency




IM3 vs. Output Power vs. Voltage



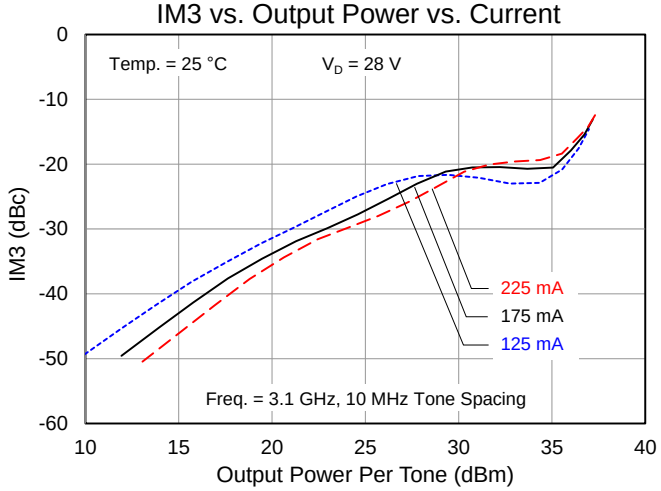

IM5 vs. Output Power vs. Voltage



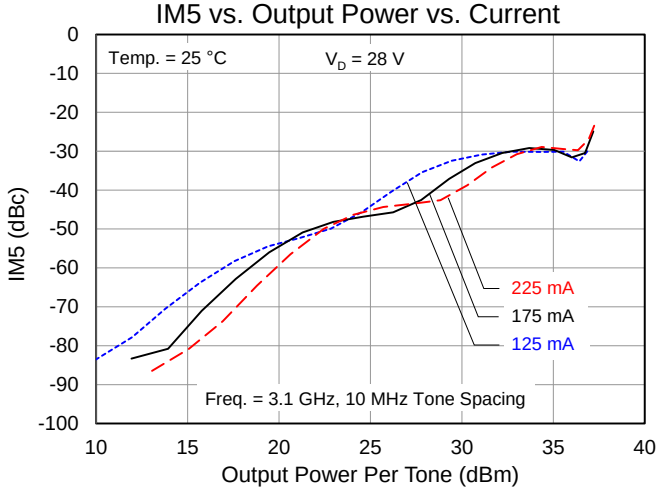
## Typical Performance: Large Signal & Linearity

Condition: CW

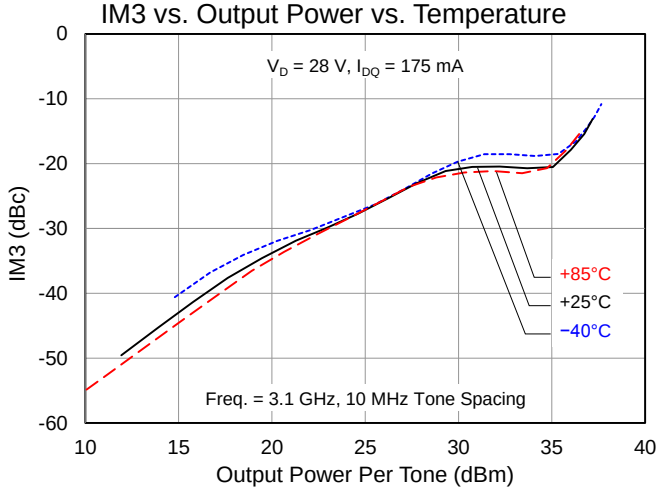
IM3 vs. Output Power vs. Current



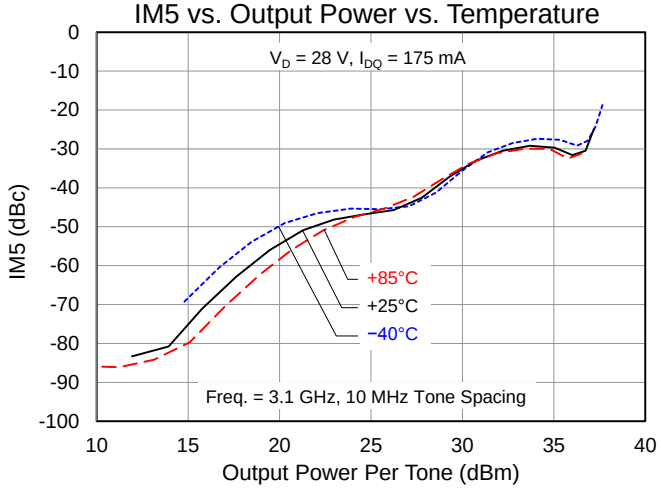

IM5 vs. Output Power vs. Current



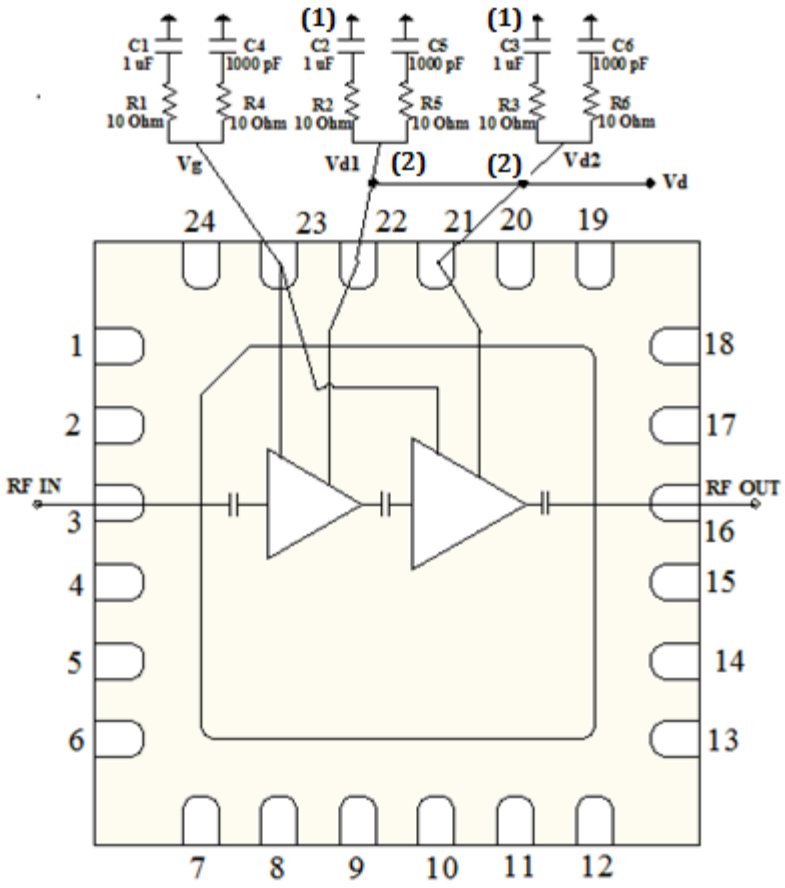

IM3 vs. Output Power vs. Temperature




IM5 vs. Output Power vs. Temperature



## Applications Information




Notes:

1. Remove if pulsing on drain
2. $V_D$: Tied $V_{D1}$ & $V_{D2}$ together

## Bias-up Procedure

| |
|---|
| 1. Set $I_D$ limit to 1.3 A, $I_G$ limit to 8 mA |
| 2. Apply −5 V to $V_G$ |
| 3. Apply +28 V to $V_D$; ensure $I_{DQ}$ is approx. 0 mA |
| 4. Adjust $V_G$ until $I_{DQ}$ = 175 mA ($V_G$ ~ −2.7 V Typ.). |
| 5. Turn on RF supply |

## Bias-down Procedure

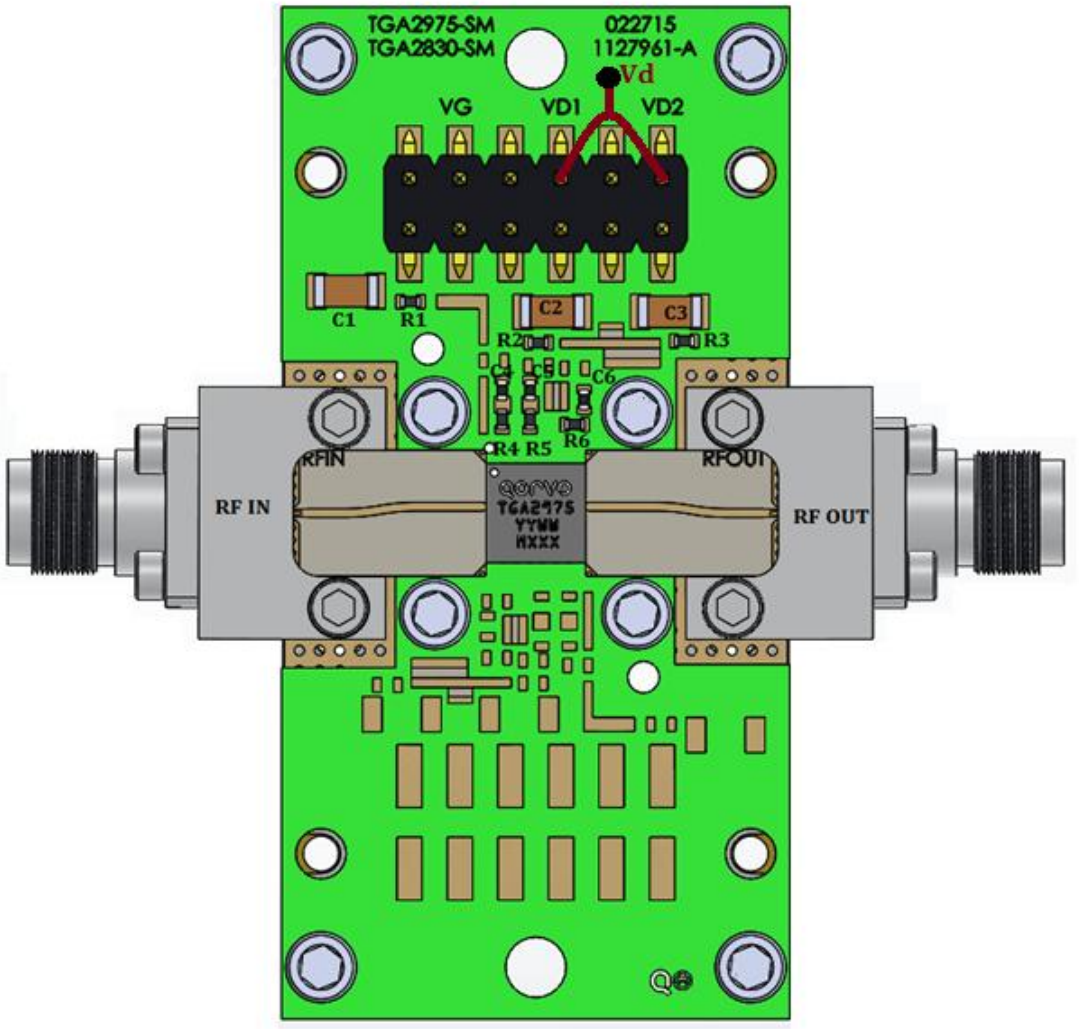
| |
|---|
| 1. Turn off RF supply |
| 2. Reduce $V_G$ to −5 V; ensure $I_{DQ}$ is approx. 0 mA |
| 3. Set $V_D$ to 0 V |
| 4. Turn off $V_D$ supply |
| 5. Turn off $V_G$ supply |

## Pin Layout


## Pin Description

| Pin No. | Symbol | Description |
|---|---|---|
| 1, 2, 4 – 15, 17 – 20, 24 | NC | No internal connection; can be grounded on PCB or left open |
| 3 | RF IN | Input; matched to 50 Ω; DC blocked |
| 16 | RF OUT | Output; matched to 50 Ω; DC blocked |
| 21 | DRAIN 2 | Drain voltage; bias network is required; see recommended Application Information on page 13 |
| 22 | DRAIN 1 | Drain voltage; bias network is required; see recommended Application Information on page 13 |
| 23 | GATE | Gate voltage; bias network is required; see recommended Application Information on page 13 |
| 25 | GND | Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance. |

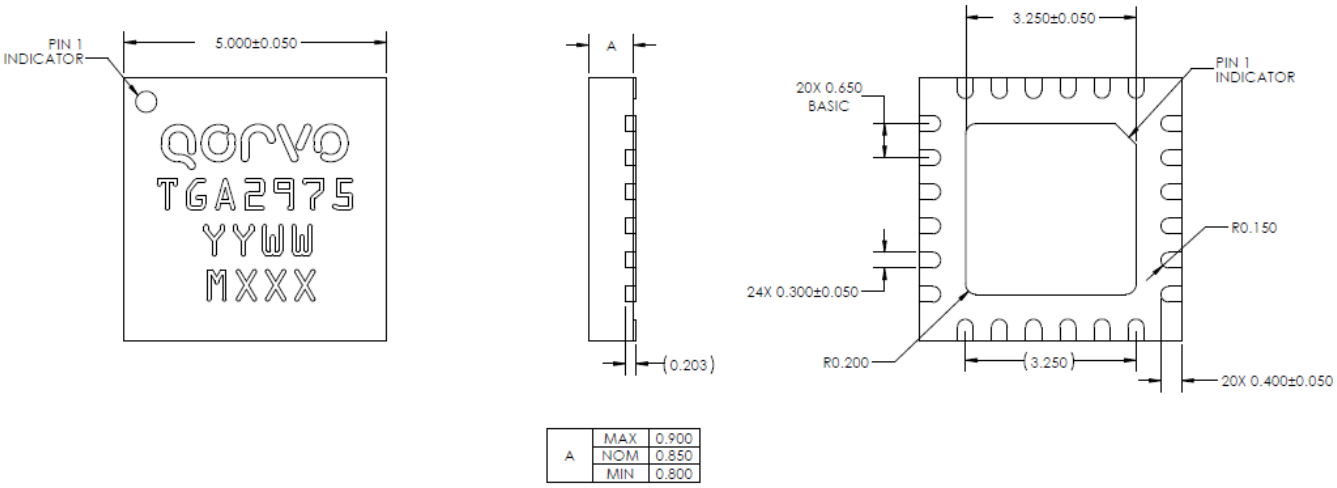
## Evaluation Board




## Bill of Material

| Reference Des. | Value | Description | Manuf. | Part Number |
|---|---|---|---|---|
| C1 – C3 | 1 µF | Cap, 1206, 50 V, 5%, X7R | Various | |
| C4 – C6 | 1000 pF | Cap, 0402, 100 V, 10%, X7R | Various | |
| R1 – R6 | 10 Ω | Res, 0402, 5% | Various | |

## Mechanical Information




| | | |
|---|---|---|
| A | MAX | 0.900 |
| | NOM | 0.850 |
| | MIN | 0.800 |

Units: millimeter (mm)

Tolerances: unless specified

x.xx = ± 0.01

x.xxx = ± 0.005

Materials:

Package Leads are Gold Plated.

Part is Mold Encapsulated.

Marking:

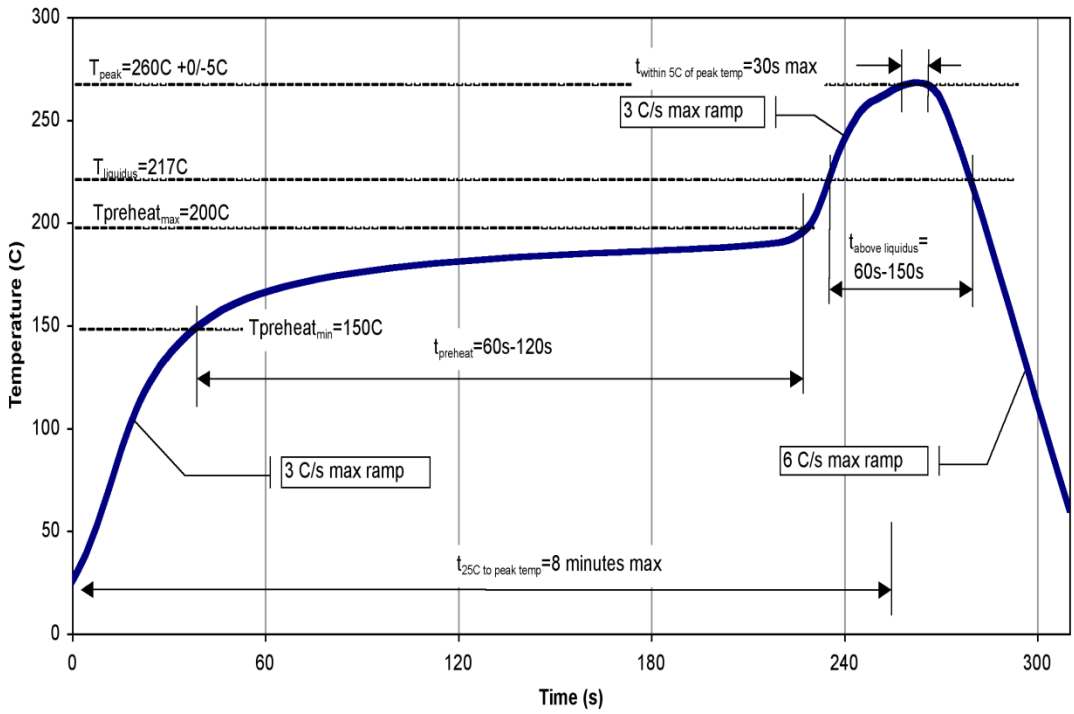
2975: Part number

YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

## Recommended Soldering Temperature Profile



# Product Compliance Information

## ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

## MSL Rating

Level TBD at TBD°C convection reflow
The part is rated Moisture Sensitivity Level TBD at TBD°C per JEDEC standard IPC/JEDEC J-STD-020.

## ECCN

US Department of Commerce: EAR99

## Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260°C

## RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

# Contact Information

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