

Applications

- Commercial and Military Radar

Product Features

- Frequency Range: 2.7 - 3.5 GHz
- P_{SAT} : > 42.5 dBm at P_{IN} = 18 dBm
- PAE: > 54 % at P_{IN} = 18 dBm
- Small Signal Gain: > 30.5 dB
- Return Loss: > 11 dB
- Bias: V_D = 20 - 32 V, I_{DO} = 225 mA, V_G = -2.9 V Typical
- Pulsed V_D : PW = 100 μ s, DC = 10 %
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

General Description

TriQuint's TGA2830-SM is a packaged MMIC power amplifier which operates from 2.7 to 3.5 GHz. The TGA2830-SM is designed using TriQuint's TQGaN25 0.25- μ m GaN on SiC process.

The TGA2830-SM typically provides more than 42.5 dBm of saturated output power, 54% power-added efficiency, and 30.5 dB small signal gain. It can operate under both pulse and CW conditions.

The TGA2830-SM is available in a low-cost, surface mount 24 lead 5x5 Overmold QFN. It is ideally suited to support both commercial and defense related radar applications.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 ohms.

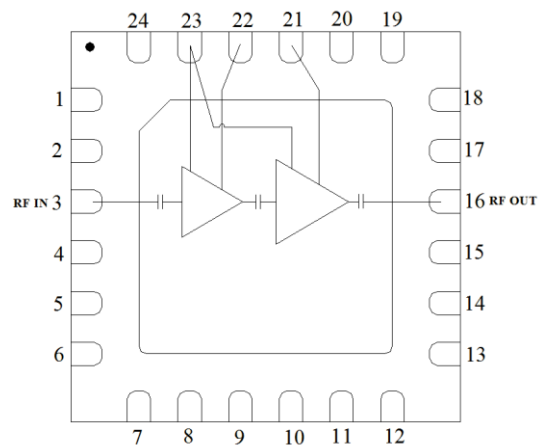
Lead-free and RoHS compliant

Evaluation Boards are available upon request.



QFN 5x5 mm 24L

Functional Block Diagram



Pin Configuration

Pad No.	Symbol
1, 2, 4-15, 17-20, 24	NC
3	RF IN
16	RF OUT
21	DRAIN 2
22	DRAIN 1
23	GATE

Ordering Information

Part	ECCN	Description
TGA2830-SM	EAR99	2.7 - 3.5 GHz, 18 W GaN Power Amplifier
TGA2830-SM_EVB	EAR99	TGA2830-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_{D1})	225 mA
Drain Current (I_{D2})	1250 mA
Gate Current (I_G)	See Graph (page 3)
Power Dissipation (P_{DISS}), 85°C	35 W
Input Power (P_{IN}), CW, 50 Ω , 85°C	30 dBm
Input Power (P_{IN}), CW, VSWR 10:1, $V_D = 28$ V, 85°C	23 dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	260°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	20 – 32 V
Drain Current (I_{DQ})	175 – 275 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 8
Gate Voltage (V_G)	-2.9 V (Typ.)
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 8

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, $V_D = 28$ V, $I_{DQ} = 225$ mA, $V_G = -2.9$ V Typ, Pulsed V_D : PW = 100 μ s, DC = 10 %

Parameter	Min	Typical	Max	Units
Operational Frequency Range	2.7		3.5	GHz
Small Signal Gain		> 30.5		dB
Input Return Loss		> 15		dB
Output Return Loss		> 11		dB
Output Power at Saturation ($P_{IN} = 18$ dBm)		> 42.5		dBm
Power-Added Efficiency ($P_{IN} = 18$ dBm)		> 54		%
Gain Temperature Coefficient		-0.05		dB/°C
Power Temperature Coefficient		-0.004		dBm/°C

Thermal and Reliability Information

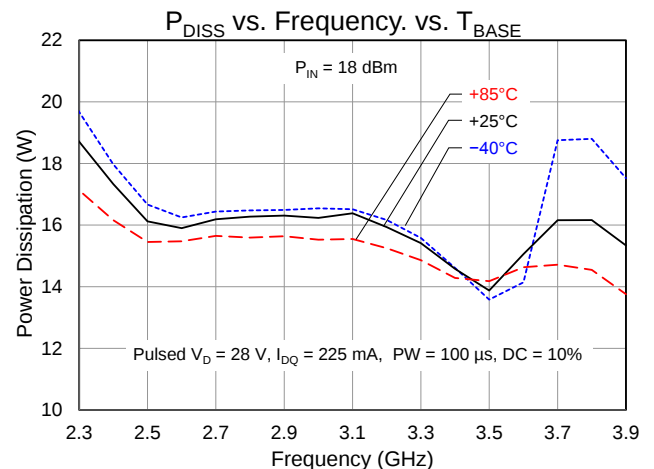
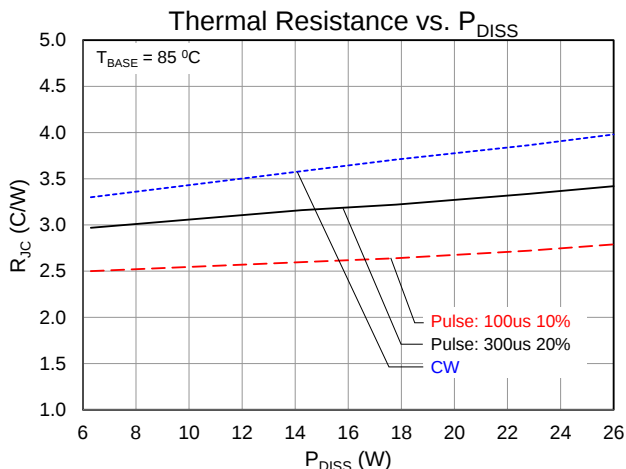
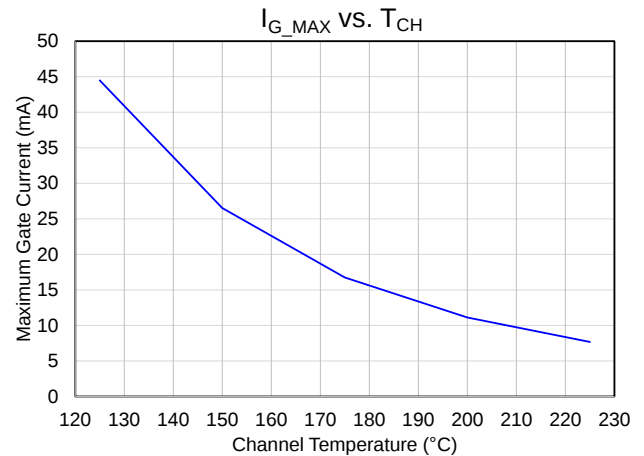
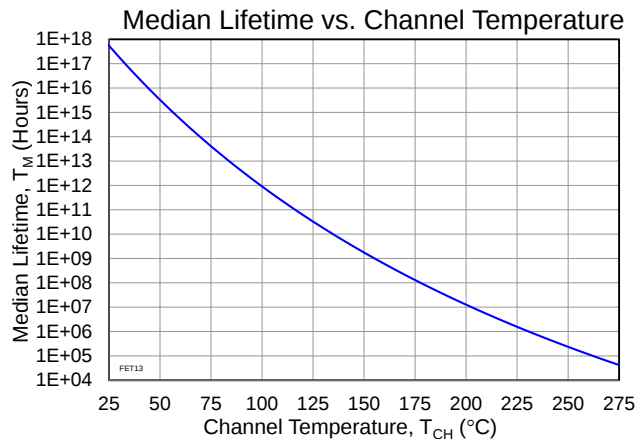
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DO} = 225\text{ mA}$ (Quiescent DC, CW) $P_{DISS} = 6.3\text{ W}$	3.3	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		106	$^{\circ}\text{C}$
Median Lifetime (T_M)		3.94E+11	Hrs
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{D Drive} = 1185\text{ mA}$ (PW = 100 μs , DC = 10%) Freq. = 3.1 GHz: $P_{IN} = 18\text{ dBm}$, $P_{OUT} = 42.5\text{ dBm}$, $P_{DISS} = 15\text{ W}$	2.61	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH}) (Under RF drive)		125	$^{\circ}\text{C}$
Median Lifetime (T_M)		3.28E+11	Hrs

Notes:

1. Thermal resistance measured to back of package.

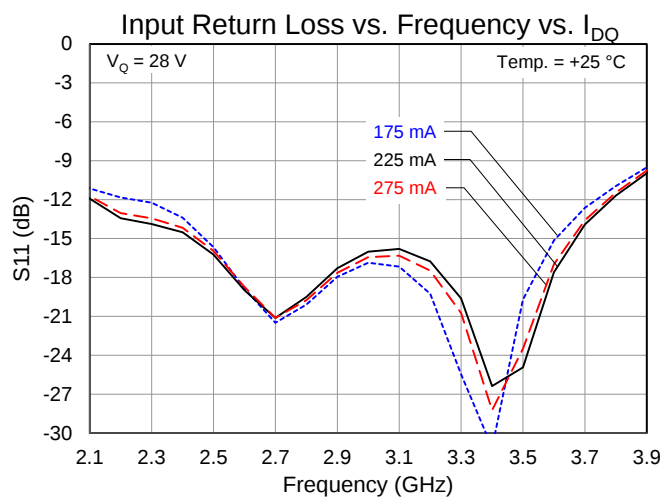
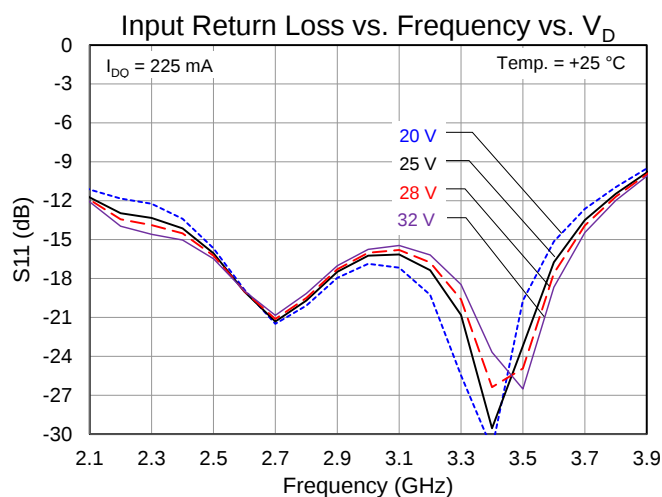
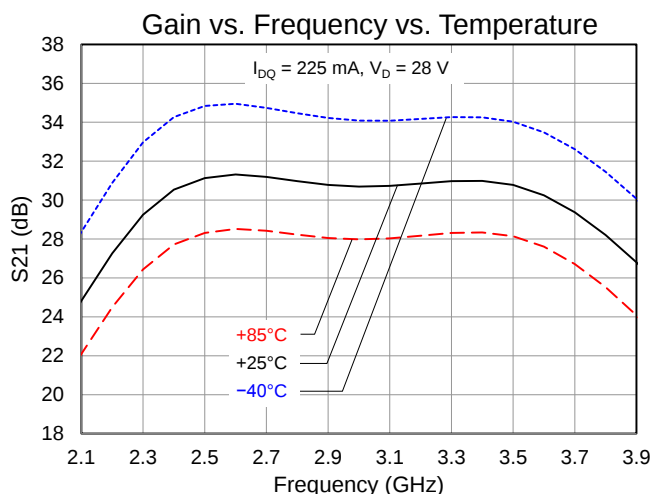
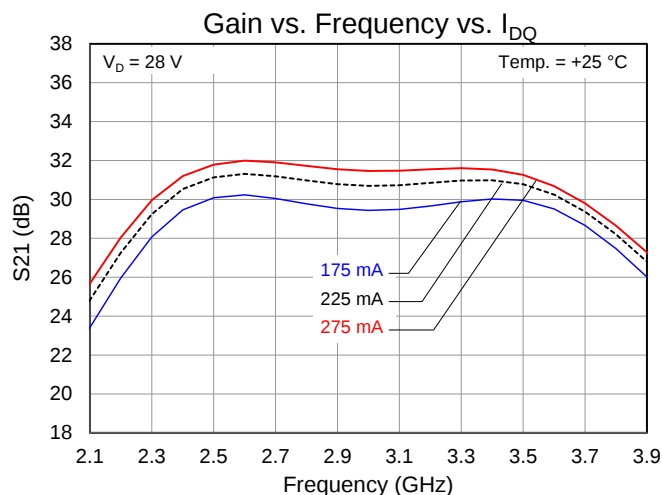
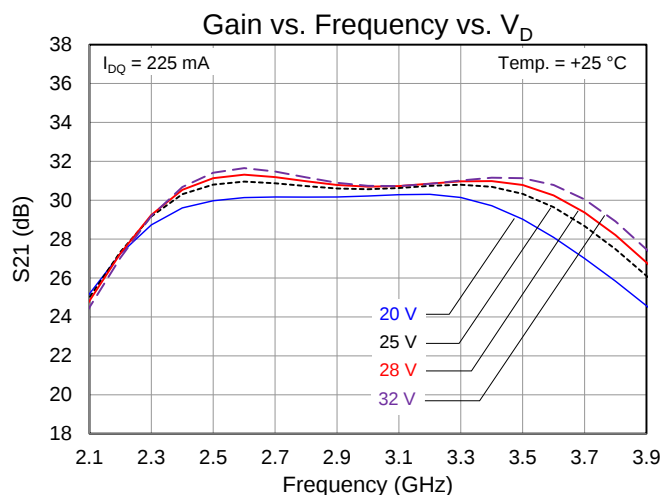
Median Lifetime, Power Dissipation and Max. Gate Current

Test conditions: $V_D = 40\text{V}$; Failure Criteria = 10% reduction in I_{D_MAX}



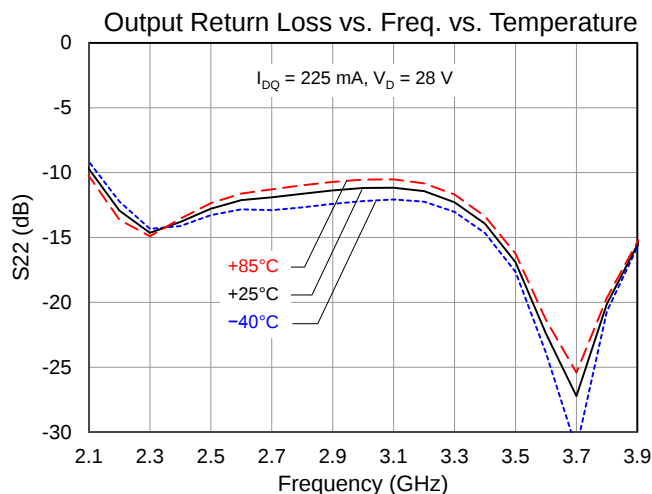
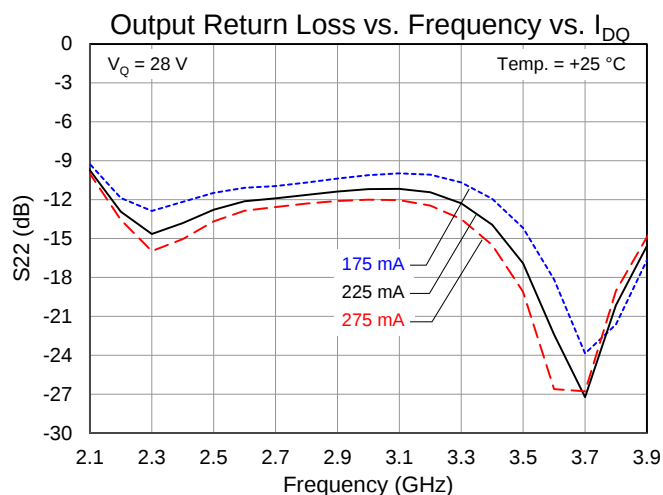
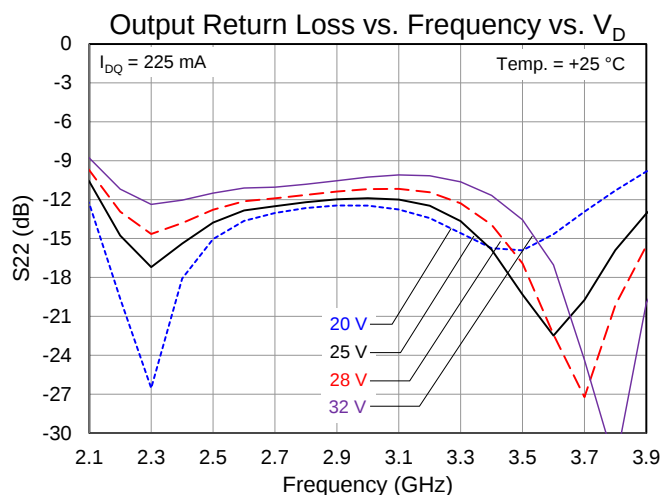
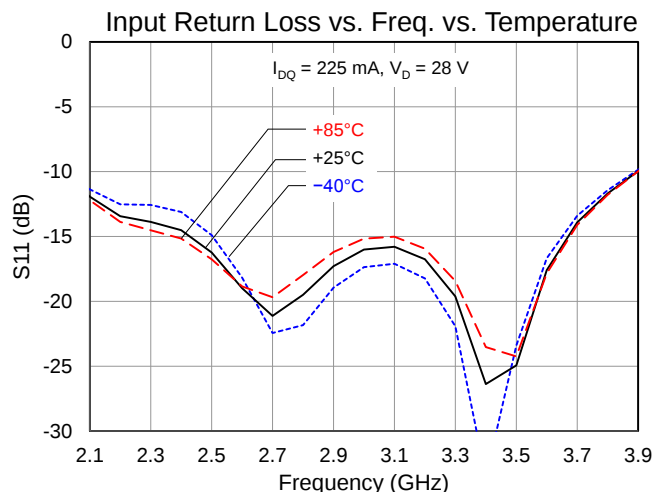
Typical Performance: Small Signal

Condition: CW



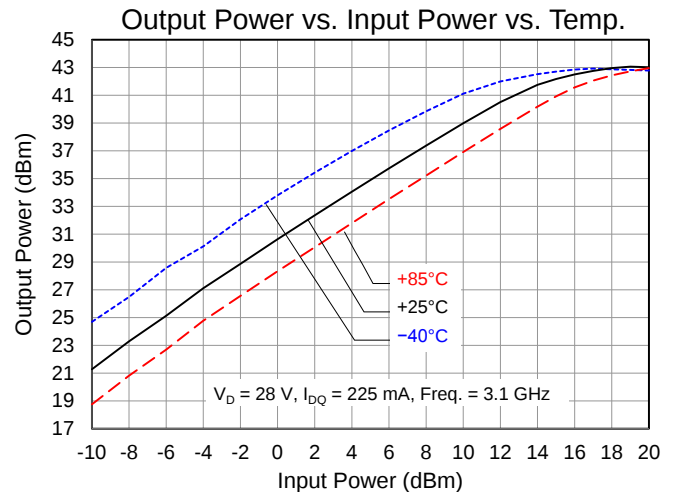
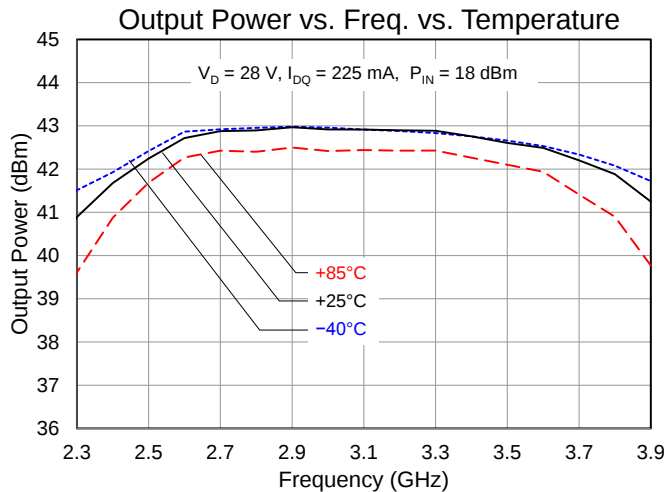
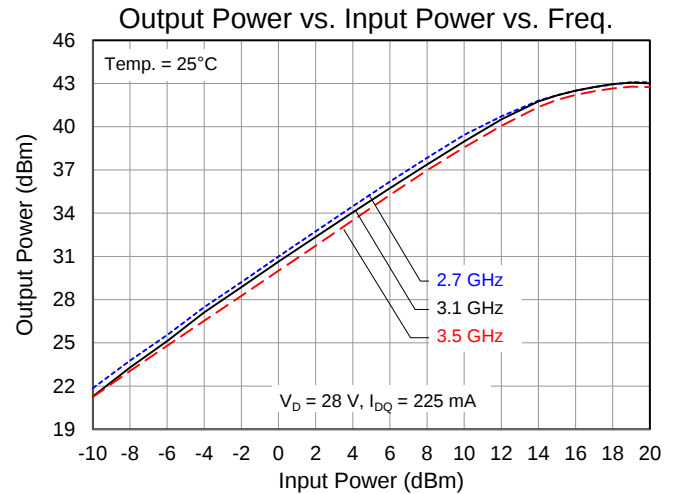
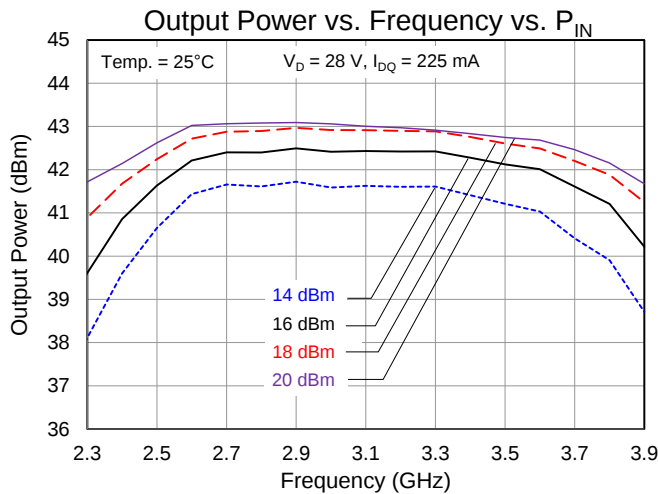
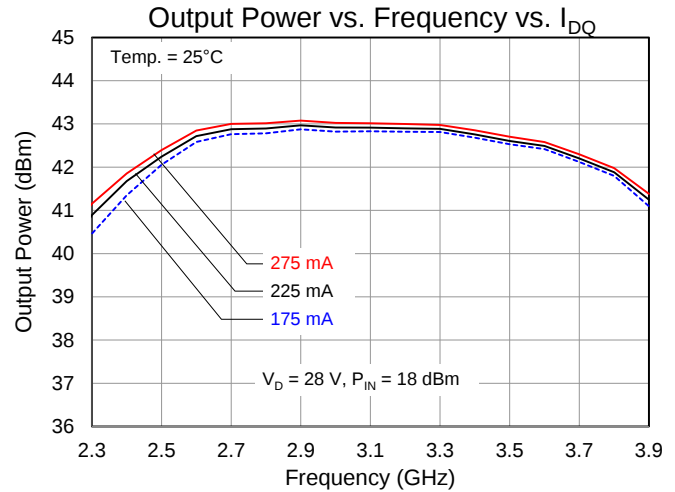
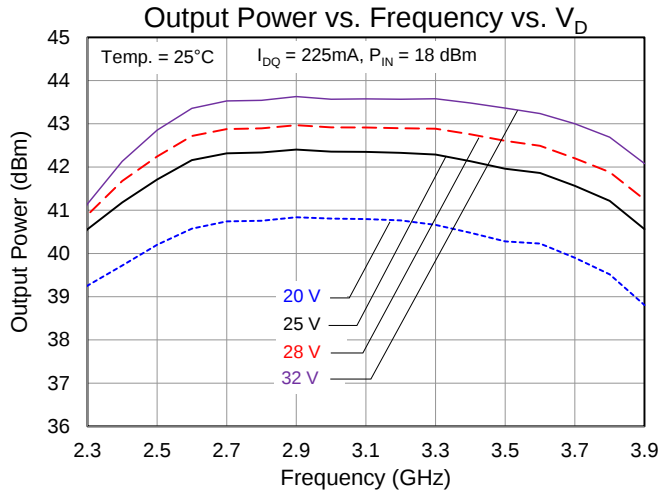
Typical Performance: Small Signal

Condition: CW



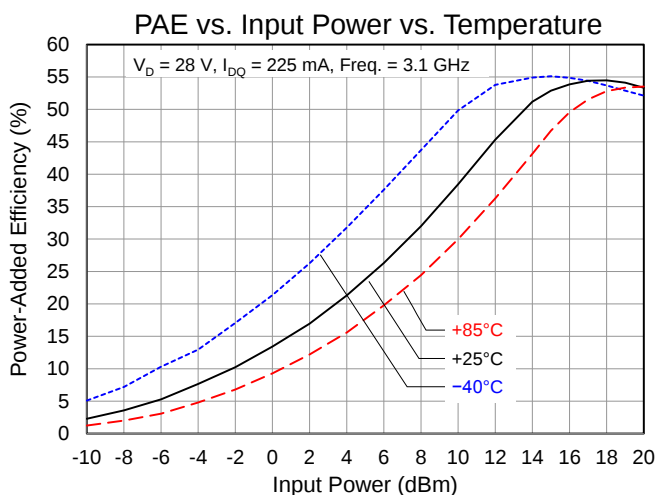
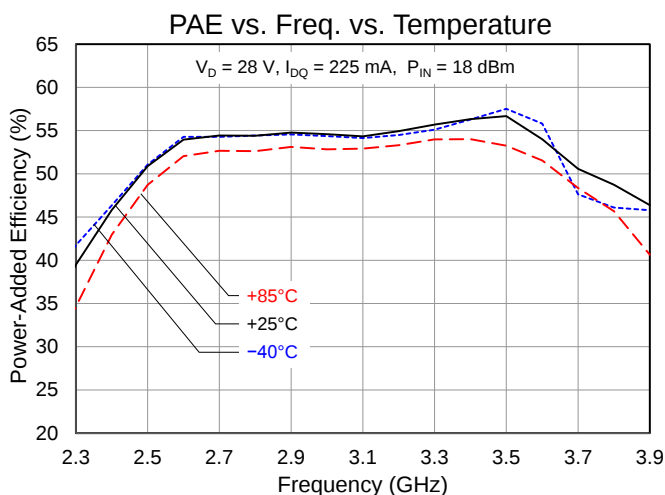
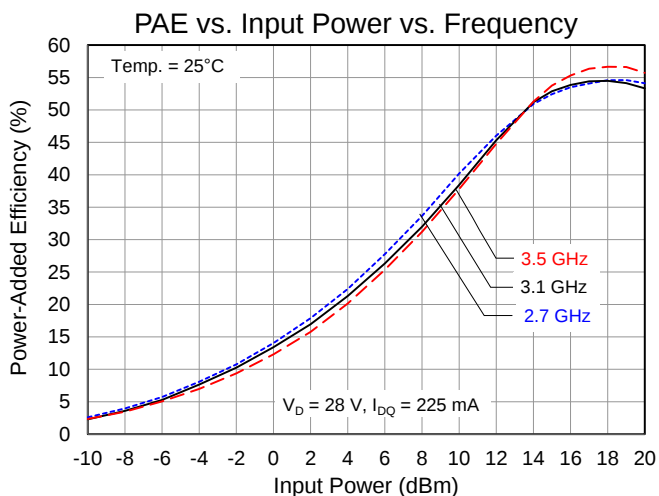
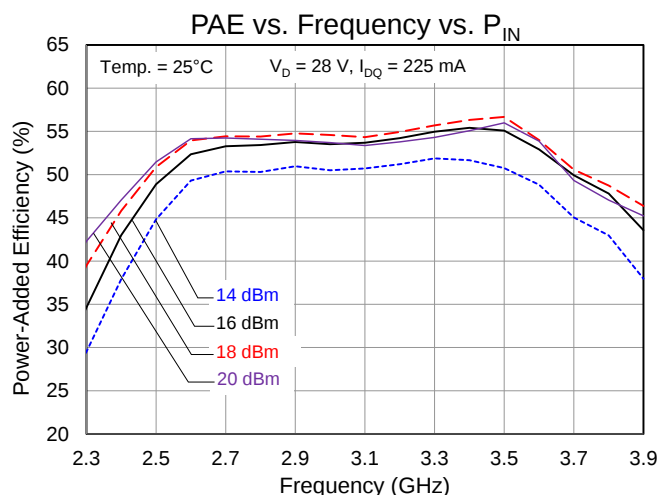
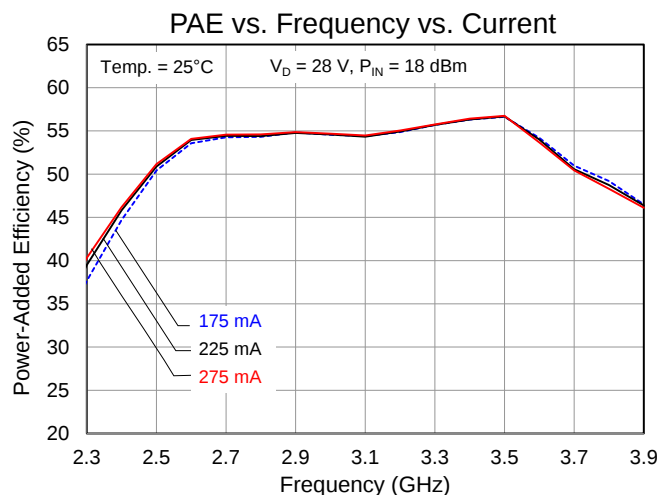
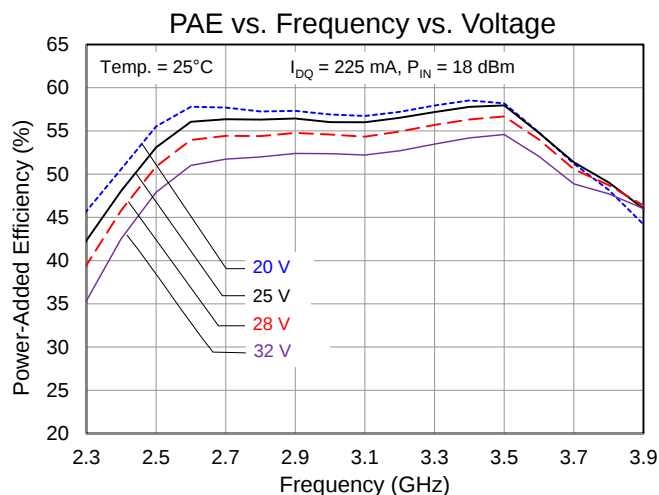
Typical Performance: Large Signal

Condition: Pulsed V_D , Pulse Width = 100 us, Duty Cycle = 10%



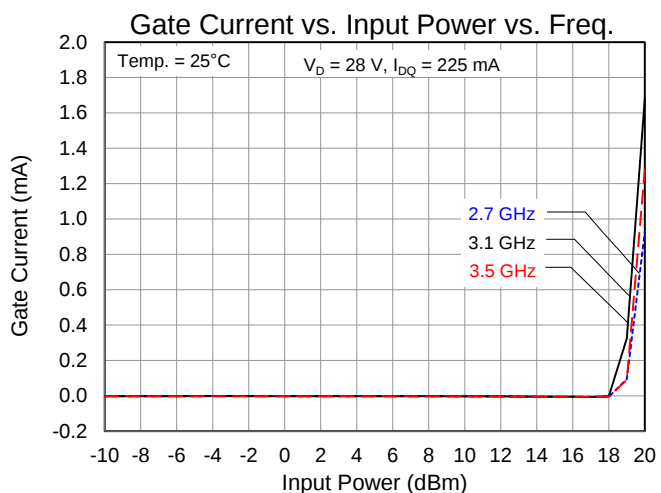
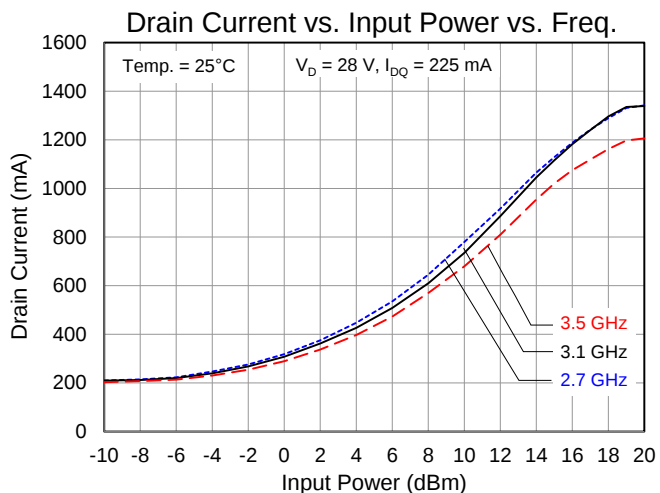
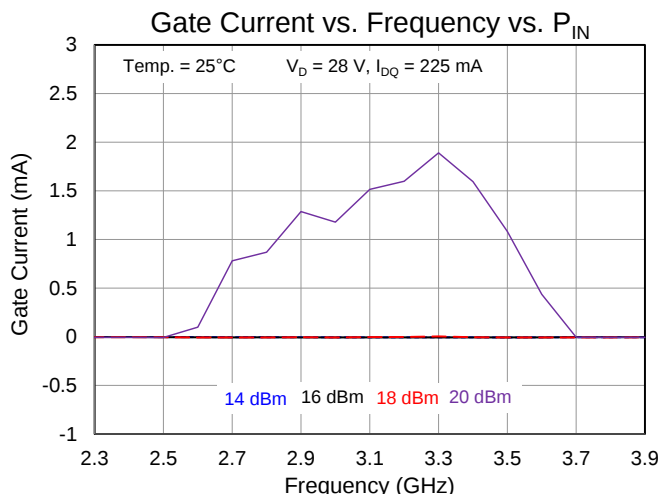
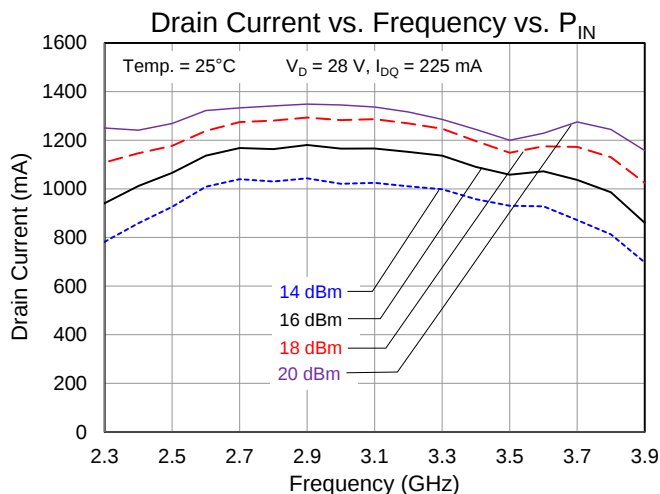
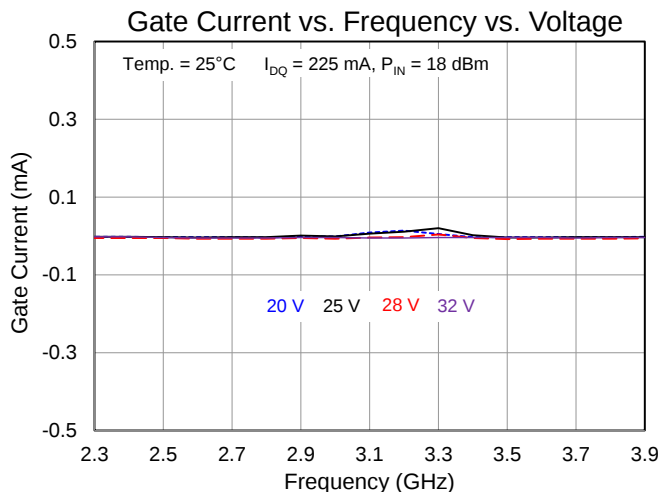
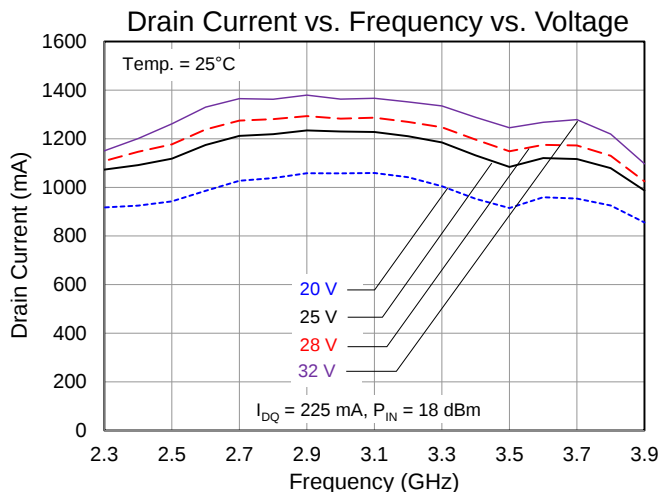
Typical Performance: Large Signal

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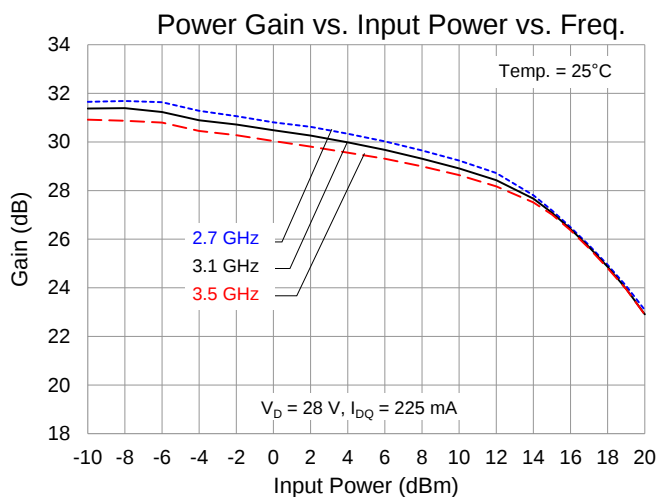
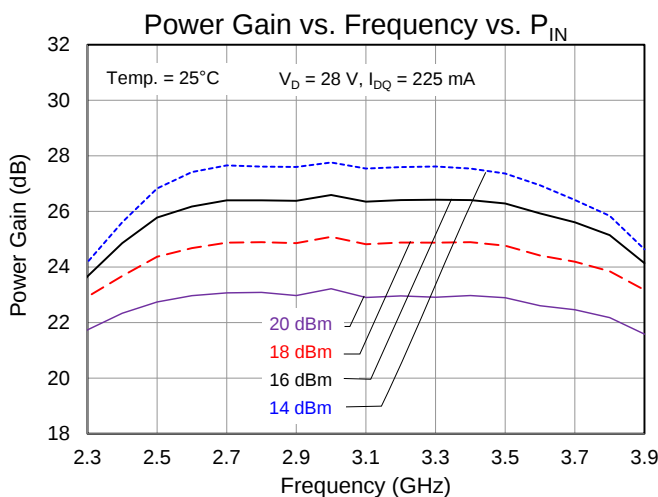
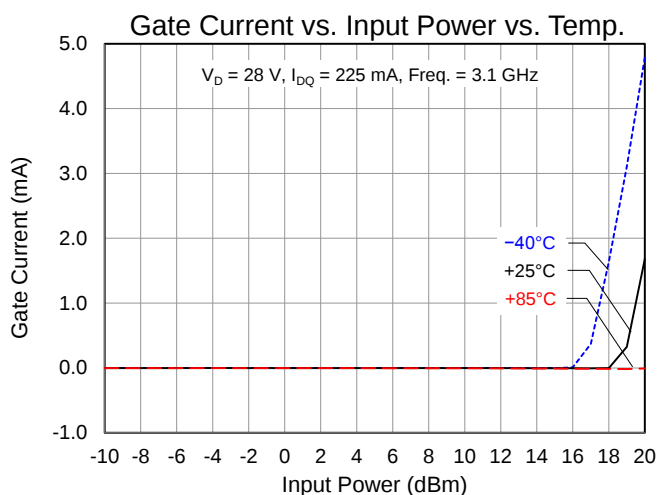
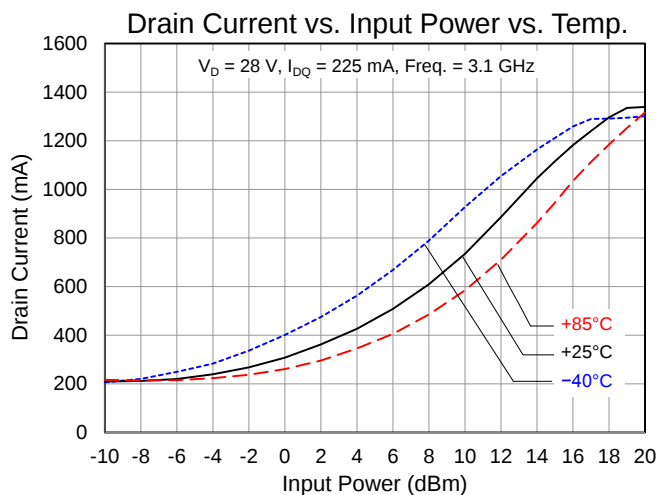
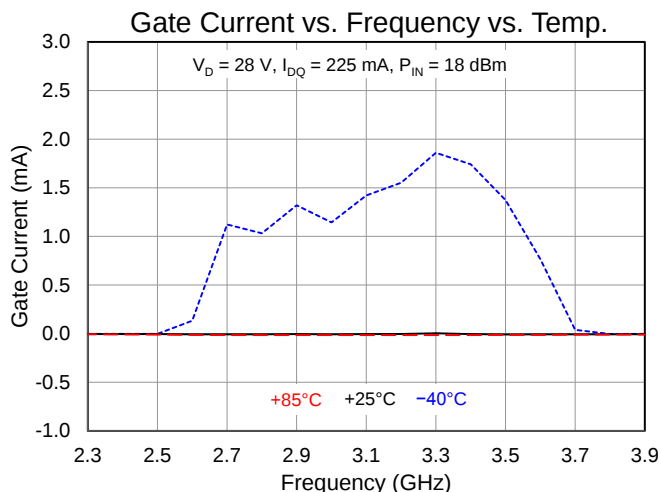
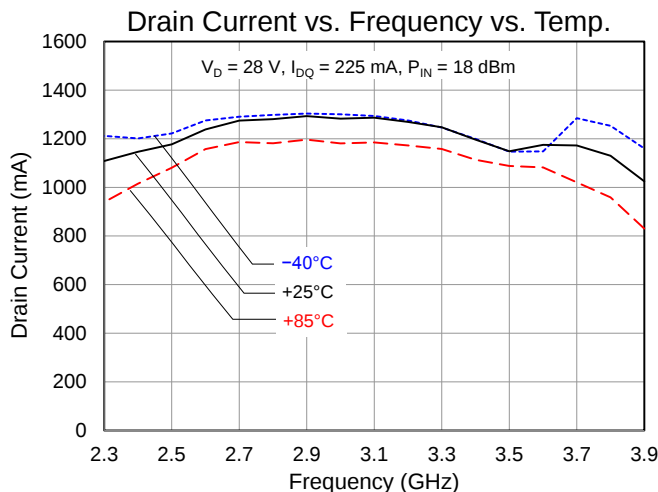
Typical Performance: Large Signal

Condition: Pulsed V_D , Pulse Width = 100 us, Duty Cycle = 10%



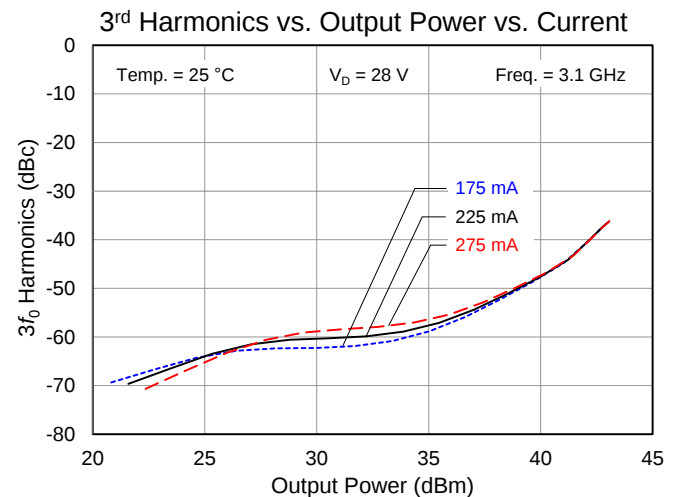
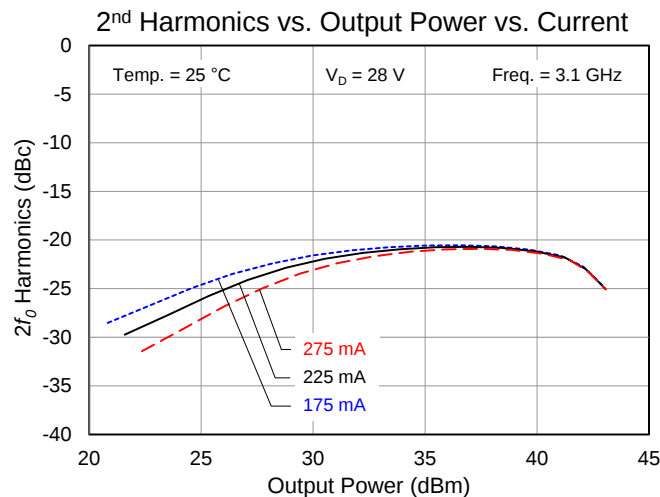
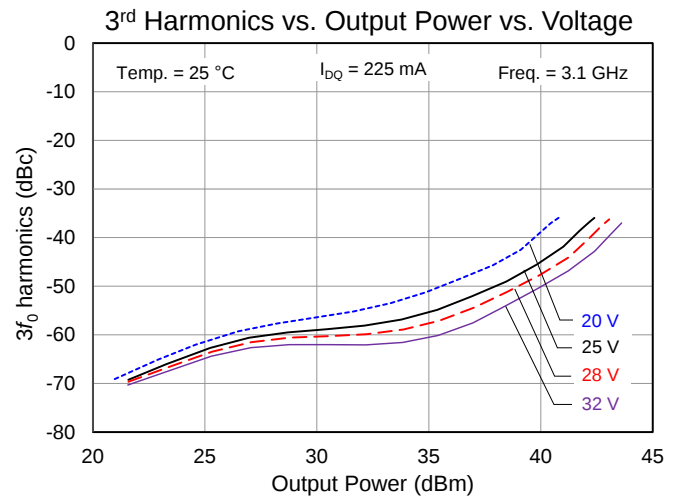
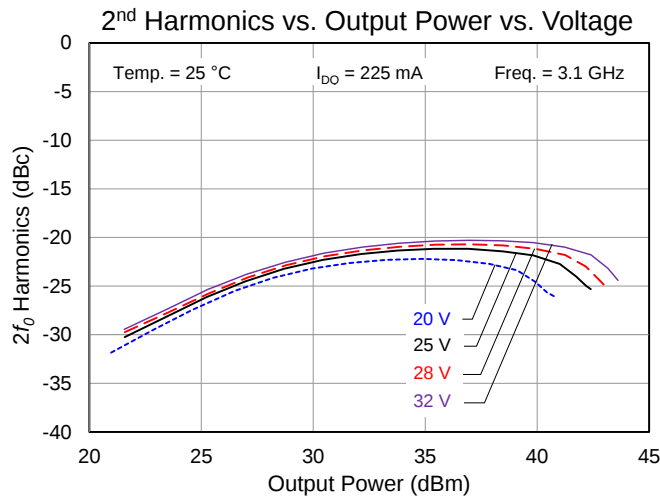
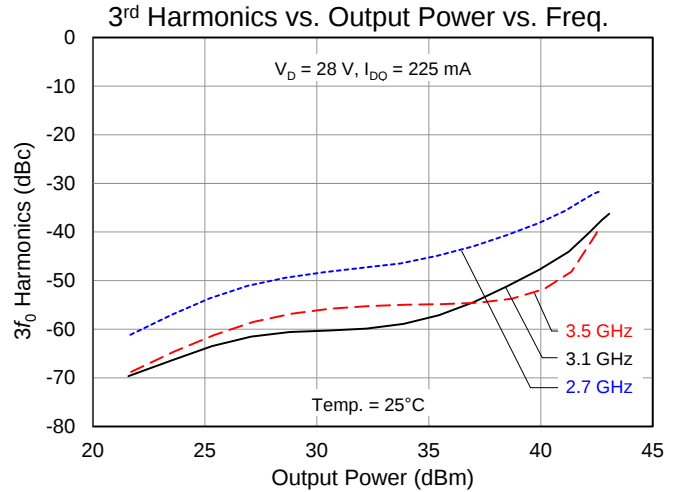
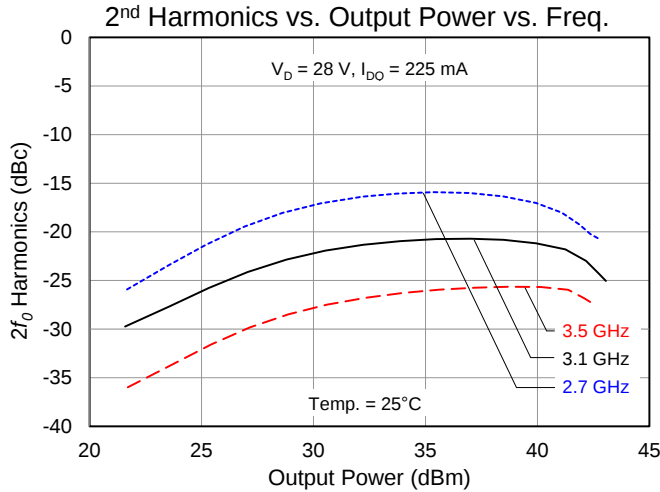
Typical Performance: Large Signal

Condition: Pulsed V_D , Pulse Width = 100 us, Duty Cycle = 10%



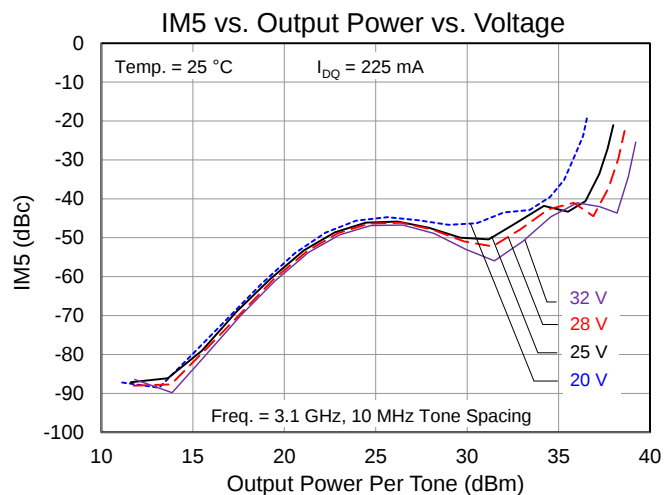
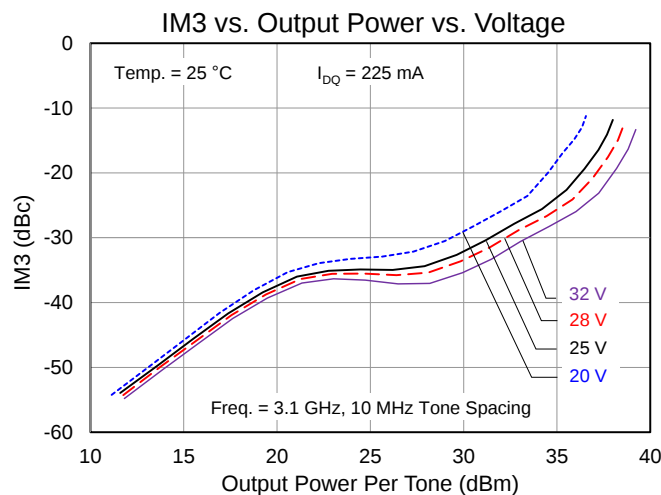
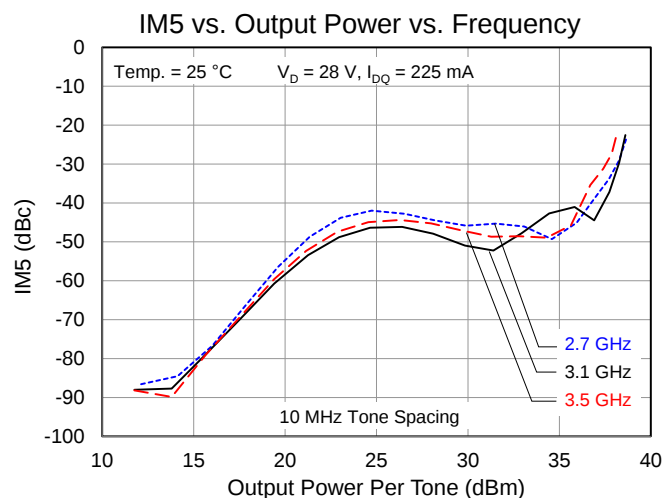
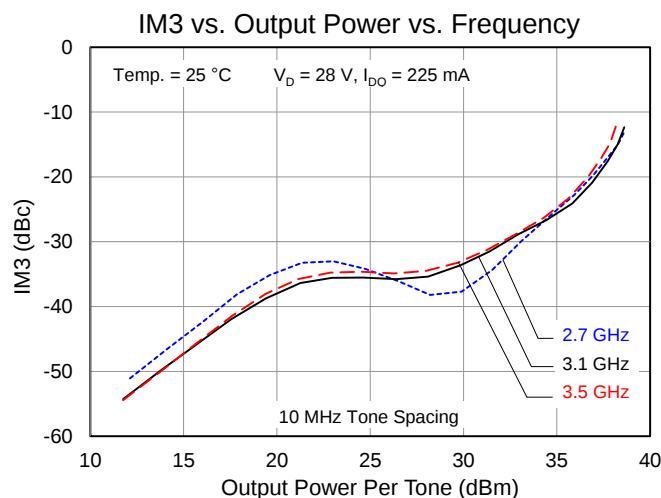
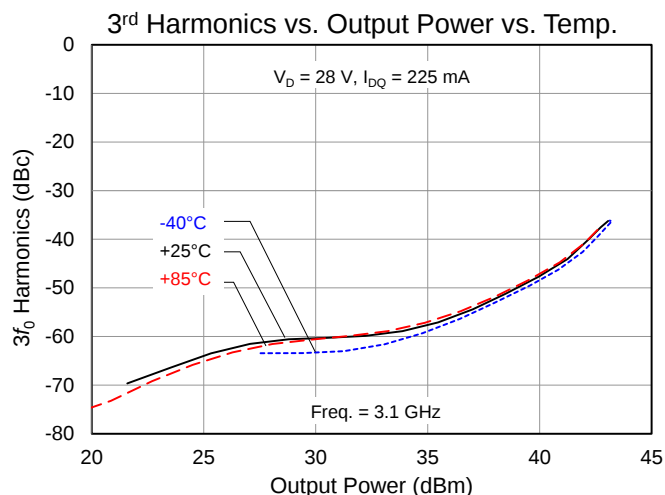
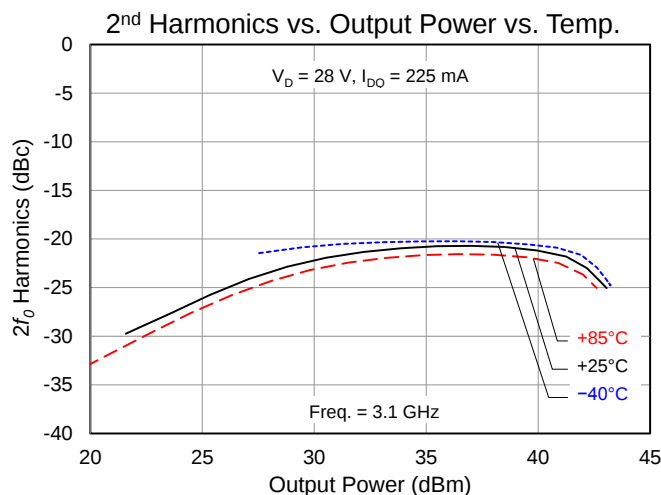
Typical Performance: Large Signal and Linearity

Condition: CW



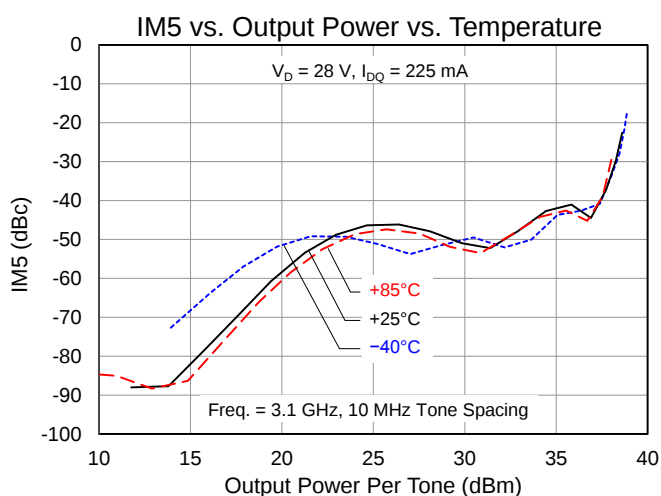
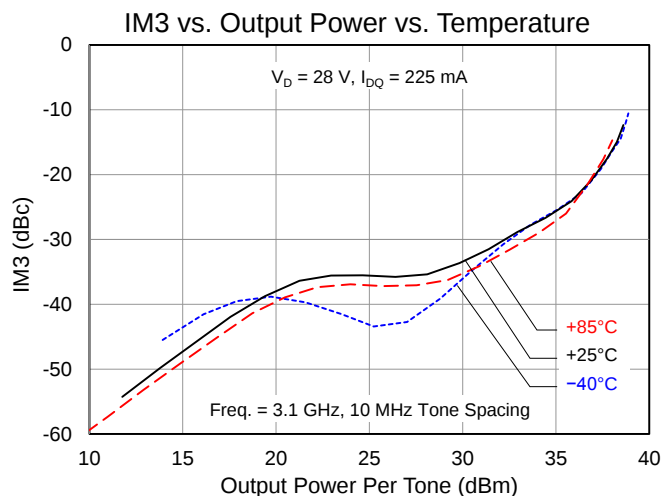
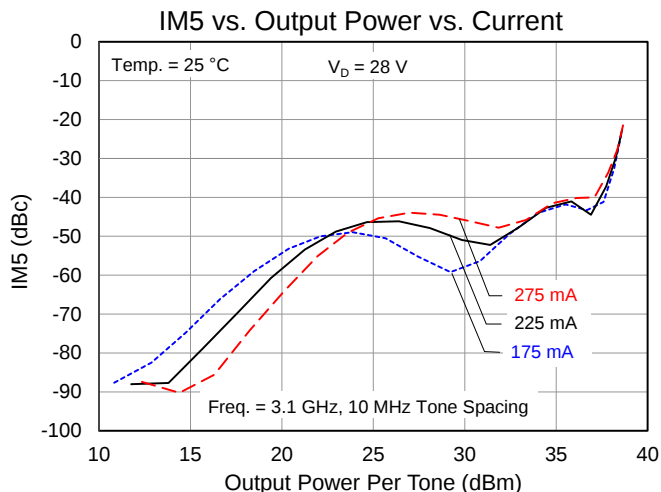
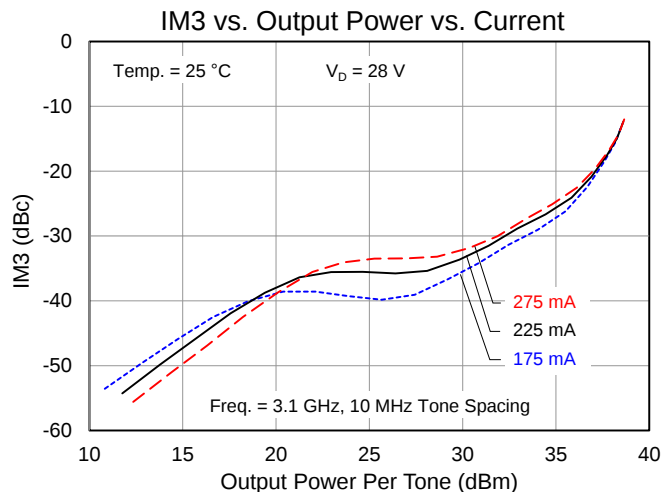
Typical Performance: Large Signal & Linearity

Condition: CW

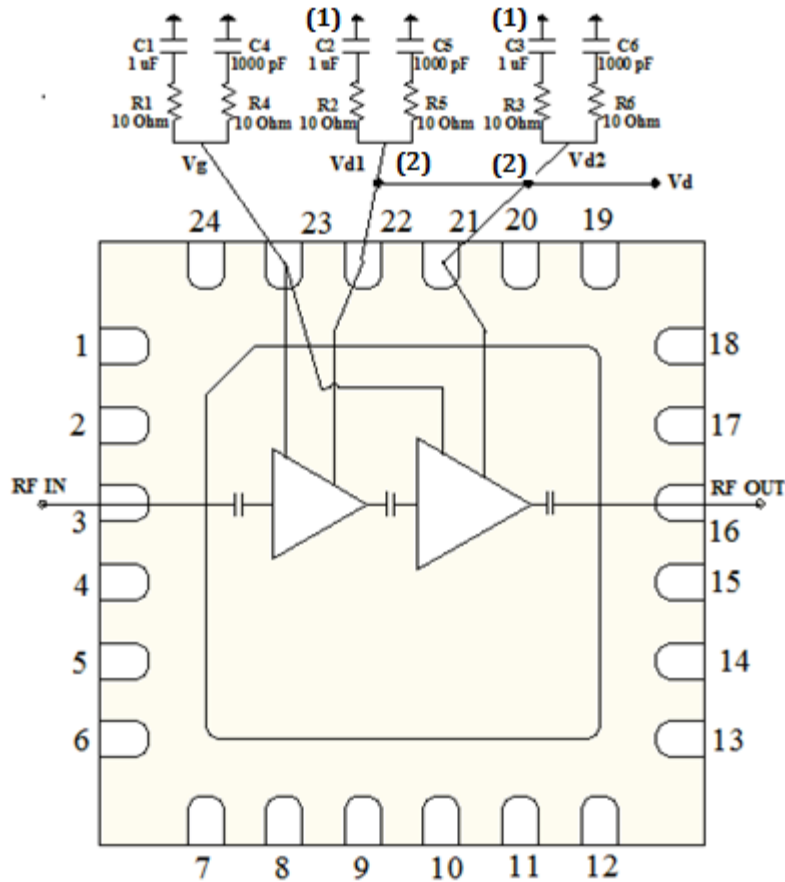


Typical Performance: Large Signal & Linearity

Condition: CW



Applications Information



Notes:

1. Remove if pulsing on drain
2. V_D : Tied V_{D1} & V_{D2} together

Bias-up Procedure

1. Set I_D limit to 1.4 A, I_G limit to 8 mA
2. Apply -5 V to V_G
3. Apply +28 V to V_D ; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until $I_{DQ} = 225$ mA ($V_G \sim -2.9$ V Typ.).
5. Turn on RF supply

Bias-down Procedure

1. Turn off RF supply
2. Reduce V_G to -5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

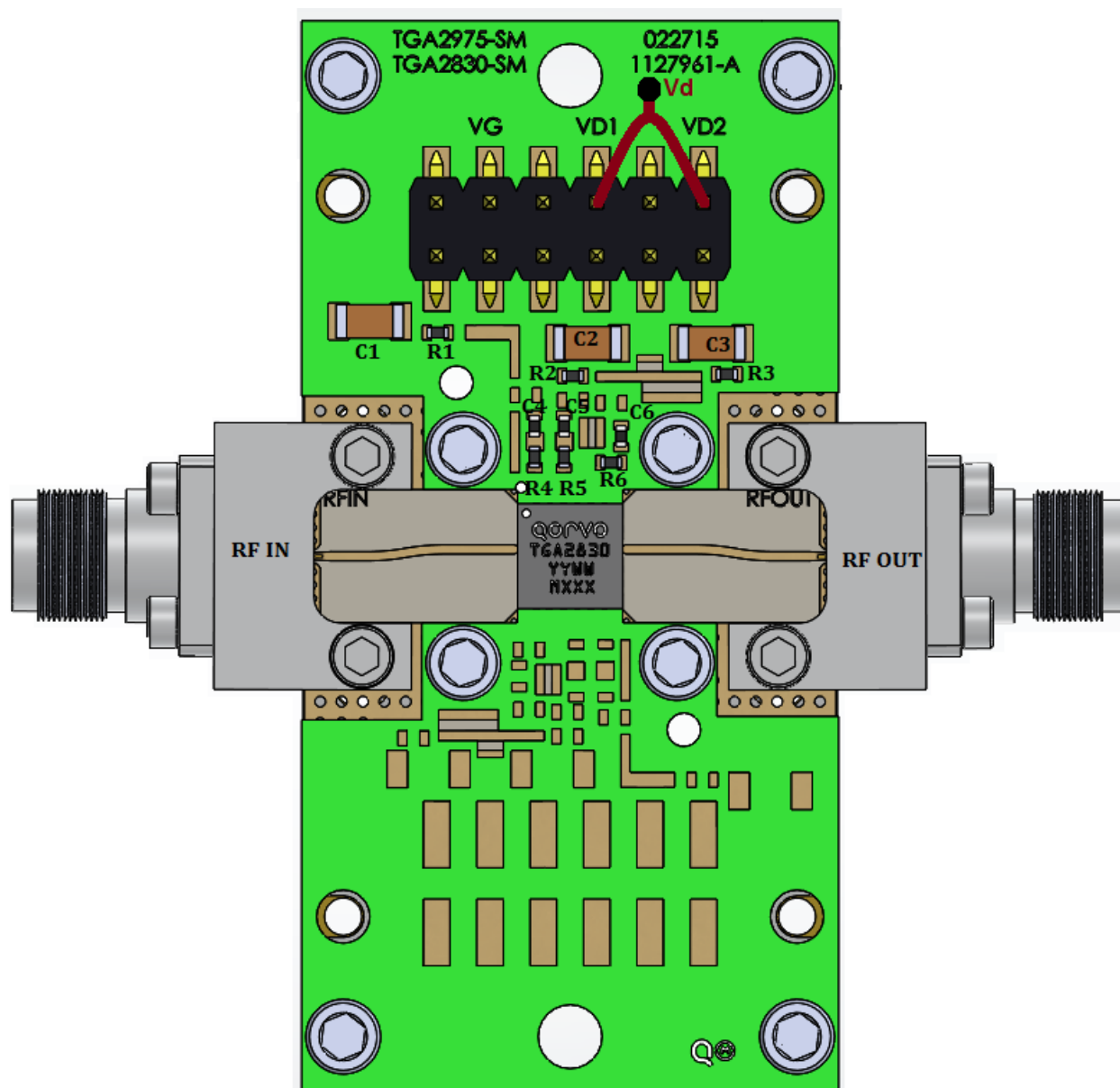
Pin Layout



Pin Description

Pin No.	Symbol	Description
1, 2, 4 – 15, 17 – 20, 24	NC	No internal connection; can be grounded on PCB or left open
3	RF IN	Input; matched to 50 Ω ; DC blocked
16	RF OUT	Output; matched to 50 Ω ; DC blocked
21	DRAIN 2	Drain voltage; bias network is required; see recommended Application Information on page 13
22	DRAIN 1	Drain voltage; bias network is required; see recommended Application Information on page 13
23	GATE	Gate voltage; bias network is required; see recommended Application Information on page 13
25	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

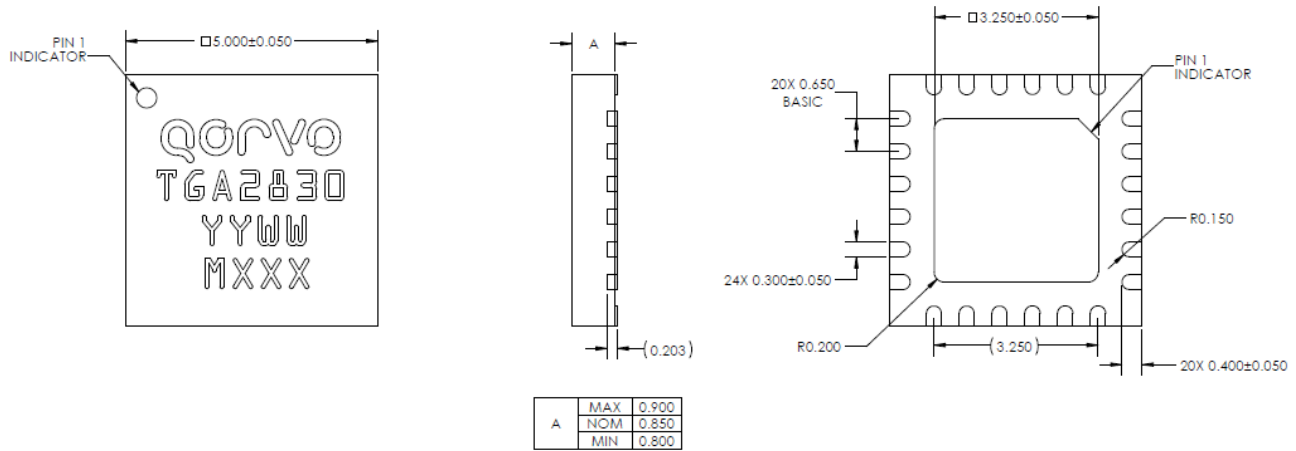
Evaluation Board



Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C3	1 μ F	Cap, 1206, 50 V, 5%, X7R	Various	
C4 – C6	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
R1 – R6	10 Ω	Res, 0402, 5%	Various	

Mechanical Information



Units: millimeter (mm)

Tolerances: unless specified

x.xx = ± 0.01

x.xxx = ± 0.005

Materials:

Package Leads are Gold Plated.

Part is Mold Encapsulated.

Marking:

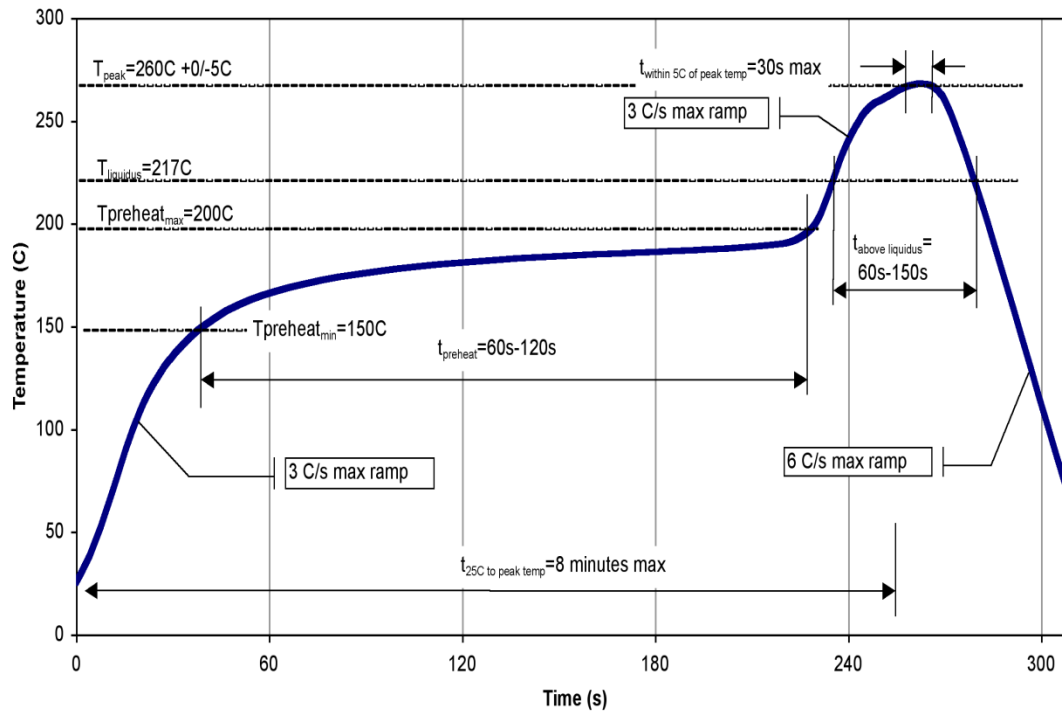
2830: Part number

YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Level TBD at TBD°C convection reflow
The part is rated Moisture Sensitivity Level TBD at TBD°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260°C

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

ECCN

US Department of Commerce: EAR99

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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