TGA2307-SM

4.5-6.5 GHz 50 Watt GaN Power Amplifier

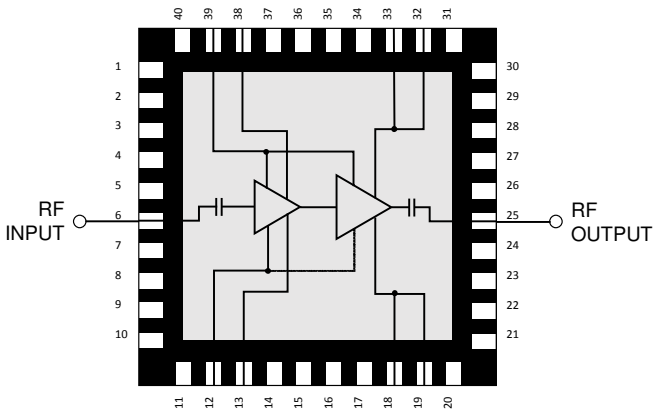
Applications

- C-Band Radar
- Satellite Communication

Product Features

- Frequency Range: 4.5 to 6.5 GHz
- Output Power (P_{IN} = 27 dBm): > 47 dBm
- Power Added Efficiency (P_{IN} = 27 dBm): > 44.4 %
- Small Signal Gain: > 26 dB
- Input Return Loss: > 17 dB
- Large Signal Gain (P_{IN} = 27 dBm): > 20 dB
- Bias Condition: V_D = 28 V, I_{DQ} = 500 mA
- Pulsed Operation
- Plastic Overmold QFN Package
- Package Dimensions: 6.00 x 6.00 x 0.85 mm

Functional Block Diagram



General Description

Qorvo's TGA2307-SM is a packaged power amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. Operating from 4.5-6.5 GHz, the TGA2307-SM produces greater than 47 dBm of saturated output power with a power-added efficiency greater than 44% and a large signal gain greater than 20 dB.

The TGA2307-SM is offered in a 6 x 6 mm plastic overmold QFN to support low cost board assembly techniques. In addition, the package uses a copper alloy base that offers superior thermal management. With both RF ports fully matched to 50 ohms with integrated DC blocking capacitors, the TGA2307 is ideally suited to support both commercial and military applications.

Lead-free and RoHS compliant.

Evaluation boards available on request.

Pad Configuration

Pad Number	Symbol
1–5, 7–11, 14–17, 20–24, 26–31, 34–37, 40	NC
6	RF Input
12, 39	VG
13, 38	VD1
18–19, 32–33	VD2
25	RF Output
41 (center pad)	GND

Ordering Information

Part	ECCN	Description
TGA2307-SM	3A001.b.2.a.4	4.5–6.5 GHz 50W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Drain Current (I_D)	7.5 A
Gate Voltage range (V_G)	-5 to 0 V
Gate Current (I_D)	See plot pg. 3
Input P_{IN}, Pulsed[1], 50 Ω, 85 ℃	34 dBm
Input P_{IN}, Pulsed[1], 3:1 VSWR, 85 ℃	34 dBm
Mounting Temperature (30 s max)	260 ℃
Storage Temperature	-40 to 150 ℃

Note:
[1] Pulse conditions: PW = 100 us, Duty Cycle = 1%

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	28 V
Drain Current, quiescent (I_{DQ})	1000 mA
Gate Voltage (V_G), typical	-2.40 V
Operating Temperature	-40 to 85 ℃

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 ℃, I_{DQ} = 500 mA, Pulse Conditions PW = 100 us, Duty Cycle = 1%

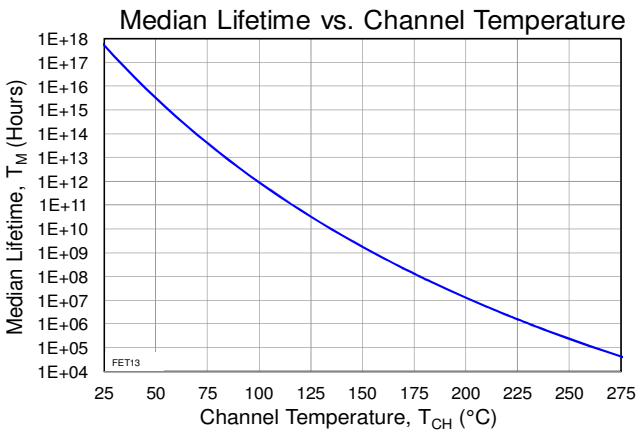
Parameter	Min	Typical	Max	Units
Operational Frequency Range	4.5		6.5	GHz
Small Signal Gain		> 26		dB
Input Return Loss		> 17		dB
Output Return Loss		> 8.5		dB
Output Power (P_{IN} = 27 dBm)		> 47		dBm
Large Signal Gain (P_{IN} = 27 dBm)		> 20		dB
Power Added Efficiency (P_{IN} = 27 dBm)		> 44.4		%
2nd Harmonic Level (P_{OUT} = 45 dBm , Freq. = 5.5 GHz)		< -47		dBc
Sm. Sig. Gain Temp. Coeff.		-0.042		dB/ ℃
Output Power Temp. Coeff.		-0.007		dB/ ℃

Thermal and Reliability Information

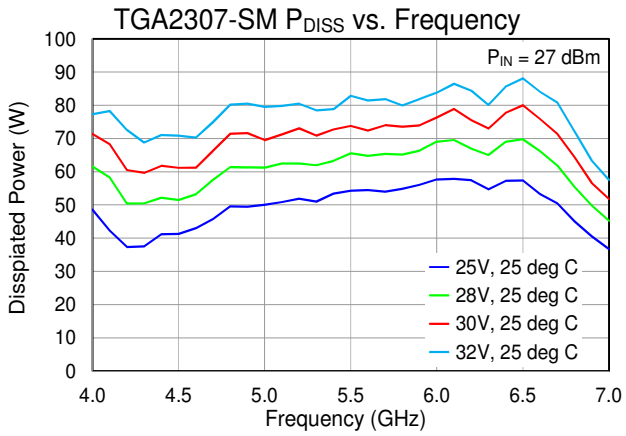
Parameter	Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 28 V, I_D = 1.0 A (quiescent), P_{DISS} = 28 W	1.214	°C/W
Channel Temperature (T_{CH})		119	°C
Median Lifetime (T_M)		7.01E+10	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 28 V, I_D = 4.3 A, P_{IN} = 27 dBm, P_{OUT} = 47.3 dBm, PW = 100 us, DC = 10%, P_{DISS} = 62 W	0.887	°C/W
Channel Temperature (T_{CH})		140	°C
Median Lifetime (T_M)		5.43E+09	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = 32 V, I_D = 5.1 A, P_{IN} = 24 dBm, P_{OUT} = 48.0 dBm, PW = 100 us, DC = 10%, P_{DISS} = 80 W	0.963	°C/W
Channel Temperature (T_{CH})		162	°C
Median Lifetime (T_M)		4.85E+08	Hrs

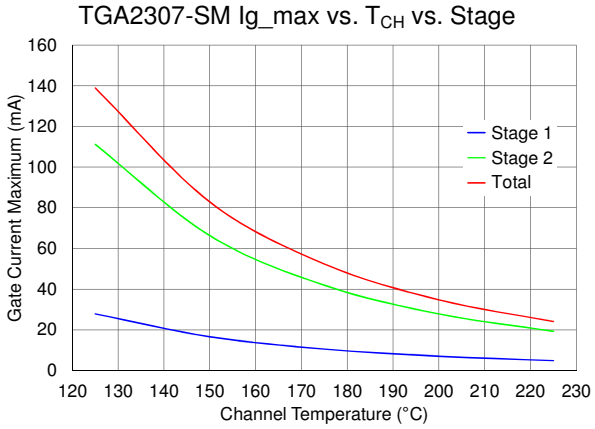
Median Lifetime

Test Conditions: 40 V
Failure Criterion = 10% reduction in $I_{D\,MAX}$



Pulse condition: PW = 100 us, Duty Cycle = 1%

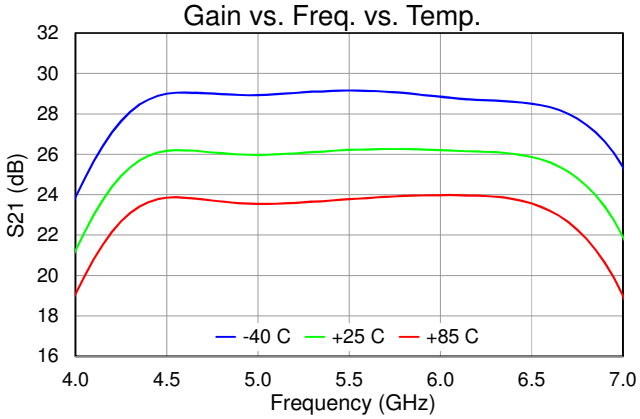




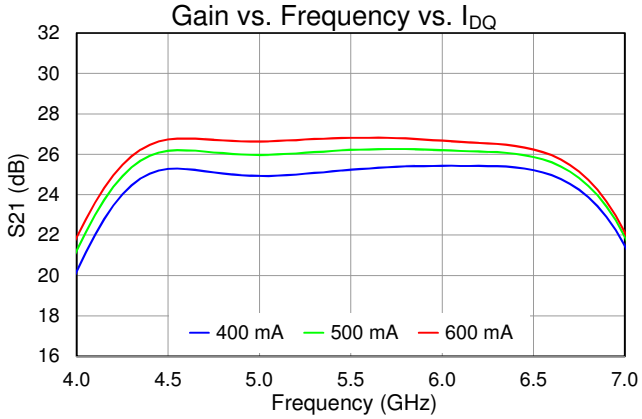
Typical Performance: Small Signal

Test conditions unless otherwise noted: 25 °C, V_D = 28 V, I_{DQ} = 500 mA

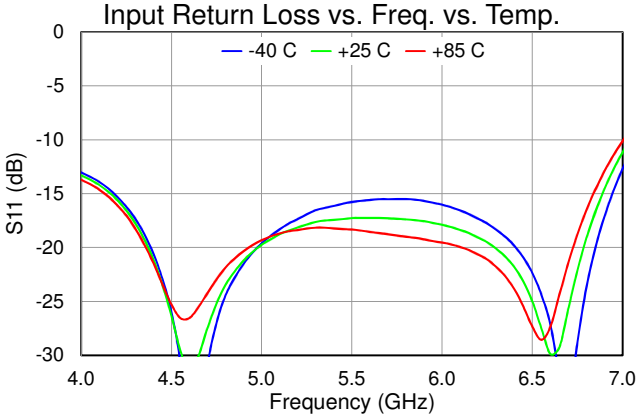
Gain vs. Freq. vs. Temp.



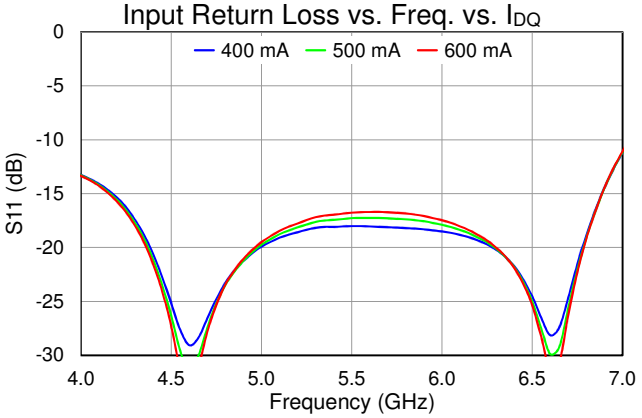
Gain vs. Frequency vs. I_{DQ}



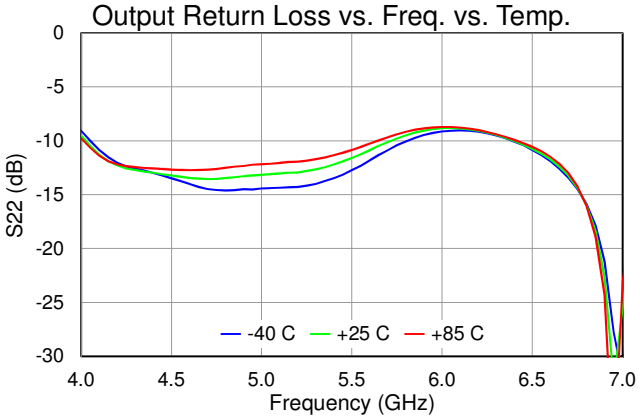
Input Return Loss vs. Freq. vs. Temp.



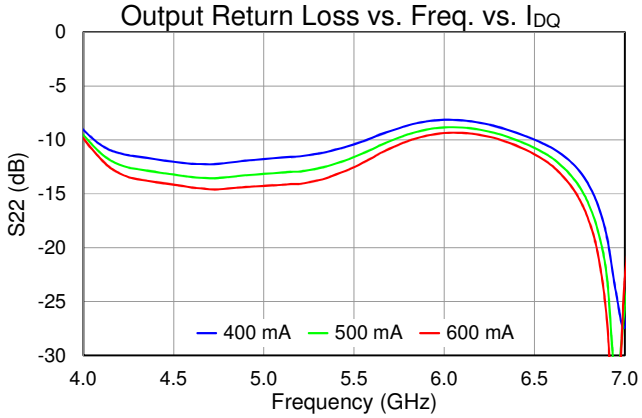
Input Return Loss vs. Freq. vs. I_{DQ}



Output Return Loss vs. Freq. vs. Temp.



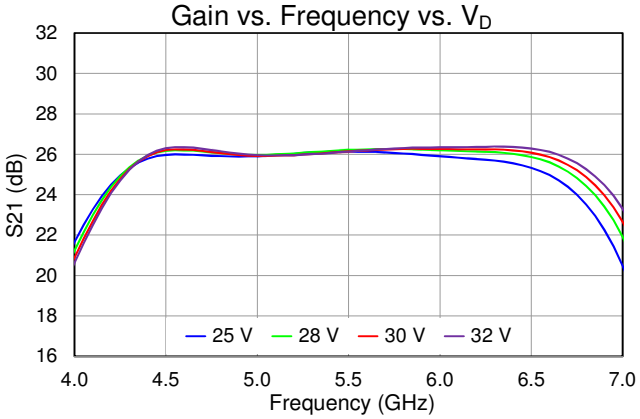
Output Return Loss vs. Freq. vs. I_{DQ}



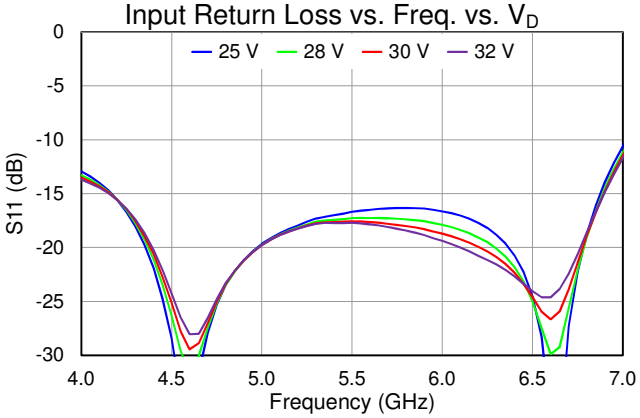
Typical Performance: Small Signal

Test conditions unless otherwise noted: 25 °C, V_D = 28 V, I_{DQ} = 500 mA

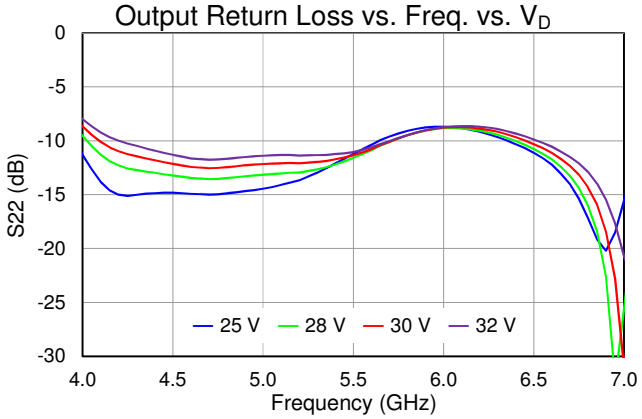
Gain vs. Frequency vs. V_D



Input Return Loss vs. Freq. vs. V_D

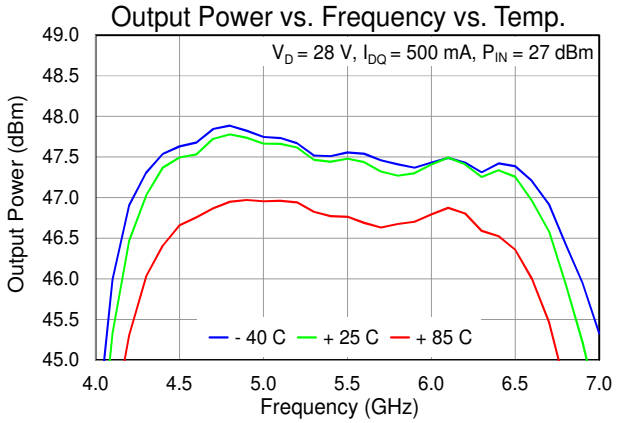


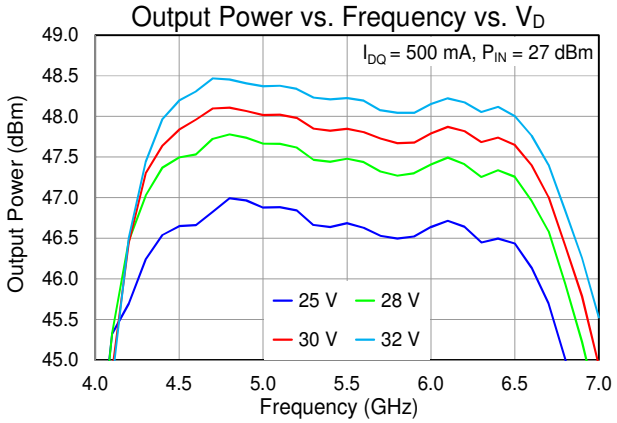
Output Return Loss vs. Freq. vs. V_D

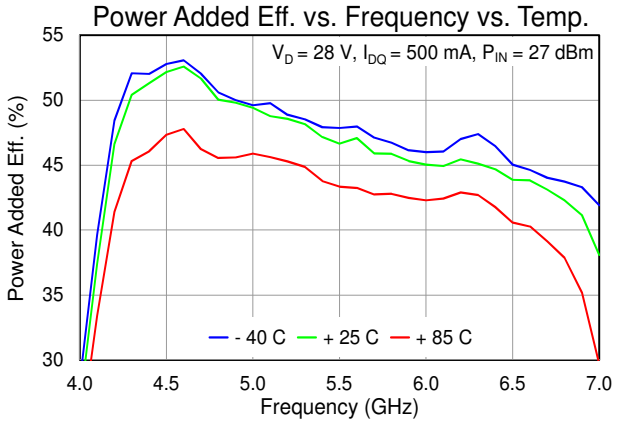


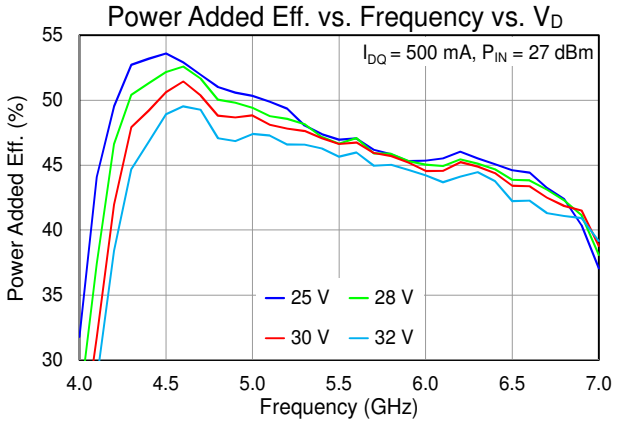
Typical Performance: Large Signal (Pulsed)

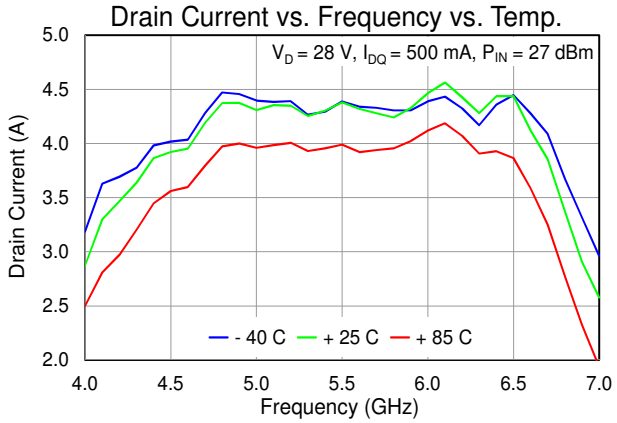
Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%

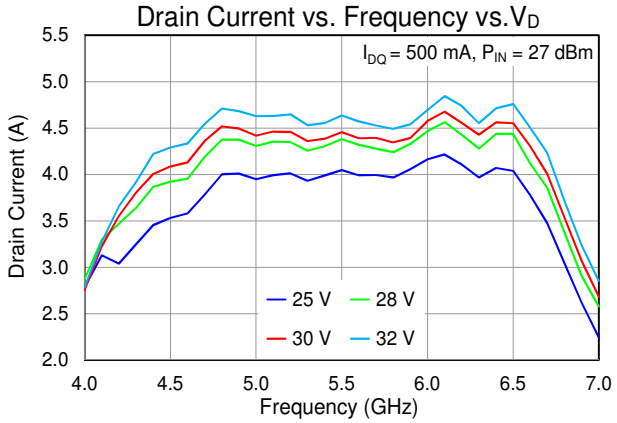






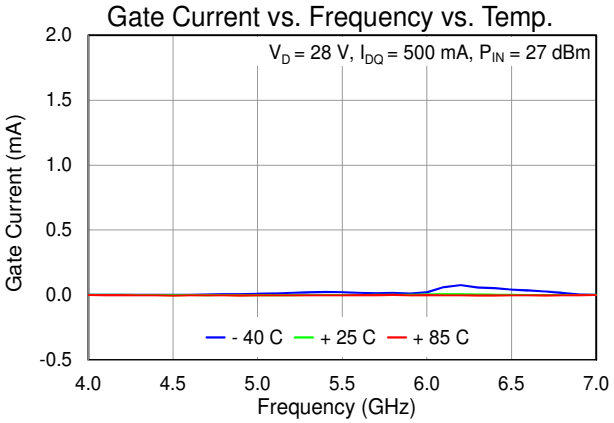


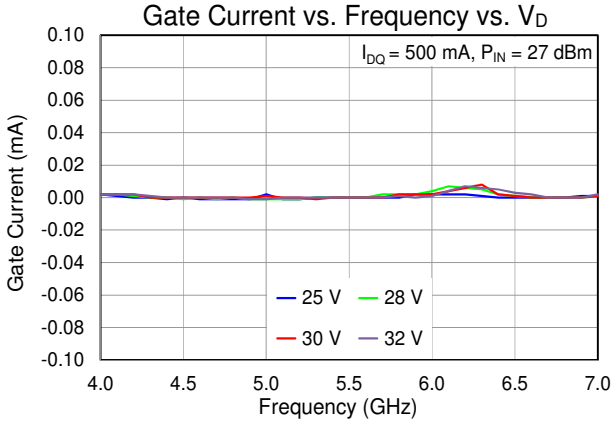




Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%

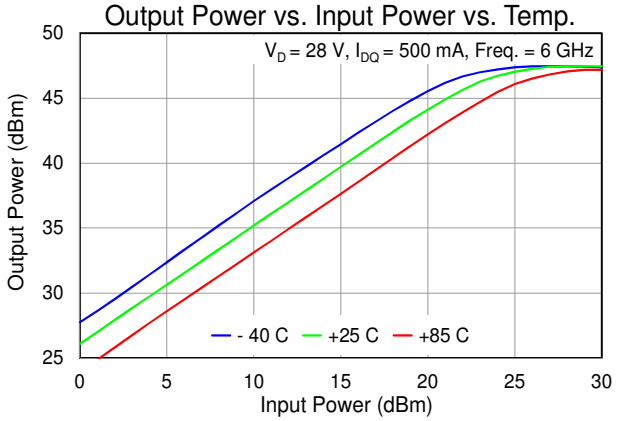




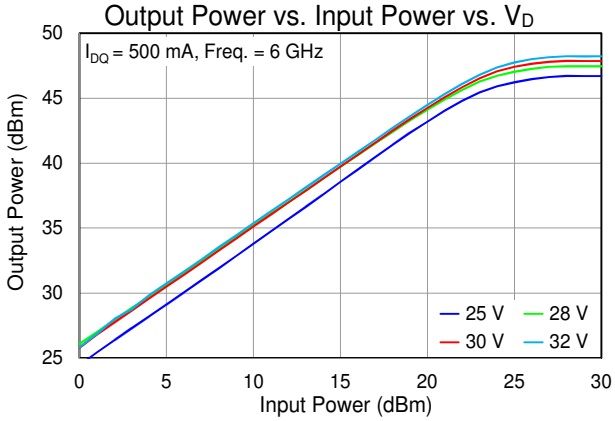
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%

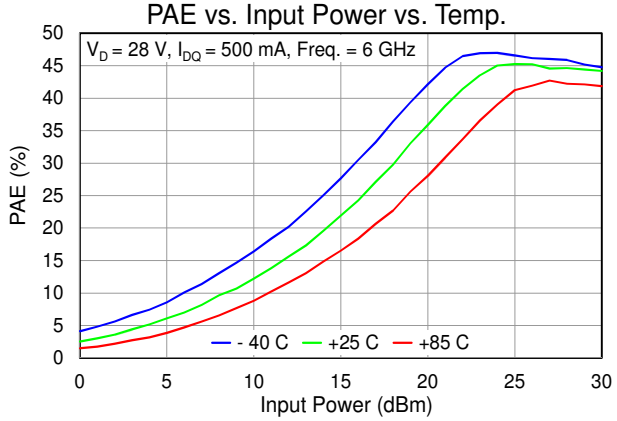
Output Power vs. Input Power vs. Temp.



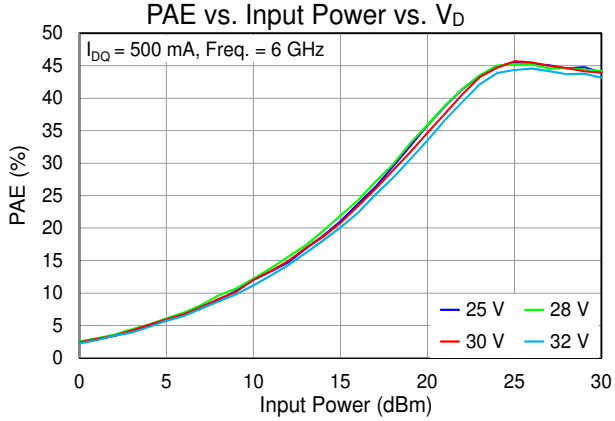
Output Power vs. Input Power vs. V_D



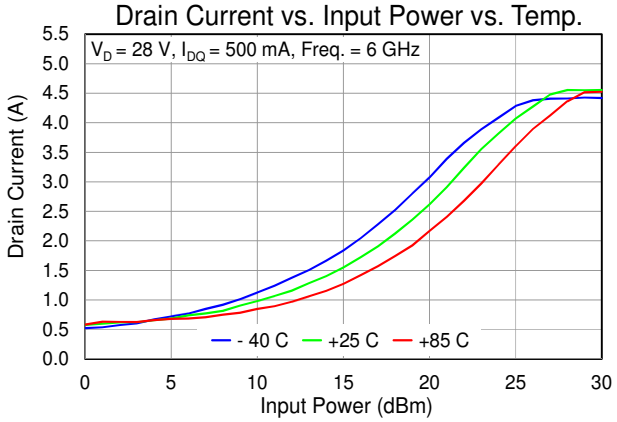
PAE vs. Input Power vs. Temp.



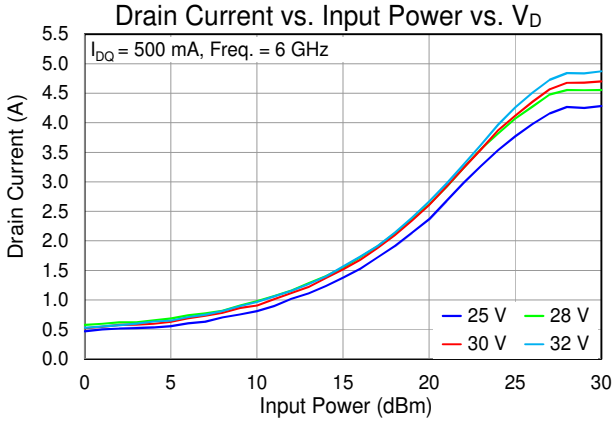
PAE vs. Input Power vs. V_D



Drain Current vs. Input Power vs. Temp.



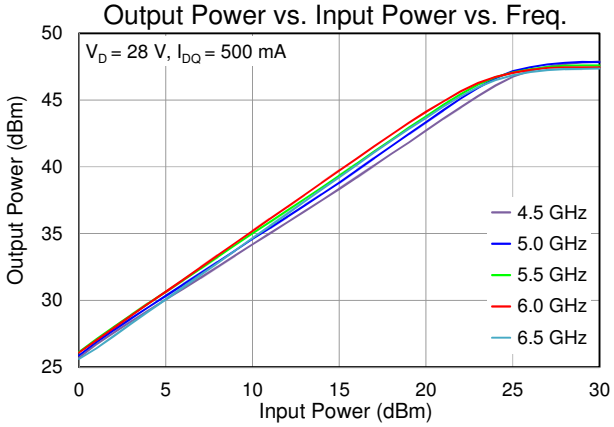
Drain Current vs. Input Power vs. V_D



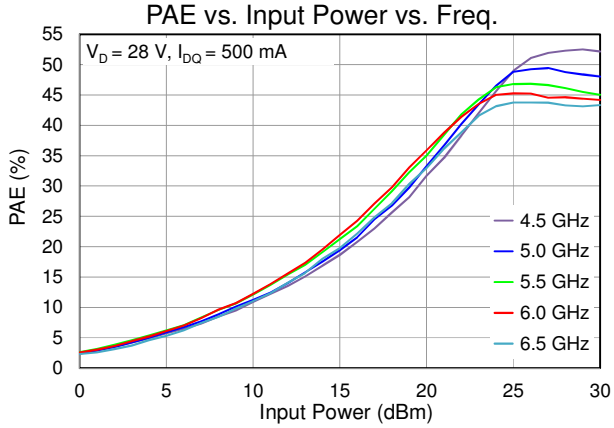
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%

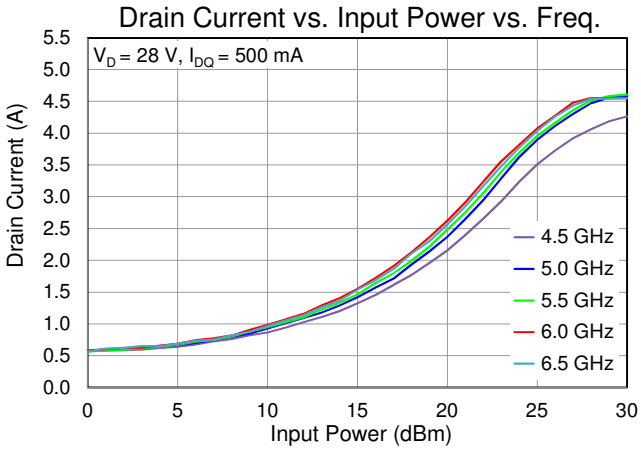
Output Power vs. Input Power vs. Freq.



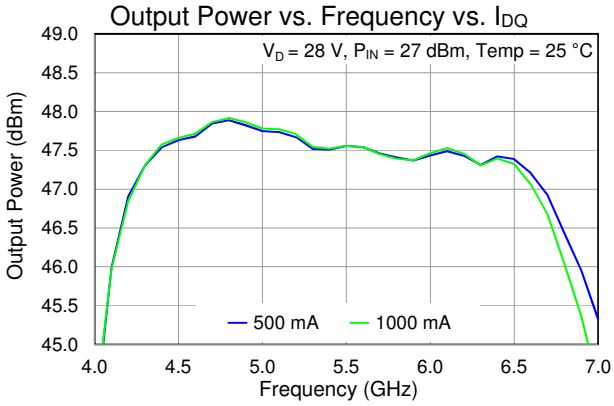
PAE vs. Input Power vs. Freq.



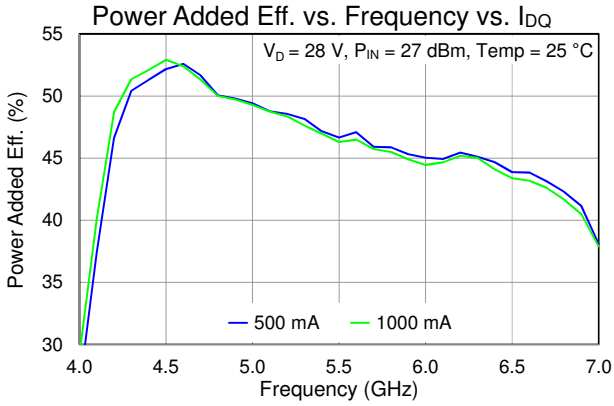
Drain Current vs. Input Power vs. Freq.



Output Power vs. Frequency vs. I_{DQ}



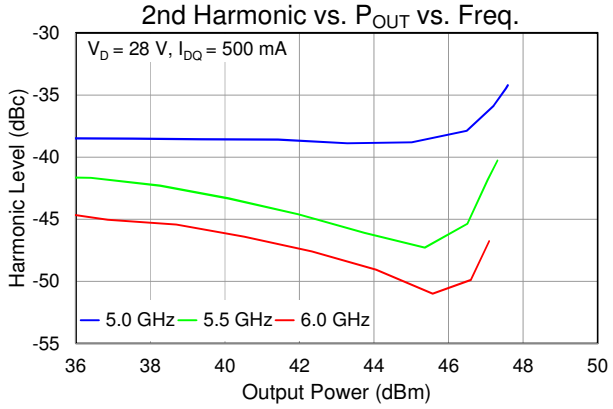
Power Added Eff. vs. Frequency vs. I_{DQ}



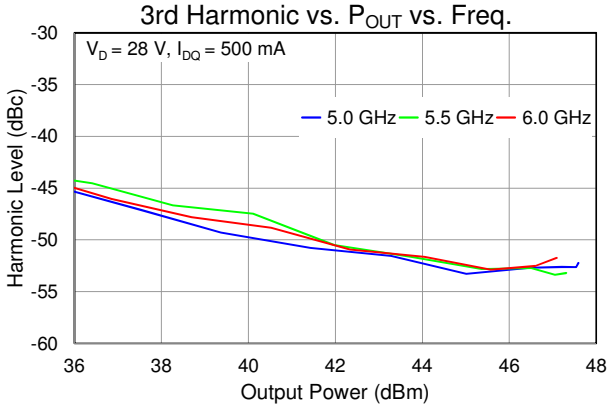
Typical Performance: 2nd Harmonic Level (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%

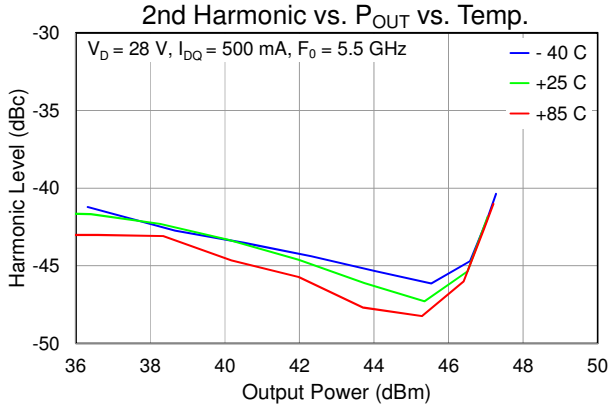
2nd Harmonic vs. P_{OUT} vs. Freq.



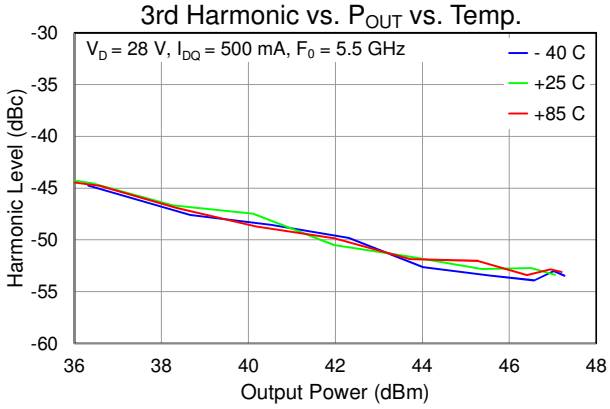
3rd Harmonic vs. P_{OUT} vs. Freq.



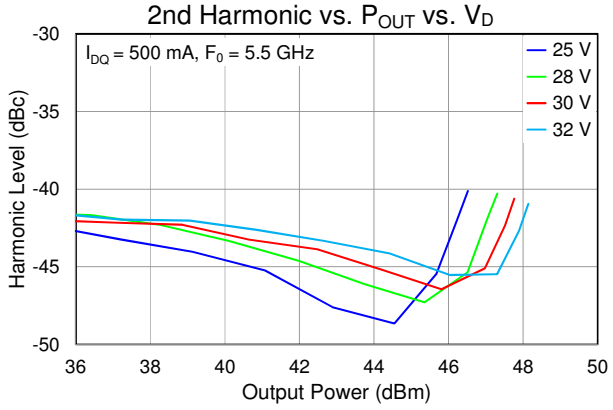
2nd Harmonic vs. P_{OUT} vs. Temp.



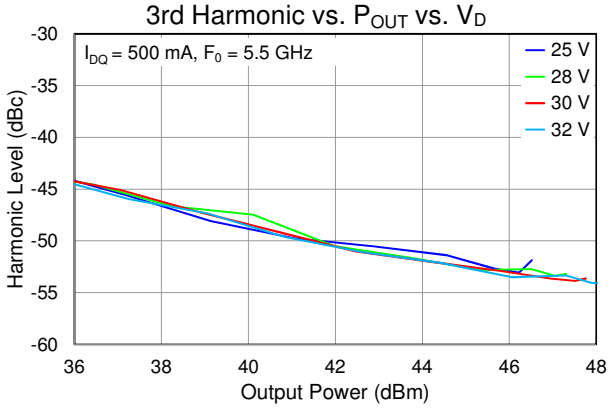
3rd Harmonic vs. P_{OUT} vs. Temp.



2nd Harmonic vs. P_{OUT} vs. V_D



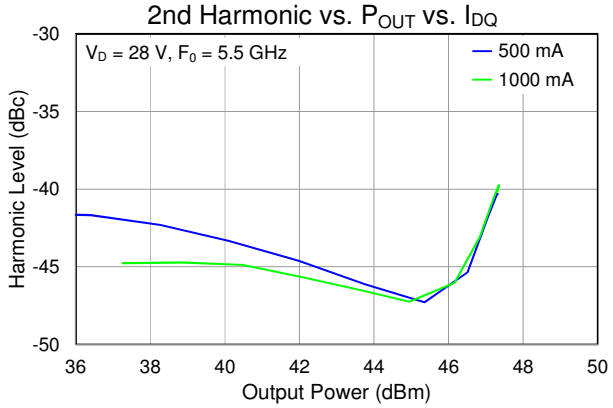
3rd Harmonic vs. P_{OUT} vs. V_D



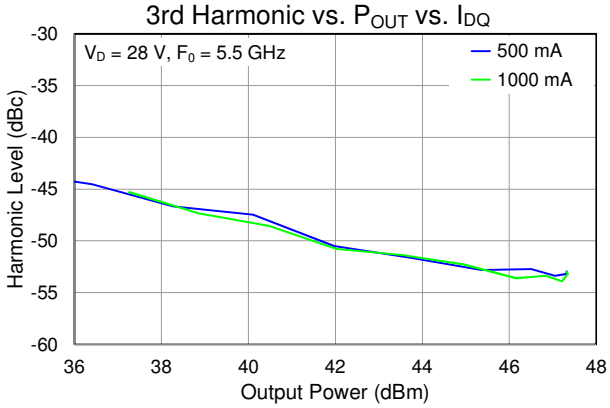
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%

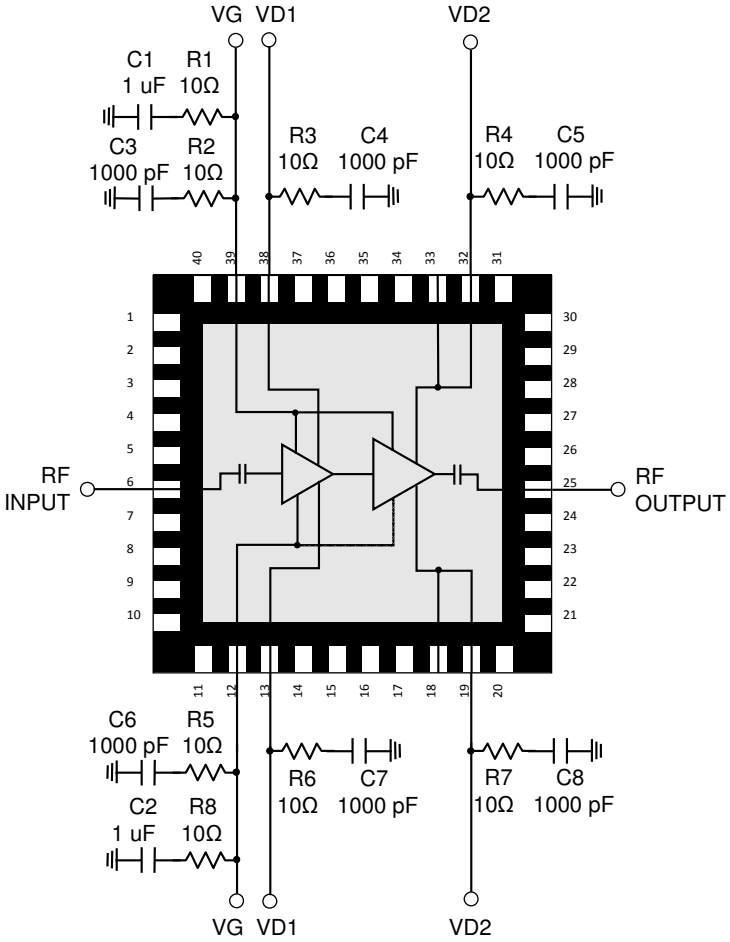
2nd Harmonic vs. P_{OUT} vs. I_{DQ}



3rd Harmonic vs. P_{OUT} vs. I_{DQ}



Application Circuit



Notes:

1. V_G and V_{D1}, V_{D2} must be biased from both sides (top and bottom).
2. V_{D1} and V_{D2} can be connected.

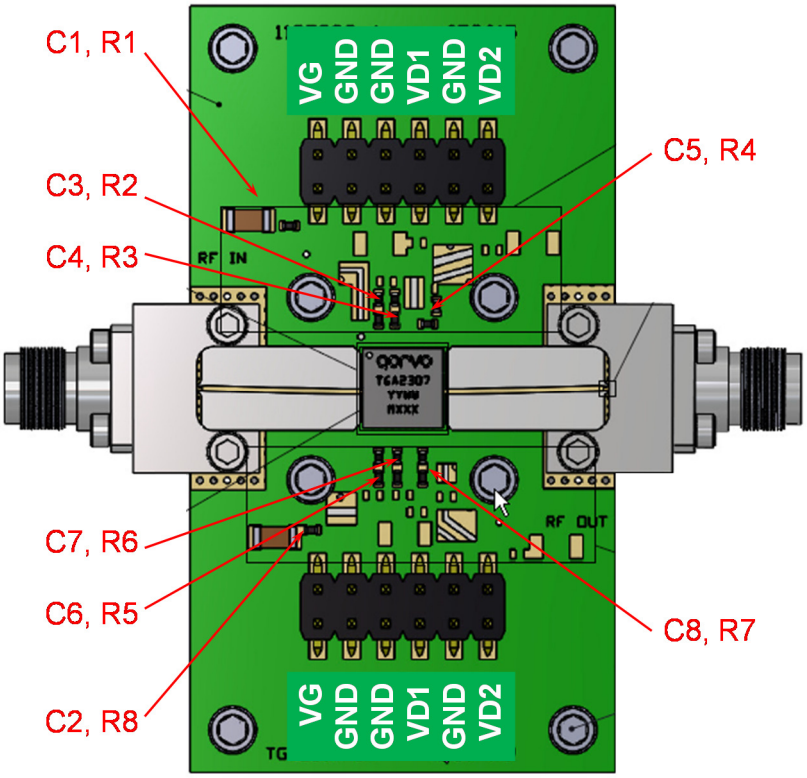
Bias-up Procedure

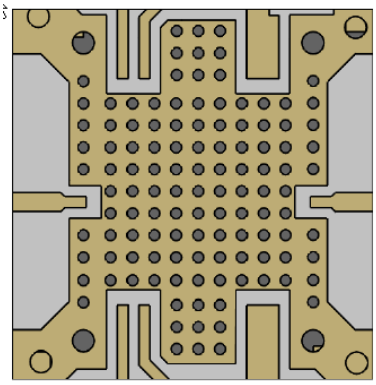
1. Set I_D limit to 6000mA, I_G limit to 140mA
2. Set V_G to -5.0 V
3. Set V_D +28 V
4. Adjust V_G more positive to achieve desired quiescent current (I_{DQ}) (V_G ~ -2.4 V Typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Applications Information – Evaluation Board (EVB)





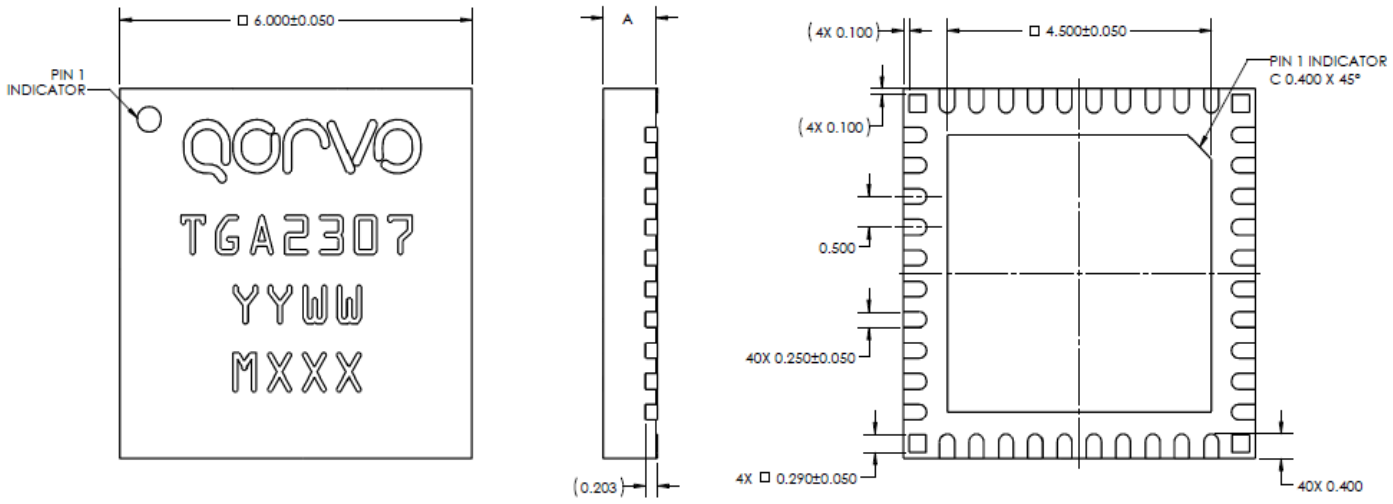
Mounting Detail

RF layer is 0.008" thick Rogers RO4003C, εr= 3.38. Metal layers are 0.5-oz copper. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-01A-5.

Reference Des.	Component	Value	Manufacturer
R1-R8	Surface Mount Res	10 Ohm, 5 % (0402)	Various
C1, C2	Surface Mount Cap	1 uF, 5 %, 50 V (1206), X7R	Various
C3-C8	Surface Mount Cap	1000 pF, 10 %, 100 V (0402), X7R	Various

Note:
Multiple copper-filled vias should be employed under die to minimize inductance and thermal resistance.

Mechanical Drawing and Pad Description



A	MAX	0.900
	NOM	0.850
	MIN	0.800

Units: mm

Tolerances: unless specified

x.xx = ± 0.25

x.xxx = ± 0.127

Materials:

All metalized features are gold plated

Part is mold encapsulated

Marking:

2307: Part number

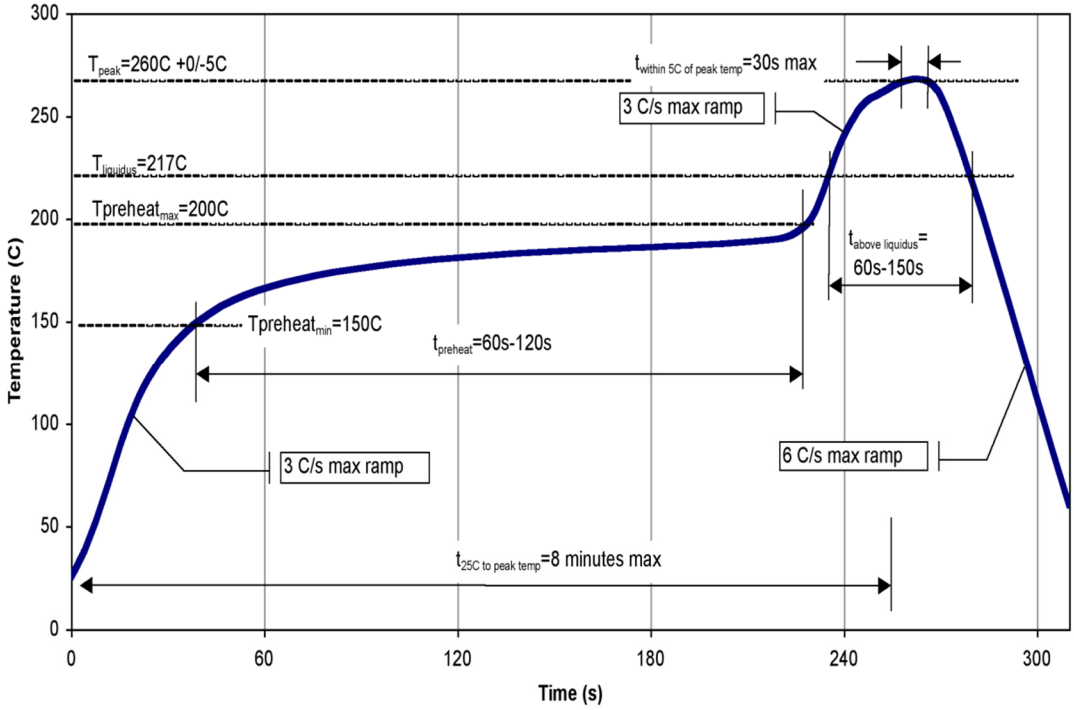
YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

Package Pad	Symbol	Description
1–5, 7–11, 14–17, 20–24, 26–31, 34–37, 40	NC	No connection, recommend to be grounded on PCB
6	RF Input	RF Input, matched to 50 Ω, DC blocked
12, 39	VG	Gate voltage
13, 38	VD1	Drain Voltage, stage 1
18–19, 32–33	VD2	Drain Voltage, stage 2
25	RF Output	RF Output, matched to 50 Ω, DC blocked
41 (center pad)	GND	Ground on PCB, multiple copper-filled vias should be employed under the center pad (41) to minimize inductance and thermal resistance

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: 0B, Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: C2A, Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

Level 3 at 260 °C convection reflow
This part is rated Moisture Sensitive Level 3 at 260 °C per JEDEC standard IPC/JEDEC J-STD-202

ECCN

US Department of Commerce: 3A001.b.2.a.4

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

RoHS-Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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