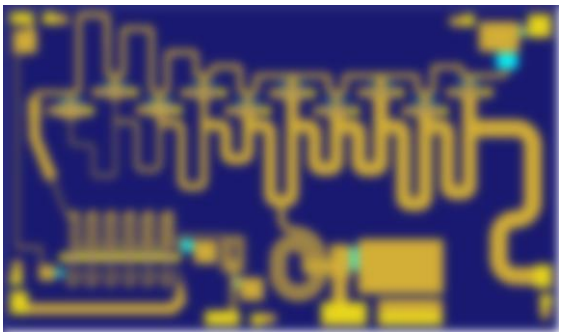
# TGA2214

## 2 – 18 GHz 5 W GaN Power Amplifier



## Product Description

Qorvo's TGA2214 is a wideband power amplifier fabricated on Qorvo's QGaN15 GaN on SiC process. The TGA2214 operates from 2 – 18 GHz and achieves 5 W of saturated output power with 14 dB of large signal gain and greater than 20 % power-added efficiency.

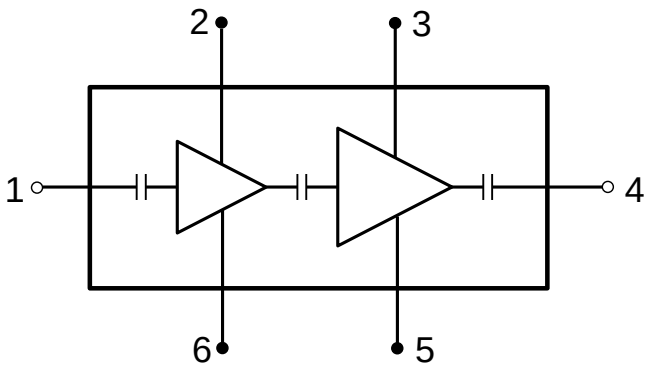
This combination of wideband power, gain and efficiency provides system designers the flexibility to improve system performance while reducing size and cost.

The TGA2214 is matched to 50 Ω with integrated DC blocking capacitors on both RF ports simplifying system integration; it is ideally suited for electronic warfare, test instrumentation and radar applications across both military and commercial markets.

Lead free and RoHS compliant.

Evaluation Boards are available upon request.

## Functional Block Diagram




## Product Features

- Frequency Range: 2 – 18 GHz
- $P_{OUT}$: 37 dBm @ $P_{IN}$ = 23 dBm
- PAE: 20 % @ $P_{IN}$ = 23 dBm
- Large Signal Gain ($P_{IN}$ = 23 dBm): 14 dB
- Small Signal Gain: 22 dB
- Return Loss: 7 dB
- Bias: $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical
- Chip Dimensions: 2.87 x 4.87 x 0.10 mm
- Performance under CW operation

*Performance is typical across frequency. Please reference electrical specification table and data plots for more details.*

## Applications

- Test Equipment
- Electronic Warfare
- Military Radar

## Ordering Information

| Part No. | Description |
|---|---|
| TGA2214 | 2 – 18 GHz 5 W GaN Power Amplifier |

## Electrical Specifications

Test conditions unless otherwise noted: 25 °C, $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical, CW.

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency Range | | 2 | – | 18 | GHz |
| Output Power @ $P_{IN}$ = 23 dBm | Frequency = 2 GHz | – | 37.3 | – | dBm |
| | Frequency = 10 GHz | – | 38.1 | – | |
| | Frequency = 18 GHz | – | 37.6 | – | |
| Power Added Efficiency @ $P_{IN}$ = 23 dBm | Frequency = 2 GHz | – | 22.8 | – | % |
| | Frequency = 10 GHz | – | 21.4 | – | |
| | Frequency = 18 GHz | – | 21.6 | – | |
| Small Signal Gain | Frequency = 2 GHz | – | 25.4 | – | dB |
| | Frequency = 10 GHz | – | 25 | – | |
| | Frequency = 18 GHz | – | 22 | – | |
| Input Return Loss | Frequency = 2 GHz | – | 10.2 | – | dB |
| | Frequency = 10 GHz | – | 11 | – | |
| | Frequency = 18 GHz | – | 13.5 | – | |
| Output Return Loss | Frequency = 2 GHz | – | 9 | – | dB |
| | Frequency = 10 GHz | – | 13.5 | – | |
| | Frequency = 18 GHz | – | 12.5 | – | |
| IM3 ($P_{OUT}$/Tone = 31 dBm/Tone, 100 MHz spacing) | | – | -20 | – | dBc |
| IM5 ($P_{OUT}$/Tone = 31 dBm/Tone, 100 MHz spacing) | | – | -33 | – | dBc |
| Small Signal Gain Temperature Coefficient | | – | -0.04 | – | dB/°C |
| Output Power Temperature Coefficient | | – | -0.008 | – | dBm/°C |

## Recommended Operating Conditions

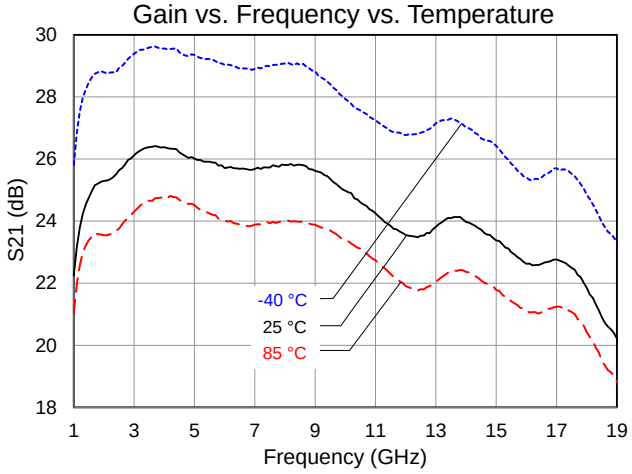
| Parameter | Value / Range |
|---|---|
| Drain Voltage ($V_D$) | +22 V |
| Drain Current ($I_{DQ}$) | 450 mA |
| Gate Voltage ($V_G$) | −2.3 V (Typ.) |
| Temperature ($T_{BASE}$) | −40 to 85 °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

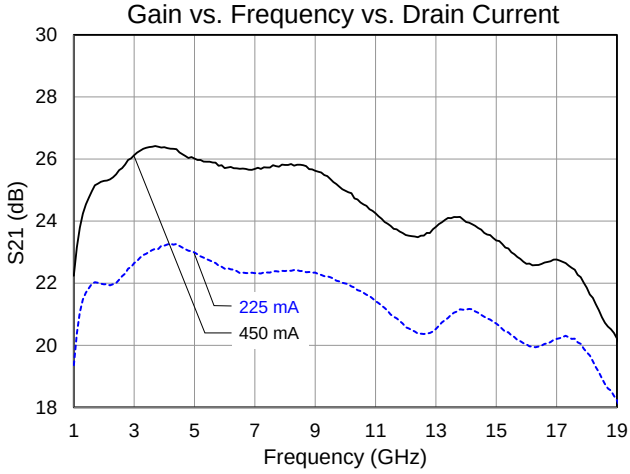
## Performance Plots – Small Signal

Conditions unless otherwise specified: $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical, CW.

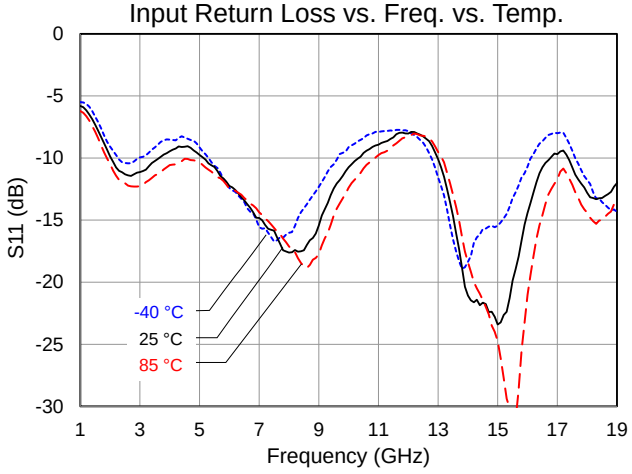
Gain vs. Frequency vs. Temperature



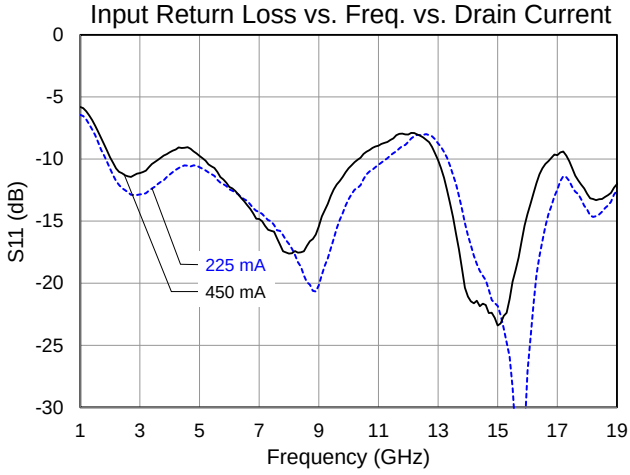

Gain vs. Frequency vs. Drain Current



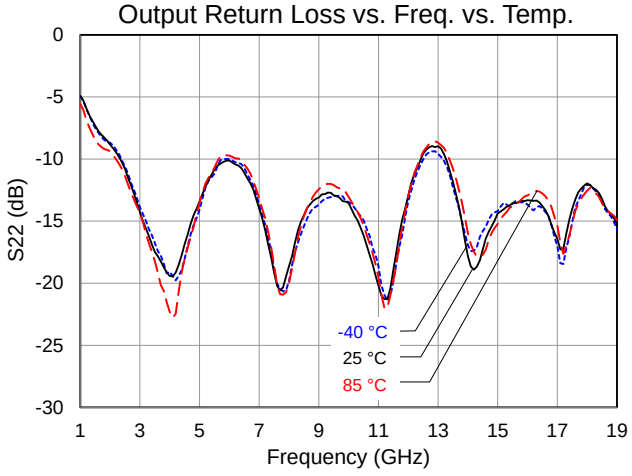

Input Return Loss vs. Freq. vs. Temp.



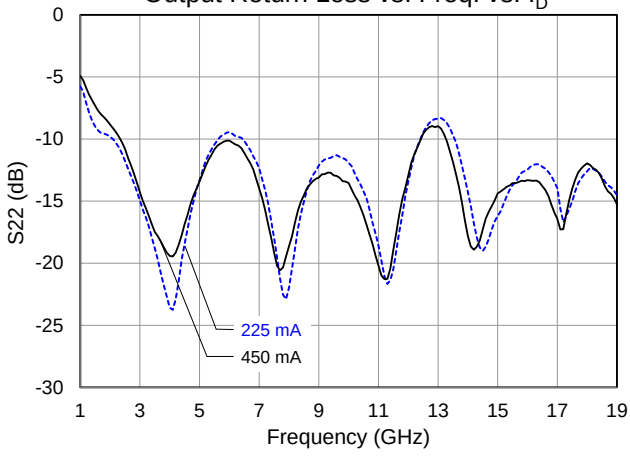

Input Return Loss vs. Freq. vs. Drain Current




Output Return Loss vs. Freq. vs. Temp.



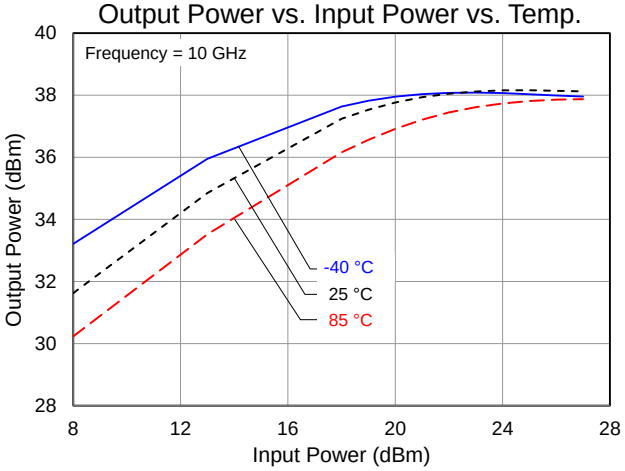

Output Return Loss vs. Freq. vs. $I_D$



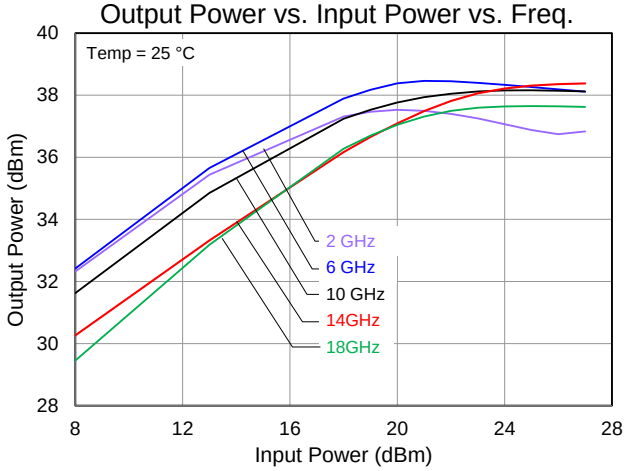
## Performance Plots – Large Signal

Conditions unless otherwise specified: $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical, CW.

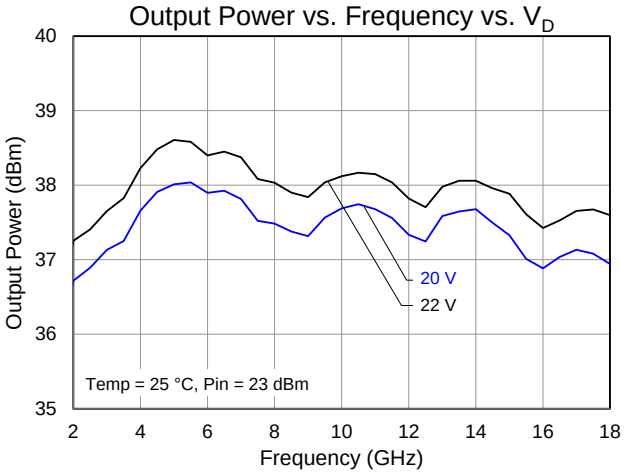
Output Power vs. Input Power vs. Temp.



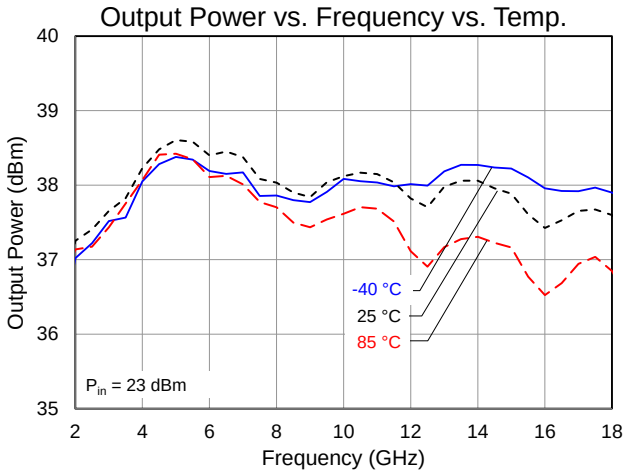

Output Power vs. Input Power vs. Freq.



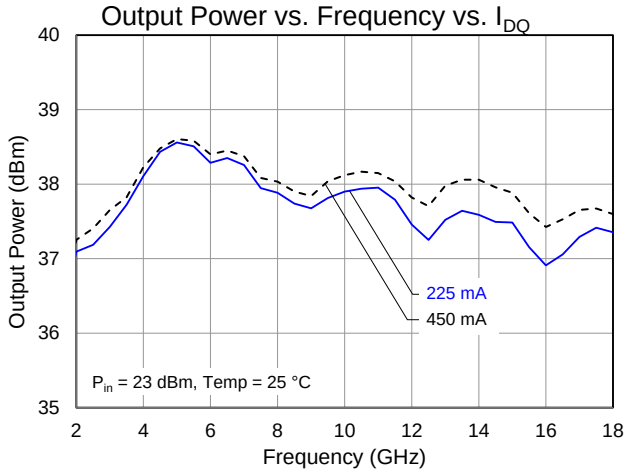

Output Power vs. Frequency vs. $V_D$




Output Power vs. Frequency vs. Temp.



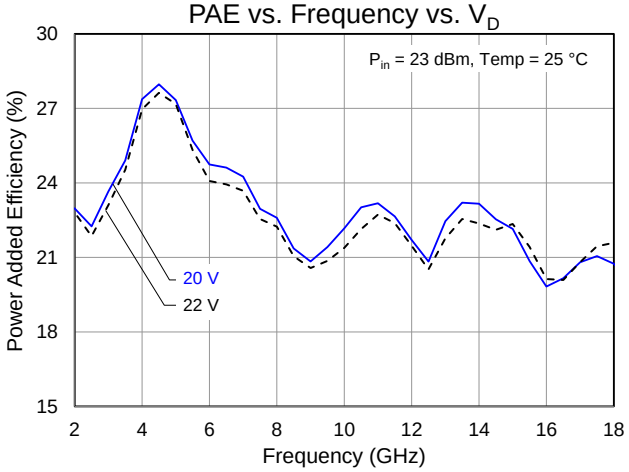

Output Power vs. Frequency vs. $I_{DQ}$



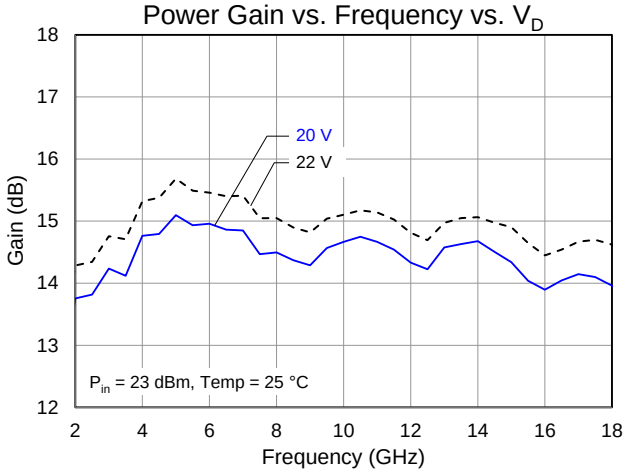
## Performance Plots – Large Signal

Conditions unless otherwise specified: $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical, CW.

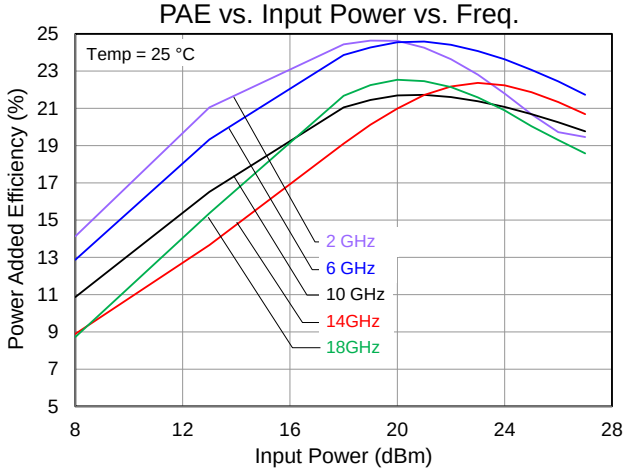
PAE vs. Frequency vs. $V_D$



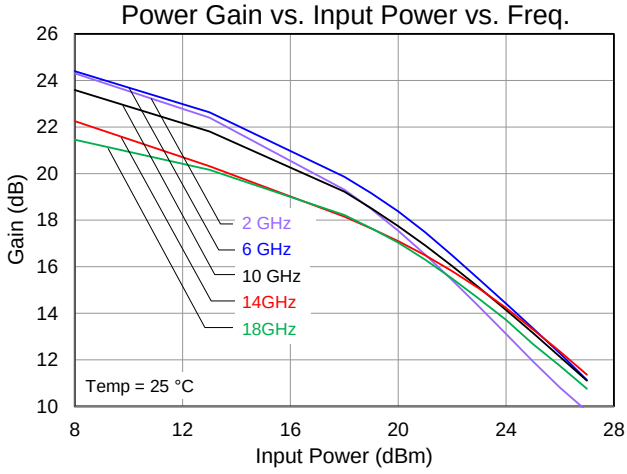

Power Gain vs. Frequency vs. $V_D$



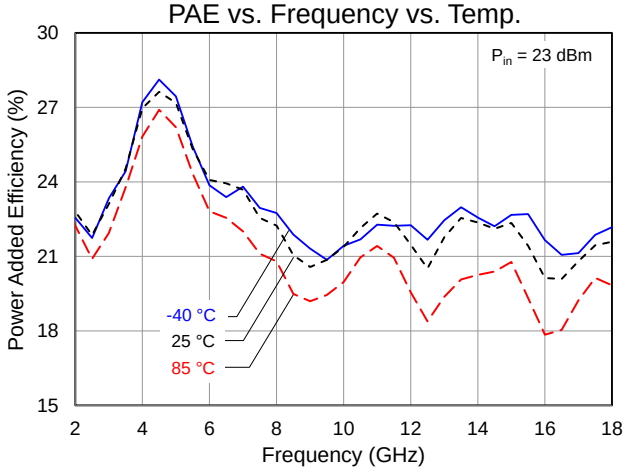

PAE vs. Input Power vs. Freq.



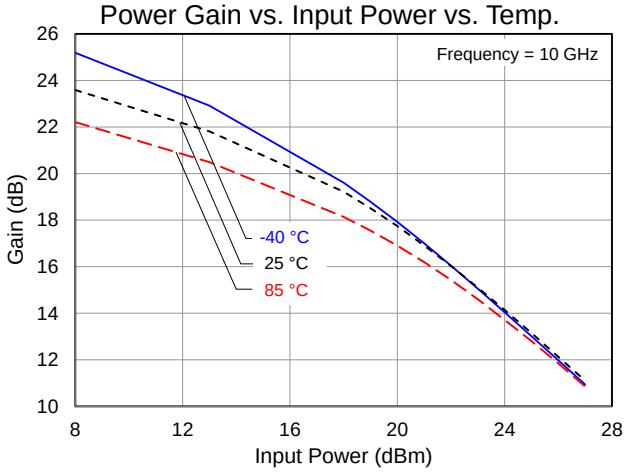

Power Gain vs. Input Power vs. Freq.




PAE vs. Frequency vs. Temp.



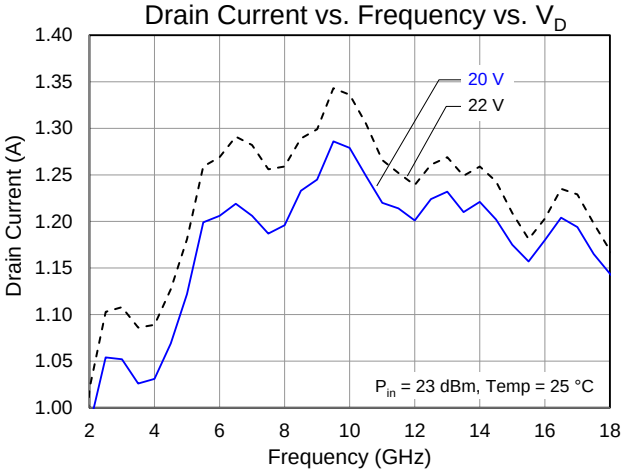

Power Gain vs. Input Power vs. Temp.



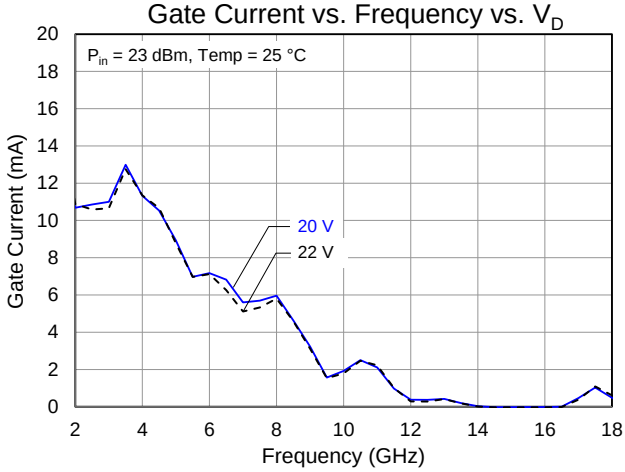
## Performance Plots – Large Signal

Conditions unless otherwise specified: $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical, CW.

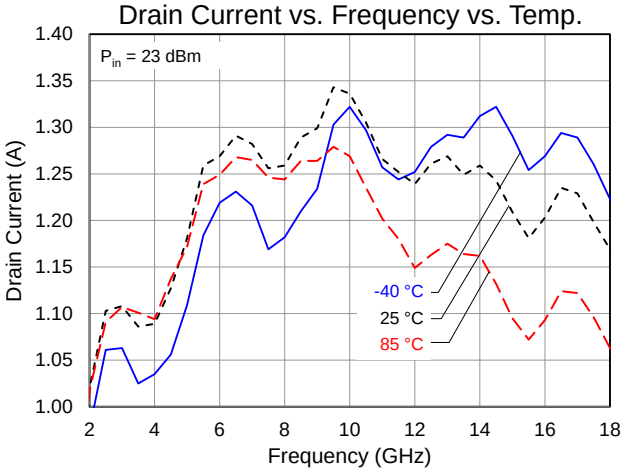
Drain Current vs. Frequency vs. $V_D$



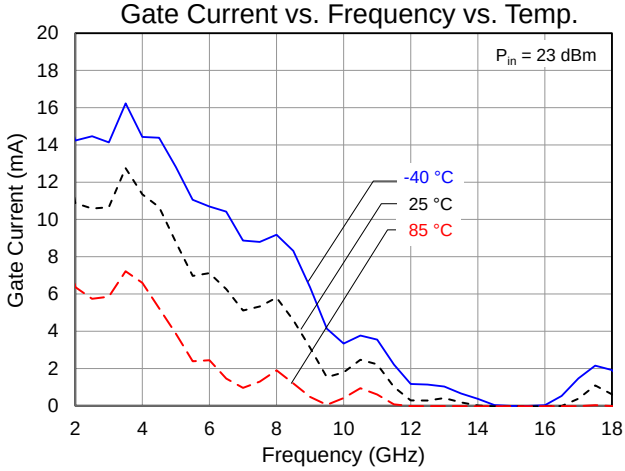

Gate Current vs. Frequency vs. $V_D$



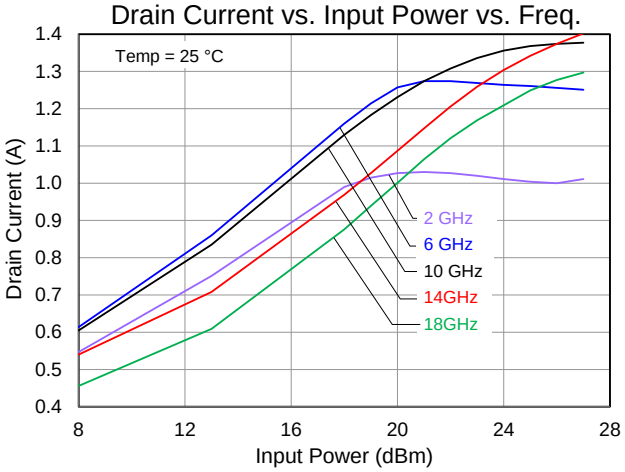

Drain Current vs. Frequency vs. Temp.



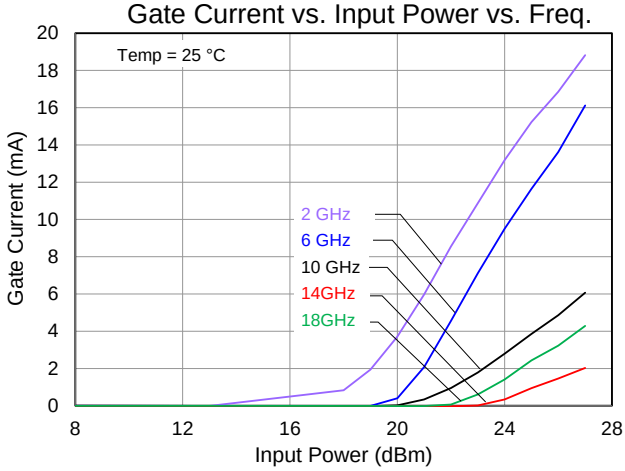

Gate Current vs. Frequency vs. Temp.




Drain Current vs. Input Power vs. Freq.



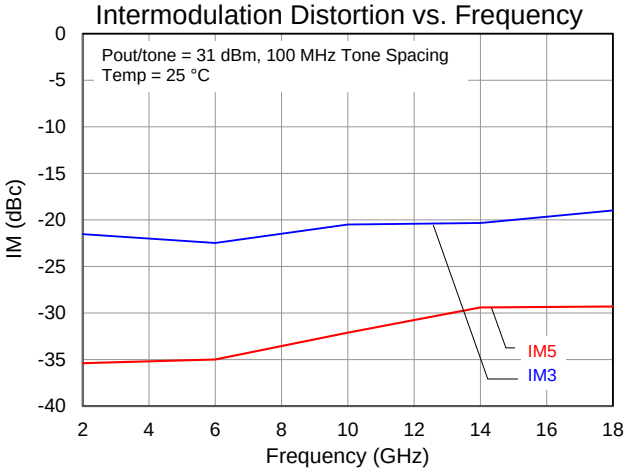

Gate Current vs. Input Power vs. Freq.



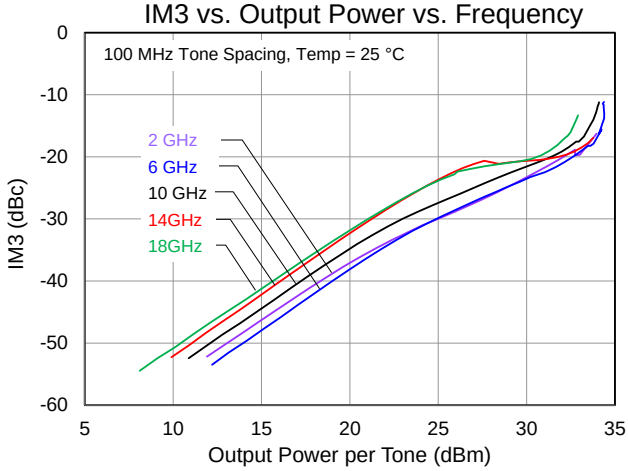
## Performance Plots – Linearity

Conditions unless otherwise specified: $V_D$ = +22 V, $I_{DQ}$ = 450 mA, $V_G$ = −2.3 V Typical, CW.

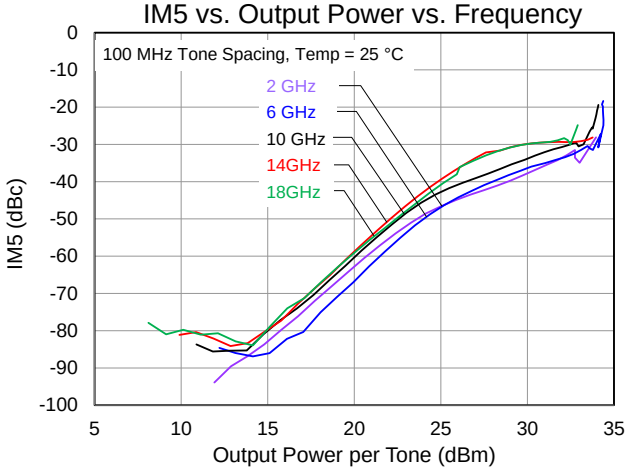
Intermodulation Distortion vs. Frequency



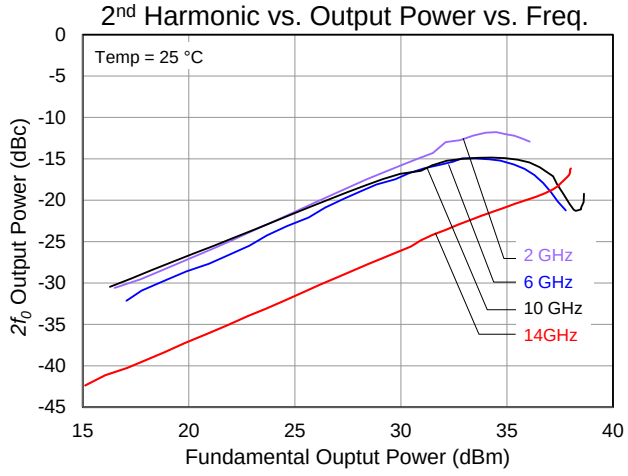

IM3 vs. Output Power vs. Frequency



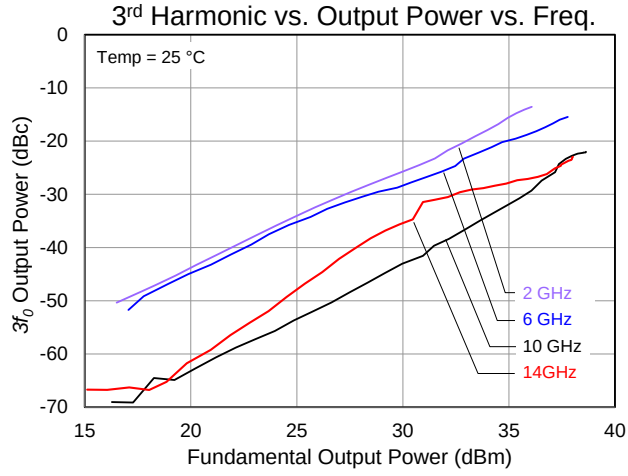

IM5 vs. Output Power vs. Frequency




2nd Harmonic vs. Output Power vs. Freq.




3rd Harmonic vs. Output Power vs. Freq.

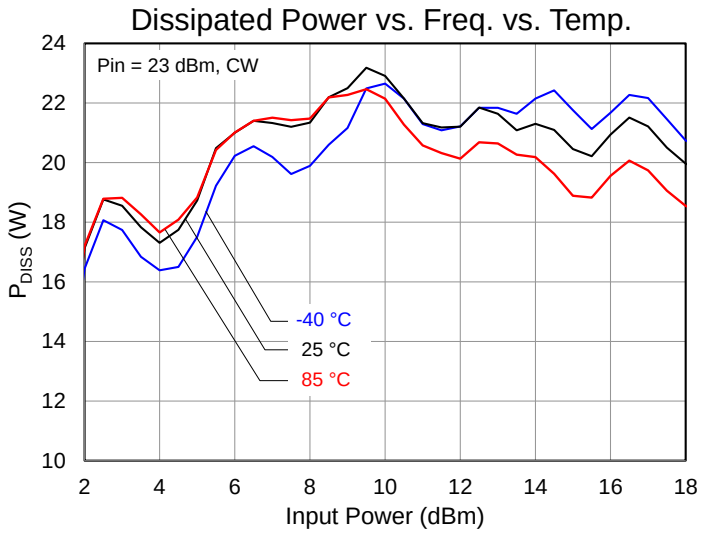


## Thermal and Reliability Information

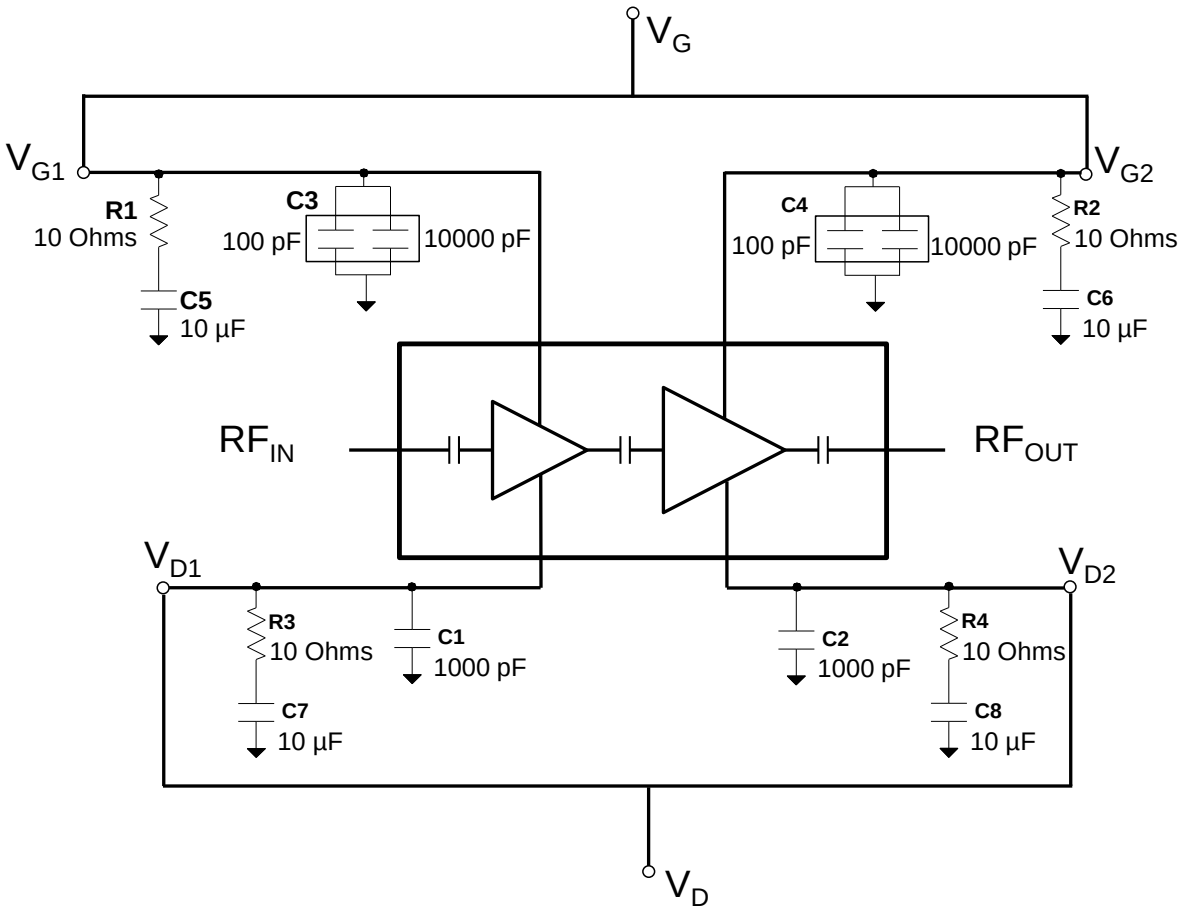
| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85 °C, $V_D$ = +22 V (CW), Freq = 9.5 GHz, $P_{IN}$ = 23 dBm, $I_{DQ}$ = 450 mA, $I_{D\_Drive}$ = 1.28 A, $P_{OUT}$ = 37.5 dBm, $P_{DISS}$ = 22.7 W | 3.92 | °C/W |
| Channel Temperature ($T_{CH}$) (Under RF drive) | | 174 | °C |

Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 20 mils CuMo carrier using AuSn.
2. Refer to the Following Document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Dissipated Power



## Applications Information and Pad Layout



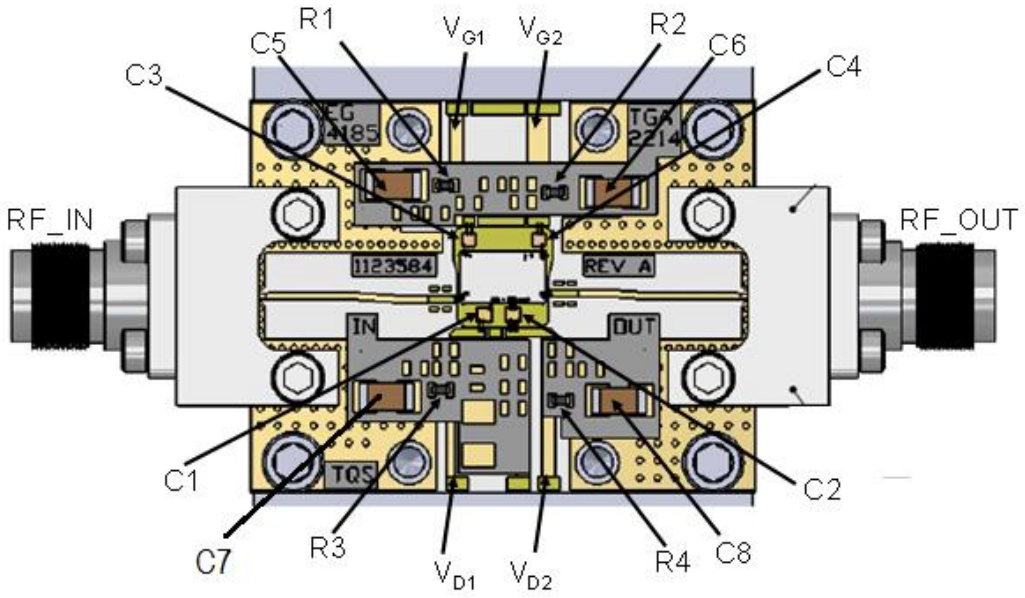

## Bias Up Procedure

| |
|---|
| 1. Set $I_D$ limit to 1.4 A, $I_G$ limit to 20 mA |
| 2. Apply −5 V to $V_G$ |
| 3. Apply +22 V to $V_D$; ensure $I_{DQ}$ is approx. 0 mA |
| 4. Adjust $V_G$ until $I_{DQ}$ = 450 mA ($V_G$ ~ −2.3 V Typ.). |
| 5. Turn on RF supply |

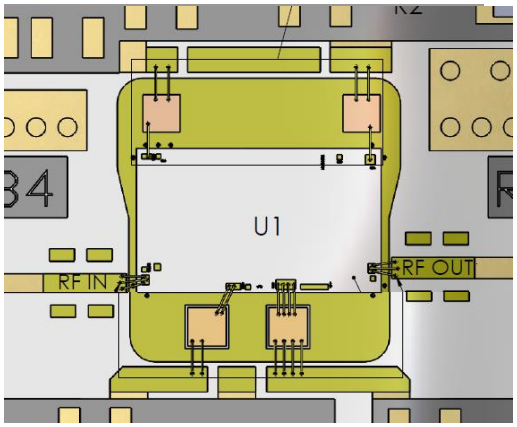
## Bias Down Procedure

| |
|---|
| 1. Turn off RF supply |
| 2. Reduce $V_G$ to −5 V; ensure $I_{DQ}$ is approx. 0 mA |
| 3. Set $V_D$ to 0 V |
| 4. Turn off $V_D$ supply |
| 5. Turn off $V_G$ supply |

## Assembly Drawing



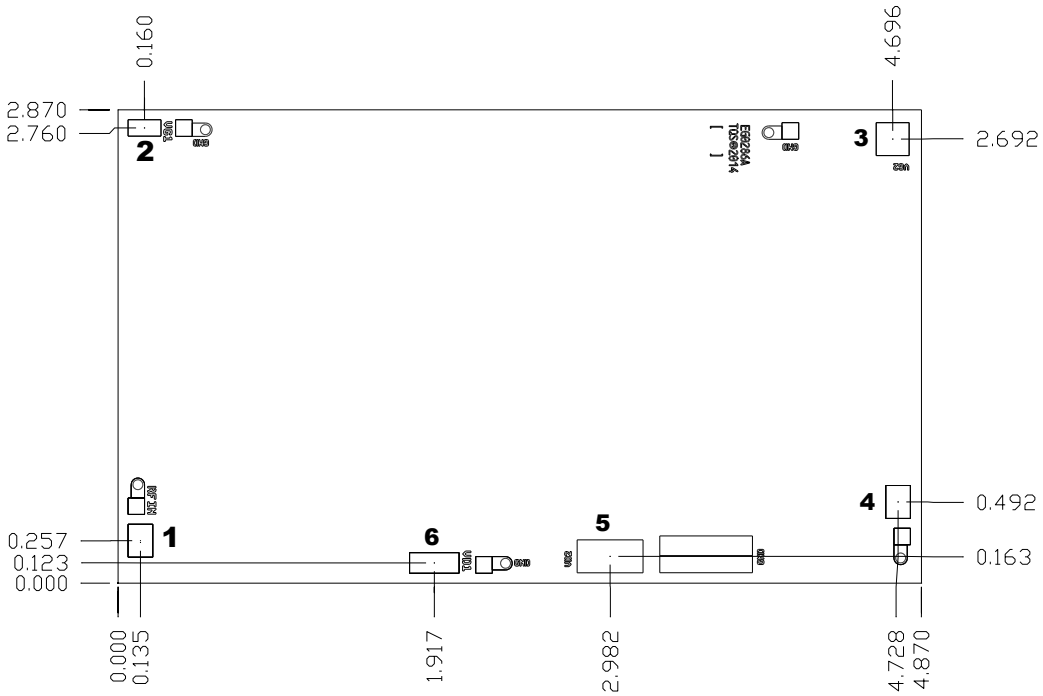

MMIC bonding detail:




## Bill of Materials

| Reference Des. | Value | Description | Manuf. | Part Number |
|---|---|---|---|---|
| C1, C2 | 1000 pF | Cap, +50 V, 10 %, SLCC | Presidio | MSA3535B102K2H5C-F |
| C3, C4 | 100 pF // 10000 pF | Cap, +50 V, 20 %, X7R, MLCC | Presidio | MVB3030X103M2H5C1F |
| C5, C6, C7, C8 | 10 µF | Cap, 1206, 20 %, +50 V, X5R | Various | – |
| R1, R2, R3, R4 | 10 Ohms | Res, 0402, 5 % | Various | – |

## Mechanical Information




Units: millimeters
Thickness: 0.10
Die x,y size tolerance: ± 0.050
Ground is backside of die

## Bond Pad Description

| Pad No. | Symbol | Pad Size (mm) | Description |
|---|---|---|---|
| 1 | RF IN | 0.150 x 0.200 | RF Input; matched to 50 Ω, DC blocked |
| 2 | $V_{G1}$ (1) | 0.200 x 0.100 | Gate voltage for stage 1, bias network is required; see Application Circuit on page 9 as an example. |
| 3 | $V_{G2}$ (1) | 0.200 x 0.200 | Gate voltage for stage 2, bias network is required; see Application Circuit on page 9 as an example. |
| 4 | RF OUT | 0.150 x 0.200 | RF Output; matched to 50 Ω, DC blocked |
| 5 | $V_{D2}$ (2) | 0.400 x 0.200 | Drain voltage for stage 2, bias network is required; see Application Circuit on page 9 as an example |
| 6 | $V_{D1}$ (2) | 0.300 x 0.125 | Drain voltage for stage 1, bias network is required; see Application Circuit on page 9 as an example |

Notes:
1) $V_{G1}$ & $V_{G2}$ may be tied together off-chip.
2) $V_{D1}$ & $V_{D2}$ may be tied together off-chip

## Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

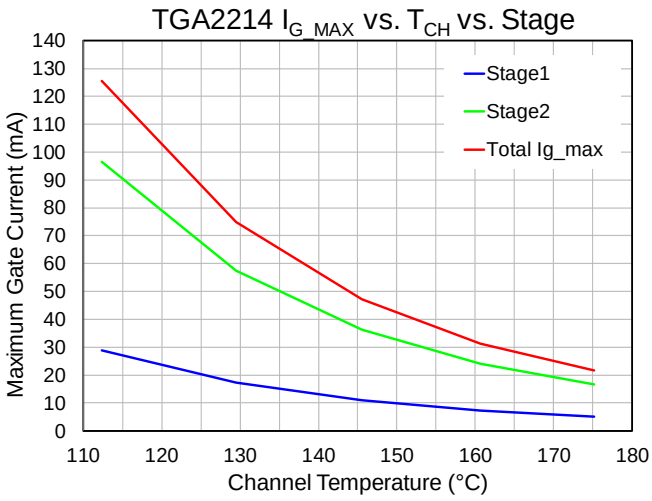
- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.

Devices with small pad sizes should be bonded with 0.0007-inch wire.

## Absolute Maximum Ratings

| Parameter | Value / Range |
|---|---|
| Drain Voltage ($V_D$) | +29.5 V |
| Gate Voltage Range ($V_G$) | −5 to 0 V |
| Drain Current<br>- 1st Stage ($I_{D1}$)<br>- 2nd Stage ($I_{D2}$) | <br>0.5 A<br>1.0 A |
| Gate Current:<br>- 1st Stage ($I_{G1}$)<br>- 2nd Stage ($I_{G2}$) | See $I_{G\_MAX}$ plot |
| Power Dissipation ($P_{DISS}$), 85 °C | 30 W |
| Input Power, CW, 50 Ω, 85 °C ($P_{IN}$) | 31 dBm |
| Input Power, CW, VSWR 3:1, 85 °C ($P_{IN}$) | 31 dBm |
| Mounting Temperature (30 Seconds) | 320 °C |
| Storage Temperature | −55 to +150 °C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.



## Handling Precautions

| Parameter | Rating | Standard |
|---|---|---|
| ESD – Human Body Model (HBM) | TBD | JEDEC Standard JESD22 A114 |

Caution!
ESD-Sensitive Device

## Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

## RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qorvo Green

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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**Tel: 1-844-890-8163**

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