QPA3055D

100 W S-Band GaN Power Amplifier

Product Overview

Qorvo's QPA3055D is a high-power, S-band amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process (QGaN25). Covering 2.9 – 3.6 GHz, the QPA3055D provides 100 W of saturated output power and 25 dB of large-signal gain while achieving 58% power-added efficiency.

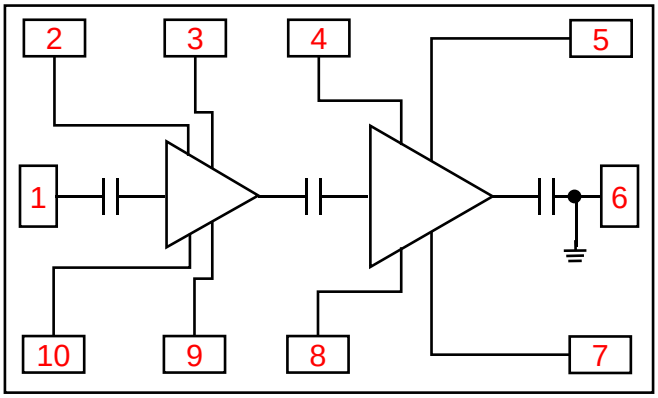
The QPA3055D can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under both short and long pulse operations.

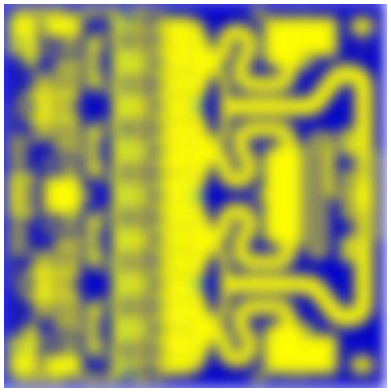
The QPA3055D MMIC has DC blocking capacitors on both
RF ports, which are matched to 50 ohms. The QPA3055D is ideal for both commercial and military radar systems.

Lead-free and RoHS compliant.

Evaluation board available on request.

Functional Block Diagram





Key Features

- Frequency Range: 2.9 – 3.6 GHz
- P_{SAT} (P_{IN}=25 dBm): > 50 dBm
- PAE (P_{IN}=25 dBm): > 58 %
- Power Gain (P_{IN}=25 dBm): > 25 dB
- Bias: V_D = 30 V, I_{DQ} = 300 mA, V_G = −2.5 V typical
- Characterized at PW = 15 ms, DC = 30%, and PW = 100 us, DC = 10%
- Chip Dimensions: 4.890 x 4.890 x 0.100 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Radar

Ordering Information

Part No.	Description
QPA3055D	100 W S-Band GaN Power Amplifier (10 Pcs.)
QPA3055DS2	Samples (2 pcs.)
QPA3055DEVB	Evaluation Board for QPA3055D

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	−8 to +1 V
Peak Drain Current (I_D)	11.7 A
Average Drain Current (I_D)	5.7 A
Duty Cycle	50%
Gate Current (I_G)	See chart, pg. 12
Power Dissipation (P_{DISS}), 85°C	150 W
Input Power (P_{IN}), Pulsed (15ms,30%), 50Ω, V_D=28V, I_{DQ}=300mA, 85 °C	31 dBm
Input Power (P_{IN}), Pulsed (15ms,30%), 3:1 VSWR, V_D=28V, I_{DQ}=300mA, 85 °C	31 dBm
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	−65 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	30 V
Drain Current (I_{DQ})	300 mA
Gate Voltage (V_G), Typical	−2.5 V
Operating Temperature	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

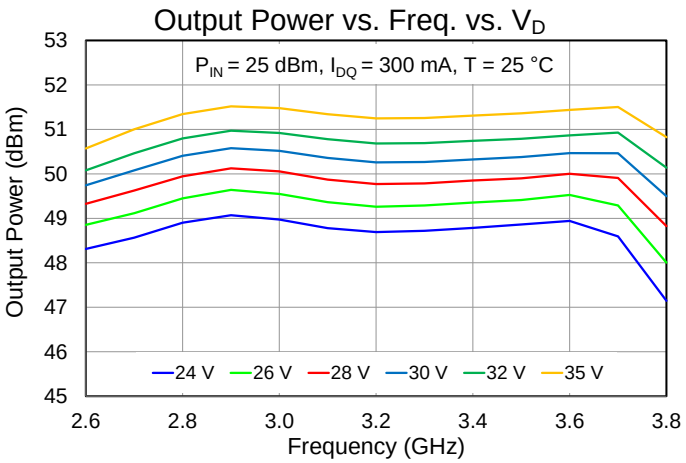
Electrical Specifications

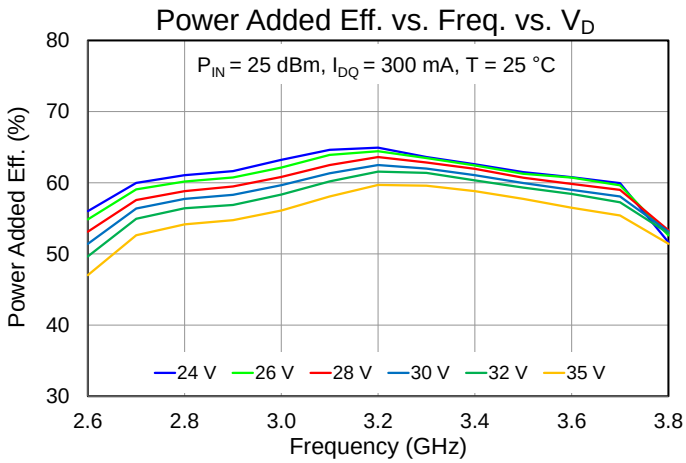
Parameter		Min	Typ	Max	Units
Operational Frequency Range		2.9		3.6	GHz
Output Power (P_{IN} = 25 dBm)	2.9 GHz 3.2 GHz 3.6 GHz		50.6 50.3 50.5		dBm dBm dBm
Power Added Efficiency (P_{IN} = 25 dBm)	2.9 GHz 3.2 GHz 3.6 GHz		58.3 62.5 59.0		% % %
Small Signal Gain (CW)	2.9 GHz 3.2 GHz 3.6 GHz		32.1 32.5 29.8		dB dB dB
Input Return Loss (CW)	2.9 GHz 3.2 GHz 3.6 GHz		13 11 16		dB dB dB
Output Return Loss (CW)	2.9 GHz 3.2 GHz 3.6 GHz		7 8 13		dB dB dB
Output Power Temp. Coeff. (85 – 25 °C, P_{IN} = 25 dBm))			−0.001		dB/°C
Sm. Signal Gain Temperature Coefficient (85 to −40 °C)			−0.057		dB/°C

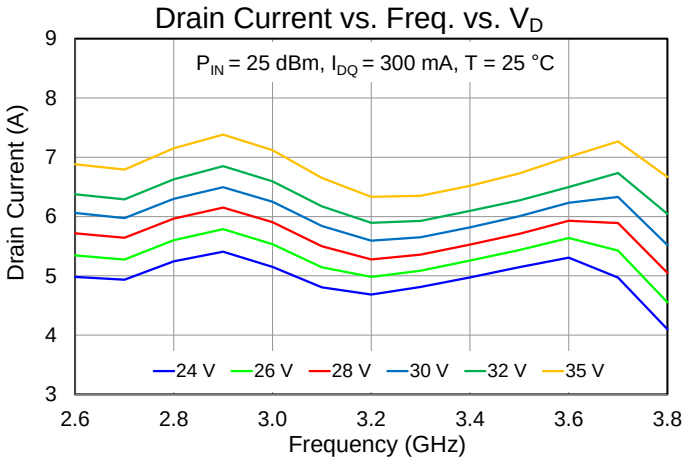
Test conditions, unless otherwise noted: T = 25 °C, V_D = 30 V, I_{DQ} = 300 mA, V_G = −2.5 V Typical, PW = 15 ms, Duty Cycle = 30%

Performance Plots – Large Signal (PW = 15 ms , Duty Cycle = 30%)

Test conditions unless otherwise noted: PW = 15 ms , Duty Cycle = 30%, T= +25 °C







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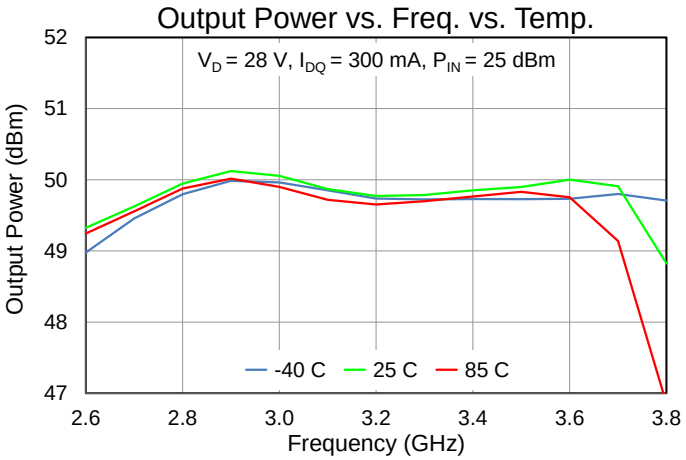
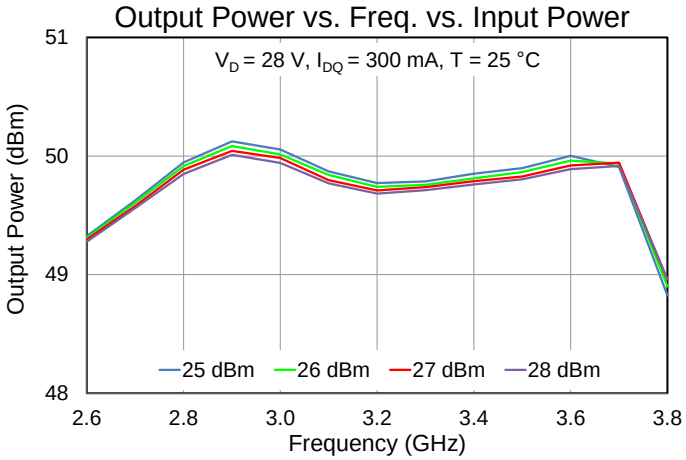
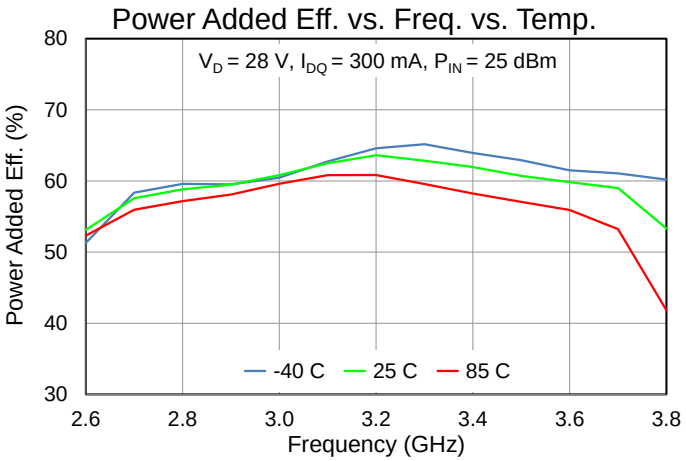
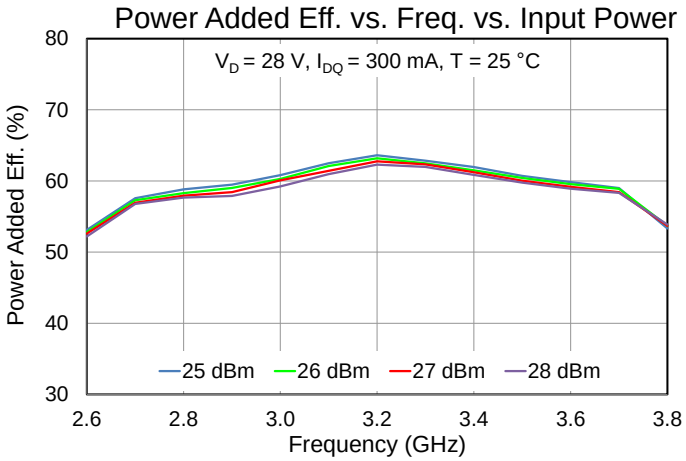
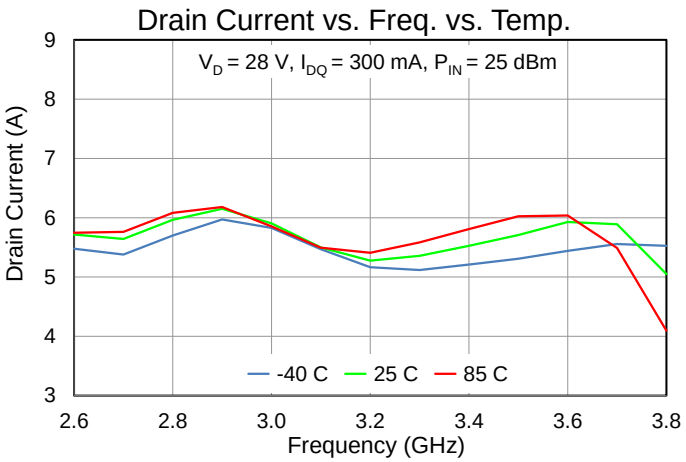
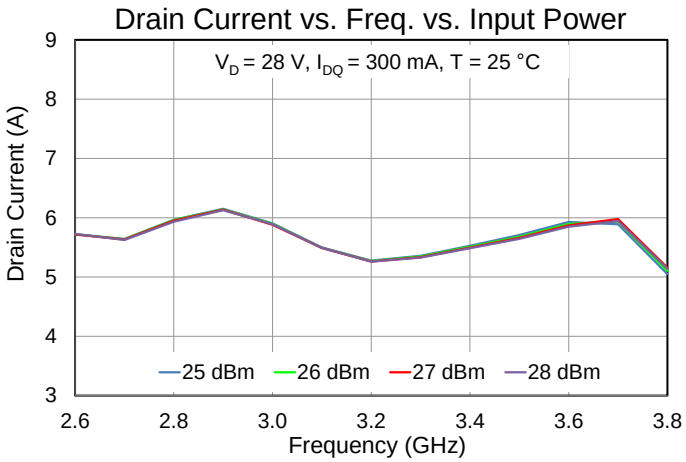








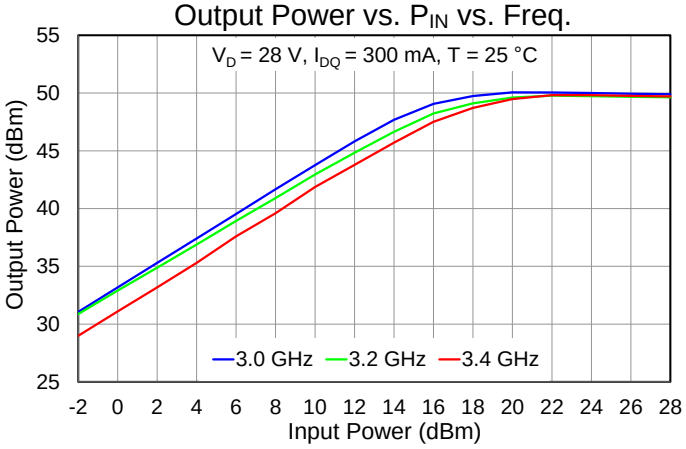




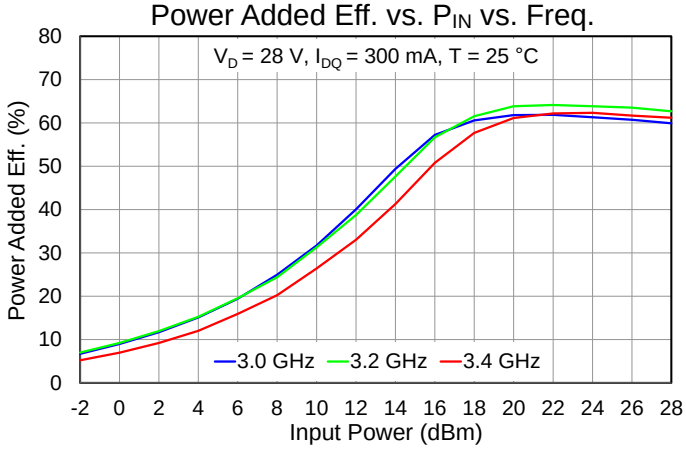
Performance Plots – Large Signal (PW = 15 ms , Duty Cycle = 30%)

Test conditions unless otherwise noted: PW = 15 ms , Duty Cycle = 30%

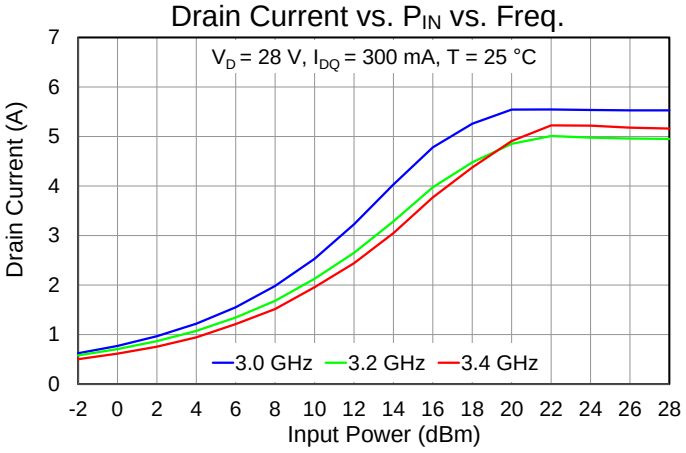
Output Power vs. P_{IN} vs. Freq.



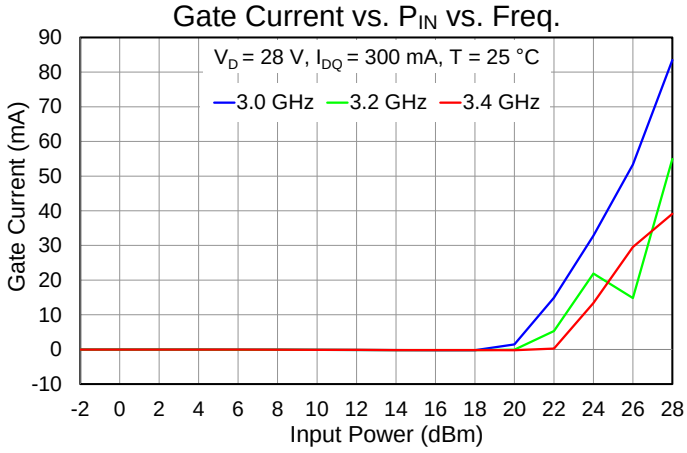
Power Added Eff. vs. P_{IN} vs. Freq.



Drain Current vs. P_{IN} vs. Freq.



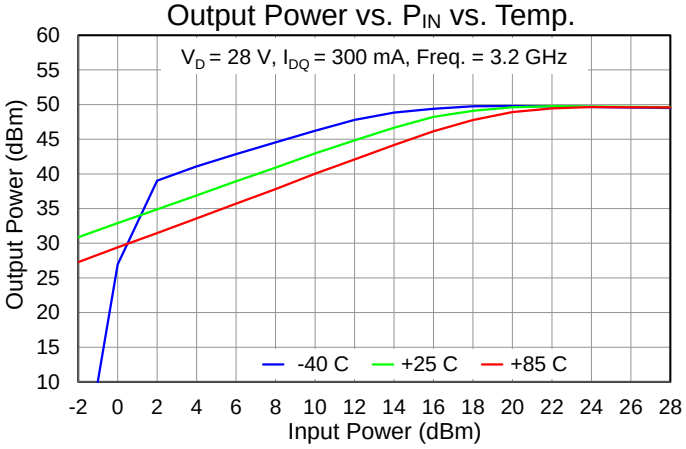
Gate Current vs. P_{IN} vs. Freq.



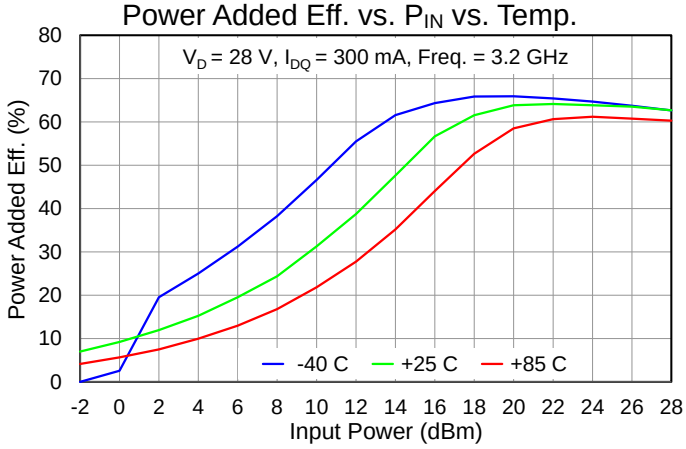
Performance Plots – Large Signal (PW = 15 ms , Duty Cycle = 30%)

Test conditions unless otherwise noted: PW = 15 ms , Duty Cycle = 30%

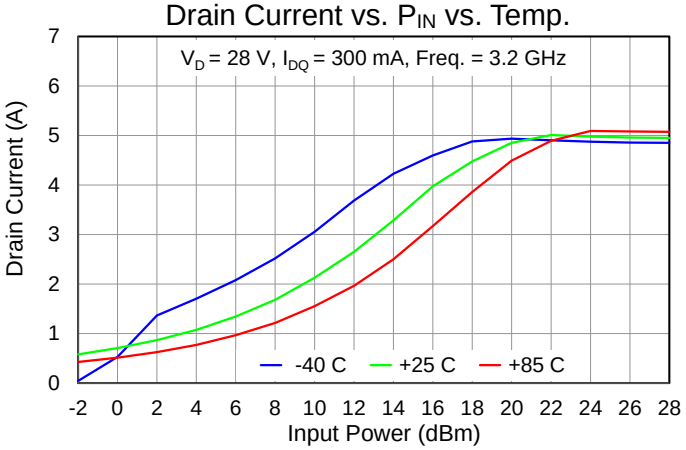
Output Power vs. P_{IN} vs. Temp.



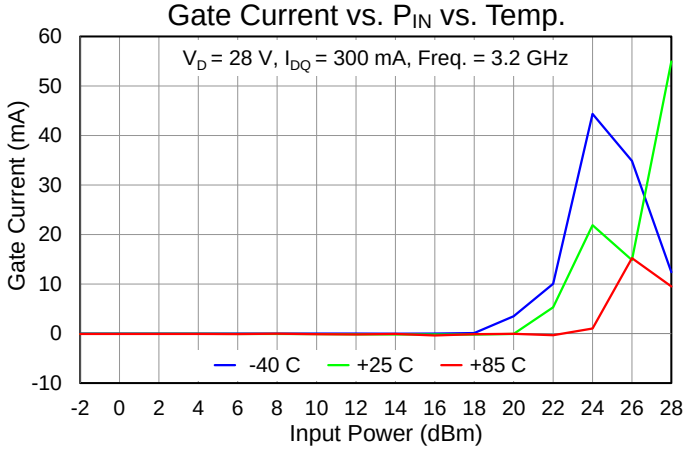
Power Added Eff. vs. P_{IN} vs. Temp.



Drain Current vs. P_{IN} vs. Temp.

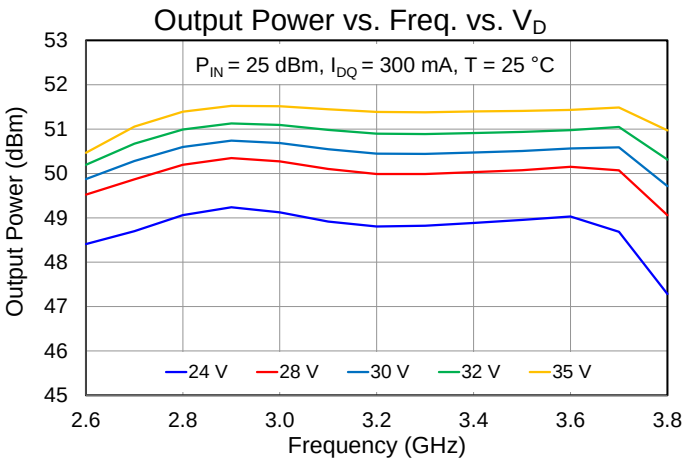


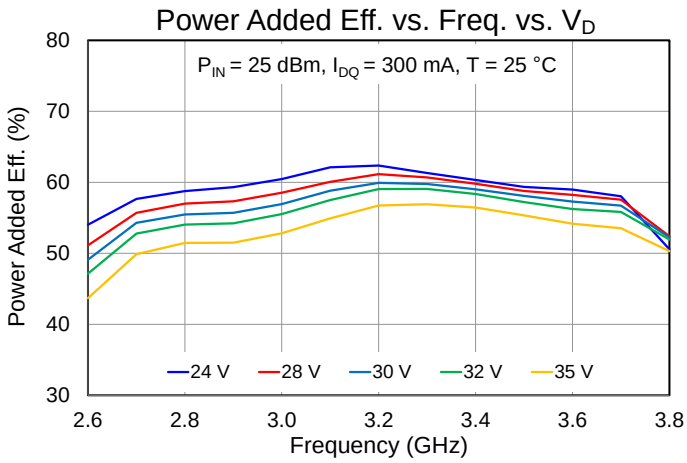
Gate Current vs. P_{IN} vs. Temp.

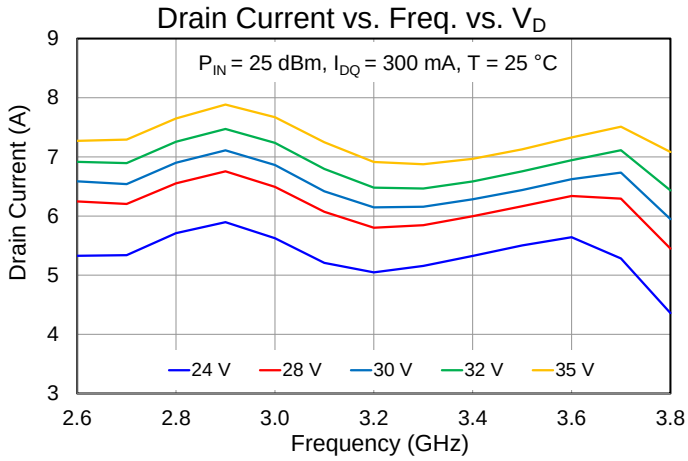


Performance Plots – Large Signal (PW = 100 us , Duty Cycle = 10%)

Test conditions unless otherwise noted: PW = 100 us , Duty Cycle = 10%

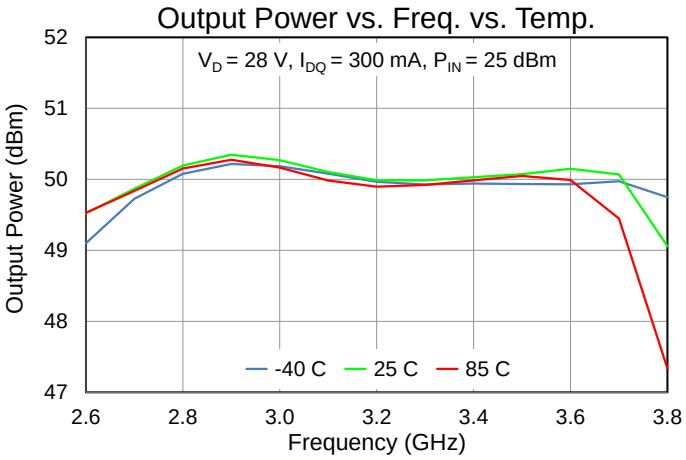


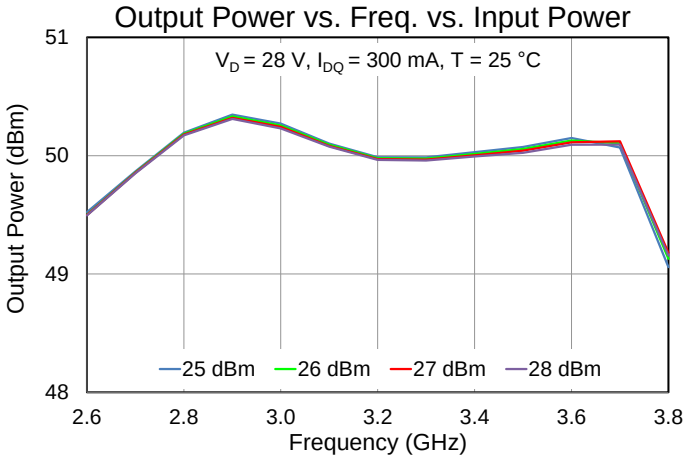


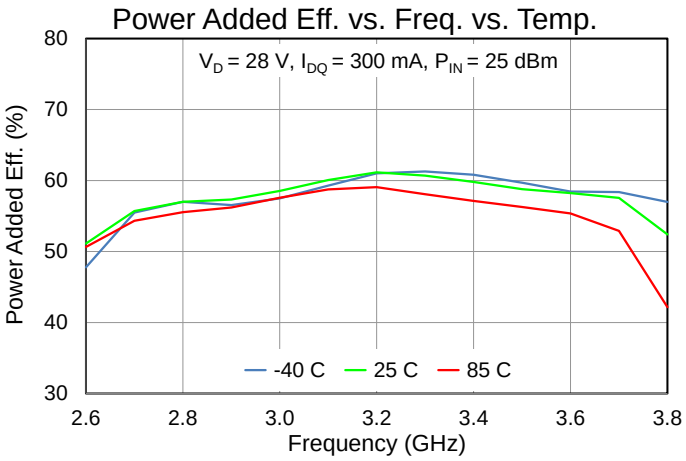


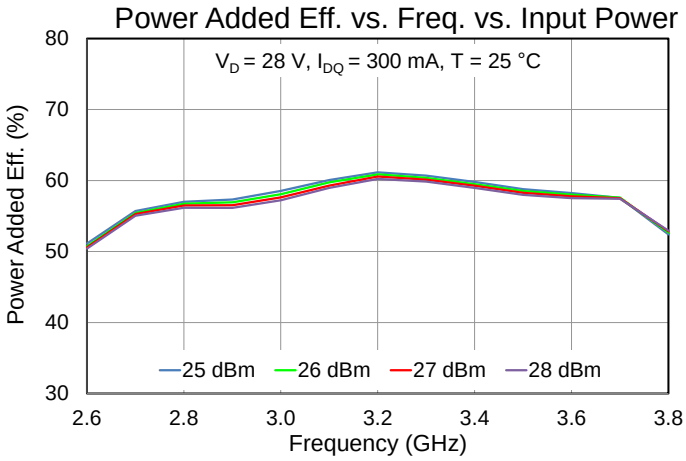
Performance Plots – Large Signal (PW = 100 us , Duty Cycle = 10%)

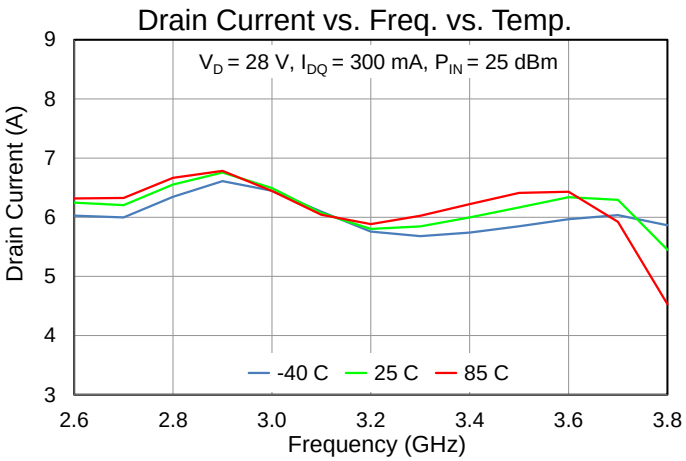
Test conditions unless otherwise noted: PW = 100 us , Duty Cycle = 10%

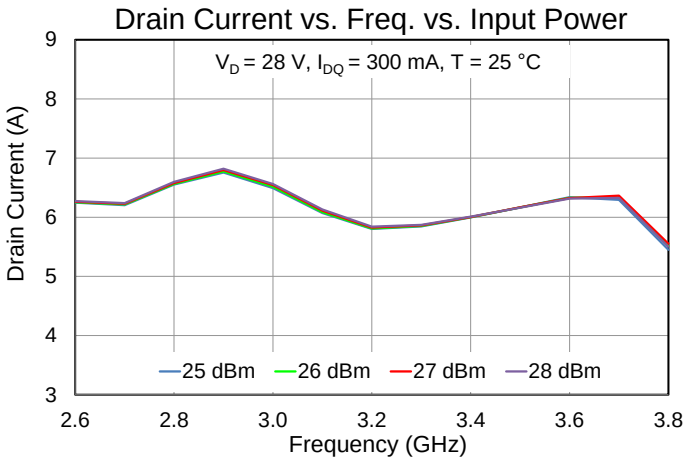








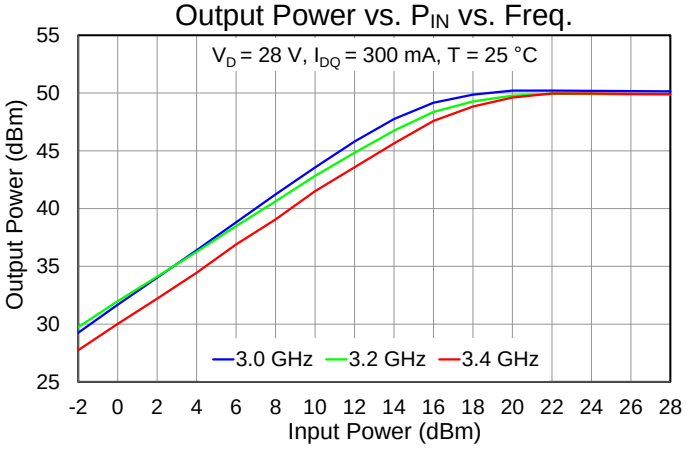




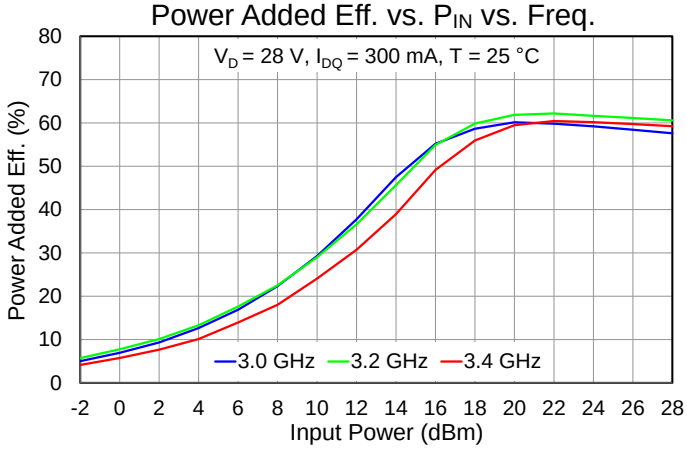
Performance Plots – Large Signal, Harmonics (PW = 100 us , Duty Cycle = 10%)

Test conditions unless otherwise noted: PW = 100 us , Duty Cycle = 10%

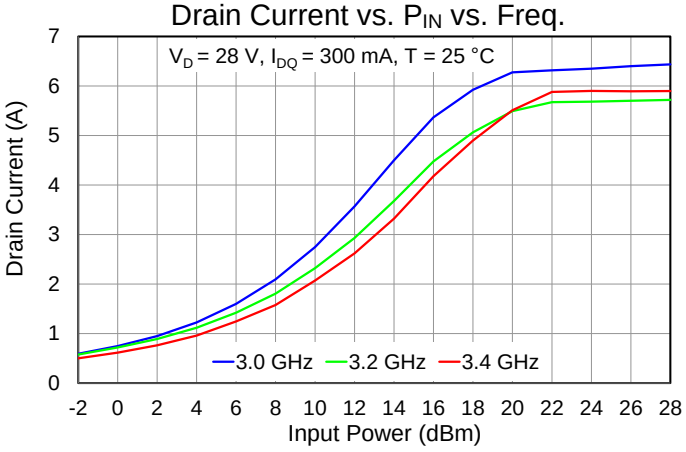
Output Power vs. P_{IN} vs. Freq.



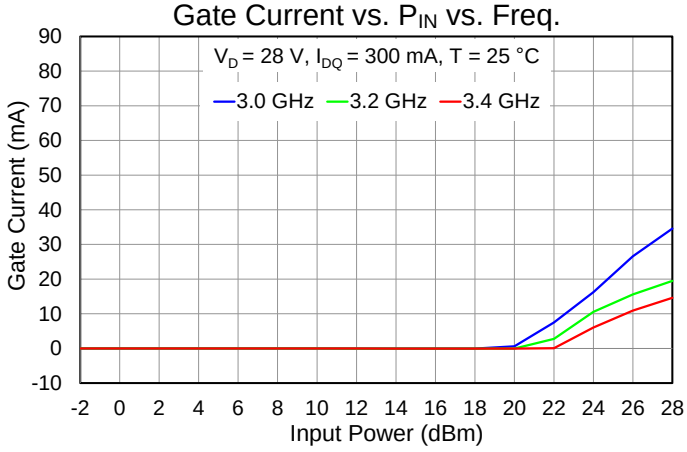
Power Added Eff. vs. P_{IN} vs. Freq.



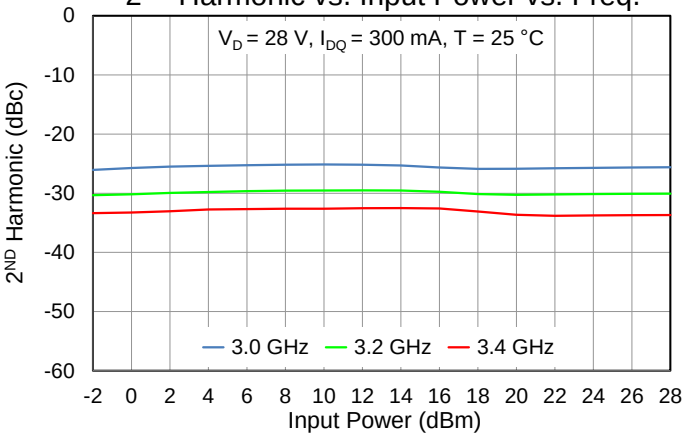
Drain Current vs. P_{IN} vs. Freq.



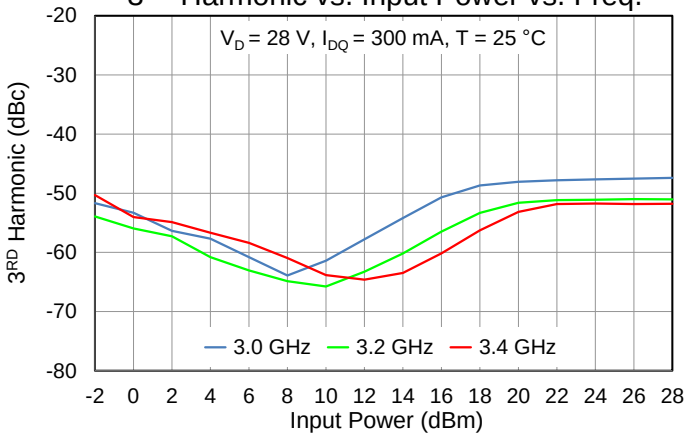
Gate Current vs. P_{IN} vs. Freq.



2^{ND} Harmonic vs. Input Power vs. Freq.

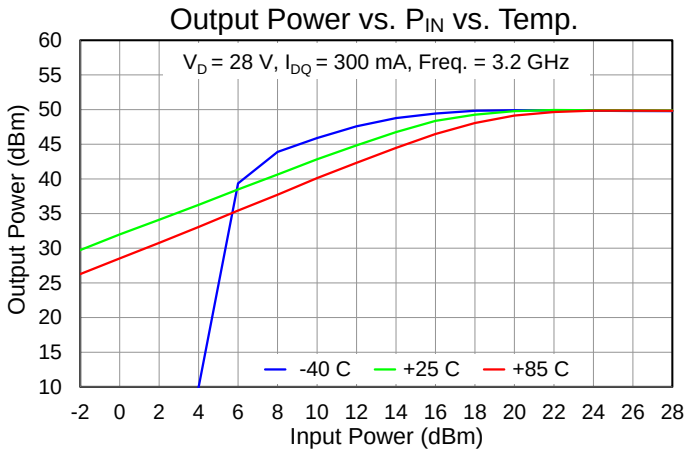


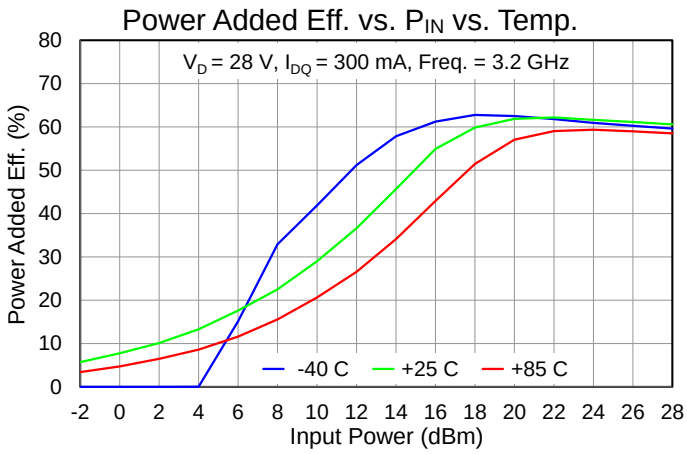
3^{RD} Harmonic vs. Input Power vs. Freq.

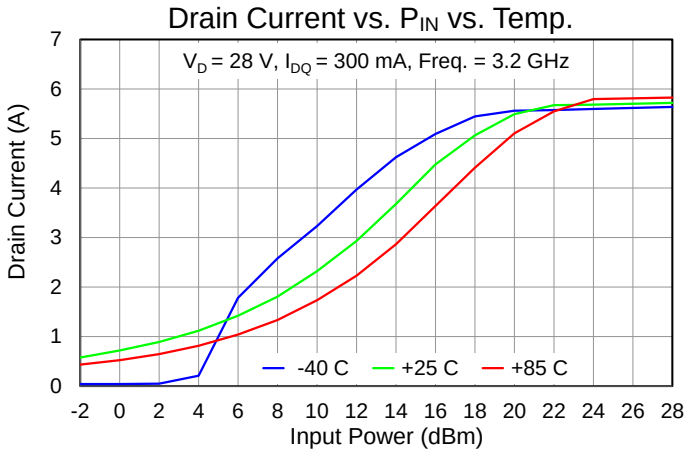


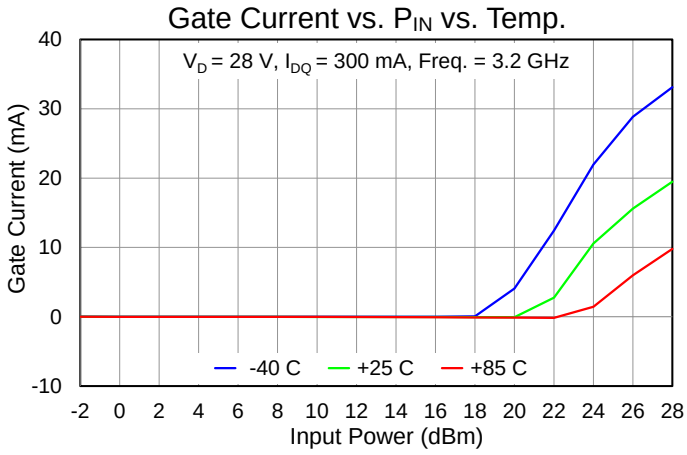
Performance Plots – Large Signal (PW = 100 us , Duty Cycle = 10%)

Test conditions unless otherwise noted: PW = 100 us , Duty Cycle = 10%





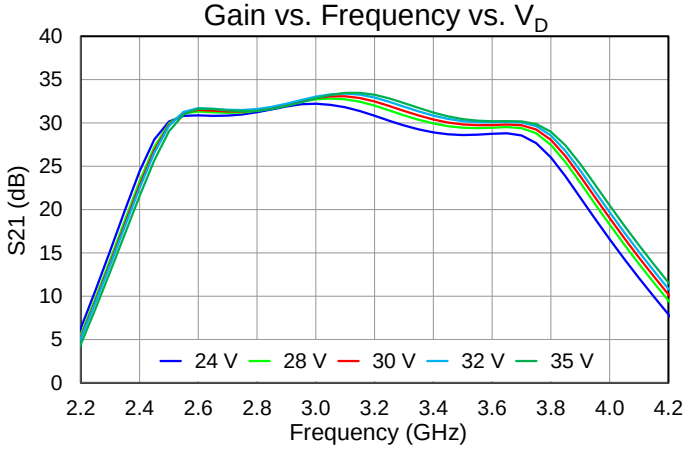




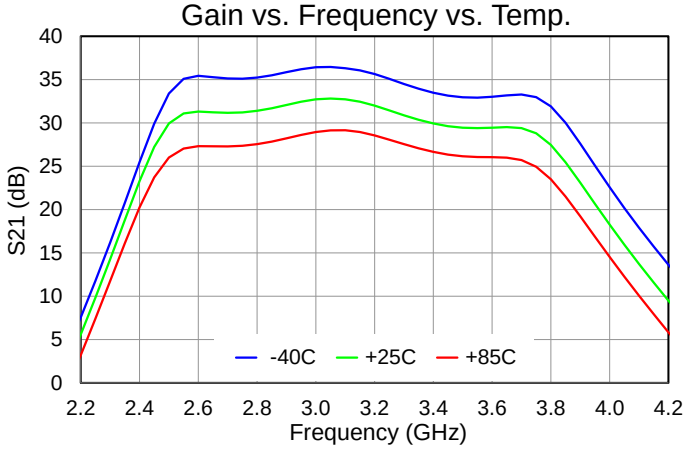
Performance Plots – Small Signal (CW)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 300 mA, CW input power, T=+25 °C

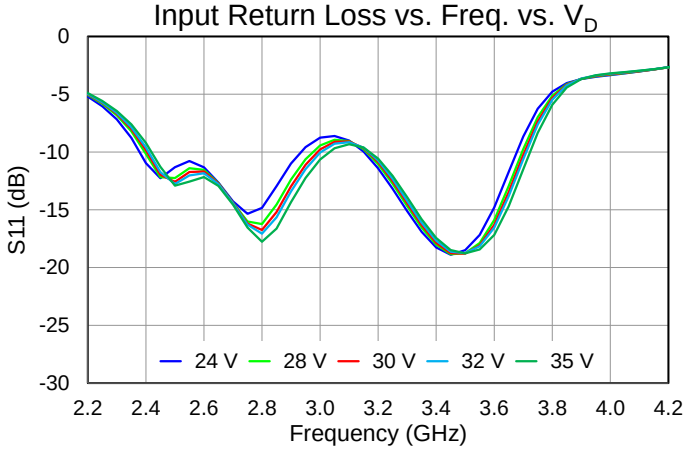
Gain vs. Frequency vs. V_D



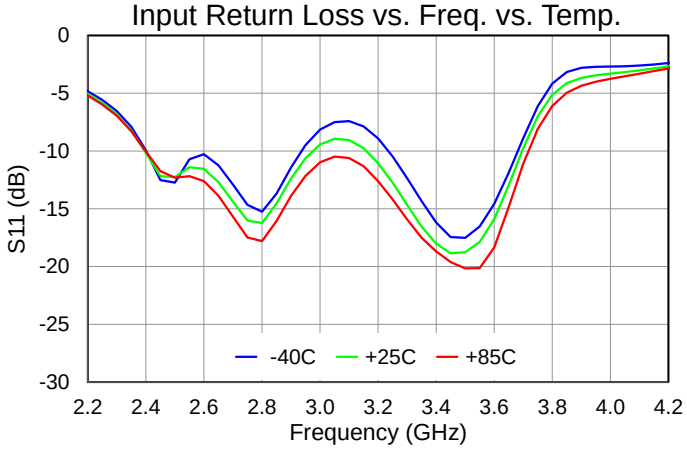
Gain vs. Frequency vs. Temp.



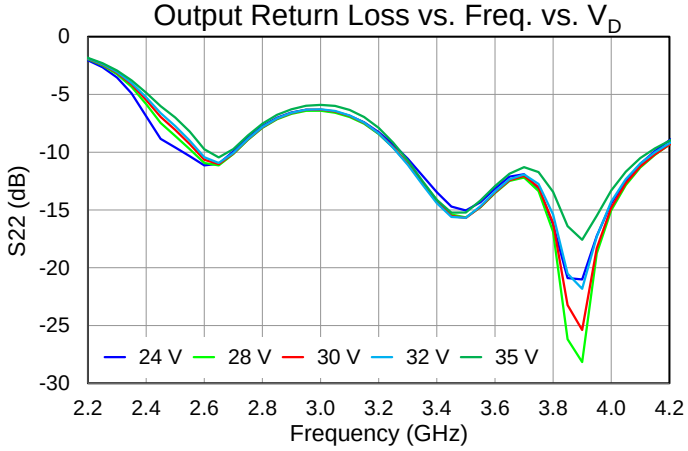
Input Return Loss vs. Freq. vs. V_D



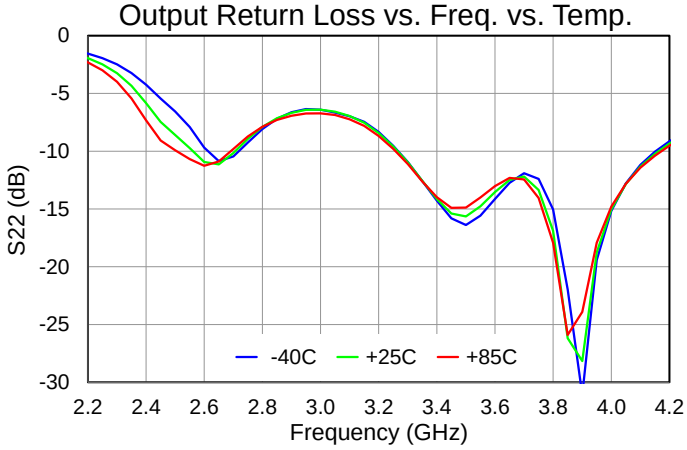
Input Return Loss vs. Freq. vs. Temp.



Output Return Loss vs. Freq. vs. V_D



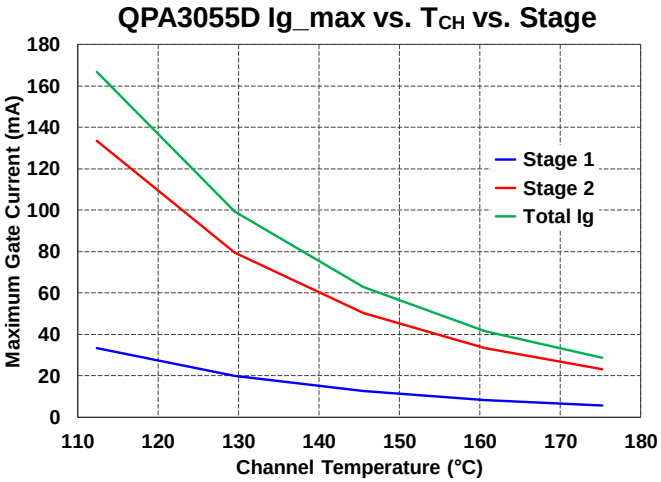
Output Return Loss vs. Freq. vs. Temp.

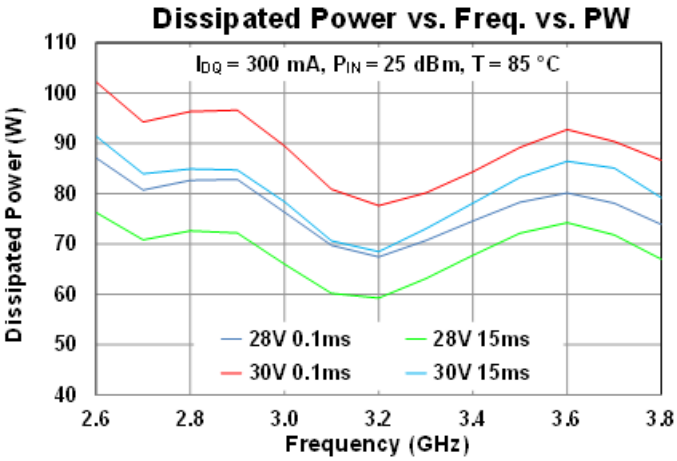


Thermal and Reliability Information

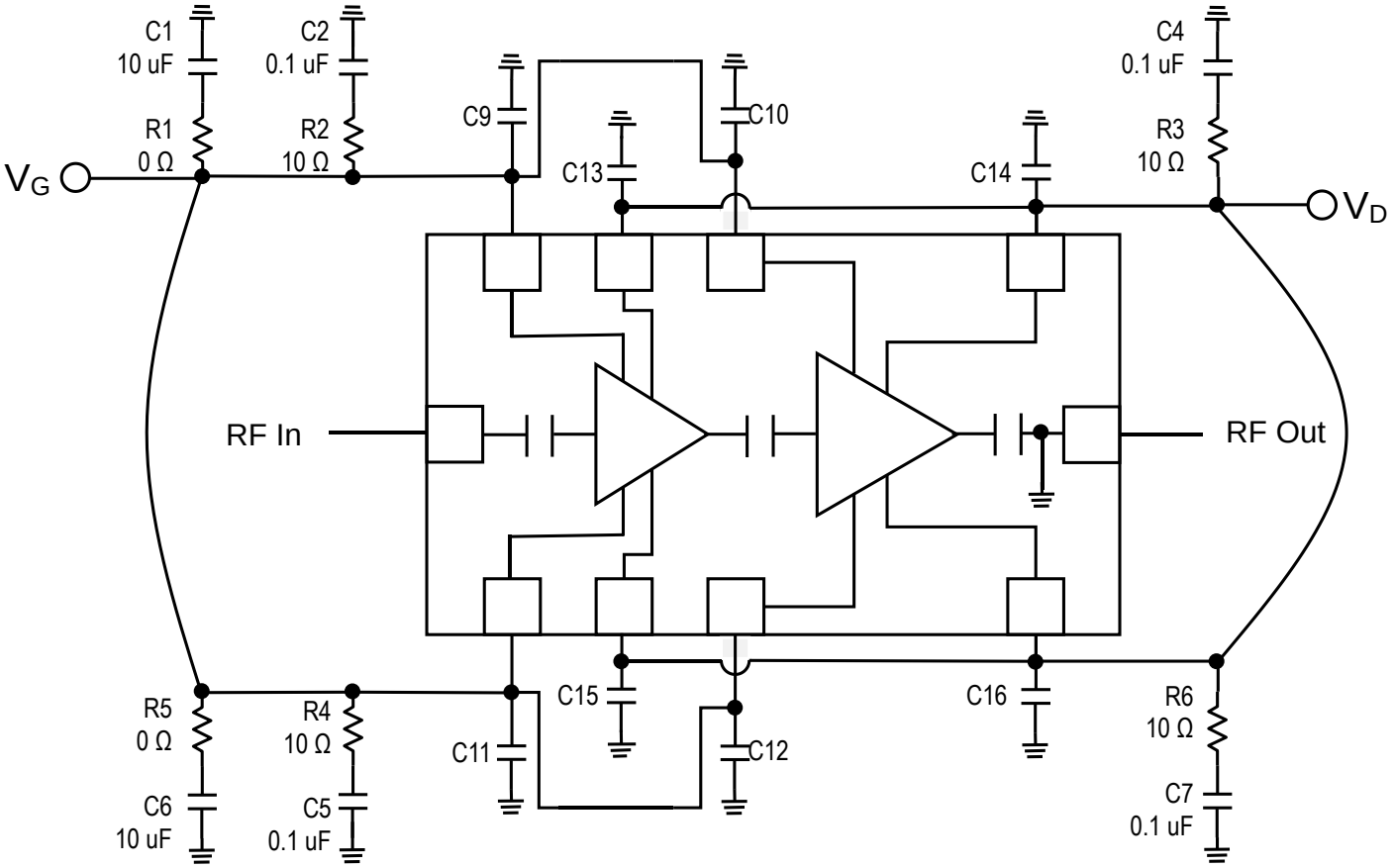
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 30 V, I_{DQ} = 300 mA, Freq = 2.8 GHz, I_{D_Drive} = 7.0 A, P_{IN} = 25 dBm, P_{OUT} = 50.5 dBm, P_{DISS} = 97.9 W, PW = 100 us, DC = 10%	0.33	ºC/W
Channel Temperature, T_{CH} (Under RF)		117	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 30 V, I_{DQ} = 300 mA, Freq = 3.6 GHz, I_{D_Drive} = 6.5 A, P_{IN} = 25 dBm, P_{OUT} = 50.3 dBm, P_{DISS} = 89.0 W, PW = 15 ms, DC = 30%	0.69	ºC/W
Channel Temperature, T_{CH} (Under RF)		146	°C

Notes:
1. Die mounted to 20 mil CuMo carrier plate with AuSn solder. Thermal resistance determined to the back of carrier (85 °C).
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates





Applications Information and Pad Layout



Notes:
1. V_G & V_D need to be biased from both sides.

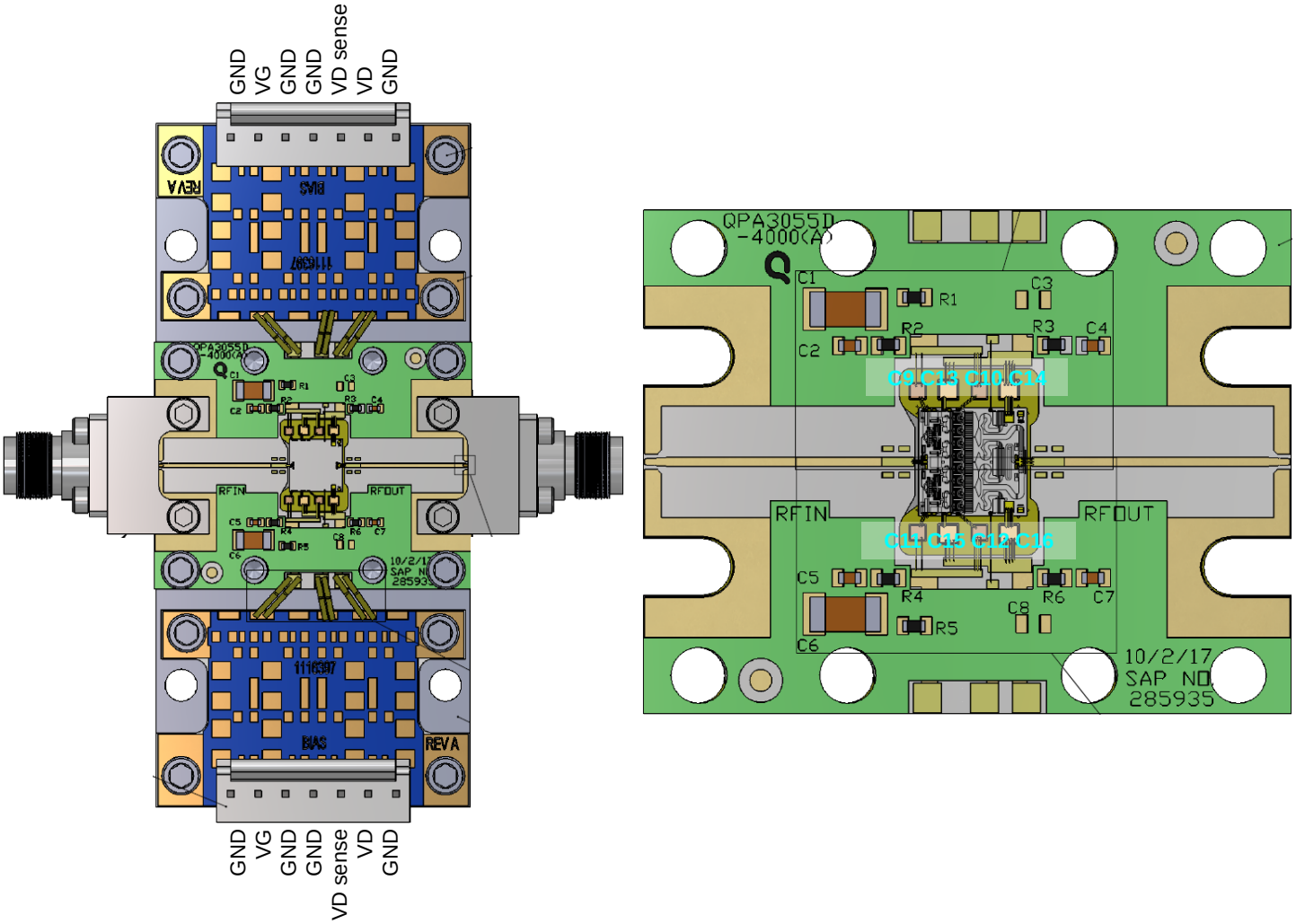
Bias-Up Procedure

1. Set I_D limit (CW) to 7000 mA, I_G limit to xx mA
2. Set V_G to −5.0 V
4. Set VD +28 V
5. Adjust V_G more positive until I_{DQ} ≈ 300 mA (V_G ~ −2.5 V Typical)
6. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −5.0 V. Ensure I_{DQ} ~ 0 mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

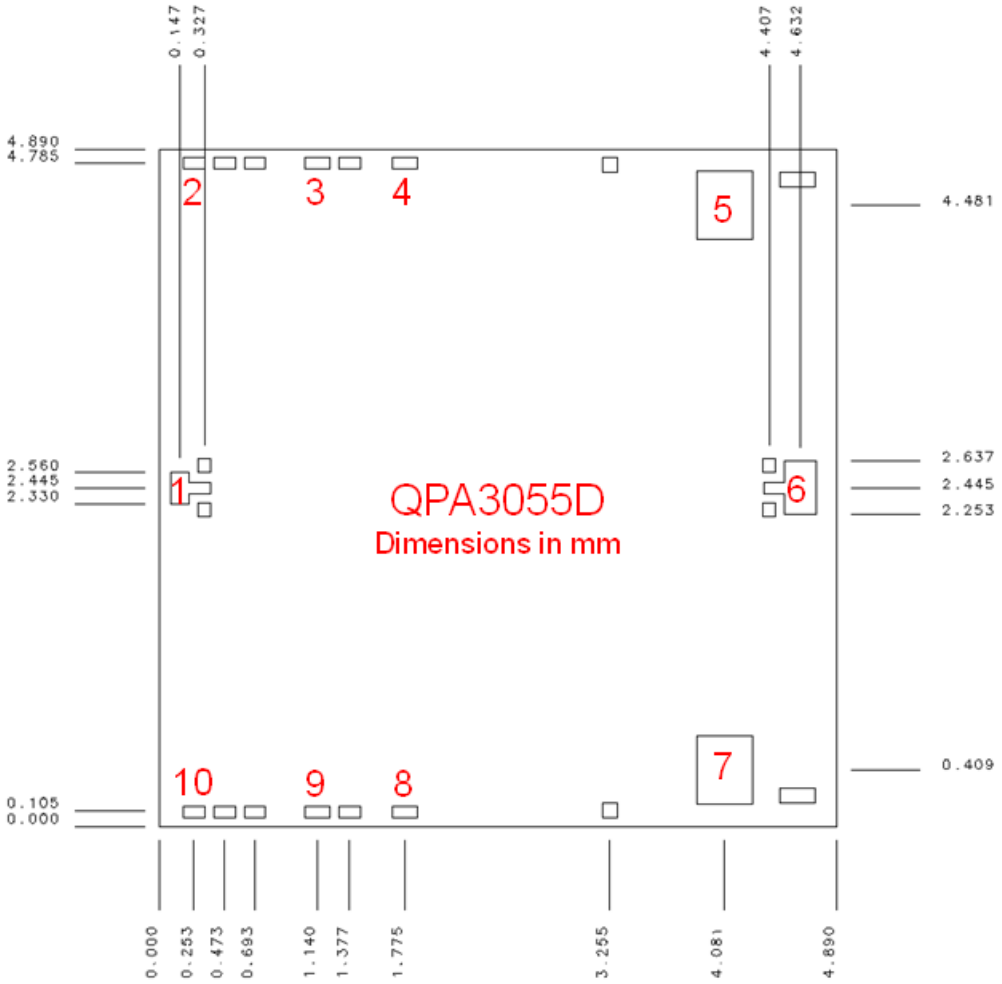
Evaluation Board (EVB) Layout Assembly



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C9,C10,C11,C12	100 pF // 10000 pF	CAP, 10000pF, ±20%, 50V, X7R, 30X30, SL	Presidio	MVB3030X103M2H5C1F
C13,C14,C15,C16	1000 pF	CAP, 1000pF, ±10% 50V, BORDER, SL	Various	
C2, C4, C5, C7	0.1 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Various	
C1,C6	10 uF	CAP, CER, 10UF, 25V, 20%, X5R, 1206	Various	
R2, R3, R4, R6	10 Ohm	RESISTOR, 10 OHM, 5%, 0402, SMD	Various	
R1, R5	0 Ohm	RES, 0 OHM, 5%, 0402	Various	

Mechanical Information and Bond Pad Description



Units: millimeters
Thickness: 0.100
Die x,y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF IN	0.132 x 0.230	RF Input; matched to 50 Ω, DC blocked
2, 10	V_{G1}	0.152 x 0.082	Gate voltage for stage 1. Bias network is required; see Application Circuit on page 13 as an example.
3, 9	V_{D1}	0.182 x 0.082	Drain voltage for stage 1. Bias network is required; see Application Circuit on page 13 as an example.
4, 8	V_{G2}	0.182 x 0.082	Gate voltage for stage 2. Bias network is required; see Application Circuit on page 13 as an example.
5, 7	V_{D2}	0.402 x 0.492	Drain voltage for stage 2. Bias network is required; see Application Circuit on page 13 as an example.
6	RF OUT	0.232 x 0.384	RF Output; matched to 50 Ω, DC blocked, DC grounded

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ANSI/ESDA/JEDEC JS-001

Caution!
ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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