QPA1011D

7.9 – 11.0 GHz 25 W GaN Power Amplifier

Product Description

Qorvo's QPA1011D is a X-band high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The QPA1011D operates from 7.9 – 11 GHz and typically provides 25 W saturated output power with power-added efficiency of 37% and large-signal gain of 20 dB. This combination of wideband performance provides the flexibility designers are looking for to improve system performance while reducing size and cost.

QPA1011D can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under both CW and pulse operations.

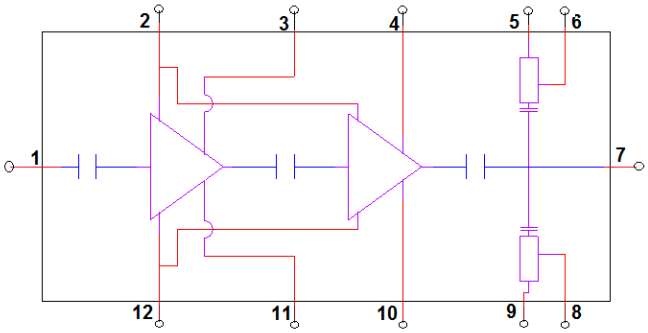
The QPA1011D is matched to 50Ω with integrated DC blocking capacitors on both RF I/O ports simplifying system integration. The wideband performance and operational flexibility allows it support satellite communication and data links, as well as, military and commercial radar systems.

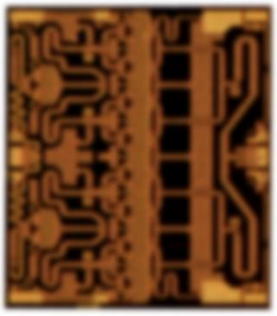
The QPA1011D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Functional Block Diagram





Product Features

- Frequency Range: 7.9 – 11 GHz
- P_{OUT}: 45 dBm at P_{IN} = 25 dBm
- PAE: 37 % at P_{IN} = 25 dBm
- Large Signal Gain: 20 dB at P_{IN} = 25 dBm
- Small Signal Gain: 26 dB
- Integrated Power Detector
- Bias: V_D = 24 V, I_{DQ} = 1200 mA, V_G = −2.0 V Typical
- Pulsed V_D: PW =100 µS, DC = 10%
- Chip Dimensions: 2.75 x 3.12 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Satellite Communications
- Data Links
- Military and Commercial Radar

Ordering Information

Part No.	ECCN	Description
QPA1011D	3A001.b.2.b.2	7.9 – 11 GHz 25 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−8 to 0V
Drain Current (I_{D1}/I_{D2})	672 mA / 2880 mA
Gate Current (I_G)	See chart, pg. 21
Power Dissipation (P_{DISS}), 85°C, CW	61 W
Input Power (P_{IN}), CW, 50Ω, V_D=28 V, I_{DQ}=1200 mA, 85 °C	30 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D=28 V, I_{DQ}=1200 mA 85 °C	30 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	24 V
Drain Current (I_{DQ})	1200 mA
Gate Voltage (V_G), Typical	−2.0 V

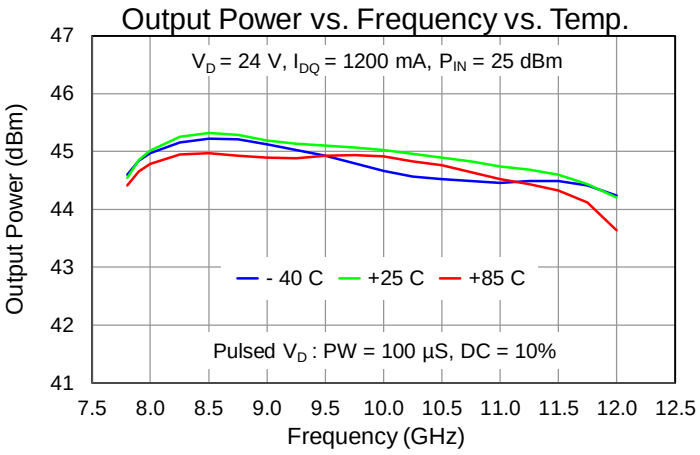
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

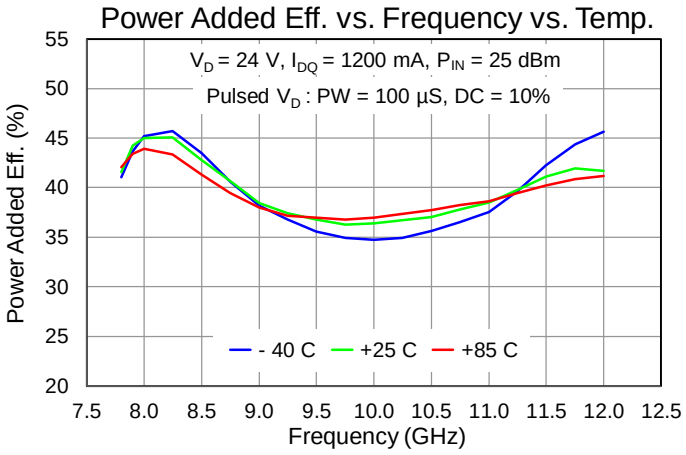
Electrical Specifications

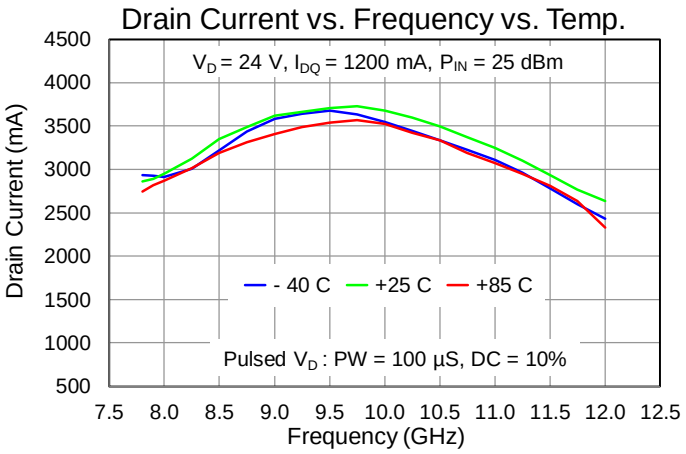
Parameter		Min	Typ	Max	Units
Operational Frequency Range		7.9		11	GHz
Output Power (P_{IN} = 25 dBm)	7.9 GHz 9.0 GHz 11.0 GHz		44.8 45.2 44.7		dBm dBm dBm
Power Added Efficiency (P_{IN} = 25 dBm)	7.9 GHz 9.0 GHz 11.0 GHz		44.2 38.4 38.5		% % %
3rd Order Intermodulation Level (P_{OUT}/Tone= 38 dBm)	7.9 GHz 10.0 GHz 11.0 GHz		−21.5 −20.5 −21.5		dBc dBc dBc
Small Signal Gain	7.9 GHz 9.0 GHz 11.0 GHz		25.9 26.2 24.9		dB dB dB
Input Return Loss	7.9 GHz 9.0 GHz 11.0 GHz		12 25.5 15		dB dB dB
Output Return Loss	7.9 GHz 9.0 GHz 11.0 GHz		8.5 7 25		dB dB dB
Output Power Temperature Coefficient (25 – 85 °C) (P_{IN} = 25 dBm)			−0.006		dB/°C
Small Signal Gain Temperature Coefficient (25 – 85 °C)			−0.049		dB/°C
Recommended Voltage Operations			24	28	V

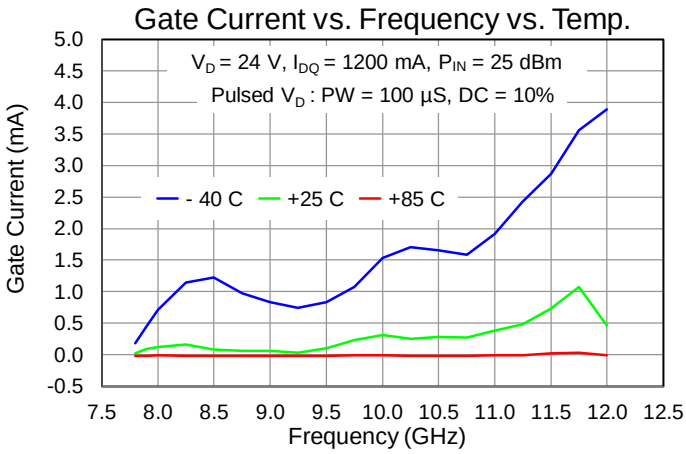
Test conditions, unless otherwise noted: 25 °C, Pulsed V_D: PW = 100 µS, DC = 10%, V_D = 24 V, I_{DQ} = 1200 mA, V_G = −2.0 V Typical

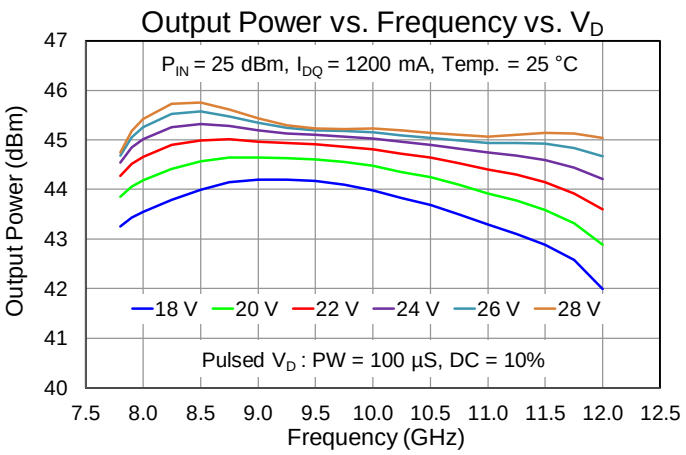
Performance Plots – Large Signal (Pulsed)

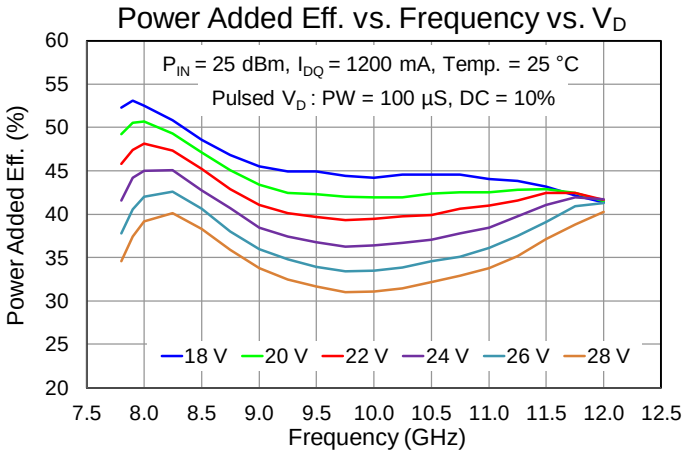












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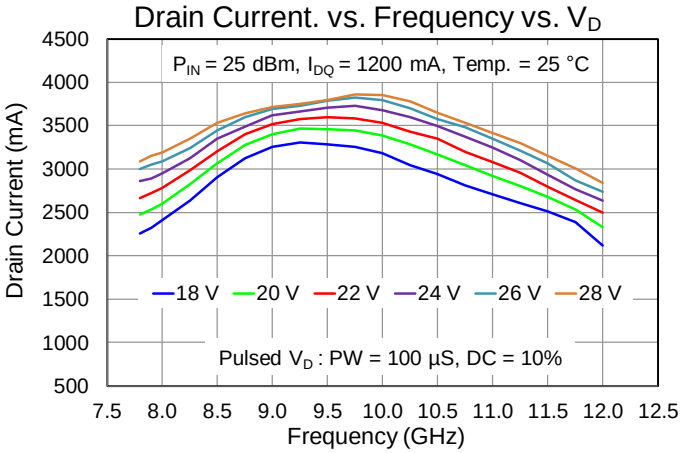

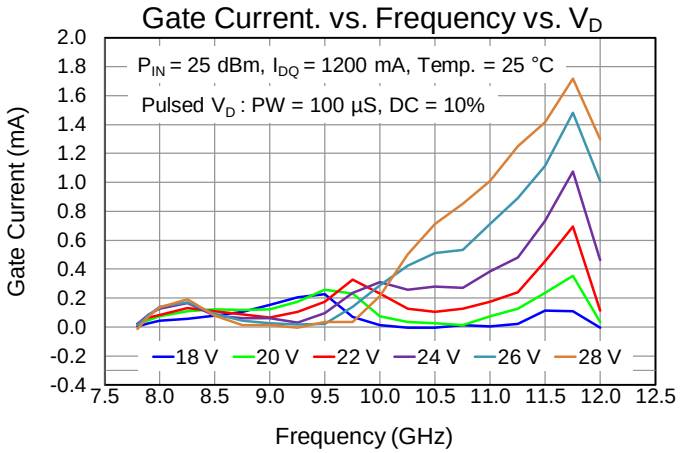

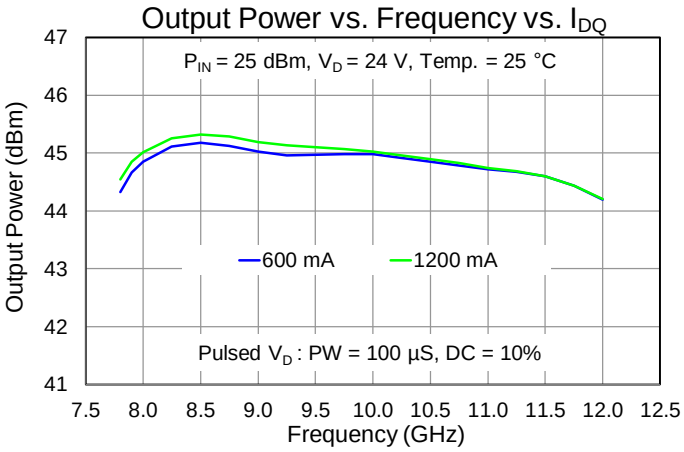

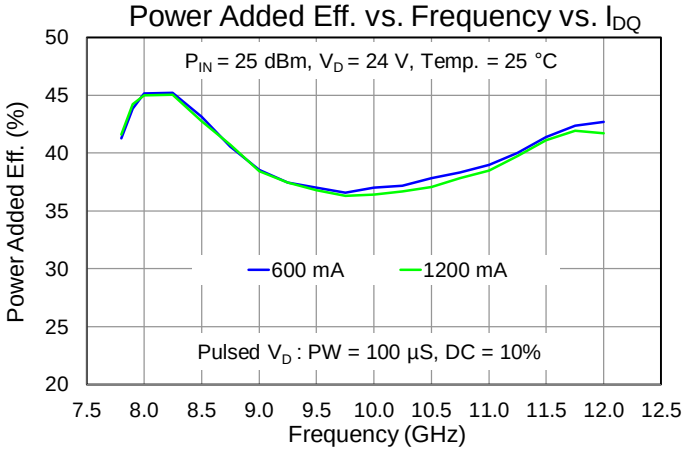

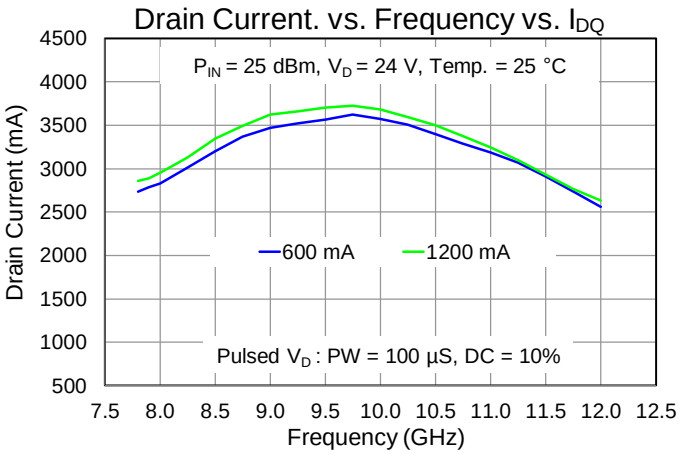

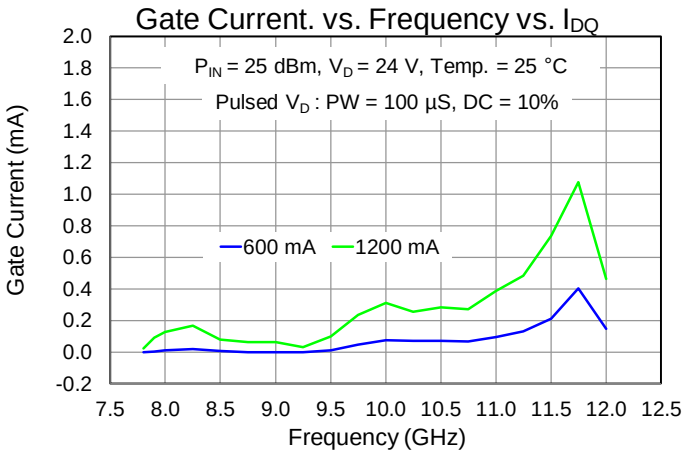

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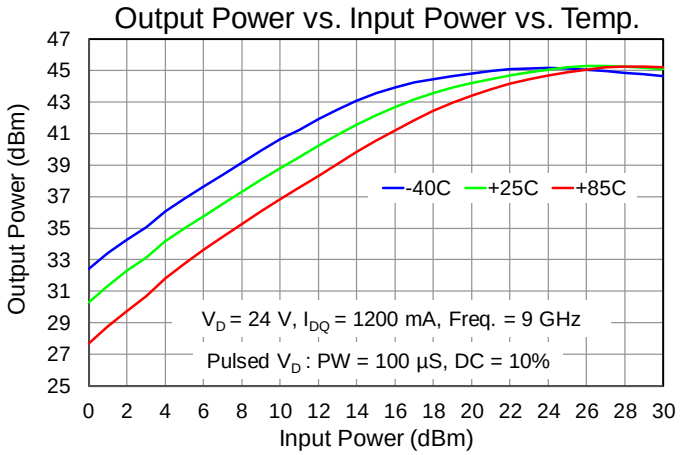

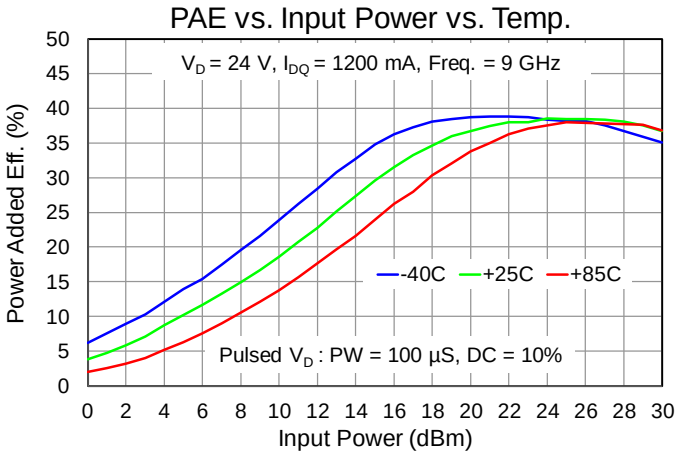

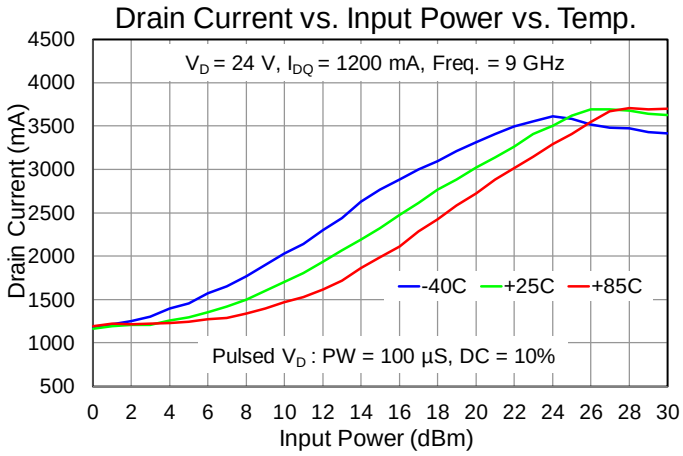

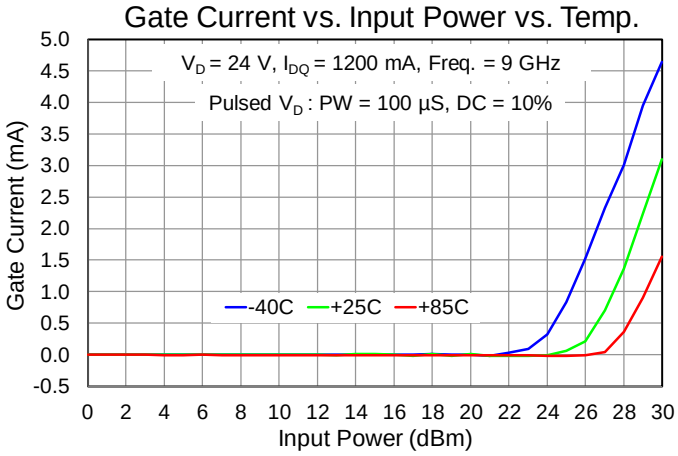

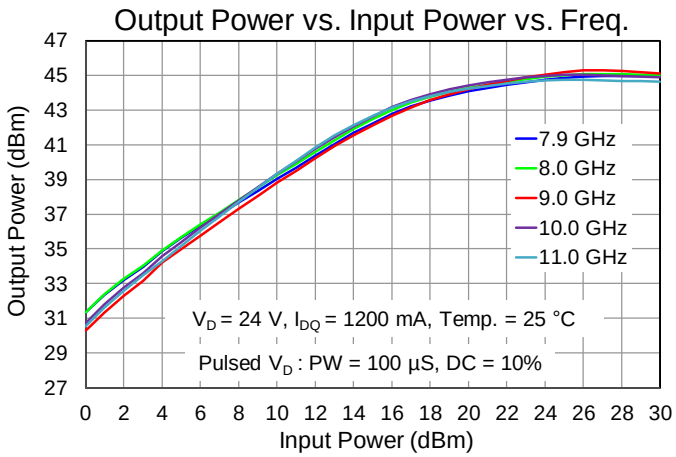

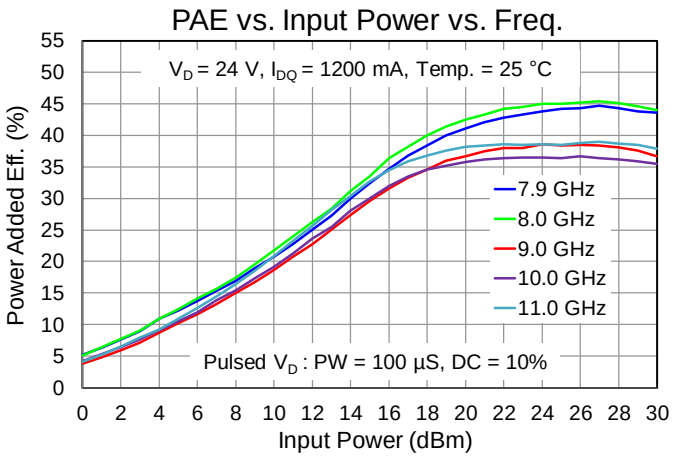

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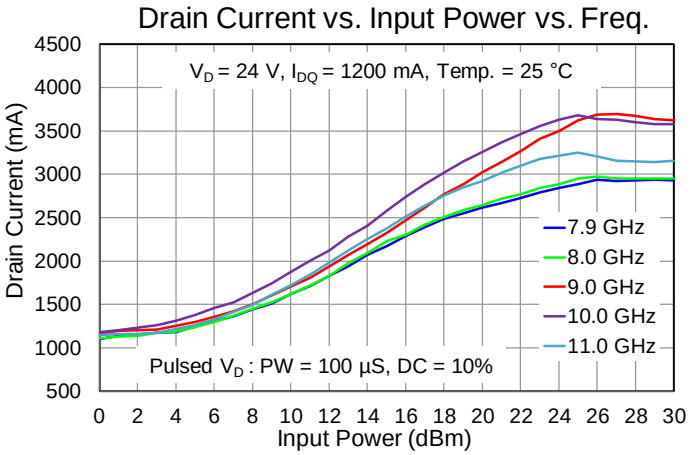
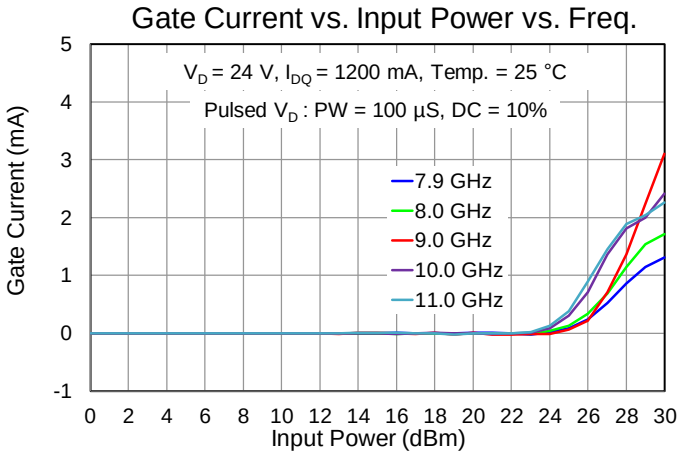
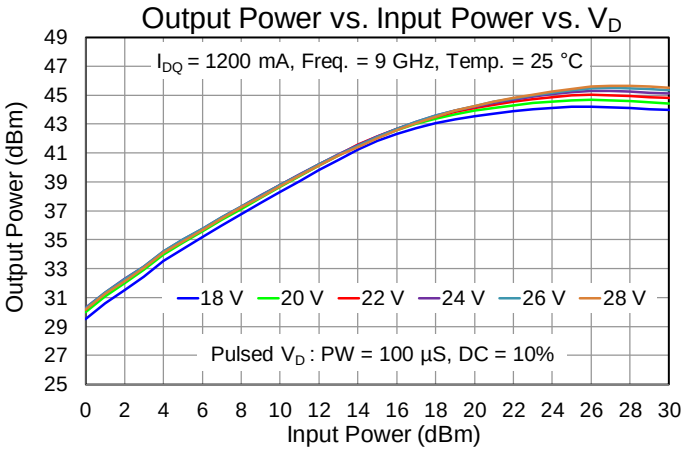
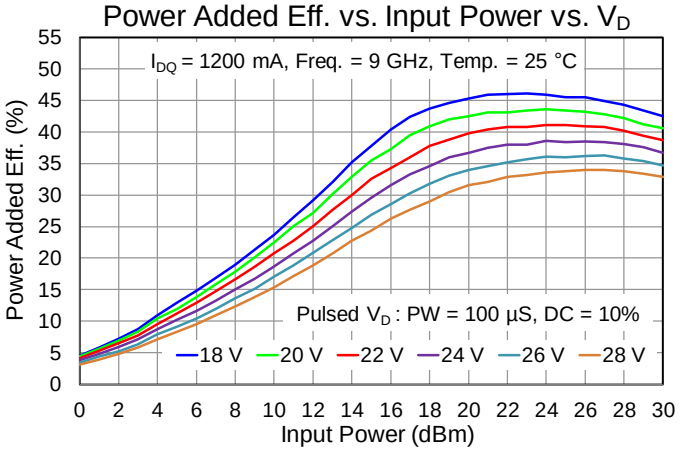
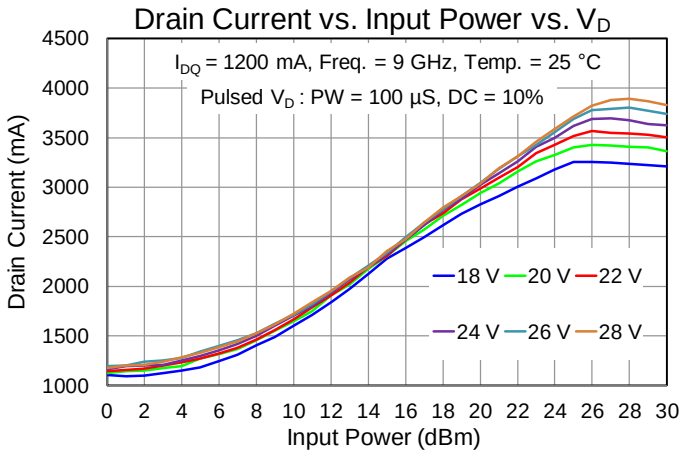
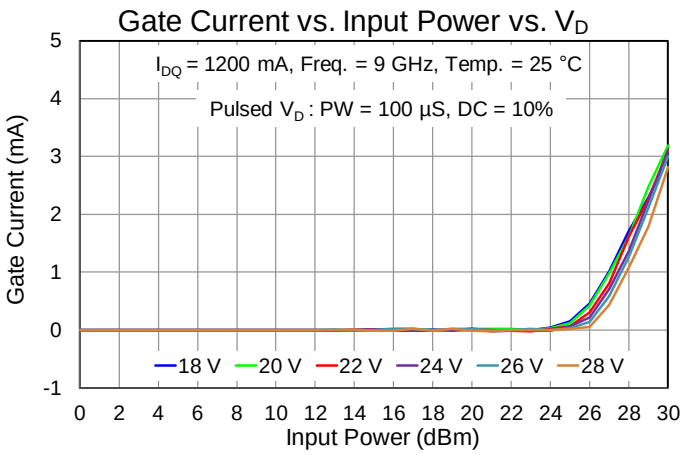




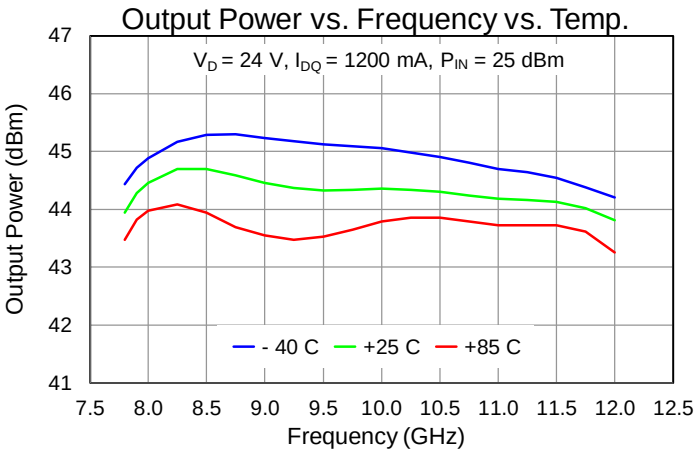


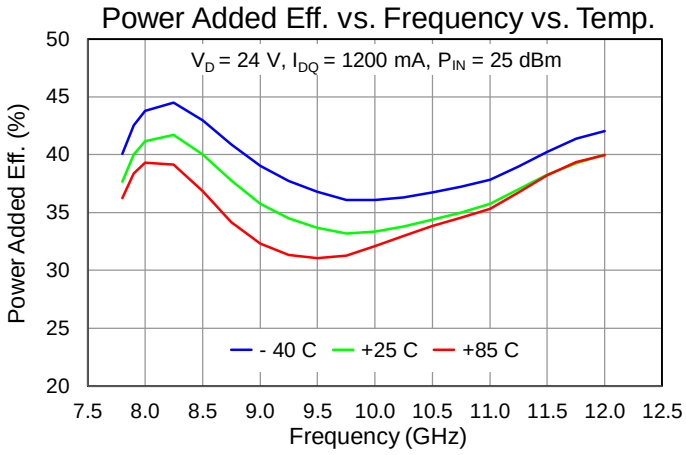


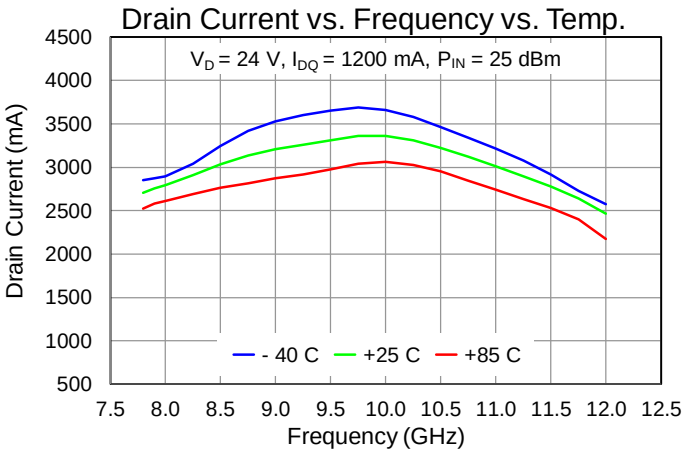


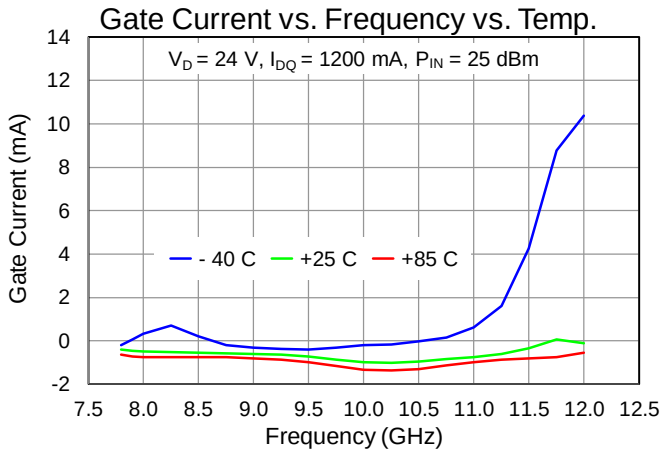


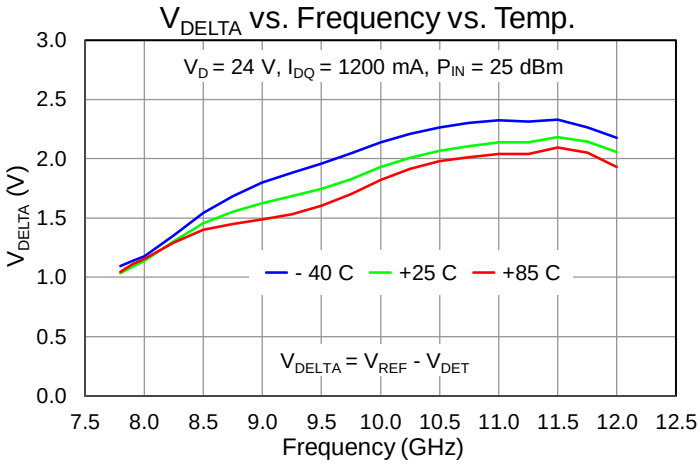
Performance Plots – Large Signal (CW)



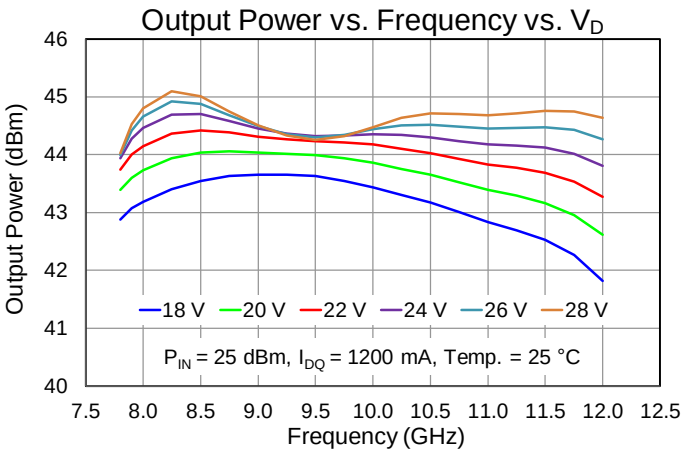


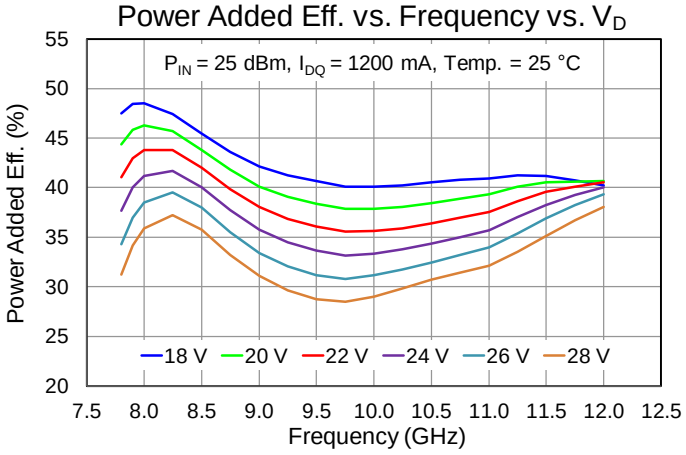


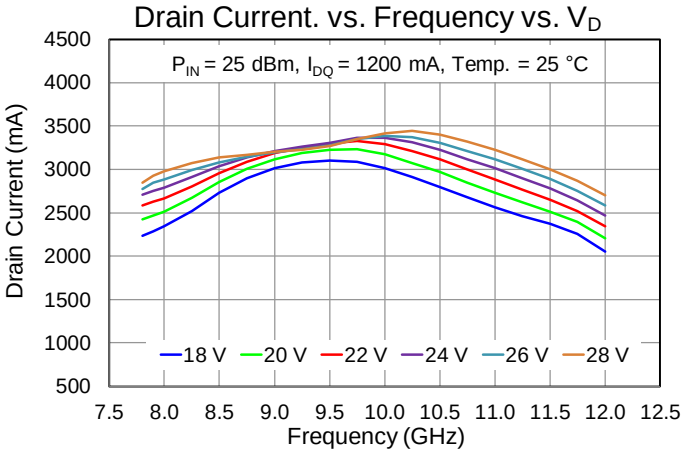


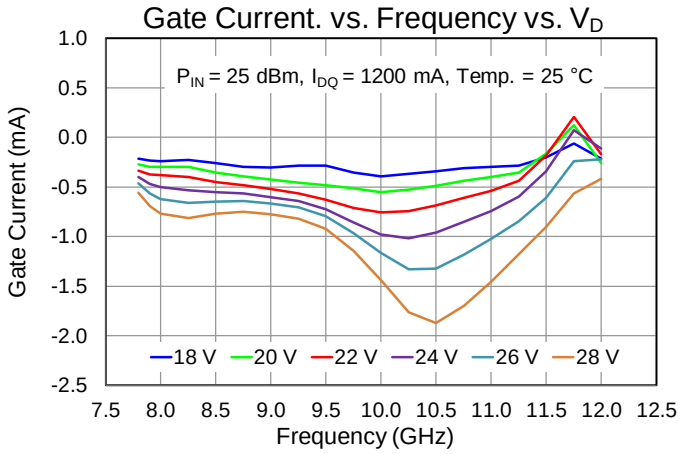


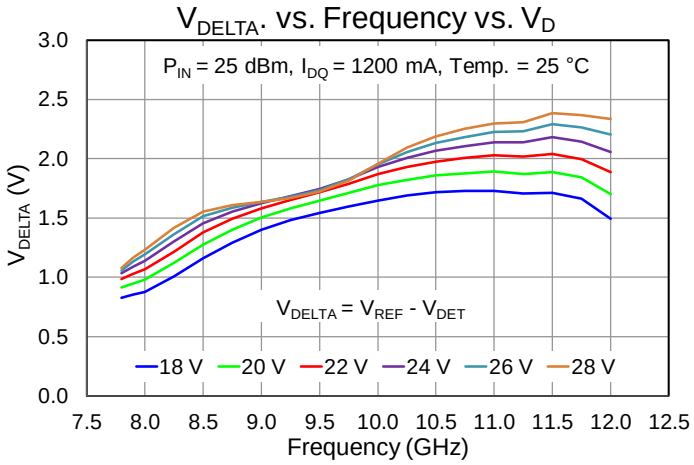
Performance Plots – Large Signal (CW)











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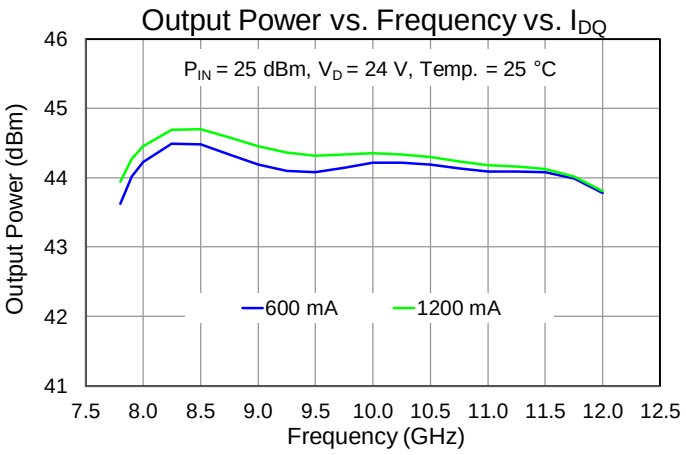

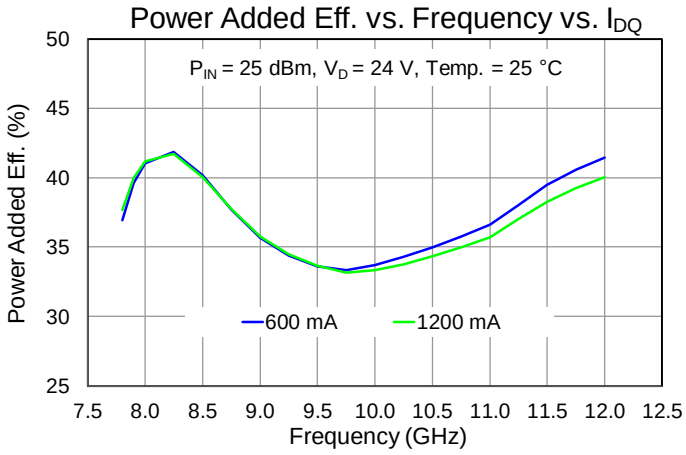

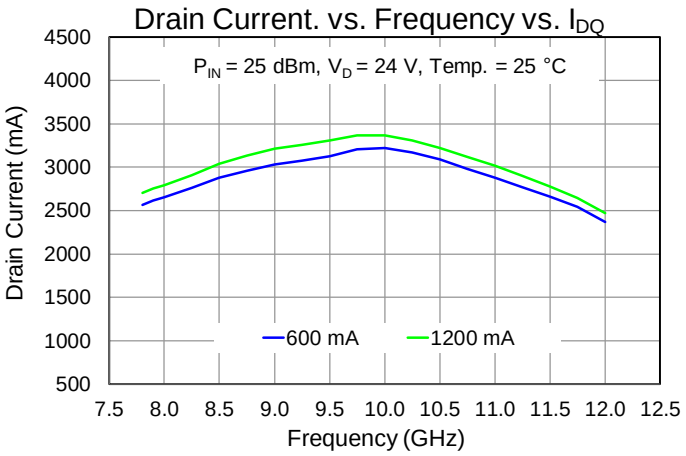

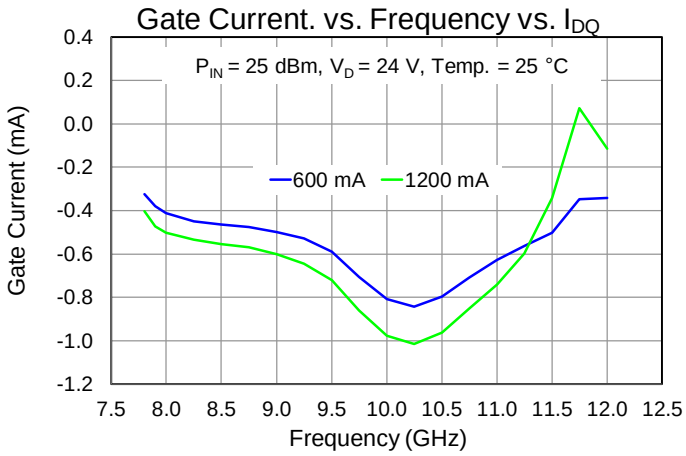

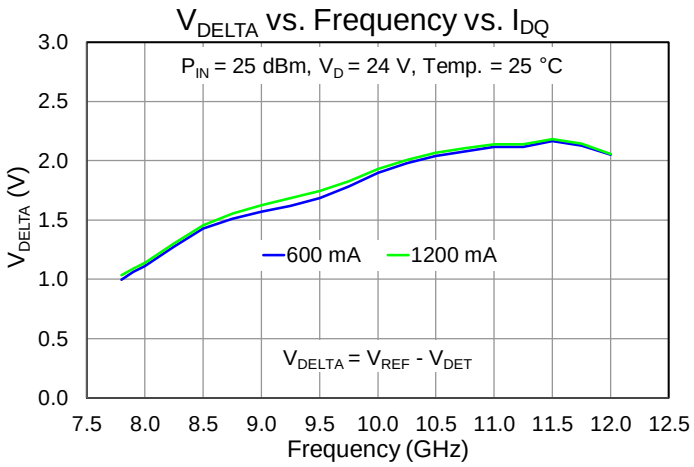

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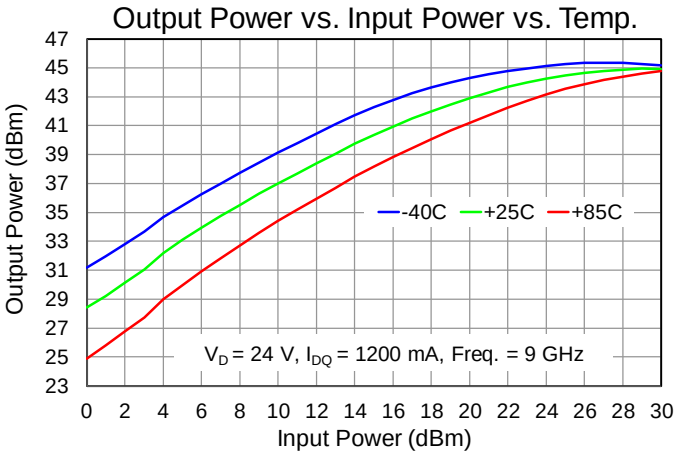

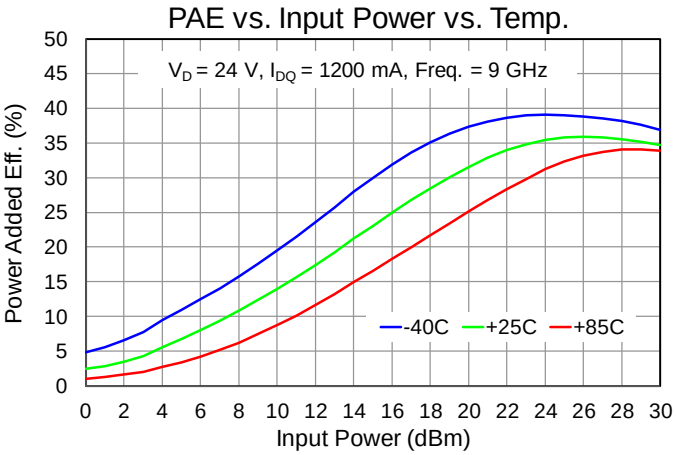

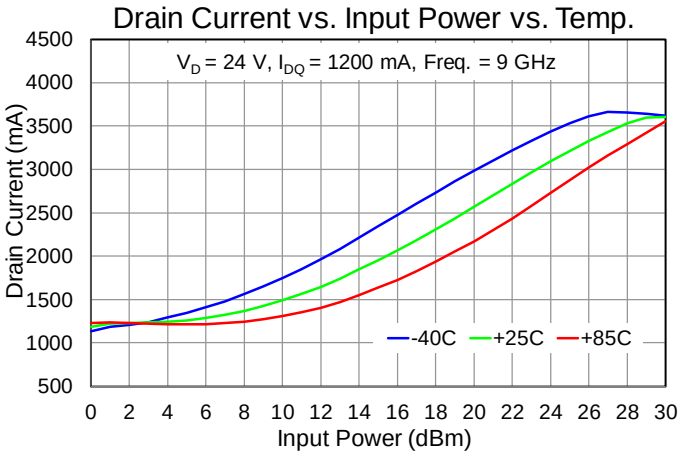

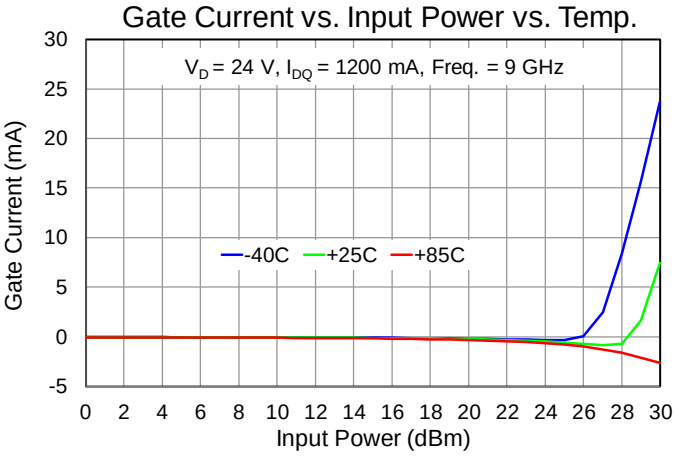

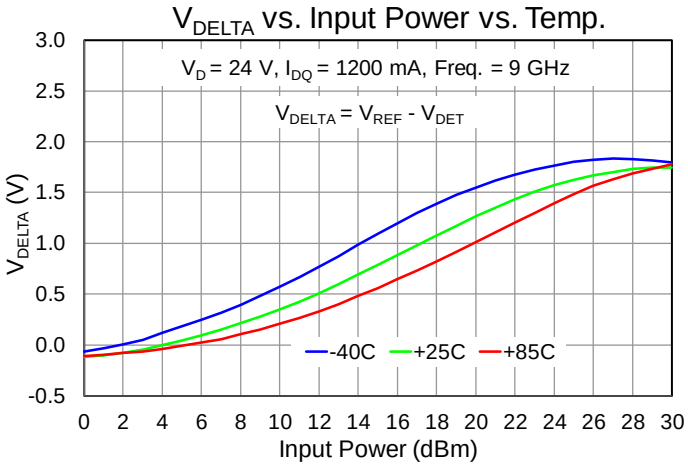

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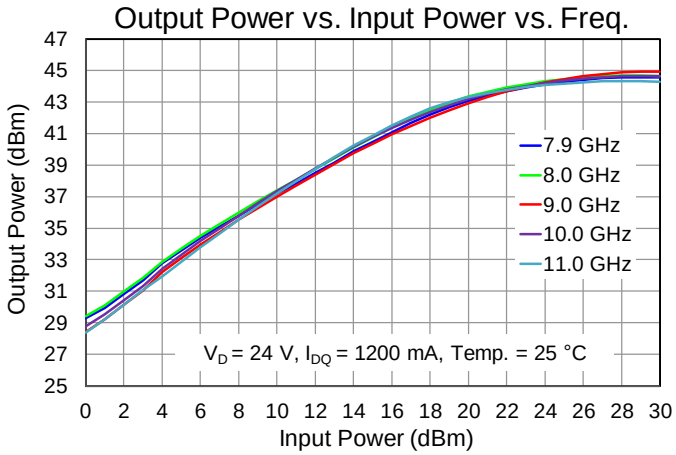
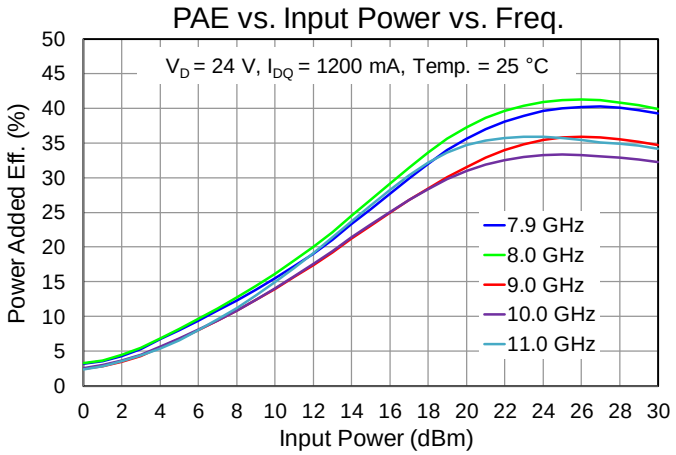
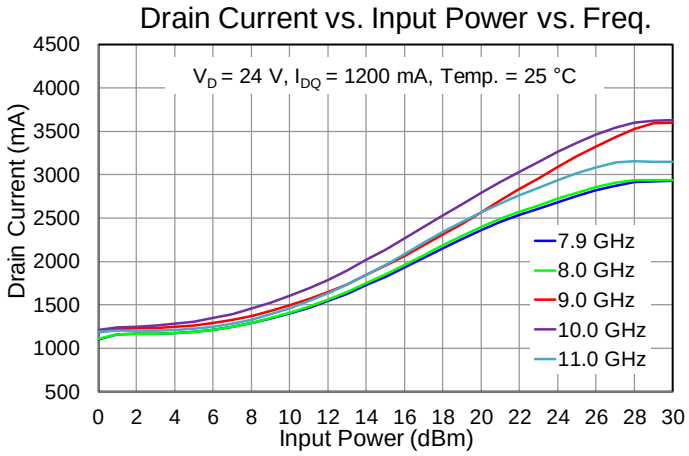
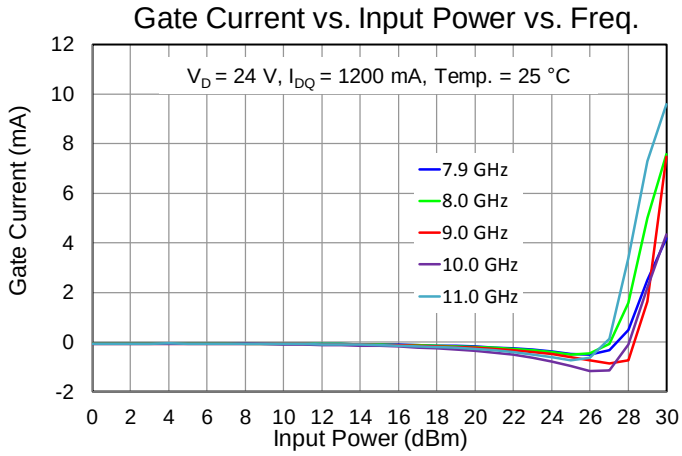
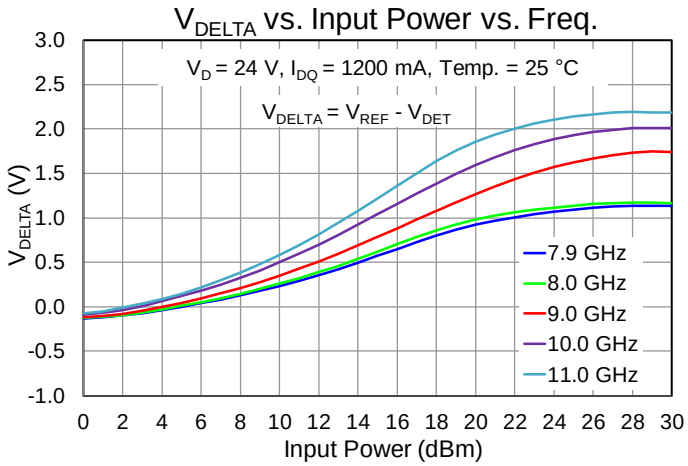


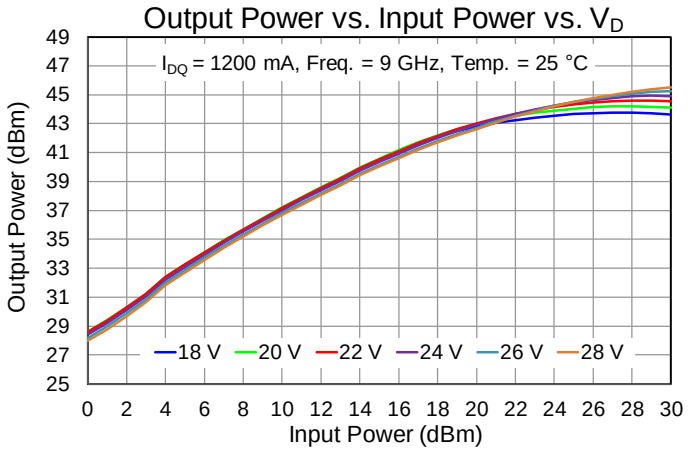


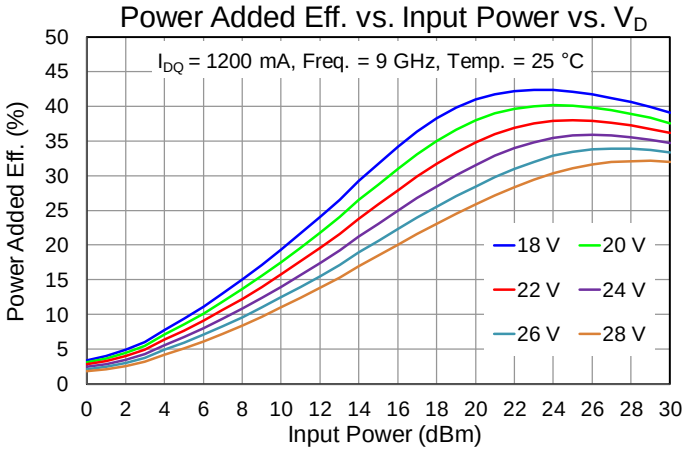


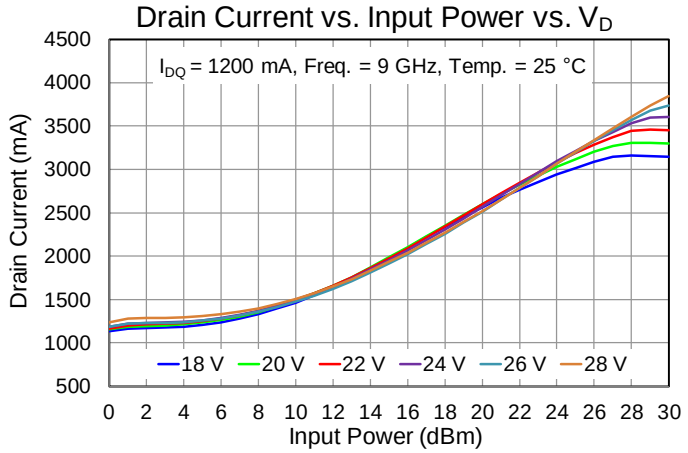


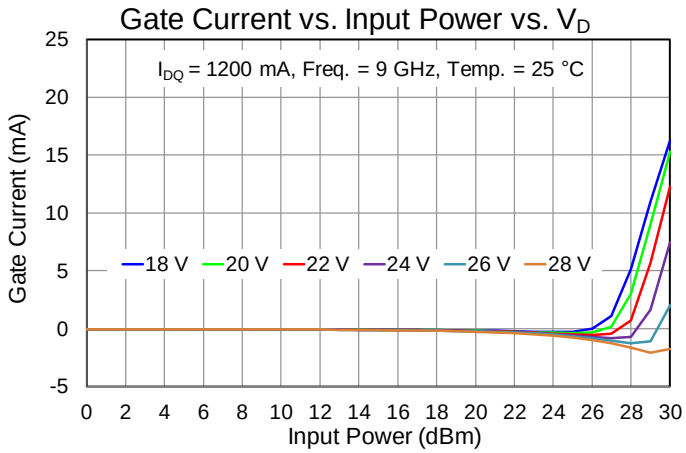


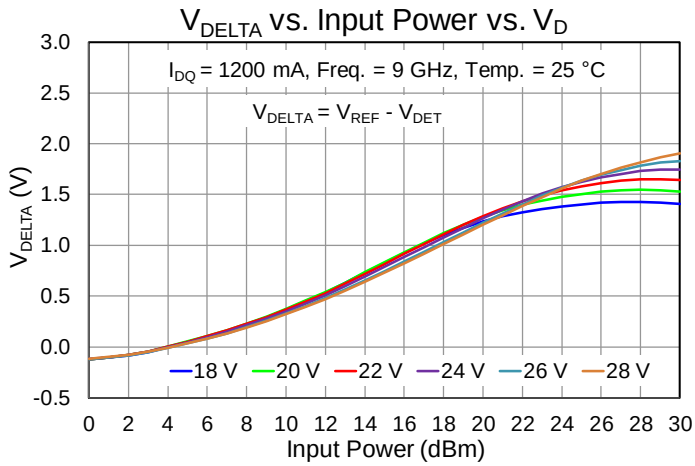
Performance Plots – Large Signal (CW)



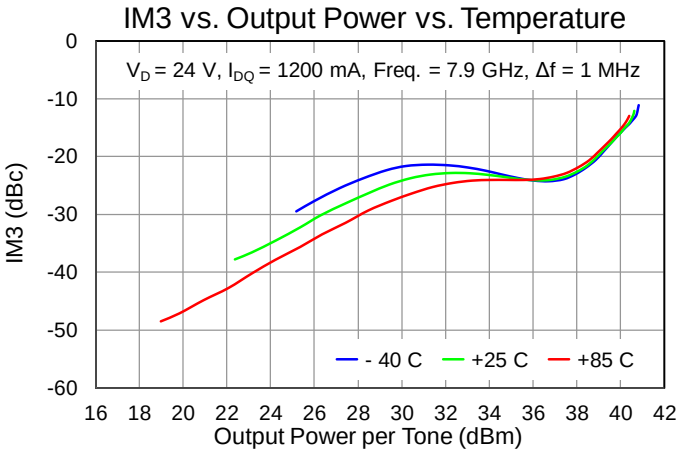


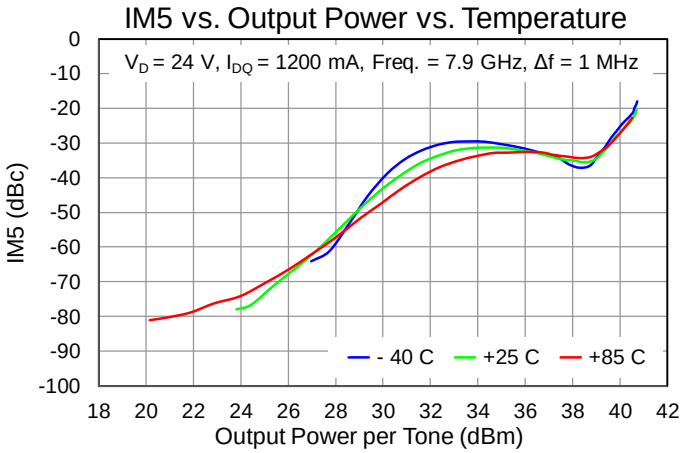


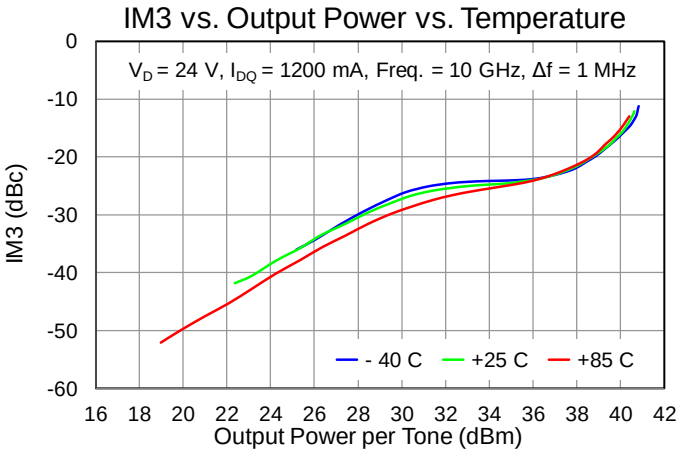


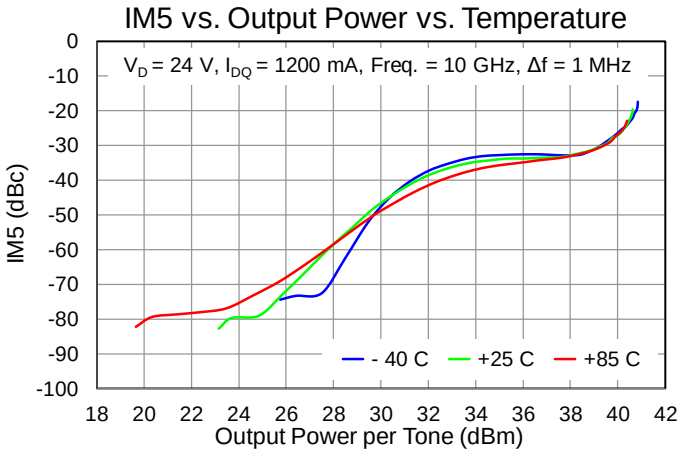


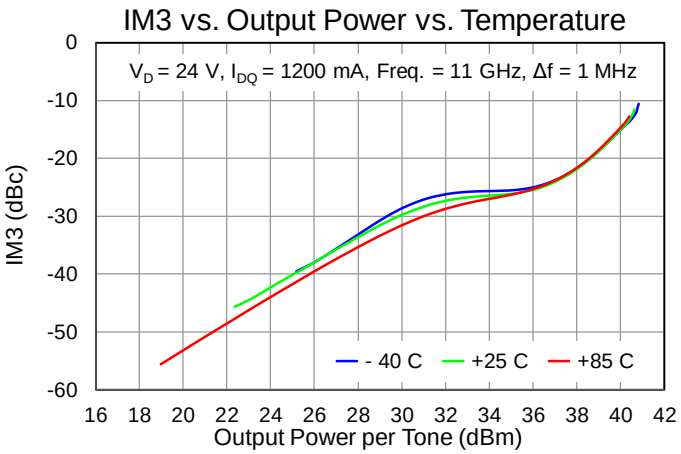
Performance Plots – Linearity

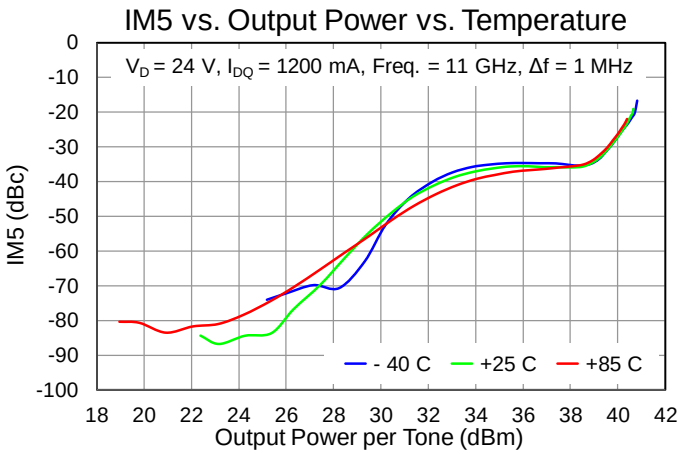




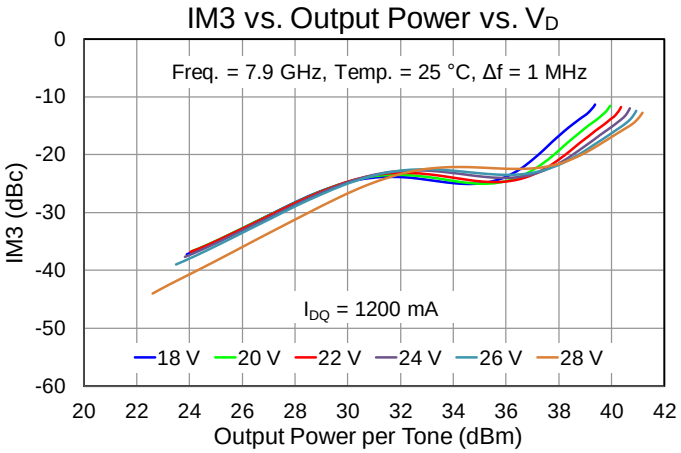


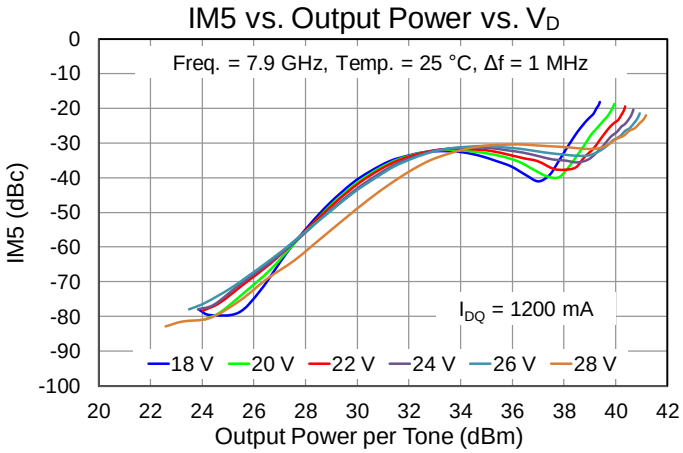


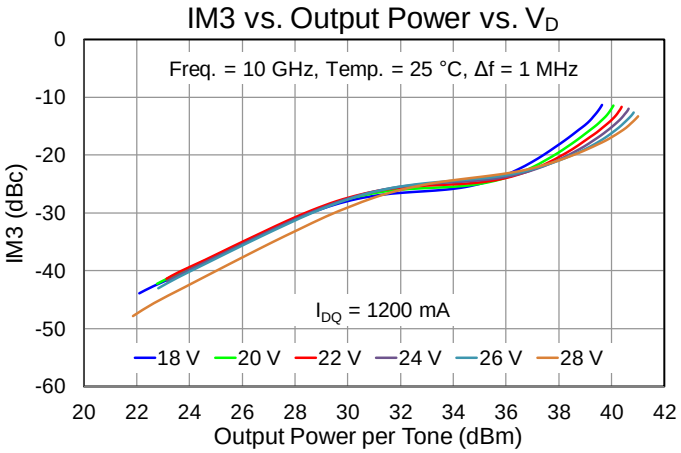


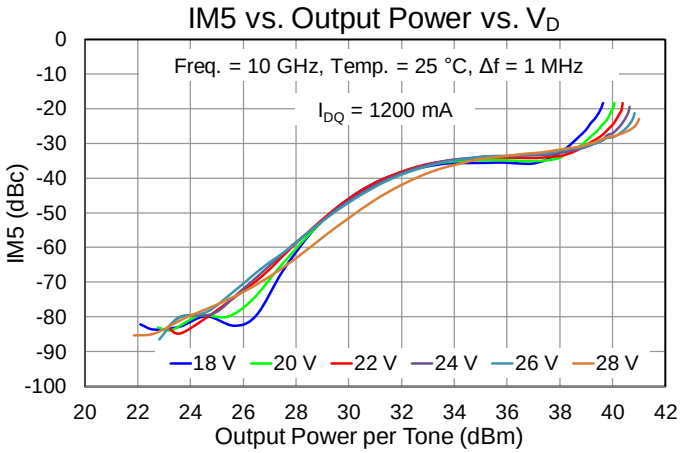


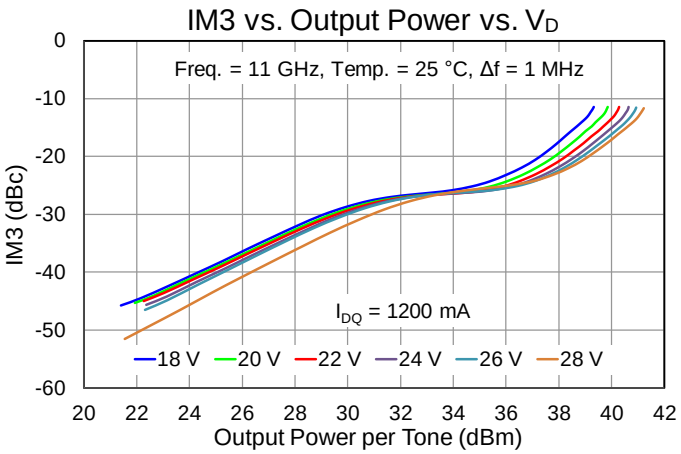
Performance Plots – Linearity

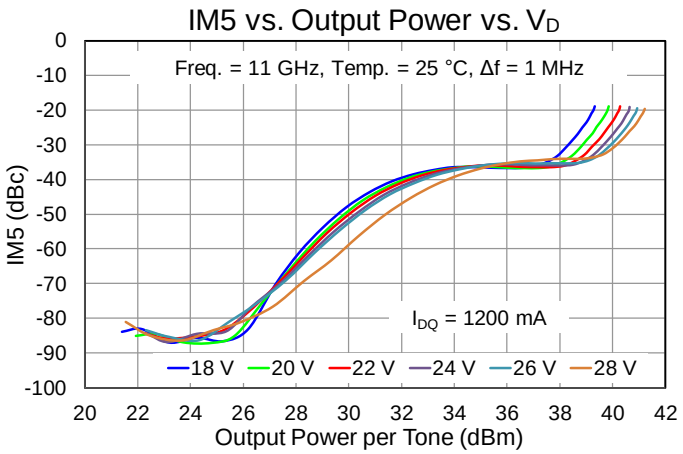




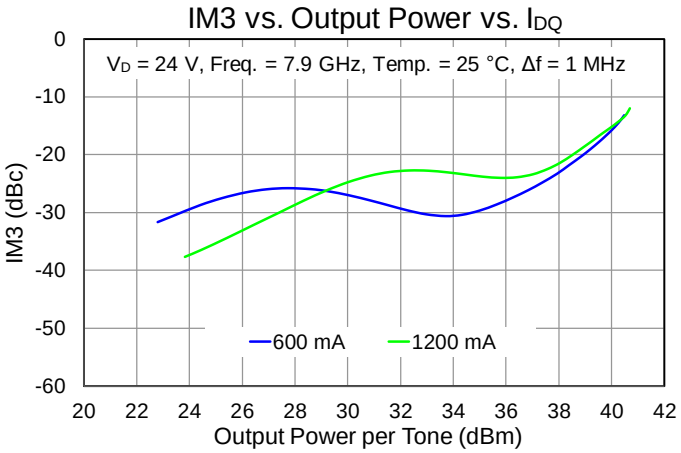


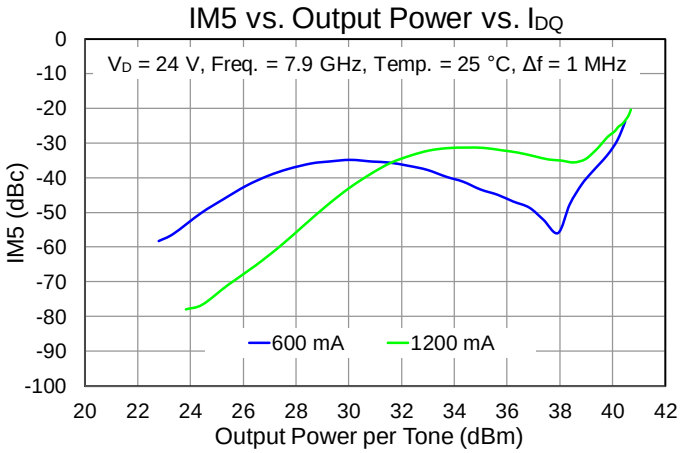


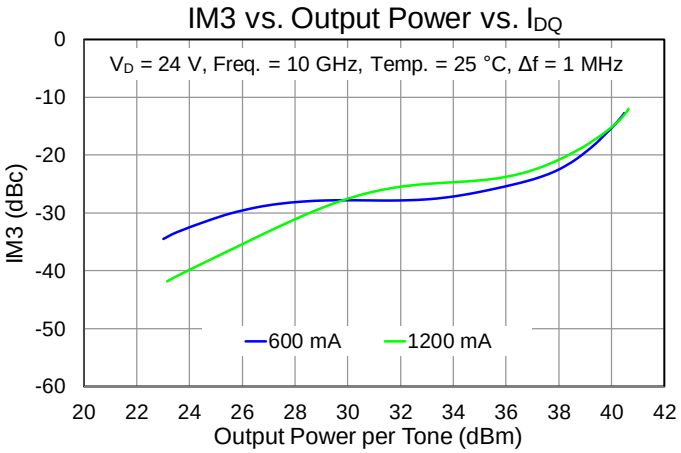


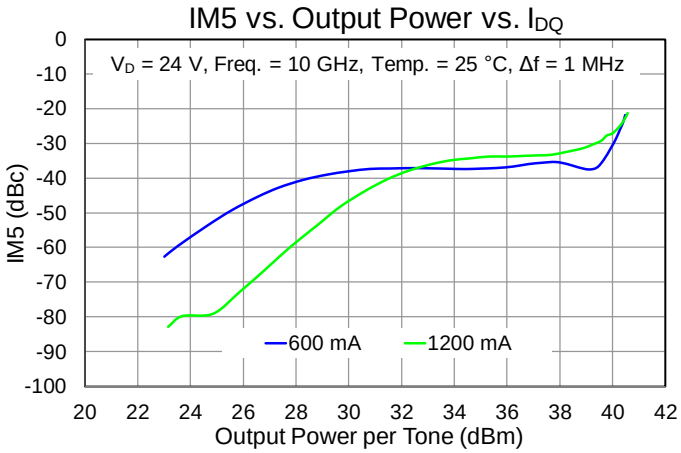


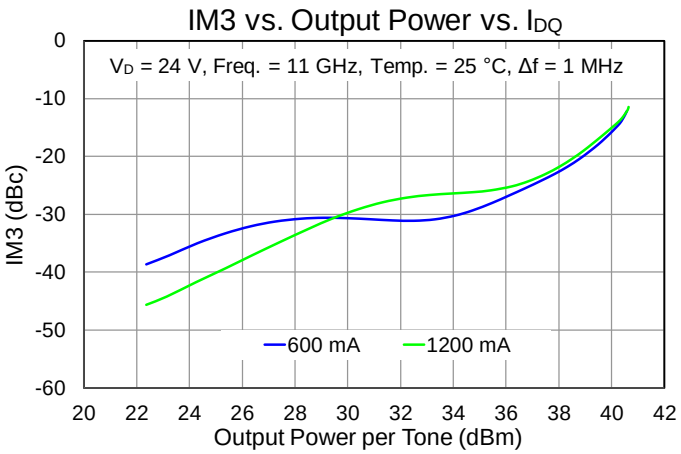
Performance Plots – Linearity

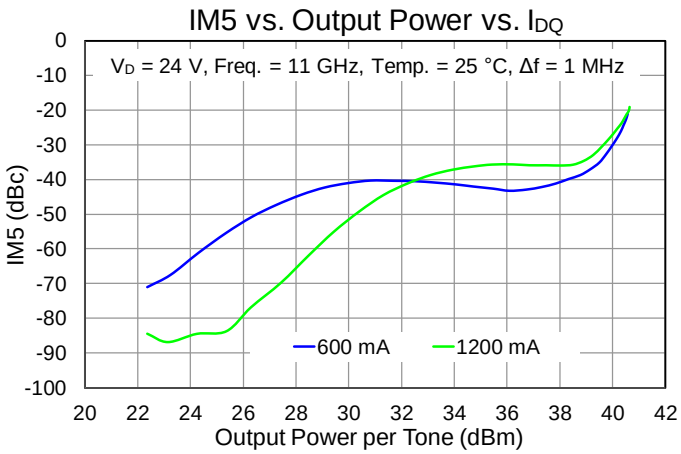




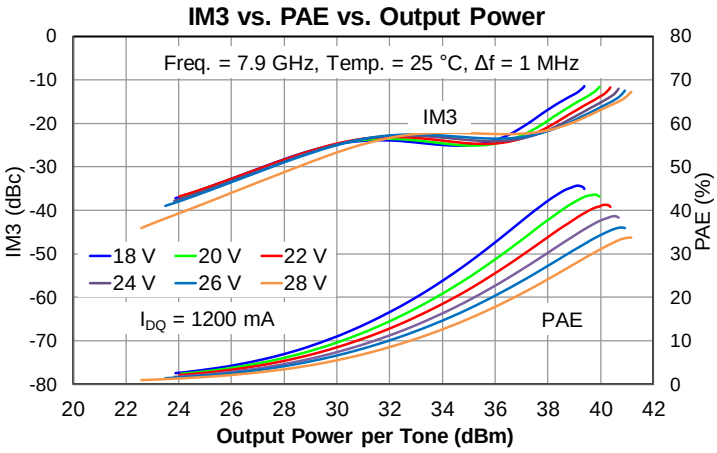


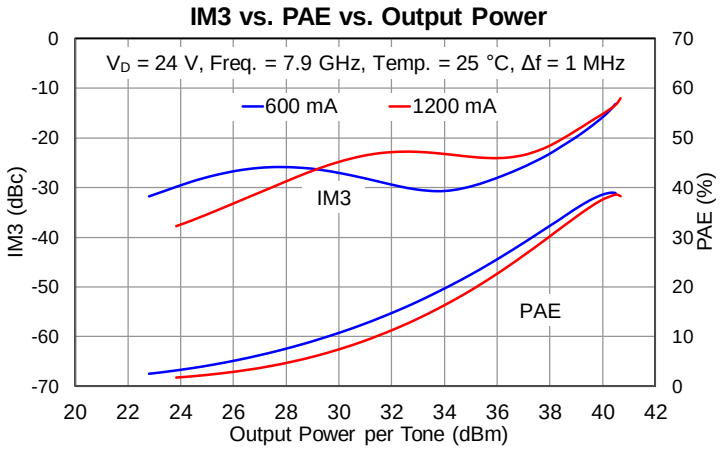




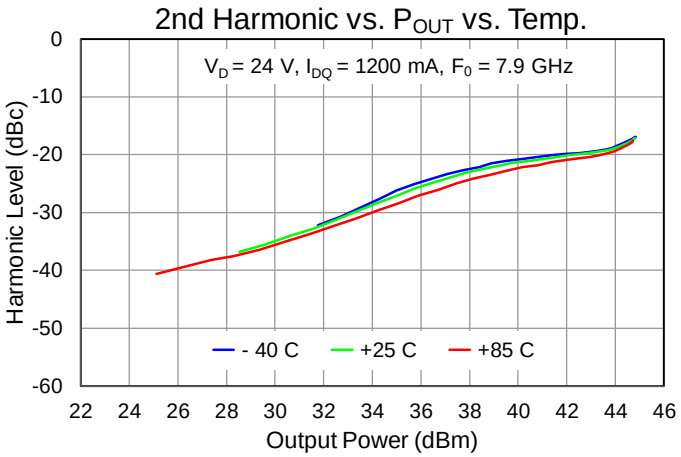


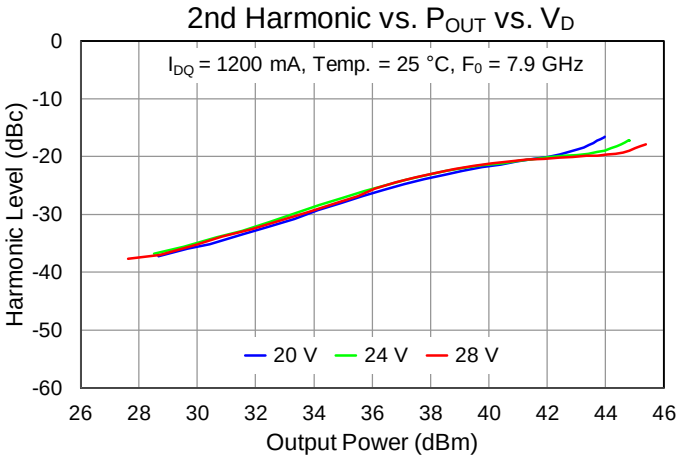
Performance Plots – Linearity

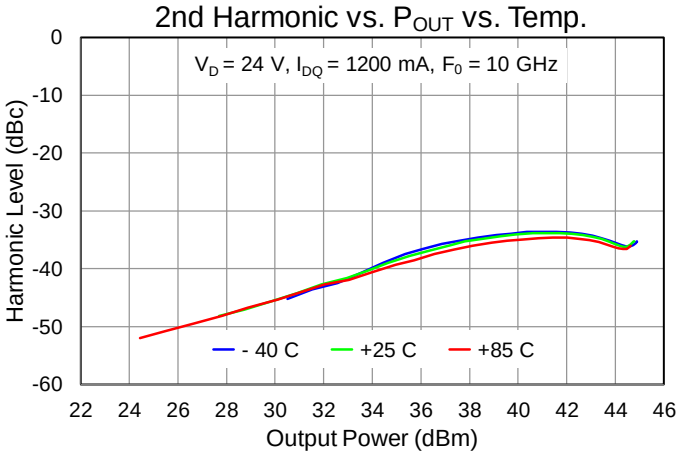


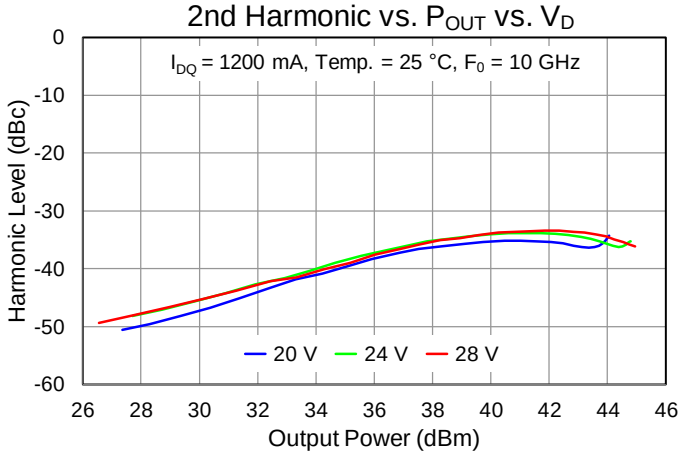


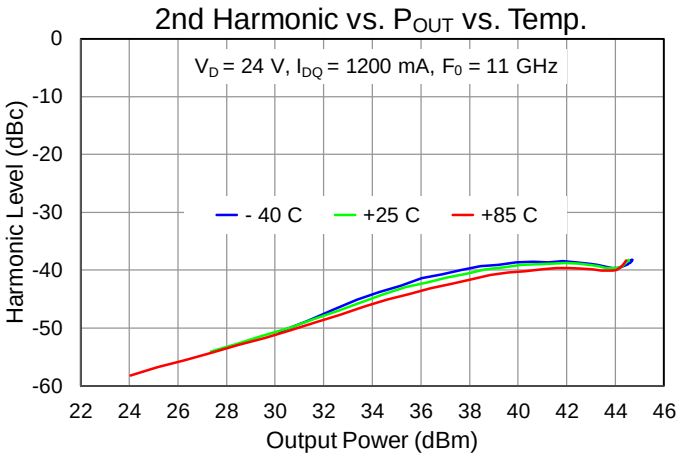
Performance Plots – Harmonics

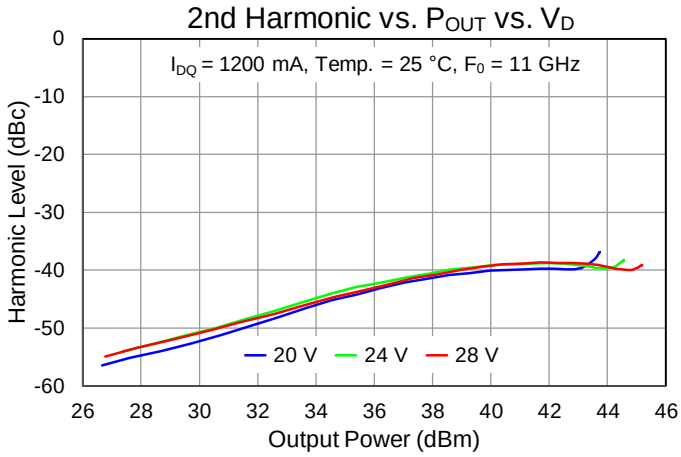






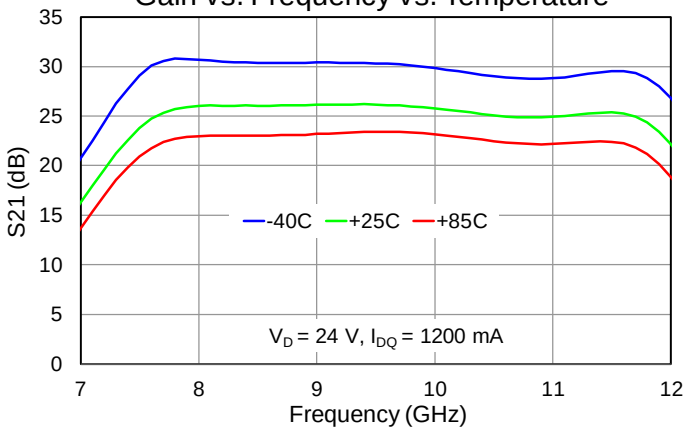




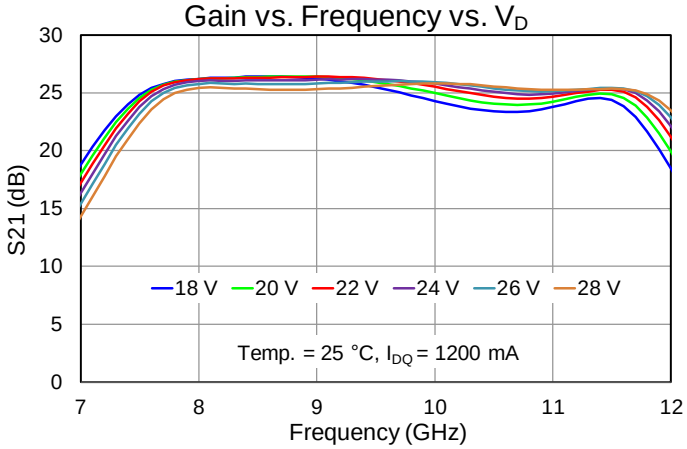


Performance Plots – Small Signal

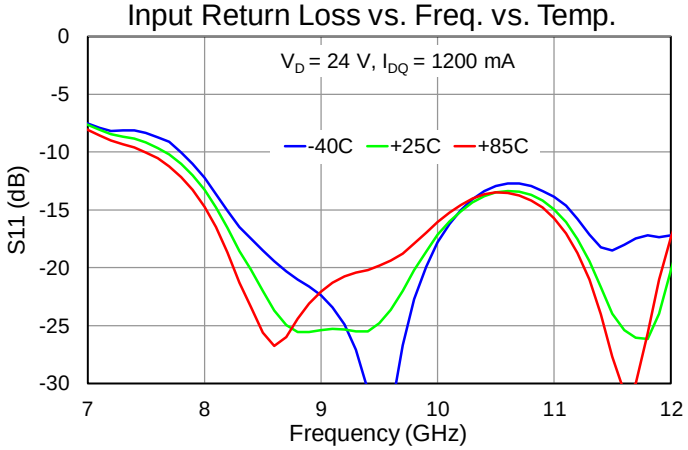
Gain vs. Frequency vs. Temperature



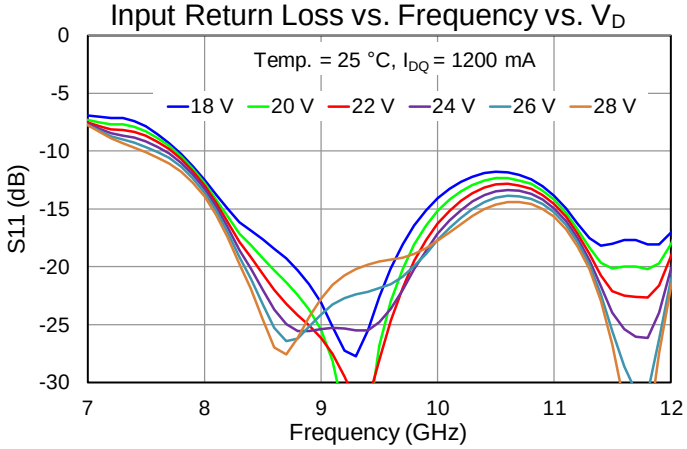
Gain vs. Frequency vs. V_D



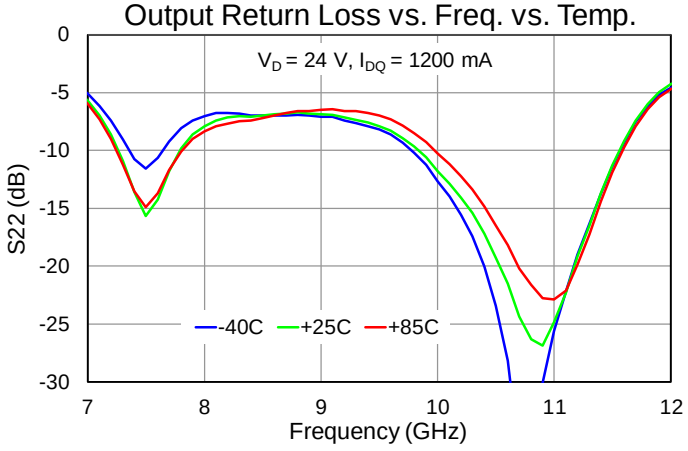
Input Return Loss vs. Freq. vs. Temp.



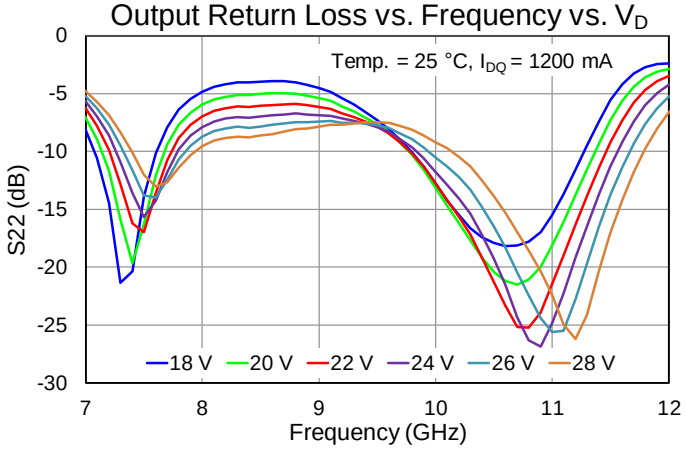
Input Return Loss vs. Frequency vs. V_D



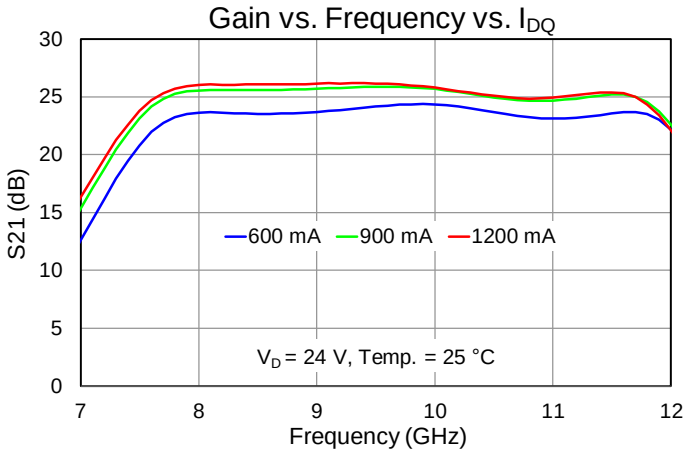
Output Return Loss vs. Freq. vs. Temp.

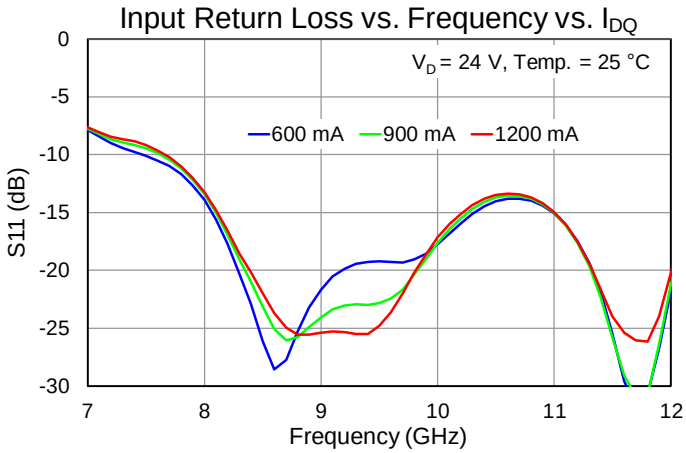


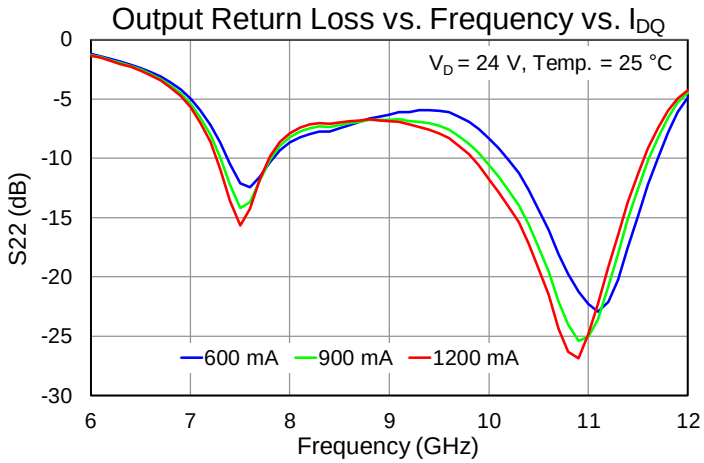
Output Return Loss vs. Frequency vs. V_D



Performance Plots – Small Signal







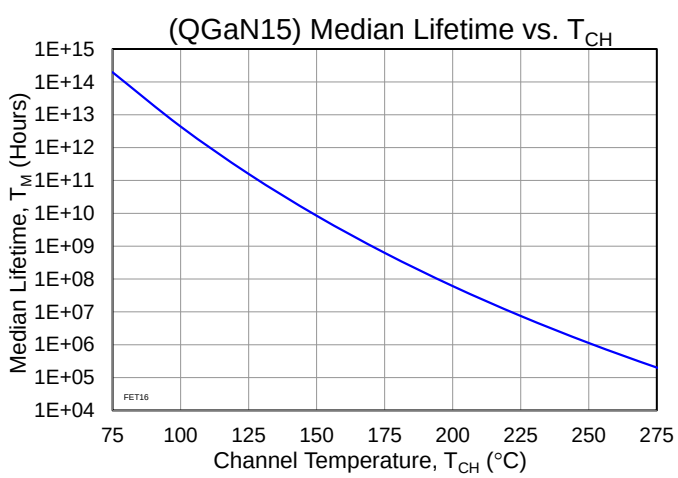
Thermal and Reliability Information

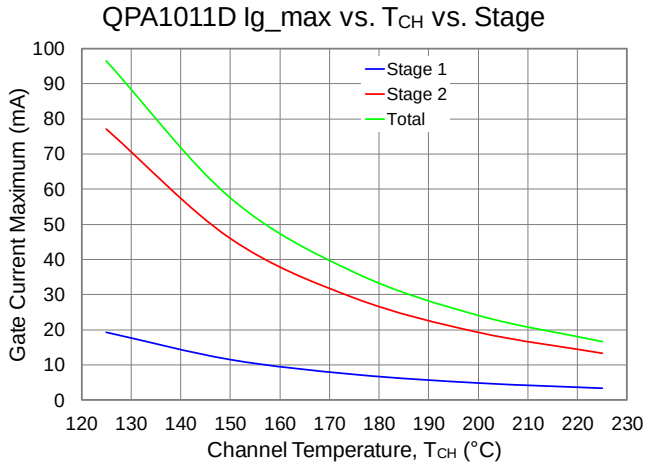
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +24 V, I_{DQ} = 1200 mA, Pulsed V_D: PW = 100 us; DC = 10%, Freq = 9.75 GHz, P_{IN} = 25 dBm, I_{D_Drive} = 3.6 A, P_{OUT} = 44.9 dBm, P_{DISS} = 53 W	1.56	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		168	°C
Median Lifetime (T_M)		1.3E +09	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = +24V, I_{DQ} = 1200 mA, CW, P_{DISS} = 28.8 W	2.78	°C/W
Channel Temperature (T_{CH}) (Quiescent, No RF)		165	°C
Median Lifetime (T_M)		1.7E 09	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +24 V, I_{DQ} = 1200 mA, CW, Freq = 9.75 GHz, P_{IN} = 25 dBm, I_{D_Drive} = 3 A, P_{OUT} = 43.6 dBm, P_{DISS} = 50 W	2.88	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		229	°C
Median Lifetime (T_M)		5.5E +06	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +20 V, I_{DQ} = 1200 mA, Pulsed V_D: PW = 100 us; DC = 10%, Freq = 9.75 GHz, P_{IN} = 25 dBm, I_{D_Drive} = 3.3 A, P_{OUT} = 44.2 dBm, P_{DISS} = 37.3 W	1.44	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		139	°C
Median Lifetime (T_M)		2.9E +10	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = +20V, I_{DQ} = 1200 mA, CW, P_{DISS} = 24 W	2.71	°C/W
Channel Temperature (T_{CH}) (Quiescent, No RF)		150	°C
Median Lifetime (T_M)		8.5E +09	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +20 V, I_{DQ} = 1200 mA, CW, Freq = 9.75 GHz, P_{IN} = 25 dBm, I_{D_Drive} = 3 A, P_{OUT} = 43.4 dBm, P_{DISS} = 38 W	2.58	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		183	°C
Median Lifetime (T_M)		2.9E +08	Hrs

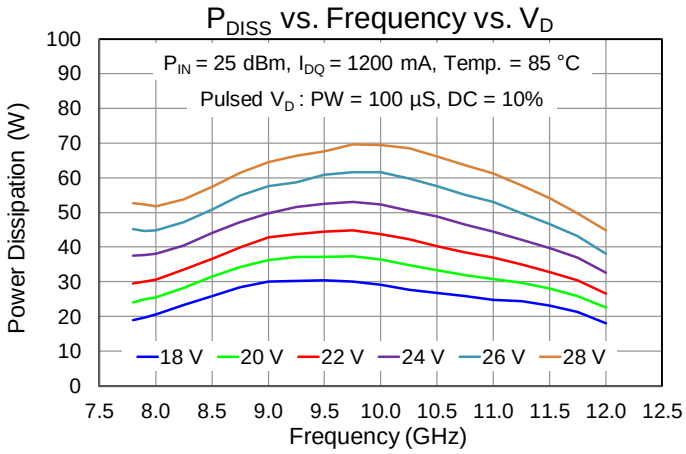
Notes:
1. Thermal resistance measured to back of carrier plate slug. MMIC mounted to 20 mil CuMo using AuSn eutectic.

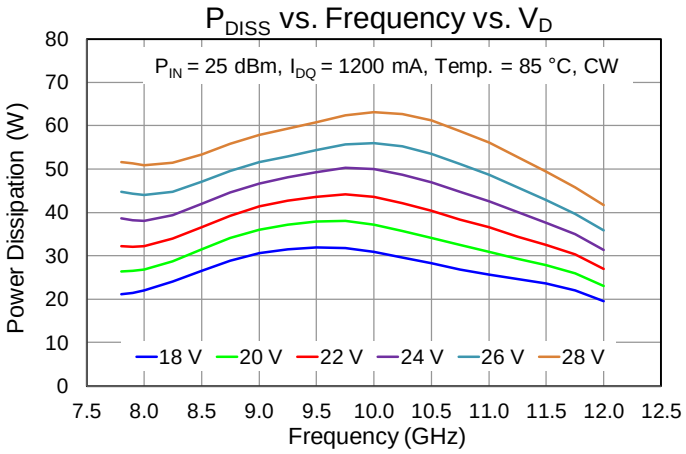
Median Lifetime

Median Life Test Conditions: V_D = +28 V; Failure Criteria = 10 % reduction in I_{D_MAX} during DC Life Testing

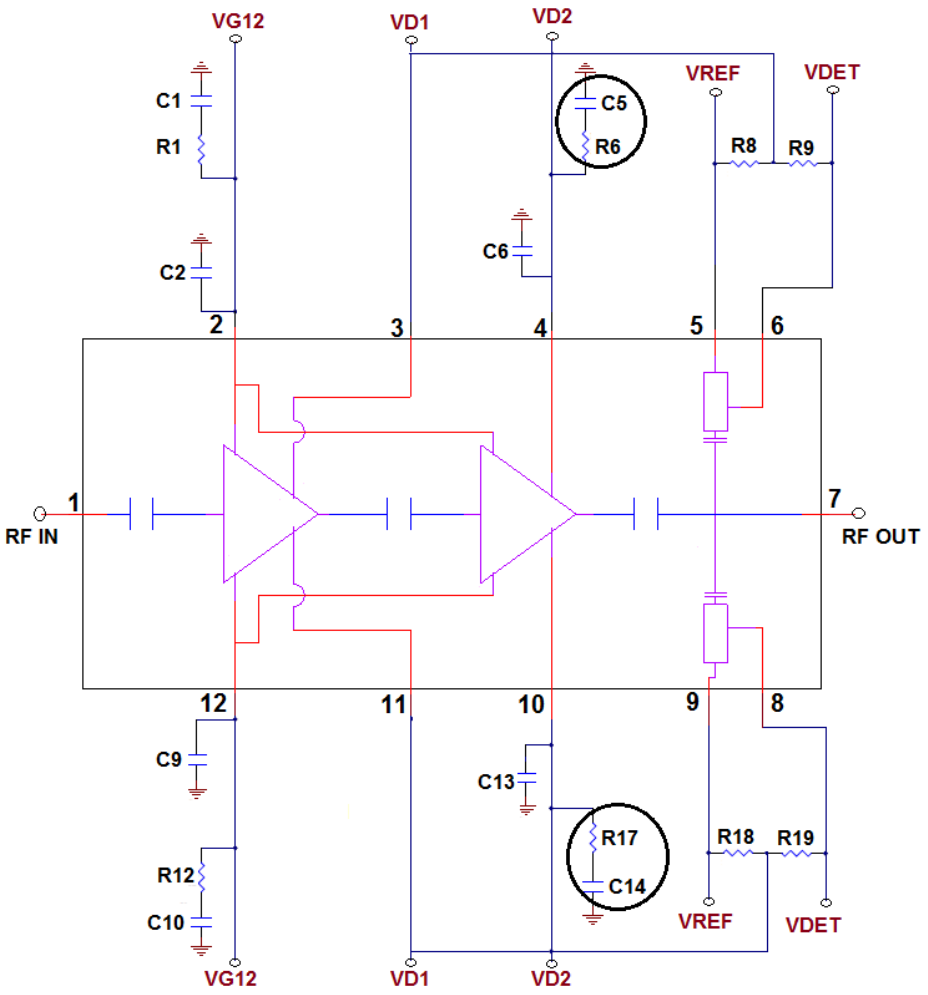








Applications Circuit for Linear and Pulsed Operations



Note: $V_{DELTA} = V_{REF} - V_{DET}$

- QPA1011D can be biased from either the top side or bottom side.
- V_{D1} and V_{D2} need to be tied together
- V_{D1} / V_{D2} and V_{REF} / V_{DET} have to be on the same side for V_{DELTA} to work.
- Bypassing components required for the side(s) being biased.
- The extra bias components (R6, R17, C5 and C14) are required for optimum linearity.

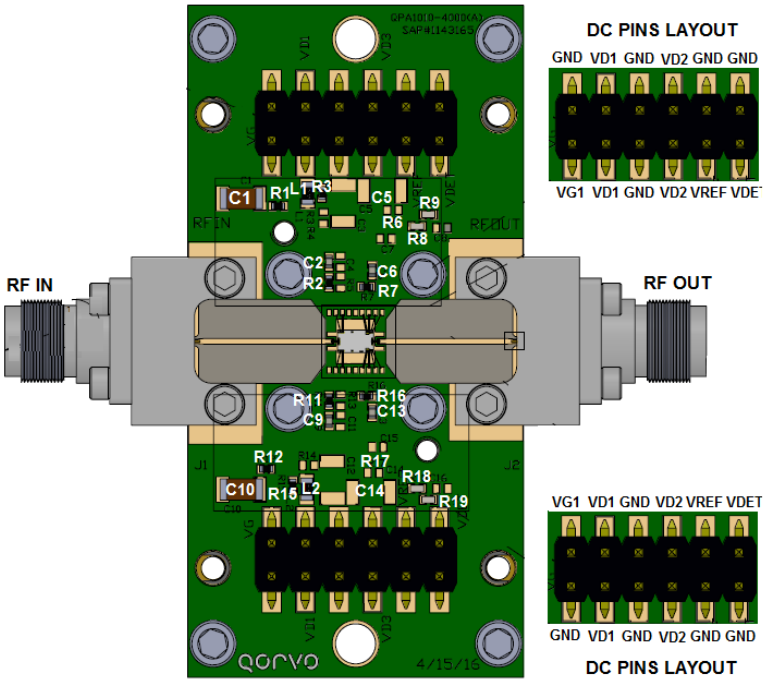
Bias Up Procedure

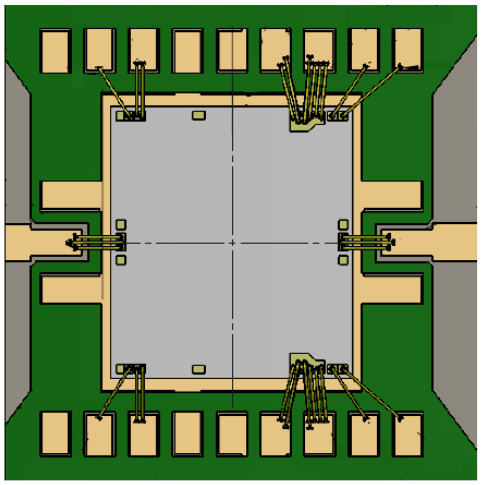
1. Set I_D limit to 4000 mA, I_G limit to 20 mA
2. Apply −5 V to V_G
3. Apply +24 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 1200 mA (V_G ~ −2.0 V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly for Pulsed Operation





MOUNTING DETAIL

Note: PCB is a multilayer

1. All 4 metal thicknesses are 0.5 oz
2. Upper core 1 is Rogers 4003C, 8 mil thick
3. Lower core 2 is 370HR, 6 mil thick
4. Pre-Preg is an epoxy coated glass fabric
5. Total finished PCB thickness is 25 ±3 mil
6. This EVB uses a copper-coined PCB for optimum thermal management under high dissipation long pulse and/or CW conditions

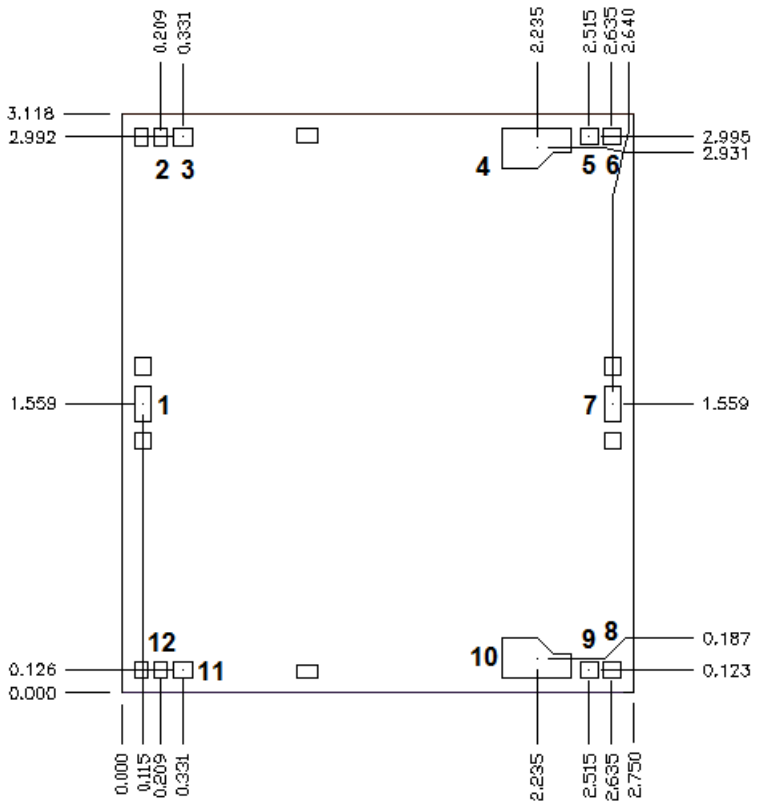
Bill of Materials for EVB

Reference Des.	Value	Description	Manuf.	Part Number
C1, C5, C10, C14	10 uF	CAP, 1206, 50 V, 20 %, X5R	Various	–
C2, C6, C9, C13	0.01 uF	CAP, 0402, 50 V, 10 %, X7R	Various	–
R1, R12	5.1 Ohm	RES, 0402, 50V, 5 %, SMT	Various	–
R2, R3, R6, R7, R11, R15, R16, R17 (1)	0 Ohm	RES, 0402, 5 %, SMD	Various	–
R8, R9, R18, R19	25.5 K Ohm	RES, 0402, 1/16W, 1%, 0402	Various	–
L1, L2 (1)	0 Ohm	RES, 0603, 1/10 W	Various	–

Note:

1. These components are acting as the jumpers for this EVB.

Mechanical Information



Units: millimeters
Thickness: 0.10
Die x,y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF IN	0.090 x 0.190	RF Input; matched to 50 Ω, DC blocked
2, 12	V_{G12}	0.074 x 0.091	Gate voltage for stage 1 & 2, bias network is required; see Application Circuit on page 22 as an example.
3, 11	V_{D1}	0.111 x 0.091	Drain voltage for stage 1, bias network is required; see Application Circuit on page 22 as an example.
4, 10	V_{D2}	0.374 x 0.212	Drain voltage for stage 2, bias network is required; see Application Circuit on page 22 as an example.
5, 9	V_{REF}	0.091 x 0.086	Reference voltage for Power detector
6, 8	V_{DET}	0.091 x 0.086	Power detector voltage
7	RF OUT	0.090 x 0.190	RF Output; matched to 50 Ω, DC blocked

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ESDA / JEDEC JS-001-2012

Caution!
ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qorvo Green

Contact Information

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